

# IBIS-AMI Channel Simulations Made Simple through WEBENCH Interface Designer



Guilherme Borba

High-speed serial-link simulations are powerful tools for signal-integrity engineers. These simulations give designers a glimpse of system performance prediction, allowing them to more easily make good decisions to meet design goals before committing a design to expensive board fabrication.

TI's [WEBENCH® Interface Designer](#) offers a simple yet powerful environment for serial-link simulations. This free Web-based tool serves as a quick and easy-to-use first step in high-speed channel analysis – a supplement to the more rigorous and time-consuming analyses traditionally performed by licensed electronic design automation (EDA) software tools. You can read more about WEBENCH Interface Designer in [this blog post](#).

This all sounds great, but will the tool give you reliable results? To answer this question, I went to the lab and made some measurements. I decided to use a 12.5 Gbps linear redriver [DS125BR820EVM](#), some FR4 printed circuit board (PCB) traces and breakout boards with SMA connectors for a back-plane sub-system. [Figure 1](#) illustrates my simple setup. A bit error rate tester (BERT) acts as the transmitter as well as the receiver for this study.

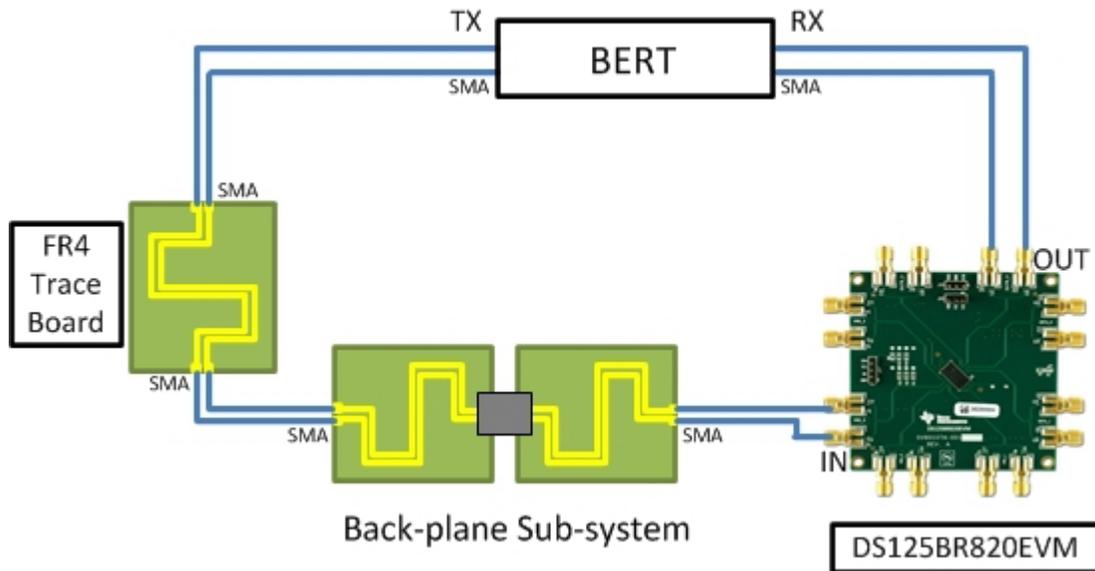


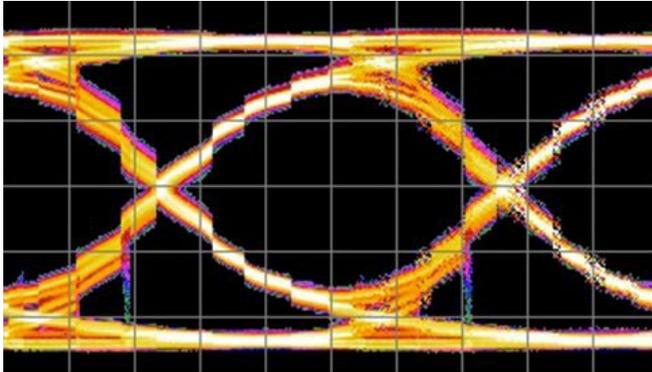
Figure 1. Lab Measurement Setup

First, I measured the S-parameters of all the cables, connectors and board trace using a four-port network analyzer and saved them to be used as channel models. I then cascaded these files to create combined models for a pre-channel (anything before the device) and a post-channel (anything after the device) for uploading into WEBENCH Interface Designer. The input/output buffer information specification-algorithmic modeling interface (IBIS-AMI) model of the [DS125BR820](#) is accessible from the tool, so the last thing to do is set up the transmitter. I used a generic IBIS-AMI transmitter model and matched the edge rates and differential-output voltage as closely as possible to the BERT. Now that my WEBENCH environment replicates my lab bench, I can run simulations for several different settings and see how well they match. Another neat thing about WEBENCH Interface Designer is that it processes the simulations remotely, so I can run them on my notebook computer in the lab without having to worry about processing power.

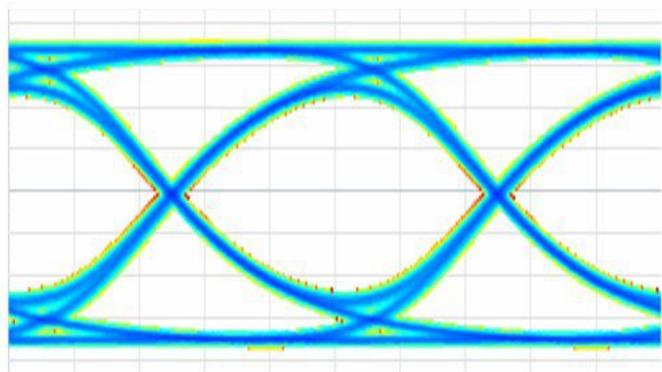
Two cases were used in this study. Case 1 is the use of PCI Express Gen 3 at a data rate of 8Gbps. Case 2 is the use of SAS Gen3 at a data rate of 12Gbps.

The specifications for case 1 were:

- BERT output: 8Gbps, 800mVpp.
- Channels: ~10dB at 4GHz pre-channel, ~2dB at 4GHz post-channel.
- [DS125BR820](#) settings: Input equalizer level 3, output amplitude level 5.



Amplitude: 780 mVpp  
 Eye Width: 87.8% UI  
 Eye Height: 510 mV

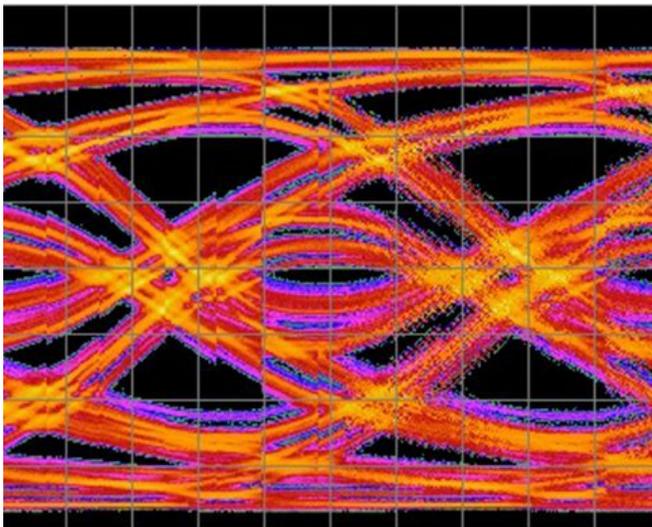


Amplitude: 720 mVpp  
 Eye Width: 84.4% UI  
 Eye Height: 470 mV

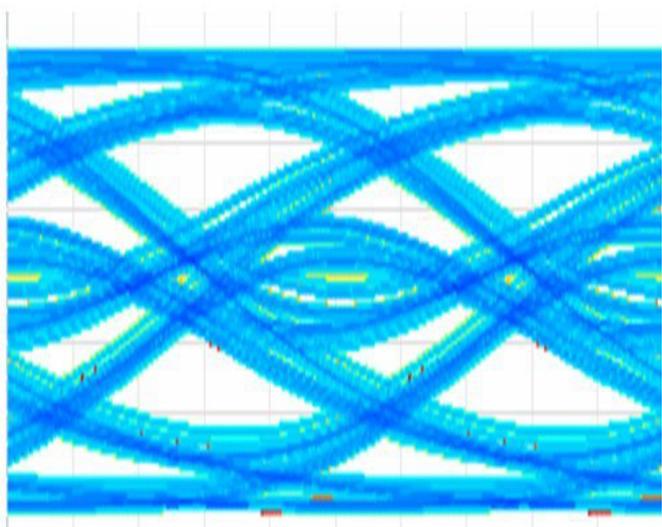
**Figure 2. Lab Data (Left) and WEBENCH Interface Designer Simulation Data (Right) for Case 1**

The specifications for case 2 were:

- BERT output: 12Gbps, 800mVpp.
- Channels: ~14dB at 6GHz pre-channel, ~3dB at 6GHz post-channel.
- [DS125BR820](#) settings: Input equalizer level 4, output amplitude level 7.



Amplitude: 760 mVpp  
 Eye Width: Closed  
 Eye Height: Closed



Amplitude: 700 mVpp  
 Eye Width: Closed  
 Eye Height: Closed

**Figure 3. Lab Data (Left) and WEBENCH Interface Designer Simulation Data (Right) for Case 2**

The [DS125BR820](#) opens the eye at the output of my system. Case 1, illustrated in [Figure 2](#), shows me that I have plenty of margins and can likely tolerate more channel loss while still maintaining an open eye. Case 2,

illustrated in [Figure 3](#), shows the opposite; my channel has too much loss and I am likely going to see bit errors at these operating conditions unless additional equalization is applied at the end of the channel.

If you do not have S-parameter measurements to upload like I did, you can simply type in the expected loss at a given frequency; WEBENCH Interface Designer will generate generic S-parameters that match your desired insertion loss.

Setting up and running a simulation like this takes about 30 minutes and produce reasonable well-matched result compared with laboratory measurements. The WEBENCH Interface Designer is a very useful web-based tool to help users to pick the right device based on their applications requirement. I hope you'll give it a try!

Let us know if you have any suggestions or comments on [WEBENCH Interface Designer](#) by logging in to post a comment below.

### Additional Resources

- Visit the [WEBENCH Design Center](#).
- Learn more about [TI's signal-conditioning portfolio](#).
- Read [other blog posts](#) about WEBENCH tools.

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