

# Accelerating the Fast Fourier Transform (FFT/iFFT) by 10x and More

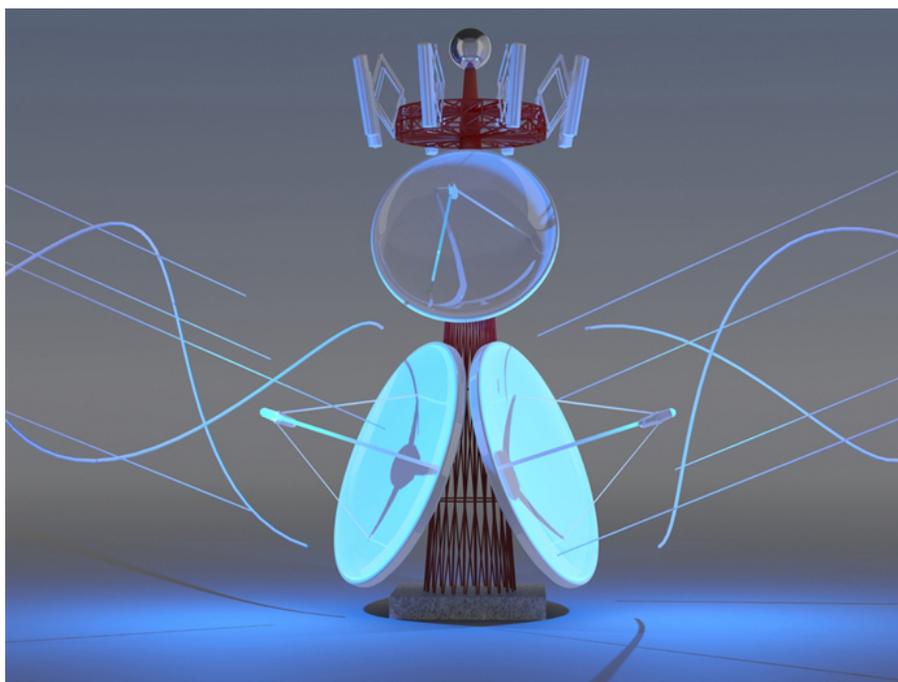


Snehaprabha Narnakaje

Arnon Friedmann

Fast Fourier transforms (FFTs) are a critical operation used in a wide range of complex systems today such as radar, communications, economics, video, music and more. Achieving acceleration for FFTs is about trading off the dynamic performance for the speed of processing. The dynamic range is a function of the precision of the calculation as well as the size of the FFT being performed. The table below shows the speed improvements of our FFT coprocessor (FFTC) that we have integrated onto a number of our processors. On the low-end of precision, it is common to see 16bit fixed point implementations (for smaller FFT lengths) and on the higher-end of precision we see double precision floating point implementations for FFT lengths as long as a billion points.

Performance metric	Processing core	FFT size			
		1024	2048	4096	8192
FFTs per second	FFT coprocessor	705,000	303,000	154,000	66,000
	C66x DSP core	74,000	35,000	9,000	4,000
SNR (dB)	FFT coprocessor	85.2	84.8	84.1	83.8
	C66x DSP core	~300	~300	~300	~300
Equivalent GFlops	FFT coprocessor	36.1	34.1	37.8	35.4
	C66x DSP core	4.5	4.2	4.5	2.5



As shown in the preceding table, the speedup is quite dramatic, with the FFTC providing 10x-15x improvements over the DSP cores. Also shown in the table, the SNR for the FFTC is ~85dB vs. the ~300dB of precision for the digital signal processor (DSP). On the DSP, we have a single precision floating point implementation. On the

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other hand, the FFTC uses a block floating point algorithm that gives about 20dB better performance than a fixed point implementation and are sufficient for many applications, such as radar.

We studied the impact of the precision on synthetic aperture radar (SAR) and compared results using the FFTC to results using the DSP cores. The comparison shows that the FFTC performs as well as the DSP cores using full precision for the SAR application. Details of the study can be found in the white paper: [Optimizing Modern Radar Systems using Low-Latency, High-Performance FFT Coprocessors](#).

Here we see one example of how an FFT coprocessor can be used in place of programmable cores (such as ARM® or DSPs) to accelerate the overall system. Leveraging the FFTC engine(s) can provide meaningful system performance lift in systems where the SNR performance of the FFTC engine meets the application requirements. To learn more:

**Devices with FFTC:**

- [66AK2L06](#)

**TI Designs for Radar:**

- [Optimized Radar System Design Using a DSP + ARM SoC](#)
- [Implementing a Real-time Synthetic Aperture Radar \(SAR\) Algorithm on TI's C6678 DSP](#)

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