Technical Article

Preparing for 5G Applications: Sync Your Multichannel JESD204B Data Acquisition Systems up to 15 GHz

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TIDA-01022 Most advanced systems like digital oscilloscopes (DSOs), phased-array radars and 5G wireless testers require multiple synchronized signal chains that include high-speed (gigasamples per second) analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). The JESD204B interface simplifies the process for synchronizing multichannel systems using phase-synchronized device clocks and the system reference (SYSREF) for data converters (ADCs and DACs) and field-programmable gate arrays (FPGAs). TI's new reference design, the Multichannel JESD204B 15GHz Clocking Reference Design for DSOs, Radars and 5G Wireless Testers, describes the requirements, setup and system performance of the entire analog signal chain.

The clocking reference design uses TI's latest wideband phase-locked loop (PLL) with an integrated voltage-controlled oscillator LMX2594 and jitter cleaner LMK04828. This design generates multichannel, high-performance (low-phase-noise) clocks using the combination of the LMX2594 and LMK61E2 programmable oscillator.

The design has several advantages for multichannel systems:

- JESD204B-complaint two-channel device clocks up to 15GHz
- The multichannel clock time skew is less than 10ps, as shown in Figure 1.
- The designed clocking board can interface with existing TI high-speed ADC and DAC evaluation modules (EVMs) using an FPGA mezzanine card (FMC) adapter board.

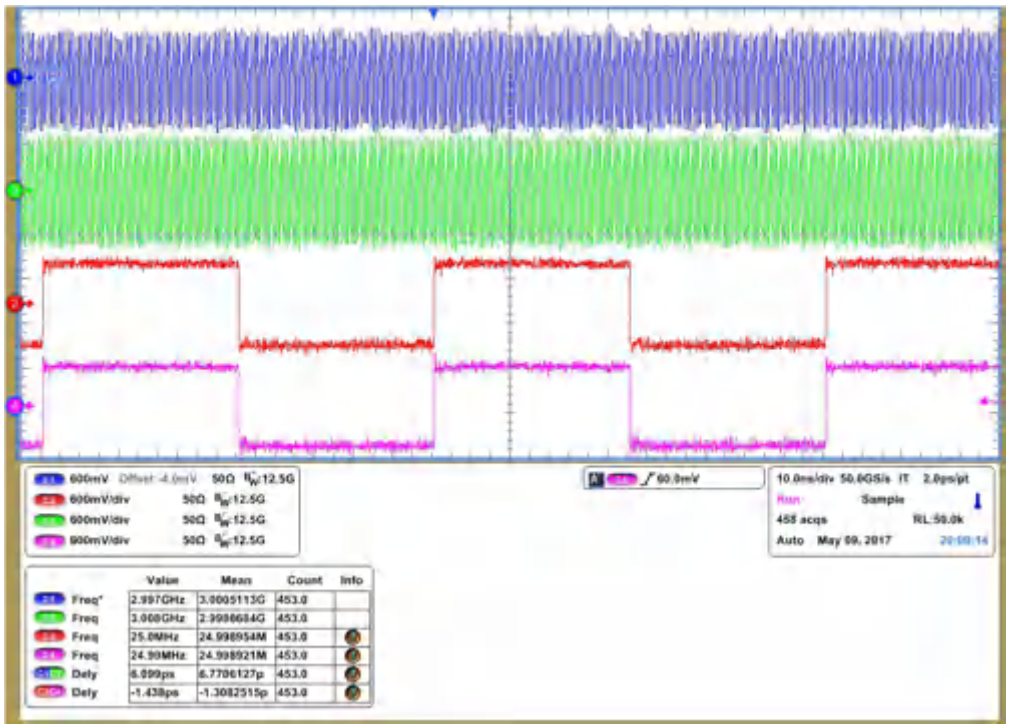

Figure 1. Measured Multichannel Clock Skew at 3GHz

The clocking reference design also demonstrates an accurate and time-stable synchronization system when paired with the 12-bit wideband ADC12DJ3200 running at a 2.7GSPS sampling frequency. In the "Get Your Clocks in Sync" hardware set up video, the onboard clocks of the ADC12DJ3200EVM are replaced with reference design-generated clocks, shown in Figure 2. Figure 3 shows the measured channel-to-channel skew.

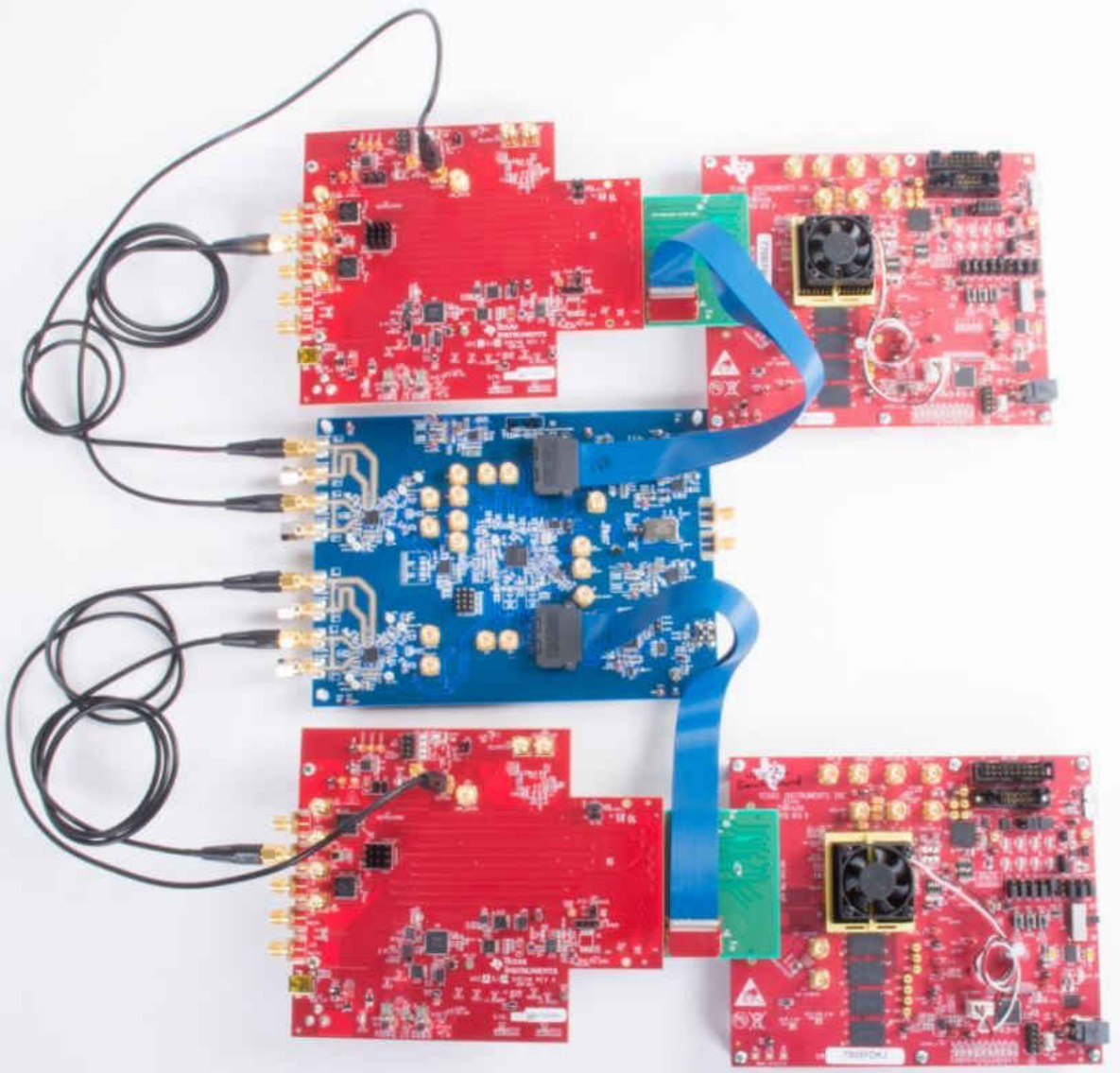

Figure 2. Channel-to-channel Skew Measurement Setup

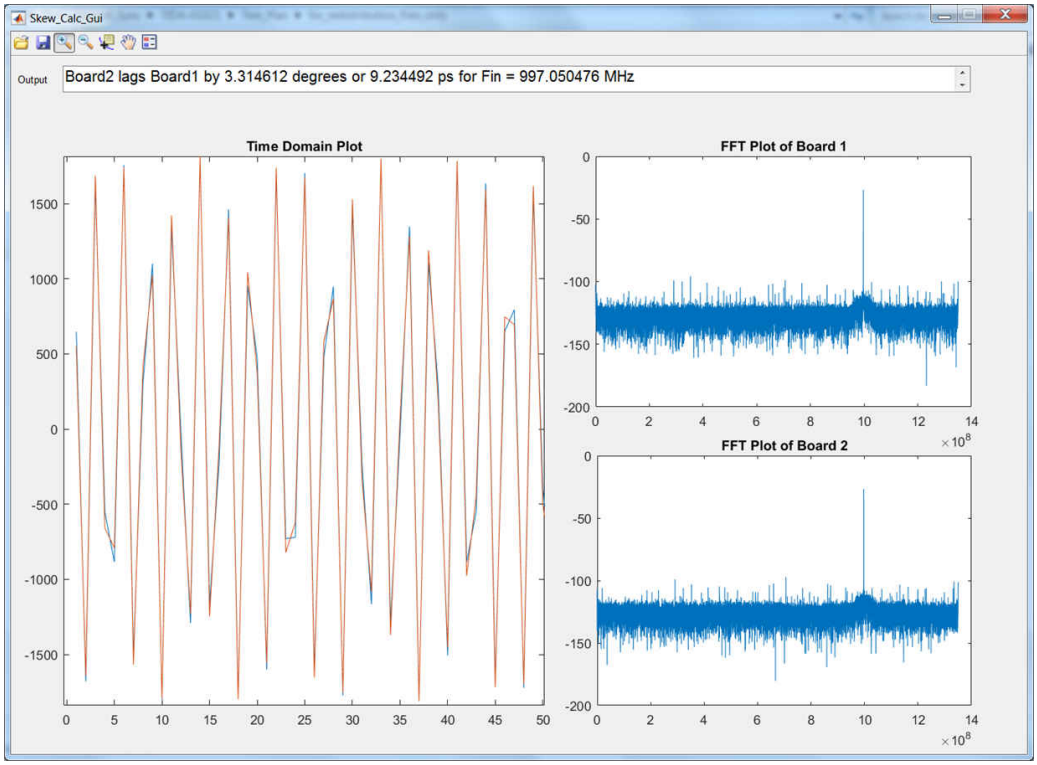

Figure 3. Measured Channel-to-channel Skew and Spectrum from Both Channels

The clocking reference design features high-performance, multichannel JESD204B clocks with better phase noise that you can use in low deterministic latency, multichannel systems. When configuring the reference design clocks along with ADC12DJ3200 EVMs for multichannel operation, it's possible to achieve channel-to-channel skew greater than 10ps and a signal-to-noise ratio greater than 54dBFs at a 997MHz input signal.

Additional Resources:

- Learn more about the Multi-Channel JESD204B 15 GHz Clocking Reference Design for DSO, Radar and 5G Wireless Testers
- Learn how to sync your JESD204B data converters with a tree structure for clocking
- Learn how to sync your JESD204B data converters by daisy-chaining your clocking
- Learn by example with the Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems
- Read this Analog Applications Journal to learn more
- Watch this video to learn how to assemble this reference design

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