Technical Article

Analog Interfacing for Grid Infrastructure with Sitara Processors

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Electrical grid systems are always trying to mitigate the risk of overcurrent events that can disrupt the flow of power from a power-generation source to millions of homes and businesses. To measure currents and voltages accurately, energy providers use equipment to monitor different parts of the power grid.

One of the most critical pieces of grid equipment is the protection relay. A relay can monitor several current transformers and potential transformers at the same time. When the relay detects unusual behavior, it activates a circuit breaker to prevent damage to the grid network. A protection relay system typically includes subsystems for measuring current or voltage, communicating information back to a substation control room and displaying information on the actual relay device.

Older relay devices relied heavily on analog circuitry to detect overcurrent events, but modern digital processors are capable of detecting events quickly and accurately, and can use up less space. One way to implement a current-measuring subsystem is by using the programmable real-time unit-industrial communication subsystem (PRU-ICSS) in TI Arm®-based Sitara™ processors, as shown in Figure 1.

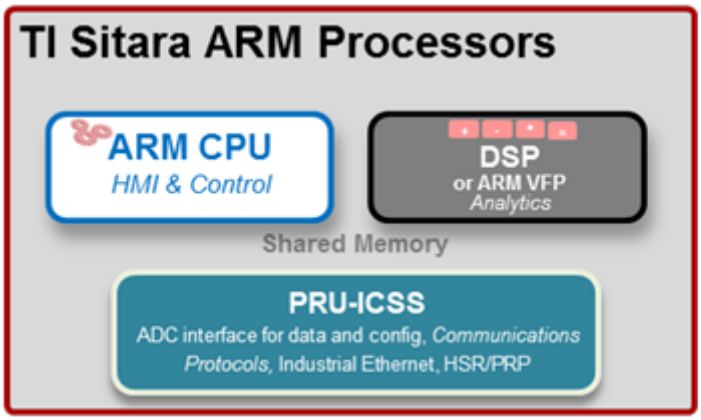

Figure 1. Overview of Sitara Processor with Arm Cores

The PRU-ICSS subsystem consists of two 32-bit reduced instruction set computer (RISC) cores designed for real-time processing, and enables additional general-purpose inputs and outputs. As an example, TI created the Flexible Interface (PRU-ICSS) Reference Design for Simultaneous, Coherent DAQ Using Multiple ADCs, which uses the PRU-ICSS to measure the output of six 8-channel ADS8688 analog-to-digital converters (ADCs) with a BeagleBone Black. Data from the ADCs are fed into the PRU-ICSS through general-purpose input pins; each PRU core then performs additional filtering functions, as shown in Figure 2.

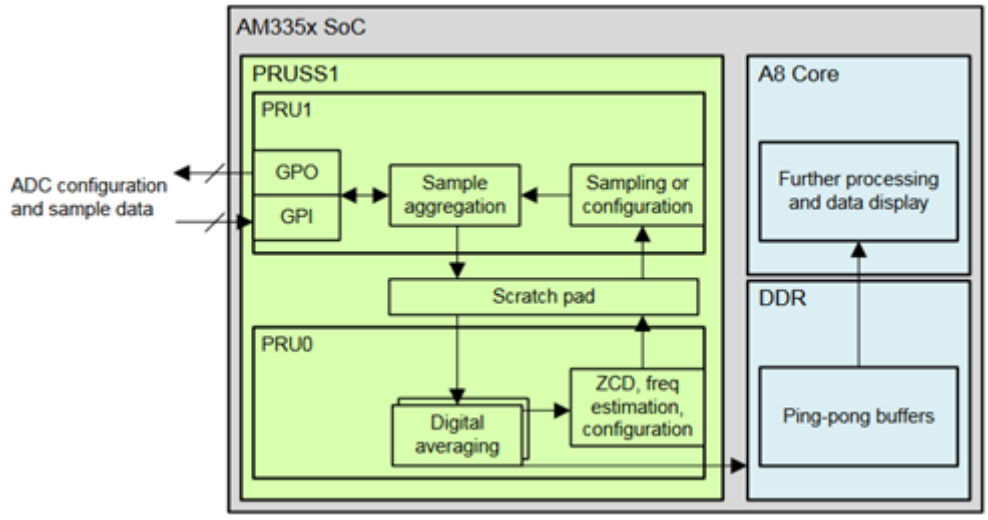

Figure 2. PRU-ICSS Processing of ADC Data

Using a PRU-ICSS has several advantages over a dedicated hardware Serial Peripheral Interface (SPI) peripheral. First, you can reconfigure the PRU-ICSS pins to connect to a variety of devices, whereas an SPI interface cannot. Second, the PRU-ICSS can run independently of the host processor to reduce processor loading where an SPI interface will send interrupt commands to the processor. Processing the data with a dedicated PRU-ICSS subsystem also enables faster ADC sampling speeds, since there are no longer competing actions for the host processor. Third, the PRU-ICSS can compensate for delayed clock edges, whereas SPI peripherals require tight control over timing requirements.

The AM335x processor family used in the reference design is limited to only one PRU-ICSS, but a processor family like AM57x devices has two. Now it becomes possible to have an analog monitoring subsystem, a communications subsystem for redundancy protocols and a human machine interface (HMI) like that shown in Figure 3.

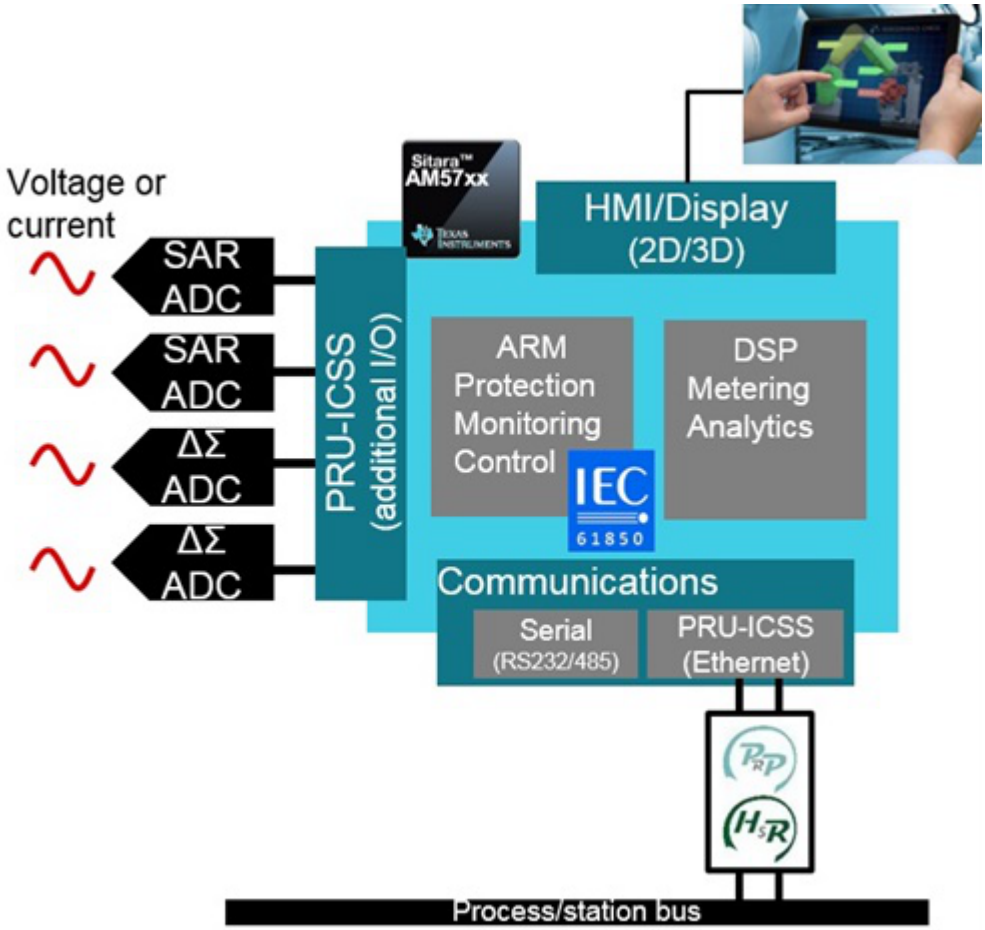

Figure 3. Example of a Protection Relay Based on the AM57xx Processor

The Sitara portfolio includes a wide range of devices for hardware scalability, but also enables software reuse with the Processor SDK for a common development framework. This flexible hardware and software platform can enable customers to design a wide range of protection relays for a smarter grid infrastructure.

Additional Resources

- Download these reference designs:
  - "Human Machine Interface (HMI) for Protection Relay Reference Design."
  - "High-Availability Seamless Redundancy Ethernet Reference Design for Substation Automation for Linux."
  - "Parallel Redundancy Protocol Ethernet Reference Design for Substation Automation on Linux."
- Learn more about Sitara processors for grid infrastructure.

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