Technical Article

Finding the Right Pixel Clock Frequency and Throughput for an LVDS Display Resolution

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Low voltage differential signaling (LVDS, also known as OpenLDI*)* thin-film transistor (TFT) liquid crystal (LCD) displays typically have a specified resolution and minimum required clock frequency to meet desired resolution. Normally, you will find this information listed in the display data sheet and won't need to perform any calculations.

However, if you do not yet have access to your display data sheet and only know what resolution you want your system to support, you can estimate what clock frequency you need and determine which serializer/deserializer (SerDes) is appropriate for your application.

Pixel Clock Frequency

Equation 1 calculates pixel clock frequency as:

$$\text{Pixel Clock} = \text{HActive} \times \text{VActive} \times \text{Frame Rate} \times (1 + \%\text{Blanking}) \quad (1)$$

Let's define each parameter of this equation.

- **HActive x VActive: R**epresents the display resolution. For example, in a 1920 x 1080 resolution display, HActive = 1920 and VActive = 1080.
- **%Blanking:** The blanking period, or the percentage of time when active video is not being displayed. As shown in Figure 1, it is represented horizontally as horizontal pulse width (HPW), horizontal back porch (HBP) and horizontal front porch (HFP). It is also represented vertically as vertical pulse width (VPW), vertical back porch (VBP) and vertical front porch (VFP).

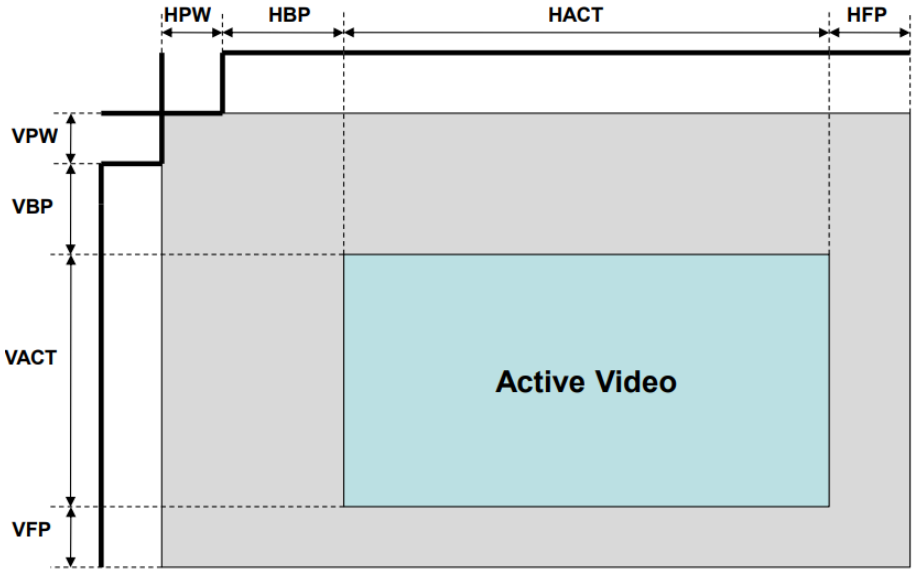

Figure 1. Video Format Parameters

The values for these blanking parameters are listed in display data sheets. The total blanking period varies from 3% to 39%. If your system uses reduced blanking, then you can estimate %Blanking at 10%. If you are not sure what blanking period your system uses, estimate around 20% and above to be conservative.

- **Frame rate (or refresh rate):** the frequency at which consecutive images (frames) are displayed, and is measured in hertz or frames per second (fps). 60Hz is the most common frame rate, but this value can vary from 24Hz to 70Hz.

Throughput

Throughput is another metric that you can use to determine whether or not a device will support your desired display resolution. The throughput is the effective payload of video data, and is derived from the required pixel clock frequency and color depth of your system, as shown in Equation 2:

$$\text{Throughput} = \text{Pixel Clock} \times \text{Color Depth} \quad (2)$$

The remaining parameter to cover:

- **Color depth:** For a first-generation SerDes like the SN65LVDS93A, color depth is typically 24-bit red-green-blue (RGB) or 18-bit RGB for single pixel in, single pixel out (SISO) applications, and 48-bit RGB or 36-bit RGB for dual pixel in, dual pixel out (DIDO) applications.

The color depth will determine how many LVDS data lanes your display requires. SerDes serialize data at a rate of 7x the pixel clock frequency on each LVDS data lane. If the color depth is 24-bit RGB, then you will need four LVDS data lanes (there are an additional four bits used for control, which brings the total bit count to 28 bits) and can use a SerDes like the SN65LVDS93A. If the color depth is 18-bit RGB, then you will need three LVDS data lanes (there are an additional 3 bits used for control, which brings the total bit count to 21 bits) and can use a SerDes like the SN74LVDS84A or the SN65LVDS93A.

If the color depth is 48-bit RGB, then you will need eight LVDS data lanes (there are an additional 8 bits used for control, which brings the total bit count to 56 bits) and will need to use a device like the DS90C387 or DS90C189-Q1, which can output as many as eight LVDS data lanes.

When calculating the throughput for DIDO applications, you need to calculate the throughput for the odd pixels and even pixels separately and then add them together. For example, for a 48-bit DIDO application, the total required throughput would be 2 x Pixel Clock x 24.

Now that you have the necessary equations for pixel clock frequency and throughput, let's go through a couple of examples.

Example 1 - SISO Application

The first example is for a SISO application. Table 1 lists the parameters needed to calculate the pixel clock frequency and throughput.

Table 1. Design Parameters for SISO Application

Design parameters	Example value
HActive (pixels)	1280
VActive (lines)	800
Frame rate (Hz)	60
Blanking period (%)	36
Color depth	24 bit
Operating mode	SISO

Using Equation 1:

$$\text{Pixel Clock} = 1280 \times 800 \times 60 \times (1 + 0.36) = 8.356 \times 10^7 \text{Hz}$$

So the minimum pixel clock frequency to support a 1280 x 800 resolution display is 83.56MHz.

Using Equation 2:

$$\text{Throughput} = 83.56 \times 24 = 2005.44\text{Mbps}$$

So the total minimum required throughput is around 2005Mbps.

Since the color depth is 24-bit RGB, you will need four LVDS data lanes. The SN65LVDS93A is a good fit for this application, since it has a pixel clock frequency range of 10MHz to 135MHz. Additionally, the maximum throughput for each LVDS data lane on this device is 135 x 7 = 945Mbps. Because this device has four LVDS data lanes, the total maximum throughput is 945 x 4 = 3780Mbps, which is higher than the minimum required throughput.

Example 2 - DIDO Application

This example is for a DIDO application. Table 2 lists the parameters needed to calculate the pixel clock frequency and throughput.

Table 2. Design Parameters for DIDO Application

Design parameters	Example value
HActive (pixels)	2048
VActive (lines)	1536
Frame rate (Hz)	60
Blanking period (%)	10
Color depth	48 bit
Operating mode	DIDO

Using Equation 1:

$$\text{Pixel Clock} = 2048 \times 1536 \times 60 \times (1 + 0.1) = 2.08 \times 10^8\text{Hz}$$

So the minimum pixel clock frequency to support a 2048 x 1536 resolution display is 208MHz. However, since this is a 48-bit DIDO application, there are actually two clocks: the frequency is split between them. Each clock must have a frequency of at least 104MHz.

Using Equation 2, the minimum required throughput **for each channel** (one channel = four data lanes) is: **Throughput = 108 x 24 = 2496Mbps.**

So the total minimum required throughput is **2 x 2496 = 4992Mbps**.

Since the color depth is 48-bit RGB, you will need eight LVDS data lanes. The DS90C387 and DS90C187 are a good fit for this application, since they have a pixel clock frequency range of 32.5MHz to 112MHz (the DS90C387) and 25MHz to 105MHz (the DS90C187) for each channel in DIDO applications. Thus, if you don't have access to the display data sheet yet, you can still estimate the required pixel clock frequency and throughput to support your desired resolution. If the SerDes does not meet these parameters, data on the display may display incorrectly, or not display at all.

Leave a comment below if you would like to learn more about anything discussed here, or if there is an LVDS topic you would like to see in the future.

Additional Resources

- Get online support in the TI E2E™ Community Interface forum.
- Learn more about TI's portfolio of LVDS solutions.

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