Technical Article

No Avalanche? No Problem! GaN FETs Are Surge Robust

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We live in silicon-dominated world that shapes our thinking. I find it interesting to imagine an alternate universe where the gallium nitride (GaN) power field-effect transistor (FET) was developed before the silicon FET. Our power converters would certainly have been smaller and more efficient, but more importantly, we'd have been thinking differently.

Take for example the issue of avalanche rating. This parameter relates to the ability of silicon power FETs to survive power-line disturbances caused by lightning strikes or other abnormal occurrences.

The ability to survive a power-line surge is important for any power device. There is concern about the surge-robustness of present-day GaN FETs due to their lack of an avalanche rating. Many of us know Albert Einstein's quote, "We cannot solve our problems with the same thinking we used when we created them," and I believe this is good advice. The use of avalanche ratings for surge robustness arose because silicon power FETs do not typically possess much voltage headroom above their maximum voltage rating. When a power-line surge hits, the FET starts breaking down by impact-ionization phenomena, or "avalanche breakdown." Over the years, the industry engineered the FETs to do this robustly, and the avalanching property has become associated with power-line surge protection. If silicon FETs had been able to switch through surge events, then the thinking would have been different. So let's rethink surge robustness in a GaN-powered world.

A technical paper at the 2019 IEEE International Reliability Physics Symposium (IRPS) describes the validation of the TI LMG3410R070's surge robustness. GaN's superior transient overvoltage capability enables GaN FETs to switch through surge events without avalanching and provides an additional design parameter: a transient surge-voltage rating, $V_{DS(SURGE)}$, which is the peak bus voltage that the FETs can withstand during active operation. A good value was determined to be 720 V, both from customer feedback and through system-level simulation.

Figure 1 illustrates the $V_{DS(SURGE)}$ definition, in coordination with the $V_{DS(TR)}$ parameter already in use on some data sheets. Using these parameters, you can easily limit the peak bus voltage at the device to 720 V during a surge event, as demonstrated in the IRPS paper.

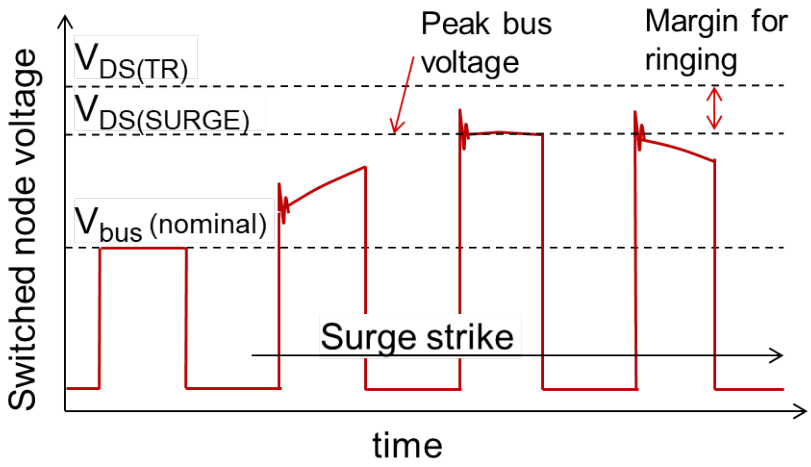

Figure 1. The surge rating parameter, $V_{DS(SURGE)}$, is the peak bus FET withstand voltage during operation when a surge strikes. Some GaN data sheets already have an off-state transient overvoltage parameter, $V_{DS(TR)}$, that serves to provide additional margin for ringing.

Figure 2 shows the switching of the LMG3410R070 through a surge strike, with the validation circuit in the inset. The circuit is powering a 1-kW load under regular operating conditions. The surge generator provides an International Electrotechnical Commission (IEC) 61000-4-5 industry-standard surge waveform, and is set so that the bus voltage at the GaN FETs surges to a peak of 720 V. The input and switched-node waveforms are overlaid to show the GaN FETs actively switching through the strike; switching at 720 V. The test consisted of 50 such strikes per the Verband der Elektrotechnik (VDE) 0884-11 standard while actively powering the load. There was no loss of efficiency, and neither the high- nor low-side GaN FET showed hard failure, demonstrating that they are surge-robust in power supplies.

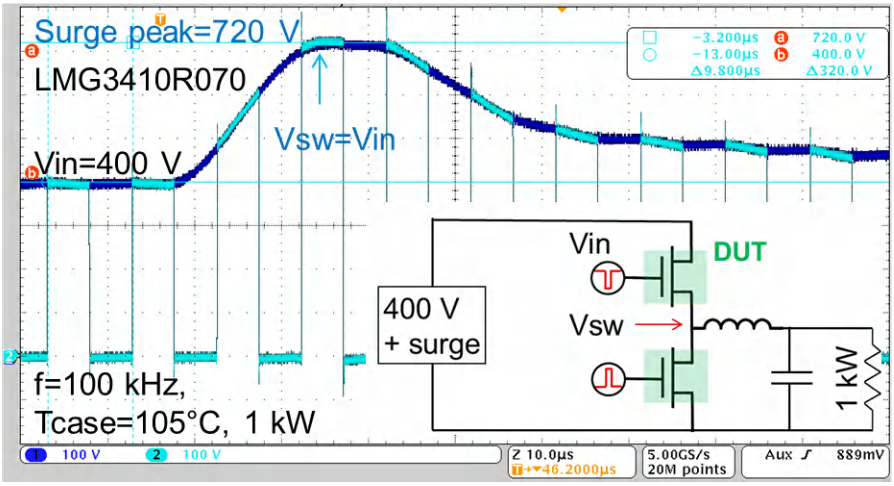

Figure 2. Demonstration of the Surge Robustness of the LMG3410R070. the Input Bus Voltage Surges from the Operating Point of 400 v to the Target Specification of 720 v When the Active Circuit (Inset) Is Struck with a Surge Waveform Conforming to the IEC 61000-4-5 Standard. the Switched-node Waveform Is Overlaid on the Input Waveform to Show That the GaN FETs Successfully Switch through a 720-v Peak Bus Voltage Surge.

At TI, we take all aspects of GaN reliability seriously. TI has leveraged its many decades of silicon technology development – while recognizing the new opportunities that GaN brings – to think differently on how to deliver a robust and reliable power solution. Hard-switching the GaN FET in the early stages of technology development is critical, as described in the white paper, "A comprehensive methodology to qualify the reliability of GaN products." Our recognition of the need for the industry to collaborate, as explored in the blog, "Let's GaN together, reliably," led us to help form the Joint Electron Device Engineering Council JC70 committee on wide-bandgap semiconductors. We have invested 20 million device hours in the reliability testing of GaN, including surge robustness.

I would love to imagine how the industry would react to a newly invented silicon power MOSFET in a GaN universe: "A silicon power MOSFET does not switch through surge – *it avalanches?*"

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