*Technical Article*

# *How to Choose the Right Power MOSFET or Power Block Package for Your Application*

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When starting a new design, engineers are often overwhelmed by the number of package options for power metal-oxide semiconductor field-effect transistors (MOSFETs) and power blocks. For example, TI offers single N-channel MOSFETs in 12 unique packages. Given this myriad of options, how do you know which package to select for your application?

There are many considerations when choosing a component package, including through-hole vs. surface mount, size, cost, lead spacing and thermal capability. In this technical article, I'd like to focus on package thermal capability and provide some rules of thumb for power dissipation in TI MOSFET and power block packages. I hope that you'll find these rules helpful, because power dissipation determines the smallest package possible in a given application.

### Start by looking at the data sheet

All power MOSFET and power block data sheets include thermal impedance specifications in the thermal information table. Figure 1 shows an example of thermal impedance specifications for the CSD17581Q5A.

## Absolute Maximum Ratings

| $T_A$ = 25°C | | VALUE | UNIT |
|---|---|---|---|
| $V_{DS}$ | Drain-to-Source Voltage | 30 | V |
| $V_{GS}$ | Gate-to-Source Voltage | ±20 | V |
| $I_D$ | Continuous Drain Current (Package Limited) | 60 | A |
| | Continuous Drain Current (Silicon Limited), $T_C$ = 25°C | 123 | |
| | Continuous Drain Current(1) | 24 | |
| $I_{DM}$ | Pulsed Drain Current(2) | 256 | A |
| $P_D$ | Power Dissipation(1) | 3.1 | W |
| | Power Dissipation, $T_C$ = 25°C | 83 | |
| $T_J$, $T_{stg}$ | Operating Junction Temperature, Storage Temperature | –55 to 150 | °C |
| $E_{AS}$ | Avalanche Energy, Single Pulse $I_D$ = 39 A, L = 0.1 mH, $R_G$ = 25 Ω | 76 | mJ |

(1) Typical $R_{\theta JA}$ = 40°C/W on a 1-in$^2$, 2-oz Cu pad on a 0.06-in thick FR4 PCB.

(2) Max $R_{\theta JC}$ = 1.5°C/W, pulse duration ≤100 µs, duty cycle ≤1%

**Figure 1. Device absolute maximum ratings for the CSD17581Q5A**

As detailed in an earlier technical article, the thermal impedance in the data sheet is determined using standard test procedures and printed circuit board (PCB) layout. Figure 2 depicts the standard test boards used to measure the thermal impedance of a 5-mm-by-6-mm small outline no-lead (SON) package. TI has developed similar standardized test boards for other TI MOSFET packages.

Usually, real-world applications use a PCB with two or more layers, thermal vias and a pad area somewhere in between those shown in Figure 2. These efforts result in low thermal impedance, allowing the heat to spread into the internal PCB layers for a space-optimized solution using the smallest board area.

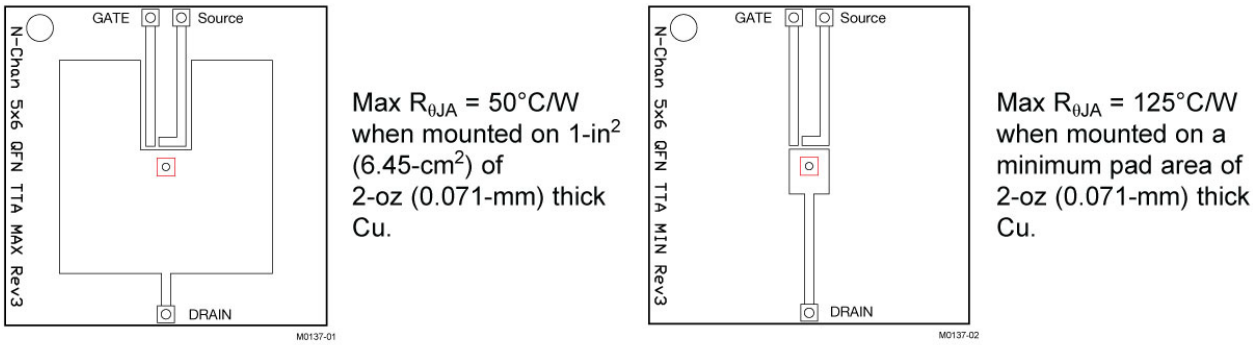


**Figure 2. 5-mm-by-6-mm SON junction-to-ambient thermal resistance ($R_{\theta JA}$) measurements as they appear in the CSD17581Q5A data sheet**

The maximum power dissipation is specified in the absolute maximum ratings table (Table 1) of a power MOSFET/power block data sheet. Maximum power dissipation is a calculated value, as shown in this technical article, and in reality, it is not very useful because the standard PCB used for this type of testing does not correlate to actual, real-world applications. Start with the absolute maximum ratings but keep in mind that the thermal capability of a particular package may be better or worse in your application, with your PCB design and ambient conditions.

$T_A$ = 25°C (unless otherwise stated)

**Table 1. CSD17581Q5A thermal impedance specifications**

| THERMAL METRIC | MIN TYP MAX | UNIT |
|---|---|---|
| $R_{\theta\ JC}$ Junction-to-case thermal resistance[1] | 1.5 | °C |
| $R_{\theta\ JA}$ Junction-to-ambient thermal resistance[1] [2] | 50 | |

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### Consider design experience and empirical data

Fortunately, there are existing designs using MOSFET packages that can give you an idea of the thermal capabilities of each package in real-world conditions. Combined with empirical data collected during testing, you should have some guidance for the amount of power that can be dissipated in a particular power MOSFET package. Table 1 through Table 5 summarize the estimated maximum power dissipation by product category and package type.

Keep in mind that the power dissipation numbers in the tables below are only estimates. Because the effective junction-to-ambient thermal impedance is very dependent upon the PCB design, your actual performance may vary; in other words, your particular design may be able to dissipate more or less power than what is presented here. Use these guidelines to help narrow down what packages to consider for your design.

### How to read the tables

Let's consider the 5-mm-by-6-mm plastic SON package. TI uses a few versions of this SON package for its power MOSFETs and power blocks. Most vendors have a similar package for their power devices, and a lot of data exists about how much power it can dissipate. TI has tested power blocks in this package on a PCB design with dimensions of 4 inches wide by 3.5 inches long by 0.062 inches high and six copper layers of 1-oz copper

[1] $R_{\theta JC}$ is determined with the device mounted on a 1-in$^2$ (6.45-cm$^2$), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
[2] Device mounted on FR4 material with 1-in$^2$ (6.45-cm$^2$), 2-oz (0.071-mm) thick Cu.

thickness. Based on the test results, a good rule of thumb is that the 5-mm-by-6mm SON package can dissipate about 3 watts in a typical application with a good layout.

**Table 2. Single N-channel MOSFET estimated power dissipation by package**

| Product category = single N-channel MOSFET | | | | |
|---|---|---|---|---|
| **Package description** | **Package type (drawing)** | **Dimensions (mm)** | **Typical $R_{\theta JA}$ (°C/W)** | **Estimated $P_{DISS}$ (W)** |
| FemtoFET™ | PicoStar™ package (YJM) | 0.73 by 0.64 | 255 | 0.5 |
| FemtoFET™ | PicoStar package (YJC, YJJ) | 1.0 by 0.6 | 245 | 0.5 |
| FemtoFET™ | PicoStar package (YJK) | 1.53 by 0.77 | 245 | 0.5 |
| Wafer-level package (W, W10) | DSBGA (YZB) | 1.0 by 1.0 | 275 | 0.4 |
| Wafer-level package (W1015) | DSBGA (YZC) | 1.0 by 1.5 | 230 | 0.5 |
| 2-mm-by-2-mm SON (Q2) | WSON (DQK) | 2.0 by 2.0 | 55 | 2.2 |
| Wirebond 3-mm-by-3mm SON (Q3A) | VSONP (DNH) | 3.3 by 3.3 | 48 | 2.5 |
| Clip 3-mm-by-3mm SON (Q3) | VSON-CLIP (DQG) | 3.3 by 3.3 | 48 | 2.5 |
| Wirebond 5-mm-by-6-mm SON (Q5A) | VSONP (DQJ) | 5.0 by 6.0 | 40 | 3.0 |
| Clip 5-mm-by-6-mm SON (Q5B) | VSON-CLIP (DNK) | 5.0 by 6.0 | 40 | 3.0 |
| Clip 5-mm-by-6-mm SON (Q5) | VSON-CLIP (DQH) | 5.0 by 6.0 | 40 | 3.0 |
| TO-220 (KCS) | TO-220 | N/A | 24 | 5.0 |
| D2PAK (KTT) | DDPAK/TO-263 | N/A | 30 | 4.0 |

**Table 3. Dual N-channel MOSFET estimated power dissipation by package**

| Product category = dual N-channel MOSFET | | | | |
|---|---|---|---|---|
| **Package description** | **Package type (drawing)** | **Dimensions (mm)** | **Typical $R_{\theta JA}$ (°C/W)** | **Estimated $P_{DISS}$ (W)** |
| LGA (L) | PicoStar package (YME) | 1.35 by 1.35 | 175 | 0.7 |
| LGA (L) | PicoStar package (YJE) | 2.2 by 1.15 | 150 | 0.8 |
| LGA (L) | PicoStar package (YJG) | 3.37 by 1.47 | 92.5 | 1.3 |
| Wafer-level package (W1723) | DSBGA (YZG) | 1.7 by 2.3 | 140 | 0.9 |
| 2-mm-by-2-mm SON (Q2) | WSON (DQK) | 2.0 by 2.0 | 55 | 2.2 |
| 3-mm-by-3-mm SON (Q3E) | VSON (DPA) | 3.3 by 3.3 | 50 | 2.4 |
| S0-8 (ND) | SOIC (D) | 5.0 by 6.0 | 60 | 2.0 |

**Table 4. Single P-channel MOSFET estimated power dissipation by package**

| Product category = single P-channel MOSFET | | | | |
|---|---|---|---|---|
| **Package description** | **Package type (drawing)** | **Dimensions (mm)** | **Typical $R_{\theta JA}$ (°C/W)** | **Estimated $P_{DISS}$ (W)** |
| FemtoFET™ | PicoStar package (YJM, YJN) | 0.73 by 0.64 | 255 | 0.5 |
| FemtoFET™ | PicoStar package (YJC, YJJ) | 1.0 by 0.6 | 245 | 0.5 |
| FemtoFET™ | PicoStar package (YJK) | 1.53 by 0.77 | 245 | 0.5 |
| LGA (L) | PicoStar package (YMG) | 1.2 by 1.2 | 225 | 0.5 |
| Wafer-level package (W10) | DSBGA (YZB) | 1.0 by 1.0 | 275 | 0.4 |
| Wafer-level package (W, W1015) | DSBGA (YZC) | 1.0 by 1.5 | 230 | 0.5 |

**Table 4. Single P-channel MOSFET estimated power dissipation by package (continued)**

| Product category = single P-channel MOSFET | | | | |
|---|---|---|---|---|
| **Package description** | **Package type (drawing)** | **Dimensions (mm)** | **Typical $R_{\theta JA}$ (°C/W)** | **Estimated $P_{DISS}$ (W)** |
| Wafer-level package (W, W15) | DSBGA (YZF) | 1.5 by 1.5 | 220 | 0.5 |
| 2-mm-by-2-mm SON (Q2) | WSON (DQK) | 2.0 by 2.0 | 55 | 2.2 |
| Wirebond 3-mm-by-3-mm SON (Q3A) | VSONP (DNH) | 3.3 by 3.3 | 48 | 2.5 |
| Clip 3-mm-by-3-mm SON (Q3) | VSON-CLIP (DQG) | 3.3 by 3.3 | 48 | 2.5 |

**Table 5. Dual P-channel MOSFET estimated power dissipation by package**

| Product category = dual P-channel MOSFET | | | | |
|---|---|---|---|---|
| **Package description** | **Package type (drawing)** | **Dimensions (mm)** | **Typical $R_{\theta JA}$ (°C/W)** | **Estimated $P_{DISS}$ (W)** |
| Wafer-level package (W1015) | DSBGA (YZC) | 1.0 by 1.5 | 230 | 0.5 |
| Wafer-level package (W15) | DSBGA (YZF) | 1.5 by 1.5 | 220 | 0.5 |

**Table 6. N-channel power block estimated power dissipation by package**

| Product category = N-channel power block | | | | |
|---|---|---|---|---|
| **Package description** | **Package type (drawing)** | **Dimensions (mm)** | **Typical $R_{\theta JA}$ (°C/W)** | **Estimated $P_{DISS}$ (W)** |
| LGA (P) | PTAB (MPC) | 3.0 by 2.5 | 67 | 1.8 |
| LGA (N) | PTAB (MPA) | 2.5 by 5.0 | 56 | 2.1 |
| LGA (M) | PTAB (MPB) | 5.0 by 3.5 | 50 | 2.4 |
| Clip 3-mm-by-3mm SON (Q3D) | LSON-CLIP (DQZ) | 3.3 by 3.3 | 58 | 2.1 |
| Clip 5-mm-by-6-mm SON (Q5D) | LSON-CLIP (DQY) | 5.0 by 6.0 | 40 | 3.0 |
| DualCool™ 5-mm-by-6-mm SON (Q5DC) packaging | VSON-CLIP (DMM) | 5.0 by 6.0 | 40 | 3.0 |

## Conclusion

You can use the information presented in this technical article to guide your package selection for power MOSFETs and power blocks. Always check that the MOSFET power loss in your application does not exceed the package capability. These are not absolute limits and the performance in your application will depend on the operating and environmental conditions, as well as the PCB layout and stackup.

Of course, power dissipation is not the only consideration when selecting a power device for a design. You'll also have to consider other parameters such as voltage and current ratings, on-resistance, package size, and lead spacing.

## Additional resources

- Find out more about TI MOSFET and power block products.
- Access the tools and information needed to understand and design thermal systems including design tools, lab analysis recommendations, education and FAQs on the Thermal Analysis page.
- Review the MOSFET technical article series, "Understanding MOSFET data sheets."

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