Application Note

How to Protect Op amps from Electrostatic Discharge & Electrical Overstress Damage

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ABSTRACT

Electrostatic discharge (ESD) cells have long been used in op amps to prevent devices from breaking before use. However, design and details are often seen as a black box. In this application note, the types of ESD cells are discussed, why the cells are required, how to read a device data sheet to determine the type of ESD cells used, and how to properly protect the circuit against ESD events.

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Trademarks

1 Introduction

Op amps can be damaged by electrostatic discharge (ESD) or other types of electrical overstress (EOS) events. The internal op amp device has ESD protection structures (called ESD cells) that are designed to protect against out of circuit ESD events. Out-of-circuit refers to the ESD applied to the device during the assembly and test process before it is soldered to a PCB. In some instances the ESD protection structures can also protect against in circuit ESD as well as other forms of EOS. However, it is important to understand what type of ESD cells are used, to understand how they behave versus overstress events. Furthermore, it is often necessary to add external components such as resistors, TVS diodes, and Schottky diodes to improve the robustness against overstress signals. Finally, knowing the type of ESD cells used can be important in board level product testing as different ESD cells have different characteristics for board level tests. This document describes the different ESD cells, and explain how to use these ESD cells with external components to protect the amplifier. The document also explains the general characteristics of the ESD cells that are normally seen in board level product tests.

2 ESD Overview

2.1 What is Electrostatic Discharge?

Electrostatic discharge (ESD) occurs when two items with a charge imbalance are brought in close proximity. There is a sudden flow of electricity between the two objects, which is called ESD. Insulators in particular are prone to developing large static charges.

ESD is the most common way that semiconductors are damaged. Looking at the voltage that ESD can generate, we see that there is a large gap between ESD discharge and human awareness. Some ICs can be damaged at 10V, but humans cannot even feel a discharge until 3500V. CMOSs and op amps are susceptible to damage at a lower voltage threshold than what humans can feel. Therefore, it is possible to damage a semiconductor without even knowing the ESD event has occurred. Static discharge arises from human handling, or contact with machines. Therefore, protecting against ESD events so that devices are not damaged is important before the application use.

2.1.1 ESD Cell Robustness in Semiconductors

Let us look more closely at the typical way in which semiconductor devices are damaged by ESD. Consider a large ESD potential, or voltage, which is applied between the inverting input and negative supply pin of an op amp (Figure 2-1).

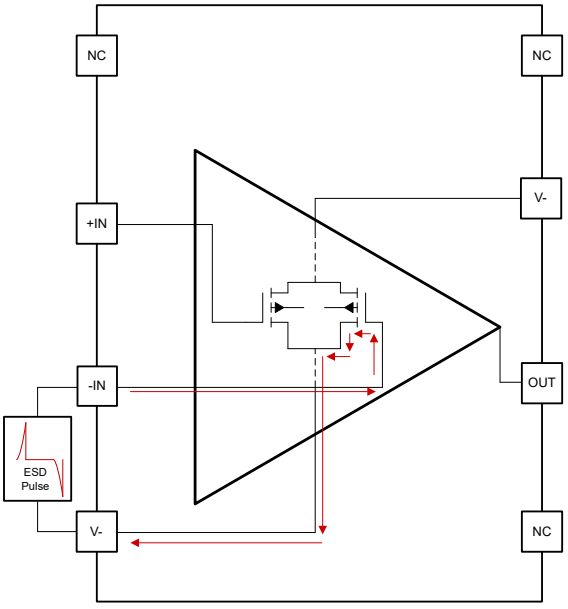

Figure 2-1. ESD Event Voltage Path

This ESD event places a large voltage from the gate to the source of one of the input MOSFETs, which can cause damage to the device. The thickness of the MOSFET gate oxide is on the scale of nanometers, making the MOSFET very susceptible to this kind of damage.

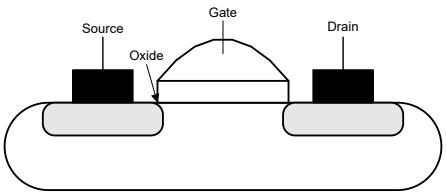

Figure 2-2. MOSFET Diagram

ESD protection diodes provide the necessary protection to prevent this damage. Improper handling of the device can lead to inadvertent ESD events. One of the most common ways an ESD pulse can occur is through IC interaction with a human. Humans can build up an electrostatic discharge through friction against walking on a

floor, brushing against furniture, etc. This charge can dissipate rapidly into an IC if touched without proper ESD protection. This is often on the scale of kilovolts, making the need for ESD cells obvious. To make sure the device can withstand these events, op amps are subjected to a quick voltage surge (in the range of kV) and tested afterwards to make sure the device is still functional. This simulation is called the human body model (HBM).

Another example of real life ESD events that is simulated in labs to make sure an IC can withstand the ESD event is the charged device model (CDM). CDM simulates events that most often occur in the manufacturing and assembly process through the build up of charge between the device and the automated test handler, or other automated devices used throughout the assembly process. When a device comes into contact with a grounded conductor, residual capacitance discharges, possibly causing damage to the IC. Careful handling of devices is required so that an ESD event is not triggered. When simulating this failure mode, devices are exposed to high voltages, then tested afterwards for functionality. Since the discharge usually takes place on the scale of nanoseconds, most failures are seen in the form of gate-oxide damage (as seen above), and junction damage.

The machine model (MM) was previously used to simulate the worst case HBM event. However, this does not accurately simulate real world ESD events, and is no longer used. Now, HBM and CDM is used to test ESD robustness in semiconductors.

JEDEC, the Joint Electron Device Engineering Council, sets the industry standards for the acceptable ESD ratings for semiconductor devices, including HBM and CDM tests. For more details on JEDEC and the industry semiconductor requirements, see the official website. All device data sheets contain the voltage threshold for the respective models. An example of a typical ESD ratings table is shown in Table 2-1, using device OPA596. Knowing the type of protection the device has is important. In the next section, the different types of ESD cells is discussed.

Table 2-1. ESD Ratings for OPA596

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	±1000	V
		Charged-device model (CDM), per JANSI/ESDA/JEDEC JS-002	±500	

3 Types of ESD Cells

So, how do we protect against ESD? There must be protection against thousands of volts that can discharge within nanoseconds. The answer is simple: use a diode. At the core, all ESD cells are variations of a diode. A diode, which is essentially a PN junction, clamps high voltages when the diode enters a forward biased state. However, in its reversed bias state, it acts as a high impedance and allows for normal operation. This makes it an excellent method to protect against ESD cells without compromising the normal operation of the IC.

There are many different types of ESD cells. However, there are advantages and disadvantages to each ESD cell. In this section, the most common forms of ESD cells is discussed, and how IC designers select the right cell type for the device.

3.1 Dual Diode Configuration

Figure 3-1 shows the most common ESD protection structure for an op amp. Dual diodes are placed on the inputs and outputs and are routed to the supplies. The ESD diodes direct any ESD transients onto the power supply. For this reason, the diodes are often called ESD steering diodes. To prevent damage to the op amp supply, an ESD absorption device is placed across the supply. The absorption device triggers on and act as a low impedance when the ESD event occurs. Thus, the absorption device limits the voltage applied across the supply and protect the device.

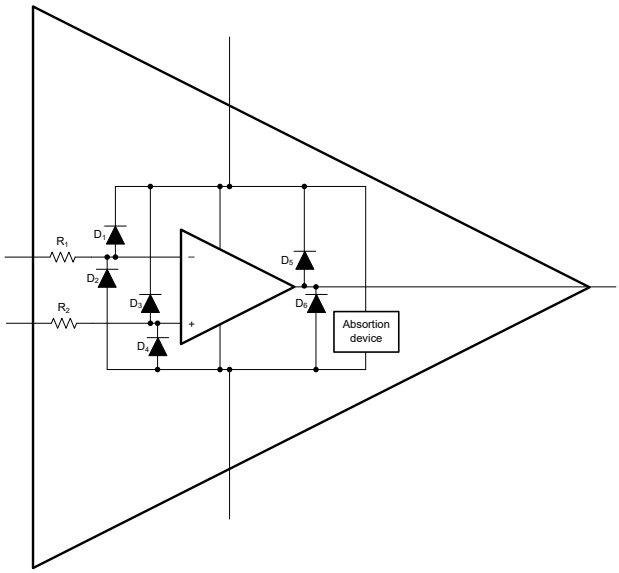

Figure 3-1. Dual Diode Configuration on Op Amp Input and Output

The benefits of the dual diode configuration include low leakage and low capacitance, making the dual diode configuration a great option for most op amps. The diodes only take up a small area, and are preferred to handle high frequency inputs and outputs. However, there are certain scenarios in which the dual diode configuration is not designed for protection.

3.1.1 Why Not Always Use Dual Diode Configuration?

The dual diode configuration is great for most op amp protection, but this is not preferred if the inputs have higher voltages than the supplies. This type of protection has issues if an input signal is applied to an amplifier before the amplifier is powered on. Some applications can turn off power on equipment, but still apply an input signal. Without additional protection, the dual diode configuration does not protect well against these input signals. This issue is explained later in the *Electrical Overstress* section of this document.

Open drain output is another scenario where dual diode configuration is not a good option. An open drain output is when the output of the device is connected to the drain of a transistor. In this setup, the device can only sink current. In cases of an open drain output, the traditional dual diodes are not placed on the output. Otherwise, the voltage clamp at the supply level, and the device is not be able to function as intended. Examples of this include timers, some comparators, and various differential amplifiers. Difference amplifiers often have an input signal that is higher than the supply voltage, making alternative methods of protection required against ESD.

3.2 Bootstrapped Diodes

Only dual diode ESD protection structure has been discussed. There is another type of ESD protection structure called bootstrapped diodes, where the diodes are placed in parallel and reverse. An additional diode is routed from the input to the supply to allow for the same protection path as seen before.

Typical ESD steering diodes have a leakage current. The current is picoamps at room temperature and thousands of picoamps at 125C. For applications with high source impedances, this leakage can create large input offset voltage errors. Bootstrapping reduces this leakage to femtoamps across temperature. Bootstrapping does this by motoring the input voltage and forcing the same voltage on the opposite side of the diode. The forced voltage is called the guard voltage. The input ESD diodes have the same voltage on both the cathode and anode so that there is zero volts across the diode. Forcing zero volts across the diode, also known as *bootstrapping*, forces the leakage current to essentially zero. During an ESD event, the input diodes channels the ESD pulse to the diodes connected to the supply. Since there are two diodes routed to the supply, voltage drop from input to supply is measured. There is a drop of 1.4V, or approximately two diode drops. A flagship device that uses this topology is the OPA928. The bootstrapped inputs allow for an input bias current of 20fA at both 25°C and 85°C.

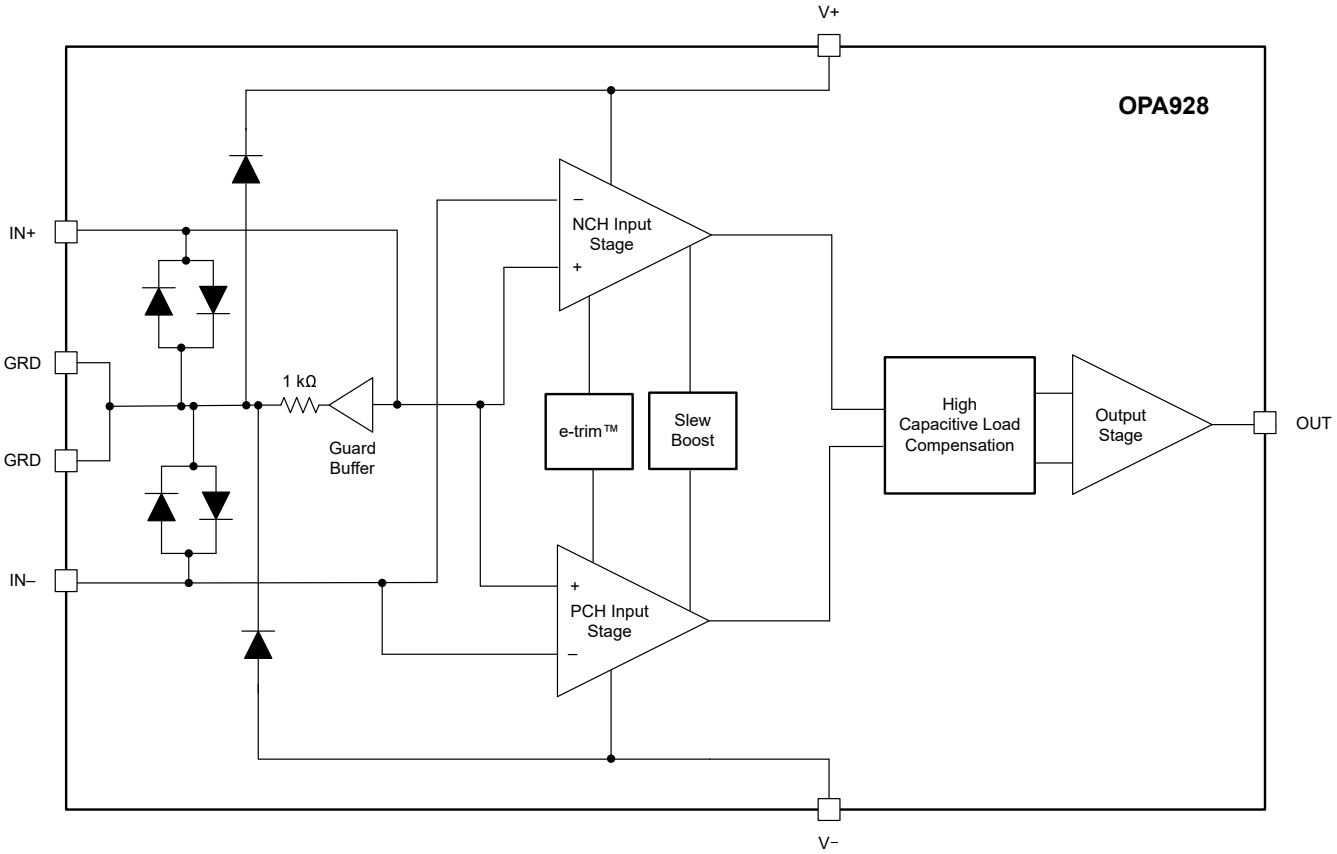

Figure 3-2. OPA928 Bootstrapped Diode Structure

3.3 Absorption Devices

The absorption device is an internal clamping device, which limits the voltage across the op amp supply when an input ESD event is directed onto the supply through the input diodes. Figure 3-3 shows the typical high-level structure of an absorption device.

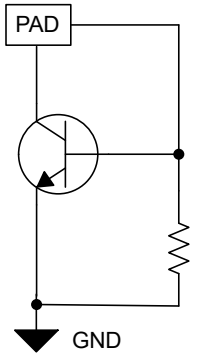

Figure 3-3. Absorption Device

The absorption device is designed to clamp the supply voltage during an **out-of-circuit** ESD event to prevent damage. Once the event ends, typically after a few nanoseconds, the absorption device turns off since there is no power supply connected to the device. If the absorption device turns on for an **in-circuit** ESD event, it can remain on and in a low impedance state until power is removed from the circuit. Thus, it is imperative that the absorption device is not allowed to turn on during in-circuit electrical overstress events.

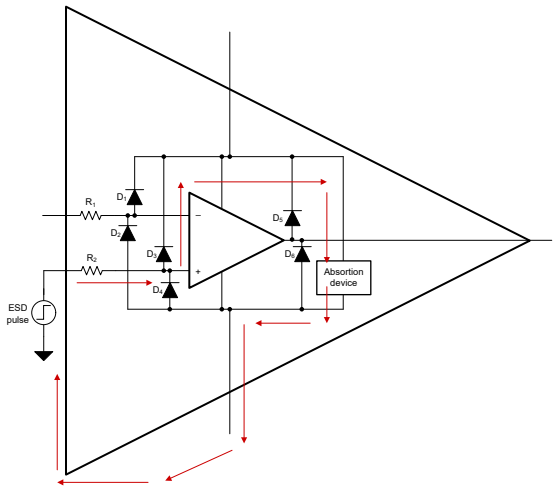

Figure 3-4. ESD Diode Steering

Figure 3-4 is an example of an ESD pulse being applied to the non-inverting node of an op amp. In the real world, this can happen by improper handling of the device; for example, assembling a PCB on a non-static safe work surface. Notice that diode D3 becomes forward biased and *steers* the ESD pulse to the absorption device. The absorption device is designed to limit the voltage and absorb the energy of the ESD pulse. Note that if the ESD pulse were applied to different pins, different diodes turn on and steer the pulse to the absorption device. Also, notice that the input resistance R2 limits the input current from the ESD pulse. A larger value of R2 makes the circuit more robust, since this limits the current going into the device. However, errors can be introduced from bias current and noise, and can also affect the frequency response of the circuit.

3.3.1 Active Clamps

An active clamp is a very common absorption device used in semiconductors. An active clamp is a very large MOS that is in active mode during ESD conditions and is high impedance under normal operating conditions. During an ESD event, the MOS acts as a switch, allowing uniform current flow with a low voltage drop. This device can be edge triggered (dv/dt based) or level triggered. These are most commonly used for protection when the supplies are powered off, but there is still an input signal.

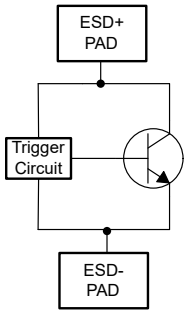

Figure 3-5. Active Clamp

An advantage of this structure is that is has a very low clamping voltage. However, the performance is based on the drain current saturation; as a result, the clamp can take up a very large area. Therefore, a different type of clamp can be more useful if the size of the integrated circuit is a key parameter.

3.3.2 GCNMOS Clamps

Gate-coupled NMOS (GCNMOS) clamps are another common form of an absorption device. The gate of the NMOS is connected to an RC trigger circuit that is pulled high during an ESD event. Generally, the response time of the circuit is less than 10ns. These clamps have similar advantages and disadvantages as the active clamp, with size being a major factor, as well as the lower clamping voltage.

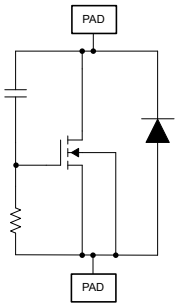

Figure 3-6. GCNMOS Clamp

Both the active clamp and GCNMOS clamp are considered forms of snapback protection structures. The next section focuses on other forms of snapback ESD protection cells.

3.4 Silicon Controlled Rectifiers

Silicon controlled rectifiers, or SCRs, are another common option used for clamping. SCRs leverage hole generation at the drain of the MOSFET to increase the base current of the NPN. This has a cascading effect, and in turn, increases the current in the parasitc PNP, leading to regeneration. SCRs leverage a cascading PNP/NPN device structure for ESD protection. The SCR has a low holding voltage (V_H), but high trigger voltage (V_T), which creates a deep snapback effect. This effect can be clearly seen in an IV curve (Figure 3-7). Figure 3-8 is a high level design figure of a typical SCR.

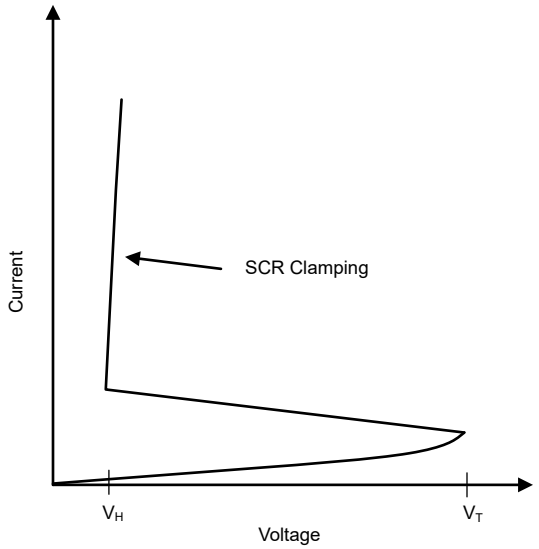

Figure 3-7. SCR IV Curve

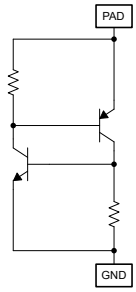

Figure 3-8. SCR Clamp

SCRs are often used in designs where area is a key parameter, due to the small size. SCRs also have very low leakage and capacitance, providing further advantage to designs with low bias current. However, these ESD cells have a higher risk of latch-up, since the holding voltage of the cell is lower than VDD. Latch up occurs when there is positive feedback between the NPN/PNP. If latch up does occur in your device, best practice is to power cycle to prevent damage to the device.

3.5 CER and ECR NPN Diodes

The CER/ECR NPN ESD protection structure is another common option, particularly for higher voltages. This behaves similarly to a snapback diode, in that the voltage reaches a certain level before dropping back to the threshold voltage. Figure 3-9 shows the general layout.

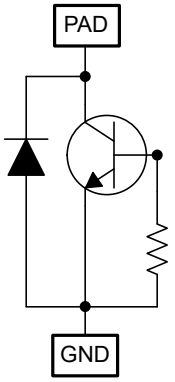

Figure 3-9. CER Diode Structure

The protection structure raises the base potential to lower the NPN trigger voltage. These are preferred when the device is tolerant to a high trigger or clamping voltage. Note that one pad is connected to ground through a diode. The other pad is voltage triggered. This offers ESD protection while taking up a relatively small area, albeit not as small as an SCR structure. These structures are also advantageous because the structures are generally considered to be a latch-up free design unlike SCRs, which are more prone to latch-up.

3.5.1 Measuring the Response of an ECR and CER ESD Cell

Figure 3-10 shows a circuit setup to measure the ESD behavior of LM2904B. Note that a 100Ω series limiting resistor is used to make sure that the device does not see an input current greater than 10mA. This device has a ECR ESD cell that is level triggered at approximately 65V.

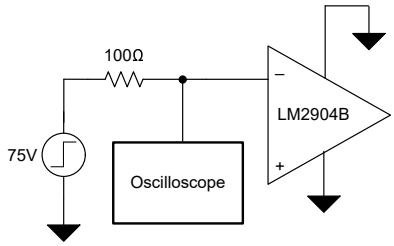

Figure 3-10. LM2904B Diode Measurement Circuit

Figure 3-11 shows the raw measurement of the ESD cell in the time domain. The ESD cell drops the voltage down to approximately 30V after forcing a 75V input.

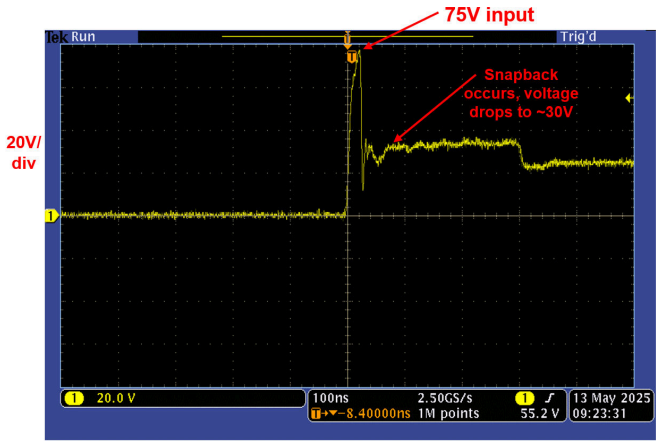

Figure 3-11. LM2904B Snapback Measurement

3.6 Comparison of ESD Cells

Overall, many factors go into the design of ESD cells for a particular op amp. Consider the trade offs each structure has when designing an op amp. Below shows the IV curve of the different types of ESD clamps, emphasizing the importance of your application when choosing the correct ESD protection structure.

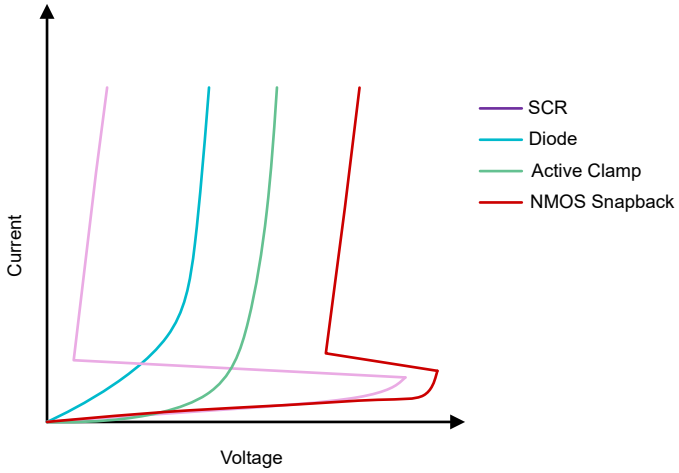

Figure 3-12. ESD Clamp Comparison

4 How to Determine the ESD Structure of the Device from the Data Sheet

How can you know what type of protection the op amp has? The effectiveness of the ESD protection is listed on the data sheet in the ESD ratings table. This specification is developed by applying an emulated ESD pulse to all the device pins and checking for damage. The ESD event is generated by special test equipment that creates a controlled ESD pulse with the same charge, voltage levels, inductance, resistance, and capacitance of a real-world situation. Typically, the real-world situation being emulated is the human-body or charged-device in contact with a low impedance. This was mentioned earlier in a previous section. The ESD voltage levels specified in Table 4-1 reflect the maximum ESD voltage that was applied without damaging the device TLV9141.

Table 4-1. TLV9141 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

There are two ways to know if a particular device contains ESD protection diodes or relies upon another method to achieve ESD robustness. Look at the *Absolute Maximum Ratings* table, or in some cases you can find a functional block diagram that illustrates the diodes. In the Absolute Maximum Ratings table, when the input voltage range is limited to approximately 0.5V beyond the supply range, then the device contains dual diode configuration ESD diodes (see Table 4-2). This is due to the forward bias voltage of a diode generally being around 0.5V. If the input signal stays inside this range the ESD diodes does not turn on. This type of protection generally also provides an input current limit of ±10mA.

Table 4-2. TLV2888 Absolute Maximum Ratings (Dual Diode Example)

			MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)			26	V
	Input voltage	Common-mode	(V–) –0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Output short-circuit (1)		Continuous		
T_J	Operating junction temperature		-40	150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Short-circuit to ground, one amplifier per package.

If the device is using a transient or level triggered protection, the input voltage range usually goes up to the maximum recommended power supply voltage operating conditions. This is shown below using the LM2904B data sheet (see Table 4-3).

Table 4-3. LM2904BQ Absolute Maximum Ratings (Level Triggered Example)

over operating ambient temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage, V_S = ([V+] – [V–])				40	V
Differential input voltage, V_{ID} (2)			–32	32	V
Input voltage, V_I	Either input		–0.3	40	V
Duration of output short circuit (one amplifier) to V– at (or below) T_A = 25°C, V_S ≤ 15V (3)			Unlimited		s
Operating ambient temperature, T_A			–40	125	°C
Operating virtual-junction temperature, T_J				150	°C
Storage temperature, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) Differential voltages are at IN+, with respect to IN−.

3) Short circuits from outputs to the supply pins can cause excessive heating and eventual destruction.

Another simple way to determine the internal ESD protection scheme is to look at the functional block diagram of the device. The data sheet often contains this, and the internal diodes are frequently included in the functional block diagram. This was previously seen from Figure 3-2, the functional block diagram for OPA928.

5 How to Protect The System from In Circuit ESD/EOS Events

Knowing the internal protection scheme of the op amp is important, because the information helps when designing protection schemes for the system as a whole. ESD diodes are designed for out of circuit events, so additional design consideration is needed if wanting to optimize your system for any in circuit electrical overstress events (EOS).

Consider Figure 5-1. This op amp has the diode to supply protection scheme, with an LDO attached to the positive supply. The max supply of the op amp is 10V, and the LDO is regulating 24V to 5V. 15V is applied to the non-inverting node of the op amp.

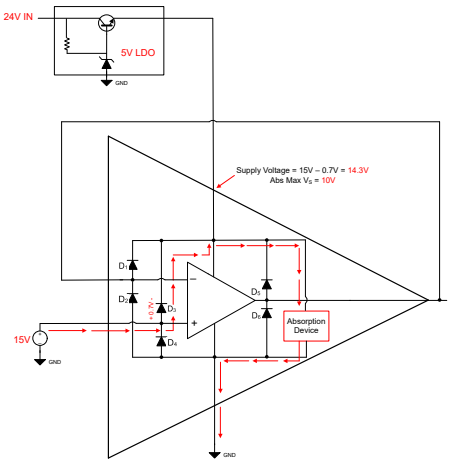

Figure 5-1. EOS Event: Overvoltage Input

D3 directs the voltage through the device into the power supply; since the voltage is above the absolute maximum rating, the absorption device turns on. However, the voltage being supplied is continuous, so the absorption device latches and stays on unless the circuit is power cycled. While the circuit is on, the absorption device is drawing large amounts of current from the LDO, generating a large amount of heat and oftentimes destroying the device.

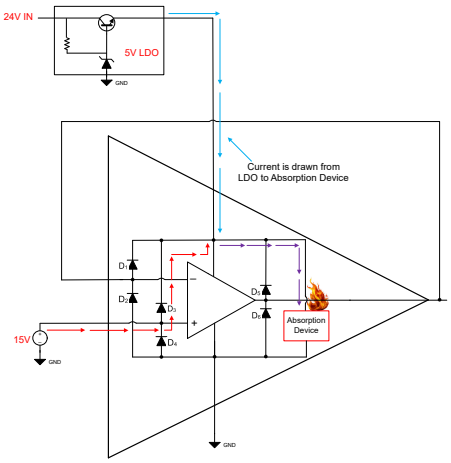

Figure 5-2. EOS Event - Absorption Device Latches

How can this be prevented from happening? There are two simple steps to take. One is to add an input resistance. The next step is to add a TVS diode to the power supply.

5.1 Using TVS Diodes and Series Resistance for Circuit Protection

A simple way to protect against the EOS event is to add a series limiting resistor to the input, as shown in Figure 5-3. This helps limit the current the op amp sees on the non-inverting node. Select the value of the resistor such that the current is limited to 10mA, and that the current is not so big that the resistor noise affects the circuit.

Now, when the overstress voltage is applied, the 1k resistor limits the voltage and current seen by the device. The current drops to 7.3mA, which is lower than the typical 10mA limit seen on most data sheets. Diode 3 steers the voltage, which is still above the maximum rating, to the power supply. The transient voltage suppressor (TVS) diode is connected to the supply such that the supply voltage is limited to 7V, and the absorption device does not turn on.

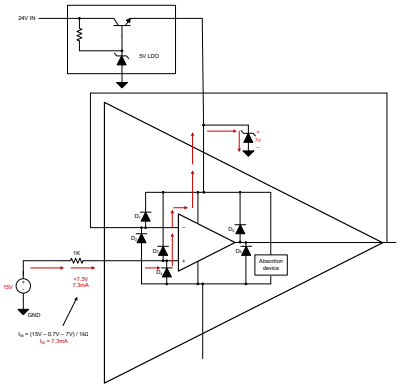

Figure 5-3. EOS Protection with TVS Diodes & Series Resistance

A TVS is designed for quick turn on and large power dissipation, making the TVS an option for handling large current and voltage surges that are typical of an ESD/EOS event. Below shows the IV curve of a unidirectional TVS diode curve.

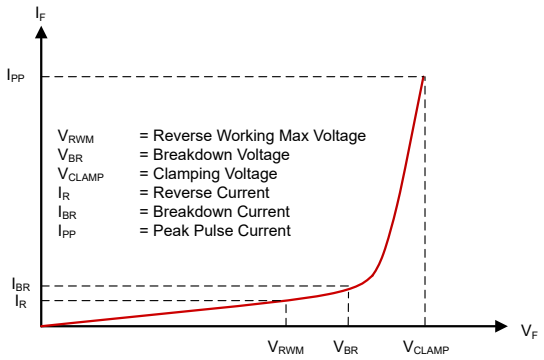

Figure 5-4. Unidirectional TVS Diode Curve

When selecting a TVS diode, understanding the characteristics of the diode is important. V_{RWM}, or the reverse working maximum voltage is the maximum voltage that can be applied to the diode before higher leakage starts to occur. I_R is the typical current seen at V_{RWM}. The TVS diode must be selected such that the supply voltage of the device equal to the V_{RWM} of the TVS diode. This allows for minimal leakage during operation.

The peak pulse current corresponds to the maximum current that the TVS diode can handle before failure. The clamping voltage is voltage level the diode regulates to when the clamping voltage sees a transient current.

The breakdown voltage, V_{BR}, is the voltage at which higher leakage current is seen. The value must be chosen to be less than the absolute maximum voltage of the device. This allows the TVS diode to turn on and clamp the supply voltage to a safe level so that the supply never reaches the absolute maximum voltage. However, this is not always possible because there is sometimes no TVS diode that has a V_{RWM} at the operating voltage and a V_{BR} below the absolute maximum rating.

Consider the OPA320. This device has a maximum operating supply voltage of 5.5V and an absolute maximum voltage rating of 6V. If V_{RWM} is set to 5.5V there is never a TVS diode that breaks down before 6V. However, external protection must still be used even though the external protection does not have the preferred characteristics.

5.2 Using Schottky Diodes for Circuit Protection

An EOS event can also occur if the op amp has a transient triggered protection scheme. However, the protection method for an edge triggered op amp is different than a dual diode protection scheme. In the edge triggered protection, the ESD cell is only triggered at a certain dv/dt level.

Here, Schottky diodes are more appropriate to use for protection. Schottky diodes have very fast switching characteristics which are preferred for ESD/EOS surges. Since the edge triggered diode protection structure does not have a set trigger voltage, the Schottky diodes help to detect the surge event, directing most, if not all, of the surge through the diodes. Schottky diodes have a low forward bias voltage, around 0.3V. Ideally, the Schottky diodes added must have a lower forward bias voltage drop than the internal diodes. This allows the majority of the EOS current to flow through the external diodes, decreasing the likelihood of damage to the op amp.

Figure 5-5 shows an op amp in a noninverting configuration. R_p has been added to the input, as well as two Schottky diodes. Adding R_p in series with the Schottky diodes further limits the current the op amp sees from the surge event.

However, Schottky diodes have a high leakage current. Thus, if this is an important design factor, other diodes must be considered. In this example, we only have input protection because only the input side is connected externally. External connections are much more prone to EOS events. Examples of this include large induced voltages, or long sensor leads often seen in factory automation.

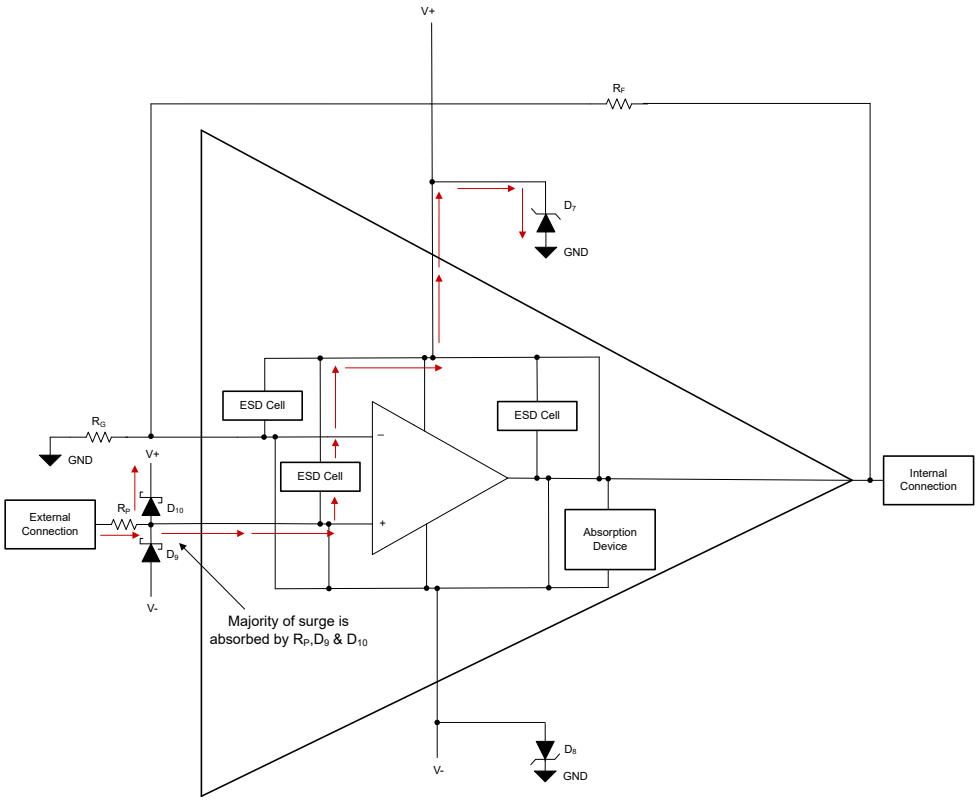

Figure 5-5. Schottky Diode Input Based Protection

Sometimes, there is a need to protect the output of the op amp (see Figure 5-6). The figure below shows a similar circuit that can be used. In this case, select R_p such that R_p does not limit the output swing of the op amp. Generally, choosing a resistance between 10 - 20Ω allows for good protection and functionality. Also note that R_p is inside the feedback loop. This allows an accurate output voltage to be maintained despite the voltage dropped across R_p . Finally, notice that very low current flows through R_F to the input of the circuit as the value of R_F is generally much larger than R_p .

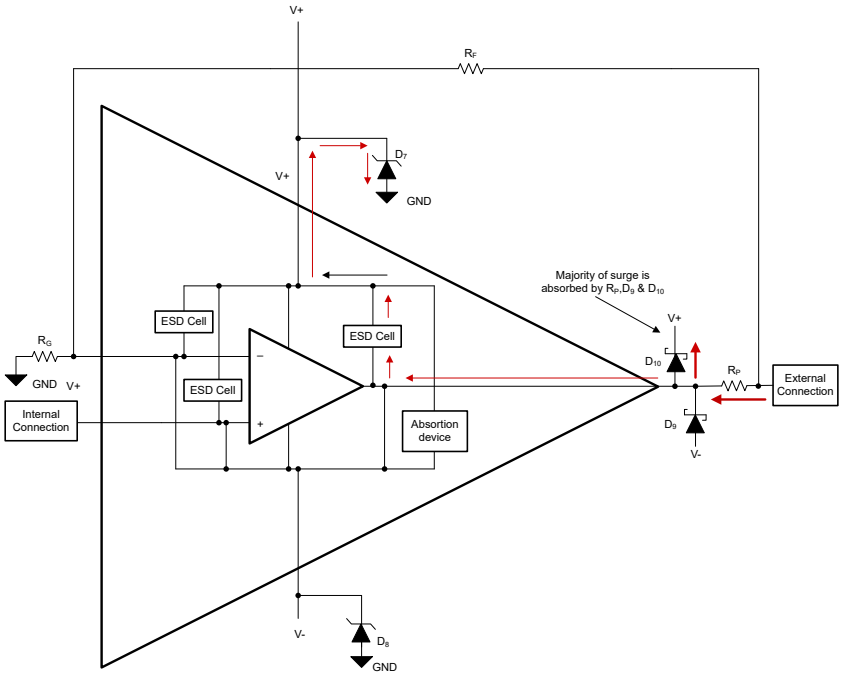

Figure 5-6. Schottky Diode Output Based Protection

Like all circuits, there are trade-offs. Adding protection to the circuit also introduces noise to the system. Consider noise, component space, and so on when designing the circuit. However, such considerations are beyond the scope of this paper. For more details on how minimize noise, see this paper on minimizing noise while protecting your op amp.

6 How to Test an Op Amp in a System Level Circuit

In many system level designs, testing is performed while op amps are powered off to confirm all components are working. When testing op amps, a voltage or current is applied to the inputs, and the resistance is measured. Depending on the internal diode structure, a wide spectrum of results are viable. The resistance that is being measured is the resistance of the ESD cell(s) inside of the op amp. However, there are a few key parameters that must be followed during a system level test to make sure there is a valid measurement, and that the op amp is not damaged in this test.

The first step is making sure that the device is not powered on. The next step is to ground the supplies of the device. Figure 6-1 shows a valid in circuit test setup for an op amp.

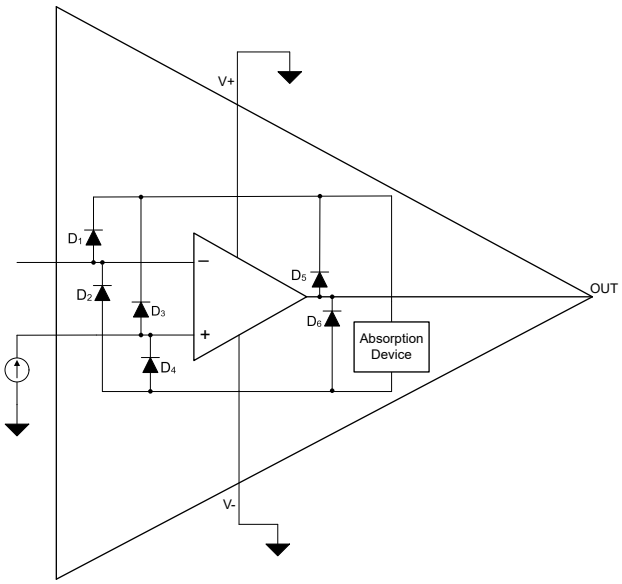

Figure 6-1. In Circuit Test Setup

Consider the following example: an op amp has a voltage placed on the inputs, while the supplies are left floating. Since the supplies are floating, the voltage has no path to the absorption device. This can lead to unintentionally powering the device on, creating undesired output signals, which can affect other devices in the system. Therefore, best practice is to ground both supplies when verifying device in a system level test. For more details on back-powering an amplifier, see this application note.

6.1 ESD Protection Cell Advancements Over the Years

Like any semiconductor technology, great advancements have been made over the decades. ESD protection was not a standard part of the op amp design until the 1990s. Thus, many devices from the 1970s and 1980s possibly does not have ESD cells! These older generation op amps have larger geometry devices so the op amps are inherently more robust against ESD damage. However, if ESD protection is the main concern, review the ESD specification and confirm that the device meets your requirement.

Some op amps have been updated over the years, moving to newer processes and technologies. During this modernization, ESD cells were added or changed. Since the topology has changed, the inherent resistance from the diode structure is also different. This can lead to false failures in a system level board test.

Most diodes follow the same general IV curve, as seen below. Usually, the forward bias voltage is around 0.7V for silicon diodes. However, all diodes vary, and updating the ESD cells can change the IV curve characteristics of ESD cells inside an op amp.

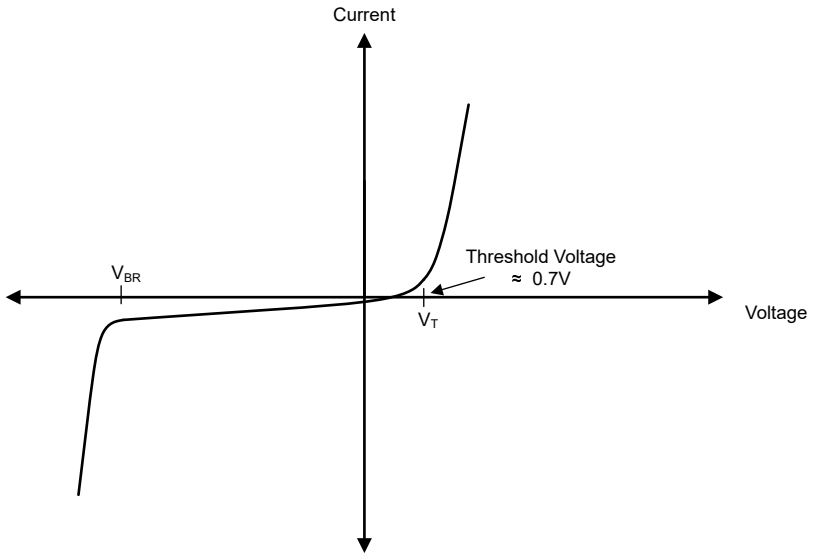

Figure 6-2. I/V Curve of Diode

One example of an op amp with updated ESD structure is the OPAx130 family. Table 6-1 shows the IV measurement differences of the op amp with the original ESD design, and the updated design. In this setup, 100µA is forced into the pin, and the voltage is measured.

Table 6-1. OPA2130 Input and Output to VCC Measurements

Pin to V+ Voltage Measurements	Pin 1 to Pin 8 (OUT A to V+)	Pin 2 to Pin 8 (-IN A to V+)	Pin 3 to Pin 8 (+IN A to V+)	Pin 5 to Pin 8 (+IN B to V+)	Pin 6 to Pin 8 (-IN B to V+)	Pin 7 to Pin 8 (OUT B to V+)
OPA2130 Original Design	0.609678V	0.699382V	0.668025V	0.670190V	0.668482V	0.610322V
OPA2130 Redesign	0.688358V	0.709175V	0.709203V	0.709174V	0.709235V	0.688545V

Note that while the diode structure of a device can change, there is no change in behavior of the device. This is because these protection structures are only triggered during abnormal device operation, such as ESD.

7 Summary

This application note has discussed what ESD is, how semiconductor chips are designed to protect against these events. Important factors such as area, trigger voltage, capacitance, and applications are all considered when designing ESD cells. Knowing the type of ESD cells your device has can help you design protection on both an individual and system level.

8 References

- Texas Instruments, TIPL ESD/EOS Training, video.
- Texas Instruments, *Opamp Input Protection Can Be Noisy*, blog.
- Texas Instruments, Op amp ESD Protection Structures, application note.
- Texas Instruments, *ESD Clamps*, presentation.

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