Errata

Errata AM261 Sitara™ Microcontroller Silicon Revision 1.0

ABSTRACT

This document describes the known exceptions to the functional specifications (advisories). This document may also contain usage notes. Usage notes describe situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness.

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1 Usage Notes and Advisories Matrices

Table 1-1 lists all usage notes and the applicable silicon revision(s). Table 1-2 lists all advisories, modules affected, and the applicable silicon revision(s).

Table 1-1. Usage Notes Matrix

Module	DESCRIPTION	SILICON REVISIONS AFFECTED
		AM261
		1.0
CLOCKS	i2324 — No synchronizer present between GCM and GCD status signals	YES

Table 1-2. Advisories Matrix

MODULE	DESCRIPTION	SILICON REVISIONS AFFECTED
		AM261
		1.0
CONTROLSS	i2352 — CONTROLSS-SDFM: Dynamically Changing Threshold Settings (LLT, HLT), Filter Type, or COSR Settings Will Trigger Spurious Comparator Events	YES
CONTROLSS	i2353 — CONTROLSS-SDFM: Dynamically Changing Data Filter Settings (Such as Filter Type or DOSR) Will Trigger Spurious Data Acknowledge Events	YES
CONTROLSS	i2354 — CONTROLSS-SDFM: Two Back-to-Back Writes to SDCPARMx Register Bit Fields CEVT1SEL, CEVT2SEL, and HZEN Within Three SD-Modulator Clock Cycles can Corrupt SDFM State Machine, Resulting in Spurious Comparator Events	YES
CONTROLSS	i2356 — CONTROLSS-ADC: Interrupts may Stop if INTxCONT (Continue-to-Interrupt Mode) is not Set	YES
CONTROLSS	i2357 — CONTROLSS-ePWM: An ePWM Glitch can Occur if a Trip Remains Active at the End of the Blanking Window	YES
CONTROLSS	i2358 — CONTROLSS-ePWM: Trip Events Will Not be Filtered by the Blanking Window for the First 3 Cycles After the Start of a Blanking	YES
CONTROLSS	i2359 — CONTROLSS-CMPSS:Prescaler counter behavior different from spec when DACSOURCE is made 0 or reconfigured as 1	YES
CPSW	i2345 — CPSW: Ethernet Packet corruption occurs if CPDMA fetches a packet which spans across memory banks	YES
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UART	i2311 — USART: Spurious DMA Interrupts	YES
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TCM	i2411 — 128 Bytes burst access is not supported for TCM	YES
OSPI	i2383 — OSPI: 2-byte address is not supported in PHY DDR mode	YES
PBIST	i2374 — PBIST fails if clock frequency of R5SS_CORE_CLK is not same as R5FSS_CLK_SELECTED frequency	YES
OSPI	i2351 — OSPI: Direct Access Controller (DAC) does not support Continuous Read mode with NAND Flash	YES
OSPI	i2189 — OSPI: Controller PHY Tuning Algorithm	YES
CPSW	i2440 - CPSW: Host to Ethernet Timestamp Sequence ID issue	YES
CPSW	i2439 - CPSW: Host to Ethernet Timestamp Accuracy Issue	YES
ICSS	i2433 - ICSS: Reading the 64-bit IEP timer does not have a lock MSW logic when LSW is read	YES

2 Silicon Revision *1.0* Usage Notes and Advisories

This section lists the usage notes and advisories for this silicon revision.

2.1 Silicon Revision *1.0* Usage Notes

This section lists all the usage notes that are applicable to silicon revision *1.0* [and earlier silicon revisions].

i2324 ***No synchronizer present between GCM and GCD status signals***

Details:

There is no synchronizer in between GCM and GCD, so the clock configuration register reads may be incorrect momentarily.

Severity:

Minor

Workaround(s):

Poll for the status registers change until it reflects the programmed SRC_SEL and DIV values.

2.2 Silicon Revision *1.0* Advisories

The following advisories are known design exceptions to functional specifications. Advisories are numbered in the order in which they were added to this document. Some advisory numbers may be removed in future revisions of this document because the design exception was fixed or documented in the device-specific data manual or technical reference manual. When items are deleted, the remaining advisory numbers are not re-sequenced.

i2189 ***OSPI: Controller PHY Tuning Algorithm***

Details:

The OSPI controller uses a DQS signal to sample data when the PHY Module is enabled. However, there is an issue in the module which requires that this sample must occur within a window defined by the internal clock. Read operations are subject to external delays, which change with temperature. In order to guarantee valid reads at any temperature, a special tuning algorithm must be implemented which selects the most robust TX, RX, and Read Delay values.

Workaround(s):

The workaround for this bug is described in detail in the application note spract2 (link: https://www.ti.com/lit/spract2). To sample data under some PVT conditions, it is necessary to increment the Read Delay field to shift the internal clock sampling window. This allows sampling of the data anywhere within the data eye. However, this has these side effects:

1. PHY Pipeline mode must be enabled for all read operations. Because PHY Pipeline mode must be disabled for writes, reads and writes must be handled separately.
2. Hardware polling of the busy bit is broken when the workaround is in place, so SW polling must be used instead. Writes must occur through DMA accesses, within page boundaries, to prevent interruption from either the host or the flash device. Software must poll the busy bit between page writes. Alternatively, writes can be performed in non-PHY mode with hardware polling enabled.
3. STIG reads must be padded with extra bytes, and the received data must be right-shifted.

i2310 *USART: Erroneous clear/trigger of timeout interrupt*

Details:

The USART may erroneously clear or trigger the timeout interrupt when RHR/MSR/LSR registers are read.

Workaround(s):

For CPU use-case.

If the timeout interrupt is erroneously cleared:

-This is OK since the pending data inside the FIFO will retrigger the timeout interrupt

If timeout interrupt is erroneously set, and the FIFO is empty, use the following SW workaround to clear the interrupt:

- Set a high value of timeout counter in TIMEOUTH and TIMEOUTL registers

- Set EFR2 bit 6 to 1 to change timeout mode to periodic

- Read the IIR register to clear the interrupt

- Set EFR2 bit 6 back to 0 to change timeout mode back to the original mode

For DMA use-case.

If timeout interrupt is erroneously cleared:

-This is OK since the next periodic event will retrigger the timeout interrupt

-User must ensure that RX timeout behavior is in periodic mode by setting EFR2 bit6 to 1

If timeout interrupt is erroneously set:

-This will cause DMA to be torn down by the SW driver

-OK since next incoming data will cause SW to setup DMA again

i2311 *USART Spurious DMA Interrupts*

Details:

Spurious DMA interrupts may occur when DMA is used to access TX/RX FIFO with a non-power-of-2 trigger level in the TLR register.

Workaround(s):

Use power of 2 values for TX/RX FIFO trigger levels (1, 2, 4, 8, 16, and 32).

i2345 *CPSW: Ethernet Packet corruption occurs if CPDMA fetches a packet which spans across memory banks*

Details:

Each memory bank in SoC has a separate memory controller. Even though memory addresses are contiguous, each bank is a separate entity with a separate controller.

If a memory bank received a memory request say 32 bytes and address of memory request is 16 bytes before end of memory bank, the behavior of the memory controller will be:

When the memory controller encounters end of memory bank after 16 bytes it will wrap around and give 16 bytes from the start of the memory bank.

i2345 (continued) ***CPSW: Ethernet Packet corruption occurs if CPDMA fetches a packet which spans across memory banks***

This results in the packet corruption.

Workaround(s):

Ensure from application side single ethernet packet does not span across memory banks.

i2351 ***OSPI: Direct Access Controller (DAC) does not support Continuous Read mode with NAND Flash***

Details:

The OSPI Direct Access Controller (DAC) doesn't support Continuous Read mode with NAND Flash since the OSPI controller can deassert the CSn signal (by design intent) to the Flash memory between internal DMA bus requests to the OSPI controller.

The issue occurs because "Continuous Read" mode offered by some OSPI/QSPI NAND Flash memories requires the Chip Select input to remain asserted for an entire burst transaction.

The SoC internal DMA controllers and other initiators are limited to 1023 B or smaller transactions, and arbitration/queuing can happen both inside of the various DMA controllers or in the interconnect between any DMA controller and the OSPI peripheral. This results in delays in bus requests to the OSPI controller that result in the external CSn signal being deasserted.

NOR Flash memories are not affected by CSn de-assertion and Continuous Read mode works as expected.

Workaround(s):

Software can use page/buffered read modes to access NAND flash.

i2352 ***CONTROLSS-SDFM: Dynamically Changing Threshold Settings (LLT, HLT), Filter Type, or COSR Settings Will Trigger Spurious Comparator Events***

Details:

When SDFM comparator settings—such as filter type, lower/upper threshold, or comparator OSR (COSR) settings—are dynamically changed during run time, spurious comparator events will be triggered. The spurious comparator event will trigger a corresponding CPU interrupt, CLA task, ePWM X-BAR events, and GPIO output X-BAR events if configured appropriately.

Workaround(s):

When comparator settings need to be changed dynamically, follow the procedure below to ensure spurious comparator events do not generate a CPU interrupt, CLA event, or X-BAR events (ePWM X-BAR/GPIO output X-BAR events):

1. Disable the comparator filter.
2. Delay for at least a latency of the comparator filter + 3 SD-Cx clock cycles.
3. Change comparator filter settings such as filter type, COSR, or lower/upper threshold.
4. Delay for at least a latency of the comparator filter + 5 SD-Cx clock cycles.
5. Enable the comparator filter.

i2353 *CONTROLSS-SDFM: Dynamically Changing Data Filter Settings (Such as Filter Type or DOSR) Will Trigger Spurious Data Acknowledge Events*

Details:

When SDFM data settings—such as filter type or DOSR settings—are dynamically changed during run time, spurious data-filter-ready events will be triggered. The spurious data-ready event will trigger a corresponding CPU interrupt, CLA task, and DMA trigger if configured appropriately.

Workaround(s):

When SDFM data filter settings need to be changed dynamically, follow the procedure below to ensure spurious data-filter-ready events are not generated:

1. Disable the data filter.
2. Delay for at least a latency of the data filter + 3 SD-Cx clock cycles.
3. Change data filter settings such as filter type and DOSR.
4. Delay for at least a latency of the data filter + 5 SD-Cx clock cycles.
5. Enable the data filter.

i2354 *CONTROLSS-SDFM: Two Back-to-Back Writes to SDCPARMx Register Bit Fields CEVT1SEL, CEVT2SEL, and HZEN Within Three SD-Modulator Clock Cycles can Corrupt SDFM State Machine, Resulting in Spurious Comparator Events*

Details:

Back-to-back writes to SDCPARMx register bit fields CEVT1SEL, CEVT2SEL, and HZEN within three SD-modulator clock cycles can potentially corrupt the SDFM state machine, resulting in spurious comparator events, which can potentially trigger CPU interrupts, CLA tasks, ePWM XBAR events, and GPIO output X-BAR events if configured appropriately.

Workaround(s):

Avoid back-to-back writes within three SD-modulator clock cycles or have the SDCPARMx register bit fields configured in one register write.

i2356 *CONTROLSS-ADC: Interrupts may Stop if INTxCONT (Continue-to-Interrupt Mode) is not Set*

Details:

If ADCINTSELxNx[INTxCONT] = 0, then interrupts will stop when the ADCINTFLG is set and no additional ADC interrupts will occur. When an ADC interrupt occurs simultaneously with a software write of the ADCINTFLGCLR register, the ADCINTFLG will unexpectedly remain set, blocking future ADC interrupts.

Workaround(s):

1. Use Continue-to-Interrupt Mode to prevent the ADCINTFLG from blocking additional ADC interrupts:

   ADCINTSEL1N2[INT1CONT] = 1;

   ADCINTSEL1N2[INT2CONT] = 1;

   ADCINTSEL3N4[INT3CONT] = 1;

   ADCINTSEL3N4[INT4CONT] = 1;
2. Ensure there is always sufficient time to service the ADC ISR and clear the ADCINTFLG before the next ADC interrupt occurs to avoid this condition.
3. Check for an overflow condition in the ISR when clearing the ADCINTFLG. Check ADCINTOVF immediately after writing to ADCINTFLGCLR; if it is set, then write ADCINTFLGCLR a second time to ensure the ADCINTFLG is cleared. The ADCINTOVF register will be set, indicating an ADC conversion interrupt was lost.

i2356 (continued) ***CONTROLSS-ADC: Interrupts may Stop if INTxCONT (Continue-to-Interrupt Mode) is not Set***

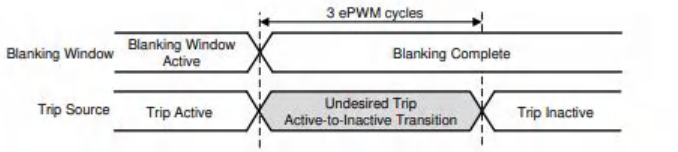
```
AdcaRegs.ADCINTFLGCLR.bit.ADCINT1 = 1; //clear INT1 flag
if(1 == AdcaRegs.ADCINTOVF.bit.ADCINT1) //ADCINT overflow
{
AdcaRegs.ADCINTFLGCLR.bit.ADCINT1 = 1; //clear INT1 again
// If the ADCINTOVF condition will be ignored by the application
// then clear the flag here by writing 1 to ADCINTOVFCLR.
// If there is a ADCINTOVF handling routine, then either insert
// that code and clear the ADCINTOVF flag here or do not clear
// the ADCINTOVF here so the external routine will detect the
// condition.
// AdcaRegs.ADCINTOVFCLR.bit.ADCINT1 = 1; // clear OVF
```

i2357 ***CONTROLSS-ePWM: An ePWM Glitch can Occur if a Trip Remains Active at the End of the Blanking Window***

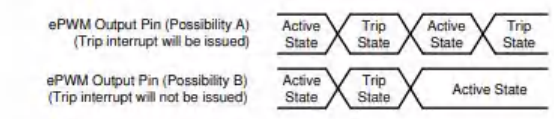
Details:

The blanking window is typically used to mask any PWM trip events during transitions which would be false trips to the system. If an ePWM trip event remains active for less than three ePWM clocks after the end of the blanking window cycles, there can be an undesired glitch at the ePWM output.

The following picture illustrates the time period which could result in an undesired ePWM output.



The following picture illustrates the two potential ePWM outputs possible if the trip event ends within 1 cycle before or 3 cycles after the blanking window closes.



Workaround(s):

Avoid configuration of blanking window such that the trip input would fall in this range (1 cycle before and 3 cycles after the blanking window closure).

i2358 ***CONTROLSS-ePWM: Trip Events Will Not be Filtered by the Blanking Window for the First 3 Cycles After the Start of a Blanking***

Details:

The Blanking Window will not blank trip events for the first 3 cycles after the start of a Blanking Window. DCEVTFILT may continue to reflect changes in the DCxEVTy signals. If

i2358 (continued) ***CONTROLSS-ePWM: Trip Events Will Not be Filtered by the Blanking Window for the First 3 Cycles After the Start of a Blanking***

DCEVTFILT is enabled, this may impact subsequent subsystems that are configured (for example, the Trip Zone submodule, TZ interrupts, ADC SOC, or the PWM output).

Workaround(s):

Start the Blanking Window 3 cycles before blanking is required. If a Blanking Window is needed at a period boundary, start the Blanking Window 3 cycles before the beginning of the next period. This works because Blanking Windows persist across period boundaries.

i2359 ***CONTROLSS-CMPSS:Prescaler counter behavior different from spec when DACSOURCE is made 0 or reconfigured as 1***

Details:

While the prescaler is running, if we make DACSOURCE = 0 the prescale counter will not reset, if the enable condition is LOW the value stays, and when the DACSOURCE is again configured as 1 the counter starts from the previous value which was retained. This bug is present only when DACSOURCE is configured during the prescale counter running.

Workaround(s):

Issue a soft reset between DACSOURCE configuration which is not a dynamic configuration.

i2374 ***PBIST fails if clock frequency of R5SS_CORE_CLK is not same as R5FSS_CLK_SELECTED frequency***

Details

The R5SS memories receive the R5SS CPU clock “R5SS_CORE_CLK” which is derived from R5SS_CLOCK_SELECTED root clock using programmable divider. When R5SS memories are tested using PBIST controller, the PBIST controller receives R5SS_CLOCK_SELECTED root clock. PBIST operation fails if different frequencies are chosen for the two clocks.

Workaround

For PBIST to work with R5SS memories the frequency of both clocks need to be same. If application usage requires R5SS_CORE_CLK to be a divided frequency of R5SS_CLOCK_SELECTED, then during PBIST operation of R5SS memories, the application shall ensure the R5SS_CORE_CLK is configured to same frequency as R5SS_CLOCK_SELECTED.

i2383 ***OSPI: 2-byte address is not supported in PHY DDR mode***

Details:

When the OSPI controller is configured for 2-byte addressing in PHY DDR Mode, an internal state machine mis-compares the number of address bytes transmitted to a value of 1 (instead of 2). This results in a state machine lockup in the address phase, rendering PHY DDR mode non-operable.

This issue does not occur when using any Tap mode or PHY SDR mode. This issue also doesn't occur when using 4 byte addressing in PHY DDR mode.

Workaround(s):

For compatible OSPI memories that have programmable address byte settings, set the amount of address bytes required from 2 to 4 on the flash. This may involve sending a specific command to change address bytes and/or writing a configuration register on the flash. Once done, update the amount of address bytes sent in the controller settings from 2 to 4.

For compatible OSPI memories that only support 2-byte addressing and cannot be re-programmed, PHY DDR mode will not be compatible with that memory. Alternative modes include:

PHY SDR mode

TAP (no-PHY) DDR mode

TAP (no-PHY) SDR mode

i2411 ***128 Bytes burst access is not supported for TCM***

Details:

Due to issue in the interconnect, 128 bytes burst access to TCM by any masters does not work as expected resulting in stale data.

Workaround(s)

Do not use 128bytes burst access. Please disable by all masters by software after reset.

i2412 ***USB can not generate interrupt upon DMA read/Write Access error***

Details:

USB does not have mechanism to generate error event / interrupt if its DMA R/W access sees read/write error response on VBUSM. This can happen if there is address/MPU error while accessing the memory, resulting in bus hang.

Workaround(s):

1. SW needs to program correct addresses for TRB’s and Data.
2. Use USB transfer time out and read following registers which log the bus error

GSTS. BUSERRADDRVLD (Host/Device Mode)
USBSTS.HSE (Host Mode)

i2427 ***RAM SEC can cause Spurious RAM writes resulting in L2 & MBOX memory corruption***

Details:

In case when a memory encounters a single-bit error during a RAM read data either due to a read or a partial write transaction, the RAM will enter a state which could lead to a later spurious write to the RAM if the next "memory read" is due to a subsequent partial write transaction. If the "memory read" is instead due to an actual memory read transaction, then the lingering bad internal state would be cleared and there wouldn't be

i2427 (continued) ***RAM SEC can cause Spurious RAM writes resulting in L2 & MBOX memory corruption***

any possibility of a later spurious write. The spurious write would be to the last memory address written prior to the partial write transaction which triggers the spurious write. The issue is only applicable to MBOX & L2.

Figure 2-1 lists possible scenarios where the issue is applicable (Example 1,2,3) and not applicable (Example 4,5,6) for more clarity. Transaction# are for illustration and doesn't necessarily represent the exact cycle each operation occurs. [SEC – Single bit Error Correction, DED – Double Bit Error Detection]

Ex #	Transaction 1	Transaction 2+N N=0,1,2,3..	Transaction 2+N+1	Transaction 2+N+2
1	Read or Partial Write Addr A (SEC) ← read with SEC	Full Write Addr X ← last write prior to partial write Note: N=0	Partial Write ← Triggers spurious write	Spurious write to Addr X with Transaction 1 corrected read data of Addr A
2	Read or Partial Write Addr A (SEC) ← read with SEC	Full Write Addr B Full Write Addr C Full Write Addr D ← last write prior to partial write Note: N=2	Partial Write ← Triggers spurious write	Spurious write to Addr D with Transaction 1 corrected read data of Addr A
3	Read or Partial Write Addr A (SEC)	Partial Write Addr B Note: N=0	Spurious write to Addr A with Transaction 1 corrected read data of Addr A (Addr A is overwritten with the RAM content prior to the Transaction 1 Partial write)	
4	Read Addr A (SEC)	Partial Write Addr B Note: N=0	No Spurious write to Addr A with Transaction 1 corrected read data of address A (no data corruption)	
5	Read or Partial Write Addr A (SEC)	Read ← Clears bad internal state Note: N=0	No spurious writes with all command combinations in subsequent cycles	
6	Read or Partial Write Addr A (SEC)	Full Write Addr B Note: N=0	Read ← Clears bad internal state	No spurious writes will all command combinations in subsequent cycles

Figure 2-1.

Workaround(s):

One of the below Options can be used as workaround.

Option 1:

Disable ECC, Applicable only for non-safety application.

Option 2:

Disallow Partial writes to the memory (only perform full line writes)

In case of L2, if the L2 space is cacheable the core will perform only full line writes and this issue is not applicable.

Option 3:

The application can treat all SEC errors like a DED (no correction only detection even in case of single bit error) since there is a possibility of RAM data corruption if application can't control the transactions immediately after a single bit error on a read or partial write transaction.

Note

Prior statements about using the ECC CTRL - SEC Counter as an indicator of normal SEC issue vs spurious write are NOT VALID. After a spurious write, the ECC CTRL SEC Counter can still be 1.

i2428 ***AES in DTHE generates extra dma request for data_in at the end of GCM encrypt***

Details:

The AES Engine produces an additional dma request for data input at the end of GCM cipher mode of Encryption. This issue only applies to Encryption with AES-GCM mode

i2428 (continued) ***AES in DTHE generates extra dma request for data_in at the end of GCM encrypt***

and it does not apply to AES-GCM Decryption or any other block cipher modes (for example CBC).

The extra DMA request goes away (deasserts) by itself after few cycles without any data written to it.

Depending on how the DMA in the system is set up for AES-GCM mode , the extra DMA request at the end of a packet transfer may cause unintended data transfer on the next packet.

Workaround(s):

None

i2433 ***ICSS: Reading the 64-bit IEP timer does not have a lock MSW logic when LSW is read***

Details:

IEPx 64-bit timestamp can be incorrect when lower 32-bit data is 0xFFFFFFFC or above (at 250MHz). In this case the upper 32-bit value is updated but lower value is the old number. The issue is seen when IEP counter (IEP_COUNT_REG1 : IEP_COUNT_REG0) is read back-to-back from ICSS PRU cores.

Example 1:

1st read : 0x000000D0(Upper):0xFFFFFFFC(lower)

2nd read : 0x000000D0(Upper):0x00000028(lower)

Example 2:

1st read : 0x000000D7(Upper):0xFFFFFFFC(lower)

2nd read : 0x000000D7(Upper):0x0000002C(lower)

Example 3:

1st read : 0x000000D6(Upper):0xFFFFFFF0(lower)

2nd read : 0x000000D7(Upper):0xFFFFFFFC((lower)

As shown above, this leads to timer increment behavior that is non-monotonic or timer differences to be unusually large as in Example 3 . This is due to 1 cycle race condition when loading 64-bit value from IEPx counter.

Workaround(s):

Note: these workarounds exist in SDK9.2 and later

Workaround in C for PRU:

```
uint64_t timestamp = (uint64_t) (0x2E0010);
```

/* Workaround starts here */

```
if ((timestamp & 0xFFFFFFFF) >= 0xFFFFFFFC)
{     timestamp = *(uint64_t*) (0x2E0010); }
```

/* Workaround ends here */

i2433 (continued) ***ICSS: Reading the 64-bit IEP timer does not have a lock MSW logic when LSW is read***

Workaround in assembly for PRU:

```
 ldi32 r4, 0xFFFFFFFC ; 0-4 for 250MHz clock
    ;load 64-bit timestamp to r2:r3
    lbco &r2, c26, 0x10, 8
    qbgt skip_iep_read_errata. r2, r4
    ;re-read IEP if IEP_COUNTER_LOW >= 0xFFFF_FFFC
    lbco &r2, c26, 0x10, 8
skip_iep_read_errata:
```

Workaround in C for R5F, A53:

```
uint64_t getIepTimeStamp64 (void)
{
    uint64_t u64Timestamp1 = (volatile uint64_t)(0x300AE010);
    uint64_t u64Timestamp2 = (volatile uint64_t)(0x300AE010);
    if (u64Timestamp2 > u64Timestamp1)
    {
#ifdef __DEBUG
        if (((u64Timestamp2 >> 32)-(u64Timestamp1 >> 32)) == 1)
        {
            /* HW errata fixed due to picking u64Timestamp1*/
            if ((u64Timestamp2 & 0xFFFFFFFF) >= (u64Timestamp1 & 0xFFFFFFFF))


{                 DebugP_log ("Errata fixed (1): %llx : %llx\r\n",
        u64Timestamp1, u64Timestamp2);             }

        }
#endif
        return u64Timestamp1;
    }
    else
    {
#ifdef __DEBUG
        if ((u64Timestamp2 & 0xFFFFFFFF) < (u64Timestamp1 & 0xFFFFFFFF))


{             /* Adjust the IEP MSW in the case running into HW errata
*/
    DebugP_log ("Errata fixed (2): %llx : %llx\r\n", u64Timestamp1,
u64Timestamp2);         }

#endif
        /* HW errata fixed due to picking u64Timestamp2*/
        return u64Timestamp2;
    }
}
```

i2439 ***CPSW: Host to Ethernet Timestamp Accuracy Issue***

Details:

When a packet is sent from the Host to Ethernet with a timestamp to be generated on Ethernet egress, a packet length with 0xD5 in the lower 8-bits results in a timestamp error.

Using timestamp for PTP messages should not be impacted as the PTP messages are usually much shorter than 0xD5 packet length.

Workaround(s):

Ethernet timestamp should be enabled only for PTP messages on Host Tx.

i2440 ***CPSW: Host to Ethernet Timestamp Sequence ID issue***

Details:

For host to Ethernet packets with timestamp enabled, certain scenarios can cause the Sequence ID associated with a timestamp to be incorrect. The timestamp is correct but the sequence ID is incorrect. The host would use the sequence ID to correlate the packet with the timestamp. The issue does not affect PTP messages.

Workaround(s):

For host to Ethernet, packets with timestamp should be disabled.

i2479 ***OSPI Boot Issue with GPIO61 Reset Pin Configuration***

Details:

During OSPI boot mode, including fallback modes that would result in OSPI boot mode, ROM configures pin GPIO61 as OSPI0_RESET_OUT0. If this pin is connected to the Reset pin of the OSPI Flash Memory, boot failures may occur due to a reset signal management issue in the OSPI controller.

During OSPI boot mode, the ROM code:

1. Configures GPIO61 in OSPI0_RESET_OUT0 mux mode
2. Correctly asserts the reset signal (drives low)
3. Fails to de-assert the reset signal due to incorrect OSPI controller configuration (GPIO61 pin remains driven low)

If GPIO61 is connected to the Flash Memory Reset pin, the flash device remains in reset state. This prevents proper boot sequence completion. This issue affects all package types where GPIO61 is utilized for OSPI Flash reset control.

Workaround(s):

Option 1: Do not use GPIO61 pin to reset the flash. Use PORz/WARMRSTn to reset the flash device on a power cycle and use another GPIO for OSPI0_REST_OUT0 and pass that signal through an AND gate with PORz/WARMRSTn. See AM261x OSPI Reset using any OSPI0_RESET_OUT0 pin AND PORz/WARMRSTn for an example.

Option 2: Gate GPIO61 to prevent propagation to the reset logic during boot, then AND that signal with PORz/WARMRSTn to use as a reset during power cycles for the flash device. One example implementation is shown in AM261x OSPI Reset using Gated GPIO61 pin AND PORz/WARMRSTn.

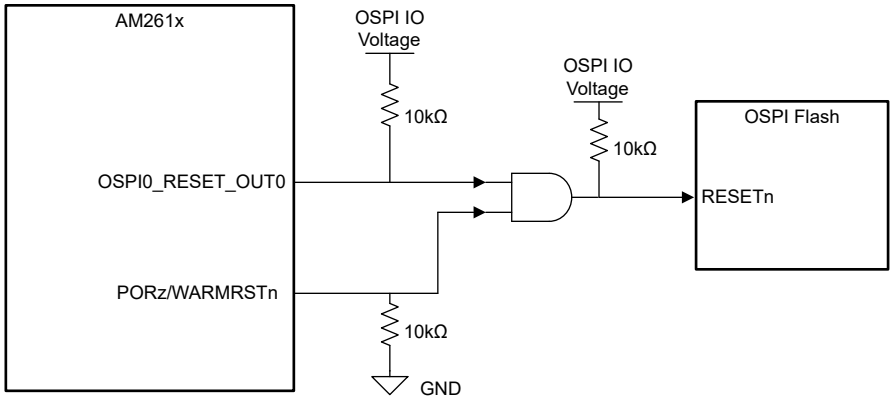


Figure 2-2. AM261x OSPI Reset using any OSPI0_RESET_OUT0 pin AND PORz/WARMRSTn

i2479 (continued) ***OSPI Boot Issue with GPIO61 Reset Pin Configuration***

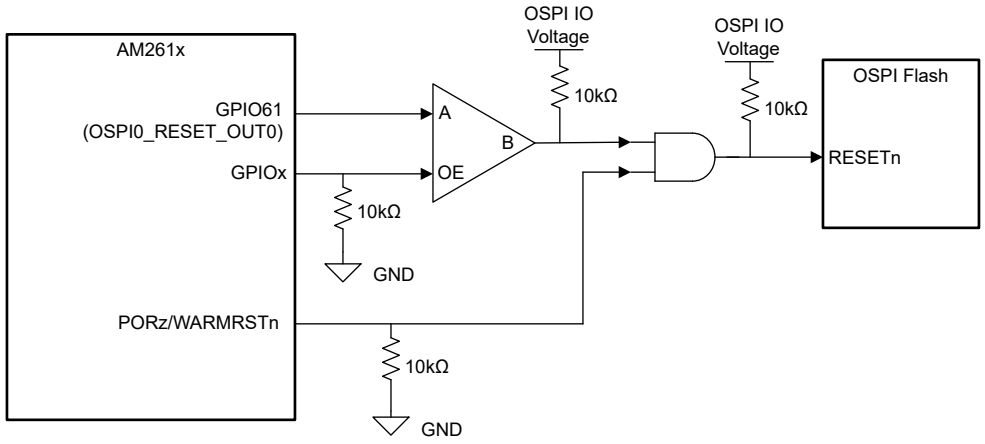


Figure 2-3. AM261x OSPI Reset using Gated GPIO61 pin AND PORz/WARMRSTn

i2480 ***1µs glitch on GPIO61/OPSI0_RESET_OUT0 during OSPI Boot***

Details:

During OSPI boot mode, including fallback modes that would result in OSPI boot mode, ROM configures pin GPIO61 as OSPI0_RESET_OUT0. If this pin is connected to the Reset pin of the OSPI Flash Memory, boot failures may occur due to a reset signal management issue in the OSPI controller.

During OSPI boot mode, the ROM code:

1. Configures GPIO61 in OSPI0_RESET_OUT0 mux mode
2. Correctly asserts the reset signal (drives low)
3. Fails to de-assert the reset signal due to incorrect OSPI controller configuration (GPIO61 pin remains driven low)

If GPIO61 is connected to the Flash Memory Reset pin, the flash device remains in reset state. This prevents proper boot sequence completion. This issue affects all package types where GPIO61 is utilized for OSPI Flash reset control. In addition, GPIO61 will remain low until user application reconfigures it.

Workaround(s):

Option 1: None. Do not use GPIO61 pin.

Option 2: User application code can reconfigure this pin in case this pin needs to be utilized. But if the application is glitch sensitive, ensure that the glitch does not affect connected peripherals by including appropriate filtering in external circuitry.

3 Trademarks

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from November 7, 2024 to April 30, 2025 (from Revision * (November 2024) to Revision A (April 2025)) **Page**

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