TMS320VC5506

Digital Signal Processor

Silicon Errata

SPRZ271A
August 2008 − Revised August 2008

REVISION HISTORY

This revision history highlights the technical changes made to SPRZ271 to generate SPRZ271A.

Scope: Deleted Advisory HWA_1 Pixel Interpolation Hardware Accelerator

PAGE(S) NO.	ADDITIONS/CHANGES/DELETIONS
8	Table 2. Quick Reference: −Deleted Hardware Accelerator row and Advisory HWA_1 Pixel Interpolation Hardware Accelerator row
26	Deleted Section 3.12 Hardware Accelerator and Advisory HWA_1 Pixel Interpolation Hardware Accelerator

Contents

1 Introduction

This document describes the silicon updates to the functional specifications for the TMS320VC5506. The updates are applicable to:

- TMS320VC5506 (144-pin LQFP, PGE suffix)
- TMS320VC5506 (179-pin MicroStar BGA™, GHH suffix)

The advisory numbers in this document are not always sequential. Some advisory numbers have been removed as they do not apply to the device revisions specified in this document. When items are moved or deleted, the remaining numbers remain the same and are not resequenced.

Issues related to CPU operation are documented in the *TMS320C55x DSP CPU Programmer's Reference Supplement* (literature number SPRU652).

1.1 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., **TMS320VC5506**). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

TMS Fully qualified production device

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

1.2 Revision Identification

The device revision can be determined by the lot trace code marked on the top of the package. The locations for the lot trace codes for the PGE and the GHH packages are shown in Figure 1 and Figure 2, respectively. The location of other markings may vary per device.

Qualified devices in the PGE and GHH packages are marked with the letters “TMS” at the beginning of the device name, while nonqualified devices are marked with the letters “TMX” or “TMP” at the beginning of the device name.

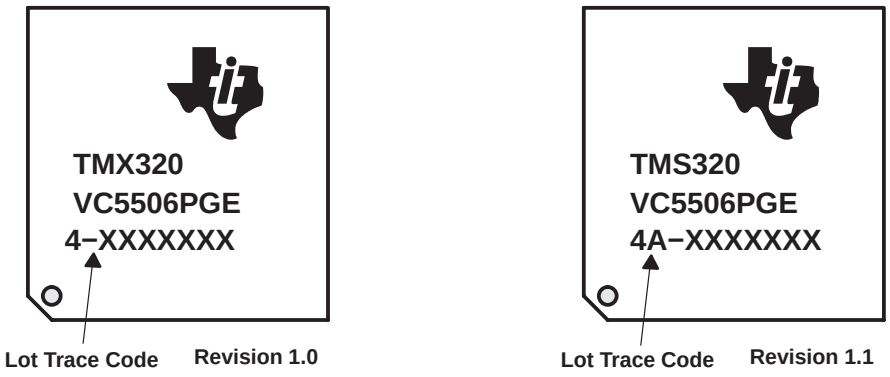

Figure 1. Example Markings for VC5506, PGE Package, Revisions 1.0 and 1.1

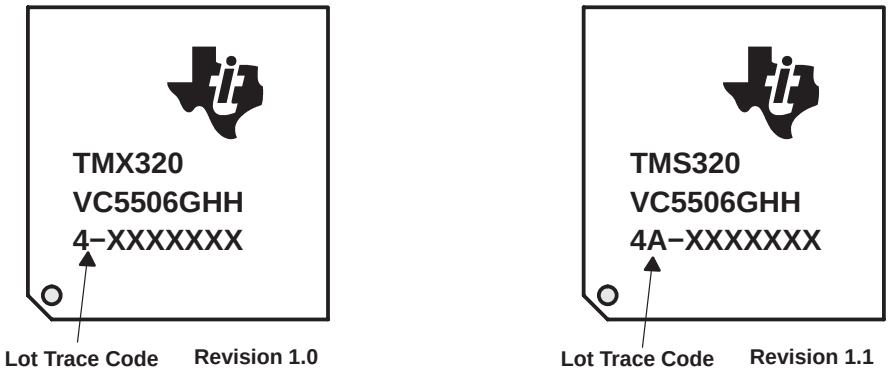

Figure 2. Example Markings for VC5506, GHH Package, Revisions 1.0 and 1.1

Table 1. Determining Silicon Revision From Lot Trace Code

Lot Trace Code	Silicon Revision
Blank (no second letter in prefix)	Indicates Original Silicon (1.0)
A (second letter in prefix is A)	Indicates Silicon Revision A (1.1)

2 Usage Notes

Usage Notes highlight and describe particular situations where the device's behavior may not match the presumed or documented behavior. This may include behaviors that affect device performance or functional correctness. These notes will be incorporated into future documentation updates for the device (such as the device-specific data sheet), and the behaviors they describe will not be altered in future silicon revisions.

RTC: Seconds Alarm Functionality

On the 5506 device, the Seconds Alarm Register (RTCSECA) *cannot* be used to generate an alarm every second, but the update-ended interrupt can.

The Real-Time Clock (RTC) executes an update cycle once per second to update the current time in the time/calendar registers:

- Seconds Register (RTCSEC)
- Minutes Register (RTCMIN)
- Hours Register (RTCHOUR)
- Day of the Week and Day Alarm Register (RTCDAYW)
- Day of the Month (Date) Register (RTCDAYM)
- Month Register (RTCMONTH)
- Year Register (RTCYEAR)

At the end of every update cycle, the RTC sets the update-ended interrupt flag (UF) in the Interrupt Flag Register (RTCINTFL). If the update-ended interrupt enable bit (UIE) in the Interrupt Enable Register (RTCINTEN) is set to 1, an interrupt request is sent to the CPU.

3 Known Design Marginality/Exceptions to Functional Specifications

3.1 Summary of Advisories

Table 2 provides a quick reference of all advisories by number, silicon revision affected, and lists their respective page location.

Table 2. Quick Reference

Advisory Number	Advisory	Revision(s) Affected	Page
Device-Level Advisories			
DL_2	Software Modification of MPNMC Bit is Not Pipeline-Protected	1.0 and 1.1	10
DL_7	RETI Instruction may Affect the XF State	1.0 and 1.1	10
DL_10	First Word of Data on Consecutive DMA Transmissions Using McBSP is Lost	1.0 and 1.1	11
Bootloader Advisories			
BL_3	USB Bootloader Returns Incorrect DescriptorType Value When String Descriptors are Requested by the Host	1.0 and 1.1	12
BL_4	USB Bootloader Returns Incorrect PID During Enumeration Phase	1.0 and 1.1	12
Direct Memory Access (DMA) Advisories			
DMA_1	Early Sync Event Stops Block Transfer	1.0 and 1.1	13
DMA_2	DMA Does Not Support Burst Transfers From EMIF to EMIF	1.0 and 1.1	13
External Memory Interface (EMIF) Advisories			
EMIF_8	ARDY Pin Requires Strong Pullup Resistor	1.0 and 1.1	14
EMIF_9	External Memory Write After Read Reversal	1.0 and 1.1	14
EMIF_10	Block Write Immediately Following a Block Read May Cause Data Corruption	1.0 and 1.1	15
EMIF_11	EMIF Asynchronous Access Hold = 0 is Not Valid for Strobe > 3	1.0 and 1.1	15
EMIF_12	8-Bit Asynchronous Writes on 5506 EMIF Not Supported	1.0 and 1.1	16
EMIF_13	After Changing CE Control Registers and Disabling SDRAM Clock in Divide-by-8 and Divide-by-16 Modes, Asynchronous Access Followed by SDRAM Access Will Not Supply a Ready Signal to CPU	1.0 and 1.1	16
EMIF_14	SETUP = 2 Configuration is not Valid for Asynchronous Memory	1.0 and 1.1	16
Real-Time Clock (RTC) Advisories			
RTC_3	RTC Interrupts are Perceived by the User as Happening One Second Before	1.0 and 1.1	18
RTC_4	Any Year Ending in 00 Will Appear as a Leap Year	1.0 and 1.1	18
RTC_5	Midnight and Noon Transitions Do Not Function Correctly in 12h Mode	1.0 and 1.1	19
Universal Serial Bus (USB) Advisories			
USB_2	CPU Might Miss Back-to-Back USB Interrupts When CPU Speed is Less Than or Equal to 24 MHz	1.0 and 1.1	20
USB_5	USB Input Cell Does Not Power Down When USB is Placed in IDLE	1.0 and 1.1	20
USB_6	CPU Read/Write to USB Module may Return Incorrect Result if the USB Clock is Running Slower Than Recommended Speed (48 MHz)	1.0 and 1.1	20
Inter-Integrated Circuit (I^2C) Advisories			
I2C_3	ARDY Interrupt is not Generated Properly in Non-Repeat Mode if STOP Bit is Set	1.0 and 1.1	21
I2C_5	Repeated Start Mode Does Not Work	1.0 and 1.1	21
I2C_6	Bus Busy Bit Does Not Reflect the State of the I^2C Bus When the I^2C is in Reset	1.0 and 1.1	22

Table 2. Quick Reference (Continued)

Advisory Number	Advisory	Revision(s) Affected	Page
I2C_8	DMA Receive Synchronization Pulse Gets Generated Falsely	1.0 and 1.1	22
Multichannel Buffered Serial Port (McBSP) Advisories			
MCBSP_1	McBSP May Not Generate a Receive Event to DMA When Data Gets Copied From RSR to DRR	1.0 and 1.1	23
Emulation Advisories			
EMU_1	Emulation Prone to Failure Under Certain Situations	1.0 and 1.1	24
Power Management Advisories			
PM_1	Repeated Interrupts During CPU Idle	1.0 and 1.1	26

3.2 Device-Level Advisories

Advisory DL_2	*Software Modification of MPNMC Bit is Not Pipeline-Protected*

Revision(s) Affected: 1.0 and 1.1

Details: Software modification of the MPNMC bit in status register 3 (ST3_55) is not pipeline-protected so changes to the device memory map may not become valid before the instructions that immediately follow the modification.

Assembler Notification: None

Workaround: Insert six NOPs after the MPNMC modification.

Advisory DL_7	*RETI Instruction may Affect the XF State*

Revision(s) Affected: 1.0 and 1.1

Details: The XF pin state is saved on the stack as a part of the ST1 context saving during interrupts servicing. If the XF pin state is changed inside the ISR, upon execution of the RETI, the XF bit will be restored to the value prior to entering the ISR. If XF state is not changed inside the ISR, then there is no issue.

Assembler Notification: None

Workaround: BIOS takes care of this problem with software workaround, which is transparent to the users. Non-BIOS users who are changing XF pin state in an ISR should also modify the ST1 value on the stack to maintain the correct XF pin state upon exiting the ISR.

Advisory DL_10	*First Word of Data on Consecutive DMA Transmissions Using McBSP is Lost*

Revision(s) Affected: 1.0 and 1.1

Details: When executing multiple DMA transfers consecutively using the same DMA Transmit Channel and McBSP, an extra DMA TX request generated by the McBSP at the end of the first transfer will not be serviced by the DMA until the next DMA transfer is initiated by the McBSP. At the next DMA transfer, this DMA TX request will be serviced as soon as the DMA TX channel is enabled.

This transmitted data will remain valid on the bus as long as the McBSP is disabled. However, once the McBSP is enabled, it sends out another DMA TX request, and the DMA transmits the second word. This results in the loss of the first word of data on consecutive DMA transmissions.

Assembler Notification: None

Workaround: Only the systems where McBSP is turned off following each block of DMA transfer are affected. In such case, a dummy DMA transfer with the DMA synchronization event set to no sync event will flush out the pending TX request from the McBSP before programming the DMA to send the next block of data to the McBSP.

3.3 Bootloader Advisories

Advisory BL_3	*USB Bootloader Returns Incorrect DescriptorType Value When String Descriptors are Requested by the Host*

Revision(s) Affected: 1.0 and 1.1

Details: When the host requests for the string descriptor, the USB bootloader returns 0x00 for DescriptorType value instead of 0x03.

Assembler Notification: None

Workaround: Ignore the DescriptorType returned by the DSP. String Descriptor is not necessary for successfully bootloading the device through the USB.

Advisory BL_4	*USB Bootloader Returns Incorrect PID During Enumeration Phase*

Revision(s) Affected: 1.0 and 1.1

Details: The correct PID is 0x9003; however, the bootloader reports 0x9001 to the host.

Assembler Notification: None

Workaround: PID 0x9001 belongs to 5509. Both 5509 and 5506 USB bootloader work the same way; hence, the incorrect PID does not affect the functionality of the USB bootmode.

3.4 Direct Memory Access (DMA) Advisories

Advisory DMA_1	*Early Sync Event Stops Block Transfer*

Revision(s) Affected: 1.0 and 1.1

Details: When a DMA block transfer is initiated by a sync event, if the same sync event occurs before the last element of the block transfer has been completed, an event drop occurs and the channel becomes disabled.

Assembler Notification: None

Workaround: Ensure that the duration between the sync events is long enough to allow the block transfer to complete. The DMA end-of-block interrupt can be used as an indicator.

Advisory DMA_2	*DMA Does Not Support Burst Transfers From EMIF to EMIF*

Revision(s) Affected: 1.0 and 1.1

Details: The DMA controller does not support burst mode transfers with the EMIF as both the source and the destination port.

Assembler Notification: None

Workaround: Do not use burst mode for EMIF-to-EMIF transfers.

3.5 External Memory Interface (EMIF) Advisories

Advisory EMIF_8 — *ARDY Pin Requires Strong Pullup Resistor*

Revision(s) Affected: 1.0 and 1.1

Details: When the parallel bus is used to access external memory, a strong pullup resistor is required for the ARDY pin for the asynchronous memory interface.

Assembler Notification: None

Workaround: Pull up ARDY with a 2.2-kΩ resistor.

Advisory EMIF_9 — *External Memory Write After Read Reversal*

Revision(s) Affected: 1.0 and 1.1

Details: If an external memory write is followed immediately by an external memory read, the external memory read will occur first, followed by the write. See the example below.

Example:

```
MOV    #1770h, *(100001h)  ; External Memory Write
MOV    *(#100000h), AR1    ; External Memory Read
```

Assembler Notification: None

Workaround: Insert two NOPs between the memory write/read pair.

Example:

```
MOV    #1770h, *(100001h)  ; External Memory Write
NOP
NOP
MOV    *(#100000h), AR1    ; External Memory Read
```

Advisory EMIF_10 — *Block Write Immediately Following a Block Read May Cause Data Corruption*

Revision(s) Affected: 1.0 and 1.1

Details: When performing a block write immediately following a block read, data may get corrupted. See the example below.

Example:

```
Write 0x55 to addr1
Write 0xAA to addr2
Read addr1
Read addr2
```

When executed, the above code will follow this order:

```
Write 0x55 to addr1
Read addr1
Write 0xAA to addr2
Read addr2
```

Assembler Notification: None

Workaround: Insert two NOPs between write and read. Since reads occur before writes in the pipeline, the read must be delayed after the write so that the read does not occur before the write.

Advisory EMIF_11 — *EMIF Asynchronous Access Hold = 0 is Not Valid for Strobe > 3*

Revision(s) Affected: 1.0 and 1.1

Details: For asynchronous EMIF accesses, a hold time of 0 is not valid for strobe lengths greater than 3 cycles if the ARDY_OFF bit is not set. If the above configuration is used but the ARDY_OFF bit is clear, then the EMIF automatically gives a hold time of 1 cycle.

Assembler Notification: None

Workaround: None

Advisory EMIF_12

8-Bit Asynchronous Writes on 5506 EMIF Not Supported

Revision(s) Affected: 1.0 and 1.1

Details: 8-bit asynchronous writes are not supported; however, 8-bit asynchronous reads *are* supported.

Assembler Notification: None

Workaround: None

Advisory EMIF_13

After Changing CE Control Registers and Disabling SDRAM Clock in Divide-by-8 and Divide-by-16 Modes, Asynchronous Access Followed by SDRAM Access Will Not Supply a Ready Signal to CPU

Revision(s) Affected: 1.0 and 1.1

Details: If the SDRAM clock (EMIF.CLKMEM) is set to divide-by-8 and divide-by-16 of the CPU clock and if the user disables the SDRAM clock before accessing asynchronous memory, the EMIF will fail to supply the ready signal to the CPU under the following two conditions:

- Case 1:
  SDRAM access
  Switch off the SDRAM clock
  Change CE Space Control Register to Asynchronous Mode
  Perform an asynchronous access to the *same* CE space
- Case 2:
  SDRAM access
  Switch off the SDRAM clock
  Change CE Space Control Register to Asynchronous Mode
  Perform an asynchronous access to a *different* CE space

This failure of the ready signal will make the CPU wait indefinitely.

Assembler Notification: None

Workaround: Switch the SDRAM clock to divide-by-1 before programming the CE Space Control Register to asynchronous memory.

Advisory EMIF_14	*SETUP = 2 Configuration is not Valid for Asynchronous Memory*

Revision(s) Affected: 1.0 and 1.1

Details: When using the EMIF in asynchronous memory mode, a read or write SETUP time setting of two clocks actually behaves like timing of one clock of setup time.

Assembler Notification: None

Workaround: If a read setup time of two clocks is required for asynchronous memory, a value of three clock cycles must be used.

3.6 Real-Time Clock (RTC) Advisories

Advisory RTC_3	*RTC Interrupts are Perceived by the User as Happening One Second Before*

Revision(s) Affected: 1.0 and 1.1

Details: When the user reads the Real Time Clock time register, these register are read one second after the RTC's internal timer counter register. The RTC interrupts are triggered by the internal counter register, thus it seems to the user that the interrupt was triggered one second earlier. For example, an alarm set to every minute alarm generates an interrupt at xx:xx:59 instead of xx:xx:00.

Assembler Notification: None

Workaround: Take into account the one second difference when using the alarm interrupt.

Advisory RTC_4	*Any Year Ending in 00 Will Appear as a Leap Year*

Revision(s) Affected: 1.0 and 1.1

Details: Since the year can be varied from 00−99 only, any year ending with 00 will always appear as a Leap Year, which is not always the case. For example, 2100 ends in 00 and is not a Leap Year.

Assembler Notification: None

Workaround: None

Advisory RTC_5	*Midnight and Noon Transitions Do Not Function Correctly in 12h Mode*

Revision(s) Affected: 1.0 and 1.1

Details: The normal transition from Midnight and Noon should be the following:

11:59am → 12:00pm → 12:59pm → 1:00pm

11:59pm → 12:00am → 12:59am → 1:00am

However, if the RTC is used in the 12h time format, the transitions around Noon and Midnight are as below:

11:59am → 12:00am → 12:59am → 1:00pm

11:59pm → 12:00pm → 12:59pm → 1:00am

Assembler Notification: None

Workaround: The problem can be worked around using the 24h mode.

3.7 Universal Serial Bus (USB) Advisories

Advisory USB_2	*CPU Might Miss Back-to-Back USB Interrupts When CPU Speed is Less Than or Equal to 24 MHz*

Revision(s) Affected: 1.0 and 1.1

Details: When the CPU operates with a clock less than or equal to half the USB module clock, back-to-back USB interrupts might be missed by the CPU. Back-to-back interrupts occur when multiple endpoints are active simultaneously or when SOF or SETUP events occur with one endpoint. The USB module needs to operate at 48 MHz, so the CPU needs to operate at a clock speed greater than 24 MHz.

Assembler Notification: None

Workaround: Recommended CPU operating frequency is 48 MHz or higher if the USB module is running.

Advisory USB_5	*USB Input Cell Does Not Power Down When USB is Placed in IDLE*

Revision(s) Affected: 1.0 and 1.1

Details: USB input cells are always powered unless the oscillator is disabled.

Assembler Notification: None

Workaround: None

Advisory USB_6	*CPU Read/Write to USB Module may Return Incorrect Result if the USB Clock is Running Slower Than Recommended Speed (48 MHz)*

Revision(s) Affected: 1.0 and 1.1

Details: If the CPU speed is x12 or higher than the USB module clock speed, then the USB RAM and register read/write will return incorrect result. This is not an issue during normal USB operation where the USB module clock is 48 MHz. But at power up, the USB DPLL is in bypass div2 mode; hence, the USB module clock is CLKIN/2. As most of the applications program the DSP PLL first and then all other modules (including USB), this can be a problem if the (CPU clock):(USB module clock) ratio > 12:1.

Assembler Notification: None

Workaround: Program the USB PLL first to speed up the USB module clock to 48 MHz before programming the DSP PLL.

3.8 Inter-Integrated Circuit (I^2C) Advisories

Advisory I2C_3	*ARDY Interrupt is not Generated Properly in Non-Repeat Mode if STOP Bit is Set*

Revision(s) Affected: 1.0 and 1.1

Details: In non-repeat mode, if the STP bit of ICMDR is set, the master sends the STOP condition and does not assert ARDY interrupt after sending data. If the STP bit is set, the I^2C sends the STOP condition and clears the ARDY bit.

Assembler Notification: None

Workaround: If the ARDY interrupt is desired after sending data, start the data transfer without setting the STP bit. If the STOP bit is not set beforehand, the master will not send the STOP condition and asserts the ARDY interrupt after sending the data. Set the STP bit when the last ARDY interrupt arrives (all data sent out).

Advisory I2C_5	*Repeated Start Mode Does Not Work*

Revision(s) Affected: 1.0 and 1.1

Details: Repeated Start Mode does not work on the I^2C peripheral.

Assembler Notification: None

Workaround: None

Advisory I2C_6

Bus Busy Bit Does Not Reflect the State of the I2C Bus When the I2C is in Reset

Revision(s) Affected: 1.0 and 1.1

Details: The Bus Busy bit (BB) indicates the status of the I2C bus. The Bus Busy bit is set to '0' when the bus is free and set to '1' when the bus is busy. The I2C peripheral cannot detect the state of the I2C bus when it is in reset (IRS bit is set to '0'); therefore, the Bus Busy bit will keep the state it was at when the peripheral was placed in reset. The Bus Busy bit will stay in that state until the I2C peripheral is taken out of reset (IRS bit set to '1') and a START condition is detected on the I2C bus. When the device is powered up, the Bus Busy bit will stay stuck at the default value of '0' until the IRS bit is set to '1' and the I2C peripheral detects a START condition.

Systems using a multi-master configuration can be affected by this issue.

Assembler Notification: None

Workaround: Wait a certain period after taking the I2C peripheral out of reset (setting the IRS bit to '1') before starting the first data transfer. The period should be set equal to or larger than the total time it takes for the longest data transfer in the application. By waiting this amount of time, it can be ensured that any previous transfers finished. After this point, BB will correctly reflect the state of the I2C bus.

Advisory I2C_8

DMA Receive Synchronization Pulse Gets Generated Falsely

Revision(s) Affected: 1.0 and 1.1

Details: When receiving an I2C data stream in master mode (i.e., a read is performed), and the DMA is started, a DMA synchronization event is triggered upon enabling the DMA channel if a byte is present in the DRR (even if it has already been read). This leads to the first byte read being a duplicate of the previous byte that was already read from the DRR.

Assembler Notification: None

Workaround: Set DMA transfers from DRR to read one more byte than necessary and discard the first byte.

3.9 Multichannel Buffered Serial Port (McBSP) Advisories

Advisory MCBSP_1 — *McBSP May Not Generate a Receive Event to DMA When Data Gets Copied From RSR to DRR*

Revision(s) Affected: 1.0 and 1.1

Details: When there is heavy peripheral activity, and the DRR is read, a new receive interrupt might not be generated to the DMA when data in the RSR is copied to the DRR. When this condition occurs, the McBSP overwrites the DRR before the DMA had an opportunity to read its value.

This problem arises when the DRR read occurs at the “exact moment” the REVT needs to be generated. The DRR servicing gets delayed if there are other heavy DMA channels or CPU activities on the peripheral bus.

Assembler Notification: None

Workaround: Optimize the peripheral bus access by the CPU and the DMA by carefully scheduling the DMA and CPU activities so the DMA channel servicing the DRR is not stalled to the point where new data is about the move in the DRR.

3.10 Emulation Advisories

Advisory EMU_1	*Emulation Prone to Failure Under Certain Situations*

Revision(s) Affected: 1.0 and 1.1

Details:

Under certain conditions, the emulation hardware may corrupt the emulation control state machine or may cause it to lose synchronization with the emulator software. When emulation commands fail as a result of the problem, Code Composer Studio™ Integrated Development Environment (IDE) may be unable to start or it may report errors when interacting with the TMS320C55x™ DSP (for example, when halting the CPU, reaching a breakpoint, etc.).

This phenomenon is observed when an erroneous clock edge is generated from the TCK signal inside the C55x™ DSP. This can be caused by several factors, acting independently or cumulatively:

- TCK transition times (as measured between 2.5 V and 0.6 V) in excess of 3 ns.
- Operating the C55x DSP in a socket, which can aggravate noise or glitches on the TCK input.
- Poor signal integrity on the TCK line from reflections or other layout issues.

A TCK edge that can cause this problem might look similar to the one shown in Figure 3. A TCK edge that does not cause the problem will look similar to the one shown in Figure 4. The key difference between the two figures is that Figure 4 has a clean and sharp transition whereas Figure 3 has a “knee” in the transition zone. Problematic TCK signals may not have a knee that is as pronounced as the one in Figure 3. Due to the TCK signal amplification inside the chip, any perturbation of the signal can create erroneous clock edges.

As a result of the faster edge transition, there is increased ringing in Figure 4. As long as the ringing does not cross logic input thresholds (0.6 V for falling edges, and 2.5 V for rising edges), this ringing is acceptable.

When examining a TCK signal for this issue, either in board simulation or on an actual board, it is very important to probe the TCK line as close to the DSP input pin as possible. In simulation, it should not be difficult to probe right at the DSP input. For most physical boards, this means using the via for the TCK pad on the back side of the board. Similarly, ground for the probe should come from one of the nearby ground pad vias to minimize EMI noise picked up by the probe.

Emulation Prone to Failure Under Certain Situations (Continued)

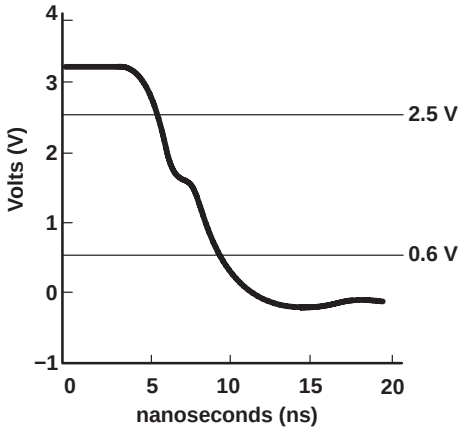

Figure 3. Bad TCK Transition

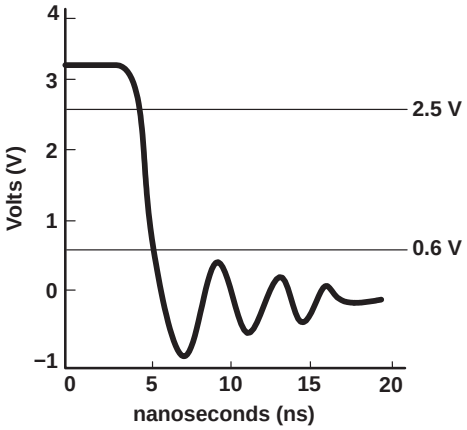

Figure 4. Good TCK Transition

Workaround: As the problem may be caused by one or more of the above factors, one or more of the steps outlined below may be necessary to fix it:

- Avoid using a socket
- Ensure the board design achieves rise times and fall times of less than 3 ns with clean monotonic edges for the TCK signal.
- For designs where TCK is supplied by the emulation pod, use a C55x Emulation Adapter Board, part number DSP8102U. To order a C55x Emulation Adapter Board, please contact the TI Product Information Center (PIC).

3.11 Power Management Advisories

Advisory PM_1	*Repeated Interrupts During CLKGEN Domain Idle*

Revision(s) Affected: 1.0 and 1.1

Details: Any external interrupt staying low for an extended period should generate only one interrupt. The interrupt signal should normally be required to go high, then low again before additional interrupts would be generated. However, on the 5506, if the external interrupt stays low while the CLKGEN domain enters the idle state, the associated interrupt flag is set again. This causes the CPU to exit the idle state, and if the associated interrupt enable bit is set, the interrupt service routine will also be executed.

In case of CLKGEN in idle and the external interrupt is driven low to wake up the CPU, repeated interrupt will be generated until the external interrupt signal driven high after the CPU wakes up.

When the CPU is not in idle, the interrupt responds as expected (only a single interrupt is generated).

Assembler Notification: None

Workaround: Limit the low pulse durations of external interrupts so that they are not still asserted when the CLKGEN goes into idle or when waking up the CPU from idle.

4 Documentation Support

For device-specific data sheets and related documentation, visit the TI web site at: **http://www.ti.com.**

For further information regarding the TMS320VC5506, please see the latest versions of:

- *TMS320C55x DSP CPU Reference Guide* (literature number SPRU371)
- *TMS320C55x DSP Mnemonic Instruction Set Reference Guide* (literature number SPRU374)
- *TMS320C55x DSP Algebraic Instruction Set Reference Guide* (literature number SPRU375)
- *TMS320C55x DSP Peripherals Overview Reference Guide* (literature number SPRU317)
- *TMS320VC5506 Fixed-Point Digital Signal Processor* data manual (literature number SPRS375)
- *TMS320C55x DSP CPU Programmer's Reference Supplement* (literature number SPRU652)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Clocks and Timers	www.ti.com/clocks	Digital Control	www.ti.com/digitalcontrol
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265