TMS320C6414T, TMS320C6415T, TMS320C6416T Digital Signal Processors Silicon Revision 2.0, 1.0

Silicon Errata

Literature Number: SPRZ216J
December 2003–Revised July 2012

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1 Introduction

This document describes the known exceptions to the functional specifications for the TMS320C6414T, TMS320C6415T, and TMS320C6416T digital signal processors. [See the *TMS320C6414T, TMS320C6415T, TMS320C6416T Fixed-Point Digital Signal Processors* data sheet (literature number SPRS226).] Throughout this document, TMS320C64x, C64x, C641xT, and C6414T/15T/16T refer to *TMS320C6414T*, *TMS320C6415T*, and *TMS320C6416T* devices.

For additional information, see the latest version of the *TMS320C6000 DSP Peripherals Overview Reference Guide* (literature number SPRU190).

This document also contains “Usage Notes”. Usage Notes highlight and describe particular situations where the device’s behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness. These notes will be incorporated into future documentation updates for the device (such as the device-specific data sheet), and the behaviors they describe will not be altered in future silicon revisions.

1.1 Device and Development Support-Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., **TMS**320C6415TGLZ7). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX / TMDX) through fully qualified production devices/tools (TMS / TMDS).

Device development evolutionary flow:

TMX — Experimental device that is not necessarily representative of the final device's electrical specifications.

TMP — Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

TMS— Fully qualified production device.

Support tool development evolutionary flow:

TMDX — Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS — Fully qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

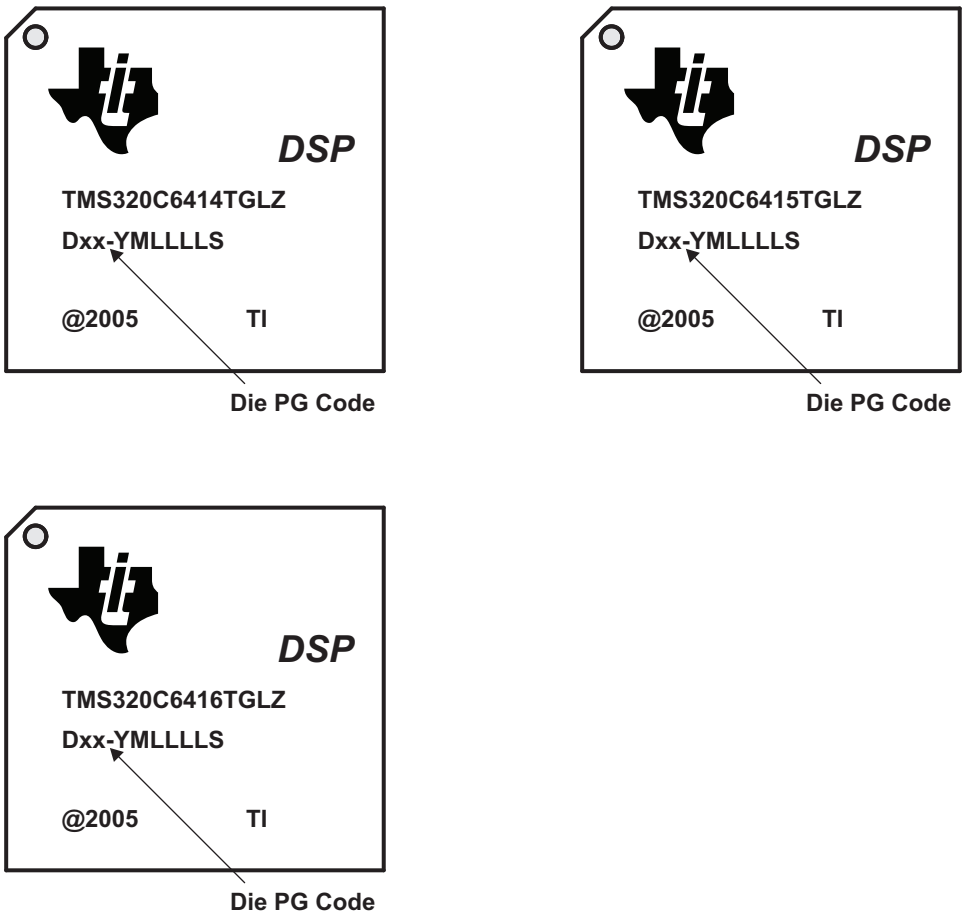
"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

1.2 Package Symbolization and Revision Identification

The device revision can be determined by the Die PG code marked on the top of the package. The location of the Die PG code for the GLZ package is shown in Figure 1. Figure 1 shows an example of the types of 6414T, 6415T, and 6416T package symbolization.



A NOTE: Qualified devices are marked with the letters “TMS” at the beginning of the device name, while non-qualified devices are marked with the letters “TMX” or “TMP” at the beginning of the device name.

Figure 1. Example, Die PG Codes for TMS320C6414T/C6415T/C6416T (GLZ)

Silicon revision is identified by a code on the chip. The code is of the format Dxx-YMLLLLS. If xx is 20, then the silicon is revision 2.0; if xx is 10, then the silicon is revision 1.0, and more.

Table 1. Die PG Codes

Die PG Code (xx)	SILICON REVISION	PART NUMBERS/COMMENTS
20	2.0	For all Silicon Revision 2.0 Devices
10	1.0	For all Silicon Revision 1.0 Devices

2 Silicon Revision 2.0 Known Design Exceptions to Functional Specifications and Usage Notes

2.1 Usage Notes for Silicon Revision 2.0

Usage Notes highlight and describe particular situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness. These notes will be incorporated into future documentation updates for the device (such as the device-specific data sheet), and the behaviors they describe will not be altered in future silicon revisions.

2.1.1 HPI: HWOB Bit in HPIC Register is Writable by CPU

On silicon revision 2.0 and earlier, the HWOB bit in the HPIC register is writable by the CPU, even though it should be writable by the Host only. Writing the incorrect value to the HPIC register will corrupt any data passed through the HPI.

When performing HPIC writes via the CPU, be sure to write the correct value into the HWOB bit.

2.1.2 TCP/VCP: TCP/VCP Memory Address Range Must be Accessed Using Only Doublewords (All C64x Devices)

On silicon revision 2.0 and earlier, the TCP/VCP memory address range (0x5000 0000 to 0x5FFF FFFF) must always be accessed by double word requests. Even if the C64x device does not support the TCP/VCP peripherals or if the TCP/VCP coprocessors are not enabled, this memory address range must always be accessed via double words. A request of ™ size will cause the chip to hang. Users should be especially careful when using Code Composer Studio Integrated Development Environment (IDE), because Code Composer Studio requests memory data using word-sized accesses. Do not attempt to view this memory map region (0x5000 0000 to 0x5FFF FFFF) in a Code Composer Studio window. (Note: this region can be disabled in the Code Composer Studio memory map ™to prevent accidental access.)

For all TMS320C64x DSP devices, always access the memory address range 0x5000 0000 to 0x5FFF FFFF via doublewords.

2.1.3 EMIFA: Dead CLKOUT4/6

On silicon revision 2.0 and earlier, there is a usage condition concerning EMIFA which can affect the functionality of CLKOUT4 and CLKOUT6.

The EMIFA Global Control register (GBLCTL) controls the logic that outputs the internal CPU/4 or CPU/6 clocks to the CLKOUT4 and CLKOUT6 pins. The GBLCTL is registered with the AECLKIN clock; therefore, without a valid EMIF clock, it is possible to have unknown values in the GBLCTL register. Furthermore, without a valid EMIF clock, the EMIFA GBLCTL will not be reset to its default value.

To avoid a dead CLKOUT4 and/or CLKOUT6, a valid clock must be provided to EMIFA at all times. This can be implemented externally using AECLKIN or by setting the BEA[17:16] pins (EMIFA_CLK_SEL bits) to select the internal CPU/4 or CPU/6.

2.1.4 L1P Cache: Incorrect Update of the L1P Tag RAMs (All C64x Devices)

On C6414T/C6415T/C6416T silicon revision 2.0 and earlier, when the CPU is executing non-cacheable code from external memory and there is snoop activity from L2 to L1P occurring at the same time, an incorrect update to the L1P Tag RAM can occur.

Snoop activity from L2 to L1P can be generated two ways:

1. EDMA/QDMA activity to L2
2. Block cache invalidates initiated in L2

When there is a non-cacheable L1P fetch that is returned from L2 to L1P, **and** there is a snoop from L2 in the very next cycle, then the snoop tag read interferes with the tag/status RAM write for the non-cacheable data. This interference causes the tag RAMs to be incorrectly updated with the tag for that line, rather than discarding the write to the tags. When the NEXT access to that non-cacheable line in L2 occurs, the L1P incorrectly registers this as a hit and transfers data from the L1P rather than the desired external data.

To *avoid* an incorrect update of the L1P tag RAMs, do the following as best practice:

1. While executing code from non-cacheable space, **do not** perform either EDMA/QDMA transfers to L2 **or** block cache invalidates initiated in L2.
2. Mark program code as cacheable as soon as possible.

2.1.5 Power Sequencing − IO Before Core

If customers are using IO before Core, which was initially supported, it is required to connect the Reserved pin W25 to ground due to insufficient pulldown strength. If IO comes up before Core, and W25 is not at ground level, this can result in the device coming up in an improper state. To ensure this does not occur, it is required to connect W25 to V_{SS}. If this is not done, then the power sequencing must be changed to Core before IO to ensure the internal state is set properly.

2.2 Silicon Revision 2.0 Known Design Exceptions to Functional Specifications

This is a list of the device silicon revision 1.0 known design exceptions to functional specifications.

Table 2. Silicon Revision 2.0 Advisory List

Advisory 2.0.1 *PCI: Slave Reads With a Long Latency Can Return Bad Data (C6415T/C6416T Only)*

Revision(s) Affected: 2.0 and earlier

Details: When an external master attempts to read memory from the DSP, it is issued a “Retry”. The PCI will then go prefetch a FIFO’s worth (32 words) of data. If this data takes an exceptionally long time to fetch (approximately 32K PCI cycles, ~1 ms @ 33-MHz PCI), the PCI port can mishandle the return data and “delete” the first word of a PCI frame. The data returned to the master is address-shifted by one 32-bit word. For example, if {0,1,2,3,4, ...} is expected and {1,2,3,4,5 ...} is returned.

Data will only take that long to fetch if the access is to a very slow external memory, or there are large, slow DMAs using the same priority queue as PCI (which, by default, is medium). For performance reasons, the separation of DMA traffic is recommended.

For more detailed information on the EDMA peripheral, EDMA performance, and EDMA performance data, see the following reference guide and application notes:

- TMS320C6000 DSP Enhanced Direct Memory Access (EDMA) Controller Reference Guide (literature number SPRU234)
- TMS320C64x EDMA Architecture Application Report (literature number SPRA994)
- TMS320C6000 EDMA IO Scheduling and Performance Application Report (literature number SPRAA00)
- TMS320C64x EDMA Performance Data Application Report (literature number SPRAA02)

PCI slave reads that start in less than 32K PCI cycles will not return bad data.

Workaround: Do not use PCI to directly read from exceptionally slow external memories.

Do not put any other DMA activity on the same priority level as PCI.

If system considerations force a user to put other DMA activity on PCI’s level, put only DMA traffic that will complete within the 32K PCI clock cycle limit.

Advisory 2.0.2 *PCI: Reads May Get Ahead of PCI Writes When PCI Exceeds the Transfer Request Limit (C6415T/C6416T Only)*

Revision(s) Affected: 2.0 and earlier

Details: When the PCI port exceeds its allocation of EDMA Transfer Requests (TRs), it can re−order read and write memory transactions. This can cause PCI slave reads to return “stale” data.

When the PCI port reaches its limit for the number of outstanding TRs, it must wait for previously issued TRs to complete. While the PCI port is waiting, any pending write data and/or read requests will be held pending in internal buffers. When a TR allocation is available, any pending read requests are serviced before any pending write data, regardless of the order in which the write data and read request were received. This can potentially allow the read request to get ahead of the write data, and return “stale” results.

Workaround: TI recommends that good EDMA resource allocation be used to prevent the problem. For detailed information on EDMA resource allocation, refer to the TMS320C64x EDMA Architecture Application Report (literature number SPRA994).

The following guidelines can help prevent PCI from running out of available TRs:

- Do not place large or slow transfers on EDMA priority levels at or above the PCI’s priority level.
- Increase PCI’s TR allocation limit. For detailed information, refer to the TMS320C6000 DSP Peripheral Component Interconnect (PCI) Reference Guide (literature number SPRU581).

The following guidelines can ensure correct read data:

- Do not read any of the previous 32 words written.
- Write 32 words of “dummy” data after writing “real” data.

3 Silicon Revision 1.0 Known Design Exceptions to Functional Specifications and Usage Notes

3.1 Usage Notes for Silicon Revision 1.0

Usage Notes highlight and describe particular situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness. These notes will be incorporated into future documentation updates for the device (such as the device-specific data sheet), and the behaviors they describe will not be altered in future silicon revisions.

3.1.1 Electronic Discharge (ESD) Performance

The TMS320C6414T/C6415T/C6416T devices were subjected to Human Body Model (HBM) ESD testing per EIA/JESD22-A114. Tests were passed at ± 2 KV with the exception of a single pin combination. When the RSV pin (G2) is stressed negative to the PLLV pin (J6) the passing voltage is 750 V. These two pins are not adjacent on the package and no more than normal ESD handling precautions are required.

The device has also been subjected to Charged Device Model (CDM) ESD testing per EIA/JESD22-C101, passing at the ± 500 V level.

3.1.2 Power Sequencing − IO Before Core

If customers are using IO before Core, which was initially supported, it is required to connect the Reserved pin W25 to ground due to insufficient pulldown strength. If IO comes up before Core, and W25 is not at ground level, this can result in the device coming up in an improper state. To ensure this does not occur, it is required to connect W25 to V_{SS}. If this is not done, then the power sequencing must be changed to Core before IO to ensure the internal state is set properly.

3.2 Silicon Revision 1.0 Known Design Exceptions to Functional Specifications

This is a list of the device silicon revision 1.0 known design exceptions to functional specifications.

Table 3. Silicon Revision 1.0 Advisory List

Advisory 1.0.1 *EMIF: PDT Write Transfers Fail When PDTWL Equals 3*

Revision(s) Affected: 1.0

Details: During a PDT write transfer, the $\overline{\text{PDT}}$, $\overline{\text{PDTA}}$, PDTDIR, $\overline{\text{SDWE}}$, and SDCAS signals will not be driven to their appropriate states when a non-PDT write is followed by a PDT write to a different bank. The incorrect behavior of $\overline{\text{PDT}}$, $\overline{\text{PDTA}}$, PDTDIR, $\overline{\text{SDWE}}$, and $\overline{\text{SDCAS}}$ can result in data corruption, as well as bus contention. This only occurs when PDTWL is set equal to 3 in the PDTCTL register.

Workaround: When performing both non-PDT writes and PDT writes to the same CE space, do not set PDTWL equal to 3.

Advisory 1.0.3 *EMIF: Asynchronous RAM AC Timings Different From Data Sheet Specifications*

Revision(s) Affected: 1.0

Details: The following “timing requirements for asynchronous memory cycles for EMIFA module” table reflects the differences between the actual C6414T/C6415T/C6416T silicon revision 1.0 values and the values specified in the TMS320C6414T, TMS320C6415T, TMS320C6416T Fixed-Point Digital Signal Processors Data Sheet (literature number SPRS226A or higher) for the EMIF peripheral - Asynchronous RAM.

timing requirements for asynchronous memory cycles for EMIFA and EMIFB modules

NO.		DATA SHEET VALUES		REVISION 1.0 ACTUAL VALUES		UNIT
		MIN	MAX	MIN	MAX	
7	$t_{h(EKO1H-ARDY)}$ Hold time, ARDY valid after ECLKOUTx high.	1		1.5		ns

Advisory 1.0.4 *PCI: AC Timings Different From Data Sheet Specifications (C6415T/C6416T Only)*

Revision(s) Affected: 1.0

Details: The following “timing requirements for PCI inputs” table reflects the differences between the actual C6415T/C6416T silicon revision 1.0 values and the values specified in the TMS320C6414T, TMS320C6415T, TMS320C6416T Fixed-Point Digital Signal Processors Data Sheet (literature number SPRS226A or higher) for the PCI peripheral.

timing requirements for PCI inputs

NO.		DATA SHEET VALUES		REVISION 1.0 ACTUAL VALUES		UNIT
		MIN	MAX	MIN	MAX	
6	$t_{h(IV-PCLKH)}$ Hold time, input valid after PCLK high	0		0.9		ns

Advisory 1.0.5 *HPI: AC Timings Different From Data Sheet Specifications*

Revision(s) Affected: 1.0

Details: The following “switching characteristics over recommended operating conditions during host-port interface cycles” table reflects the differences between the actual C6414T/C6415T/C6416T silicon revision 1.0 values and the values specified in the TMS320C6414T, TMS320C6415T, TMS320C6416T Fixed-Point Digital Signal Processors Data Sheet (literature number SPRS226A or higher) for the HPI peripheral.

switching characteristics over recommended operating conditions during host-port interface cycles

NO.		DATA SHEET VALUES		REVISION 1.0 ACTUAL VALUES		UNIT
		MIN	MAX	MIN	MAX	
8	$t_{d(HDV-HRDYL)}$ Delay time, HD valid to $\overline{HRDY}$ low	-3		-3.5		ns

Advisory 1.0.6 *L2 Cache: Accesses to Mapped L2 RAM Update L2 LRU Information*

Revision(s) Affected: 1.0

Details:

CPU accesses to L2 RAM addresses incorrectly cause updates to the “Least-Recently Used” (LRU) state information in the L2 cache. This may cause an increased number of L2 cache misses in some systems.

The L2 cache implements a 4-way set-associative cache. The cache uses the (LRU) information to determine what “way” within each set is least recently used. When the CPU accesses data in L2 cache, the L2 controller determines what “way” holds the data in that set, and marks that “way” as most-recent. When allocating a new line in the cache, the L2 controller evicts the line in the set from the least-recently used “way” under the assumption that more-recently accessed data is more relevant.

When the CPU accesses data in L2 SRAM, either via program fetches or data accesses, the L2 cache is incorrectly updated by the L2 controller. The L2 controller updates the LRU as if the access was to “way 0” in the cache. This causes the LRU history to not reflect the actual sequence of accesses to L2 cache. As a result, the L2 may not choose the actual least-recently used line during an eviction.

Only CPU accesses to L2 RAM cause this update to LRU information in L2 cache. DMA accesses to L2 RAM do not trigger updates to the L2 LRU information.

Workaround:

Perform one of the following three workarounds:

- Choose an L2 cache size that fits your cached working set. The advisory primarily impacts programs that are significantly larger than the L2 cache size.
- Explicitly remove cached contents from L2 when finished with them. The L2 cache allocates “invalid” lines within each set before consulting the LRU. Programs may do this using “block invalidate” or “block writeback-invalidate” commands in the L2 cache.
- Lay out buffers in L2 RAM so they do not conflict with buffers or code held in L2 cache. L2 RAM addresses map onto L2 sets in the same manner as external memory addresses.

For more detailed information on the organization and manipulation of the L2 cache, see the TMS320C64x DSP Two-Level Internal Memory Reference Guide (literature number SPRU610).

Advisory 1.0.7 *L2 Cache: L2 Controller Incorrectly Updates LRU for Accesses in L2 Cache*

Revision(s) Affected: 1.0

Details:

The L2 cache implements a 4-way set-associative cache. The cache uses the “Least-Recently Used” (LRU) information to determine what “way” within each set is least recently used. When the CPU accesses data in L2 cache, the L2 controller determines what “way” holds the data in that set, and marks that “way” as most-recent. When allocating a new line in the cache, the L2 controller evicts the line in the set from the least-recently used “way” under the assumption that more-recently accessed data is more relevant.

For this advisory, CPU accesses which hit L2 cache do not correctly update the LRU information for the set accessed. Instead of storing the LRU information back to the set being accessed, the L2 controller stores the information to 3 adjacent sets.

LRU information is stored in groups of 4 sets. The 3 adjacent sets affected by the current set are defined as follows:

- Group 1 contains sets 0, 1, 2, 3
- Group 2 contains sets 4, 5, 6, 7
- and more

For example, during an access to set 5, the L2 controller incorrectly stores the LRU information to sets 4, 6, 7.

As a result of this issue, repeated misses to the same set with no intervening accesses to adjacent sets will allocate from the same “way”. This can make the L2 cache appear to “thrash”. A series of misses to consecutive sets in L2 cache may appear to allocate with reduced associativity; that is, L2 could appear to behave as a 2-way or direct-mapped cache.

Workaround:

Perform one of the following three workarounds:

- Choose an L2 cache size that fits your cached working set. The advisory primarily impacts programs that are significantly larger than the L2 cache size.
- Explicitly remove cached contents from L2 when finished with them. The L2 cache allocates “invalid” lines within each set before consulting the LRU. Programs may do this using “block invalidate” or “block writeback-invalidate” commands in the L2 cache.
- Offset external buffers that are accessed as part of the same working set so that accesses to the buffers are at least 4 L2 sets apart (512 bytes). This will prevent the buffers from ”thrashing” each other in L2 cache.

For more detailed information on the organization and manipulation of the L2 cache, see the TMS320C64x DSP Two-Level Internal Memory Reference Guide (literature number SPRU610).

Advisory 1.0.8 *JTAG: Boundary Scan IDCODE_REGISTER Incorrect*

Revision(s) Affected: 1.0

Details: When reading the Boundary Scan IDCODE_REGISTER, an incorrect value is returned. The upper 16 bits of the Boundary Scan IDCODE_REGISTER, which contain the variant field (silicon revision information) and a portion of the device id field, are incorrect. This problem is due to data corruption in the reset configuration logic.

Workaround: Disregard the upper 16 bits of data contained in the Boundary Scan IDCODE_REGISTER. The lower 16 bits of the Boundary Scan IDCODE_REGISTER, which include the lower 4 bits of the device id field, can still be read.

This advisory issue will be fixed in the next major silicon revision.

Advisory 1.0.9 *EMIF: PDT Transfers Fail When Acessing the Same SDRAM Page as Non-PDT Transfers (All C64x Devices)*

Revision(s) Affected: 1.0

Details: When PDT and non-PDT transfers occur to the same SDRAM page, $\overline{\text{PDTA}}$, $\overline{\text{PDT}}$, and PDTDIR may not be driven to their appropriate state. The incorrect behavior of these signals can result in PDT data corruption.

Workaround: Place all PDT transfers, whether reads or writes, in a memory range that is an aliased version of the physical SDRAM. For example, if SDRAM is in CE0 and is 128 Mbytes (MB) in depth, then the functional addressable space is 0x8000 0000 through 0x87FF FFFF and all normal CPU and non-PDT DMA transfers should access this memory range. The “aliased” view of the SDRAM is at address 0x8800 0000 through 0x8FFF FFFF and must be used for all PDT transfers. Similarly, if SDRAM is 64 MB in depth, the functional addressable view is 0x8000 0000 through 0x83FF FFFF and the “aliased” view is 0x8400 0000 through 0x87FF FFFF. The aliased view accesses the same underlying physical address as the functional view.

The address space for the “aliased” view can be created by bit-wise ORing the “logical address” (functional address) in use as follows.

- For 128 MB, OR with 0x0800 0000
- For 64 MB, OR with 0x0400 0000
- For 32 MB, OR with 0x0200 0000
- For 16 MB, OR with 0x0100 0000

This workaround is ONLY applicable if the CE space has less than or equal to 128 MB of SDRAM connected to it. If a CE space is full (maximum addressable space is 256 MB), then that CE space cannot support PDT transfers.

Advisory 1.0.11 *PCI/HPI: Data Corruption Can Occur When DV_{DD} Powers Up Before CV_{DD}*

Revision(s) Affected: 1.0

Details:

Advisory 1.0.11- PCI\HPI: Data Corruption Can Occur When DV_{DD} Powers Up Before CV_{DD} (for all device speeds) supersedes Advisory 1.0.2 − PCI/HPI: Data Corruption Can Occur When CV_{DD} = 1.1 V.

When DV_{DD} powers up before CV_{DD}, the PCI/HPI I/O buffers can be initialized incorrectly − causing them to be stuck in a Hi-Z condition. This can result in incorrect data on the bus, deadlocked interface or other undesirable operation.

Workaround:

One of the following options is available as a Workaround:

- Power up the CV_{DD} supply before the DV_{DD} supply [see timing requirements for power-on sequence table and Figure 2] or
- Do not use the PCI and/or HPI peripherals. Do not use GP[15:9] as outputs.

timing requirements for power-on sequence(1)

NO.		-600, -720, -850, −1G		UNIT
		MIN	MAX	
1	$t_{d(CVDD-DVDDR)}$ Delay time, CV_{DD} supply ready to DV_{DD} supply ramp start	0.5	200	ms

(1) Delay time from CV_{DD} is referenced to the supply reaching its minimum operating voltage.

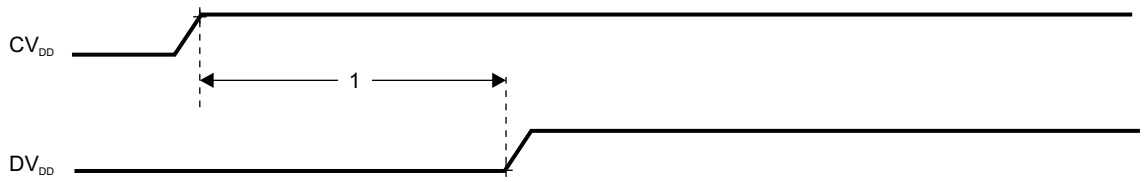


Figure 2. Power-On Sequence Timing

Revision History

This silicon errata revision history highlights the technical changes made to SPRZ216I to make it a **J** revision.

Scope: Applicable updates relating to the device has been incorporated.

Revision History

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
Figure 1	Updated figure.
Section 1.2	Removed last sentence.
Table 1	Removed part numbers from table.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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