TMS320C6203, TMS320C6203B

Digital Signal Processors

Silicon Errata

C6203 Silicon Revision 1.x

C6203B Silicon Revisions 2.x, 3.0, 3.1

SPRZ174L
November 2000
Revised February 2004

TEXAS INSTRUMENTS

REVISION HISTORY

This silicon errata revision history highlights the technical changes made to the SPRZ174K revision to make it an SPRZ174L revision.

Scope: This document has been reviewed for technical accuracy; the technical content is up-to-date as of the specified release date.

PAGE(S) NO.	ADDITIONS/CHANGES/DELETIONS
	None

Contents

1 Introduction

This document describes the silicon updates to the functional specifications for the TMS320C6203 silicon releases 1.x and earlier, and for the TMS320C6203B silicon releases 2.x, 3.0, and 3.1.

For additional information, see the latest version of *TMS320C6000 DSP Peripherals Overview Reference Guide* (literature number SPRU190) and the latest verion of *TMS320C6203B Fixed-Point Digital Signal Processor* data sheet (literature number SPRS086).

1.1 Quality and Reliability Conditions

TMX Definition

Texas Instruments (TI) does not warranty either (1) electrical performance to specification, or (2) product reliability for products classified as “TMX.” By definition, the product has not completed data sheet verification or reliability performance qualification according to TI Quality Systems Specifications.

The mere fact that a “TMX” device was tested over a particular temperature and voltage ranges should not, in any way, be construed as a warranty of performance.

TMP Definition

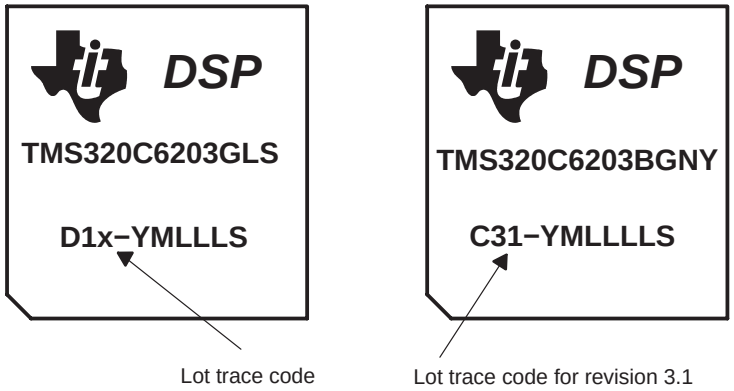
TI does not warranty product reliability for products classified as “TMP.” By definition, the product has not completed reliability performance qualification according to TI Quality Systems Specifications; however, products are tested to a published electrical and mechanical specification.

TMS Definition

Fully-qualified production device.

1.2 Revision Identification

The device revision can be determined by the lot trace code marked on the top of the package. The location for the lot trace codes for the GLS and the GNY packages are shown in Figure 1 and Table 1.



NOTE: Qualified devices are marked with the letters “TMS” at the beginning of the device name, while nonqualified devices are marked with the letters “TMX” at the beginning of the device name.

Figure 1. Example, Lot Trace Code for TMS320C6203 and TMS320C6203B

Table 1. Lot Trace Code Names

Lot Trace Code	Silicon Revision	Comments
31	3.1	TMS320C6203**B** (GNZ/GNY). There are ***no*** known design exceptions to functional specifications or usage notes for TMS320C6203B silicon revision 3.1.
30	3.0	TMS320C6203**B** (GNZ/GNY). All advisory issues presented on TMS320C6203B silicon revision 2.5 and earlier and TMS320C6203 silicon revision 1.x and earlier have been resolved.
2x	2.x	TMS320C6203B (GNZ/GLS). Revisions beyond 2.5 have been done to improve yield and are functionally the same as Rev. 2.5.
1x	1.x	TMS320C6203 (GNZ/GLS). There have been multiple silicon revisions done to improve yield that are functionally the same.

2 C6203B Silicon Revision 3.1 Known Design Exceptions to Functional Specifications and Usage Notes

There are no known design exceptions to functional specifications or usage notes for the TMS320C6203B silicon revision 3.1.

3 C6203B Silicon Revision 3.0 Known Design Exceptions to Functional Specifications and Usage Notes

3.1 Usage Notes for Silicon Revision 3.0

Usage Notes highlight and describe particular situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness. These notes will be incorporated into future documentation updates for the device (such as the device-specific data sheet), and the behaviors they describe will not be altered in future silicon revisions.

3.2 Silicon Revision 3.0 Known Design Exceptions to Functional Specifications

Advisory 3.0.1	*Memory: Potential Read After Write Error*

Revision(s) Affected: 2.x and 3.0

Details: In the event that ALL of the following five conditions are met simultaneously, a data bit misread may occur in internal device memory:

1. Write immediately followed by a read
2. The write and read occur in back-to-back cycles without any stalls
3. Read must be in same 16-bit-wide bank as preceding write.
   (The addressing structure of the physical banks is described below.)
4. Read must access the same physical column as the preceding write (read offset from write by a multiple of 0x100 bytes)
5. Read value must be of a different state than that of the preceding write (e.g., if write value is 0x0, then read value must be different from 0x0)

Note: The read and/or write conditions can occur via the CPU, DMA, or a combination of the two.

- CPU Write, DMA Read
- CPU Write, CPU Read
- DMA Write, DMA Read
- DMA Write, CPU Read

Back-to-back accesses typically occur in tightly looped code. Tightly looped code rarely does both reads and writes to the same bank offset by a multiple of 0x100 bytes. In algorithms that do stride by this amount, typically loads are done for different iterations than stores so they are not offset in the software pipelined loop by this amount.

Memory: Potential Read After Write Error (Continued)

The C6203B data memory consists of 16 separate 16-bit-wide banks. These banks are broken down into 2 blocks, each containing 2 subblocks of 4 banks. Data memory is addressed as follows:

ADDR[31] → Data Memory Select
ADDR[30..19] → Reserved
ADDR[18] → Block Select
ADDR[17] → Subblock Select
ADDR[16..8] → Row Select
ADDR[7..3] → Column Select
ADDR[2..1] → 16-bit Bank Select
ADDR[0] → Byte Enable

Only when a write followed by a read occurs and the Row Select bits (ADDR[16..8]) are different will this error potentially occur.

For example, the error may occur using the following sequence:

Write 0x12345678 to address 0x80010042

Read from address 0x80010542 ← Only Row Select changes

In this case, the read may come back with a different value than expected.

The error will ***not*** occur under the following sequences:

Write 0xFEDCBA98 to address 0x80010054

Read from address 0x80030554 ← Different Block

or

Write 0x55AA55AA to address 0x80010042

Read from address 0x80010562 ← Different column

Assuming all five conditions above have been met, this issue is more likely to be encountered at:

- 1.5-V, rather than 1.7-V core supply voltage. 1.7 V significantly reduces the likelihood of the error.
- Higher, rather than lower, device case operating temperature
- Higher, rather than lower, device operating frequency. 250-MHz operation significantly reduces the likelihood of error.

Note that this behavior is ***NOT*** a reliability risk. It should not degrade for a given set of operating conditions and code.

Workaround: The occurrence of all five conditions is application-specific. Code should be examined to determine if the five conditions above are met. If all conditions are met, insert at least one dead cycle between the write and read.

4 C6203B Silicon Revision 2.5 Known Design Exceptions to Functional Specifications

Changes shown in this section refer to two data sheets by their literature numbers: *TMS320C6203 Fixed-Point Digital Signal Processor* data sheet (literature number SPRS086D) and *TMS320C6202, TMS320C6202B, TMS320C6203, TMS320C6204 Fixed-Point Digital Signal Processors* data sheet (literature number SPRS104A). The SPRS104A data sheet has been replaced with SPRS104C, when the TMS320C6203 device was moved back to SPRS086D and then later updated to become the TMS320C6203B device-specific data sheet (SPRS086I or later). Errata values relate solely to a specific revision of the silicon and do not appear in either data sheet.

PLL Component Change

Details: New component values must be implemented to optimize the performance of the PLL on revision 2.x of the C6203B DSP. Earlier revisions should still use the values listed in the data sheet. The new values added to the PLL Component Selection Table of the C6203 (rev 1.x), C6203B (rev 2.x) data sheet are as follows:

- R1 − 45.3 Ω
- C1 − 47 nF
- C2 − 10 pF

Workaround: Use the values in Table 2.

Table 2. TMS320C6203, TMS320C6203B PLL Component Selection Table†

CLKMODE‡	CLKIN RANGE (MHz)	CPU CLOCK FREQUENCY RANGE (MHz)	CLKOUT2 RANGE (MHz)	R1 [±1%] (Revision No.)	C1 [±10%] (Revision No.)	C2 [±10%] (Revision No.)	TYPICAL LOCK TIME (μs)
x4	32.5−75	130−300	65−150	60.4 Ω (1.x) 45.3 Ω (2.x, 3.x)	27 nF (1.x) 47 nF (2.x, 3.x)	560 pF (1.x) 10 pF (2.x, 3.x)	75
x6	21.7−50						
x7	18.6−42.9						
x8	16.3−37.5						
x9	14.4−33.3						
x10	13−30						
x11	11.8−27.3						

† Under some operating conditions, the maximum PLL lock time may vary as much as 150% from the specified typical value. For example, if the typical lock time is specified as 100 μs, the maximum value may be as long as 250 μs.

‡ CLKMODE x1, x4, x6, x7, x8, x9, x10, and x11 apply to the GLS device. The GJL device is restricted to x1, x4, x8, and x10 multiply factors.

Advisory 2.5.1 — *EMIF: Synchronous-Burst Memory AC Timing Differs From Data Sheet*

Revision(s) Affected: 2.5 and earlier

Details: The timing parameters in Table 3 and Table 4 differ from the ones specified in the C6203 data sheet (SPRS104A) and the *TMS320C6203B Fixed-Point Digital Signal Processor* data sheet (SPRS086I or later). Table 3 and Table 4 list the differences between the data sheet values and the actual values on silicon revision 2.5 or earlier.

The change in ac timings may cause SBSRAM interface timing violations, especially at low or high temperature conditions.

Table 3. Timing Requirements For Synchronous-Burst SRAM Cycles

NO.			SPRS104A (OLD VALUES) -250, -300				2.5 AND EARLIER VALUES -250, -300				UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
8	$t_{h(CKO2H-EDV)}$	Hold time, read EDx valid after CLKOUT2 high	2.0		1.5		2.0		1.9		ns

Table 4. Switching Characteristics Over Recommended Operating Conditions For Synchronous-Burst SRAM Cycles †‡

NO.	PARAMETER		SPRS104A (OLD VALUES) -250, -300				2.5 AND EARLIER VALUES -250, -300				UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
2	$t_{oh(CKO2H-CEV)}$	Output hold time, $\overline{CEx}$ valid after CLKOUT2 high	P − 3		P − 2.3		P − 4.3		P − 4.1		ns
4	$t_{oh(CKO2H-BEIV)}$	Output hold time, $\overline{BEx}$ invalid after CLKOUT2 high	P − 3		P − 2.3		P − 4.3		P − 4.1		ns
6	$t_{oh(CKO2H-EAIV)}$	Output hold time, EAx invalid after CLKOUT2 high	P − 3		P − 2.3		P −4. 3		P − 4.1		ns
10	$t_{oh(CKO2H-ADSV)}$	Output hold time, $\overline{SDCAS}$/$\overline{SSADS}$ valid after CLKOUT2 high	P − 3		P − 2.3		P − 4.3		P − 4.1		ns
12	$t_{oh(CKO2H-OEV)}$	Output hold time, $\overline{SDRAS}$/$\overline{SSOE}$ valid after CLKOUT2 high	P − 3		P − 2.3		P − 4.3		P − 4.1		ns
13	$t_{osu(EDV-CKO2H)}$	Output setup time, EDx valid before CLKOUT2 high§	P − 1.2		P + 0.1		P − 1.2		P − 0.3		ns
14	$t_{oh(CKO2H-EDIV)}$	Output hold time, EDx invalid after CLKOUT2 high	P − 3		P − 2.3		P − 4.4		P − 4.2		ns
16	$t_{oh(CKO2H-WEV)}$	Output hold time, $\overline{SDWE}$/$\overline{SSWE}$ valid after CLKOUT2 high	P − 3		P − 2.3		P − 4.3		P − 4.1		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 300 MHz, use P = 3.3 ns.
‡ $\overline{SDCAS}$/$\overline{SSADS}$, $\overline{SDRAS}$/$\overline{SSOE}$, and $\overline{SDWE}$/$\overline{SSWE}$ operate as $\overline{SSADS}$, $\overline{SSOE}$, and $\overline{SSWE}$, respectively, during SBSRAM accesses.
§ For the first write in a series of one or more consecutive adjacent writes, the write data is generated one CLKOUT2 cycle early to accommodate the ED enable time.

Workaround: Although these new numbers do not coincide with current memory specifications, no problems associated with these misalignments have been reported. It is suggested that the fastest available memories be used to reduce the possibility of setup and hold timing violations. Silicon revision 3.0 will correct this issue.

Advisory 2.5.2 — *EMIF: Synchronous DRAM AC Timing Differs From Data Sheet*

Revision(s) Affected: 2.5 and earlier

Details: The timing parameters in Table 5 and Table 6 differ from the ones specified in the C6203 data sheet (SPRS104A) and the *TMS320C6203B Fixed-Point Digital Signal Processor* data sheet (SPRS086I or later). Table 5 and Table 6 list the differences between the data sheet values and the actual values on silicon revision 2.5 or earlier.

The change in ac timings may cause SDRAM interface timing violations, especially at low or high temperature conditions.

Table 5. Timing Requirements For Synchronous DRAM Cycles

NO.			SPRS104A (OLD VALUES) -250, -300				2.5 AND EARLIER VALUES -250, -300				UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
7	$t_{su(EDV-CKO2H)}$	Setup time, read EDx valid before CLKOUT2 high	1.2		0.5		1.2		1.2		ns
8	$t_{h(CKO2H-EDV)}$	Hold time, read EDx valid after CLKOUT2 high	2.7		2		2.9		2.8		ns

Table 6. Switching Characteristics Over Recommended Operating Conditions For Synchronous DRAM Cycles †‡

NO.	PARAMETER		SPRS104A (OLD VALUES) -250, -300				2.5 AND EARLIER VALUES -250, -300				UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{osu(CEV-CKO2H)}$	Output setup time, $\overline{CEx}$ valid before CLKOUT2 high	P − 0.9		P + 0.6		P − 0.9		P		ns
2	$t_{oh(CKO2H-CEV)}$	Output hold time, $\overline{CEx}$ valid after CLKOUT2 high	P − 2.9		P − 1.8		P − 4.2		P − 4.0		ns
3	$t_{osu(BEV-CKO2H)}$	Output setup time, $\overline{BEx}$ valid before CLKOUT2 high	P − 0.9		P + 0.6		P − 0.9		P		ns
4	$t_{oh(CKO2H-BEIV)}$	Output hold time, $\overline{BEx}$ invalid after CLKOUT2 high	P − 2.9		P − 1.8		P − 4.2		P − 4.0		ns
5	$t_{osu(EAV-CKO2H)}$	Output setup time, EAx valid before CLKOUT2 high	P − 0.9		P + 0.6		P − 0.9		P		ns
6	$t_{oh(CKO2H-EAIV)}$	Output hold time, EAx invalid after CLKOUT2 high	P − 2.9		P − 1.8		P − 4.2		P − 4.0		ns
9	$t_{osu(CASV-CKO2H)}$	Output setup time, $\overline{SDCAS}$/$\overline{SSADS}$ valid before CLKOUT2 high	P − 0.9		P + 0.6		P − 0.9		P		ns
10	$t_{oh(CKO2H-CASV)}$	Output hold time, $\overline{SDCAS}$/$\overline{SSADS}$ valid after CLKOUT2 high	P − 2.9		P − 1.8		P − 4.2		P − 4.0		ns
11	$t_{osu(EDV-CKO2H)}$	Output setup time, EDx valid before CLKOUT2 high§	P − 1.5		P + 0.6		P − 1.5		P − 0.3		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 300 MHz, use P = 3.3 ns.
‡ $\overline{SDCAS}$/$\overline{SSADS}$, $\overline{SDRAS}$/$\overline{SSOE}$, and $\overline{SDWE}$/$\overline{SSWE}$ operate as $\overline{SDCAS}$, $\overline{SDRAS}$, and $\overline{SDWE}$, respectively, during SDRAM accesses.
§ For the first write in a series of one or more consecutive adjacent writes, the write data is generated one CLKOUT2 cycle early to accommodate the ED enable time.

Table 6. Switching Characteristics Over Recommended Operating Conditions For Synchronous DRAM Cycles †‡ (Continued)

NO.	PARAMETER		SPRS104A (OLD VALUES) -250, -300				2.5 AND EARLIER VALUES -250, -300				UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{oh}(CKO2H-EDIV)	Output hold time, EDx invalid after CLKOUT2 high	P − 2.8		P − 1.8		P − 4.3		P − 4.2		ns
13	t_{osu}(WEV-CKO2H)	Output setup time, SDWE/SSWE valid before CLKOUT2 high	P − 0.9		P + 0.6		P − 0.9		P		ns
14	t_{oh}(CKO2H-WEV)	Output hold time, SDWE/SSWE valid after CLKOUT2 high	P − 2.9		P − 1.8		P − 4.2		P − 4.0		ns
15	t_{osu}(SDA10V-CKO2H)	Output setup time, SDA10 valid before CLKOUT2 high	P − 0.9		P + 0.6		P − 0.9		P		ns
16	t_{oh}(CKO2H-SDA10IV)	Output hold time, SDA10 invalid after CLKOUT2 high	P − 2.9		P − 1.8		P − 4.2		P − 4.0		ns
17	t_{osu}(RASV-CKO2H)	Output setup time, SDRAS/SSOE valid before CLKOUT2 high	P − 0.9		P + 0.6		P − 0.9		P		ns
18	t_{oh}(CKO2H-RASV)	Output hold time, SDRAS/SSOE valid after CLKOUT2 high	P − 2.9		P − 1.8		P − 4.2		P − 4.0		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 300 MHz, use P = 3.3 ns.
‡ SDCAS/SSADS, SDRAS/SSOE, and SDWE/SSWE operate as SDCAS, SDRAS, and SDWE, respectively, during SDRAM accesses.
§ For the first write in a series of one or more consecutive adjacent writes, the write data is generated one CLKOUT2 cycle early to accommodate the ED enable time.

Workaround: Although these new numbers do not coincide with current memory specifications, no problems associated with these misalignments have been reported. It is suggested that the fastest available memories be used to reduce the possibility of setup and hold timing violations. Silicon revision 3.0 will correct this issue.

Advisory 2.5.3

XBUS FIFO: Expansion Bus Synchronous FIFO AC Timing Differs From Data Sheet

Revision(s) Affected: 2.5 and earlier

Details: The timing parameters in Table 7 differ from the ones specified in the C6203 data sheet (SPRS104A) and the *TMS320C6203B Fixed-Point Digital Signal Processor* data sheet (SPRS086I or later). Table 7 lists the differences between the data sheet values and the actual values on silicon revision 2.5 or earlier.

In glueless FIFO interfaces, the negative delay time may violate the hold time of the FIFO. Use external glue logic to meet the FIFO hold time requirements.

Table 7. Switching Characteristics Over Recommended Operating Conditions For Synchronous FIFO Interface

NO.	PARAMETER		SPRS104A (OLD VALUES) -250, -300		2.5 AND EARLIER VALUES -250, -300		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{d(XFCKH-XCEV)}$	Delay time, XFCLK high to $\overline{XCEx}$ valid	1.5	4.5	−1.8	4.5	ns
2	$t_{d(XFCKH-XAV)}$	Delay time, XFCLK high to $\overline{XBE[3:0]}$/XA[5:2] valid†	1.5	4.5	−1.8	4.5	ns
3	$t_{d(XFCKH-XOEV)}$	Delay time, XFCLK high to $\overline{XOE}$ valid	1.5	4.5	−1.8	4.5	ns
4	$t_{d(XFCKH-XREV)}$	Delay time, XFCLK high to $\overline{XRE}$ valid	1.5	4.5	−1.8	4.5	ns
7	$t_{d(XFCKH-XWEV)}$	Delay time, XFCLK high to $\overline{XWE}$/$\overline{XWAIT}$‡ valid	1.5	4.5	−1.8	4.5	ns
9	$t_{d(XFCKH-XDIV)}$	Delay time, XFCLK high to XDx invalid	1.5		−2.1		ns

† $\overline{XBE[3:0]}$/XA[5:2] operate as address signals XA[5:2] during synchronous FIFO accesses.
‡ $\overline{XWE}$/$\overline{XWAIT}$ operates as the write-enable signal $\overline{XWE}$ during synchronous FIFO accesses.

Workaround: Although these new numbers do not coincide with current memory specifications, no problems associated with these misalignments have been reported. It is suggested that the fastest available memories be used to reduce the possibility of setup and hold timing violations. Silicon revision 3.0 will correct this issue.

Advisory 2.5.4

XBUS 8:1 Ratio Limitation

Revision(s) Affected: 2.5 through 2.2

Details: Advisory 2.1.4 is fixed on silicon revision 2.2. The fix has a restriction that limits the maximum operating frequency at which the expansion bus can operate. The expansion bus frequency should operate at less than one-eighth the CPU frequency. For example, if the CPU clock is operating at 300 MHz, XCLKin should operate no faster than 37.5 MHz. At a CPU clock speed of 250 MHz, XCLKin should operate no faster than 31.25 MHz.

Workaround: Silicon revision 3.0 will correct this issue.

Advisory 2.5.5	*XBUS: XBUS and DMA Hang When Using XRDY During ASYNC I/O Read*

Revision(s) Affected: 2.5 and earlier

Details: An XRDY synchronization problem causes incorrect operation on the expansion bus. When using the expansion bus asynchronous I/O interface with XRDY, the last word in a data transfer may not be captured. The XBUS interface will seem to act correctly but the last word will not be stored in memory and the direct memory access (DMA) will not complete. The XBUS and the DMA are stalled after the last access, not allowing any subsequent DMA or XBUS transfers to complete. This problem has not been reported internally or externally to date but it could affect the XBUS operation if the recommendations in the workaround are not followed.

Workaround: Do not use XRDY to stall the expansion bus. Instead lengthen the access parameters (setup, strobe, hold) to the maximum and ensure that the external device is ready in that time frame or only make XBUS requests after the external device is ready.

Advisory 2.5.6	*XBUS − EMIF: Sync Host XBUS to EMIF SDRAM Corruption of Data*

Revision(s) Affected: 2.5 and earlier

Details: When performing an XBUS Synchronous Host Master Read, corruption of data may occur in some cases where an XBUS wait occurs concurrently with a not-ready input. One word may be overwritten by a subsequent word, corrupting the data. An example of a transfer as it was intended is shown in Figure 2. Figure 3 shows an example of how the data might be corrupted with D3 overwriting D2.

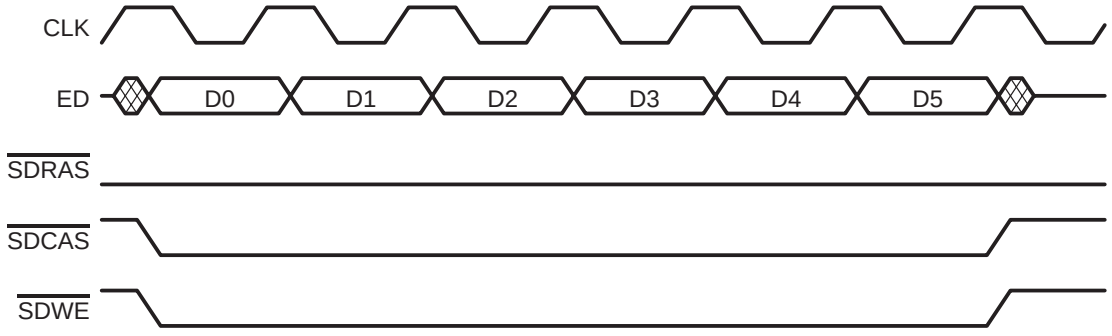


Figure 2. Original Transfer

XBUS − EMIF: Sync Host XBUS to EMIF SDRAM Corruption of Data (Continued)

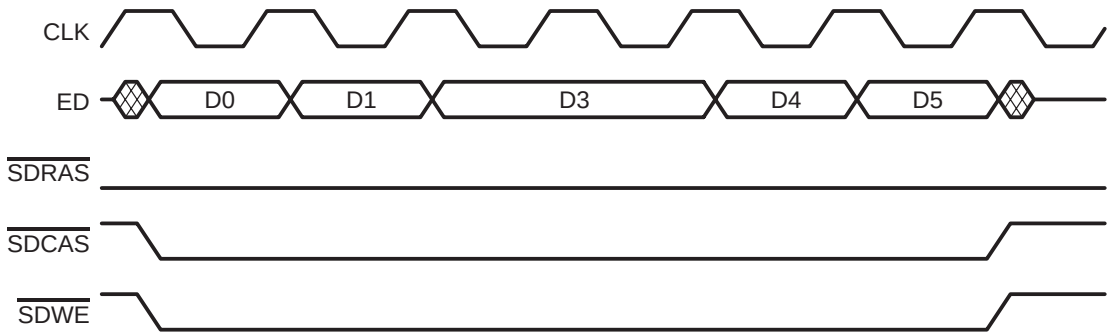


Figure 3. Failing Transfer as Seen at Destination

Workaround: To avoid this issue, use the following:

- Do not stall the XRDY signal during the cycle when there is an XWAIT asserted.
- This frequency may be alleviated by increasing the CPU CLK:CLK frequency ratio past 10:1.

5 C6203B Silicon Revision 2.1 Known Design Exceptions to Functional Specifications

Advisory 2.1.4	*XBUS: Corruption of Data Via Synchronous Host Port Mode*

Revision(s) Affected: 2.1 and earlier

Details: While the expansion bus is operating in Synchronous Host Port Mode, certain expansion Bus output signals may be corrupted. The corruption occurs on output signals only and there are no known issues with any other XBUS modes (Asynchronous Host Mode, Asynchronous I/O Mode, or Synchronous FIFO Mode). In Synchronous Host Port Mode, some or all outputs of the XD signal lines move from the next word into the current word being transferred. This corruption not only affects the XD signal lines, but the output control signals as well (XAS, XBLAST, etc.). Figure 4 shows what a typical Synchronous Host transfer should look like. Figure 5 shows the address (AD), as well as data word 2 (D2) being corrupted by the next word. In this figure, the address is corrupted by D0 and D2 is written over by D3. Figure 6 is an example showing D0 being completely corrupted by D1 and D3 being partially corrupted by D4. The transfer should be 0x0001, 0xFF02, 0x0003, ..., 0xFF1F to Address 0x8000.

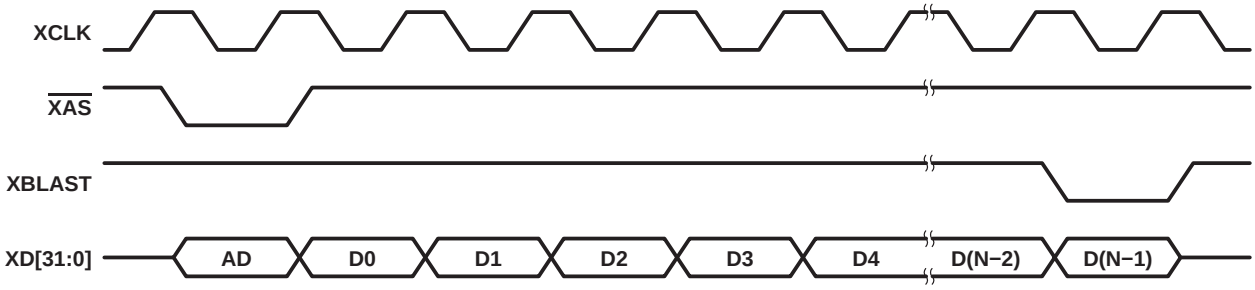


Figure 4. Correct Transfer of Address and Data via the Synchronous Host Port Mode of the Expansion Bus

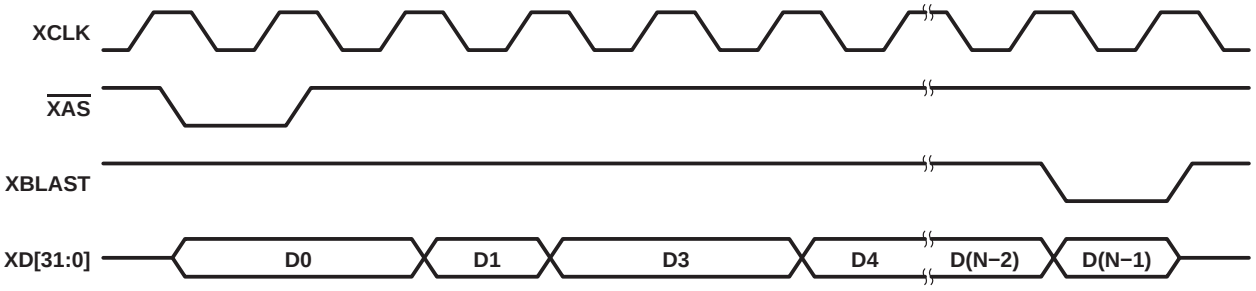


Figure 5. Incorrect Transfer via the Synchronous Host Port Mode of the Expansion Bus.

XBUS: Corruption of Data Via Synchronous Host Port Mode (Continued)

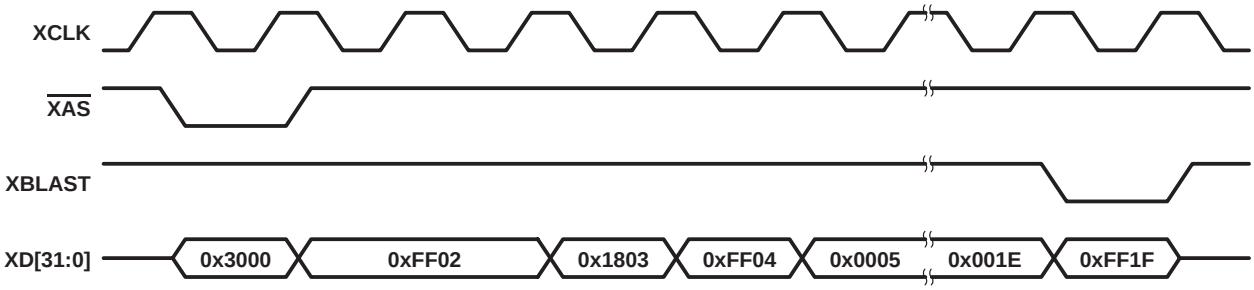


Figure 6. Example Showing Partial Corruption

Workaround: The best method of reducing the number of failures resulting from this issue is to increase the voltage and decrease the CPU Clock speed. For Rev. 2.1 and earlier revisions, 1.5-V / 300-MHz devices should operate correctly at 1.7 V / 250 MHz. This issue will be fixed in the next major revision.

6 C6203 Silicon Revision 1.x Known Design Exceptions to Functional Specifications

Advisory 1.x.1	*XBUS: FIFO Data and Control Signals Zero Delay/Skewed From XFCLK High*

Revision(s) Affected: 1.x, 0 (TMS320C6203)

Details:

In XBUS Synchronous FIFO mode, the delay time of data and control signals from XFCLK high differ from the values shown in the TMS320C6203 data sheet (literature number SPRS104A).

For FIFO glueless and non-glueless reads (at all FIFO clock rates), the following parameters have a delay time close to zero:

- $\overline{\text{XCE}}$ high-to-low transition after XFCLK high (Parameter 1a in Figure 7 and Figure 8)
- $\overline{\text{XBE}}$/XA[5:2] valid after XFCLK high (Parameter 2a in Figure 7 and Figure 8)
- $\overline{\text{XOE}}$ high-to-low transition after XFCLK high (Parameter 3a in Figure 7 and Figure 8)
- $\overline{\text{XRE}}$ high-to-low transition after XFCLK high (Parameter 4a in Figure 7 and Figure 8)

For FIFO reads with XFCLK = 1/2 CPU clock rate, the following parameters have a delay time close to zero. For FIFO reads with XFCLK = 1/4, 1/6, or 1/8 CPU clock rate, the same set of parameters have a delay time close to P, where P = CPU clock period.

- $\overline{\text{XCE}}$ low-to-high transition after XFCLK high (Parameter 1b in Figure 7 and Figure 8)
- $\overline{\text{XBE}}$/XA[5:2] invalid after XFCLK high (Parameter 2b in Figure 7 and Figure 8)
- $\overline{\text{XOE}}$ low-to-high transition after XFCLK high (Parameter 3b in Figure 7 and Figure 8)
- $\overline{\text{XRE}}$ low-to-high transition after XFCLK high (Parameter 4b in Figure 7 and Figure 8)

XBUS: FIFO Data and Control Signals Zero Delay/Skewed From XFCLK High (Continued)

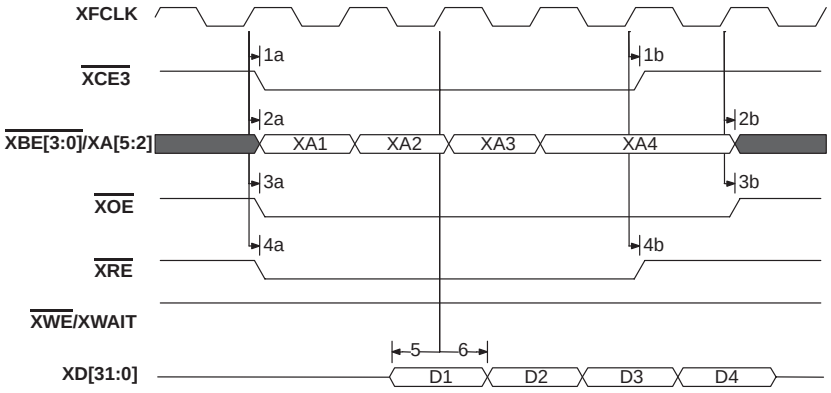


Figure 7. FIFO Read Timing, Glueless Read Mode

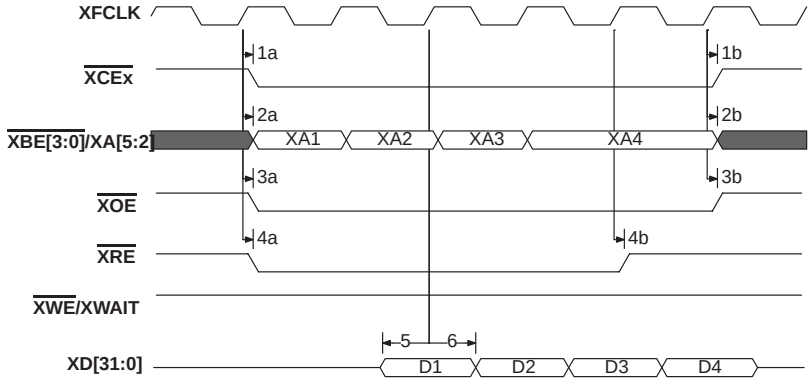


Figure 8. FIFO Read Timing

For FIFO writes, the following parameters have a delay time close to zero:

- $\overline{\text{XCE}}$ high-to-low transition after XFCLK high (Parameter 1a in Figure 9)
- $\overline{\text{XCE}}$ low-to-high transition after XFCLK high (Parameter 1b in Figure 9)
- $\overline{\text{XBE}}$/XA[5:2] valid after XFCLK high (Parameter 2a in Figure 9)
- $\overline{\text{XBE}}$/XA[5:2] invalid after XFCLK high (Parameter 2b in Figure 9)
- $\overline{\text{XWE}}$ high-to-low transition after XFCLK high (Parameter 7a in Figure 9)
- $\overline{\text{XWE}}$ low-to-high transition after XFCLK high (Parameter 7b in Figure 9)
- XD[31:0] valid after XFCLK high (Parameter 8 in Figure 9)
- XD[31:0] invalid after XFCLK high (Parameter 9 in Figure 9)

XBUS: FIFO Data and Control Signals Zero Delay/Skewed From XFCLK High (Continued)

In glueless FIFO interfaces, this zero delay time may violate the hold time of the FIFO. (Internal reference number C631252)

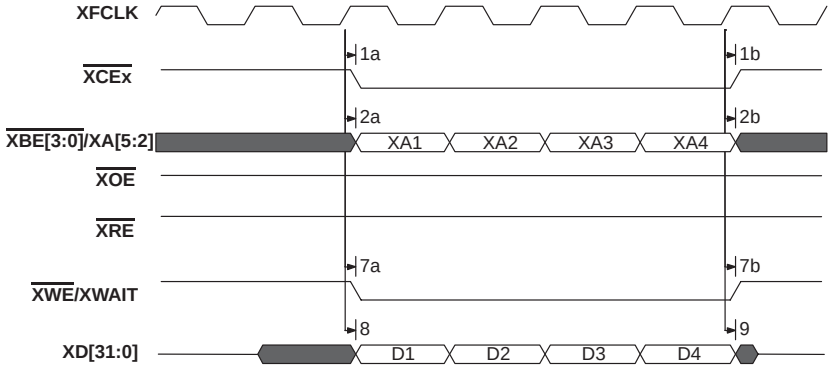


Figure 9. FIFO Write Timing

Workaround: Do not use the glueless synchronous FIFO interface. Use external glue logic to meet the FIFO hold time requirements.

7 Documentation Support

For device-specific data sheets and related documentation, visit the TI web site at: **http://www.ti.com**.

The *TMS320C6203B Fixed-Point Digital Signal Processor* data sheet (literature number SPRS086I or later) describes features of the C6203B device.

The *TMS320C6000 DSP Peripherals Overview Reference Guide* (literature number SPRU190) provides an overview and briefly describes the peripherals available on the TMS320C6000™ DSPs.

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