TMS320VC5402A

Digital Signal Processor

Silicon Errata

SPRZ018
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TEXAS INSTRUMENTS

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Contents

1 Introduction

This document describes the silicon updates to the functional specifications for the TMS320VC5402A silicon. The errata are applicable to:

- TMS320VC5402A (144-pin LQFP, PGE suffix)
- TMS320VC5402A (144-pin MicroStar BGA™, GGU suffix)

1.1 Quality and Reliability Conditions

TMX Definition

Texas Instruments (TI) does not warranty either (1) electrical performance to specification, or (2) product reliability for products classified as “TMX.” By definition, the product has not completed data sheet verification or reliability performance qualification according to TI Quality Systems Specifications.

The mere fact that a “TMX” device was tested over a particular temperature and voltage ranges should not, in any way, be construed as a warranty of performance.

TMP Definition

TI does not warranty product reliability for products classified as “TMP.” By definition, the product has not completed reliability performance qualification according to TI Quality Systems Specifications; however, products are tested to a published electrical and mechanical specification.

TMS Definition

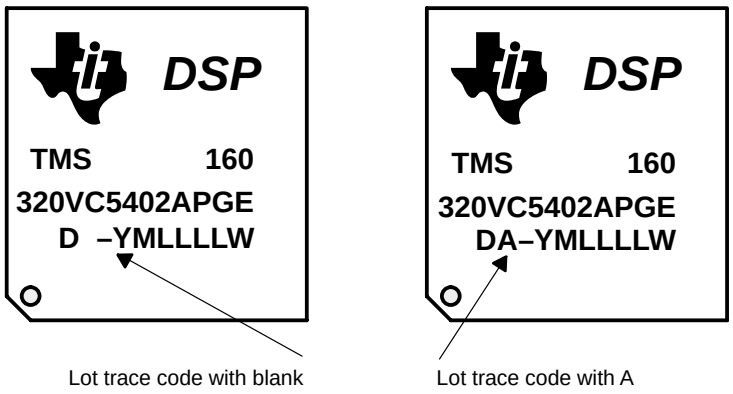
Fully-qualified production device.

MicroStar BGA is a trademark of Texas Instruments.

1.2 Revision Identification

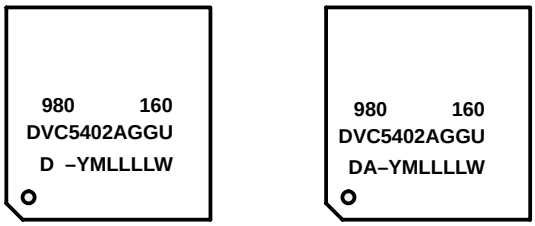
The device revision can be determined by the lot trace code marked on the top of the package. The location for the lot trace codes for the PGE and the GGU packages are shown in Figure 1 and Figure 2, respectively.

Figure 1. Example, Typical Lot Trace Code for TMS320VC5402A DSP (PGE)



Lot Trace Code	Silicon Revision	Comments
Blank (no second letter in prefix)	Indicates Initial Silicon	
A (second letter in prefix is A)	Indicates Silicon Revision A	
B (second letter in prefix is B)	Indicates Silicon Revision B	

Figure 2. Example, Typical Lot Trace Code for TMS320VC5402A DSP (GGU)



NOTE: Qualified devices in the PGE package are marked with the letters “TMS” at the beginning of the device name, while nonqualified devices in the PGE package are marked with the letters “TMX” or “TMP” at the beginning of the device name. Similarly, qualified devices in the GGU package are marked with the letters “DV” at the beginning of the device name, and nonqualified devices in the GGU package are marked with the letters “XDV” or “PDV” at the beginning of the device name.

2 Known Design Marginality/Exceptions to Functional Specifications

Table 1. Summary of Advisories

Description	Revision Affected	Page
HPI HINT	All revisions	5
Far Branches/Calls/Interrupts from Active Repeat Blocks (BRAF)	All revisions	6
Round (RND) Instruction Clears Pending Interrupts	All revisions	7
TOUT Jitter	All revisions	7
CPU Read/DMA Write	Initial silicon	7
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Advisory *HPI HINT*

Revision(s) Affected: All revisions

Details: The HPI will become locked up, with HRDY stuck low, if both the host processor and the TMS320VC5402A CPU write a one (1) to HINT as the same time.

Workaround: Avoid performing redundant operations to the HINT bit. Both the Host and the CPU should check to see if HINT is set before trying to write a one (1) to this bit.

For:	If...	Then...
the HOST	HINT is ***not*** set...	Do not try to clear HINT by writing a one (1) to it, because the CPU may try to set it.
the CPU	HINT is ***already*** set...	Do not try to set HINT again by writing a one (1) to it, since the HOST may try to clear it.

Advisory *Far Branches/Calls/Interrupts from Active Repeat Blocks (BRAF)*

Revision(s) Affected: All revisions

Details: When a block repeat is interrupted by a far call, far branch, or interrupt to another page; and a program memory address in the called routine happens to have the same lower 16 bits as the block-repeat end address (REA), a branch to the 16-bit block-repeat start address (RSA) is executed on the current page until the block-repeat counter decrements to 0. The XPC is ignored during these occurrences.

Workaround: Use one of the following workarounds:

1. If the called routine must be on a different page and has a program memory address that has the same lower 16 bits as the REA, save ST1 and clear the BRAF in the vector table before entering the called routine with the following two instructions:

```
PSHM ST1
RSBX BRAF
```

   Then, restore ST1 before returning from the called routine. In the case of an interrupt service routine, these two instructions can be included in the delay slots following a delayed-branch instruction (BD) at the interrupt vector location. Then, the ST1 is restored before returning from the routine. With this method, BRAF is always inactive while in the called routine. If BRAF was not active at the time of the call, the RSBX BRAF has no effect.

2. Put the called routine on the same page as the interruptible block-repeat code. This can be achieved automatically by placing the interrupt vector table and the interrupt service routines or other called routines on the overlay pages. If this approach is used, far branches/calls are not necessary and the situation is completely avoided.
3. Avoid putting the called routine on other pages where a program memory address has the same lower 16 bits as the REA.
4. Use the BANZ instruction as a substitute for the block repeat.

Advisory — *Round (RND) Instruction Clears Pending Interrupts*

Revision(s) Affected: All revisions

Details: The RND (round) instruction opcode is decoded incorrectly and will write to the interrupt flag register (IFR) with the data from the data write bus (E bus). Therefore, it could cause the pending interrupt to be missed.

Workaround: Do not use the RND instruction. Replace the RND instruction with an ADD instruction as follows:

For this instruction ...	Use ...
`RND src[,dst]`	`ADD #1,15,src[,dst]`

Advisory — *TOUT Jitter*

Revision(s) Affected: All revisions

Details: When the CLKOUT divide factor is set to a non-zero value, the timer output exhibits jitter because pulse width differ by one or two CLKOUT periods.

Workaround: Set DIVFCT to 0.

Advisory — *CPU Read/DMA Write*

Revision(s) Affected: Initial Silicon

Details: A CPU read of on-chip memory can be corrupted if it reads the address that was last written by the CPU, while external DMA writes are occurring. The following characteristics apply to this problem:

- This problem happens when external DMA writes are active (i.e., whenever the destination of a DMA transfer is an external memory address (program, data, or IO)).
- The source of the DMA transfer is not relevant to the problem.
- The DMA and CPU do not have to be accessing the same block of memory for the problem to occur.
- This can affect CPU reads of DARAM memory blocks.

Workaround: The following workarounds apply:

1. Rearrange code such that CPU reads of the last address written by the CPU do not occur. For example in sections of code where this is a problem, always precede a CPU read with a write of a different address.
2. Do not use the DMA controller to perform external writes.

Advisory	*DMPREC*

Revision(s) Affected: Initial silicon

Details:

When updating the DE bits of the DMPREC register while one or more DMA channel transfers are in progress, it is possible for the write to the DMPREC to cause an additional transfer on one of the active channels.

The problem occurs when an active channel completes a transfer at the same time that the user updates the DMPREC register. When the transfer completes, the DMA logic attempts to clear the DE bit corresponding to the complete channel transfer, but the register is instead updated with the CPU write (usually an ORM instruction) which can set the bit and cause an additional transfer on the channel. Refer to the example below for further clarification:

Example:

DMPREC value = 00C1h, corresponding to the following channel activity:

Channel 0 – enabled and running.	(DE0 = 1)
Channel 1 – disabled.	(DE1 = 0)
Channel 2 – disabled.	(DE2 = 0)
Channel 3 – disabled.	(DE3 = 0)
Channel 4 – disabled.	(DE4 = 0)
Channel 5 – disabled.	(DE5 = 0)

If the following conditions occur simultaneously:

- Channel 0 transfer completes and DMA logic clears DE0 internally.
- User code attempts to enable another channel (e.g., ORM #2, DMPREC)

The user code will re-enable channel 0 (DMPREC value written = 00C3h), and an additional, unintended transfer will begin on channel 0.

Workaround:

There are a few conditions under which this problem does not occur. If all active DMA channels are configured in ABU mode or in autoinitialization mode, then the problem does not occur because the channels remain enabled until they are disabled by user code. The problem is also avoided in applications that use only one DMA channel at a time.

Systems that use multiple DMA channels simultaneously in multiframe mode without autoinitialization are most likely to have this problem. In such systems one of the following methods can be used to avoid the problem:

- Always wait for all channels to complete existing transfers before re-enabling any channels, and always enable all channels at the same time.
- Before enabling a channel, check the progress of any on-going transfers by reading the element and frame counts of each active channel. If any active channel is within two element transfers of completing a block transfer, then wait until the active channel completes the block transfer before writing to the DMPREC register. Otherwise, if all active channels have more than two element transfers left in a block transfer, it is safe to update the DMPREC register.

DMPREC (Continued)

Workaround: A hardware workaround has been implemented on the 5402A, Revision A device. This solution consists of an additional memory mapped register, DMCECTL (DMA Channel Enable Control), at address 0x003E, with the following characteristics:

Figure 3. DMA Channel Enable Control Register (DMCECTL)

15	14 6	5	4	3	2	1	0
Set/Reset	Reserved	CH5	CH4	CH3	CH2	CH1	CH0
W–0	W–0	W–0	W–0	W–0	W–0	W–0	W–0

Table 2. DMA Channel Enable Control Register (DMCECTL) Description

BIT FIELD	RESET| VALUE	DESCRIPTION
CH0–CH5	0	These bits are used in conjunction with the set/reset bit to write to the individual DE bits of the DMPREC register. 0) Corresponding DE bit in the DMPREC register is unaffected by the Set/Reset bit. 1) Corresponding bit in the DMPREC register is set or cleared depending on the state of Set/Reset.
Reserved	0	Reserved.
Set/Reset	0	Sets or clears individual DE bits of the DMPREC register according to the values of CH0–CH5. 0) Clears the DE bits of the DMPREC register as specified by CH0–CH5. 1) Sets the DE bits of the DMPREC register as specified by CH0–CH5.

Use this register to enable or disable DMA channels instead of writing to the DMPREC register. For example, to enable channels zero and five, write a value of 0x8021 to address 0x03E. In this case only DE0 and DE5 of the DMPREC are set to 1. Or for another example, to disable channel one, write a value of 0x02 to address 0x03E. In this case only DE1 is cleared. Note that this is a write-only register

Advisory — *On-Chip Oscillator Support*

Revision(s) Affected: Initial silicon

Details: On-chip oscillator does not function properly.

Workaround: Avoid using crystal as clock source with the on-chip oscillator. Functionality described in *TMS320VC5402A Fixed-Point Digital Signal Processor* data manual (literature number SPRS015) is not supported until silicon revision A.

3 Documentation Support

For device-specific datasheets and related documentation, visit the TI web site at: **http://www.ti.com**

To access documentation on the web site:

1. Go to **http://www.ti.com**
2. Open the "**Products & Services**" dialog box and choose "**Digital Signal Processors**"
3. Scroll to the "**C54x™ DSP Generation**" or "**C55x™ DSP Generation**" and click on "**DEVICE INFORMATION**"
4. Click on a device name and then click on the documentation type you prefer.

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