WHITE PAPER

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TEXAS INSTRUMENTS

KeyStone™ II-based processors: 10Gb Ethernet as an optical interface between remote radio head and signal processing card for radars

Introduction

With the progress being made in the processor technology, processors are becoming extremely powerful miniature complex systems, with a multifold increase in high-speed peripherals to communicate to the external world. The line of processors based on KeyStone™ II architecture from Texas Instruments (TI) are complex heterogeneous processors which have tremendous processing power offering up to Dhrystone 19600 DMIPS (Dhrystone million instructions per second), 198.4 GFLOPS (Giga floating-point operations per second) and 352 GMACS (Giga multiply and accumulation operations per second). This portfolio of devices (66AK2H14, 66AK2E05 and AM5K2E04 SoCs) come with integrated DSP cores and ARM® Cortex®-A15 MPCore™ , and have a wide array of peripherals like multiple 10GbE (Gigabit Ethernet) Ports, 1GbE Ports, PCIE lanes, USB 3.0 etc. These processors are used to reduce the board complexity and BOM costs of the systems used in mission-critical radars, high-performance computing, media gateways, avionics, and general-purpose embedded computing for industrial, networking and mission-critical applications.

This white paper deals with how the 10GbE interface and the processing power of the processors based on KeyStone II architecture helps to address complex time-critical systems like radar systems.

The conventional radars use the SFP/SFP+ interface to transfer a high bandwidth of data from the analog front end (AFE; viz the radio head) to the signal processing modules. The radio head receives the data from the high-speed ADCs via low-voltage differential signaling (LVDS)/JESD204B interface on glue logic and down converts them to the base band frequency. The down-converted data are sent to the signal processing modules. Signal processing modules need an FPGA-based SFP/SFP+ (small form factor pluggable transceivers) interface to receive the data which is then sent to signal processors (SPs) via SRIO (Serial RapidIO®) or PCIe interface for signal processing.

With the integration of a 10GbE interface on the processor, these 10GbE lanes can be directly used to transfer the data from the AFE to the SPs. The 10GbE lanes on KeyStone II-based processors support an XFI interface which can be used to connect to the optical fibers over the XFP (10 Gigabit small form factor pluggable) interfaces. Optical fibers can also be connected over the SFP/SFP+ interfaces by making use of appropriate XFI to SFI converters. This can be done with the help of supplemental hardware like TI's ***DS100DF410*** *retimer. Thus optical fibers interface through the XFP/SFP+ interface support high bandwidth of data exchange between the AFE and SPs.*

Radar

Radar systems are mission-critical systems extensively used for object detection for defense, search and rescue operations. Radar systems transmit pulses of radio waves or microwaves which are reflected back from the object in their path with a part of the original transmit energy sent back to the receive antennas. Signals received on the antennas are usually of low energy and are recovered using a combination of electronic amplifications and complex signal processing.

A typical radar system consists of a processing module, AFE (i.e., the radio end) and the power amplifiers. Based on the application, the processing module and AFE might be together in a single card or in a closed box in different cards, or in different cards in separate locations. These modules needs to be connected via high-speed interfaces characterized by low latency and sustained throughput. The SFP/SFP+ connectors are conventionally used in the radar for communication between the radio head and the processing cards. The SFP/SFP+ connectors with optical fibers carry data of different bandwidths varying from 1Gb/s to 10Gb/s, across varying distance based on the different wavelength.

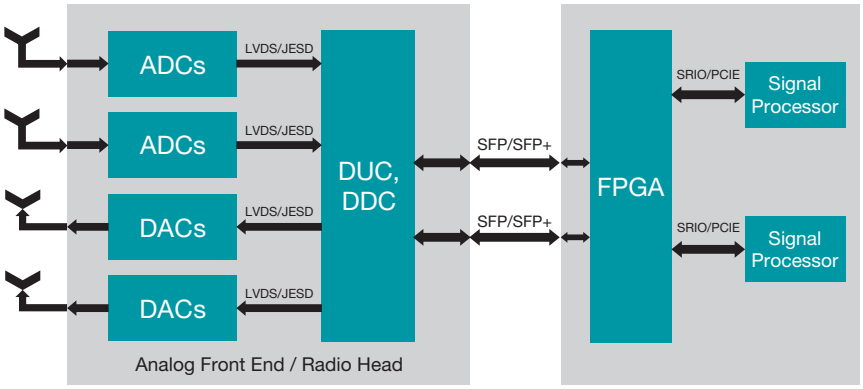

Figure 1: Conventional radar

SFP/SFP+ interfaces are commonly used in radars like:

- Airborne radars
- Ground-controlled interception radars
- SONARS in submarines and naval ships
- Costal and harbor surveillance radars
- Wide band radar receivers

KeyStone II 10Gigabit XFP/SFP+ interface for radar systems

KeyStone II-based processors introduce 10GbE to a whole new class of devices. The XFI interface on these devices replaces the older four-lane XAUI interface by a single-lane SERDES interface. 10 gigabit ports on the processors adhere to the following industry standards:

- Supports IEEE 802.3 specifications
  - 10GBASE-R (10G)
  - 10/100/1000 Base-T (1G)
- Supports IEEE 1588 (v2008) specification

- Supports XFI SFF INF-8077i spec for 10 GbE
- Supports SFF-8431 (i.e., SFI for SFP+) with a supplement hardware (ex.: TI's DS100DF410 retimer)
- Supports Serial GMII (SGMII) specifications for 10/100/1000Mb

The XFI SFF INF-8077i spec enables the ports to be connected over optical fiber using the XFP interfaces. Below is the diagram of an XFP interface, which converts XFI electrical interface to the optical interface into pluggable form factor.

Figure 2: XFP interface

ADCs on the analog front end digitizes the signals, which are then fed to the digital signal processors (DSPs) for processing. As the system complexity increases, a huge set of signals from different sensor nodes that are digitized by the ADCs has to be synchronously transferred to the DSP maintaining the real-time coherency of the system. This stringent real-time requirement demands a rugged communication medium of sustained high bandwidth and low latency between the analog front end and the processing module. The 10GbE serves to be a medium of communication in such systems.

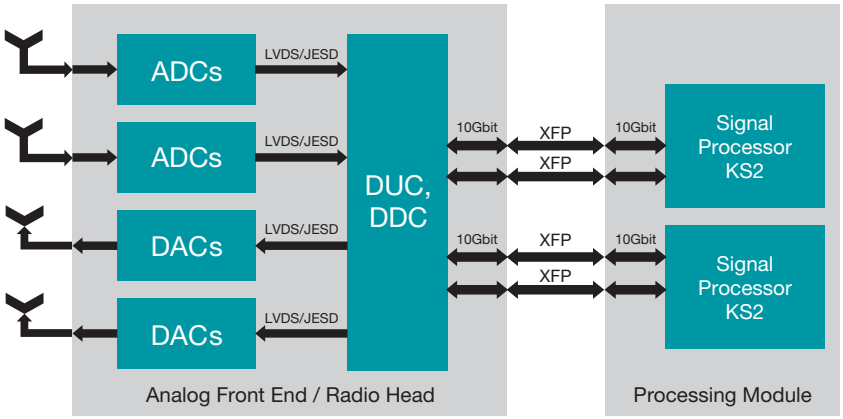

Figure 3: Proposed radar sytem with XFP interface

The 10GbE ports on KeyStone II-based processors can be used to directly communicate with the AFE over the XFP/SFP+ interface reducing the board cost and complexity of the conventional radar systems. Once the signals are digitized by the ADCs they are received by glue logic over the LVDS/JESD interface and

down convert the digitized signals from the IF freqeuncy to the base band frequency. These glue logic on the AFE have a small 10GbE IP core which packetizes these base band data and continously streams them over the XFP/SFP+ interface to the KeyStone II-based processors for signal processing. The packets that are continously received on the 10GbE hardware on the processor are coherrent to the processor cache thus significantly reducing the software latency involved. The hardware coherence controller presents part of the MSMC (Multicore Shared Memory Controller) along with the snoop controller maintains the coherency between the I/O issuing necessary read and writeback invalidate commands to the snoop controller, thus mainitaing a hardware controlled cohorency for I/O.

Along with the 10GbE hardware, the **Network Coprocessor** (NetCP) module on the KeyStone II-based processor can be leveraged for packet classification to reduce the overall system latency for implementing the 10GbE solution. NetCP is capable of classifying standard layers 2–4 (i.e., MAC, IPV4/IPV6, UDP/TCP). It also provides cryptography support (i.e., IPSEC ESP/AH, SRTP). IP re-assembly acceleration is also provided. Some KeyStone II-based processors, such as the 66AK2H14, 66AK2E05 and AM5K2E04 SoCs, can fully offload IP re-assembly as well as assist in firewall (ACL) processing.

The XFI interface on KeyStone II-based processors, which is a single lane SERDES interface, also provides a significant advantage in terms of power by consuming a few hundred of miliwatts compared to an earlier XAUI-based solution which consumes more than 1W of power.

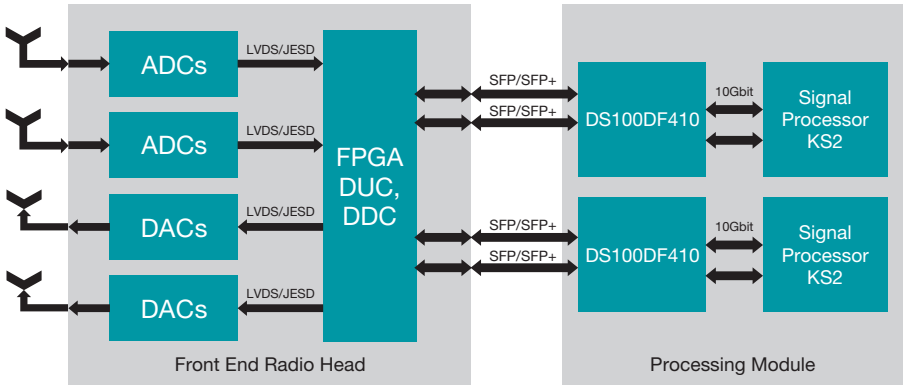

Figure 4: Proposed radar sytem with SFP+ interface with the supplemental hardware DS100DF410 retimer for converting XFI to SFI interface

Note: LRM (Long Reach Multi-mode optical fiber) and complaince to SFI has not been characterized yet.

Example showing the electrical interface for KeyStone II-based processors 10Gb Port and XFP module

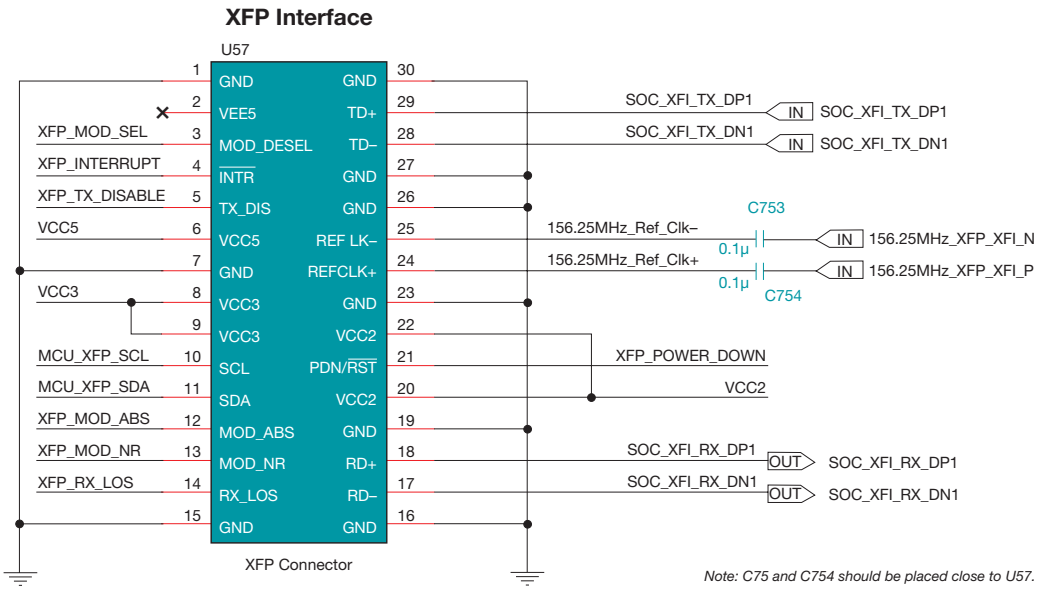

Figure 5: Typical electrical interface for XFI-to-XFP connector

Signals and interface

Signal name	Signal source
SOC_XFI_TX_DP1/DN1	SERDES TX differential pair from the KeyStone II processor
SOC_XFI_RX_DP1/DN1	SERDES RX differential pair from the KeyStone II processor
156.25Mhz_XFP_XFI_N/P	Input reference clock of 156.25 MHz driven from the clock source like CDCM6208
MCU_XFP_SCL	Controlled by the board management microcontroller
MCU_XFP_SDA	Controlled by the board management microcontroller
XFP_MOD_SEL	Control information for XFP module controlled by board management microcontroller: Module de-select; when held low, allows module to respond to 2-wire serial interface
XFP_INTERRUPT	Control information for XFP module controlled by board management microcontroller: Indicates presence of an important condition which can be read over the 2-wire serial interface
XFP_TX_DISABLE	Control information for XFP module controlled by board management microcontroller: Transmitter disable; turns off transmitter laser output
XFP_MOD_ABS	Indicates module is not present. Grounded in the module
XFP_MOD_NR	Module not ready; indicating module operational fault
XFP_RX_LOS	Receiver loss of signal indicator

Conclusion

10GbE used over optical interface as a communication channel between the remote radio head and the processing modules in radar-type systems offers a low-latency sustained throughput and also eliminates the glue logic needed for protocol translation on the processing cards. This along with unmatched signal-processing capability of the processors based on KeyStone II architecture can be effectively used to reduce the overall cost and complexity of systems such as radar systems.

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