WHITE PAPER

Punya Prakash,
Product Marketing Manager,
Sitara™ processors

Kazunobu Shin,
Systems Engineer,
Sitara™ processors

Texas Instruments

TEXAS INSTRUMENTS

Power optimization techniques for energy-efficient systems

Introduction

Advancement in technology has aided progression of automation and control systems that provide a cohesive operation of various mechanical, electronics and lighting systems. Apart from offering a convenient lifestyle, these solutions play an essential role in energy monitoring. These solutions require diligent understanding and optimization of complete systems.

While each solution has a common goal of energy conservation, they have completely different system requirements. The Texas Instruments (TI) Sitara™ processor solutions offer the flexibility to design application-specific systems. The latest Sitara AM335x processors provide a scalable architecture with speed ranging from 300MHz to 1GHz. In addition to the scalable frequency, pin-to-pin compatible devices enable customers to innovate and develop a highly flexible and comprehensive range of solutions.

This white paper will outline system choices and their impact on the system power. It will provide a comprehensive overview of the processor power management features and discuss the key contributors to the overall system power.

Building blocks of a power-efficient system

Several techniques can be implemented to reduce active and static power consumption. Typically the highest impact on power consumption is due to four key components – the processor, DDR memory, display and power design, as shown by Figure 1. Power optimization can be achieved by selecting the right system components and designing dynamic software architecture.

System Power
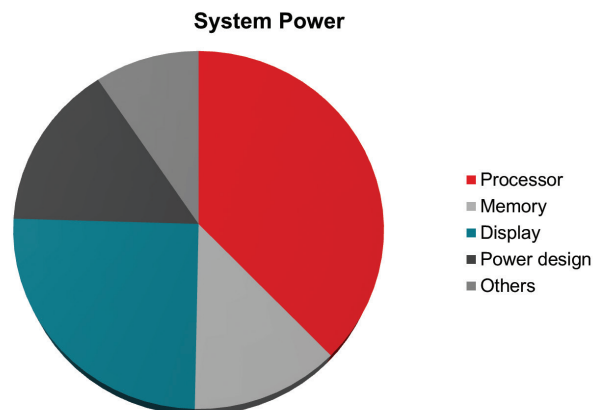
- Processor
- Memory
- Display
- Power design
- Others

Figure 1: Power consumption of various key system components. This figure assumes 85 percent power design efficiency, DDR3 memory and active display.

Processor

TI's Sitara AM335x processors provide highly flexible power management architecture. Depending on the application, the processor and core can be adapted to take advantage of the best performance and power configuration.

The power, reset and clock management (PRCM) module, shown in Figure 2, and the Linux™ power management software stack can be used to optimize AM335x processor power. This minimizes power consumption of the processor since it aids control of the core

modules. Voltage domain is critical in controlling different operating performance points (OPP). OPP is a combination of processor voltage and frequency that can be controlled by the user for optimal processor power for any given performance requirement.

The voltage control and the voltage regulator are external and enabled through a power management IC (PMIC). While the system is active, individual power domain(s) and all its modules can be turned off. Similarly, specific modules can also be controlled. While one module is functional, another could be completely turned off when not in use.
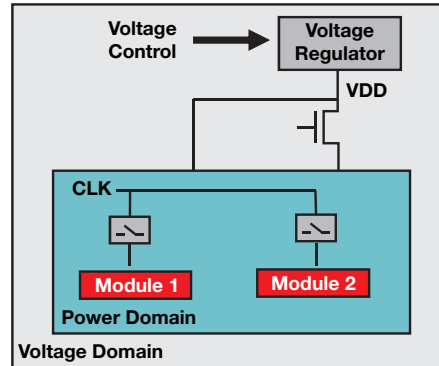

Figure 2: PRCM architecture.

TI's Sitara AM335x processors support separate voltage domains for MPU and CORE. By having different voltage domains, MPU and CORE OPPs can be configured and controlled independently.

Depending on the application requirement, the MPU OPP can be dynamically changed. The AM335x processors support five different operating points: OPP50, OPP100, OPP120, Turbo and Nitro. With a wide frequency range of 10MHz to 1GHz, it provides flexible configuration. Custom processor frequency can be supported with a dedicated processor DPLL. Figure 3 shows MPU voltage and performance at the five different supported OPPs.

The CORE OPP supports two voltage operating points and interconnects frequency sets. Lower CORE OPP can be used for significant power savings provided the bus throughput supported by lower CORE OPP is sufficient for system performance requirements. CORE OPP voltage and performance operating points are shown in Figure 4 on the following page.

VDD_MPU OPP	VDD_MPU	ARM® Cortex™-A8
Nitro	1.325 V	1 GHz
Turbo	1.26 V	800 MHz
OPP120	1.2 V	720 MHz
OPP100	1.1 V	600 MHz
OPP50	0.95 V	300 MHz

Figure 3: Microprocessor (MPU) operating performance points (OPPs).

VDD_CORE OPP	VDD_CORE	DDR3, DDR3L	DDR2	mDDR	L3 and L4
OPP00	1.1 V	400 MHz	266 MHz	200 MHz	200 MHz and 100 MHz
OPP50	0.95 V	–	125 MHz	90 MHz	100 MHz and 50 MHz

Figure 4: CORE operating performance points (OPPs).

DDR memory

TI's Sitara AM335x processor memory controller supports a breath of DDR memory – LPDDR1, DDR2, DDR3 (L) (RS). While the period of availability for each DDR option is determined by the memory vendor(s), the choice of the memory has an impact of up to 20 percent on the overall system power.

In general, the LPDDR memory has the lowest active and stand-by power. In addition to this, LPDDR and DDR2 memory is supported at OPP50, which reduces the power consumption significantly in active mode when the reduced memory bandwidth is sufficient for applications.

VTT termination is required for better signal integrity in applications where higher DDR speed is essential. This added integrity comes at the cost of some power dissipation. DDR VTT termination can be avoided when single DDR3/DDR3L device is used with the AM335x processor and PCB board is designed by following TI's recommended PCB design guidelines. The **Sitara AM335x processor datasheet** describes the PCB design guidelines to implement this solution.

Display

There are several ways a display-based application can be tailored for power optimization. The processor also offers an optional resistive-touch controller and SGX graphics accelerator. Using the AM335x PRCM module, each of these sub-systems could be disabled while not in use.

Applications can be developed to turn off the display panel after a certain duration or through a manual event and could save up to 23 percent of processor power. The display can be re-enabled through external events such as touch or proximity sensor.

In addition to this, the display resolution, refresh rate and brightness of the display can be tweaked to achieve higher system power optimization.

Power design

TI provides an array of PMIC solutions for the AM335x processor, based on the application requirements. The PMIC solution can be selected to optimize the solution. As shown in Figure 5, each of the PMIC solutions supports a variety of processor frequency and memory configuration. In addition to this, some additional features can directly benefit the system cost of the solution.

	TPS65217x				TPS65910x		TPS650250
	A	B	C	D	A	A3	
Battery charger	Yes				No		No
Boost	WLED backlighting				5-V boost		No
AM335x OPP	OPP50, OPP100	OPP50, OPP100, OPP120, Turbo, Nitro			OPP50, OPP100, OPP120, Turbo, Nitro		OPP50, OPP100
Power	3 DCDC @ 1.2A 4 LDO				2 DCDC @ 1.5A 1 DCDC @ 1A 9 LDO		1 DCDC @ 1.6A 2 DCDC @ 0.8A 3 LDO
Input voltage range	2.7 – 5.8 V				2.7 – 5.5 V		2.5 – 6.5 V
DVFS / SmartReflex™	Yes				Yes		No
RTC-only mode	Yes				Yes		No
DDR	DDR2, LPDDR1		DDR3	DDR3L	DDR2, LPDDR1	DDR3	DDR2, LPDDR1, DDR3
Package	48-pin QFN, 6mm × 6mm				48-pin QFN, 6mm × 6mm		32-pin QFN, 5mm × 5mm
T_A	−40°C to 105°C				−40°C to 85°C		−40°C to 85°C

Figure 5: TI offers a range of PMIC solutions for TI's Sitara™ AM335x processors.

The TPS65217x supports portable solutions with the integrated battery charger. Backlight for display-based applications can be supported using this PMIC solution. The TPS65910x provides support from 300MHz – 1GHz and provides advanced power management features such as SmartReflex™ and RTC mode support aids flexible power management architecture. The third variant, TPS650250, is a simple, low-cost solution that supports OPP50 and OPP100.

There is a trade-off between the board footprint, BOM cost and efficiency when selecting power IC components. The efficiency of the power ICs can impact the system power significantly. Dissipation from the various power IC components could penalize the overall system contributing to the system power consumption. It is challenging to quantify this due to the broad spectrum of applications that have a variety of board cost and size targets. The power IC datasheet provides efficiency curves at certain operating conditions. Understanding efficiency at target input and output voltages and selecting the right DC-DC converter to meet system power consumption target is important to design power-efficient systems.

Processor power optimization practices

Power latency trade-off

TI's Sitara AM335x processors offer several deep sleep (DS) modes, which are directly proportional to the power consumption of the core processor. There are several factors which determine the DS mode – period of inactivity, manual over-ride and the active peripherals connected to the core. While the deepest mode, DS0, can provide the lowest core power, it also has to bring longer latency to wake the system. Complementary to the DS mode, the stand-by mode offers faster wake-up latency. Details of each of these power modes are shown in Figure 6 on the following page.

TI's Sitara AM335x processors support five DPLLs, which in turn can support independent frequency control, regulate processor, DDR and display clock frequency based on the application needs. In addition to this, six dual-voltage I/O banks can be configured for 1.8V or 3.3V. The 1.8V I/O will benefit reduction of processor power consumption.

Power modes	Processor state	Wakeup sources
Standby	All power supplies are ON. Main oscillator is ON. All DPLLs are in bypass. PD_PER and PD_WKUP power domains are ON. DDR is in self-refresh.	Any GPIO pins
Deepsleep1	All power supplies are ON. Main oscillator is OFF. All DPLLs are in bypass. PD_PER and PD_WKUP power domains are ON. DDR is in self-refresh.	DeepSleep0 wakeup sources and USB remote signal
Deepsleep0	All power supplies are ON. Main oscillator is OFF. All DPLLs are in bypass. Only PD_WKUP power domain is ON. DDR is in self-refresh.	GPIO0 bank, Timer1, Touch-screen controller, UART0, I^2C0, RTC alarm
RTC-only	RTC timer remains active and all other device functionality is disabled.	RTC alarm, EXT_WAKEUP pin

Figure 6: DS modes excel + wake source.

The AM335x processor supports various wake sources such as the resistive touch, UART0, USB or GPIO0 with 32 pins. In addition to these, RTC alarm is also supported, which can be used for timer-based wake.

Additional information on Texas Instruments' power management architecture is described in TI's white paper on "**Power saving techniques lead to ultra-low-power processors for battery-operated devices**."

Power-efficient display-based application

In order to provide a better perspective on the various topics discussed here, this section will describe a display-based application optimized for efficient power solution. In this Wi-Fi® enabled application, TI's Sitara AM335x processor is used to process the data aggregated from various end nodes.

If USB and Ethernet sub-systems are not used in this application, using the flexible PRCM architecture these modules can be disabled.

1. Data aggregation from various nodes, the end nodes are connected to the processor through I^2C and Wi-Fi.
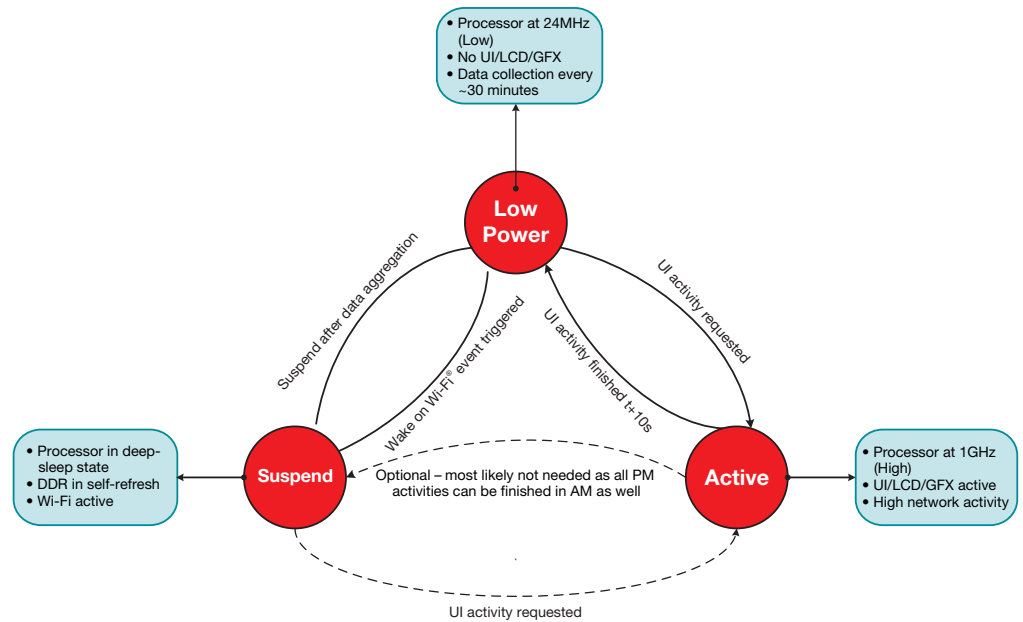2. Wi-Fi is connected through SDIO and GPIO is used as the wake source.

Figure 7: State diagram of example application for optimized power.

The state diagram in Figure 7 depicts system transition from active mode to low-power mode. In active mode, the processor is running at 1GHz and has the display and graphics engine enabled. When the high network activity reduces and there is no user interface (UI) activity for over 10s, the system could transition to a low-power state. The system can be rendered active with any UI activity such as a proximity sensor or touch event.

In low-power mode the display and graphics engine modules are disabled. In addition to turning off the display, the processor frequency can be reduced to as low as 10MHz. After data collection every, say 30 minutes, the processor can be suspended to a deep-sleep state. In suspend state, the DDR is in self-refresh. A Wi-Fi event can wake the processor through a GPIO and restore the processor in low-power mode.

The processor can be suspended to a deep-sleep state from active mode directly; any wake event while in suspend mode will restore the system to active state.

Conclusions   With rising energy costs, system automation is an increasing trend. Investments in these systems require a scalable solution with low power/performance to high performance. TI's Sitara AM335x processor offers a flexible architecture with high processing capability for computationally intensive applications. With the various power and performance knobs to turn, users can benefit from an intelligent whole product that has been designed for efficiency which provides a competitive advantage.

Resources   For more information about TI's Sitara AM335x processors, please visit **ti.com/am335x**.

For more information about power solutions for TI's Sitara AM335x processor, please visit **ti.com/pmic**.

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