Brett Larimore,
Application Engineer;
Bilal Akin, Ph.D.,
Application Engineer;
Nene Hrishikesh,
Application Engineer;
Manish Bhardwaj,
Application Engineer;
Texas Instruments

TEXAS INSTRUMENTS

HVAC Dual-AC Motor Control with Active PFC Implementation Using Piccolo™ MCUs

Introduction

Cost-sensitive drives such as heating, ventilating and air conditioning (HVAC) appliances use variable-speed drives to maximize efficiency and comfort; most of these applications employ more than one motor to handle ventilation and compression.

But with various regulations limiting the input-current harmonic content, the power factor correction (PFC) stage has become an integral part of most rectifier designs. For example, the IEC 61000-3-2 standard defines the harmonic components that an electronic load can inject into the supply line, forcing manufacturers to minimize low-order input harmonics.

This paper discusses how the low-cost, 32-bit Piccolo™ microcontroller from Texas Instruments provides a true single-chip solution for multiple motor drives, including the front-end PFC. Implementation of controlling two motors using field-oriented control (FOC), and an interleaved PFC using a single controller is described/illustrated. The overall system helps users reduce the number of critical components in the bill of materials, reduce the size of bulky passive components, improve efficiency, minimize input-current harmonic content, maximize PFC, precisely regulate the DC bus, and save development time.

Overview

Many cost-sensitive applications like heating, ventilating and air conditioning (HVAC) systems use variable-speed drives in order to run more than one motor and to manage compressors and fans. Most designs require separate controllers for each motor and another to implement power factor correction (PFC). Now, thanks to the recent architectural and performance enhancements of the 32-bit Piccolo™ MCU from Texas Instruments (TI), managing two motors with active PFC using a single chip is possible without significant increases to system cost.

One of the key considerations when selecting an MCU architecture for this type of application is the amount of functionality integrated onto a single chip. By performing tasks in the digital domain, component count can be reduced, which directly reduces system cost and improves reliability. Efficient control across all speed ranges enables developers to design power device circuits to optimally match the capacity and needs of their applications, increasing power and cost efficiency.

Controlling a motor, for example, might require a control loop operating with a frequency as high as 20 kHz. PFC, on the other hand, typically requires an operating frequency of 100 kHz. Thus, to reliably implement such high-frequency control algorithms – in this case, two controlling motors and one managing PFC – an MCU must be able to process computations quickly and efficiently with little latency.

The ability to control multiple motors not only reduces system cost but improves overall power efficiency and performance. For applications that operate dual motors, having both motors controlled by the same MCU enables the controller to coordinate how quickly it ramps one motor up relative to the speed of the other. And because both motors draw from the same current source, the PFC implementation can be coordinated as well for better results.

Field-oriented control (FOC) across all speed ranges enables developers to design power device circuits to optimally match the capacity and needs of their applications, increasing power and cost efficiency. This also results in smoother operation and better performance, reducing issues such as torque ripple and vibration that can impact operating life.

The FOC structure is supported by a sliding mode observer (SMO) to estimate the rotor position, yielding an accurate position feedback down to 50 RPM, which is low enough for HVAC applications. In addition to removing these sensors from the system, going sensorless

also eliminates the need to install interfaces to the sensors. Not only are systems cheaper to manufacture, there are fewer points of failure.

On the other hand, PFC ensures that the current waveform follows the voltage waveform and regulates the output DC voltage to a constant value, regardless of any changes in load or input conditions. When PFC is implemented in an active, digital fashion, it can be more precise and eliminate any phase shift between voltage and current.

PFC also has an impact further down the power chain. Because power companies need to be able to generate greater power capacity to accommodate spikes, electronics manufacturers have been encouraged to employ technologies such as PFC to smooth out power draw. In some cases, PFC has been mandated – IEC 60730 requires PFC in white goods sold in European markets.

Analog or passive implementations of PFC are locked into a single mode and have a limited ability to react to changes in operating conditions. Active or digitally controlled PFC, in contrast, can act on and adapt to changes in operating conditions. For example, when an air conditioner is about to turn on its compressor, PFC can actively compensate for the larger load as it hits.

Active PFC also reduces the number of transients generated, while the flexibility of digital PFC enables developers to employ more complex PFC topologies. Active PFC reduces inductor volume and input filter sizes, thus reducing component costs. Higher efficiency is also possible by load-shedding during low-load conditions.

System overview

The system shown in Figure 1 can serve as a reference design and provide a means to learn and experiment with digital control. For the sake of safety, the power level of the system is kept low, at 80-W maximum. The system is designed to control (FOC) two permanent magnet motors without using incremental encoders.
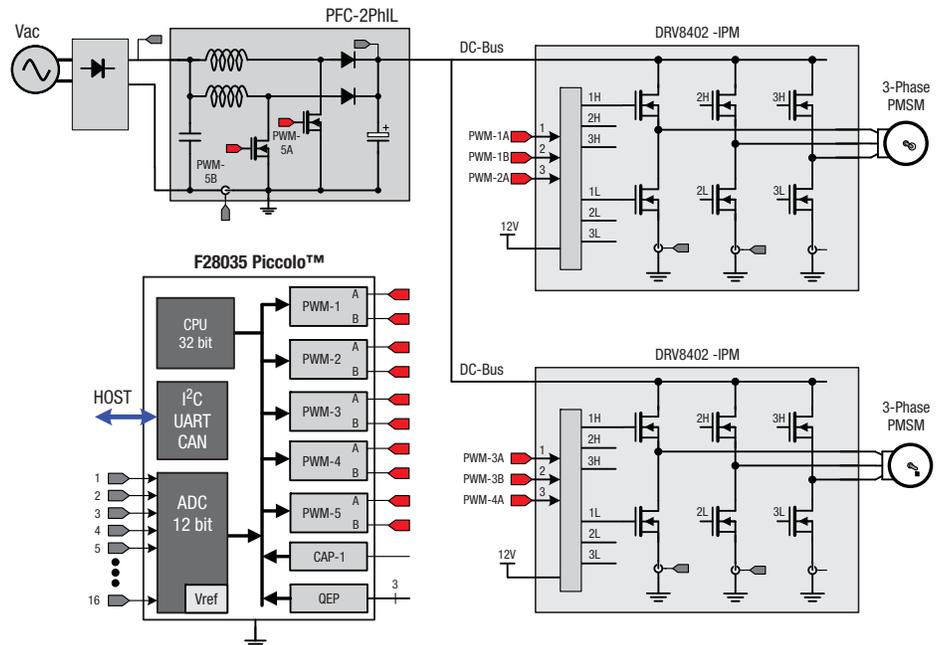

Figure 1. Overall system overview.

The three-phase inverters (TI DRV8402 IPM) run at 10 kHz, accepting single-channel pulse-width modulators as input and generating the complementary PWM pulse internally. The phase currents are sensed through low-side shunt resistors and high-speed op-amps (TI OPA2350). The PFC stage regulates the DC bus voltage and operates at approximately 90 percent efficiency. The PFC control loop frequency is 50 kHz and the switching frequency is 100 kHz. A UART communication header is provided for host control.

The 32-bit fixed-point Piccolo™ (TMS320F28035) microcontroller is used to control both motors and PFC stages. Piccolo MCUs provide hybrid ADCs, allowing flexible conversion starts and continuous sampling up to 5 MSPS, high-resolution PWMs with frequency, duty-cycle modulation up to 150 ps, and two internal and three-tier clock protection for IEC-60730.

Power factor correction

Figure 2 shows the implementation of the PFC stage. The input AC line is passed through an EMI filter and then through a bridge rectifier. The next stage is a two-phase interleaved boost converter that boosts the AC line voltage to the DC bus voltage. Finally, a capacitor at the boost converter output acts as an energy reservoir, reducing the output voltage ripple. The MCU interacts with the hardware by way of feedback signals and PWM outputs.
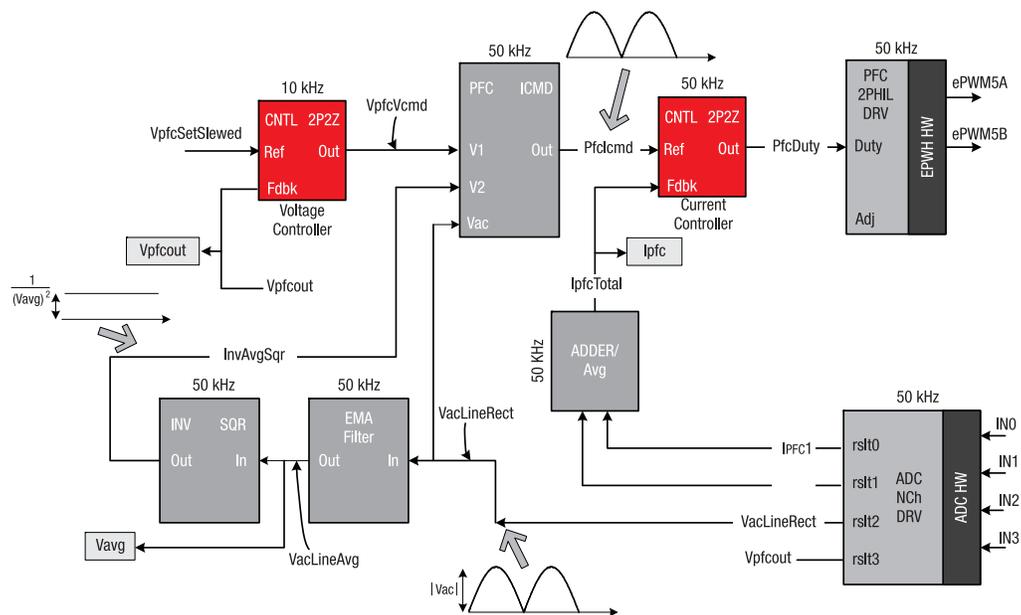

Figure 2. PFC control flow.

Figure 2 also illustrates the PFC algorithm: the system is controlled by two feedback loops. The outer voltage loop regulates the output DC voltage, while a faster inner-current loop wave shapes the input current to maintain a high power factor at the input. The MCU achieves PFC by controlling the duty cycle of the PWM outputs, driving the two phases such that the rectified input current – which is a numerical addition of the two phase currents – follows the rectified input voltage while providing load and line regulation at the same time. The current controller is executed at a rate of 50 kHz (half the PWM switching frequency), while the voltage controller is

executed 5× slower. A phase management block could be added to provide a means to share the load between the two phases, facilitating phase-shedding to increase system efficiencies at low loads.

Improving PF and THD under high-line and low-load conditions

To control the PFC stage, the leg current on each phase is sampled at the midpoint of the PWM cycle. However, under high-line and low-load conditions, the input current stays discontinuous for a longer portion in each sine quarter of the input line voltage; in other words, PFC operates in discontinuous conduction mode (DCM).

During DCM operation, the sensed current is not equal to the average current (averaged over one switching cycle). This results in a distorted input current waveform during DCM operation in each quarter cycle – and possibly a jump in the input voltage current sine quarter when the input current crosses the DCM/continuous conduction mode (CCM) mode boundary and vice versa. A side effect of this behavior is a possible reduction in system efficiency under high-line and low-load conditions.

Therefore, the difference between the measured and true average current values under different line-load conditions needs a compensating factor to be subtracted from the measured current. This factor varies in an inverse-sine fashion with the input line voltage.

Around the zero crossing of the input line voltage, the discrepancy between the measured and true average current is the largest, while it is minimum or zero at the peak of the line voltage. This compensation factor is given as:

$$CA = (P_{MAX} - P_{Curr}) * S.F. * \frac{(Vac_{rms} - Vac_{minrated})}{Vac_{ratedrange}}$$

where CA is the compensation amplitude, P_{MAX} is the maximum power rating for the PFC stage, P_{Curr} is the current operating power level, $S.F.$ is the scale factor dependent on line conditions, Vac_{rms} is the input AC RMS value, $Vac_{minrated}$ is the minimum AC RMS value for which the stage is rated, and $Vac_{ratedrange}$ is the AC range for which the stage is rated.

This compensation factor is a slow varying parameter and can be updated in a slow running background task.

PFC and motor control software design and integration

We've already discussed the advantages of implementing both PFC and motor control on a single controller. A typical active PFC stage is switched at 100 kHz and the motor-control stage is switched at 10 kHz. To meet fast response requirements in case of transients, the duty cycle for both the PFC and motor control needs to be calculated every switching cycle or alternate switching cycle.

The duty cycle for the PFC and motor-control stage is estimated by running the motor-control algorithm and the PFC algorithm. Guaranteeing execution for these algorithms on a cycle-by-cycle basis poses a set of challenges, however. As these algorithms/control loops need to run at different frequencies, a simple solution to this problem is to have two interrupts configured for each control loop.

This approach has its drawbacks, as there can be multiple instances when interrupt service routines (ISRs) occur simultaneously. In these cases, even though the controller can prioritize between the ISRs, in certain situations the slower control loop (the 10-kHz motor control) can conflict with the faster control loop such that it shadows its calculation for one or more cycles.

This incident and its impact on system performance can be negligible or significant, depending on the relationship between the frequency of the loops being executed. Additionally, having two different ISRs doubles the context-save penalty. Therefore, a software architecture using a single ISR was chosen to implement both the control loops on the same controller. This ISR was triggered at the rate of the faster control loop (50-kHz PFC), with the complete PFC control loop executed at each trigger along with a time-slice (TS) engine. The motor control algorithm for the two motors was split into five parts and the TS engine executed one part on each ISR call, thus completing the motor algorithm on the fifth ISR trigger.

PWM generation

The PWMs are configured to operate in an up/down count mode to generate complementary waveforms and to correctly trigger the ADC. Figure 3 illustrates the PWM generation. The PWMs are synched at every inverter PWM cycle, ensuring that the calculations are finished and duty cycles updated before the TS engine starts again to guarantee cycle-by-cycle control on the motor control stage.
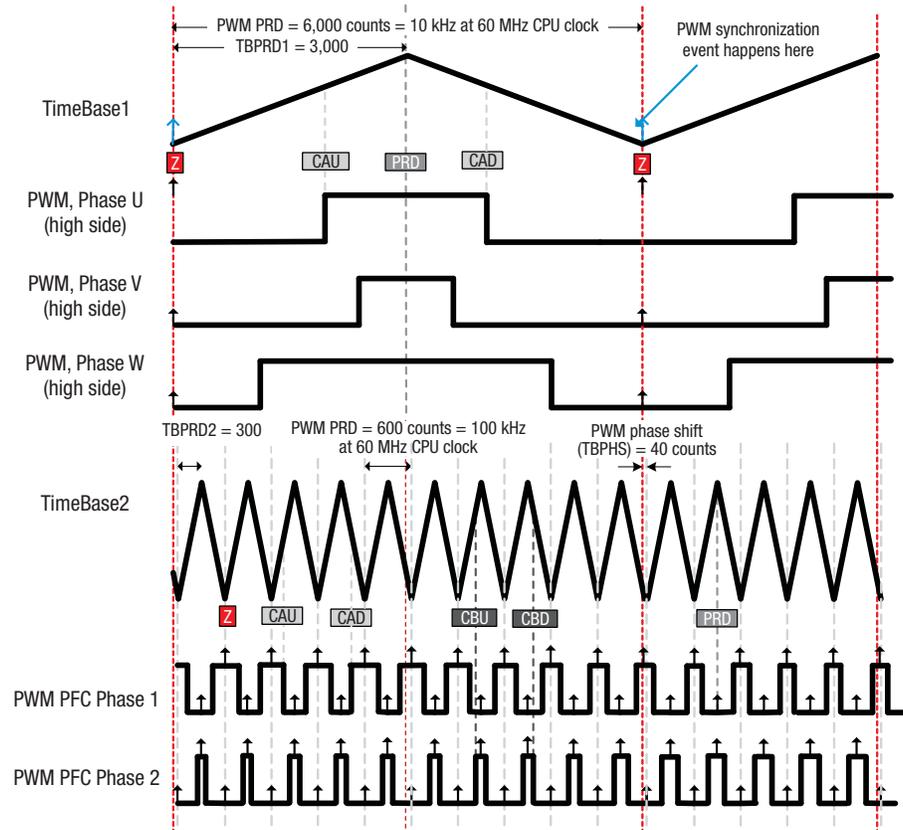

Figure 3. PWM configuration and timing.

ADC sampling

The integrity of ADC signals is of high importance, since this is where signals from the analog and digital domains interface. The ADC results are used as inputs to the control algorithm, which then provides the duty value to be driven on the PWM signals. Switching the PFC stage and the inverter can result in noise or disturbance on the signals to be sensed around this point in time.

Even with all the filtering on these signals to avoid noise at the ADC inputs, it is prudent to sample the inputs at a time such that this disturbance is avoided. Thus, the signals for the PFC stage and three-phase motor control inverters are sampled at the midpoint of the PWM signal – as far away from the MOSFET switching as possible – to avoid having any switching noise reflected on the ADC result (Figure 4). The flexibility of ADC and PWM modules is essential to enable such precise and flexible triggering of ADC conversions.
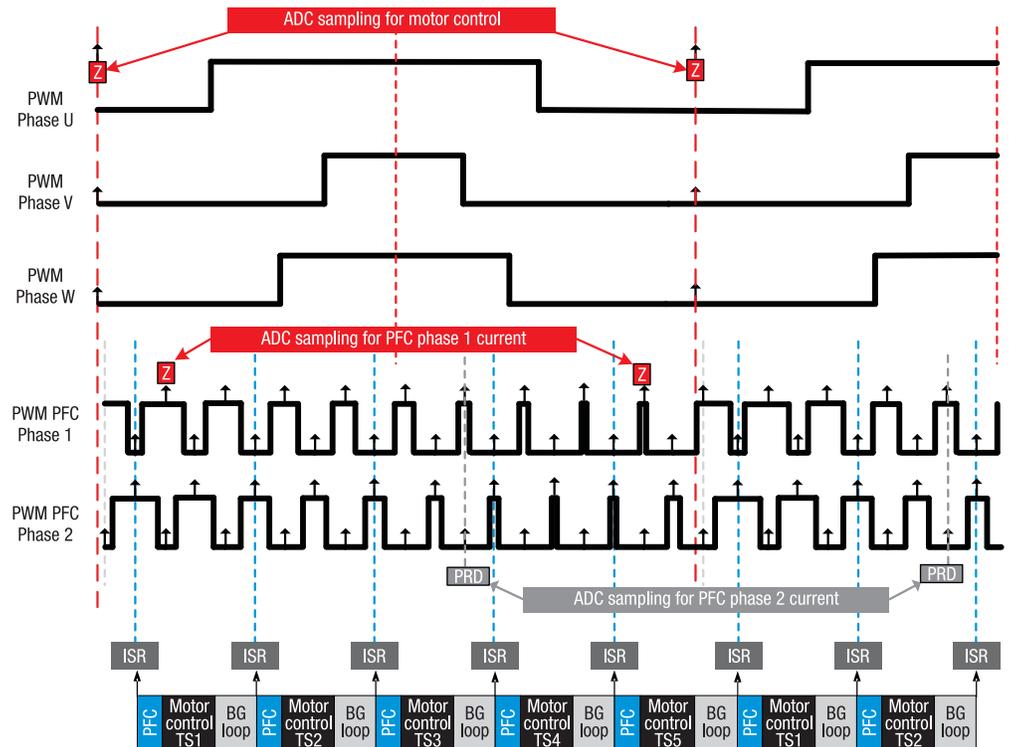

Figure 4. ADC sampling.

Software partitioning

Figure 5 on the following page shows the system timing and how it relates to code execution. As ISR is triggered once the ADC finishes sampling the leg currents for the PFC stage. Because it runs at the highest frequency in the system (50 kHz), the PFC portion is executed first in the ISR. A part of the motor-control code is then executed according to which TS window is also currently being executed, as shown in Figure 5.

The ISR code is executed every 20 µs; that is, at a rate of 50 kHz. However, the ISR code (PFC plus TS code) doesn't take this long to execute and runs for only a part of the 20-µs time interval. The slower background loop is executed in the remaining interval time. This is also where slower system tasks like instrumentation, soft start/shutdown and communications are executed. The motor control algorithm is run in C, whereas the PFC control is run entirely using assembly code.

Motor control

Both of the motors are controlled using the FOC technique to achieve high enough performance, as shown in Figure 6 on page 8. Two phase currents are sensed through ADCs for the FOC loop, while DC bus voltage is
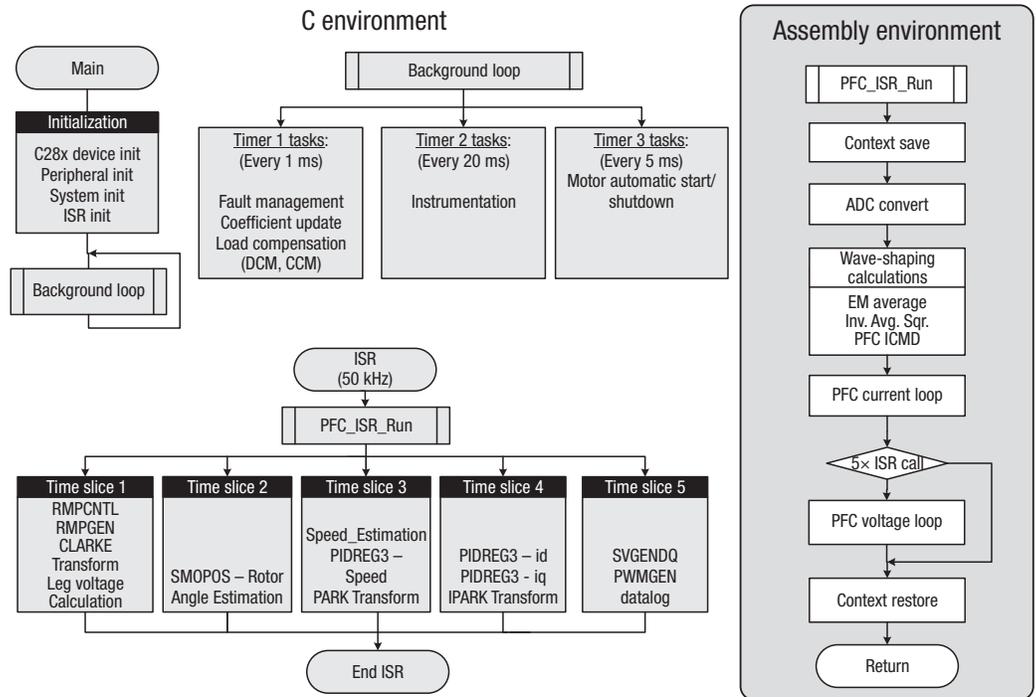
Figure 5. System timing.

sensed for position estimation. This DC bus voltage is necessary to calculate the three phase voltages when the switching functions are known. The position feedback is obtained through a sliding-mode observer to eliminate the incremental encoders and reduce the cost. The PMSM model can be written as:

$$\frac{di_s}{dt} = Ai_s + B\,(v_s - e_s) \quad \text{where } A = -\frac{R}{L}\,I_2,\ B = \frac{1}{L}\,I_2, \text{ with } L = \frac{3}{2}\,L_m,$$

where I_2 is the 2-by-2 identity matrix, R is the stator resistance and L_m is the magnetizing inductance.

The sliding-mode current observer consists of a model-based current observer and a bang-bang control generator driven by the error between estimated motor currents and actual motor currents. The mathematical equations for the observer and control generator are given as:

$$\frac{d}{dt}\,\widetilde{i_s} = A\widetilde{i_s} + B\,(v_s - \widetilde{e_s} + z) \quad z = k\,sign(\widetilde{i_s} - i_s).$$

The goal of bang-bang control z is to drive the current estimation error rate to zero. It is achieved by the proper selection of k and the correct formation of estimated back electromotive force (EMF), e_s. Note that the symbol ~ indicates that a variable is estimated.

Estimated back EMF is obtained by filtering bang-bang control z, with a first-order low-pass filter described as:

$$\frac{d}{dt}\,\widetilde{e} = -w_0\widetilde{e} + w_0 z\,.$$

The estimated rotor flux angle is obtained as:

$$e_s = \frac{3}{2}\,k_e w \begin{pmatrix} -\sin\theta \\ \cos\dot{\theta} \end{pmatrix}$$

Therefore, given the estimated back EMF, the estimated rotor position can be calculated as:

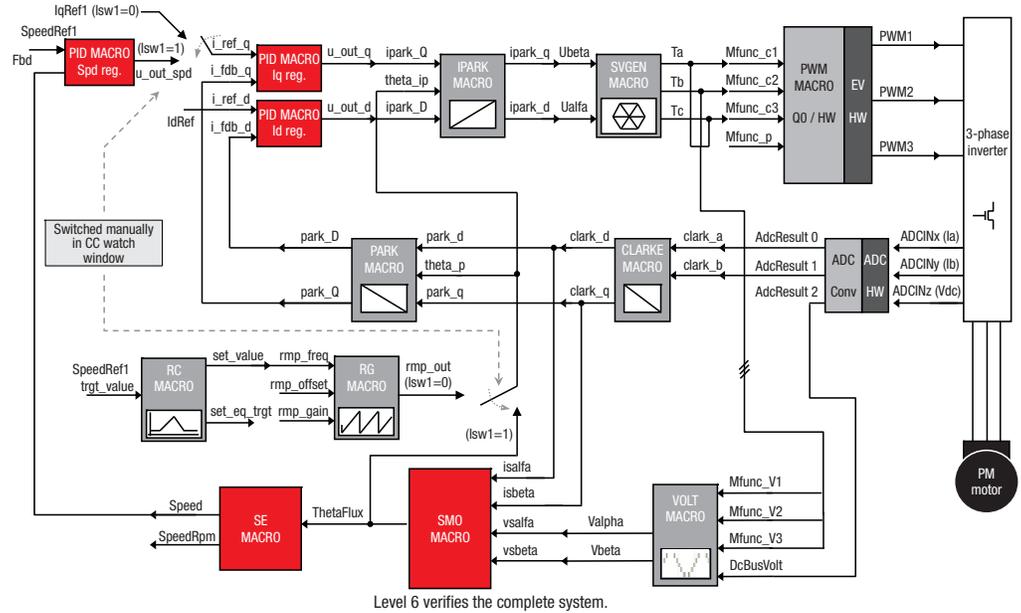$$\theta_{eu} = \ \arctan(-e_{s\alpha}, e_{s\beta}).$$

Figure 6. Control block diagram of each motor.

To minimize the number of cycles, digital motor control library modules like proportional integral derivative (PID), park, clarke, space-vector generator and sliding mode are optimized and converted to C macros. Optimization (turning the function into a macro expansion) is sometimes possible. This allows the compiler to optimize further under certain circumstances, producing less code and consuming fewer cycles to execute. Table 1 lists the computational details of the modules and total CPU utilization for a 10-kHz motor control loop update:

Table 1. CPU utilization of sensorless FOC of permanent magnet motor

Name of modules	Number of cycles
Ramp controller	29
Clarke transform	28
Park transform	142
I_Park transform	41
Sliding-mode observer	263
Speed estimator	72
Phase volt calc.	115
$3 \times$ PID	167
Space vector generator	137
PWM driver	74
Contxt save, etc.	53
Total number of cycles	**1121**
CPU utilization at 60 MHz	**18.7%**

Because this application includes two motor FOC, and a separate PFC unit running at high switching frequency, the size of the code and the number of cycles for each stage becomes very critical in order not to violate CPU utilization. The code optimization analysis in Table 2 shows the system-level CPU utilization for control-loop updates at 10 kHz and 50 kHz for motor control and PFC control, respectively. Table 2 shows that there is more than enough bandwidth for tasks like system monitoring, protection and signal conditioning.

Table 2. System-level utilization @ 60-MHz CPU

PMSM-I	18.7%
PMSM-II	18.7%
2Ph_Int_PFC	21.6%
Total	**59.0%**

Experimental results

The experimental results of PMSM control and PFC control are given in Figure 7. In Figures 7a and 7b, estimated theta by SMO and phase A currents are shown under a 0.5-pu load. In Figures 7c and 7d, the Id and Iq components in the synchronous frame are shown under 0.5-pu step load at 0.25-pu speed.

Figure 8 shows the input voltage and currents when the PFC stage is running under medium load conditions.
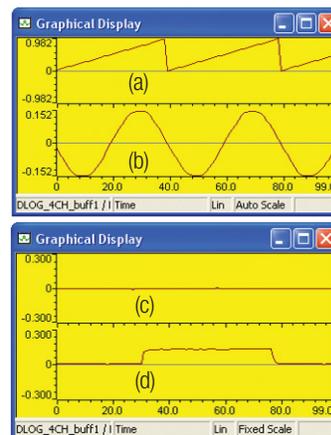

Figure 7. (a) Estimated theta by sliding-mode observer; (b) Phase A current; (c) Id; and (d) Iq components of the stator current in the synchronous frame under a 0.5-pu step load at a 0.25-pu speed.
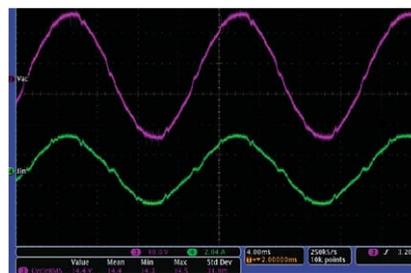

Figure 8. Input voltage and input current clearly illustrating PFC action under medium load.

Conclusion

TI's motor control and PFC developer's kit, as well as the dual-motor control and PFC developer's kit, are based on Piccolo™ MCUs to give developers a platform that accelerates development and troubleshooting of motor-control systems. The intuitive kits even teach developers unfamiliar with PFC how to merge PFC with motor-control applications of all types.

The motor control and PFC kits (**www.ti.com/c2000hwtools**) provide direct access to all of the enhancements and features of the Piccolo MCU architecture. Thorough documentation and controlSUITE™ software libraries (**www.ti.com/controlsuite**) lead developers through the process of creating a complete motor-control system using real-time algorithms. The kit also enables developers to quickly determine the processing resources required to implement basic motor control. From this baseline, they are then able to bring in advanced algorithms to trade-off the remaining processing capacity for greater accuracy, better performance, higher power efficiency, control of multiple motors and a myriad of other options. In this way, developers can architect systems specifically optimized for their application constraints and requirements.

TMS320C2000™ Piccolo MCUs are available across a wide roadmap of configurations to ensure that developers can find a processor optimized in terms of performance, memory and peripherals for their application. TI also supplies all of the analog components necessary for voltage and current sensing, as well as a wide range of standard and advanced motor drivers.

TI understands the challenges developers face when designing cost-effective and power-efficient motor-control applications. With the Piccolo series of MCUs, TI has brought together an unparalleled combination of high performance and integrated peripherals, enabling developers to implement dual-motor control – using a single processor – with enough headroom for precision-control algorithms, advanced power efficiency and sensorless feedback, all while reducing system cost.

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