EVM User's Guide: TAS67CD-AEC

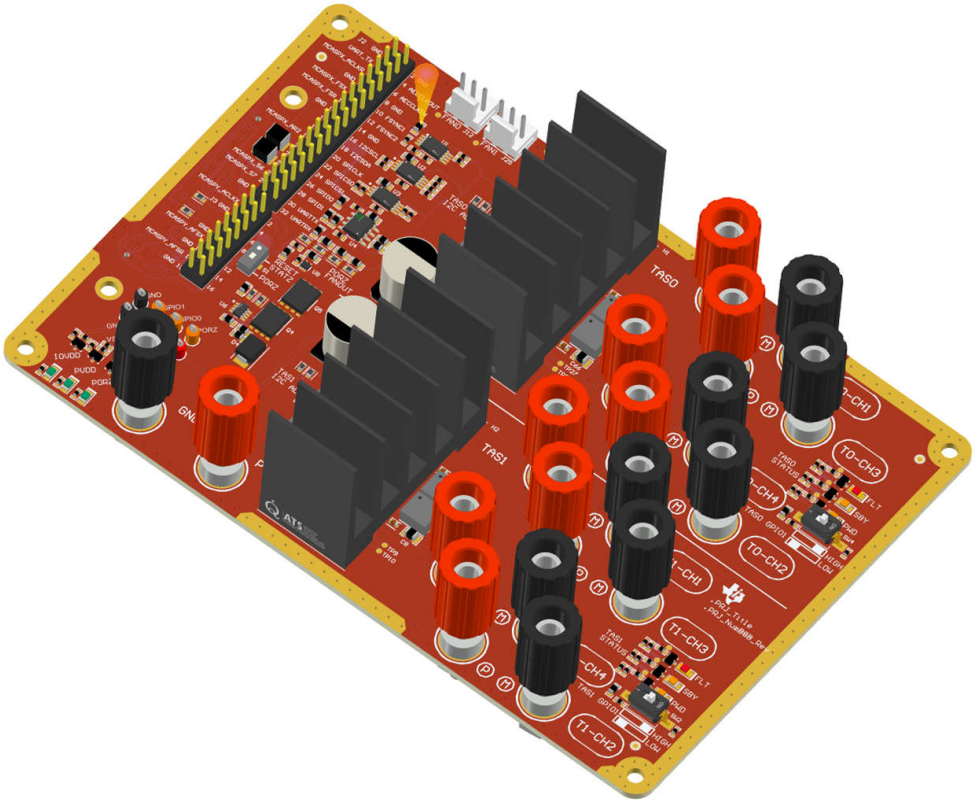
TAS67CD-AEC User's Guide

Description

The TAS67CD-AEC add-on card implements two, 4-channel TAS67x Class-D audio amplifier ICs and is compatible with TI Audio DSP EVMs through the AEC form-factor connector. Each add-on card provides up to 8 channels of 50W amplified digital audio output.

Features

- 2x TAS6754-Q1, Automotive Rated, 4-Channel Class-D Amplifiers
- Up to 50 Watt output per channel, up to 8 channels, to 4mm banana plug output
- TI DSP Audio Expansion Card (AEC) Form-Factor. Compatible with:
  - AUDIO-AM275-EVM
  - AUDIO-AM62D-EVM
- Amplifier PVDD power input 4.25V to 18.5V through banana plugs
  - Reverse polarity and over-voltage protection for amplifier power



1 Evaluation Module Overview

1.1 Introduction

The TAS67CD-AEC add-on card was developed to enable prototyping of multi-channel digital audio systems based on the TAS6754-Q1 4-channel Class-D amplifier and TI AM275x and AM62Dx families of processors. The TAS67CD-AEC implements the TI Audio Expansion Connector (AEC) interface available on audio baseboard EVM such as the AUDIO-AM275-EVM and AUDIO-AM62D-EVM.

With audio baseboard EVM providing two AEC interfaces, this enables creating 16-channel amplified audio systems. Combined with the audio baseboard EVM's onboard audio ADC, DAC and networking resources, the combined audio EVM system can be used to prototype a range of networked audio systems typical of automotive, in-vehicle, installations and industry standard surround sound topologies.

This user's guide describes how to properly use the add-on card with the audio baseboard EVM. This user's guide also details many important aspects of the add-on board including but not limited to power tree description, signal pathways, pin header descriptions, test points, and selectable switch settings.

Please see the TAS67CD-AEC tools page for schematics, bill of materials and PCB design files for this add-on card.

1.1.1 Important Usage Notes

Note

This is the first revision of this User's Guide. For any questions or points of clarity, refer to E2E®.

Note

An external power supply is required for operation of this add-on board. Requirements for J13/J15 PVDD input power:

- Nominal output voltage: 4.5-18.5 VDC
- Peak current: 11 Amps

Note

The TAS67CD-AEC J13/J15 PVDD banana plug receptacles can sink a peak of 11 Amps.

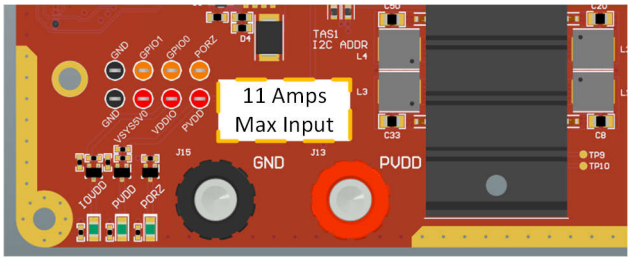


Figure 1-1. TAS67CD-AEC - High Current Warning

Note

Multiple indicator LED are located on the TAS67CD-AEC to quickly inform the user of normal or faulty operating states. See Indicator LED for full description of the different indicator LED states.

Note

The AM275 and AM62 Version 11.0 SDKs are designed for a previous revision of the TAS67CD-AEC (Revision E1) and require adding a GPIO write for each TAS67 device's STBY pin to wake the device out of standby mode.

Note

TI recommends using an external power supply or accessory which complies with applicable regional safety standards such as (by example) UL, CSA, VDE, CCC, PSE.

1.2 Kit Contents

- TAS67CD-AEC PCB assembly
- Mounting screws, nuts and washers for attaching the TAS67CD-AEC to either the AUDIO-AM275-EVM or AUDIO-AM62D-EVM for desktop usage convenience

1.3 Specification

The TAS67CD-AEC EVM is intended to expand on compatible TI Audio DSP EVMs. The Audio Expansion Connector (AEC) enables up to eight channels of 50W amplified digital audio output using two TAS6754-Q1 devices. The Audio DSP EVM uses I2C through the AEC to manage the TAS67 devices. Digital audio data is sent to the TAS67 devices using the MCASP peripheral of the SOC on the Audio DSP EVM.

An external power supply is needed to power the TAS67 devices and the PVDD and VBAT power rails. The allowed input range for PVDD and VBAT is 4.25V to 18.5V, with a maximum current draw of 11A.

Figure 2-1 shows the complete block diagram for the TAS67CD-AEC.

1.4 Device Information

TAS6754-Q1

TAS6754-Q1 is a four-channel digital-input Class-D audio amplifier that implements 1L modulation only requiring one inductor per BTL channel reducing system size and cost by removing four inductors compared to a traditional design. Additionally, 1L modulation lowers switching losses compared to traditional Class-D modulation schemes.

More information about the TAS6754-Q1 can be found on the TAS6754-Q device product page.

2 Hardware

2.1 System Components

The highlight of the TAS67CD-AEC is the two TAS6754-Q1 (TAS67x), 4-channel, Class-D audio amplifier devices (U5, U7) and the supporting components for these devices. The AEC connector (J1) provides I/O power (IOVDD), resets, I2C control, and MCASP TDM data stream from an attached host processor. A low-current, 5V accessory power rail (VSYS5V) is also provided from the AEC for LED and heatsink fans.

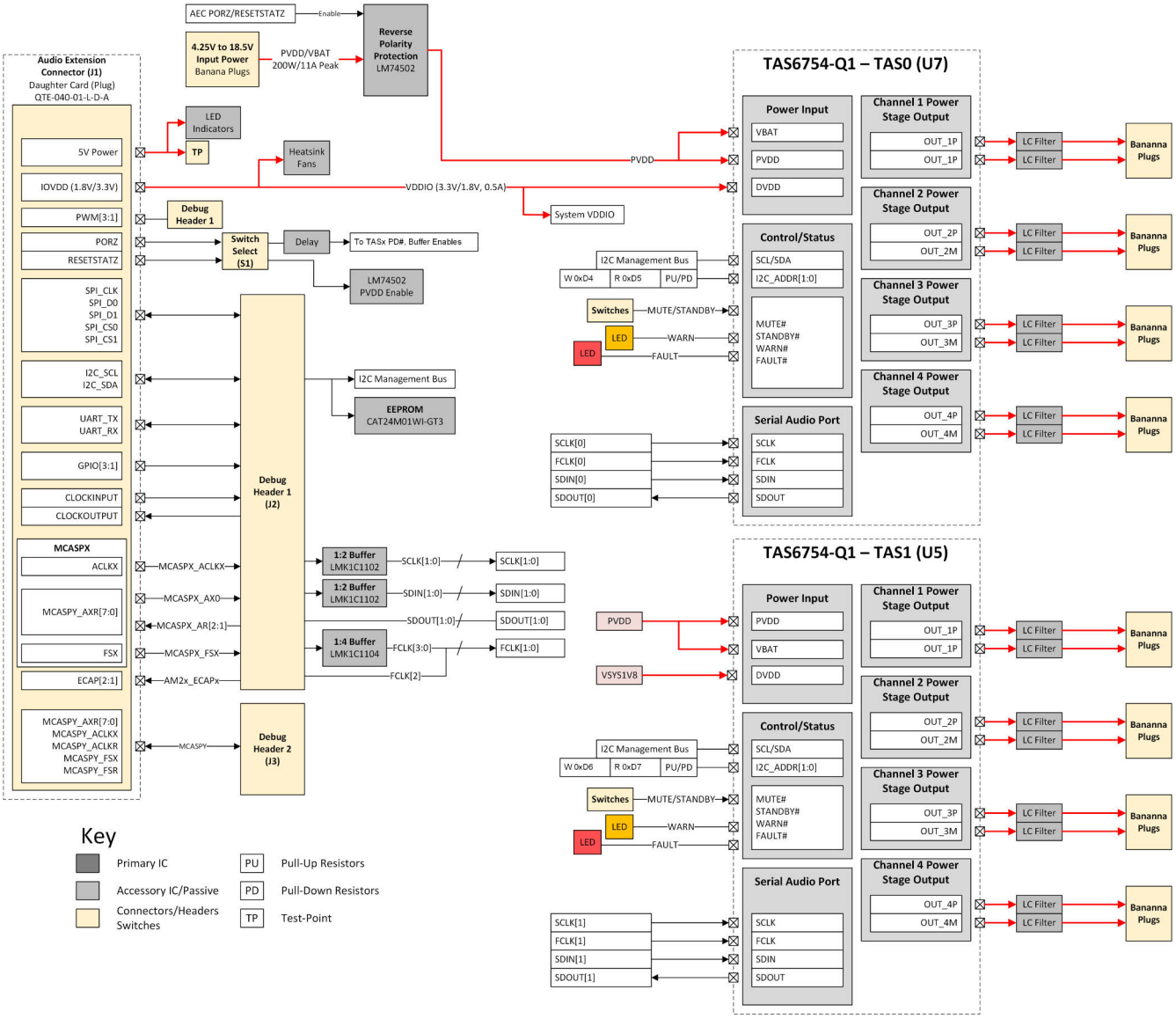


Figure 2-1. TAS67CD-AEC System Block Diagram

TAS67x high-current amplifier power (PVDD) and accessory battery power (VBAT) are provided through a set of banana plugs which feed into an LM74502 reverse-polarity, over-voltage, and over-current protection circuit.

MCASP TDM audio data is provided from the MCASPX port of the AEC connector. The MCASP TDM signals are buffered through a set of LMK1C1102 1:2 buffers with each output going to one of the TAS67x amplifiers. MCASP Frame Sync (FSYNC) is buffered through an LMK1C1104 1:4 buffer, with two of the outputs routed to the onboard TAS67x amplifiers and two outputs routed back to the AEC to provide frame-sync synchronization feedback for the host processor through the AEC ECAP pins.

A manual switch (SW1) is provided for selecting between PORZ and RESETSTATZ AEC reset paths. Each TAS67x also has switches (SW2, SW4) for toggling the GPIO0/MUTE# optional input to the TAS67x devices.

Breakout/debug headers (J2, J3) provide an easy to probe location for all of the AEC signals used on the design and most of the unused AEC signals as well.

2.1.1 System Components Top

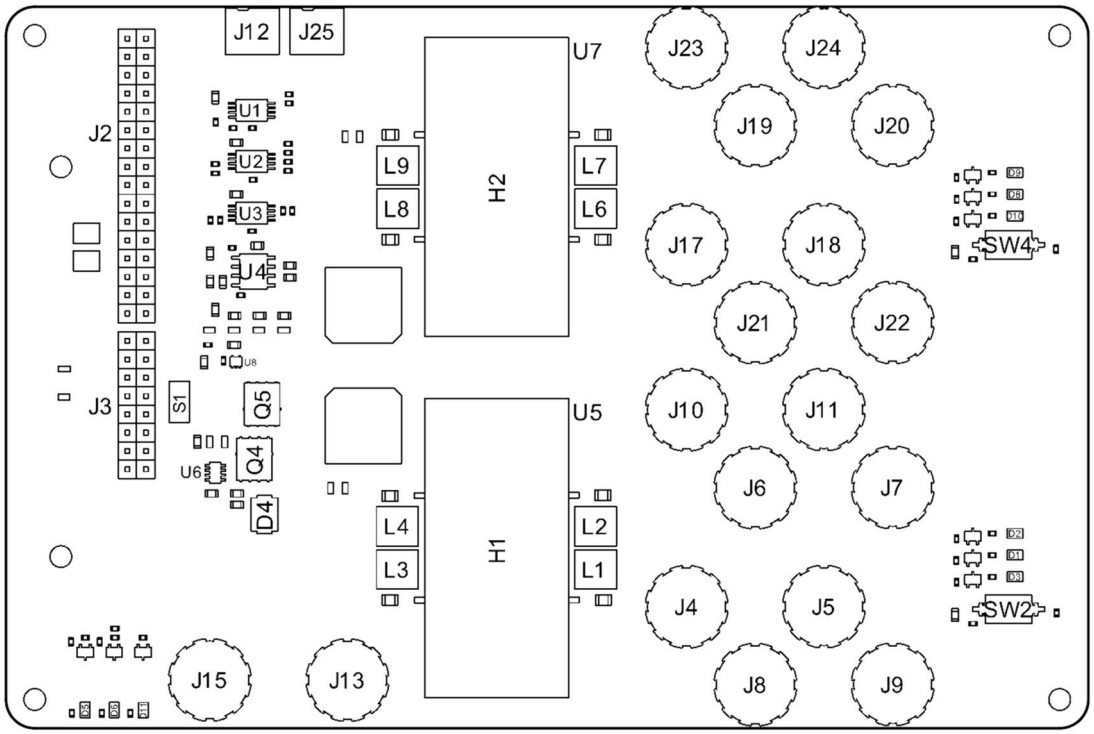


Figure 2-2. System Components Top

Table 2-1. System Components Top

Reference Designator	Description	Reference Designator	Description
U7, H2	TAS67x Device 0 IC and Heatsink	J2, J3	AEC Breakout Headers
U5, H1	TAS67x Device 1 IC and Heatsink	S1	PORZ/RESETSTATZ AEC Select
U1, U2, U3, U4	LMK1C1102/04 MCASP TDM buffers	S4	TAS0 GPIO0/MUTE# Select
J13, J15	PVDD Input Power/Ground Banana Plug Receptacles	S2	TAS1 GPIO0/MUTE# Select
J17, J18, J19, J20, J21, J22, J23, J24	TAS67x Device 0 (TAS0) Output Audio Banana Plug Receptacles	U6, D4,Q4, Q5	LM74502 Input Power Protection
J4, J5, J6, J7, J8, J9, J10, J10, J11	TAS67x Device 1 (TAS1) Output Audio Banana Plug Receptacles	J12, J25	Optional Heatsink Fan Power
L1, L2, L3, L4	TAS1 Output Inductors	L6, L7, L8, L9	TAS0 Output Inductors

2.1.2 System Components Bottom

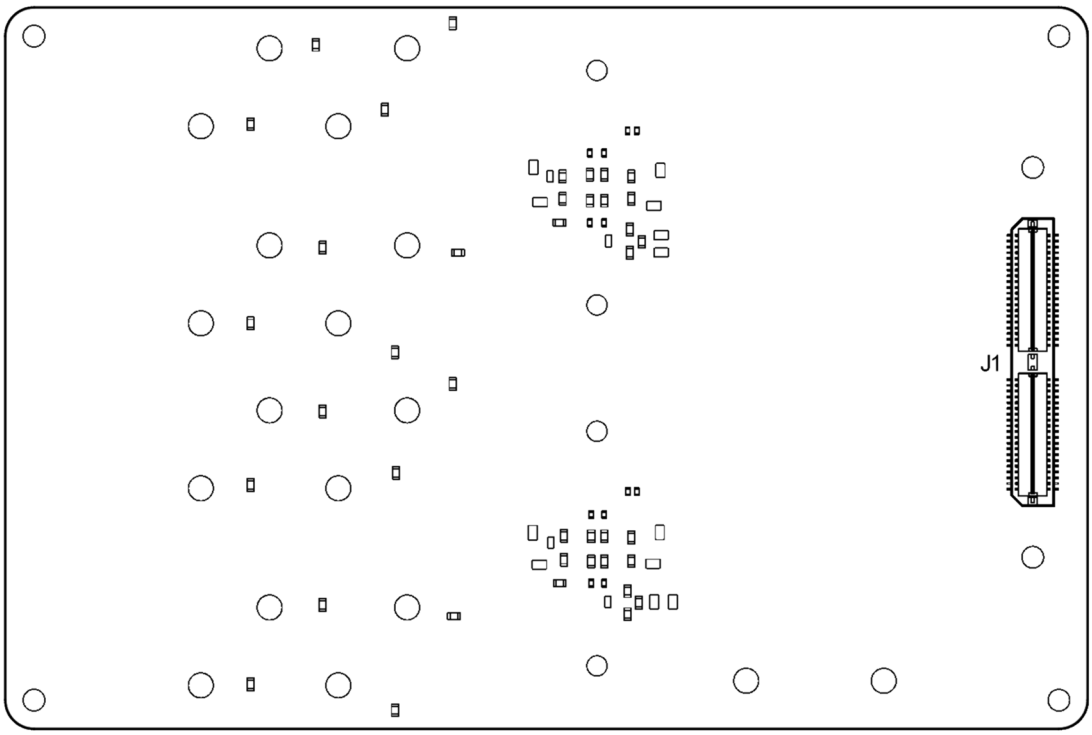


Figure 2-3. Components Bottom

Table 2-2. System Components Bottom

Reference Designator	Description	Reference Designator	Description
J1	Audio Expansion Card (AEC) Connector		

2.2 Power Requirements

The TAS67CD-AEC requires multiple power inputs for operation. The TAS67CD-AEC power tree is shown in the below block diagram. IOVDD and VSYS5V0 are provided through the AEC connector from the host processor board. PVDD is provided through a set of banana plug receptacles and requires an external compatible DC supply be attached to the board.

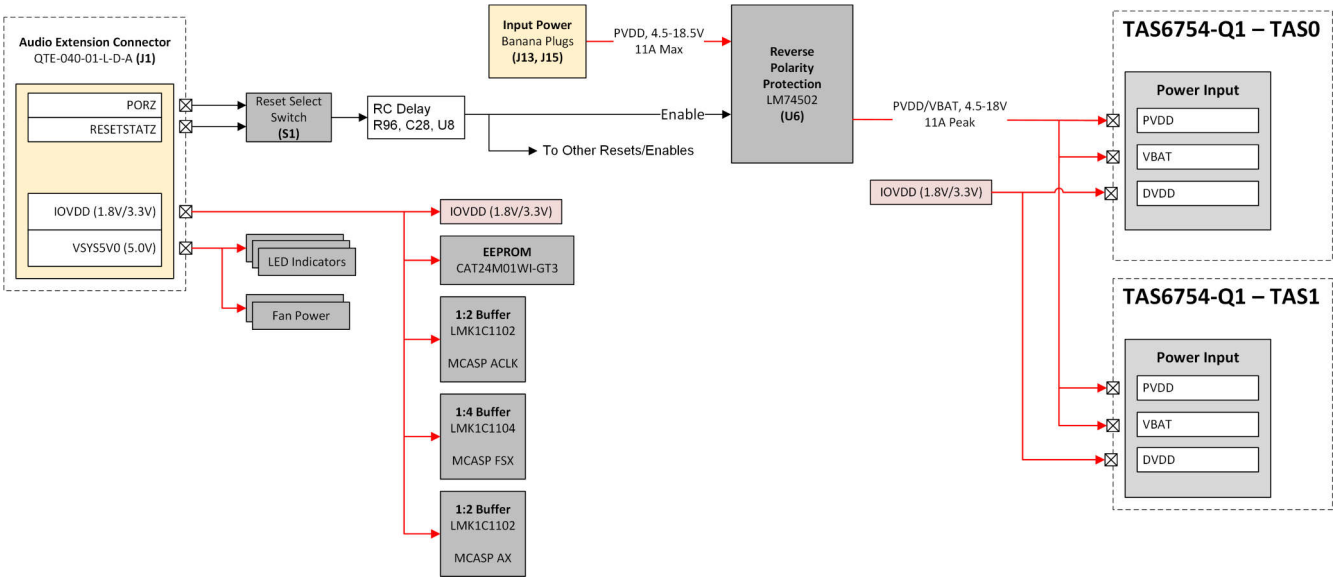


Figure 2-4. TAS67CD-AEC Power Tree

The requirements for all of these power inputs are described in the table below. The IOVDD and VSYS5V0 requirements are compatible with the AM275-AUDIO-EVM and AM62D-AUDIO-EVM AEC interface implementations.

Table 2-3. Power Requirements

Power Rail	Connector Location	Description	Min	Max	Units
PVDD/VBAT	Banana Plug Receptacles • J13 - PVDD/ VBAT • J15 - GND	TAS67x Amplifier Power (PVDD) and battery power(VBAT)	4.5	18.5	Volts
				11	Amps
IOVDD	AEC Connector J1.10, J1.12	Digital I/O Power	1.71	3.465	Volts
				TBD	Amps
VSYS5V0	AEC Connector J1.2, J1.4, J1.6	5.0V LED and Fan Power	4.75	5.25	Volts
				TBD	Amps

2.3 Setup

Typical audio baseboard EVM and TAS67CD-AEC system setup is described below. The TAS67CD-AEC add-on card requires a compatible host processor baseboard that includes the TI audio expansion connector (AEC) interface.

Note

As of the publication of this document the TAS67CD-AEC has only been tested with the AM275-AUDIO-EVM and the AM62D-AUDIO-EVM. Other audio baseboards implementing compatible AEC interface signals don't work in a similar manner.

Setup Steps

- The baseboard and add-on card system is assembled by attaching the TAS6CD-AEC AEC connector (J1, bottom of the board) with the baseboard EVM AEC1 and/or AEC2 (J13, J12) located on the top of the baseboard EVM.

  - Additional mounting screws can be attached to the TAS67CD-AEC and audio baseboard to provide a level mounting when using the system on a bench top environment.
- Switch S1 can be setup for RESETSTATZ or PORZ usage depending on attached baseboard EVM reset output options.
  - See Reset Select Switch for SW1 setup information.
- TAS0/TAS1 audio output banana jack binding posts can be attached to compatible speakers.
  - See External Speaker Setup and Requirements below for speaker requirements.
  - See TAS67x Audio Output for description of all audio outputs.
- J13/J15 banana jack binding posts for PVDD/VBAT can be powered from DC source supply. PVDD supply can be powered before the baseboard EVM is powered. Power is gated based on reset signal from attached host board.
- The audio baseboard EVM can now be powered and TAS67CD-AEC compatible application run.

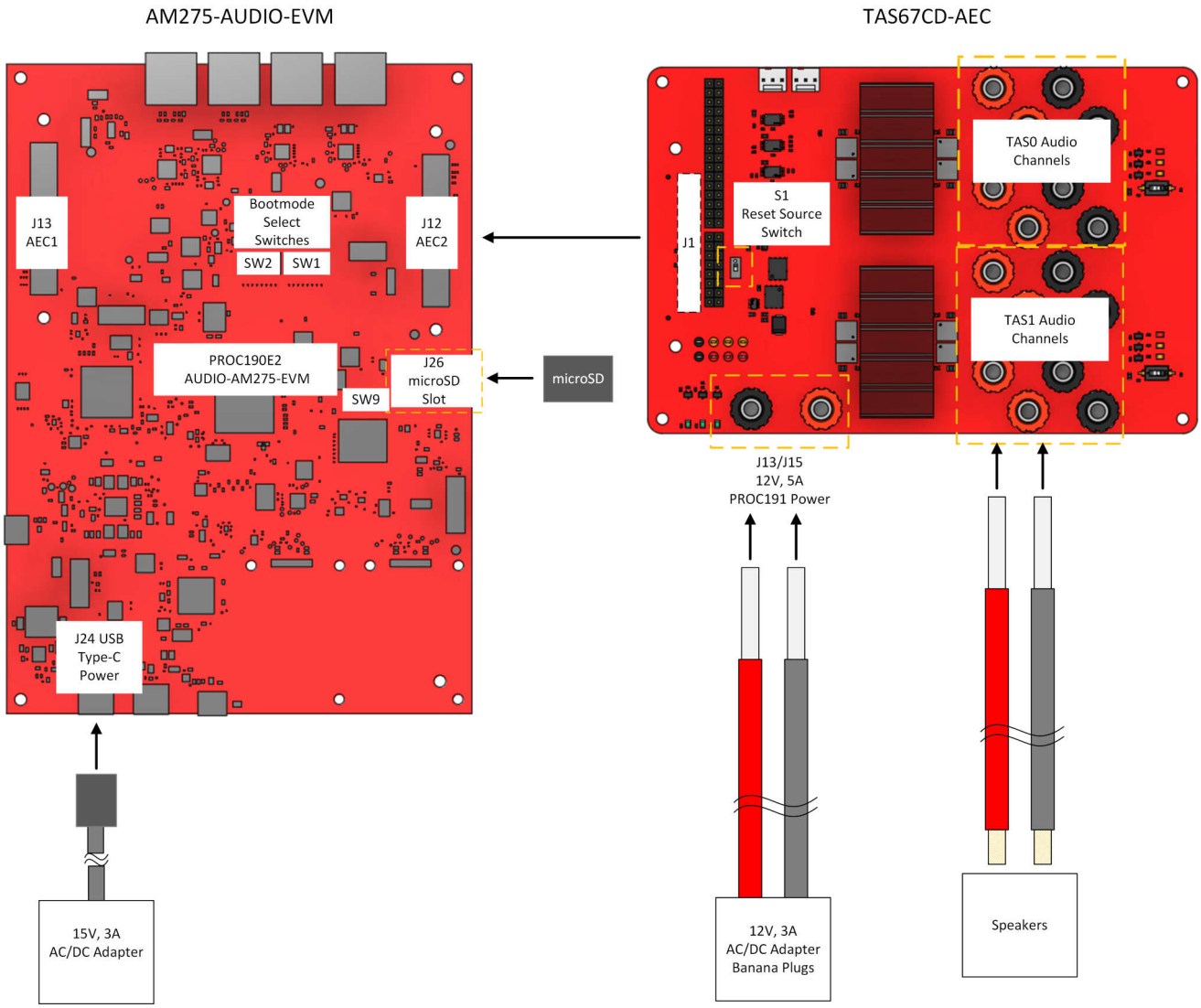


Figure 2-5. AM275-AUDIO-EVM and TAS67CD-AEC Setup

External Speaker Setup and Requirements

The TAS67x amplifiers are designed to work with externally attached speakers with load between 2-ohm minimum and 4-ohm typical. This range is typical of many available speaker systems.

The 4-ohm typical loading aligns with the characterized audio and power efficiency performance quoted in the TAS6754-Q1 data sheet. See TAS6754-Q1 Datasheet for full description of TAS67x output loading requirements.

2.4 Header Information

The TAS67CD-AEC includes two primary data headers. These are the AEC J1 header on the bottom side of the board and the AEC breakout/debug headers J2 and J3 on the top of the board. These headers are described in the tables below.

The AEC J1 header on this add-on board is implemented with a Samtec QTE-040-01-L-D-A. The mating baseboard connector is a Samtec QSE-040-01-L-D-A. Not all signals available on the full super-set of the AEC interface are implemented on this add-on board.

2.4.1 Connector Pinout

Table 2-4 includes the full pinout for the AEC connector with the pin numbers, baseboard EVM I/O direction, and TAS67CD-AEC schematic net name.

Direction of signals are relative to baseboard EVM.

- I - used as input to baseboard EVM
- O - used as output from baseboard EVM
- IO - used as either input/output baseboard EVM
- PWR - power
- GND - ground return
- X - unused on this design

Table 2-4. AEC Header (J1) Description

AEC Net Name	Type	J1 Pin Number		Type	AEC Net Name
PORZ_AEC	O	1	2	PWR	VSYS5V0
	X	3	4	PWR	VSYS5V0
	X	5	6	PWR	VSYS5V0
GND	GND	7	8	GND	GND
ECAP_FRAMESYNC1	I	9	10	PWR	VDDIO
ECAP_FRAMESYNC2	I	11	12	PWR	VDDIO
	X	13	14	X	
GND	GND	15	16	GND	GND
SPI_CLK	O	17	18	O	I2C_SCL
SPI_D0	O	19	20	IO	I2C_SDA
SPI_D1	I	21	22	GND	GND
SPI_CS0	O	23	24	O	SPI_CS1
GND	GND	25	26	GND	GND
MCASPX_AX0	O	27	28	I	MCASPX_AR2
MCASPX_AX1	O	29	30	I	MCASPX_AR3
GND	GND	31	32	IO	MCASPX_SERIAL4
AECCLKIN	I	33	34	IO	MCASPX_SERIAL5
GND	GND	35	36	GND	GND
MCASPX_ACLKX	O	37	38	IO	MCASPX_SERIAL6
MCASPX_FSX	O	39	40	IO	MCASPX_SERIAL7
MCASPX_FSR	I	41	42	O	GPIO0
MCASPX_ACLKR	I	43	44	O	GPIO1
GND	GND	45	46	GND	GND
AECCLKOUT	O	47	48	X	
GND	GND	49	50	GND	GND
	X	51	52	X	
	X	53	54	X	

Table 2-4. AEC Header (J1) Description (continued)

AEC Net Name	Type	J1 Pin Number		Type	AEC Net Name
RESETSTATZ_AEC	O	55	56	X	
GND	GND	57	58	GND	GND
	X	59	60	X	
	X	61	62	O	UART_TX
	X	63	64	I	UART_RX
GND	GND	65	66	GND	GND
MCASPY_SERIAL0	IO	67	68	IO	MCASPY_SERIAL4
MCASPY_SERIAL1	IO	69	70	IO	MCASPY_SERIAL5
MCASPY_SERIAL2	IO	71	72	IO	MCASPY_SERIAL6
MCASPY_SERIAL3	IO	73	74	IO	MCASPY_SERIAL7
GND	GND	75	76	GND	GND
MCASPY_ACLKX	O	77	78	I	MCASPY_ACLKR
MCASPY_AFSX	O	79	80	I	MCASPY_AFSR

2.4.2 Debug Connector Pinouts

The below tables Table 2-5 and Table 2-6 describe the two AEC breakout/debug headers. These headers provide a convenient location to probe all of the AEC signals used on this design and most of the unused AEC signals as well.

Direction of signals are relative to baseboard EVM.

- I - used as input to baseboard EVM
- O - used as output from baseboard EVM
- IO - used as either input/output baseboard EVM
- PWR - power
- GND - ground return
- X - unused on this design

Table 2-5. Debug Header 1(J2) Description

AEC Net Name	Type	J1 Pin Number		Type0	AEC Net Name
GND	GND	1	2	GND	GND
MCASPX_ACLKX	O	3	4	O	AECCLKOUT
MCASPX_ACLKR	I	5	6	I	AECCLKIN
GND	GND	7	8	GND	GND
MCASPX_FSX	O	9	10	I	ECAP_FRAMESYNC1
MCASPX_FSR	I	11	12	I	ECAP_FRAMESYNC2
GND	GND	13	14	GND	GND
MCASPX_AX0	O	15	16	O	I2C_SCL
MCASPX_AX1	O	17	18	IO	I2C_SDA
MCASPX_AR2	I	19	20	O	SPI_CLK
MCASPX_AR3	I	21	22	O	SPI_CS0
MCASPX_SERIAL4	IO	23	24	O	SPI_CS1
MCASPX_SERIAL5	IO	25	26	O	SPI_D0
MCASPX_SERIAL6	IO	27	28	I	SPI_D1
MCASPX_SERIAL7	IO	29	30	O	UART_TX
GND	GND	31	32	I	UART_RX

Table 2-6. Debug Header 2 (J3) Description

AEC Net Name	Type	J1 Pin Number		Type0	AEC Net Name
GND	GND	1	2	GND	GND
MCASPX_ACLKX	O	3	4	O	AECCLKOUT
MCASPX_ACLKR	I	5	6	I	AECCLKIN
GND	GND	7	8	GND	GND
MCASPX_FSX	O	9	10	I	ECAP_FRAMESYNC1
MCASPX_FSR	I	11	12	I	ECAP_FRAMESYNC2
GND	GND	13	14	GND	GND
MCASPX_AX0	O	15	16	O	I2C_SCL
MCASPX_AX1	O	17	18	IO	I2C_SDA
MCASPX_AR2	I	19	20	O	SPI_CLK
MCASPX_AR3	I	21	22	O	SPI_CS0
MCASPX_SERIAL4	IO	23	24	O	SPI_CS1
MCASPX_SERIAL5	IO	25	26	O	SPI_D0
MCASPX_SERIAL6	IO	27	28	I	SPI_D1
MCASPX_SERIAL7	IO	29	30	O	UART_TX
GND	GND	31	32	I	UART_RX

2.5 Interfaces

The below sections describe the individual signal paths in this design. See Figure 2-1 for overall signal connectivity.

I2C Configuration Interface

The AEC I2C management bus I2C interface (pins 18 and 20) is used to control and configure the TAS67x Device 0 (TAS0, U7), TAS67x Device 1 (TAS1, U5) and an onboard 4Kbit EEPROM (CAT24C04WI-GT3, U4).

Table 2-7. TAS67CD-AEC I2C Addresses

Device	7-bit Address (Omitting Read/Write# bit)	8-bit Address (Including Read/Write# bit)
TAS67x Device 0 (TAS0, U7)	0x70	Write: 0xE0
		Read: 0xE1
TAS67x Device 1 (TAS1, U5)	0x71	Write: 0xE2
		Read: 0xE3
4Kbit EEPROM (CAT24C04WI-GT3, U4).	0x54/0x55	Write: 0xA8/0xAA
		Read: 0xA9/0xAB

MCASP TDM Data Interface

A subset of the AEC MCASPX interface is used to stream TDM audio data to the TAS67x Device 0 (TAS0, U7), TAS67x Device 1 (TAS1, U5) and stream amplifier telemetry data back to the host processor.

The AEC MCASPX_AX0 signal provides a TDM bitstream and synchronous bit block to a set of LMK1C1102 (U1, U3) 1:2 buffers. These buffers direct the bitstream to both TAS0 and TAS1. Likewise the AEC MCASPX_FSX frame-sync signal feeds an LMK1C1104 (U2) 1:4 buffer, providing frame synchronization to both TAS0 and TAS1 and providing feedback framesync signals ECAP_FRAMESYNC1 and ECAP_FRAMESYNC2 for the host processor through the AEC interface.

Finally, TAS0 outputs to AEC MCASPX_AR2 and TAS1 outputs to AEC MCASPX_AR3. These RX bitstreams carry optional, realtime amplifier telemetry data back to the host processor.

TAS67x Audio Output

An array of standard 4mm, banana plug binding posts are provided for quick speaker attachment to each of the TAS67x audio outputs. These are implemented as color coded posts, with Keystone model 7006 RED for positive output and model 7007 BLACK for negative output. PCB silkscreen is also provided to help guide connections during system setup.

Figure 2-6 and Table 2-8 describe this output array.

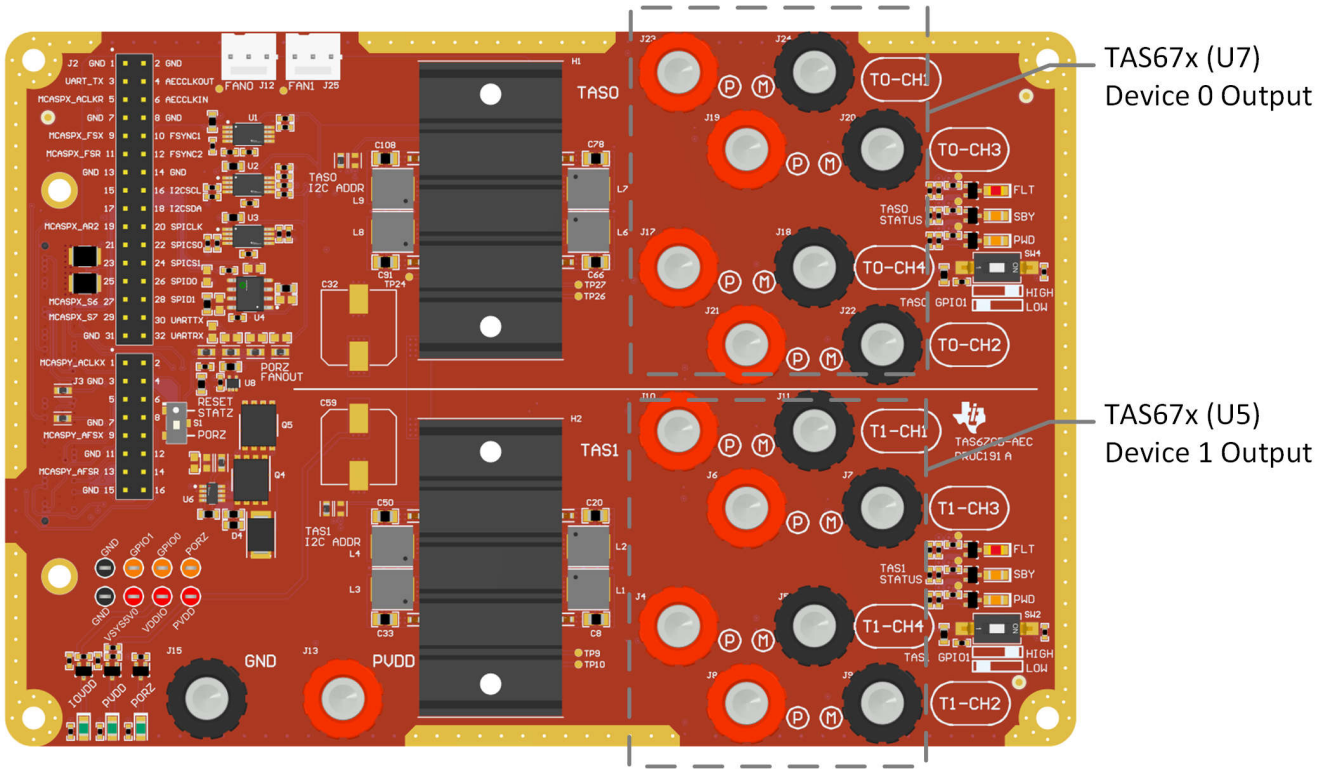


Figure 2-6. TAS67x Audio Output Banana Plug Binding Posts

Table 2-8. TAS67x Audio Output Banana Plug Binding Posts

TAS67x Device	Silkcreen Labels	Audio Output Channel	Reference Designator
TAS67x Device 0 (TAS0, U7)	T0-CH1	OUT_1P	J23
		OUT_1M	J24
	T0-CH2	OUT_2P	J21
		OUT_2M	J22
	T0-CH3	OUT_3P	J19
		OUT_3M	J20
	T0-CH4	OUT_4P	J18
		OUT_4M	J17

Table 2-8. TAS67x Audio Output Banana Plug Binding Posts (continued)

TAS67x Device	Silkcreen Labels	Audio Output Channel	Reference Designator
TAS67x Device 1 (TAS1, U5)	T1-CH1	OUT_1P	J11
		OUT_1M	J10
	T1-CH2	OUT_2P	J9
		OUT_2M	J8
	T1-CH3	OUT_3P	J7
		OUT_3M	J6
	T1-CH4	OUT_4P	J5
		OUT_4M	J4

2.6 Switch Information

There are multiple manual switches on this design to allow for static option selection.

Reset Select Switch

The reset select switch (SW1) is used to select the TAS67CD-AEC reset source from the AEC interface. This is a single pole, double throw (SPDT) switch that selects between the AEC PORZ and RESETSTATZ signals. This switch is set depending on the supported reset signal provided by the attached audio baseboard EVM.

In the orientation shown, and as shown in PCB silkscreen, the lower switch position can be selected for use with the AUDIO-AM62D-EVM using the PORZ output. Likewise, the upper position is used to select the

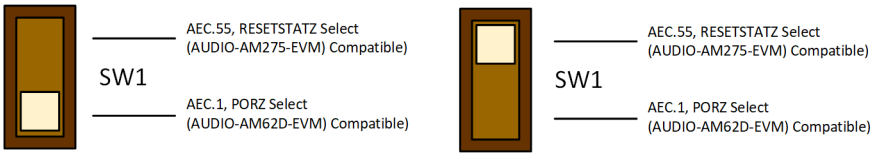


Figure 2-7. Reset Select Switch Diagram

TAS67x GPIO Select Switches

The reset select switches (SW4 and SW2) are used to toggle the TAS67x GPIO0 input high or low. This GPIO0 is a software configurable input option which can be used to select a few different modes of operation, including the MUTE mode. This is a single pole, single throw (SPST) switch that selects between the IOVDD and GND being applied to the TAS67x GPIO0 pin. By default, the switch state is ignored by the TAS67x until the GPIO0 programmable input is programmed by I2C register writes.

See the TAS6754-Q1 data sheet for more information on using the GPIO0 input.

In the orientation shown, and as described in PCB silkscreen, the left switch position sets the GPIO0 input to GND. Likewise the right switch position sets the GPIO0 to IOVDD.

With no external pulls on GPIO0 and GPIO1, STBY uses internal pull down to hold the state of these signals. TAS0 and TAS1 can not play audio until GPIO0 and GPIO1 are written high.

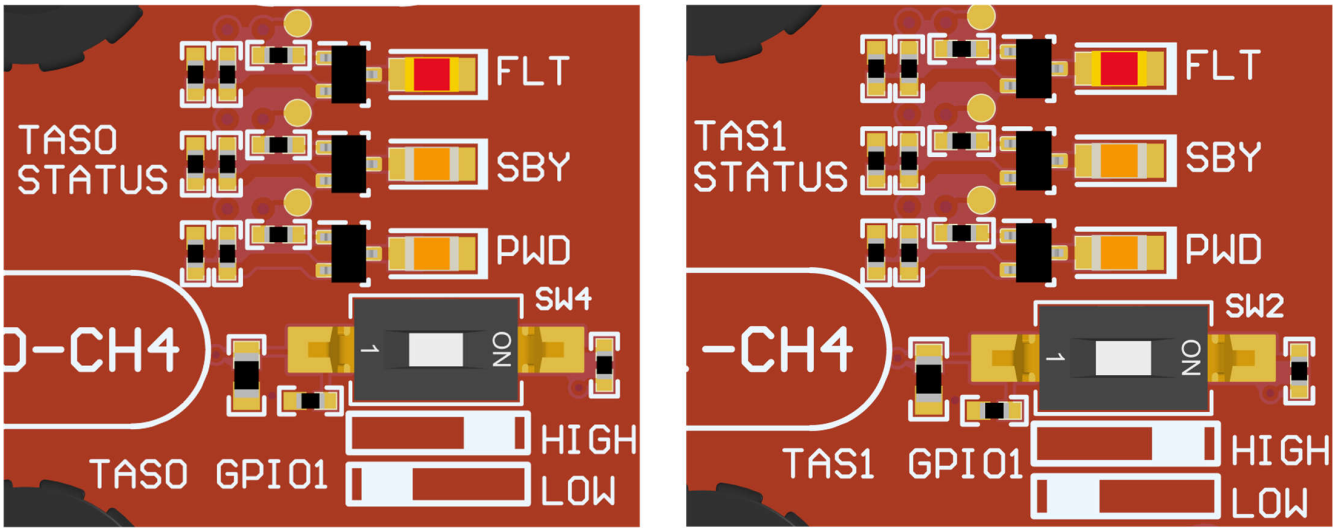


Figure 2-8. TAS0 and TAS1 GPIO0 Select Switch PCB Detail Excerpt

2.7 Indicator LED

Multiple LEDs are used to provide quick visual indication of the operating state of the TAS67CD-AEC. See the Figure 2-9 figure for all LED locations and Table 2-9 for all LED state definitions.

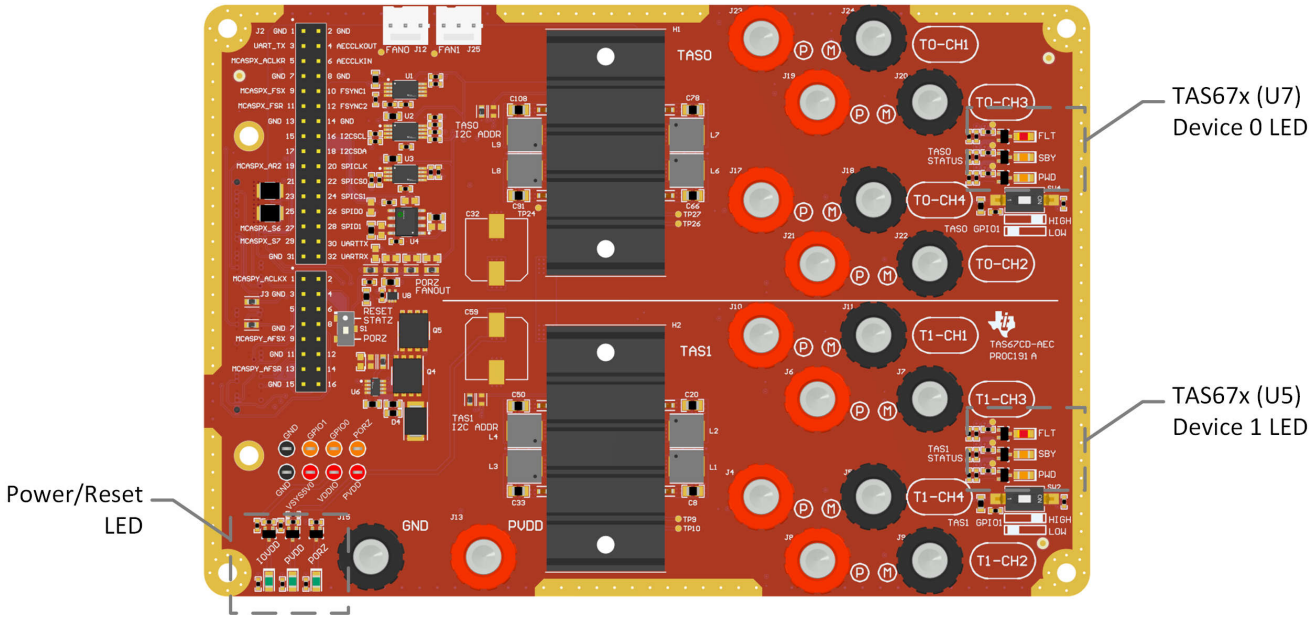


Figure 2-9. TAS67CD-AEC Indicator LED Locations

Table 2-9. Indicator LED Definitions

Function Grouping	Reference Designator	Description	
Power Enabled Indicators	D5	VDDIO - Digital I/O Power Power Enabled	• Lit: VDDIO enabled • Unlit: VDDIO not enabled
	D6	PVDD - Amplifier Power Power Enabled	• Lit: PVDD enabled • Unlit: PVDD not enabled
Reset Indicators	D11	System PORZ State Indicator	• Lit: PORZ high - system out of reset • Unlit: PORZ low - system held in reset

Table 2-9. Indicator LED Definitions (continued)

Function Grouping	Reference Designator	Description	
TAS0 (U7) Indicators	D8	Standby (STBY#) state indicator	• Lit: TAS67x in standby • Unlit: TAS67x not in standby (normal operating state)
	D9	Fault (FAULT#) state indicator	• Lit: TAS67x in fault state • Unlit: TAS67x not in fault (normal operating state)
	D10	Power-Down (PD#) state indicator	• Lit: TAS67x in power down • Unlit: TAS67x out of power down (normal operating state)
TAS1 (U5) Indicators	D1	Standby (STBY#) state indicator	• Lit: TAS67x in standby • Unlit: TAS67x not in standby (normal operating state)
	D2	Fault (FAULT#) state indicator	• Lit: TAS67x in fault state • Unlit: TAS67x not in fault (normal operating state)
	D3	Power-Down (PD#) state indicator	• Lit: TAS67x in power down • Unlit: TAS67x out of power down (normal operating state)

2.8 Test Points

Multiple debug hooks are included to enable quick probing of critical system power and signal nets. These are implemented as small through-hole mounted loops for ease of attaching different oscilloscope probes and meter leads.

Table 2-10. Debug Hook Description

Reference Designator	Attached Signal
TP4	VSYS5V0
TP6	PVDD
TP33	VDDIO
TP35, TP34	GND
TP5	PORZ
TP20	GPIO0
TP22	GPIO1

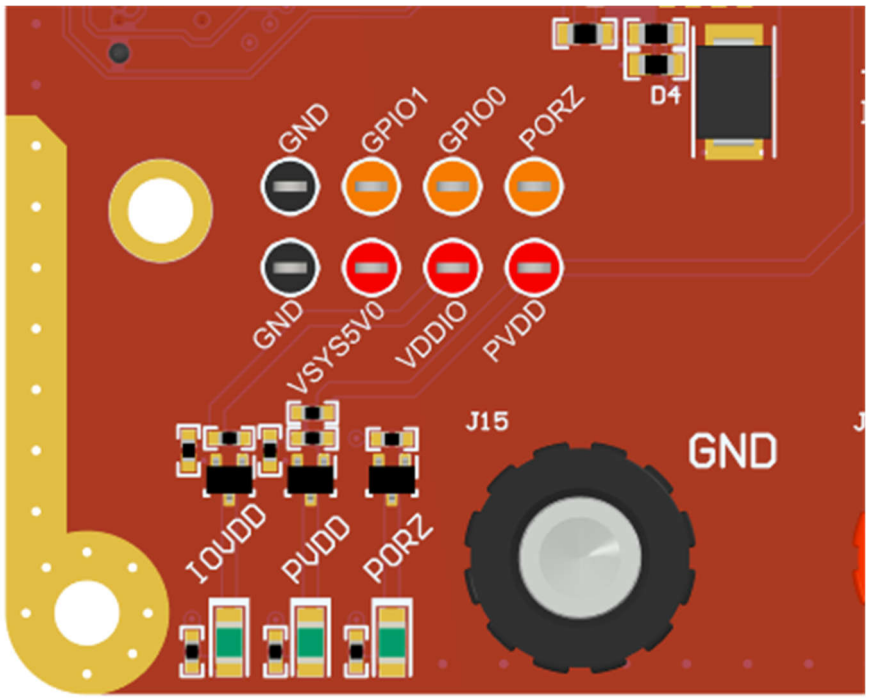


Figure 2-10. Debug Hooks

3 Software

AM275 Software Development Kits

AM275x software development kits (SDK) are available for download at the AM2754-Q1 Product Page. Each of these SDK include application software examples making use of the TAS67CD-AEC add-on board. See SDK documentation for details.

- AM275-FREERTOS-SDK FreeRTOS SDK for AM275 – RTOS, No-RTOS
- AM275-AWE-SDK Audio Weaver SDK based on AM275 (available upon request)

AM62D Software Development Kits

AM62D software development kits (SDK) are available for download at the AM62D-Q1 Product Page. Each of these SDK include application software examples making use of the TAS67CD-AEC add-on board. See SDK documentation for details.

- AM62D-RESTRICTED-SW AM62D SDKs for the early customers (available upon request)
- AM62D-AWE-SDK Audio Weaver SDK based on AM62d (available upon request)

AM275 and AM62D SDK version 11.0 support

The examples in version 11.0 of both the AM275 and AM62D SDK require additional modification to work with Rev A of the TAS67CD-AEC. The Rev A design requires writing a logic 1 to the STBY pins of each TAS67 device to wake the device from standby mode. Waking the device from standby must be done before sending any I2C commands to the TAS67 for configuration so the TAS67 is configured correctly. The TAS67 STBY pins are routed to the AEC connector and are connected to the AM275 and AM62D devices GPIO pins as specified in Table 3-1

Table 3-1. TAS67 STBY routing to AM275 and AM62D

TAS67	AM275 EVM	AM62D EVM
AEC1 TAS0	MCU_GPIO0_15 (A6)	EXP1_GPIO0_33 (L17)
AEC1 TAS1	GPIO0_12 (C16)	EXP1_GPIO0_34 (K19)
AEC2 TAS0	MCU_GPIO0_4 (A9)	EXP2_GPIO0_57 (W20)
AEC2 TAS1	MCU_GPIO0_3 (B8)	EXP2_GPIO0_58 (W19)

4 Hardware Design Files

TAS67CD-AEC Rev A Design Files

See the **TAS67CD-AEC Design File Package** for the full TAS67CD-AEC design package.

- Altium Designer 24 project files schematic, layout and BOM
- Fabrication ready CAM in Gerber/ODB++ formats

5 References

Reference Documents

In addition to this document, the following references are available for download:

TAS6754-Q1 Documentation

- TAS6754-Q1 Automotive, 19V, digital-input four-channel Class-D audio amplifier with 1L modulation
- TAS6754-Q1 Datasheet
- **TAS6754Q1EVM** TAS6754-Q1 evaluation module

AM275x DSP Documentation

- **AM2754-Q1** 80 GFLOPS DSP microcontroller for automotive audio with quad core ARM® Cortex®-R5F, 10.75MB SRAM
- AUDIO-AM275-EVM AM275x audio evaluation module

AM62Dx DSP Documentation

- **AM62D-Q1** Automotive 40GFLOPS DSP audio processor with Arm® Cortex®-A53, Cortex-R5F and LPDDR4
- AUDIO-AM62D-EVM AM62D expandable hardware for premium audio

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7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2025	*	Initial release.

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3.1.1 *Notice applicable to EVMs not FCC-Approved:*

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3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

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Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

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