Description

The AUDIO-AM62D-EVM evaluation module (EVM) is a low-cost expandable hardware designed for evaluating and prototyping multi-channel audio applications across various use cases. At the core of the AUDIO-AM62D-EVM EVM is the AM62D System-on-Chip (SoC), featuring TI's vector-based C7x DSP core tightly coupled with Matrix Multiplication Accelerator (MMA), single-cycle accessible 1.25MB of L2 memory, a Quad-Core Arm®-Cortex® A53 microprocessor, a Dual-core Arm Cortex-R5F MCU and a LPDDR4 32-bit controller, all protected by an automotive-grade security hardware module. It is an excellent choice for those looking to develop Automotive premium amplifier.

The AUDIO-AM62D-EVM includes multiple audio jacks and expansion connectors for high-performance audio processing, two Gigabit Ethernet expansion connectors, two USB Type-C® ports, CAN-FD and other interfaces to facilitate easy prototyping. Additionally, it features two on-board temperature sensors for monitoring SoC and LPDDR4 thermal conditions.

Get Started

1. Order the EVM at AUDIO-AM62D-EVM
2. Download the EVM design files.
3. Download the software from AUDIO-AM62D-EVM
4. Read this EVM User's Guide.

Features

- 4x 3.5mm TRS Audio Jack Line In
- 4x 3.5mm TRS Audio Jack Line Out
- 2x Audio expansion connector
- 2x Gigabit Ethernet expansion connector
- 4GB LPDDR4 memory
- 512Mb OSPI Flash memory
- 32GB eMMC Flash memory
- MicroSD card slot
- 1x USB2.0 Type-C
- 1x USB2.0 Type-A
- 2x MCAN headers

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1 Evaluation Module Overview

1.1 Introduction

This technical user’s guide describes the hardware architecture of the AM62D Audio EVM, a low-cost EVM built around the AM62D System-on-Chip (SoC). The AM62D processor comprises of a single-core C7x DSP with Matrix Multiplication Accelerator, a Quad-Core Arm Cortex- A53 microprocessor, and a Dual-core Arm Cortex-R5F MCU. The EVM with 4x TRS Audio Jack Line In and 4x TRS Audio Jack Line Out, along with two audio expansion and two Ethernet expansion connectors is an excellent choice for evaluation and prototyping of multi-channel audio applications using high-performance DSP. The embedded emulation logic in the EVM allows for emulation and debugging using standard development tools such as Code Composer Studio™ IDE from Texas Instruments.

1.2 Kit Contents

This package includes:

- "AUDIO-AM62D-EVM" EVM
- EVM user's guide pamphlet
- EVM disclaimer and standard terms

1.3 Specification

Figure 1-1 shows the functional block diagram of the AM62D Audio EVM.

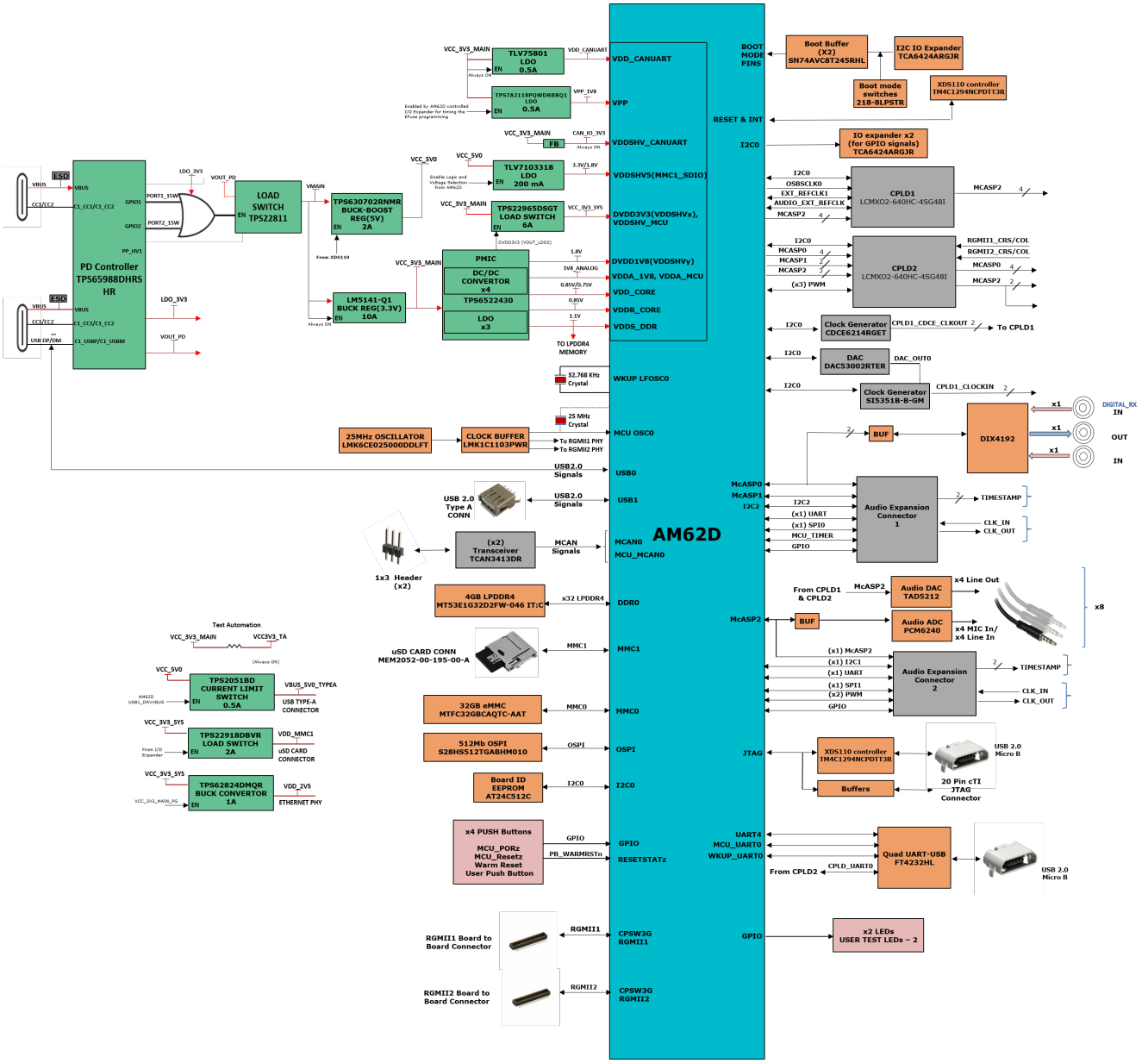


Figure 1-1. Functional Block Diagram of the AM62D Audio EVM

1.4 Device Information

The AUDIO-AM62D-EVM supports FreeRTOS development with a feature-rich software development kit (SDK). On-chip emulation logic allows for emulation and debugging using standard development tools such as the Code Composer Studio IDE from TI as well as an intuitive out-of-box user's guide to quickly start design evaluation.

1.5 EVM Revisions and Assembly Variants

The various AM62D Audio EVM PCB design revisions, and assembly variants are listed in Table 1-1. Specific PCB revision is indicated in silkscreen on the PCB. Specific assembly variant is indicated with additional sticker label.

Table 1-1. EVM PCB Design Revisions, and Assembly Variants

OPN	PCB Revision	Assembly Variant	Revision and Assembly Variant Description
AUDIO-AM62D-EVM	PROC180E1	N/A (single variant produced)	First prototype, early release revision of the AM62D Audio EVM.

Table 1-1. EVM PCB Design Revisions, and Assembly Variants (continued)

OPN	PCB Revision	Assembly Variant	Revision and Assembly Variant Description
AUDIO-AM62D-EVM	PROC180E2	N/A	Second prototype, early release revision of the AM62D Audio EVM. Implements a number of changes and bug fixes.

2 Hardware

2.1 Additional Images

This section shows the AM62D Audio EVM images and location of various blocks on the board.

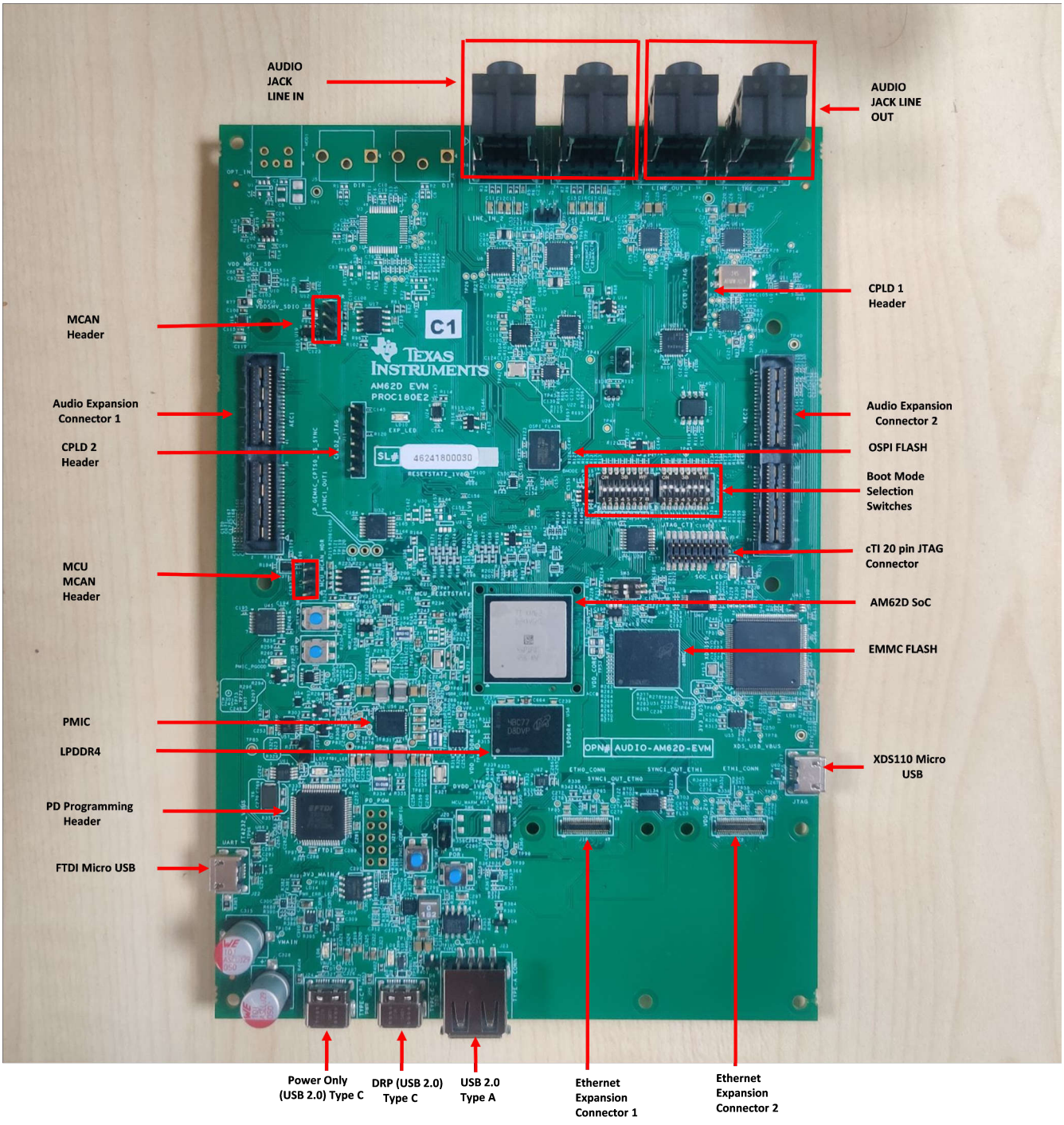


Figure 2-1. AM62D Audio EVM Top Side

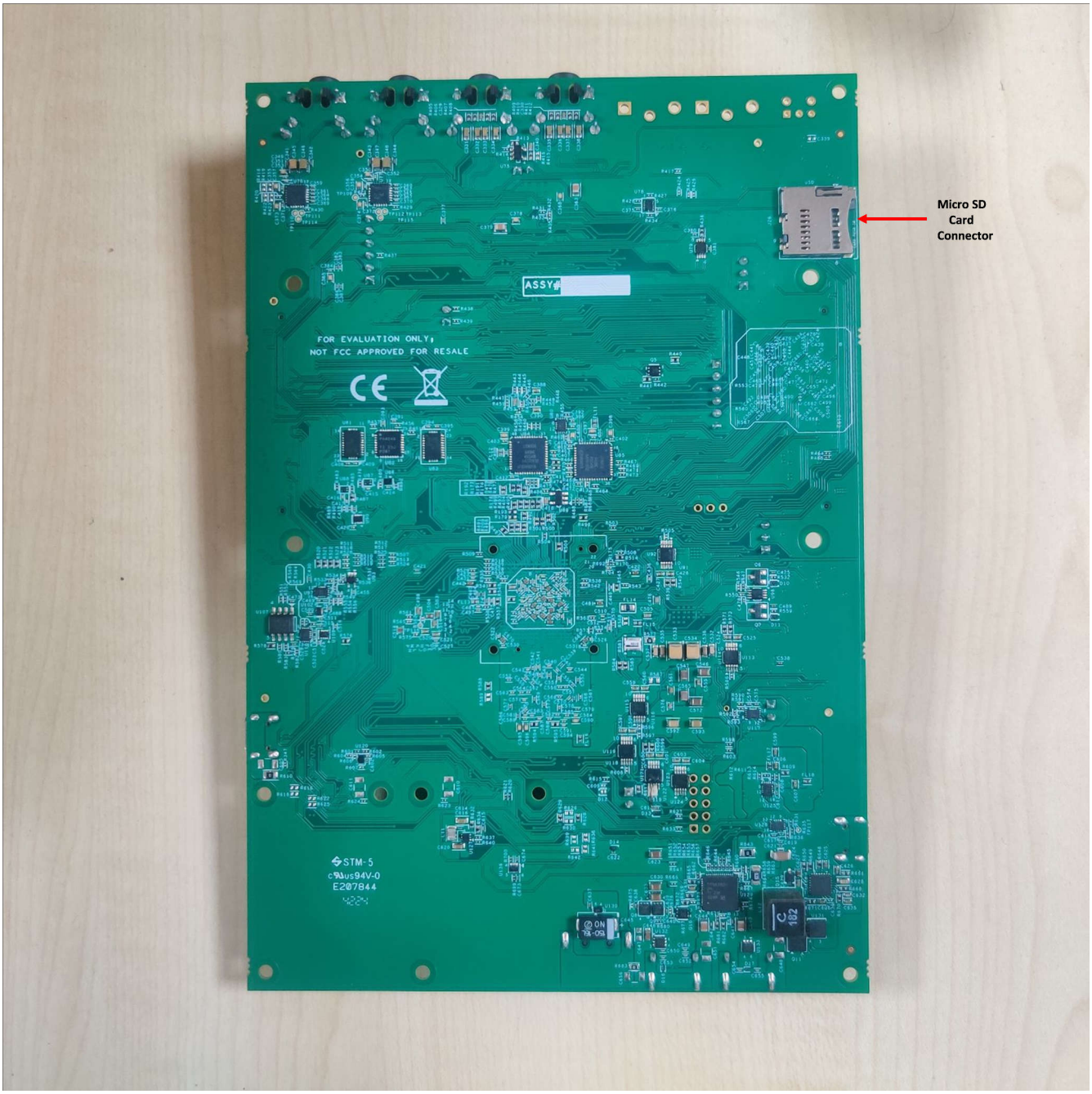


Figure 2-2. AM62D Audio EVM Bottom Side

2.2 Key Features

The AM62D Audio EVM is a high performance, standalone development platform that enables users to evaluate and develop audio applications for the AM62D System-on-Chip (SoC) from Texas Instruments.

The following sections discuss the key features of the AM62D Audio EVM.

2.2.1 Processor

- AM62D SoC, 18mm x 18mm, 0.8mm pitch, 484-pin fcBGA.

2.2.2 Power Supply

- Two USB2.0 Type-C ports (5V-15V input range).

- Optimized power designs with PMIC, discrete regulators and LDOs for the processor and peripherals.

2.2.3 Memory

- 4GB LPDDR4 supporting data rate up to 3733MT/s.
- MicroSD® Card slot with UHS-1 support.
- 512Mbit Octal SPI NOR Flash memory.
- 512Kbit Inter-Integrated Circuit (I2C) board ID EEPROM.
- 32GB eMMC Flash.

2.2.4 JTAG/Emulator

- XDS110 On-Board Emulator.
- Supports 20-pin JTAG connection from external emulator.

2.2.5 Supported Interfaces and Peripherals

- 1x USB2.0 Type-C Interface, support DFP and UFP modes (Data) and DRP mode (Power).
- 1x USB2.0 Host Interface, Type-A.
- Analog audio interface consists of 4x Stereo Audio Jack Mic/Line In, 4x Stereo Audio Jack Line In and 8x Stereo Audio Jack Line out
- Digital audio interface consists of 1x Coaxial input, 1x Optical Input and 1x Coaxial Output.
- 2x Gigabit Ethernet signals supporting 10/100/1000Mbps data are terminated on expansion connectors.
- Quad port UART-to-USB circuit over micro-B USB connector.
- User Test LEDs.
- INA devices for current monitoring.
- 2x Temperature Sensors near SoC and LPDDR4 for thermal monitoring.

2.2.6 Expansion Connectors/Headers to Support Application Specific Add-On Boards

- 2x Gigabit Ethernet expansion connectors
- 2x Audio Expansion connectors
- 2x MCAN headers

2.3 Power Requirement

The AM62D Audio EVM can be powered through either of the two USB2.0 Type-C Connectors:

- Connector 1 (J24) - Power role – SINK, No Data role
- Connector 2 (J25) - Power role – DRP, Data role – USB2.0 DFP or UFP

The AM62D Audio EVM supports voltage input ranges of 5V-15V and 3A of current. A USB PD controller manufacturer part number TPS65988DHRSHR is used for PD negotiation upon cable detection to get necessary power required for the board. Connector 1 is configured to be an UFP Port and has no Data role. Connector 2 is configured as a DRP port, it can act as DFP only when the board is being powered by Connector 1. When both the connectors are connected to external power supply, the port with highest PD power contract will be selected to power the board.

Table 2-1. Type-C Port Power Roles

J24 (UFP)	J25 (DRP)	Board Power	Remarks
Plugged in	NC	ON – J24	J24 will be UFP and will only sink power & J25 can act as DFP if a peripheral is connected
NC	Plugged in	ON – J25	J25 will be UFP and can only sink power
Plugged in	Plugged in	ON – J24 or J25	Board will be powered by the port with highest PD power contract

The PD IC uses a SPI EEPROM to load the necessary configuration on power up so it can negotiate a power contract with a compatible power source.

The configuration file is loaded to the EEPROM using header J21. Once the EEPROM is programmed the PD obtains the configuration files via SPI communication. Upon loading the configuration files, the PD negotiates with the source to obtain the necessary power requirement.

Note

The EEPROM is preprogrammed with the configuration file for the operation of the PD controller

Power indication LEDs are provided for both the Type-C connectors for the user to identify which connector is powering the EVM Board. An external power supply (Type-C output) can be used to power the EVM but is not included as part of the EVM kit.

The external power supply requirements (Type-C) are:

Table 2-2. Recommended External Power Supplies

DigiKey Part Number	Manufacturer	Manufacturer Part Number
1939-1794-ND	GlobTek, Inc.	TR9CZ3000USBCG2R6BF2
Q1251-ND	Qualtek	QADC-65-20-08CB

Note

Minimum Voltage: 5VDC, Recommended Minimum Current: 3000mA
Maximum Voltage: 15VDC, Maximum current: 5000mA.
Because AM62D implements USB PD for power, the device is able to negotiate to the highest Voltage/ Current combination supported by both the Device and Power Adapter, as such, if the power supply exceeds the maximum voltage and current requirements listed above is acceptable as long as the power adapter is compliant with the USB-C PD specification.

2.4 Setup and Configuration

2.4.1 EVM DIP Switches

The AM62D Audio EVM has two 8-position DIP Switches to set the desired SoC Boot mode.

2.4.2 Boot modes

The boot mode for the EVM board is defined by two banks of switches SW1 and SW2. This allows for AM62D SoC Boot mode control by either the user (DIP Switch Control).

All the bits of switch (SW1 and SW2) have a weak pull down resistor and a strong pull up resistor as shown in Figure 2-3. Note that OFF setting provides a low logic level (‘0’) and an ON setting provide a high logic level (‘1’).

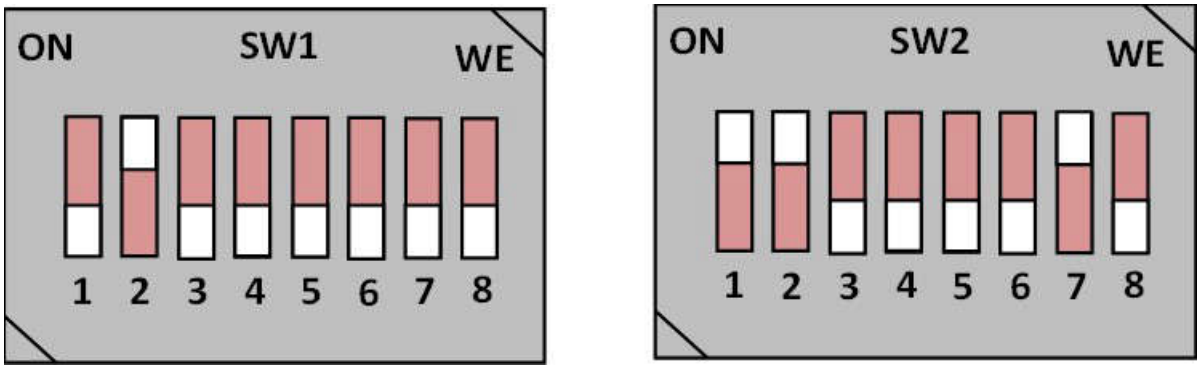


Figure 2-3. Boot Mode switch (MMCSD Boot)

The boot mode pins of the SoC have associated alternate functions during normal operation. Hence isolation is provided using Buffer ICs to cater for alternate pin functionality. The output of the buffer is connected to the boot mode pins on the AM62D SoC and the output is enabled only when the boot mode is needed during a reset cycle.

The input to the buffer is connected to the DIP switch circuit and to the output of an I2C I/O Expander set by the test automation circuit. If the test automation circuit controls the boot mode, all the switches should be manually set to the OFF position. The boot mode buffer is powered by an always ON power supply to ensure that the boot mode remains present even if the SoC is power cycled.

Switch SW1 and SW2 bits [15:0] are used to set the SoC boot mode.

The switch map to the boot mode functions is provided in the following tables.

Table 2-3. BOOTMODE Pin Mapping

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	Reserved	Backup Boot Mode Configuration	Backup Boot Mode			Primary Boot Mode Configuration			Primary Boot Mode				PLL Configuration		

- BOOTMODE [2:0] – Denote system clock frequency for PLL configuration.
  - Table 2-4 gives details on PLL reference clock selection.
- BOOTMODE [6:3] – This provides primary boot mode configuration to select the requested boot mode after POR, that is, the peripheral/memory to boot from primary boot device selection details.
  - Table 2-5 gives the primary boot mode configuration details.
- BOOTMODE [9:7] – These pins provide optional settings and are used in conjunction with the primary boot device selected.
  - Table 2-6 gives primary boot media configuration details.
- BOOTMODE [12:10] – Select the backup boot mode, that is, the peripheral/memory to boot from, if primary boot device failed.
  - Table 2-7 provides backup boot mode selection details.
- BOOTMODE [13] – These pins provide optional settings and are used in conjunction with the backup boot device. Switch SW1.6 when ON sets 1 and sets 0 if OFF, see the device-specific TRM.
- BOOTMODE [15:14] – Reserved. Provides backup boot media configuration options.

Table 2-4. PLL Reference Clock Selection BOOTMODE [2:0]

SW2.3	SW2.2	SW2.1	PLL REF CLK (MHz)
OFF	OFF	OFF	19.2
OFF	OFF	ON	20
OFF	ON	OFF	24
OFF	ON	ON	25
ON	OFF	OFF	26
ON	OFF	ON	27
ON	ON	OFF	RSVD
ON	ON	ON	RSVD

Table 2-5. Boot Device Selection BOOTMODE [6:3]

SW2.7	SW2.6	SW2.5	SW2.4	Primary Boot Device Selected
OFF	OFF	OFF	OFF	Serial NAND
OFF	OFF	OFF	ON	OSPI
OFF	OFF	ON	OFF	QSPI
OFF	OFF	ON	ON	SPI
OFF	ON	OFF	OFF	Ethernet RGMII
OFF	ON	OFF	ON	Ethernet RMII
OFF	ON	ON	OFF	I2C
OFF	ON	ON	ON	UART
ON	OFF	OFF	OFF	MMC/SD card
ON	OFF	OFF	ON	eMMC

Table 2-5. Boot Device Selection BOOTMODE [6:3] (continued)

SW2.7	SW2.6	SW2.5	SW2.4	Primary Boot Device Selected
ON	OFF	ON	OFF	USB0
ON	OFF	ON	ON	GPMC NAND
ON	ON	OFF	OFF	GPMC NOR
ON	ON	OFF	ON	Rsvd
ON	ON	ON	OFF	xSPI
ON	ON	ON	ON	No boot/Dev Boot

Table 2-6. Primary Boot Media Configuration BOOTMODE [9:7]

SW1.2	SW1.1	SW2.8	Boot Device
Reserved	Read Mode 2	Read Mode 1	Serial NAND
Reserved	Iclk	Csel	QSPI
Reserved	Iclk	Csel	OSPI
Reserved	Mode	Csel	SPI
Clkout	0	Link Info	Ethernet RGMII
Clkout	Clk src	0	Ethernet RMII
Bus Reset	Reserved	Addr	I2C
Reserved	Reserved	Reserved	UART
1	Reserved	Fs/raw	MMC/ SD card
Reserved	Reserved	Reserved	eMMC
Core Volt	Mode	Lane swap	USB0
Reserved	Reserved	Reserved	GPMC NAND
Reserved	Reserved	Reserved	GPMC NOR
Reserved	Reserved	Reserved	Reserved
SFPD	Read Cmd	Mode	xSPI
Reserved	ARM/Thumb	No/Dev	No boot/Dev Boot

Table 2-7. Backup Boot Mode Selection BOOTMODE [12:10]

SW1.5	SW1.4	SW1.3	Backup Boot Device Selected
OFF	OFF	OFF	None(No backup mode)
OFF	OFF	ON	USB
OFF	ON	OFF	Reserved
OFF	ON	ON	UART
ON	OFF	OFF	Ethernet
ON	OFF	ON	MMC/SD
ON	ON	OFF	SPI
ON	ON	ON	I2C

2.4.3 User Test LEDs

The AM62D Audio EVM board contains two LEDs for user defined functions.

Table 2-8 indicates the User Test LEDs and the associated GPIOs used to control it.

Table 2-8. User Test LEDs

Sl #	LED	GPIO used	SCH Net Names
1	LD1	GPIO1_49	SOC_GPIO1_49
2	LD10	U21.24(P27)	IO_EXP_TEST_LED

2.5 Power ON/OFF Procedures

Power to the EVM is provided through an external power supply with PD capability to either of the two USB Type-C Ports.

Note

TI recommends the maximum length of the I/O cables not exceed 3 meters.

2.5.1 Power ON Procedure

1. Place the EVM boot switch selectors (SW1, SW2) into selected boot mode. Example boot mode for SD card is shown in Figure 2-4.
2. Connect your boot media (if applicable).
3. Attach the PD capable USB Type-C® cable to the EVM Type-C (J24 or J25) Connector.
4. Connect the other end of the Type-C cable to the source, either AC Power Adapter, or Type-C source device (such as a laptop/computer)
5. Visually inspect that either LD8 or LD9 LED is illuminated.
6. XDS110 JTAG and UART debug console outputs are routed to micro-USB ports J17 and J22, respectively.

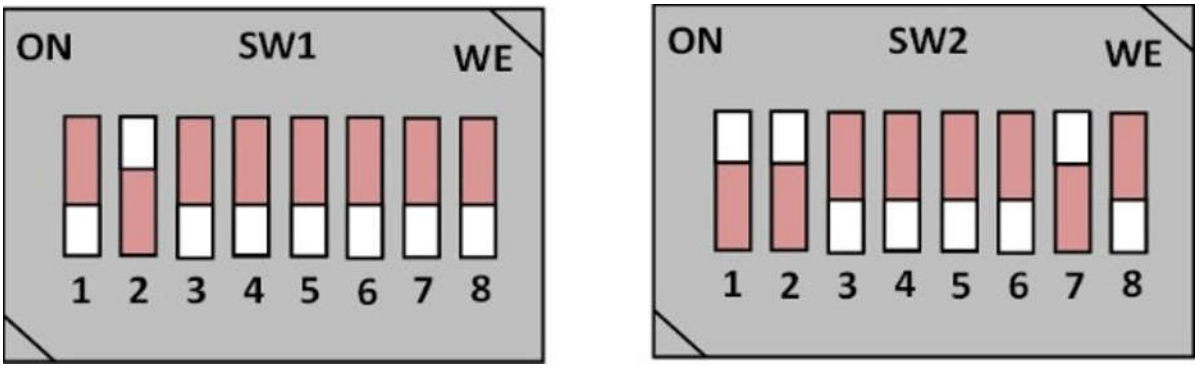


Figure 2-4. Example Boot Mode (MMCSD Boot)

2.5.2 Power OFF Procedure

1. Disconnect AC power from AC/DC converter.
2. Remove the USB Type-C cable from the EVM.

2.5.3 Power Test Points

Test points for each power output on the board are mentioned in Table 2-9.

Table 2-9. Power Test Points

Sl #	Power Supply	Test Point	Voltage
1	VMAIN	TP104	12V
2	VCC_3V3_MAIN	TP102	3.3V
3	VCC_3V3_SYS	TP48	3.3V
4	VDD_CORE	TP53	0.85V
5	VDDR_CORE	TP60	0.85V
6	VCC1V8_SYS	TP86	1.8V
7	VDDA_1V8	TP79	1.8V
8	VDD_LPDDR4	TP81	1.1V
9	VDD_MMC1_SD	TP21	3.3V
10	VCC_5V0	TP103	5V
11	VDD_CANUART	TP52	0.85V
12	VDDSHV_SDIO	TP35	3.3V
13	VPP_1V8	TP69	1.8V

Table 2-9. Power Test Points (continued)

Sl #	Power Supply	Test Point	Voltage
14	VDD_2V5	TP92	2.5V
15	VBUS_TYPEC1	TP107	5V
16	VBUS_TYPEC2	TP108	5V
17	VBUS_5V0_TYPEA	TP105	5V
18	VCC3V3_XDS	TP68	3.3V
19	XDS_USB_VBUS	TP78	5V
20	FT4232_USB_VBUS	TP96	5V
21	VCC_3V3_FT4232	C285.1	3.3V

2.6 Interfaces

The following sections provide an overview of the different interfaces and circuits on the AM62D Audio EVM. Table 2-10 shows the interface mapping for the AM62D Audio EVM.

2.6.1 AM62D Audio EVM Interface Mapping

Table 2-10. Interface Mapping

Interface Name	Port on SoC	Device Part Number
Memory – LPDDR4	DDR0	MT53E1G32D2FW-046 IT:C
Memory – OSPI	OSPI0	S28HS512TGABHM010
Memory – MicroSD Socket	MMC1	MEM2052-00-195-00-A
Memory – eMMC	MMC0	MTFC32GAZAQHD-IT
Memory – Board ID EEPROM	SoC_I2C0	AT24C512C-MAHM-T
Ethernet Expansion Connector CPSW 1	SoC_RGMII1	DF40GB-48DP-0.4V
Ethernet Expansion Connector CPSW 2	SoC_RGMII2	DF40GB-48DP-0.4V
GPIO Port Expander1	SoC_I2C0	TCA6424ARGJR
Audio Expansion Connector 1	SPI0, SPI2, UART5, SoC_I2C2, McASP1, McASP0 and GPIOs	QSE-040-01-L-D-A-K
Audio Expansion Connector 2	SPI0, SPI1, UART6, SoC_I2C1, McASP2 and GPIOs	QSE-040-01-L-D-A-K
USB2.0 Type-C	USB0	2012670005
USB2.0 Type-A	USB1	629104151021
On-board Audio MIC / Line IN	McASP2_ACLKR , McASP2_AFSR andSoC_I2C	PCM6240QRTVRQ1 + STX-4235
On-board Audio Stereo Line OUT	McASP2_ACLKX ,McASP2_AFSX andSoC_I2C0	TAD5212IRGER + STX-4235
GPIO Port Expander2	SoC_I2C0	TCA6416ARTWR
MCAN header - 1x3 HDR	MCU_MCAN0, MCAN0	
UART Terminal (UART-to-USB)	SoC_UAR SoC_UART4, WKUP_UART0 , CPLD_UART0 and MCU_UART0	FT4232HL + 629105150521
Temperature Sensors	SoC_I2C0	TMP100NA/3K
Current Monitors	SoC_I2C0	INA228AIDGSR

2.6.2 Audio Interface

2.6.2.1 Audio Stereo Lineouts

The AM62D Audio EVM supports TI's TAD5212IRGER Stereo DAC interfaced to McASP2 group of signals. The EVM shall have 4x stereo digital to analog converters (DAC).

The device is provided with an analog supply of 3.3V and digital core supply of 1.8V. The TAD5212 configuration are supported through I2C interface. (SoC_I2C0) The I2C addresses of the TAD5212 devices are 0x50, 0x51,

0x52 and 0x53. Each TAD5212 device receives the digital input data, clock and frame sync signals from the CPLD which acts as buffer for MCASP2 signals.

The DAC IC is connected to 2 stacked 3.5mm TRS Audio Jack connectors J3 and J4 with manufacturer part number STX-4235 for 4x Stereo audio Jack Line out.

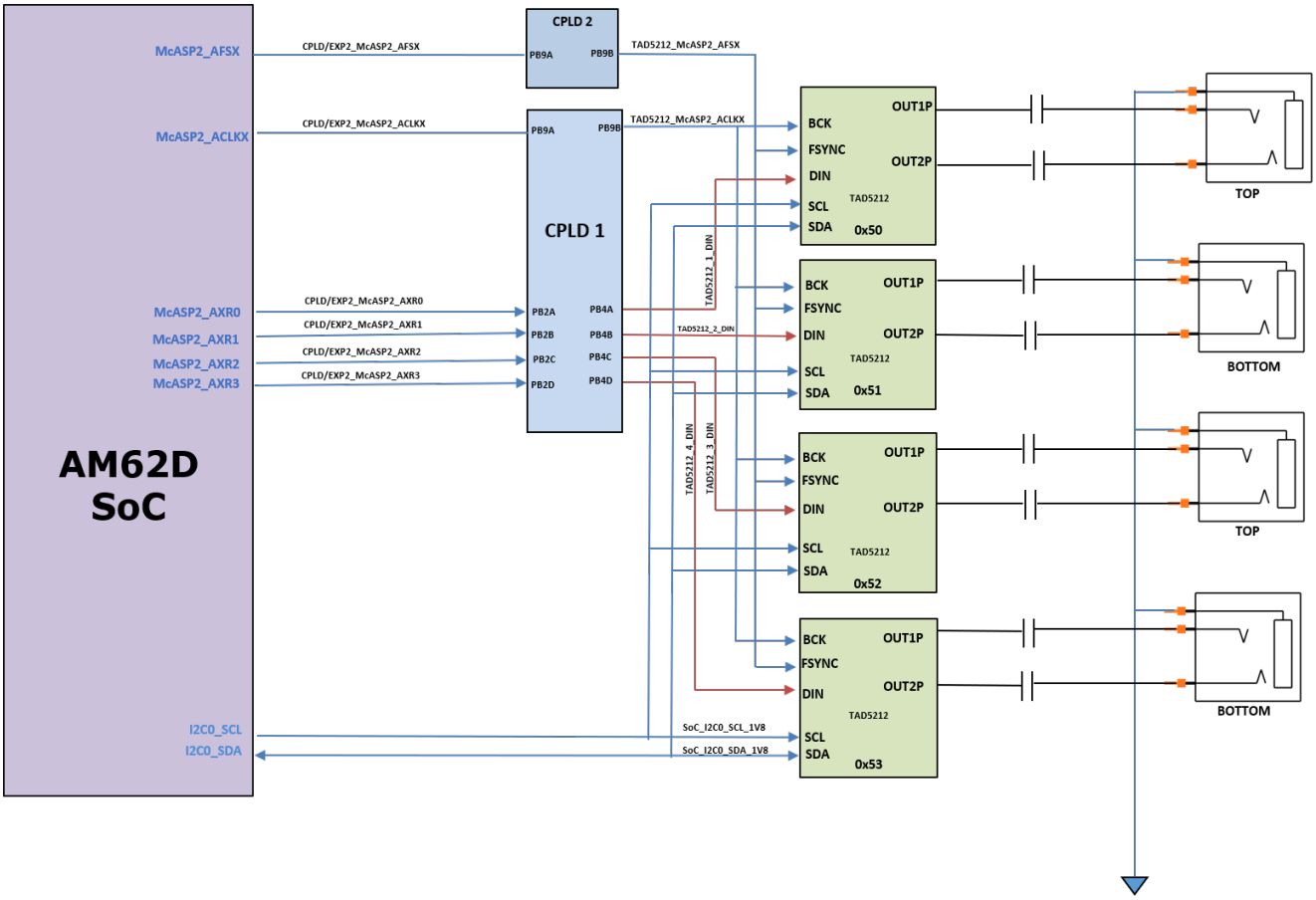


Figure 2-5. Audio Stereo Lineout Block Diagram

2.6.2.2 Audio Microphone / Line In

The AM62D Audio EVM will have audio analog-to-digital converters (ADC) manufacturer part number PCM6240QRTVRQ1 to interface with McASP2 of SoC. The PCM6240 has Analog supply of 3.3V and digital supply of 1.8V and VBAT_IN is used for enabling input fault diagnostics.

The PCM6240QRTVRQ1 configuration control is supported over the SoC_I2C0 instance. In PCM6240QRTVRQ1 I2C target address is set using ADDR1_MISO and ADDR0_SCLK pins. The I2C address for audio device (PCM6240) are 0x48 and 0x49. The Buffer enable manufacturer part number SN74LVC1G126DBVR for the serial data output is controlled by the CPLD1.

The ADC is connected to 2x stacked 3.5mm TRS Audio Jack connectors with manufacturer part number STX-4235 for 4x Stereo Audio Jack Mic/Line In.

Reset: The reset for the PCM6240 is connected to a circuit that ANDs the RESETSTATz from the AM62D SoC with the signal GPIO_PCM_RST from the I/O expander. A pull-up resistor is provided on PCM_RSTn to set the default active state.

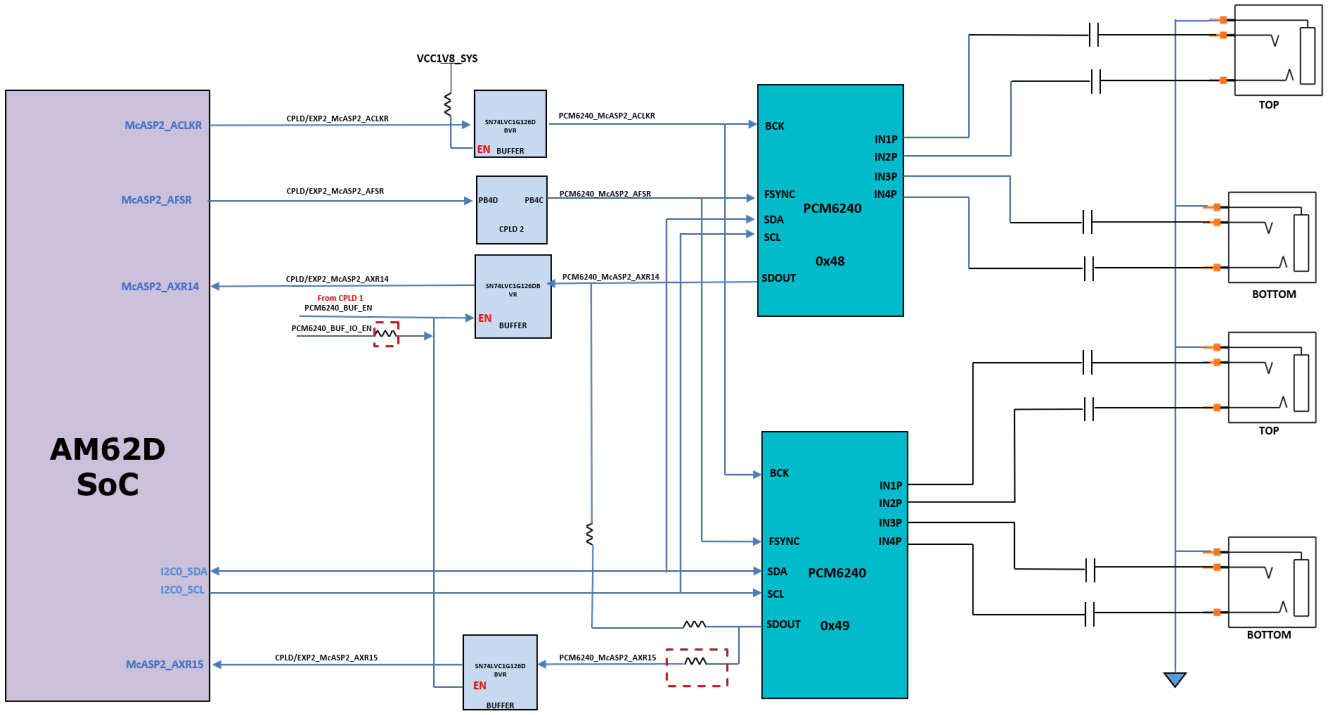


Figure 2-6. Audio Microphone / Line In Block Diagram

2.6.3 JTAG Interface

The AM62D Audio EVM board includes XDS110 class on-board emulation. The connection for this emulator uses an USB 2.0 micro-B connector and the circuit acts as a Bus powered USB device. The VBUS power from the connector is used to power the emulation circuit such that connection to the emulator is not lost when the power to the EVM is removed. Voltage translation buffers are used to isolate the XDS110 circuit from the rest of the EVM.

Optionally, the JTAG Interface on the AM62D Audio EVM is also provided through a 20-pin Standard JTAG cTI Header J19. This allows the user to connect an external JTAG Emulator Cable. Voltage translation buffers are used to isolate the JTAG signals of cTI header from the rest of the EVM. The output of the voltage translators from XDS110 Section and cTI Header Section are muxed and connected to the AM62D JTAG Interface. If a connection to the cTI 20-pin JTAG connector is sensed using an auto presence detect circuit, the mux routes the 20-pin signals from the cTI connector to the AM62D SoC in place of the on-board emulation circuit.

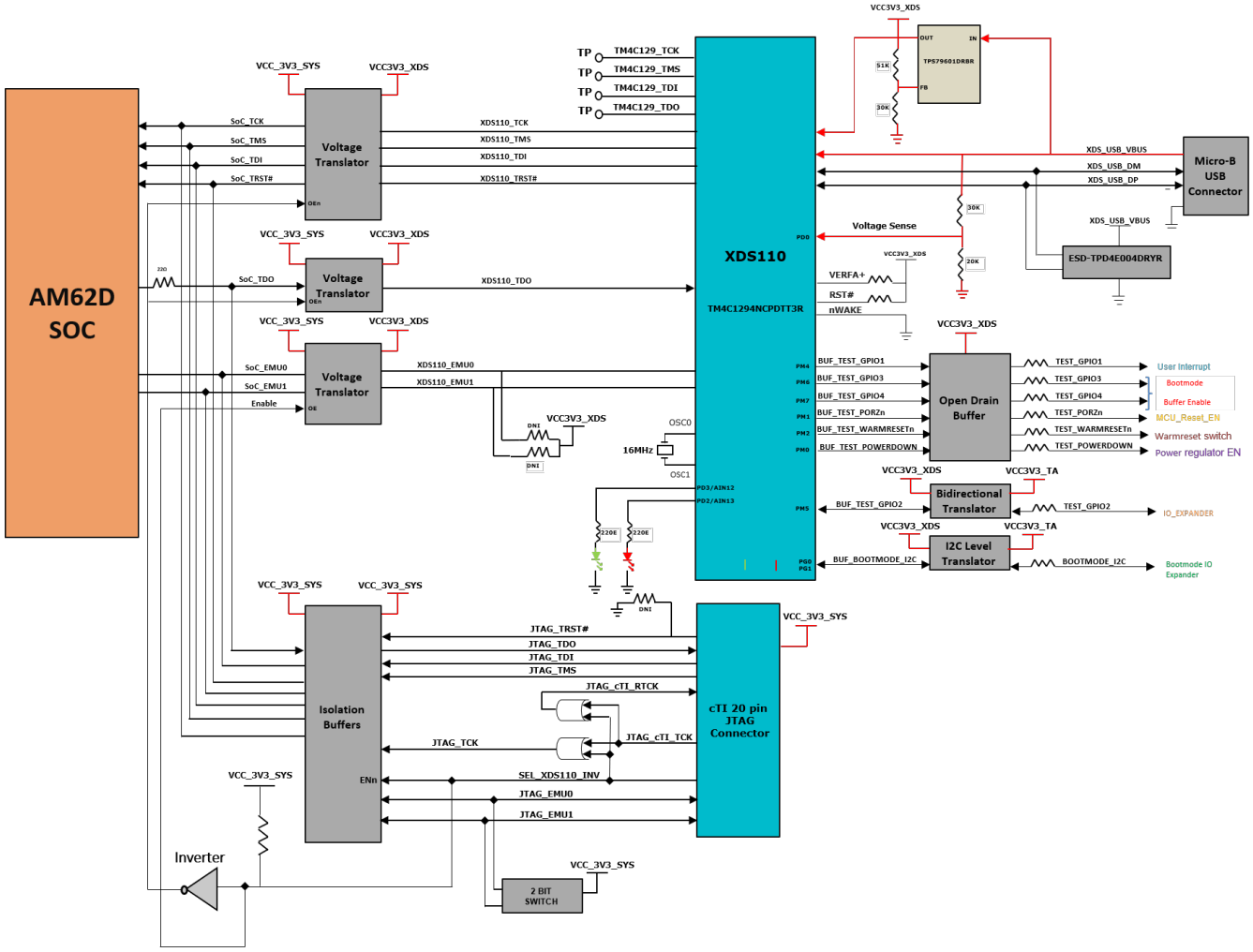


Figure 2-7. JTAG Interface Block Diagram

The pin-outs of the cTI 20-pin JTAG connector are given in Table 2-11. An ESD protection part number TPD4E004 is provided on USB signals to steer ESD current pulses to VCC or GND. TPD4E004 protects against ESD pulses up to ±15kV Human-Body Model (HBM) as specified in IEC 61000-4-2 and provides ±8kV contact discharge and ±12kV air-gap discharge.

Table 2-11. JTAG Connector (J14) Pinout

Pin No.	Signal
1	JTAG_TMS
2	JTAG_TRST#
3	JTAG_TDI
4	JTAG_TDIS
5	VCC_3V3_SYS
6	NC
7	JTAG_TDO
8	SEL_XDS110_INV
9	JTAG_cTI_RTCK
10	DGND
11	JTAG_cTI_TCK
12	DGND
13	JTAG_EMU0

Table 2-11. JTAG Connector (J14) Pinout (continued)

Pin No.	Signal
14	JTAG_EMU1
15	JTAG_EMU_RSTn
16	DGND
17	NC
18	NC
19	NC
20	DGND

2.6.4 UART Interface

The four UART ports of the SoC (MCU UART0, WKUP UART0, SoC UART4 and CPLD UART0) are interfaced with an FTDI Bridge FT4232HL for USB-to-UART functionality and then terminated on a micro-B USB connector (J22) on board. When the AM62D Audio EVM is connected to a Host using USB cable, the computer can establish a Virtual COM Port which can be used with any terminal emulation application. The FT4232HL device is bus powered.

Since the circuit is powered through the USB BUS, the connection to the COM port will not be lost when the EVM power is removed.

Table 2-12. UART Port Interface

UART Port	USB-to-UART Bridge	USB Connector	COM Port
SoC_UART4	FT4232HL	J22	COM1
CPLD_UART0			COM2
WKUP_UART0			COM3
MCU_UART0			COM4

The FT4232 chip is configured to operate in "Single-chip USB to four-channel UART" mode using the configuration file from an external SPI EEPROM connected to it. The EEPROM (93LC46B) supports 1Mbit/s clock rate. The EEPROM is programmable in-circuit over USB using a utility program called FT_PROG available from FTDI's web site. The FT_PROG is also used for programming the board serial number for users to identify the connected COM port with board serial number when one or more boards are connected to the computer.

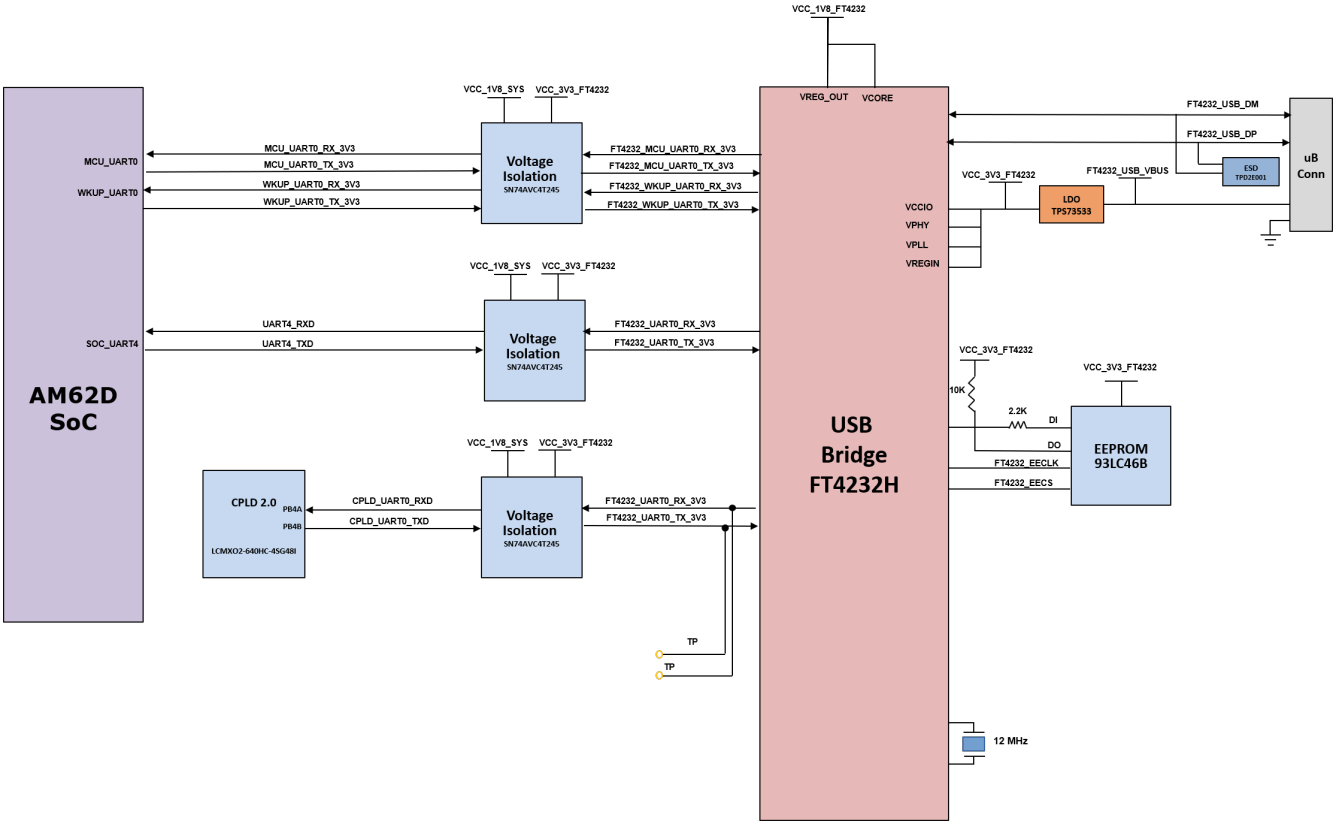


Figure 2-8. UART Interface Block Diagram

2.6.5 USB Interface

2.6.5.1 *USB2.0 Type-A Interface*

USB2.0 Data lines DP and DM from Type-A connector J23 are connected to the USB1 interface of the AM62D SoC to provide USB high-speed/full-speed communication. USB1_VBUS to the SoC is provided through a resistor divider network to support (5V-30V) VBUS operation. USB1_DRVVBUS from SoC is connected to the enable pin of a 500mA current limited Load switch manufacturer part number TPS2051BD to allow on board 5V supply to power the VBUS. This load switch has an over current indication pin connected to I2C based GPIO expander on the EVM.

A common mode choke of manufacturer part number DLW21SZ900HQ2B is provided on USB Data lines for EMI/EMC reduction. Along with ESD Protection IC manufacturer part number TPD4S012DRYR to suppress any transient voltages.

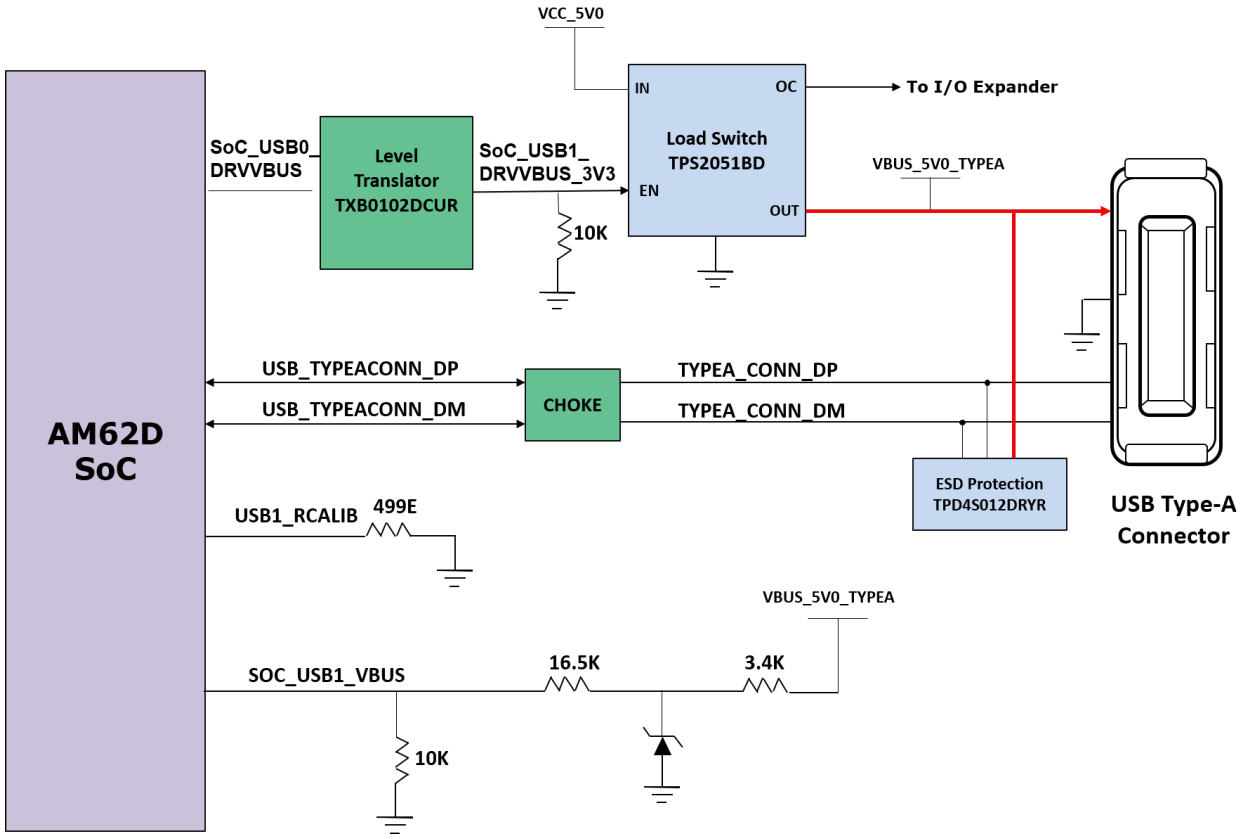


Figure 2-9. USB2.0 Type-A Interface block diagram

2.6.5.2 USB2.0 Type-C Interface

On the AM62D Audio EVM, USB2.0 Interface is offered through USB Type-C Connector J25 manufacturer part number 2012670005 which supports data rate up to 480Mbps. J25 can be used for data communication and also as a power connector sourcing supply to the EVM. It is configured as DRP port using PD controller TPS65988DHRSHR IC. So it can act as either a Host or Device. The role of the port depends on the type of the device getting connected on the connector and its ability to either sink or source. When the port is acting as DFP, it can source up to 5V @500mA.

USB2.0 Data lines DP and DM from J25 are provided with a choke and an ESD protection device. USB0_VBUS to the SoC is provided through a resistor divider network to support (5V-30V) VBUS operation.

A common mode choke of manufacturer part number DLW21SZ900HQ2B is provided on USB Data lines for EMI/EMC reduction. An ESD protection device of part number ESD122DMXR is included to dissipate ESD strikes on USB2.0 DP/DM signals. An ESD protection device of part number TPD1E01B04DPLT is included on CC signals and TVS2200DRVR IC is included on VBUS rail of Type-C Connector J25 to dissipate ESD strikes.

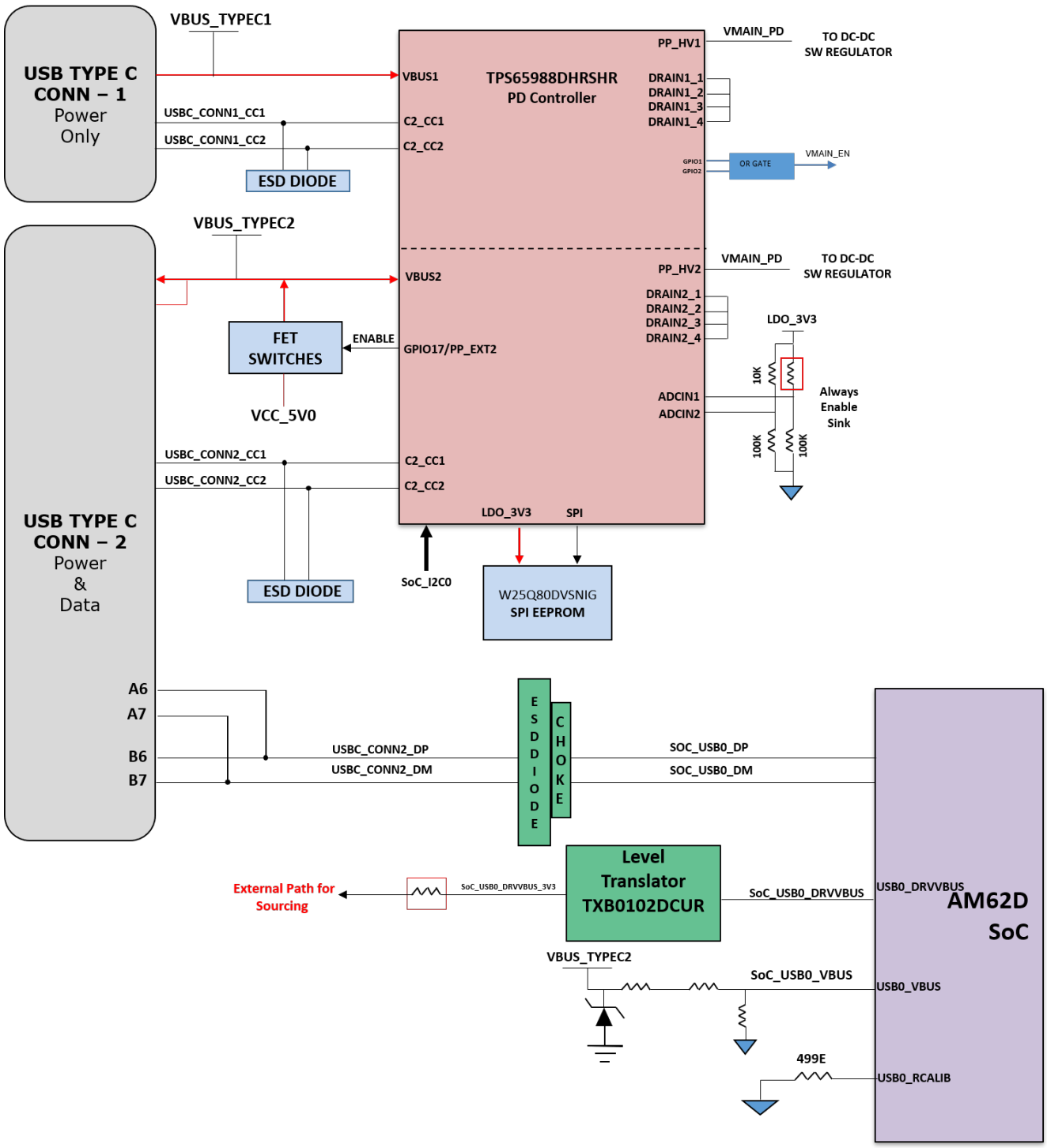


Figure 2-10. USB2.0 Type-C Interface Block Diagram

2.6.6 MCAN Interface

The AM62D Audio EVM is equipped with a dual MCAN Transceivers manufacturer part number TCAN3413DR that is connected to the MCAN0 and MCU_MCAN0 interface of the AM62D SoC. The MCAN Transceiver has two power inputs, VIO is the transceiver 1.8V system level shifting supply voltage and VCC is the transceiver 3.3V supply voltage. The SoC CAN data transmit data input is mapped to TXD of the transceiver and the CAN receive data output of the transceiver is mapped to the RXD of the SoC.

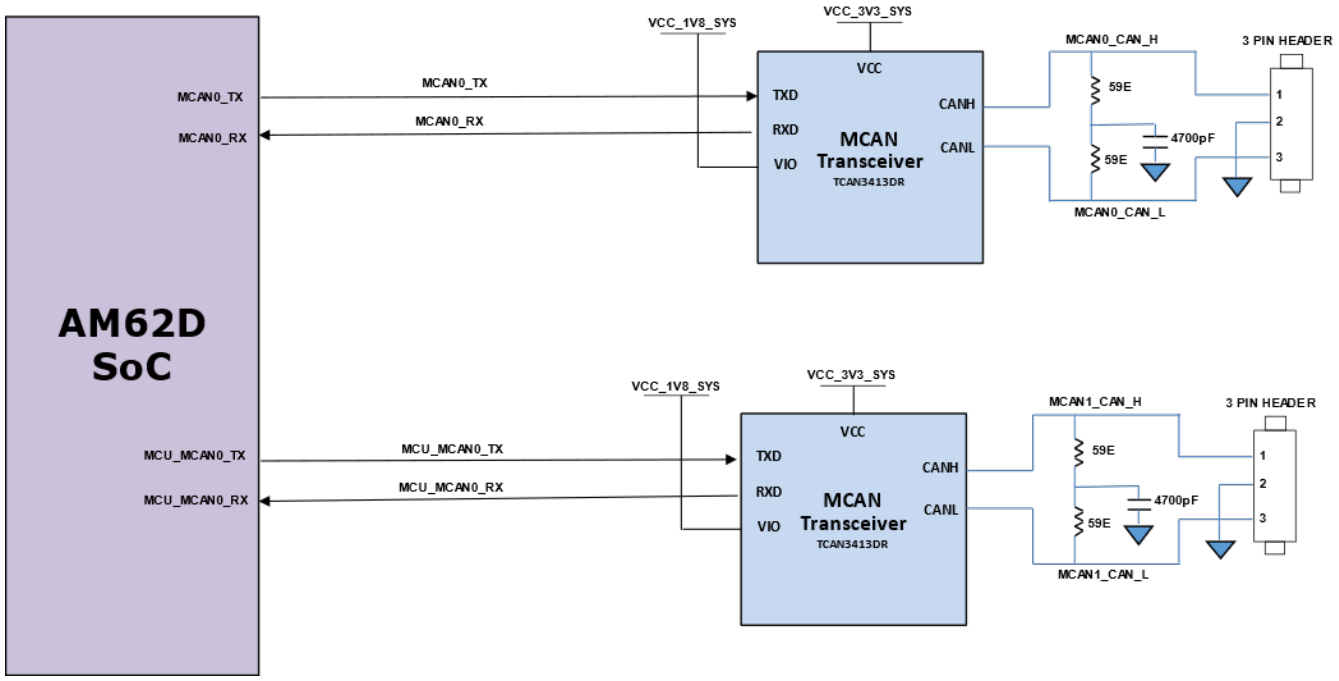


Figure 2-11. MCAN Block Diagram

The system has a 120Ω split termination on the CANH and CANL signals to improve EMI performance. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

The low-level and high-level CAN bus input output lines are terminated to a three-pin header.

2.6.7 Memory Interfaces

2.6.7.1 LPDDR4 Interface

The AM62D Audio EVM houses the dual-rank, dual-die 4GB, 32-bit wide LPDDR4 memory (MT53E1G32D2FW-046 IT:C) from Micron supporting data rates up to 3733MT/s. The LPDDR4 memory is placed optimally and routed to the DDR0 group of the SoC to support point-to-point communication.

The LPDDR4 memory requires 1.8V for its core supply, thus reducing power demand. The I/Os are supplied from a 1.1V supply output from the PMIC. LPDDR4 reset (Active low) controlled by the AM62D SoC is pulled down to set the default active state. The provision for mounting a pull up resistor is also provided.

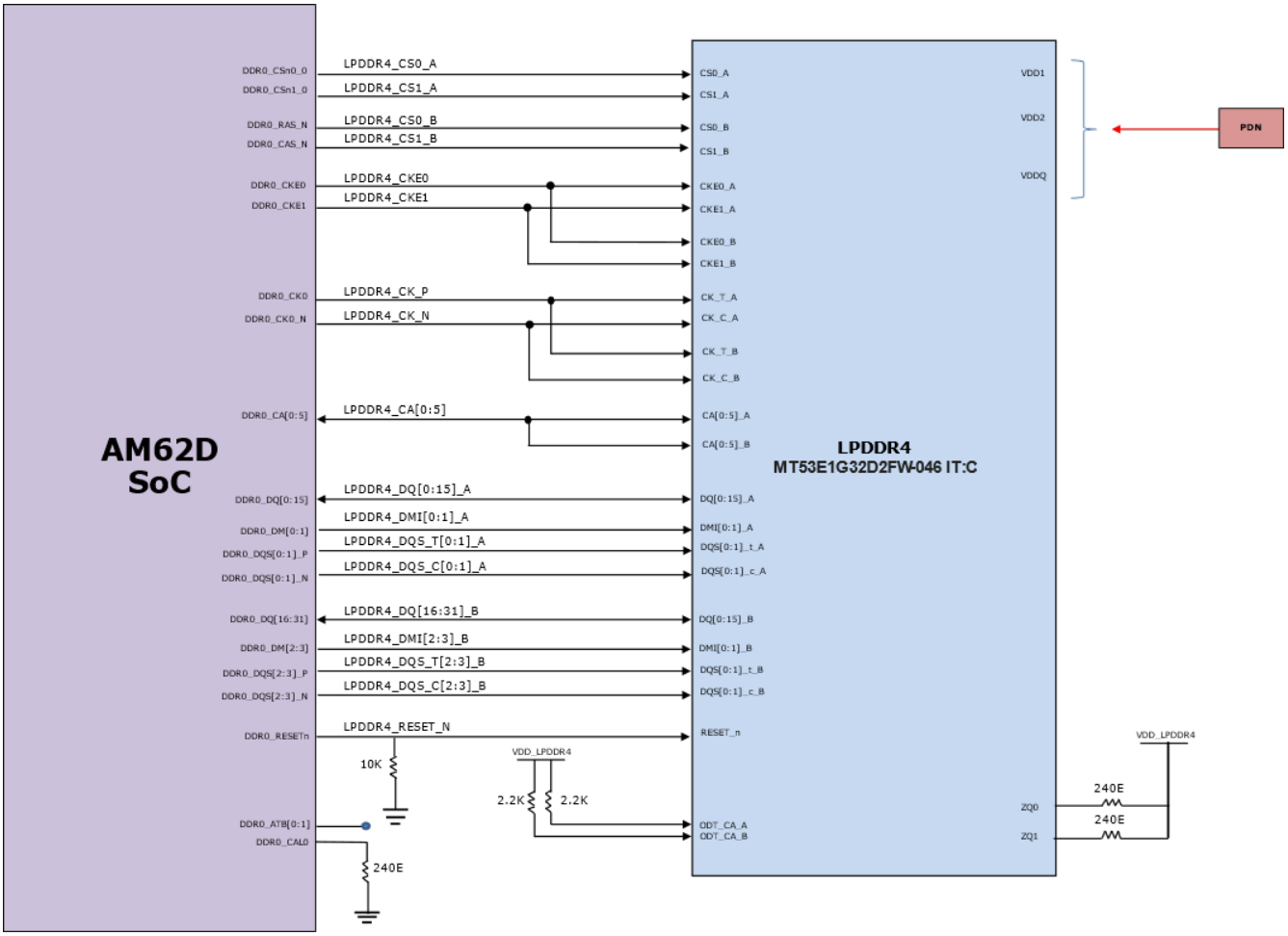


Figure 2-12. LPDDR4 Interface Block Diagram

2.6.7.2 Octal Serial Peripheral Interface (OSPI)

The AM62D Audio EVM board features a 512Mb OSPI memory device from Cypress part number S28HS512TGABHM010 which is connected to the OSPI0 of the AM62D SoC. The OSPI supports single and double data rates with clock speeds up to 200MBps SDR and 400MBps DDR (200MHz clock speed).

OSPI & QSPI implementation: 0Ω resistors are provided for DATA[7:0], DQS, INT# and CLK signals. External pull up resistors are provided on DATA[7:0] to prevent bus floating. The footprint for the OSPI memory also allows the installation of either a QSPI memory or an OSPI memory. The 0Ω series resistors provided for pins OSPI_DATA[4:7] can be removed if a QSPI Flash is to be mounted.

Reset: The reset for the OSPI flash is connected to a circuit that ANDs the RESETSTATz from the AM62D SoC with the signal GPIO_OSPI_RSTn from the SoC. A pull-up resistor is provided on GPIO_OSPI_RSTn to set the default active state.

Power: Both VCC and VCCQ pins of the OSPI Flash memory is supplied through an on board 1.8V system power. The OSPI I/O group is powered by the VDDSHV1 domain of SoC and is also connected to 1.8V system power.

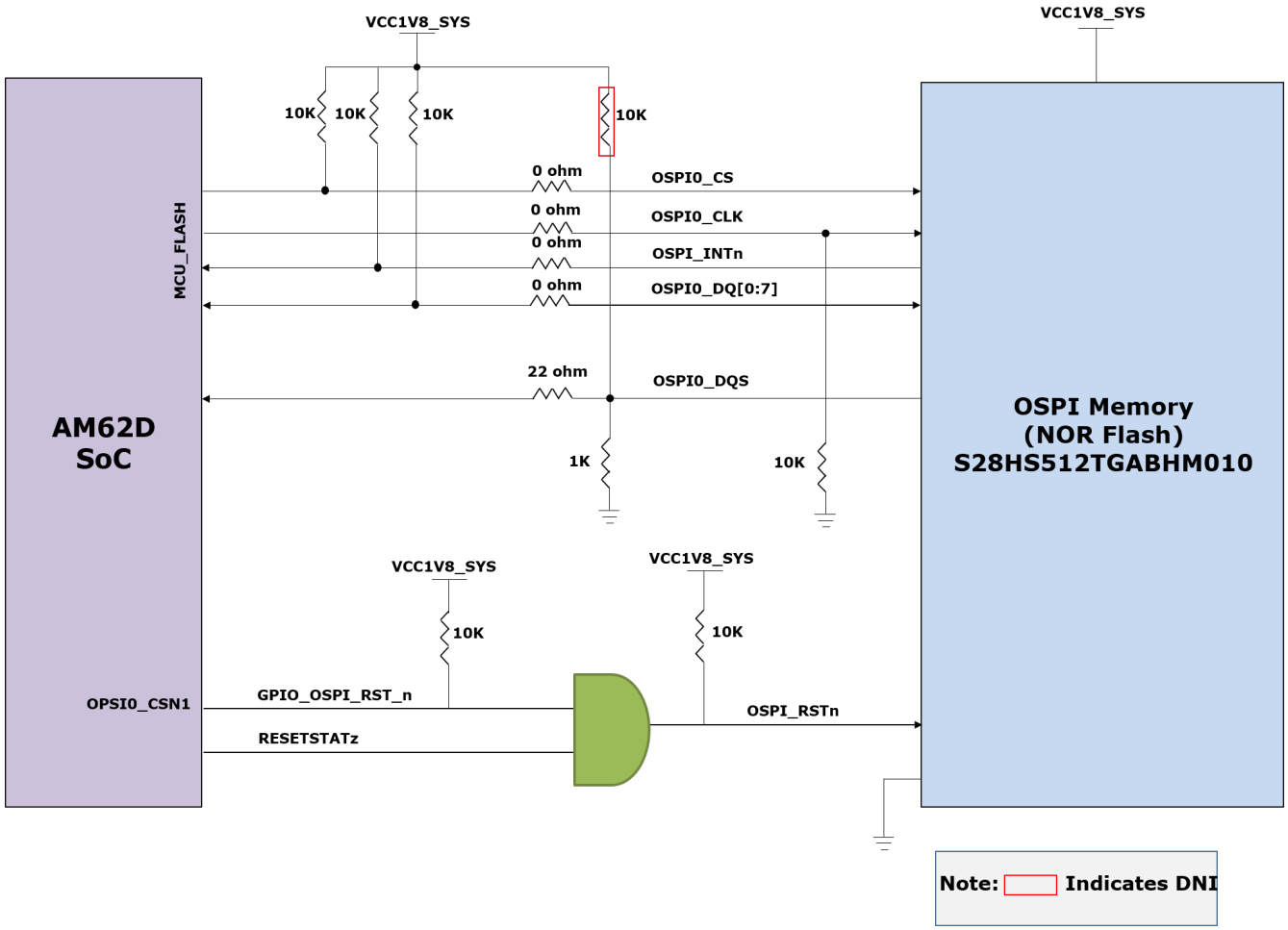


Figure 2-13. OSPI Block Diagram

2.6.7.3 MMC Interfaces

The AM62D SoC features three MMC ports (MMC0, MMC1 and MMC2). MMC0 is connected to eMMC, MMC1 is interfaced with a microSD Card connector and MMC2 is terminated to Audio Expansion Connector 1 for McASP1 Interface.

2.6.7.3.1 MMC0 - eMMC Interface

The EVM board contains 32GB of eMMC flash memory from Micron Part # MTFC32GBCAQTC connected to MMC0 port of the AM62D SoC.

The data bus from the flash memory is connected to 8 bits of the MMC0 interface supporting HS400 double data rates up to 200MHz. The Micron eMMC is a communication and mass data storage device that includes a Multimedia Card (MMC) interface and a NAND Flash component. Option to mount external pull up resistors are provided on DAT[7:1] to prevent bus floating and series resistor is provided for CLK signal close to SoC pad to match the characteristic impedance of PCB.

The eMMC device requires two power supplies, 3.3V for NAND memory and 1.8V for the eMMC interface. The MMC0 interface I/Os of the SoC is powered by the VDDSHV4 power domain, which is connected to 1.8V I/O supply.

The eMMC device requires active low reset from host. By default, the RST_n signal is temporarily disabled in the device. The host must set ECSD register byte 162, bits[1:0] to 0x1 to enable this functionality before the host can use it. The External Reset is provided by ANDing RESETSTATz from SoC and a GPIO from I/O Expander. A pull up is provided on GPIO pin to set the default active state.

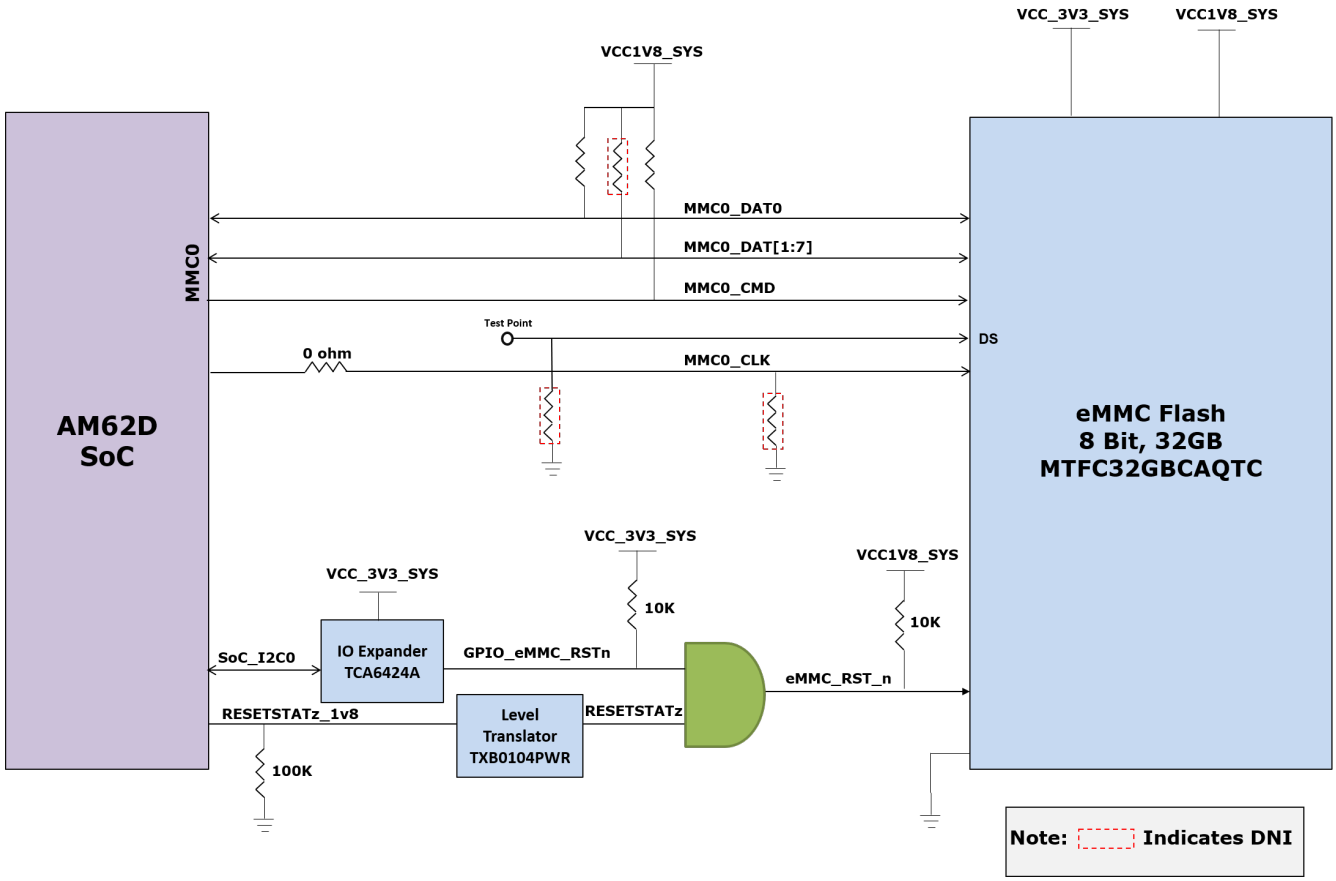


Figure 2-14. eMMC Interface Block Diagram

2.6.7.3.2 MMC1 - MicroSD Interface

The EVM board provides a microSD card Socket of manufacturer part number MEM2052-00-195-00-A connected to the MMC1 port of AM62D SoC. This supports this UHS1 operation is supported, including I/O operations at both 1.8V and 3.3V. The microSD card interface is set to operate in SD mode by default. For high-speed cards, the ROM Code of the SOC attempts to find the fastest speed that the card and controller can support and then have a transition to 1.8V through a VSEL_SD_SoC signal from the SoC

The microSD card connector power is provided using a load switch of manufacturer part number TPS22918DBVR, which is controlled by ANDing the output of RESETSTATz, PORz_OUT and a GPIO from I/O Expander.

An ESD protection device of part number TPD6E001RSE is provided for data, clock, and command signals. TPD6E001RSE is a line termination device with integrated TVS diodes providing system-level IEC 61000-4-2 ESD protection, ±8kV contact discharge and ±15kV air-gap discharge.

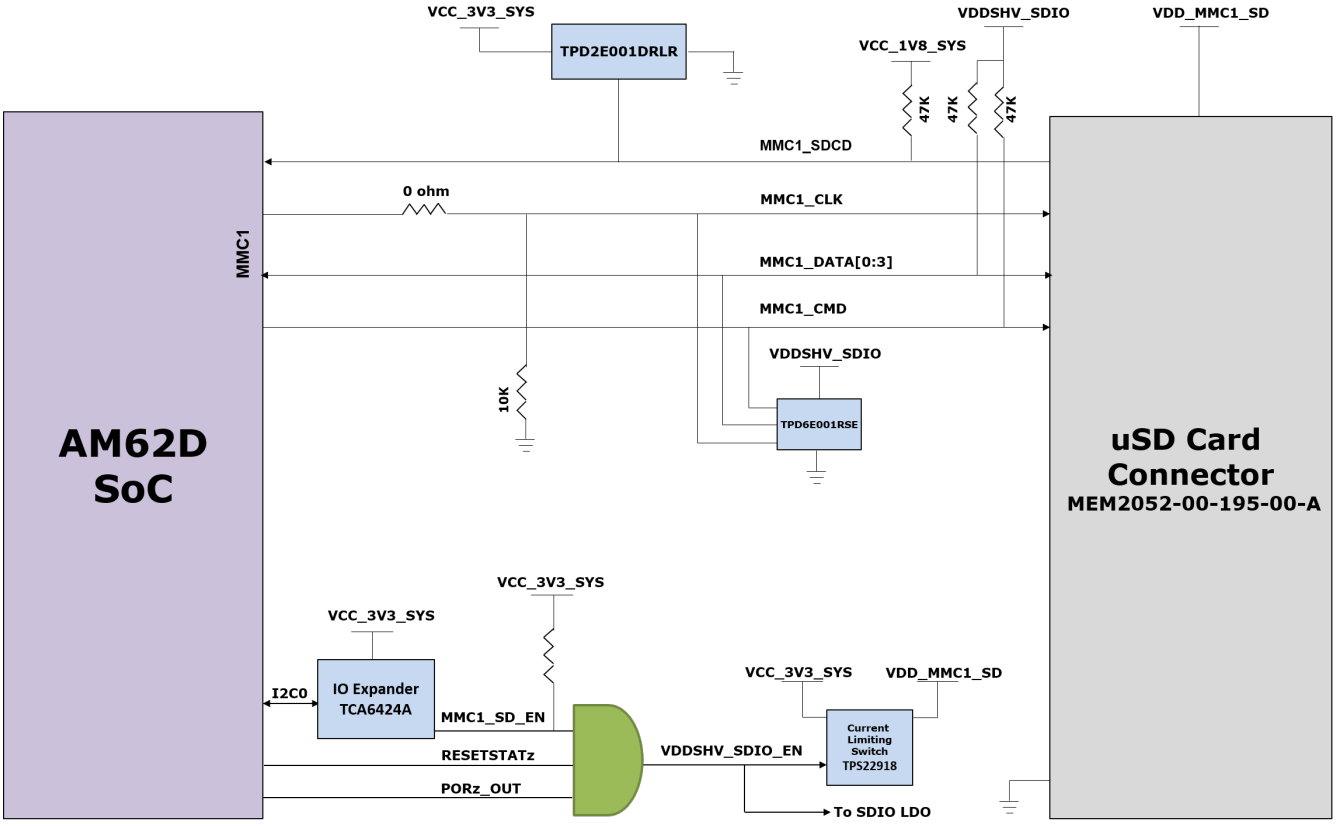


Figure 2-15. MicroSD Interface Block Diagram

2.6.7.4 Board ID EEPROM

The AM62D Audio EVM board can be identified remotely from its version and serial number data stored on the on-board EEPROM.

Board ID memory AT24C512C-MAHM-T from Microchip is interfaced to the I2C0 port of the SoC and is configured to respond to address 0x54 programmed with the header description. I2C address of the EEPROM can be modified by driving the A2 pin to high and A1, A0 pins to LOW. The first 259 bytes of memory are preprogrammed with identification information for each board. The remaining 65277 bytes are available to the user for data or code storage.

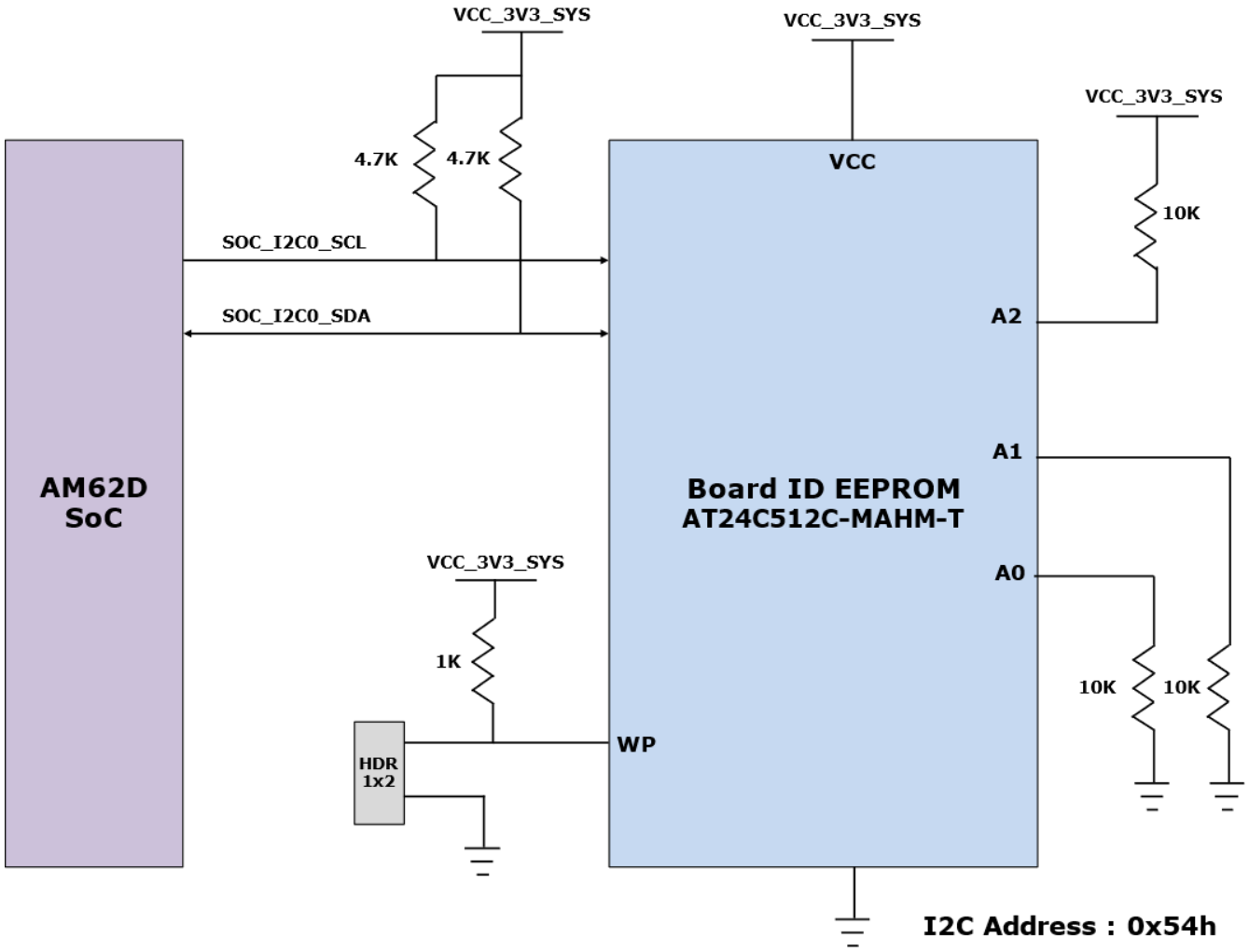


Figure 2-16. Board ID EEPROM Interface Block Diagram

2.6.8 Ethernet Interface

The AM62D EVM offers two Ethernet Ports of 1 Gigabit Speed for external Communication. Two channels of RGMII Gigabit Ethernet CPSW Port from AM62D SoC are connected to separate Ethernet Expansion connector manufacturer part number DF40C-50DP-0.4V.

This expansion connector providing flexibility of interfacing either to an Industrial Ethernet Daughter card or an Automotive Ethernet Daughter card. The Industrial PHY MDI lines are terminated to the RJ45 Jack while the Automotive PHY MDI lines terminate to an Auto grade MATEnet™ connector.

The CPSW_RGMII1 and CPSW_RGMII2 Ports share a common MDIO Bus to communicate with the external PHY Transceiver.

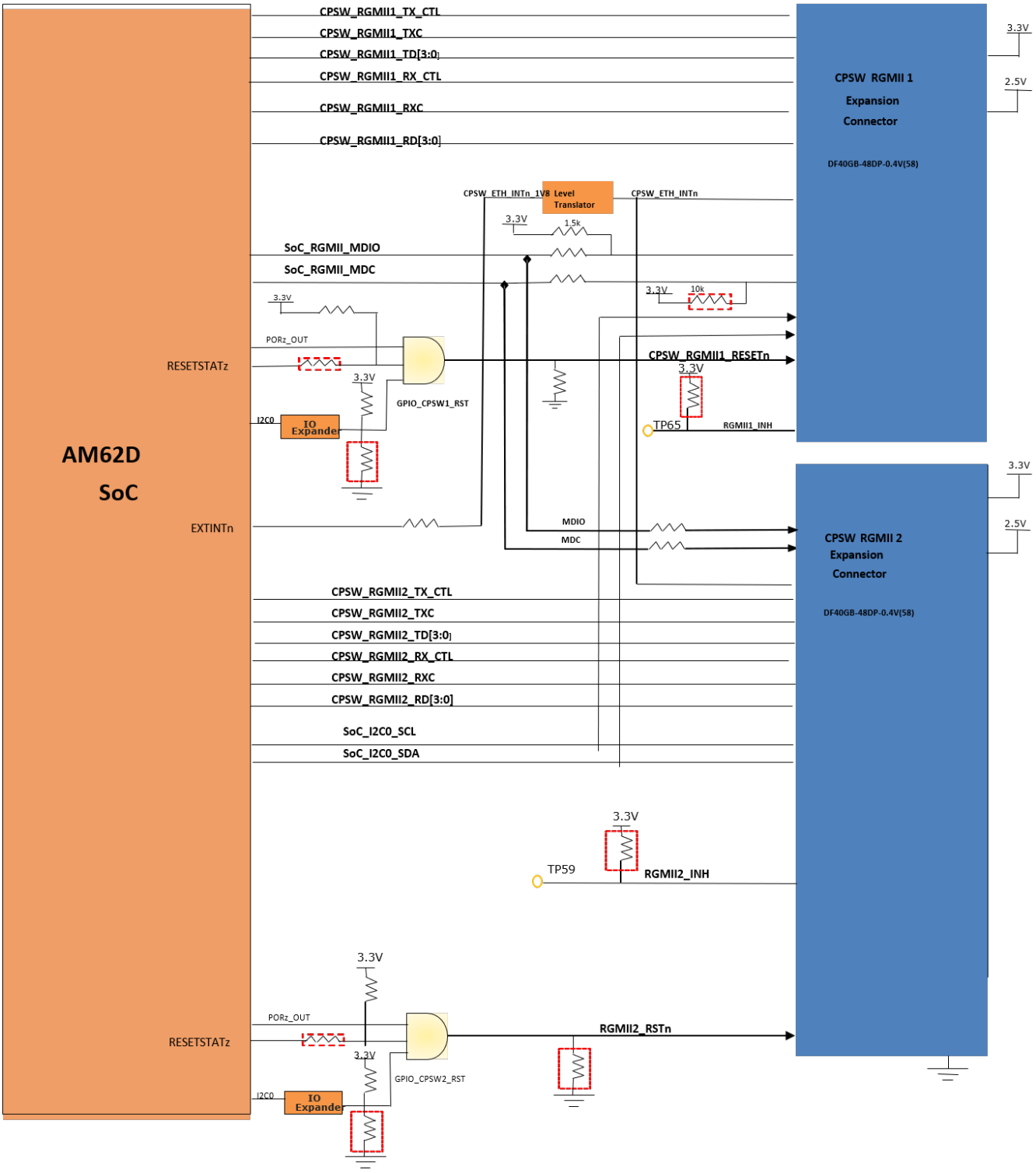


Figure 2-17. Ethernet Interface Block Diagram

2.6.9 CPSW Ethernet 1 and CPSW Ethernet 2

The CPSW_RGMII1 port and the CPSW_RGMII2 port of the AM62D SoC is terminated to a Expansion connector manufacturer part number DF40C-50DP-0.4V. This provides a flexibility of plugging in either an Industrial Grade Ethernet daughter card or an Automotive Grade Ethernet daughter card. The details of these are captured in the design documents of the respective cards.

Table 2-13 lists out the pinout for the Ethernet Expansion connector.

Table 2-13. CPSW Ethernet 1 & CPSW Ethernet 2 Expansion Connector Pinout

Pin No.	Signal	I/O Direction	Pin No.	Signal	I/O Direction
1	DGND	POWER	25	CPSW_RGMII_RD1	OUTPUT
2	EXT_VMON	POWER	26	RGMII_INH	OUTPUT
3	CPSW_RGMII_TXC	INPUT	27	CPSW_RGMII_RD2	OUTPUT
4	VDD_2V5	POWER	28	CPSW_RGMII_ETH_CLK	INPUT
5	DGND	POWER	29	CPSW_RGMII_RD3	OUTPUT
6	VDD_2V5	POWER	30	CPLD_CPSW_RGMII_CRS	OUTPUT
7	CPSW_RGMII_TD0	INPUT	31	DGND	POWER
8	DGND	POWER	32	DGND	POWER
9	CPSW_RGMII_TD1	INPUT	33	DGND	POWER
10	CPSW_RGMII_INTn	OUTPUT	34	DGND	POWER
11	CPSW_RGMII_TD2	INPUT	35	CPSW_RGMII_TX_EN	INPUT
12	RGMII_RSTn	INPUT	36	CPSW_RGMII_BRD_CONN_DET	OUTPUT
13	CPSW_RGMII_TD3	INPUT	37	I2C_ADDR0_A2	INPUT
14	CPLD_CPSW_RGMII_COL	OUTPUT	38	SYNC1_OUT_ETH1	POWER
15	DGND	POWER	39	RGMII_RX_ER	OUTPUT
16	DGND	POWER	40	SoC_I2C0_SCL	INPUT
17	DGND	POWER	41	DGND	POWER
18	DGND	POWER	42	SoC_I2C0_SDA	BIDIRECTIONAL
19	CPSW_RGMII_RXC	OUTPUT	43	RGMII_RX_LINK	OUTPUT
20	SoC_RGMII_MDC	INPUT	44	VCC_3V3_SYS	POWER
21	DGND	POWER	45	CPSW_RGMII_RX_DV	OUTPUT
22	SoC_RGMII_MDIO	BIDIRECTIONAL	46	VCC_3V3_SYS	POWER
23	CPSW_RGMII_RD0	OUTPUT	47	I2C_ADDR0_A0	INPUT
24	DGND	POWER	48	CPLD_CPSW_RGMII_BCLK	OUTPUT

2.6.10 GPIO Port Expander

Table 2-14. I/O Expander Signal Details

I/O Expander - 01			
Pin no	**Signal**	**Direction**	**Purpose**
P00	GPIO_CPSW2_RST	OUTPUT	CPSW Ethernet PHY-2 Reset Control GPIO
P01	GPIO_CPSW1_RST	OUTPUT	CPSW Ethernet PHY-1 Reset Control GPIO
P02	NC	-	
P03	MMC1_SD_EN	OUTPUT	SD Card Load Switch Enable
P04	VPP_EN	OUTPUT	SOC eFuse Voltage(VPP=1.8V) Regulator Enable
P05	GPIO_DIX_RST	OUTPUT	DIX4192 reset control GPIO
P06	IO_EXP_OPT_EN	OUTPUT	Optical Buffer Enable
P07	DIX_INT	INPUT	DIX4192 Interrupt signal
P10	GPIO_eMMC_RSTn	OUTPUT	eMMC Reset control GPIO
P11	CPLD2_DONE	INPUT	CPLD2 Programming Indication
P12	CPLD2_INTN	INPUT	CPLD 2 Interrupt signal
P13	CPLD1_DONE	INPUT	CPLD1 Programming Indication
P14	CPLD1_INTN	INPUT	CPLD 1 Interrupt signal
P15	USB_TYPEA_OC_INDICATION	INPUT	Type A Overcurrent Indication
P16	PCM1_INT	INPUT	PCM6240 Audio device 1 Interrupt signal

Table 2-14. I/O Expander Signal Details (continued)

I/O Expander - 01			
Pin no	**Signal**	**Direction**	**Purpose**
P17	PCM2_INT	INPUT	PCM6240 Audio device 2 Interrupt signal
P20	GPIO_PCM1_RST	OUTPUT	PCM6240 Audio device 1 reset control GPIO
P21	TEST_GPIO2	INPUT	TEST GPIO2 from Interrupt switch
P22	GPIO_PCM2_RST	OUTPUT	PCM6240 Audio device 2 reset control GPIO
P23	NC	-	
P24	IO_MCAN0_STB	OUTPUT	MCAN 0 STB Control
P25	IO_MCAN1_STB	OUTPUT	MCAN 1 STB Control
P26	PD_I2C_IRQ	INPUT	Interrupt Request from PD Controller
P27	IO_EXP_TEST_LED	OUTPUT	User Test _LED _Enable
Pin no	Signal	Direction	Device
P00	PCM6240_BUF_IO_EN	OUTPUT	PCM6240 Buffer enable
P01			
P02	CPLD1_JTAGENB	OUTPUT	CPLD 1 JTAG enable
P03	CPLD1_PROGRAMN	OUTPUT	CPLD 1 Programn Enable
P04	CPLD2_JTAGENB	OUTPUT	CPLD 2 JTAG enable
P05	CPLD2_PROGRAMN	OUTPUT	CPLD 2 Programn Enable
P06	NC		
P07	NC		
P10	CPLD1 TCK	OUTPUT	CPLD1_JTAG
P11	CPLD1 TMS	OUTPUT	
P12	CPLD1 TDI	OUTPUT	
P13	CPLD1 TDO	INPUT	
P14	CPLD2 TCK	OUTPUT	CPLD2_JTAG
P15	CPLD2 TMS	OUTPUT	
P16	CPLD2 TDI	OUTPUT	
P17	CPLD2 TDO	INPUT	

2.6.11 GPIO Mapping

Table 2-15 describes the detailed GPIO mapping of AM62D Low Power SoC with AM62D Audio EVM peripherals.

Table 2-15. Mapping of AM62D Low Power SoC with AM62D Low Power SK EVM peripherals

SL NO.	GPIO Description	GPIO Netname	Functionality	GPIO Used	Package Signal Name	Direction with Respect to Control	Default State	Active State	Voltage Domain on SoC Side	Voltage Rail Connected on SKEVM
1	Audio Expansion Connector 1	EXP1_GPIO0_1	GPIO	GPIO0_1	OSPI0_LBCLKO	NA	NA	NA	VDDSHV1	SoC_DVDD1V8
2	OSPI Interrupt	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSN1	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
3	Audio Expansion Connector 1	EXP1_GPIO0_13	GPIO	GPIO0_13	OSPI0_CSN2	NA	NA	NA	VDDSHV1	SoC_DVDD1V8
4	Audio Expansion Connector 1	EXP1_GPIO0_14	GPIO	GPIO0_14	OSPI0_CSN3	NA	NA	NA	VDDSHV1	SoC_DVDD1V8
5	Audio Expansion Connector 1	EXP1_GPIO0_31	GPIO	GPIO0_31	GPMC0_CLK	NA	NA	NA	VDDSHV1	SoC_DVDD1V8
6	Audio Expansion Connector 1	EXP1_GPIO0_32	GPIO	GPIO0_32	GPMC0_ADVN_ALE	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
7	MCASP Header	EXP1_GPIO0_33	GPIO	GPIO0_33	GPMC0_OEN_REN	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
8	Audio Expansion Connector 1									
9	MCASP Header	EXP1_GPIO0_34	GPIO	GPIO0_34	GPMC0_WEN	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
10	Audio Expansion Connector 1									

Table 2-15. Mapping of AM62D Low Power SoC with AM62D Low Power SK EVM peripherals (continued)

SL NO.	GPIO Description	GPIO Netname	Functionality	GPIO Used	Package Signal Name	Direction with Respect to Control	Default State	Active State	Voltage Domain on SoC Side	Voltage Rail Connected on SKEVM
11	Audio Expansion Connector 1	EXP1_GPIO0_35	GPIO	GPIO0_35	GPMC0_BEON_CLE	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
12	Audio Expansion Connector 1	EXP1_GPIO0_37	GPIO	GPIO0_37	GPMC0_WAIT0	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
13	Audio Expansion Connector 2	EXP1_GPIO0_45	GPIO	GPIO0_45	VOUT0_DATA0	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
14	Audio Expansion Connector 2	EXP1_GPIO0_46	GPIO	GPIO0_46	VOUT0_DATA1	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
15	Audio Expansion Connector 2	EXP1_GPIO0_47	GPIO	GPIO0_47	VOUT0_DATA2	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
16	Audio Expansion Connector 2	EXP1_GPIO0_48	GPIO	GPIO0_48	VOUT0_DATA3	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
17	Audio Expansion Connector 2	EXP1_GPIO0_55	GPIO	GPIO0_55	VOUT0_DATA10	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
18	Audio Expansion Connector 2	EXP1_GPIO0_56	GPIO	GPIO0_56	VOUT0_DATA11	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
19	Audio Expansion Connector 2	EXP1_GPIO0_57	GPIO	GPIO0_57	VOUT0_DATA12	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
20	Audio Expansion Connector 2	EXP1_GPIO0_58	GPIO	GPIO0_58	VOUT0_DATA13	NA	NA	NA	VDDSHV3	SoC_DVDD1V8
21	User test LED control signal	SOC_GPIO1_49	ENABLE	GPIO0_49	MMC1_SDWP	INPUT	LOW	HIGH	VDDSHV5	SoC_DVDD1V8
22	SD Card I/O Voltage Selection	VSEL_SD_SOC	SELECTION	GPIO0_59	VOUT0_DATA14	OUTPUT	NA	NA	VDDSHV2	SoC_DVDD3V3
23	Low power mode enable	PMIC_LPM_EN0	ENABLE	MCU_GPIO0_22	PMIC_LPM_EN0	OUTPUT	HIGH	LOW	VDDSHV_CANUART	CAN_IO_3V3
24	PMIC Interrupt	PMIC_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
25	MCU Interrupt	MCU_INTn	INTERRUPT	MCU_GPIO0_23	WKUP_CLKOUT0	INPUT	HIGH	LOW	WKUP_MCU	SoC_DVDD3V3
IO EXPANDER - 01										
1	GPIO_CPSW2_RST	RGMII2_RST	ENABLE	IO EXPANDER-P00		OUTPUT	HIGH	LOW		VCC_3V3_SYS
2	GPIO_CPSW1_RST	RGMII1_RST	ENABLE	IO EXPANDER-P01		OUTPUT	HIGH	LOW		VCC_3V3_SYS
3	PCM/EXP2_SEL	PCM/ EXP2_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P02		OUTPUT	HIGH	-		VCC_3V3_SYS
4	MMC1_SD_EN	MMC1_SD_EN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
5	VPP_EN	VPP_EN	ENABLE	IO EXPANDER-P04		OUTPUT	NA	HIGH		VCC_3V3_SYS
6	GPIO_DIX_RST	DIX4192_RST	ENABLE	IO EXPANDER-P05		OUTPUT	HIGH	LOW		VCC_3V3_SYS
7	IO_EXP_OPT_EN	OPT_BUF_EN	ENABLE	IO EXPANDER-P06		OUTPUT	HIGH	LOW		VCC_3V3_SYS
8	DIX_INT	DIX4192_INT	INTERRUPT	IO EXPANDER-P07		INPUT	HIGH	LOW		VCC_3V3_SYS
9	GPIO_eMMC_RSTn	eMMC_RST	ENABLE	IO EXPANDER-P10		OUTPUT	HIGH	LOW		VCC_3V3_SYS
10	CPLD2_DONE	CPLD2_DONE	ENABLE	IO EXPANDER-P11		INPUT	HIGH	LOW		VCC_3V3_SYS
11	CPLD2_INTN	CPLD2_INT	INTERRUPT	IO EXPANDER-P12		INPUT	HIGH	LOW		VCC_3V3_SYS
12	CPLD1_DONE	CPLD1_DONE	ENABLE	IO EXPANDER-P13		INPUT	HIGH	LOW		VCC_3V3_SYS
13	CPLD1_INTN	CPLD1_INT	INTERRUPT	IO EXPANDER-P14		INPUT	HIGH	LOW		VCC_3V3_SYS
14	USB Type-A overcurrent indicator	USB_TYPEA_OC_INDICATION	INTERRUPT	IO EXPANDER-P14		INPUT	HIGH	LOW		VCC_3V3_SYS
15	PCM1_INT	PCM6240_INT	INTERRUPT	IO EXPANDER-P16		INPUT	NA	NA		VCC_3V3_SYS
16	PCM2_INT	PCM6240_INT	INTERRUPT	IO EXPANDER-P17		INPUT	HIGH	LOW		VCC_3V3_SYS
17	GPIO_PCM1_RST	HDMI_INTn	INTERRUPT	IO EXPANDER-P20		INPUT	HIGH	LOW		VCC_3V3_SYS
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO	IO EXPANDER-P21		NA	HIGH	NA		VCC_3V3_SYS
19	GPIO_PCM2_RST	PCM6240_RST	ENABLE	IO EXPANDER-P22		OUTPUT	HIGH	LOW		VCC_3V3_SYS

Table 2-15. Mapping of AM62D Low Power SoC with AM62D Low Power SK EVM peripherals (continued)

SL NO.	GPIO Description	GPIO Netname	Functionality	GPIO Used	Package Signal Name	Direction with Respect to Control	Default State	Active State	Voltage Domain on SoC Side	Voltage Rail Connected on SKEVM
20	CPLD/EXP2_SEL	CPLD/ EXP2_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P23		OUTPUT	HIGH	-		VCC_3V3_SYS
21	IO_MCAN0_STB	MCAN_STB	ENABLE	IO EXPANDER-P24		OUTPUT	HIGH	LOW		VCC_3V3_SYS
22	IO_MCAN1_STB	MCAN_STB	ENABLE	IO EXPANDER-P25		OUTPUT	HIGH	LOW		VCC_3V3_SYS
23	Power Delivery I2C Interrupt Request	PD_I2C_IRQ	ENABLE	IO EXPANDER-P26		OUTPUT	HIGH	LOW		VCC_3V3_SYS
24	User Test LED 2	IO_EXP_TEST_ LED	GPIO	IO EXPANDER-P27		OUTPUT	LOW	HIGH		VCC_3V3_SYS
IO EXPANDER - 02										
1	PCM6240_BUF_IO_EN	PCM6240_Buffe r_EN	ENABLE	IO EXPANDER-P00		OUTPUT	HIGH	-		VCC_3V3_SYS
2	NC	NC	NC	IO EXPANDER-P01		NC	NC			NC
3	CPLD1_JTAGENB	CPLD1_JTAGE NB	ENABLE	IO EXPANDER-P02		OUTPUT	LOW	-		VCC_3V3_SYS
4	CPLD1_PROGRAMN	CPLD1_PROGR AMN	INTERRUPT	IO EXPANDER-P03		OUTPUT	HIGH	-		VCC_3V3_SYS
5	CPLD2_JTAGENB	CPLD2_JTAGE NB	ENABLE	IO EXPANDER-P04		OUTPUT	LOW	-		VCC_3V3_SYS
6	CPLD2_PROGRAMN	CPLD2_PROGR AMN	INTERRUPT	IO EXPANDER-P05		OUTPUT	HIGH	-		VCC_3V3_SYS
7	NC	NC	NC	IO EXPANDER-P06		NC	NC			NC
8	NC	NC	NC	IO EXPANDER-P07		NC	NC			NC
9	CPLD1_TCK	CPLD1_TCK	CPLD1_JTAG	IO EXPANDER-P10		OUTPUT	NA	-		VCC_3V3_SYS
10	CPLD1_TMS	CPLD1_TMS	CPLD1_JTAG	IO EXPANDER-P11		OUTPUT	HIGH	-		VCC_3V3_SYS
11	CPLD1_TDI	CPLD1_TDI	CPLD1_JTAG	IO EXPANDER-P12		OUTPUT	NA	-		VCC_3V3_SYS
12	CPLD1_TDO	CPLD1_TDO	CPLD1_JTAG	IO EXPANDER-P13		INPUT	NA	-		VCC_3V3_SYS
13	CPLD2_TCK	CPLD2_TCK	CPLD2_JTAG	IO EXPANDER-P14		OUTPUT	NA	-		VCC_3V3_SYS
14	CPLD2_TMS	CPLD2_TMS	CPLD2_JTAG	IO EXPANDER-P14		OUTPUT	HIGH	-		VCC_3V3_SYS
15	CPLD2_TDI	CPLD2_TDI	CPLD2_JTAG	IO EXPANDER-P16		OUTPUT	NA	-		VCC_3V3_SYS
16	CPLD2_TDO	CPLD2_TDO	CPLD2_JTAG	IO EXPANDER-P17		INPUT	NA	-		VCC_3V3_SYS

2.7 Power

2.7.1 Power Input

Both Type-C Connectors (VBUS and CC lines) are connected to a Dual PD controller manufacturer part number TPS65988. The TPS65988 is a stand-alone USB Type-C and Power Delivery (PD) controller providing cable plug and orientation detection for two USB Type-C Connectors. Upon cable detection, the TPS65988 communicates on the CC wire using the USB PD protocol. When cable detection and USB PD negotiation are complete, the TPS65988 enables the appropriate power path. The two internal power paths of TPS65988 are configured as sink paths for the two Type-C ports and an external FET path is provided for Type-C CONN 2 to source 5V when acting as DFP. The external FET path is controlled by GPIO17/PP_EXT2 of the PD controller along with a resistor option to also enable using USB0 DRVVBUS from AM62D SoC. TPS65988 PD controller can provide an output of 3A (15V max) through CC negotiation. The VBUS pins from both the Type-C connectors are connected to the VBUS pins of the PD controller. The output of the PD GPIO1 and GPIO2 are used for negotiation if the power is >= 15W. This logic enables the load switch TPS22810 for VMAIN supply. This VMAIN which is supplied to on board Buck-Boost and Buck regulators to generate fixed 5V and 3.3V supply for the EVM board.

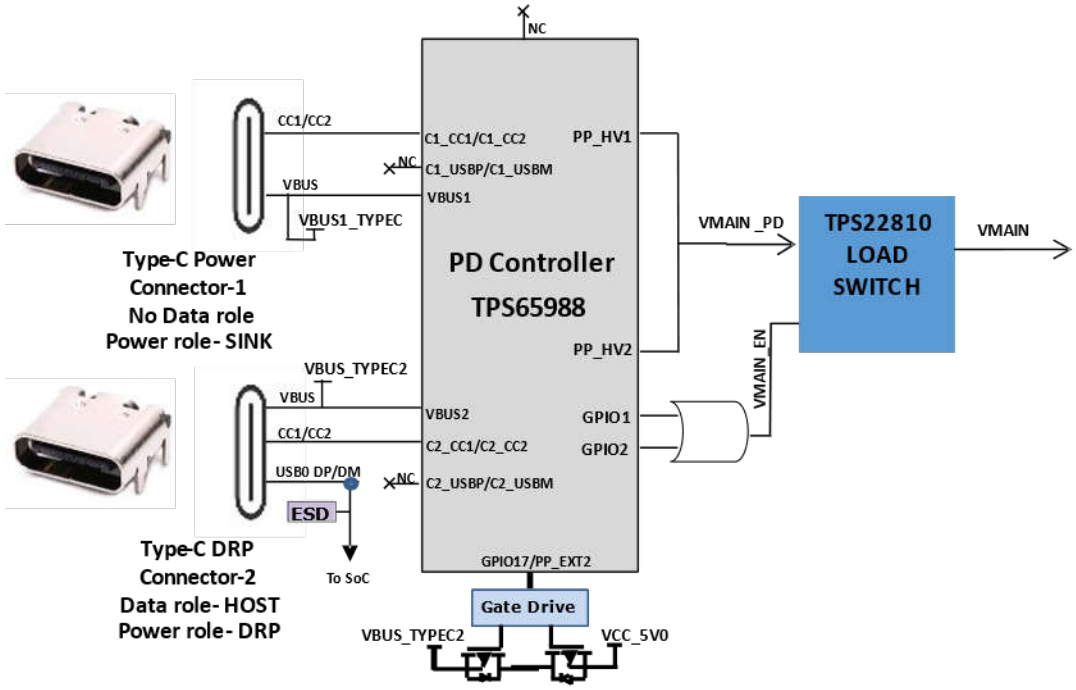


Figure 2-18. Power Input Block Diagram

2.7.2 Power Supply

The AM62D Audio EVM utilizes an array of DC-DC converters to supply the various memories, clocks, SoC and other components on the board with the necessary voltage and the power required.

Figure 2-19 shows the various discrete regulators, PMIC and LDOs used to generate power rails and the current consumption of each peripheral on the AM62D Audio EVM board.

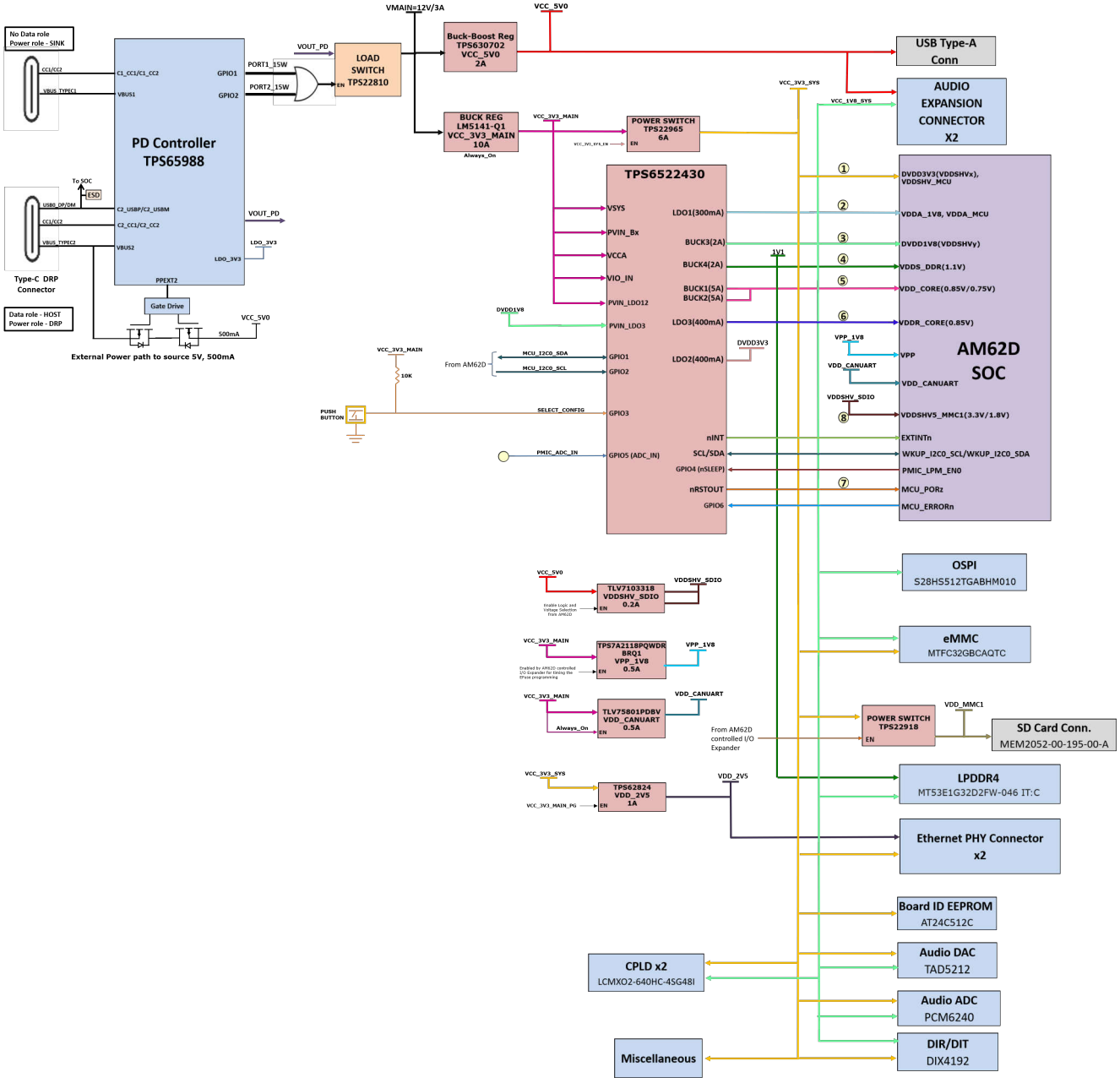


Figure 2-19. Power Architecture

The following sections describe the power distribution network topology that supplies the EVM board, supporting components and reference voltages.

The AM62D Audio EVM board includes a power solution based on discrete power supply components. The initial stage of the power supply will be VBUS voltage from either of the two USB Type-C connectors J24 and J25. USB Type-C Dual PD controller of manufacturer part number TPS65988DHRSHR is used for negotiation of the required power to the system. The GPIO1 and GPIO2 of the PD are used for negotiation if the power is ≥ 15W.This logic enables the load switch for VMAIN supply .

Buck-Boost controller TPS630702RNMR and Buck converter LM5141-Q1 are used for the generation of 5V and 3.3V respectively and the input to the regulators is the PD output. These 3.3V and 5V are the primary voltages for the AM62D Audio EVM Board power resources. The 3.3V supply generated from the Buck regulator LM5141-Q1 is the input supply to the PMIC, various SOC regulators and LDOs. The 5V supply generated from

the Buck Boost regulator TPS630702RNMR is used for powering the on-board peripherals. Discrete regulators and LDOs used on Board are:

- TPS62824DMQR – To generate VDD_2V5 rail for PHY and DDR peripherals
- PTPS6522430RAHRQ1 (PMIC) – To generate various SoC and Peripheral supplies
- TLV75801PDBVT LDO – VDD_CANUART power of SoC
- TPS7A2118PQWDRBRQ1 – To generate VPP_1V8 for SoC
- TPS79601 LDO - XDS110 On board emulator
- TPS73533 LDO - FT4232 USB-to-UART Bridge

2.7.3 Power Sequencing

Figure 2-20 shows the Power Up and Power Down sequence of the AM62D SoC power supplies

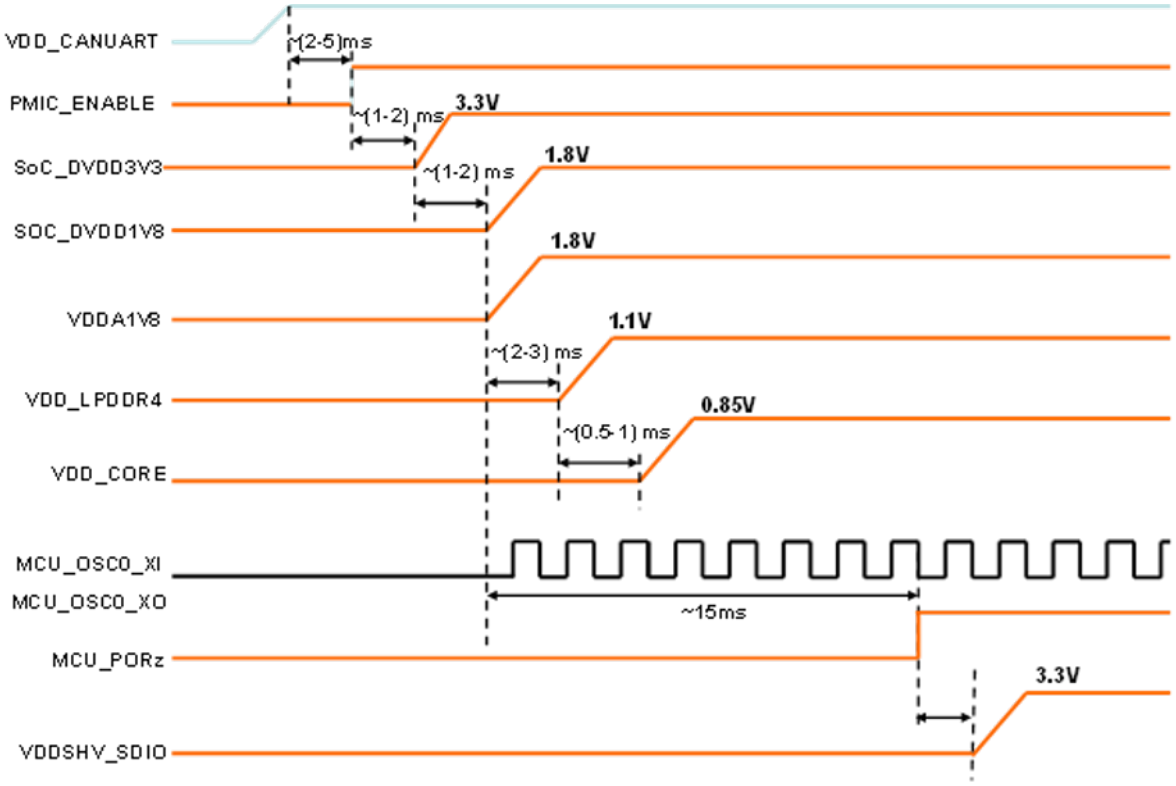


Figure 2-20. Power Sequence

2.7.4 AM62D SOC Power

The Core voltage of the AM62D SoC can be 0.75V or 0.85V based on the PMIC Configuration and on the power optimization requirement. By Default the PMIC is configured to supply VDD_CORE to 0.75V, it can be changed to 0.85V by changing the PMIC Configuration register. Current monitors are provided on all of the SoC Power rails.

The SoC has different I/O groups. Each I/O group is powered by specific power supplies as listed in Table 2-16.

Table 2-16. SoC Power Supply

Sl.No	Power Supply	SoC Supply Rails	I/O Power Group	Voltage
1	VDD_CORE	VDDA_CORE_USB	USB	0.75/ 0.85
		VDDA_CORE_CSI	CSI	
		VDD_CANUART	CANUART	
		VDD_CORE	CORE	
2	VDDR_CORE	VDDR_CORE	CORE	0.75

Table 2-16. SoC Power Supply (continued)

Sl.No	Power Supply	SoC Supply Rails	I/O Power Group	Voltage
3	VDDA_1V8	VDDA_1V8_CSIRX	CSI	1.8
		VDDA_1V8_USB	USB	
		VDDA_1V8_MCU	MCU GENERAL	
		VDDA_1V8_OSCO	OSCO	
		VDDA_PLL[0:4]		
4	VDD_LPDDR4	VDDS_DDR	DDR0	1.1
		VDDS_DDR_C		
5	CAN_IO_3V3	VDDSHV_CANUART	CANUART	3.3
6	VPP_1V8	VPP_1V8		1.8
7	SoC_VDDSHV5_SDIO	VDDSHV5	MMC1	3.3/ 1.8
8	SOC_DVDD1V8	VDDSHV1	OSPI	1.8
		VDDSHV4	MMC0	
		VDDSHV6	MMC2	
		VMON_1P8_SOC		
9	SOC_DVDD3V3	VDDSHV0	GENERAL	1.8
		VDDSHV3	GPMC	
		VDDSHV2	RGMII	3.3
		VDDSHV_MCU	MCU GENERAL	
		VMON_3P3_SOC		
		VDDA_3P3_USB	USB	

2.7.5 Current Monitoring

INA228 power monitor devices are used to monitor current and voltage of various power rails of AM62D processor. The INA228 interfaces to the AM62D through I2C interface (SoC_I2C0). Four terminal, high precision shunt resistors are provided to measure load current.

Table 2-17. INA I2C Device Address

Source	Supply Net	Device Address	Value of the Shunt Connected to the Supply Rail
VCC_CORE	VDD_CORE	0x40	1mΩ± 1%
VCC_0V85	VDDR_CORE	0x41	10mΩ± 1%
VCC_3V3_SYS	SoC_DVDD3V3	0x4C	10mΩ± 1%
VCC1V8_SYS	SoC_DVDD1V8	0x45	10mΩ± 1%
VDDA1V8	VDDA_1V8	0x4D	10mΩ± 1%
VCC1V1	VDD_LPDDR4	E1 revision: 0x47 E2 revision: 0x44	1mΩ± 1%

2.8 Clocking

The Clock architecture of the AM62D Audio EVM is shown in Figure 2-21.

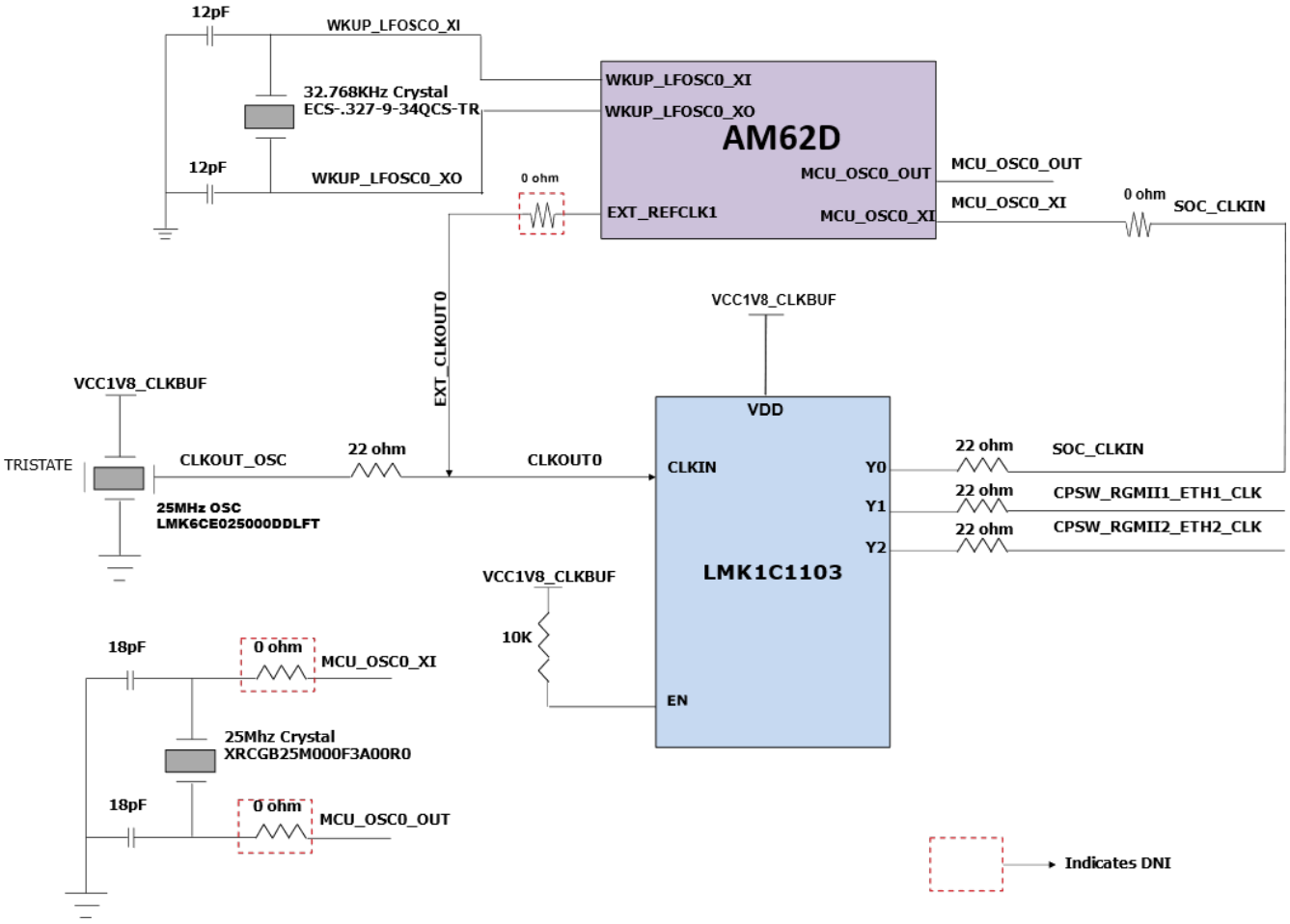


Figure 2-21. Clock Architecture

A clock generator of part number LMK1C1103PWR is used to drive the 25MHz clock to the SoC & two Ethernet PHYs. LMK1C1103PWR is a 1:3 LVCMOS clock buffer, which takes the 25MHz crystal/LVCMOS reference input and provides four 25MHz LVCMOS clock outputs. The source for the clock buffer shall be either the CLKOUT0 pin from the SoC or a 25MHz oscillator, the selection of which is made using a set of resistors. By default, an oscillator is used as an input to the clock buffer on the AM62D Audio EVM. Output Y1 and Y2 of the clock buffer are used as reference clock inputs for the two Gigabit Ethernet PHYs.

There is one external crystal (32.768KHz) attached to the AM62D SoC to provide clock to its WKUP domain.

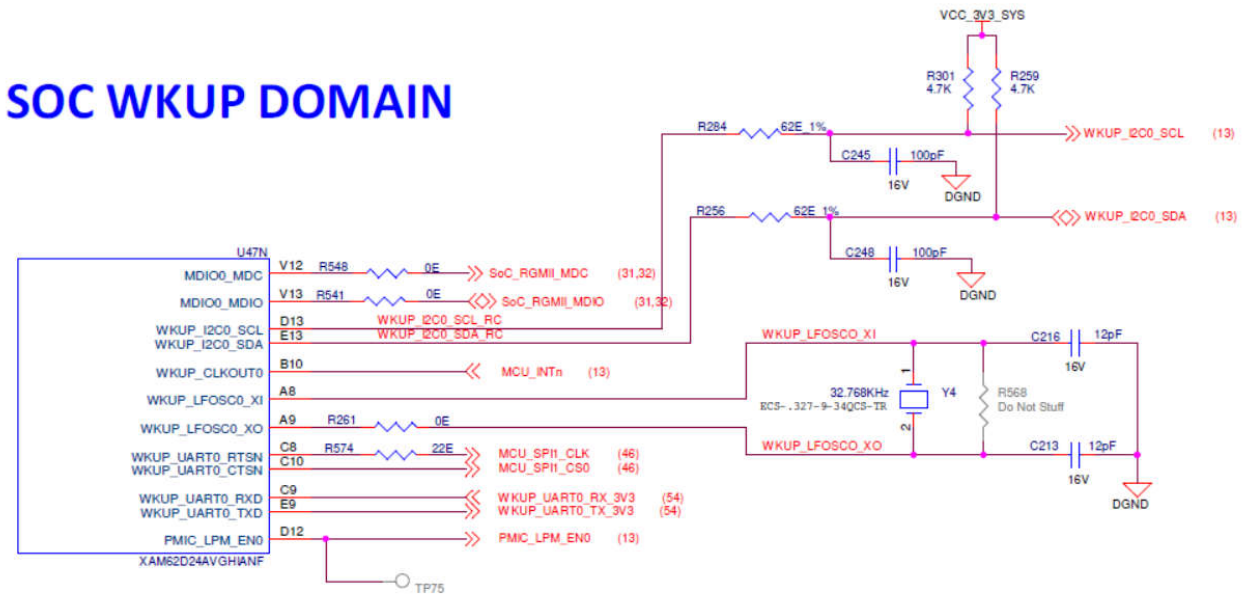


Figure 2-22. SoC WKUP Domain Clock

2.8.1 Peripheral Ref Clock

Clock inputs required for peripherals such as XDS110, FT4232, CDCE Clock generator, SI5351B-B-GM are generated locally using separate crystals or oscillators. Crystals or Oscillators used to provide the reference clocks to the EVM peripherals are shown in Table 2-18.

Table 2-18. Clock Table

Peripheral	Manufacturer Part Number	Description	Frequency
XDS110 emulator (Y5)	XRCGB16M000FXN01R0	CRY 16.000MHz 8pF SMD	16.000MHz
FT4232 Bridge (Y6)	445I23D12M00000	CRY12.000MHz 18pF SMD	12.000MHz
CDCE Clock generator (Y1)	ABMM-24.576MHZ-B2-T	CRY 24.576MHz 18pF SMD	24.576MHz
SI5351B-B-GM (Y2)	ABM8-27.000MHZ-10-1-U-T	CRY 27.000MHz SMD	27MHz

2.9 Reset

The Reset Architecture of AM62D Audio EVM is shown in Figure 2-23. The SoC has the following resets:

- RESETSTATz is the MAIN domain warm reset status output
- PORz_OUT is the MAIN domain power ON reset status output
- RESET_REQz is the MAIN domain warm reset input
- MCU_PORz is the MCU domain power ON/ Cold Reset input
- MCU_RESETSTATz is the MCU domain warm reset status output

Upon Power on Reset, all peripheral devices connected to the MAIN domain get reset by RESETSTATz.

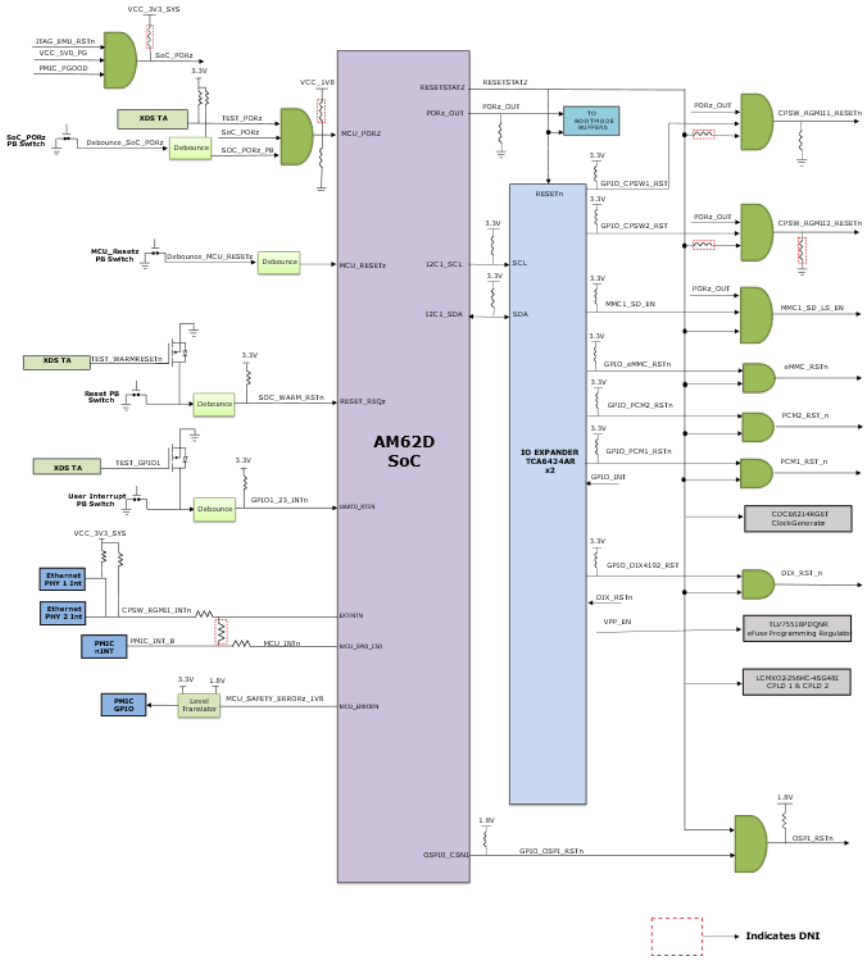


Figure 2-23. Reset Block Diagram

2.10 CPLD Mapping

The AM62D Audio EVM supports 2x CPLDs manufacturer part number LCMXO2-640HC-1SG32I for the Mux/ Demux of low frequency audio clocks (<30MHz) and the CPLDs are programmed in buffer logic for audio signals from the SoC to On-board Audio peripheral devices.

The CPLD requires 3.3V for Core (VCC) and VCCIO0 and 1.8V for other I/Os (VCCIO1, VCCIO2 & VCCIO3). 2x 1x6 HDR manufacturer part number 61300611121 are installed for JTAG programming.

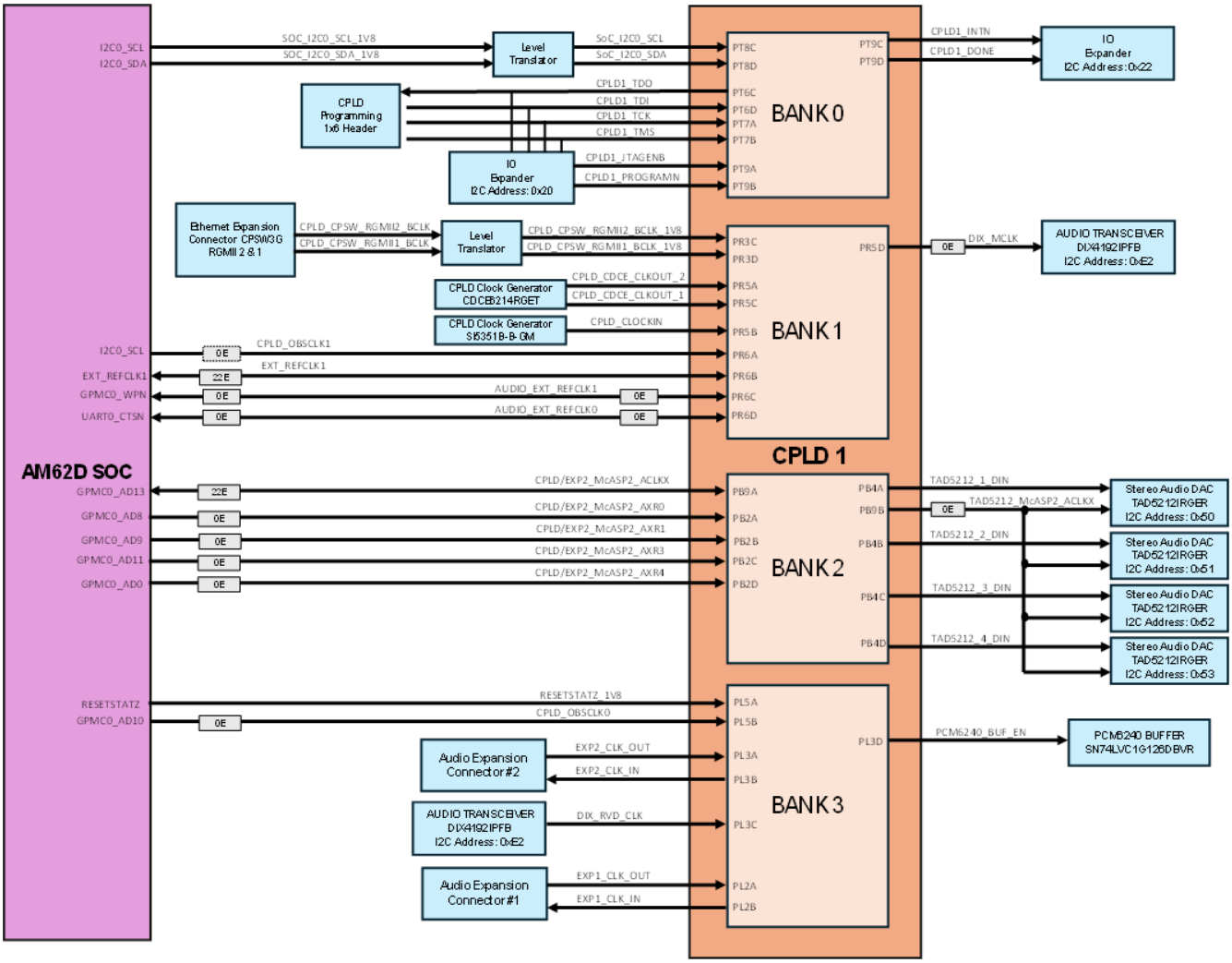


Figure 2-24. CPLD1 Block Diagram

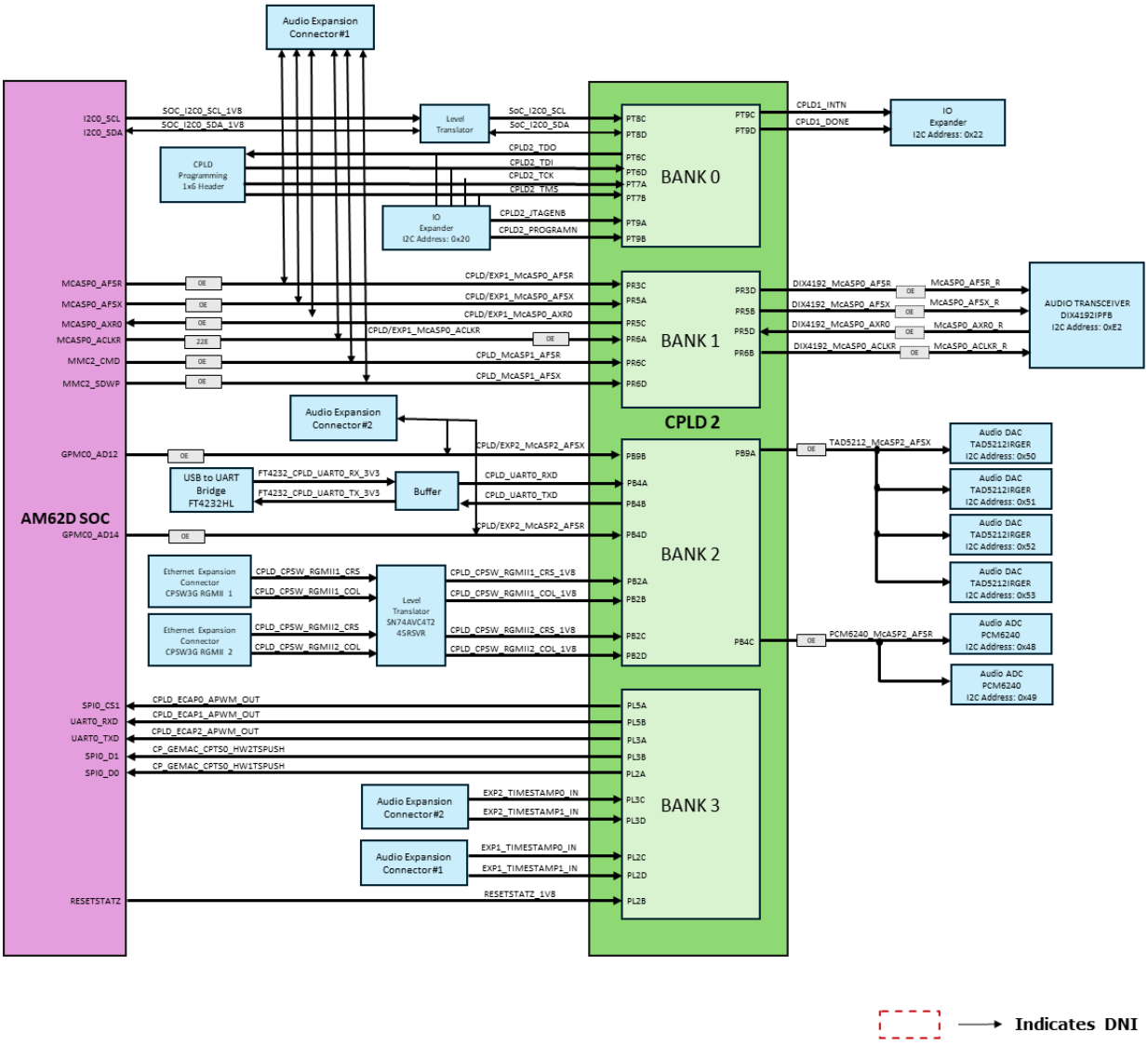
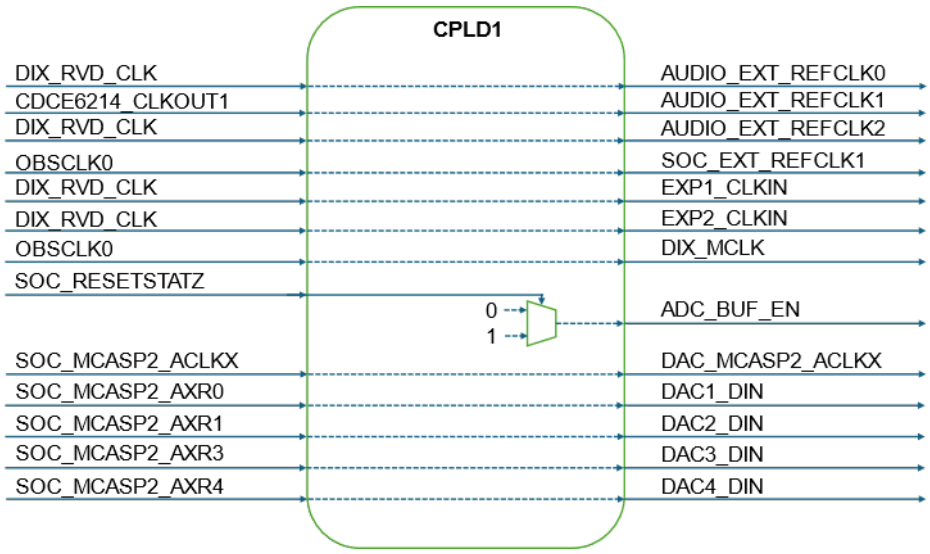


Figure 2-25. CPLD2 Block Diagram

The current AM62D Audio EVM has CPLD mapping as shown below.

CPLD1 Configuration E1



CPLD1 Configuration E1

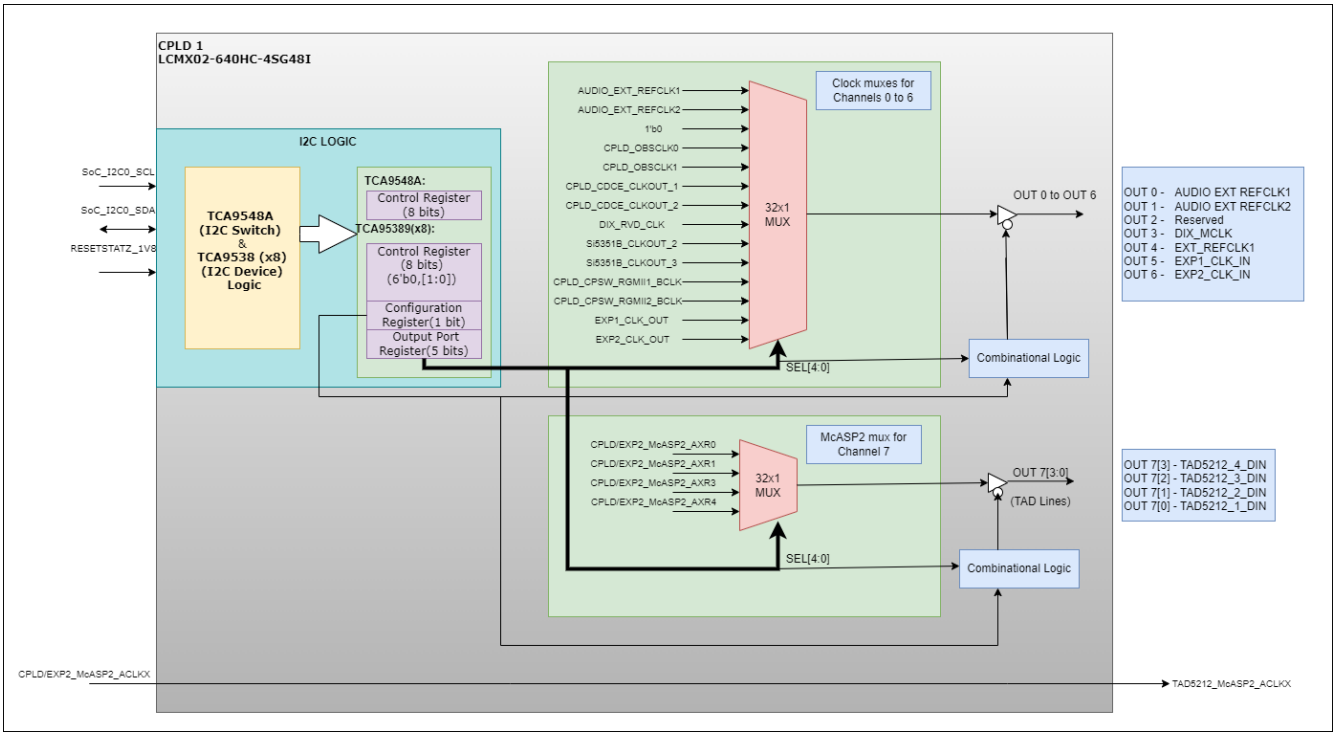
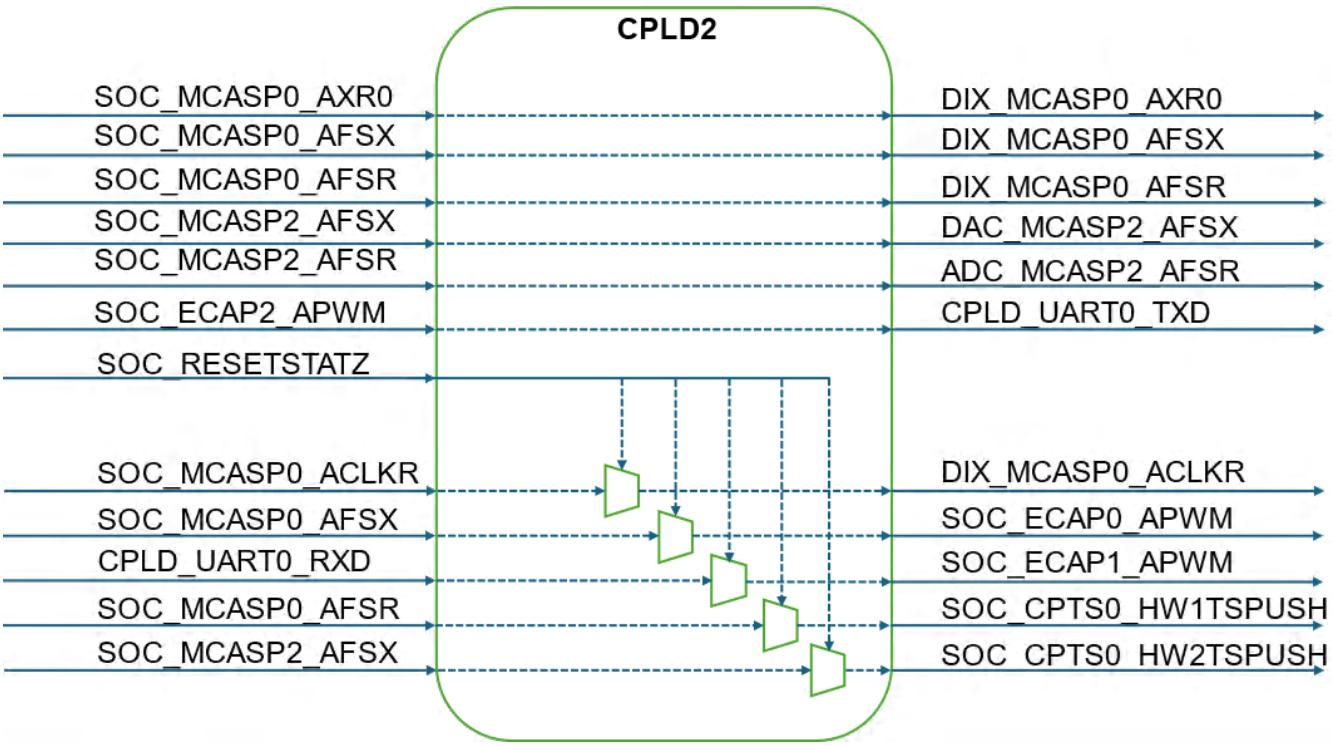


Figure 2-26. CPLD1 Pin Mapping

CPLD2 Configuration E1



CPLD2 Configuration E1

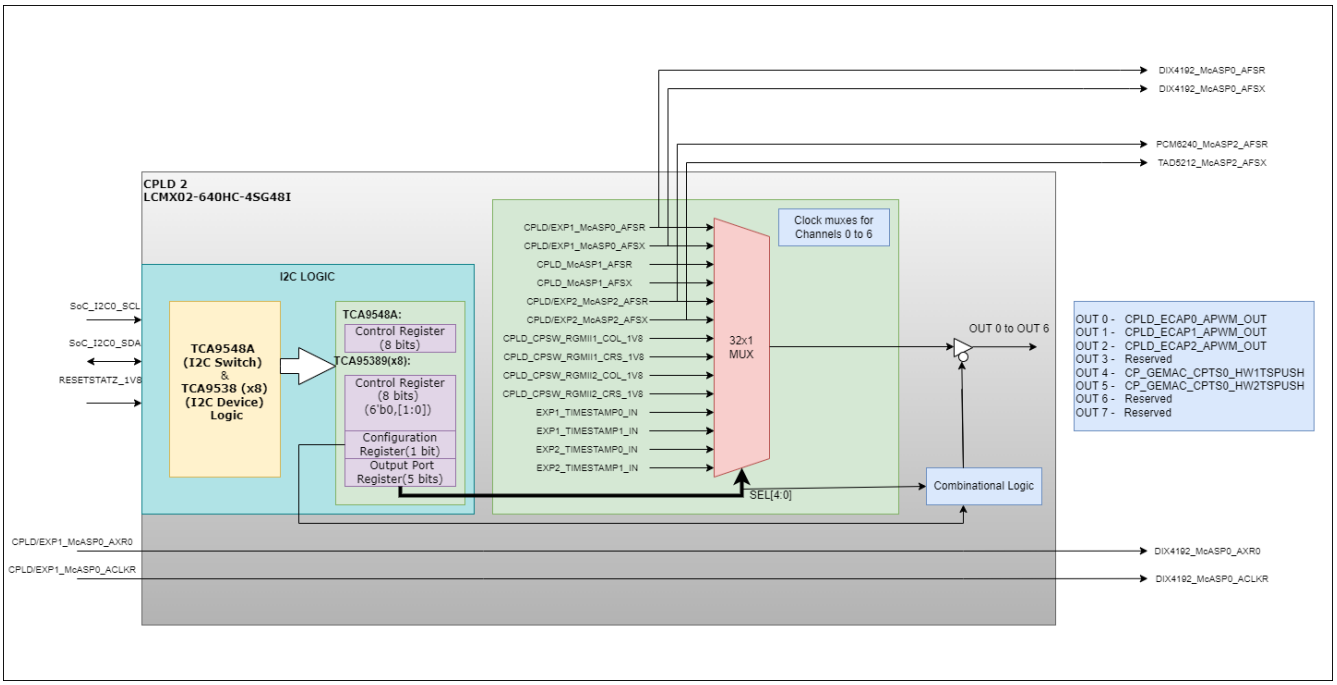


Figure 2-27. CPLD2 Pin Mapping

2.11 Audio Expansion Connectors (Headers)

The AM62D Audio EVM features two Audio expansion connectors, and each connector comprises of 80 pins.

2.11.1 Audio Expansion Connector 1

The AM62D Audio EVM comprises of two shielded audio expansion connectors manufacturer part number QSE-040-01-L-D-A. These two symmetric connectors will be placed at fixed distance at specified locations on left and right sides of the EVM.

The following interfaces and IOs are included on Audio Expansion Connector 1:

- 1x SPI: SPI0 with 1 CS
- 1x I2C: SoC_I2C2
- 1x UART: UART5
- 2x PWM: EHRPWM0_A, EHRPWM1_B
- 1x CLK: CLKOUT0
- 2x Timer_IO
- 1x CLK: CLK_IN from CPLD
- 2x daughtercard reference timestamp signals.
- 2x McASP: McASP0 and McASP 1
- 10x GPI0: GPIOs from main domain
- 5V and 1.8V supply (current limited to 150mA and 250mA)

Signals routed to Audio Expansion Connector 1 are listed in Table 2-19.

Table 2-19. Audio Expansion Connector 1 Pinout

PIN	SOC BALL	NET NAME
1	F18	PORz_OUT_1V8
2	-	VCC_5V0
3	C11	MCU_TIMER_IO1_1V8
4	-	VCC_5V0
5	D7	MCU_TIMER_IO2_1V8
6	-	VCC_5V0
7	-	GND
8	-	GND
9	-	EXP1_TIMESTAMP0_IN
10	-	VCC1V8_SYS
11	-	EXP1_TIMESTAMP1_IN
12	-	VCC1V8_SYS
13	-	NC
14	-	NC
15	-	GND
16	-	GND
17	B13	MCU_SPI0_CLK_1V8
18	M22	EXP1_I2C2_SCL
19	A15	MCU_SPI0_D0_1V8
20	M20	EXP1_I2C2_SDA
21	B12	MCU_SPI0_D1_1V8
22	-	GND
23	E11	MCU_SPI0_CS0_1V8
24	K22	EXP1_GPIO0_1
25	-	GND
26	-	GND
27	E20	EXP1_McASP1_AXR0
28	F20	EXP1_McASP1_AXR2
29	F21	EXP1_McASP1_AXR1
30	G21	EXP1_McASP1_AXR3

Table 2-19. Audio Expansion Connector 1 Pinout (continued)

PIN	SOC BALL	NET NAME
31	-	GND
32	K20	EXP1_GPIO0_13
33	CPLD	EXP1_CLK_IN
34	G20	EXP1_GPIO0_14
35	-	GND
36	-	GND
37	F22	EXP1_McASP1_ACLKX
38	N22	EXP1_GPIO0_31
39	E21	CPLD_McASP1_AFSX
40	L18	EXP1_GPIO0_32
41	G22	CPLD_McASP1_AFSR
42	L17	EXP1_GPIO0_33
43	H22	EXP1_McASP1_ACLKR
44	K19	EXP1_GPIO0_34
45	-	GND
46	-	GND
47	-	EXP1_CLK_OUT
48	-	NC
49	-	GND
50	-	GND
51	R18	EXP1_GPIO0_37
52	L19	EXP1_GPIO0_35
53	R17	EXP1_GPIO0_38
54	-	NC
55	-	NC
56	-	NC
57	-	GND
58	-	GND
59	-	NC
60	V21	UART5_TXD
61	-	NC
62	V22	UART5_RXD
63	-	NC
64	-	NC
65	-	GND
66	-	GND
67	-	CPLD/EXP1_McASP0_AXR0
68	-	NC
69	B18	EXP1_McASP0_AXR1
70	-	NC
71	B19	EXP1_McASP0_AXR2
72	-	NC
73	C19	EXP1_McASP0_AXR3
74	-	NC
75	-	GND
76	-	GND
77	A19	EXP1_McASP0_ACLKX

Table 2-19. Audio Expansion Connector 1 Pinout (continued)

PIN	SOC BALL	NET NAME
78	A21	CPLD/EXP1_McASP0_ACLKR
79	A20	CPLD/EXP1_McASP0_AFSX
80	B21	CPLD/EXP1_McASP0_AFSR

2.11.2 Audio Expansion Connector 2

Following interfaces and IOs are included on Audio Expansion connector 2:

- 1x SPI : SPI1 with 2 CS
- 1x I2C: SoC_I2C1
- 1x UART: UART6
- 2x PWM: EHRPWM0_A, EHRPWM1_A
- 1x CLK: CLKOUT0
- 1x CLK: CLK_IN from CPLD
- 1xTimer_IO
- 2x daughtercard reference timestamp signals.
- 1x McASP : McASP2_AFSR, AFSX, ACLKR, ACLKX with 15 Serializers
- 8x GPI0: GPIOs from MAIN domain
- 5V and 1.8V supply (current limited to 150mA and 25mA)

Signals routed to Audio Expansion connector 2 are listed in Table 2-20.

Table 2-20. Audio Expansion Connector 2 Pinout

PIN	SOC BALL	NET NAME
1	F18	PORz_OUT_1V8
2	-	VCC_5V0
3	D16	EXP2_EHRPWM0_A
4	-	VCC_5V0
5	A17	EXP2_EHRPWM1_A
6	-	VCC_5V0
7	-	GND
8	-	GND
9	-	EXP2_TIMESTAMP0_IN
10	-	VCC1V8_SYS
11	-	EXP2_TIMESTAMP1_IN
12	-	VCC1V8_SYS
13	-	NC
14	-	NC
15	-	GND
16	-	GND
17	C8	MCU_SPI1_CLK_1V8
18	C17	SoC_I2C1_SCL
19	B11	MCU_SPI1_D0_1V8
20	E17	SoC_I2C1_SDA
21	D10	MCU_SPI1_D1_1V8
22	-	GND
23	C10	MCU_SPI1_CS0_1V8
24	B9	EXP2_MCU_SPI1_CS2_1V8
25	-	GND
26	-	GND
27	P22	CPLD/EXP2_McASP2_AXR0

Table 2-20. Audio Expansion Connector 2 Pinout (continued)

PIN	SOC BALL	NET NAME
28	R22	CPLD/EXP2_McASP2_AXR3
29	R19	CPLD/EXP2_McASP2_AXR1
30	N21	CPLD/EXP2_McASP2_AXR4
31	-	GND
32	N20	EXP2_McASP2_AXR5
33	CPLD	EXP2_CLK_IN
34	N19	EXP2_McASP2_AXR6
35	-	GND
36	-	GND
37	R21	CPLD/EXP2_McASP2_ACLKX
38	N18	EXP2_McASP2_AXR7
39	T22	CPLD/EXP2_McASP2_AFSX
40	N17	EXP2_McASP2_AXR8
41	T20	CPLD/EXP2_McASP2_AFSR
42	U22	EXP2_GPIO0_45
43	T21	CPLD/EXP2_McASP2_ACLKR
44	U21	EXP2_GPIO0_46
45	-	GND
46	-	GND
47	-	EXP2_CLK_OUT
48	-	NC
49	-	GND
50	-	GND
51	U20	EXP2_GPIO0_47
52	C15	TIMER_IO7
53	U19	EXP2_GPIO0_48
54	-	NC
55	-	NC
56	-	NC
57	-	GND
58	-	GND
59	-	NC
60	V18	UART6_TXD
61	-	NC
62	V19	UART6_RXD
63	-	NC
64	-	NC
65	-	GND
66	-	GND
67	P18	EXP2_McASP2_AXR9
68	K18	EXP2_McASP2_AXR13
69	P19	EXP2_McASP2_AXR10
70	M19	CPLD/EXP2_McASP2_AXR14
71	P21	EXP2_McASP2_AXR11
72	M21	CPLD/EXP2_McASP2_AXR15
73	M18	EXP2_McASP2_AXR12
74	-	NC

Table 2-20. Audio Expansion Connector 2 Pinout (continued)

PIN	SOC BALL	NET NAME
75	-	GND
76	-	GND
77	W22	EXP2_GPIO0_55
78	W20	EXP2_GPIO0_57
79	W21	EXP2_GPIO0_56
80	W19	EXP2_GPIO0_58

2.12 Interrupt

The AM62D Audio EVM supports two interrupts for providing Reset input and User Interrupt to the processor. The interrupt are push buttons placed on the Top side of the Board and are listed in Table 2-21.

Table 2-21. EVM Push Buttons

Sl #	Push Buttons	Signal	Function
1	SW4	SoC_WARM_RESETZ	MAIN domain Warm Reset input
2	SW5	GPIO_MCU	Generates interrupt on GPIO1_23 (UART0_RTSn)

2.13 I2C Address Mapping

There are four I2C interfaces used in EVM board:

- SoC_I2C0 Interface: SoC I2C[0] is connected to Board ID EEPROM, USB PD controller, PCM6240 (x2), TAD5212 (x4), CDCE621, DIX4192, SIL5351B, DAC53002, Current Monitors (x6), Temperature Sensors (x2), CPLD (x2), CPSW Expansion Connector (x2) and GPIO Port Expander (x2).
- SoC I2C1 Interface: SoC I2C[1] is connected to Audio Expansion Connector 2 (AEC 2).
- SoC I2C2 Interface: SoC I2C[2] is connected to Audio Expansion Connector 1 (AEC 1).
- MCU I2C0 & WKUP_I2C0 Interface: MCU I2C[0] and WKUP_I2C[0] is connected PMIC.

Figure 2-28 depicts the I2C tree, and Table 2-22 provides the complete I2C address mapping details present on the AM62D Audio EVM.

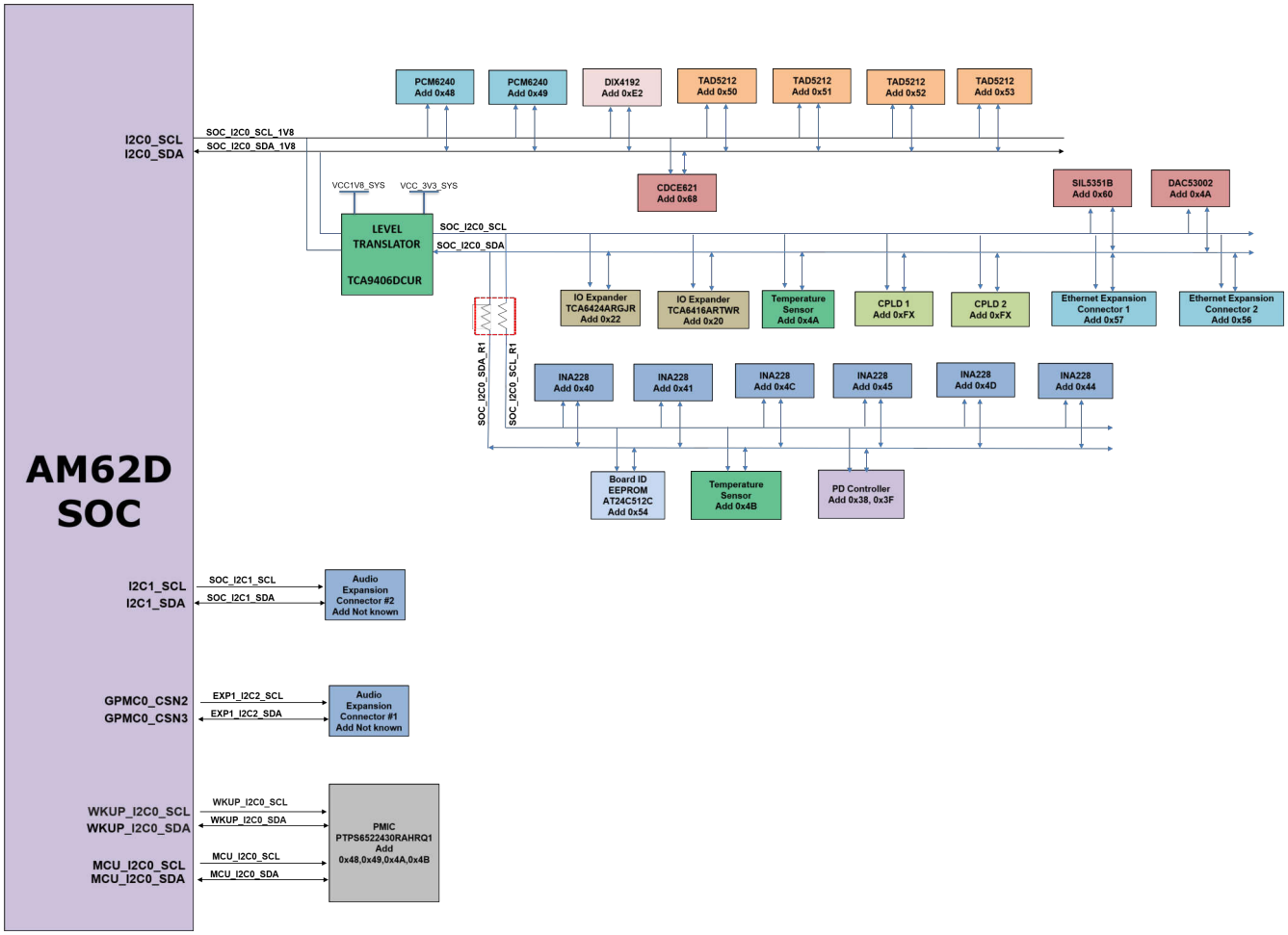


Figure 2-28. I2C Interface Tree

Table 2-22. I2C Mapping Table

I2C Port	Device/Function	Part Number	I2C Address
SoC_I2C0	Board ID EEPROM	AT24C512C-MAHM-T	0x54
SoC_I2C0	Ethernet Expansion Connector 1	<connector interface>	
SoC_I2C0	Ethernet Expansion Connector 2	<connector interface>	
SoC_I2C0	USB PD Controller	TPS65988DHRSHR	0x38, 0x3F
SoC_I2C0	Audio Microphone Line IN	PCM6240QRTVRQ1	0x48, 0x49
SoC_I2C0	Audio Stereo LINEOUT	TAD5212IRGER	0x50, 0x51, 0x52, 0x53
SoC_I2C0	Audio Digital IN & OUT Optical IN	DIX4192IPFB	0xE2
SoC_I2C0	Clock Generator 1	CDCE6214RGET	0x68
SoC_I2C0	DAC	DAC53002	0x62
SoC_I2C0	Clock Generator 2	SI5351B-B-GM	0x60
SoC_I2C0	Current Monitors	INA228AIDGSR	0x40, 0x41, 0x4C, 0x45, 0x4D & 0x44(E2)/0X47(E1)
SoC_I2C0	Temperature Sensors	TMP100NA/3K	0x4A, 0x4B
SoC_I2C0	GPIO Port Expander 1	TCA6424ARGJR	0x22
SoC_I2C0	GPIO Port Expander 2	TCA6416ARTWR	0x20
SoC_I2C0	CPLD	LCMXO2-256HC-4SG48I	Can be Programmed
SoC_I2C1	Audio Expansion Connector 2	<connector interface>	
SoC_I2C2	Audio Expansion Connector 1	<connector interface>	

Table 2-22. I2C Mapping Table (continued)

I2C Port	Device/Function	Part Number	I2C Address
MCU_I2C0	PMIC	PTPS6522430RAHRQ1	0x48,0x49,0x4A, 0x4B
WKUP_I2C0			
Others			
BOOTMODE_I2C	I2C Bootmode Buffer	TCA6424ARGJR	0x22

3 Hardware Design Files

The hardware design files such as schematics, BOM, PCB Layout, Assembly Files and Gerber files are available in the link below.

Design Files

4 Compliance Information

4.1 Compliance and Certifications

EMC, EMI and ESD Compliance

Components installed on the product are sensitive to Electric Static Discharge (ESD). TI recommends this product be used in an ESD controlled environment. This can include a temperature or a humidity controlled environment to limit the buildup of ESD. TI also recommends to use ESD protection such as wrist straps and ESD mats when interfacing with the product.

The product is used in the basic electromagnetic environment as in laboratory conditions, and the applied standard is as per EN IEC 61326-1:2021.

5 Additional Information

5.1 Known Hardware or Software Issues

This section describes the currently known issues on each EVM revision and applicable workarounds. Issues that have been patched have modification labels attached to the EVM assembly.

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   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

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NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

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