User's Guide

AM62P Power Estimation Tool

ABSTRACT

The Excel based AM62P Power Estimation Tool allows users to estimate thermal power based on specified loadings for different components (compute cores and peripherals) of the system-on-chip (SoC). The tool allows the user to pre-populate the various fields (which components are used, and utilization of the major components) from a set of representative use cases. This gives a starting point from which a new use case can be customized to judge the power and loadings of their own use case. The tool provides a breakdown of thermal power at the junction temperature (Tj) entered. The loadings represent the average activity over a duration of seconds or minutes.

Note

Power Estimation Tool generated estimates should not be used for power supply sizing.

Download the tool described in this document from: https://www.ti.com/lit/zip/sprujd9.

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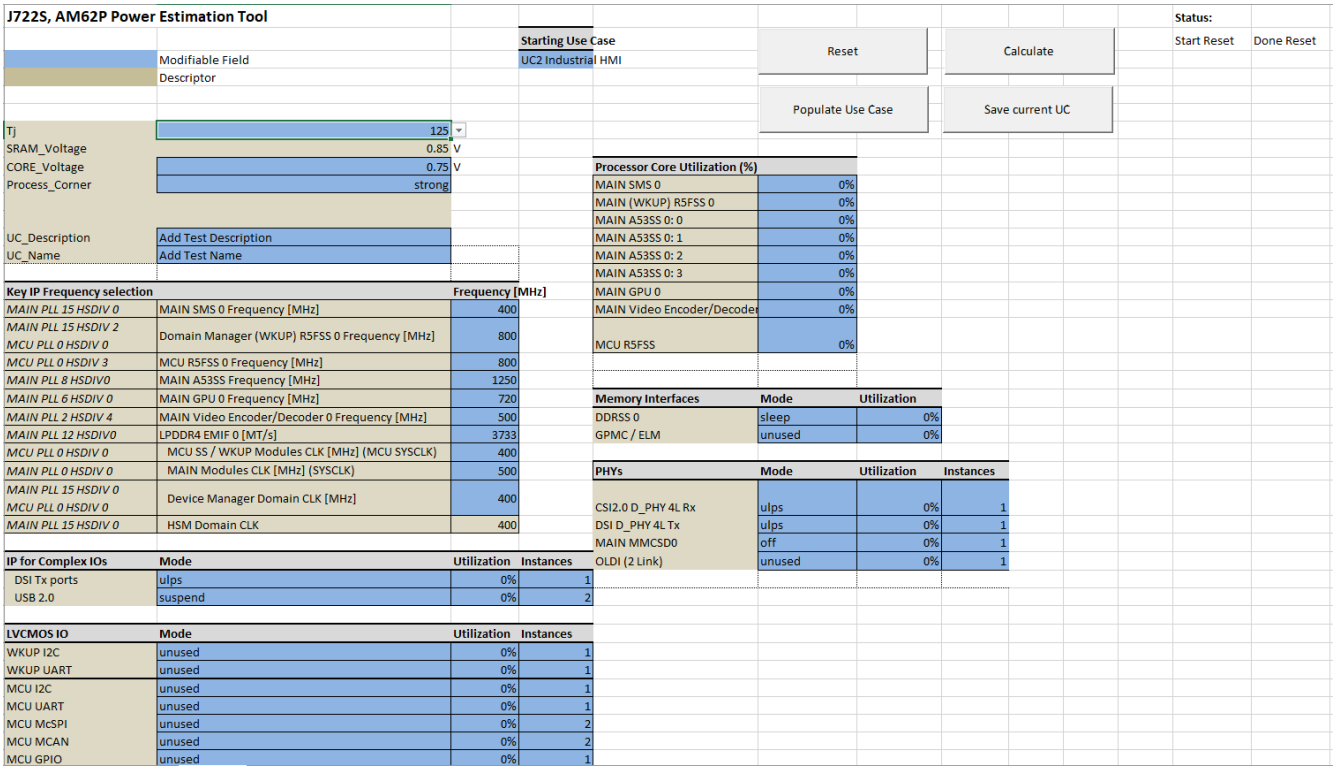
Trademarks

1 How to Use the Tool

The tool has two pages:

- Use Case: The Use Case sheet contains components which the user configures to match the desired use case and corresponding power estimate.
- Results: The Results sheet starts blank at initial tool launch and is populated with resulting power information from the Use Case inputs after the 'Calculate' button has been pressed.



J722S, AM62P Power Estimation Tool

Status: Start Reset | Done Reset

Starting Use Case: UC2 Industrial HMI

Reset | Calculate | Populate Use Case | Save current UC

Modifiable Field
Descriptor

Tj	125	
SRAM_Voltage	0.85	V
CORE_Voltage	0.75	V
Process_Corner	strong	
UC_Description	Add Test Description	
UC_Name	Add Test Name	

Key IP Frequency selection		Frequency [MHz]
MAIN PLL 15 HSDIV 0	MAIN SMS 0 Frequency [MHz]	400
MAIN PLL 15 HSDIV 2 MCU PLL 0 HSDIV 0	Domain Manager (WKUP) R5FSS 0 Frequency [MHz]	800
MCU PLL 0 HSDIV 3	MCU R5FSS 0 Frequency [MHz]	800
MAIN PLL 8 HSDIV0	MAIN A53SS Frequency [MHz]	1250
MAIN PLL 6 HSDIV 0	MAIN GPU 0 Frequency [MHz]	720
MAIN PLL 2 HSDIV 4	MAIN Video Encoder/Decoder 0 Frequency [MHz]	500
MAIN PLL 12 HSDIV0	LPDDR4 EMIF 0 [MT/s]	3733
MCU PLL 0 HSDIV 0	MCU SS / WKUP Modules CLK [MHz] (MCU SYSCLK)	400
MAIN PLL 0 HSDIV 0	MAIN Modules CLK [MHz] (SYSCLK)	500
MAIN PLL 15 HSDIV 0 MCU PLL 0 HSDIV 0	Device Manager Domain CLK [MHz]	400
MAIN PLL 15 HSDIV 0	HSM Domain CLK	400

IP for Complex IOs	Mode	Utilization	Instances
DSI Tx ports	ulps	0%	1
USB 2.0	suspend	0%	2

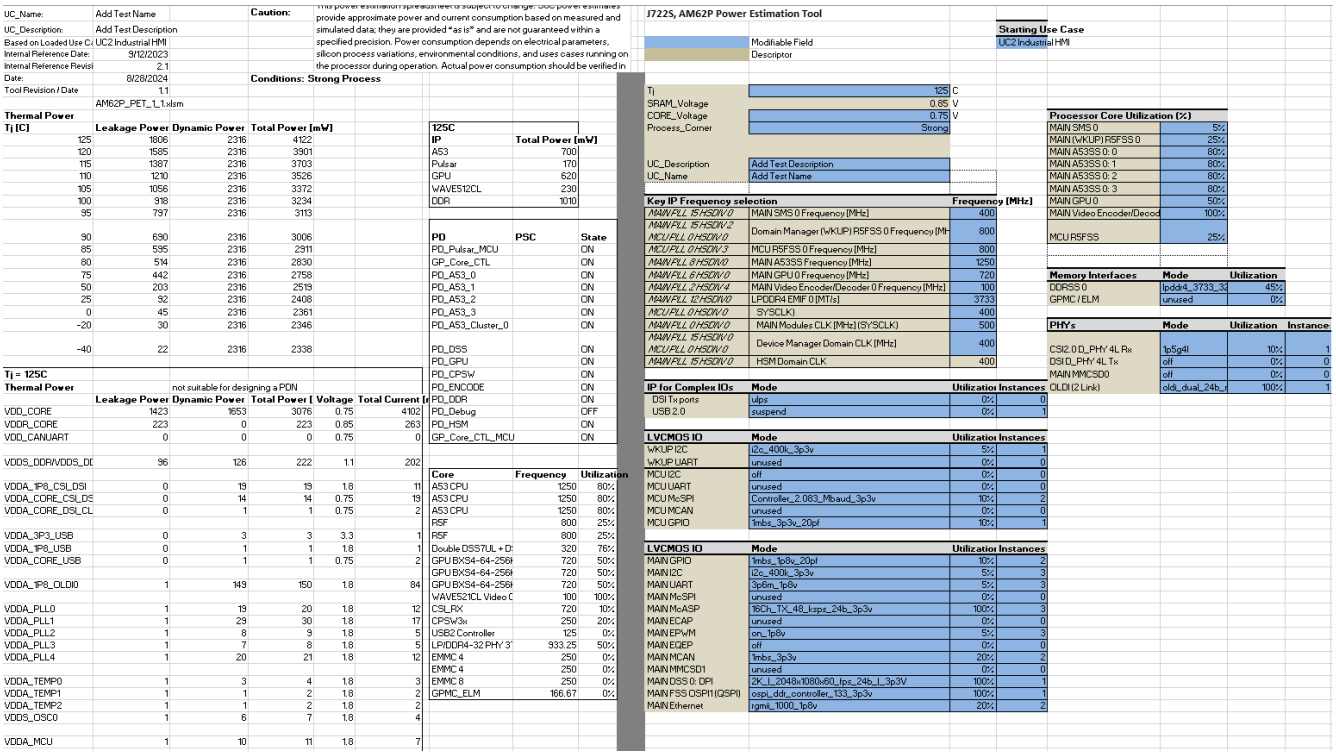
LVCMOS IO	Mode	Utilization	Instances
WKUP I2C	unused	0%	1
WKUP UART	unused	0%	1
MCU I2C	unused	0%	1
MCU UART	unused	0%	1
MCU McSPI	unused	0%	2
MCU MCAN	unused	0%	2
MCU GPIO	unused	0%	1

Processor Core Utilization (%)	
MAIN SMS 0	0%
MAIN (WKUP) R5FSS 0	0%
MAIN A53SS 0: 0	0%
MAIN A53SS 0: 1	0%
MAIN A53SS 0: 2	0%
MAIN A53SS 0: 3	0%
MAIN GPU 0	0%
MAIN Video Encoder/Decoder	0%
MCU R5FSS	0%

Memory Interfaces	Mode	Utilization
DDRSS 0	sleep	0%
GPMC / ELM	unused	0%

PHYs	Mode	Utilization	Instances
CSI2.0 D_PHY 4L Rx	ulps	0%	1
DSI D_PHY 4L Tx	ulps	0%	1
MAIN MMCSD0	off	0%	1
OLDI (2 Link)	unused	0%	1

Figure 1-1. Example Use Case Sheet



UC_Name: Add Test Name
UC_Description: Add Test Description
Based on Loaded Use C: UC2 Industrial HMI
Internal Reference Date: 9/12/2023
Internal Reference Revisi: 2.1
Date: 8/28/2024
Tool Revision / Date: 1.1
AM62P_PET_1_1.xlsm

Caution: This power estimation spreadsheet is subject to change. SoC power estimates provide approximate power and current consumption based on measured and simulated data; they are provided "as is" and are not guaranteed within a specified precision. Power consumption depends on electrical parameters, silicon process variations, environmental conditions, and uses cases running on the processor during operation. Actual power consumption should be verified in

Conditions: Strong Process

Thermal Power

Tj [C]	Leakage Power	Dynamic Power	Total Power [mW]
125	1806	2316	4122
120	1585	2316	3901
115	1387	2316	3703
110	1210	2316	3526
105	1056	2316	3372
100	918	2316	3234
95	797	2316	3113
90	690	2316	3006
85	595	2316	2911
80	514	2316	2830
75	442	2316	2758
50	203	2316	2519
25	92	2316	2408
0	45	2316	2361
-20	30	2316	2346
-40	22	2316	2338

Tj = 125C
Thermal Power — not suitable for designing a PDN

	Leakage Power	Dynamic Power	Total Power [	Voltage	Total Current [
VDD_CORE	1423	1653	3076	0.75	4102
VDDR_CORE	223	0	223	0.85	263
VDD_CANUART	0	0	0	0.75	0
VDDS_DDR/VDDS_DD	96	126	222	1.1	202
VDDA_1P8_CSI_DSI	0	19	19	1.8	11
VDDA_CORE_CSI_DS	0	14	14	0.75	19
VDDA_CORE_DSI_CL	0	1	1	0.75	2
VDDA_3P3_USB	0	3	3	3.3	1
VDDA_1P8_USB	0	1	1	1.8	1
VDDA_CORE_USB	0	1	1	0.75	2
VDDA_1P8_OLDI0	1	149	150	1.8	84
VDDA_PLL0	1	19	20	1.8	12
VDDA_PLL1	1	29	30	1.8	17
VDDA_PLL2	1	8	9	1.8	5
VDDA_PLL3	1	7	8	1.8	5
VDDA_PLL4	1	20	21	1.8	12
VDDA_TEMP0	1	3	4	1.8	3
VDDA_TEMP1	1	1	2	1.8	2
VDDA_TEMP2	1	1	2	1.8	2
VDDS_OSC0	1	6	7	1.8	4
VDDA_MCU	1	10	11	1.8	7

125C

IP	Total Power [mW]
AS3	700
Pulsar	170
GPU	620
WAVE512CL	230
DDR	1010

PD	PSC	State
PD_Pulsar_MCU		ON
GP_Core_CTL		ON
PD_A53_0		ON
PD_A53_1		ON
PD_A53_2		ON
PD_A53_3		ON
PD_A53_Cluster_0		ON
PD_DSS		ON
PD_GPU		ON
PD_CPSW		ON
PD_ENCODE		ON
PD_DDR		ON
PD_Debug		OFF
PD_HSM		ON
PD_Core_CTL_MCU		ON

Core	Frequency	Utilization
A53 CPU	1250	80%
A53 CPU	1250	80%
A53 CPU	1250	80%
R5F	800	25%
R5F	800	25%
Double DSS7UL + D	320	76%
GPU BXS4-64-256	720	50%
GPU BXS4-64-256	720	50%
GPU BXS4-64-256	720	50%
WAVE521CL Video C	100	100%
CSI_RX	720	10%
CPSW3x	250	20%
USB2 Controller	125	0%
LPDDR4-32 PHY 3	933.25	50%
EMMC 4	250	0%
EMMC 4	250	0%
EMMC 8	250	0%
GPMC_ELM	166.67	0%

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Starting Use Case: UC2 Industrial HMI

Modifiable Field
Descriptor

Tj	125	C
SRAM_Voltage	0.85	V
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UC_Name	Add Test Name	

Key IP Frequency selection		Frequency [MHz]
MAIN PLL 15 HSDIV 0	MAIN SMS 0 Frequency [MHz]	400
MAIN PLL 15 HSDIV 2 MCU PLL 0 HSDIV 0	Domain Manager (WKUP) R5FSS 0 Frequency [MH	800
MCU PLL 0 HSDIV 3	MCU R5FSS 0 Frequency [MHz]	800
MAIN PLL 8 HSDIV0	MAIN A53SS Frequency [MHz]	1250
MAIN PLL 6 HSDIV 0	MAIN GPU 0 Frequency [MHz]	720
MAIN PLL 2 HSDIV 4	MAIN Video Encoder/Decoder 0 Frequency [MHz]	100
MAIN PLL 12 HSDIV0	LPDDR4 EMIF 0 [MT/s]	3733
MCU PLL 0 HSDIV 0	SYSCLK)	400
MAIN PLL 0 HSDIV 0	MAIN Modules CLK [MHz] (SYSCLK)	500
MAIN PLL 15 HSDIV 0 MCU PLL 0 HSDIV 0	Device Manager Domain CLK [MHz]	400
MAIN PLL 15 HSDIV 0	HSM Domain CLK	400

IP for Complex IOs	Mode	Utilization	Instances
DSI Tx ports	ulps	0%	0
USB 2.0	suspend	0%	1

LVCMOS IO	Mode	Utilization	Instances
WKUP I2C	i2c_400k_3p3v	5%	1
WKUP UART	unused	0%	0
MCU I2C	off	0%	0
MCU UART	unused	0%	0
MCU McSPI	Controller_2.083_Mbaud_3p3v	10%	2
MCU MCAN	unused	0%	0
MCU GPIO	1mbs_3p3v_20pf	10%	1

LVCMOS IO	Mode	Utilization	Instances
MAIN GPIO	1mbs_1p8v_20pf	10%	2
MAIN I2C	i2c_400k_3p3v	5%	3
MAIN UART	3p6m_1p8v	5%	3
MAIN McSPI	unused	0%	0
MAIN McASP	16Ch_TX_48_ksps_24b_3p3v	100%	3
MAIN ECAP	unused	0%	0
MAIN EPWM	on_1p8v	5%	3
MAIN EQEP	off	0%	0
MAIN MCAN	1mbs_3p3v	20%	2
MAIN MMCSD1	unused	0%	0
MAIN DSS 0: DPI	2K_I_2048x1080x60_fps_24b_I_3p3V	100%	1
MAIN FSS OSPI1 (QSPI)	ospi_ddr_controller_133_3p3v	100%	1
MAIN Ethernet	rgmii_1000_1p8v	20%	2

Processor Core Utilization (%)	
MAIN SMS 0	5%
MAIN (WKUP) R5FSS 0	25%
MAIN A53SS 0: 0	80%
MAIN A53SS 0: 1	80%
MAIN A53SS 0: 2	80%
MAIN A53SS 0: 3	80%
MAIN GPU 0	50%
MAIN Video Encoder/Decod	100%
MCU R5FSS	25%

Memory Interfaces	Mode	Utilization
DDRSS 0	lpddr4_3733_32	45%
GPMC / ELM	unused	0%

PHYs	Mode	Utilization	Instance
CSI2.0 D_PHY 4L Rx	1p5g4l	10%	1
DSI D_PHY 4L Tx	off	0%	0
MAIN MMCSD0	off	0%	0
OLDI (2 Link)	oldi_dual_24b_r	100%	1

Figure 1-2. Example Result Sheet

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