EVM User's Guide: DP83TG720-EVM-AM2

DP83TG720-EVM-AM2 User Guide

Description

The DP83TG720-EVM-AM2 is an Automotive Ethernet PHY add-on board to be used with AM2x series Sitara™ high-performance microcontroller evaluation modules. This add-on board is an excellent choice for initial Ethernet evaluation and prototyping using AM2x EVMs. DP83TG720-EVM-AM2 is equipped with a TI DP82TG720S-Q1 1000BASE-T1 automotive Ethernet PHY with RGMII & SGMII, and a MATEnet connector. DP83TG720-EVM-AM2 is currently supported on TMDSCNCD263P and the AM263Px MCU PLUS SDK.

Features

- DP83TG720S-Q1 1000BASE-T1 automotive Ethernet PHY with RGMII & SGMII
- MATEnet Ethernet networking connector
- Shielded DF40GB 48-pin connector for interfacing with Sitara™ AM2x series evaluation modules
- Link status and activity LED indicators
- On-board TLV755P LDO

1 Evaluation Module Overview

Preface: Read This First

1.1 Sitara MCU+ Academy

Texas Instruments offers the *MCU+ Academy* as a resource for designing with the MCU+ software and tools on supported devices. The MCU+ Academy features easy-to-use training modules that range from the basics of getting started to advanced development topics.

1.2 If You Need Assistance

If you have any feedback or questions, support for the Sitara AM2x MCUs and the AM2x EVM Automotive Ethernet PHY Add-on Board development kit is provided by the TI Product Information Center (PIC) and the TI E2E™ Forum. Contact information for the PIC can be found on the TI website. Additional device-specific information can be found in Section 5.1.

1.1 Introduction

The AM2x EVM Automotive Ethernet PHY Add-on Board was developed to enable additional Ethernet peripheral support on AM2x EVMs and allow for rapid prototyping of the core SoC for Automotive Ethernet applications. This user's guide details the design of the add-on board and how to properly use the interface. The user's guide also details many important aspects of the board including, but not limited to pin header descriptions, test points, and signal routing.

1.2 Kit Contents

The Sitara AM2x EVM Automotive Ethernet PHY Add-on Board kit contains the following items:

- DP83TG720-EVM-AM2 Automotive Ethernet PHY Add-on Board

Not included:

- Sitara AM2x EVM

Note

DP83TG720-EVM-AM2 can be available as a virtual bundle with select Sitara AM2x EVMs. Visit the EVM page on ti.com for more information.

1.3 Device Information

The DP83TG720S-Q1 device is an IEEE 802.3bp and Open Alliance compliant automotive Ethernet physical layer transceiver. The DP83TG720S-Q1 provides all physical layer functions needed to transmit and receive data over unshielded and shielded single twisted-pair cables. The device provides xMII flexibility with support for RGMII and SGMII MAC interfaces.

DP83TG720 is compliant to Open Alliance EMC and interoperable specifications over unshielded twisted cable. DP83TG720 is front print compatible to TI’s 100BASE-T1 PHY enabling design scalability with single board for both speeds. This device offers the Diagnostic Tool Kit, with an extensive list of real-time monitoring tools, debug tools and test modes. Within the tool kit is the first integrated electrostatic discharge (ESD) monitoring tool. This tool is capable of counting ESD events on both the xMII and MDI as well as providing real-time monitoring through the use of a programmable interrupt. Additionally, the DP83TG720S-Q1 includes a data generator and checker tool to generate customizable MAC packets and check the errors on incoming packets. This enables systemlevel datapath tests and optimizations without dependency on MAC.

For additional information, refer to the DP83TG720S-Q1 data sheet.

2 Hardware

2.1 Component Identification

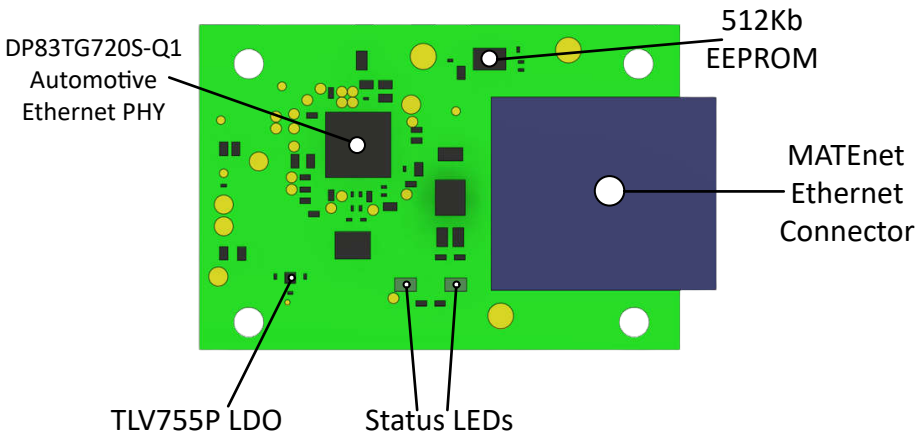

Figure 2-1. DP83TG720-EVM-AM2 Top Side

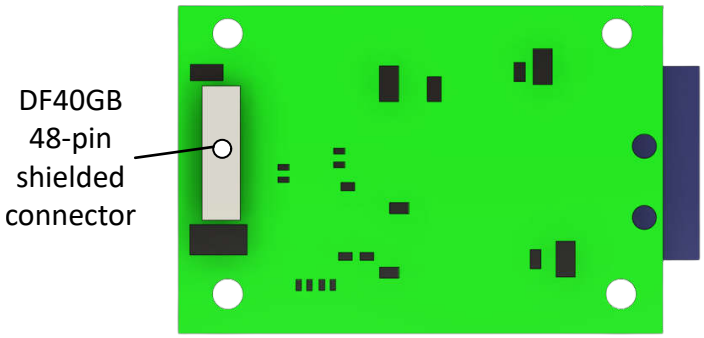

Figure 2-2. DP83TG720-EVM-AM2 Bottom Side

2.2 Power Requirements

The AM2x EVM Industrial Ethernet PHY Add-on Board is powered from 2.5V and 3.3V inputs from the DF40GB 48-pin connector that interfaces the DP83TG720-EVM-AM2 with the main MCU EVM. There is an on-board LDO that steps the 2.5V input down to 1.0V to supply the DP83TG720S-Q1 VDD inputs. The following sections describe the power distribution network topology that supply the AM2x EVM Industrial Ethernet PHY Add-on Board, supporting components, and reference voltages.

2.2.1 Power Tree

The DP83TG720-EVM-AM2 power is supplied from the main Sitara AM2x EVM via the DF40GB connector.

3.3V (VDDIO) is connected to pin 44 and 46 on the DF40GB connector, and is passed to the 3.3V source inputs on the DP83TG720S-Q1 Automotive Ethernet PHY through a pair of ferrite beads (one per supply net).

2.5V (VDD_2V5) is connected to pins 4 and 6 on the DF40GB connector, stepped down to 1.0V by the TLV755P LDO, and is passed to the 1.0V source inputs on the DP83TG720S-Q1 Automotive Ethernet PHY through a ferrite bead.

Figure 2-3 shows the power connections of DP83TG720-EVM-AM2.

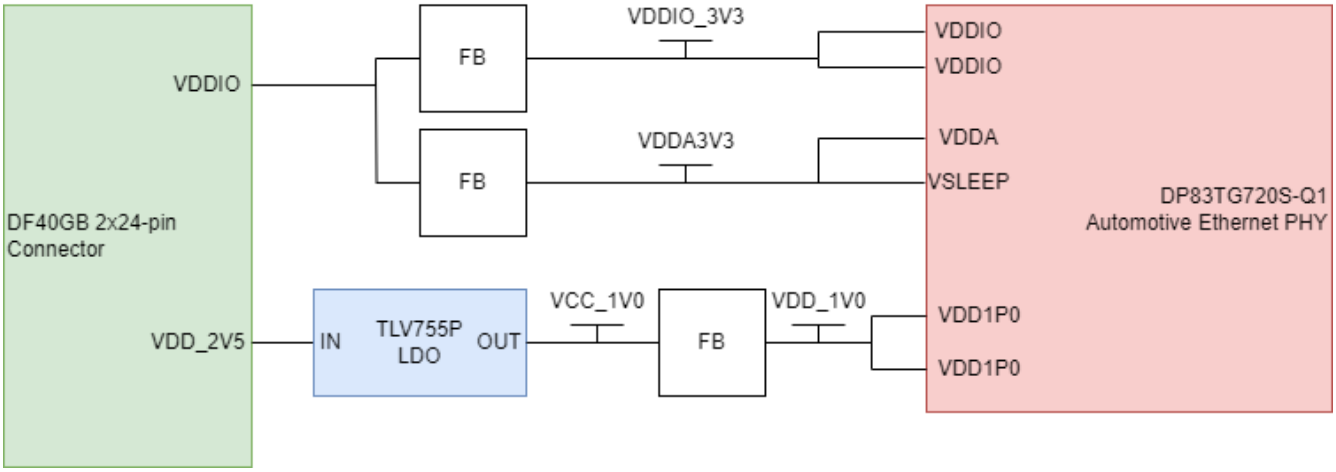

Figure 2-3. Power Tree

2.3 Functional Block Diagram

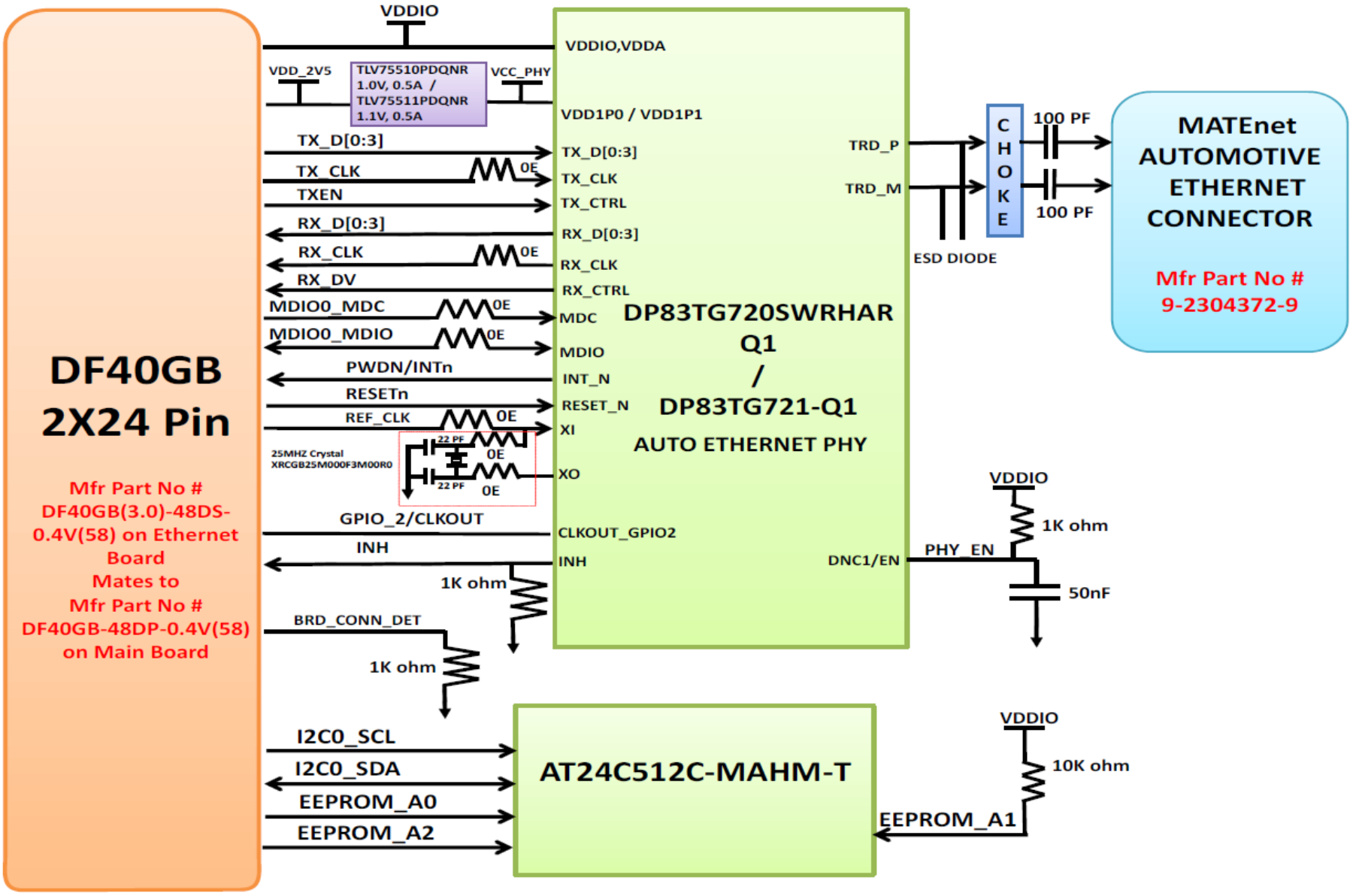

Figure 2-4. AM2x Automotive Ethernet PHY Add-on Board Block Diagram

2.4 Header Information

The DP83TG720-EVM-AM2 is equipped with a Hirose DF40GB 2x24-pin connector (J2) to connect to Sitara AM2x EVMs. Listed below are the features of this connector relevant to this EVM:

- 2x24 pins
- Shielded type to support high-speed signals and prevent noise
- High density mounting

Refer to Table 2-1 for a complete list of the header pins and descriptions.

Table 2-1. DF40GB Header Pinout

Pin #	Signal	Description		Description	Signal	Pin #
1	GND	Ground		PMIC External Voltage Monitor	EXT_VMON2	2
3	TX_CLK	Transmit Clock		2.5V supply	VDD_2V5	4
5	GND	Ground		2.5V supply	VDD_2V5	6
7	TX_D0	Transmit Data 0		Ground	GND	8
9	TX_D1	Transmit Data 1		Interrupt To Ethernet PHY	PWDN/INTn	10
11	TX_D2	Transmit Data 2		Reset input to Ethernet PHY	RESETn	12
13	TX_D3	Transmit Data 3		Collision Detected	COL	14
15	GND	Ground		Ground	GND	16
17	GND	Ground		Ground	GND	18
19	RX_CLK	Receive Clock		MDIO Clock	MDIO_MDC	20
21	GND	Ground		MDIO Data	MDIO_MDIO	22
23	RX_D0	Receive Data 0		Ground	GND	24
25	RX_D1	Receive Data 1		Inhibit	INH	26
27	RX_D2	Receive Data 2		PRUx Reference Clock	REF_CLK	28
29	RX_D3	Receive Data 3		Carrier Sense	CRS	30
31	GND	Ground		Ground	GND	32
33	GND	Ground		Ground	GND	34
35	TXEN	Transmit Enable		Board Connection Detect	BRD_CONN_DET	36
37	EEPROM_A2	EEPROM I2C Address bit [2]		IEEE 1588 SFD	1588_SFD	38
39	RX_ER	Receive Data Error		I2C Clock	I2C_SCL	40
41	GND	Ground		I2C Data	I2C_SDA	42
43	RX_LINK	Receive Indicator		IO Voltage Supply	VDDIO	44
45	RXDV	Receive Data Valid		IO Voltage Supply	VDDIO	46
47	EEPROM_A0	EEPROM I2C Address bit [0]		Audio Bit Clock	GPIO_2/CLKOUT	48

2.5 Test Points

DP83TG720-EVM-AM2 is equipped with multiple test points for hardware debug and bench testing. DP82TG720-EVM-AM2 Test Pointsshows the test points on the board and their associated signal net.

Table 2-2. DP83TG720-EVM-AM2 Test Points

Test Point	Signal	Description
TP1	GND	Ground
TP2	GND	Ground
TP3	GND	Ground
TP4	RXCLK	Receive Clock
TP5	RXD1	Receive Data 1
TP6	RXD3	Receive Data 3
TP7	TXCLK	Transmit Clock
TP8	RXD0	Receive Data 0
TP9	RXD2	Receive Data 2
TP10	CLK_OUT2	DP83TG720S-Q1 25-MHz reference clock output
TP11	GND	Ground
TP12	TXEN	Transmit Enable
TP13	TXD3	Transmit Data 3
TP14	GND	Ground
TP15	RXDV	RGMII Receive Control
TP16	TXD1	Transmit Data 1
TP17	TXD2	Transmit Data 2
TP18	TXD0	Transmit Data 0
TP19	RXER	Receive Data Error
TP20	1588_SFD	EEE 1588 SFD
TP21	RXLINK	Receive Indicator
TP22	MDIO_MDIO	MDIO Data
TP23	INH	Inhibit
TP24	RESETn	PHY Reset
TP25	CRS	Carrier Sense
TP26	MDIO_MDC	MDIO Clock
TP27	REF_CLK	Reference Clock Input
TP28	COL	Collision Detected
TP29	EXT_VMON	PMIC External Voltage Monitor
TP30	LED1	Link Status and BLINK for TX/RX Activity
TP31	VCC_1V0	1.0V PHY supply
TP32	GND	Ground

2.6 Interfaces

2.6.1 Automotive Ethernet PHY

The AM2x EVM Automotive Ethernet PHY Add-on Board uses one port of RGMII signals and the PRUx core of the PRU-ICSS to be connected to a 48-pin Ethernet PHY (DP83TG720SWRHARQ1). The PHY is configured to advertise 1-Gb operation. The Ethernet data signals of the PHY are terminated to a MATEnet connector. LEDs are used to indicate link status and activity.

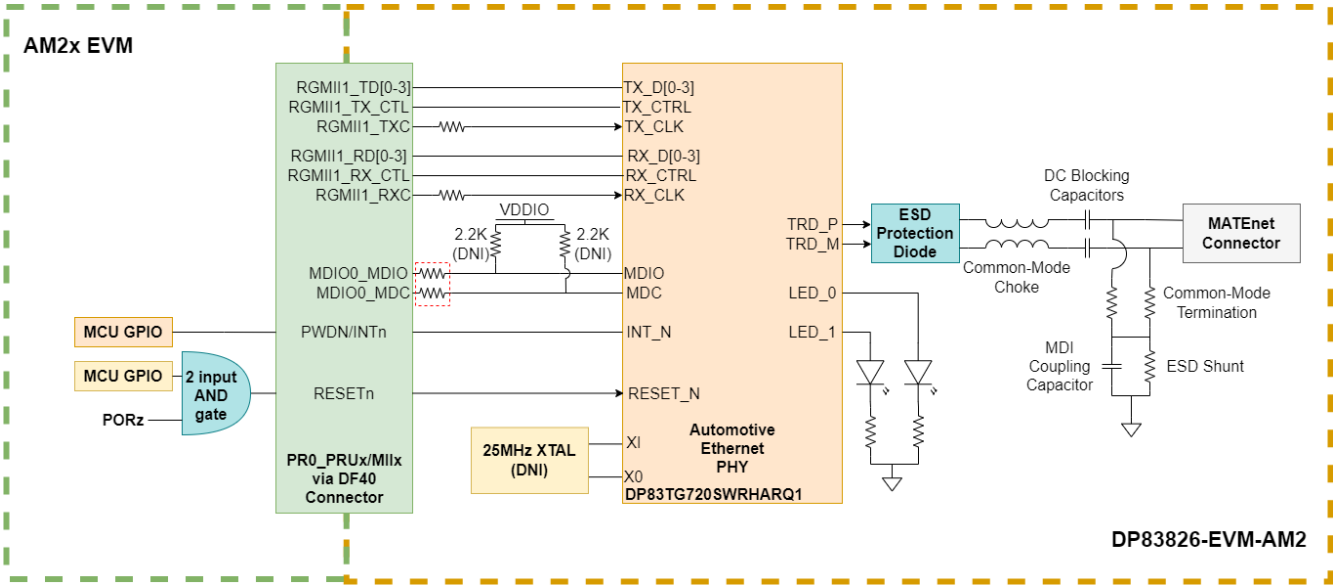

Figure 2-5. Automotive Ethernet PHY

The Ethernet PHY requires three power sources, VDDIP0 (1.0V), VDDIO (3.3V) and VDDA (3.3V) which are supplied through the DF40GB connector (J2) and an on-board LDO (U4).

Note

DP83TG720-EVM-AM2 is configured for VDDIO=3.3V, but can be supplied using VDDIO=2.5V or VDDIO=1.8V

On some AM2x EVMs, The RGMII port of the CPSW signals are internally muxed on the same balls of the MCU as the PRU-ICSS Ethernet signals. To use RGMII, the balls must be set to the appropriate mux mode for RGMII.

The MDIO and Interrupt signals from the main EVM SoC to the PHY require 2.2KΩ pull up resistors to the I/O supply voltage for proper operation. These resistors are not assembled by default on the DP83TG720-EVM-AM2, but there are footprints if the main EVM does not have these signals pulled up. The interrupt signal is driven by a GPIO signal that is mapped from the main EVM SoC.

The reset signal for the Ethernet PHY is most often driven by a 2-input AND gate. The AND gate's inputs are a GPIO signal that is generated by the main SoC EVM and a power-on reset signal on the main EVM.

2.6.2 Automotive Ethernet PHY Strapping Resistors

The Ethernet PHY uses many functional pins as strap option to place the device into specific modes of operation.

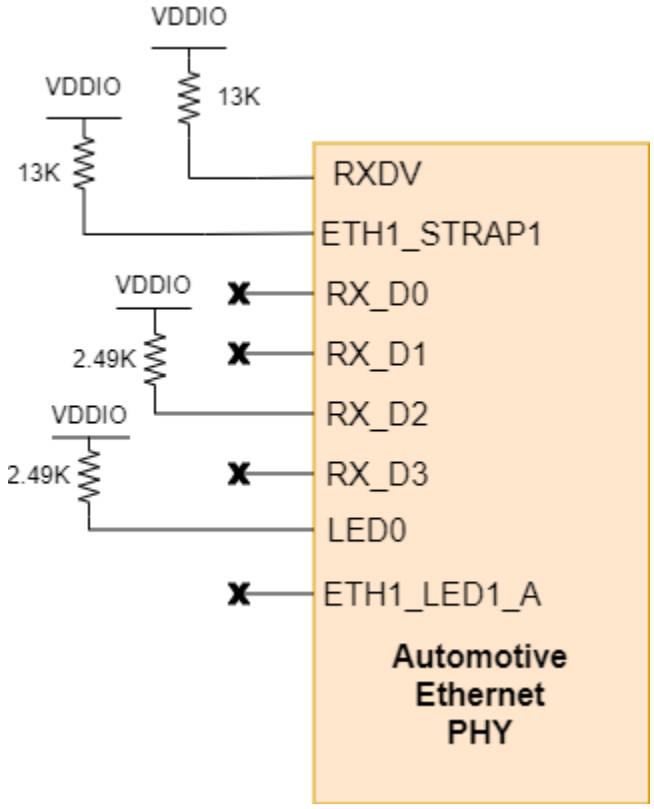

Figure 2-6. Automotive Ethernet PHY Strapping Resistors

Table 2-3. Recommended 3-level Strap Resistor Ratios

MODE	IDEAL RH (kΩ) for VDDIO = 3.3V
1	OPEN
2	13
3	4.5

Table 2-4. Recommended 2-level Strap Resistor

MODE	IDEAL RH (kΩ)
1	OPEN
2	2.49

Table 2-5. Industrial 1 Gbit Ethernet PHY Strapping Resistors

Functional Pin	Default Mode	Mode on DP83TG720-EVM-AM2	Pull-Up	Function
RX_D0	1	1	OPEN	MAC Interface: RGMII (Align mode)
RX_D1	1	1	OPEN	
RX_D2	1	2 (2-level)	2.49kΩ	
RX_CTRL		2 (3-level)	13kΩ	PHY address: 0xC (0b01100)
STRP_1		2 (3-level)	13kΩ	
LED_0	1	2 (2-level)	2.49kΩ	MS=0
LED_1	1	1	OPEN	Autonomous

2.6.3 Multi-Connector Addressing

For Sitara AM2x EVMs with more than one Ethernet add-on board connector, each DP83TG720-EVM-AM2 requires a different EEPROM I2C address and PHY address. The EEPROM A0 and A2 nets, set by pull resistors on the main Sitara AM2x EVM drive the PHY address nets via a FET network implemented on the DP83TG720-EVM-AM2. Table 2-6 details the multi-connector I2C and PHY addressing scheme implemented on the add-on PHY board.

Note

- The EEPROM I2C address bits A2 and A0 are driven via pull resistors on the main Sitara AM2x EVM. The pull resistors for each enumerated connector follow the table below.
- EEPROM I2C address bit A1 will **always** be pulled high to VDDIO on the add-on board
- The EEPROM I2C address is defined by the following 8 bits: 8b1010[A2][A1][A0][R/W]
- Pulls to VDDIO/GND are via 10kOhm resistor
- All EVMs with a single connector are configured as CONNECTOR_0

Table 2-6. Multi-Connector I2C / PHY Addressing Scheme

Connector_#	EEPROM_A2 (connector pin 37)		EEPROM_A1		EEPROM_A0 (connector pin 47)		I2C Address	DP83TG720 PHY Address
	Pull	A2	Pull	A1	Pull	A0		
CONNECTOR_0	GND	0	VDDIO	1	GND	0	0x52	4b1111
CONNECTOR_1	GND	0	VDDIO	1	VDDIO	1	0x53	4b1010
CONNECTOR_2	VDDIO	1	VDDIO	1	GND	0	0x56	4b0101
CONNECTOR_3	VDDIO	1	VDDIO	1	VDDIO	1	0x57	4b0000

2.7 Integration Guide

The Sitara AM2x Ethernet Add-on Board ecosystem is not limited to the DP83TG720x Automotive Ethernet PHY. A wide variety of Automotive Ethernet PHYs with Sitara AM2x MCU compatible signals can be designed onto add-on boards to be used across Sitara AM2x MCU EVMs. This section details the mechanical information and provide the necessary dimensions for designing an Automotive Ethernet PHY add-on board.

Note

All dimensions are measured in inches.

2.7.1 Board Dimensions

Figure 2-7 shows the proper PCB dimensions for an Industrial Ethernet PHY add-on board to be compatible with Sitara AM2x EVMs.

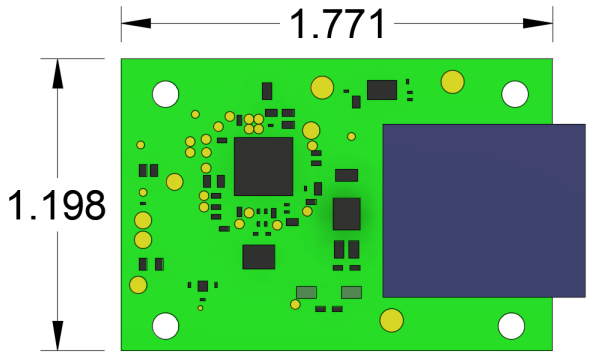

Figure 2-7. Automotive Ethernet PHY Add-on Board Dimensions

Figure 2-8 shows the side profile of the PCB.

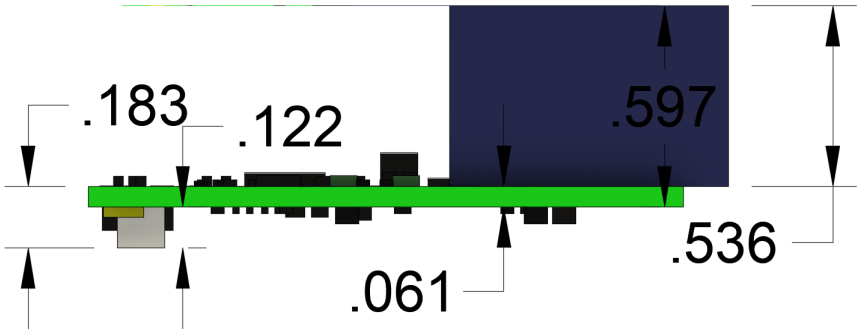

Figure 2-8. Automotive Ethernet PHY Add-on Board Side Profile

2.7.2 DF40GB Connector

TI recommends the 48-pin (2x24) Hirose DF40GB high-density, shielded connector for Ethernet PHY Add-on Boards interfacing with Sitara AM2x EVMs. Figure 2-9 shows the mounting position of the DF40GB connector on the DP83TG720-EVM-AM2.

The origin of the connector is to be placed at **(x,y)=(0.157,0.537)**.

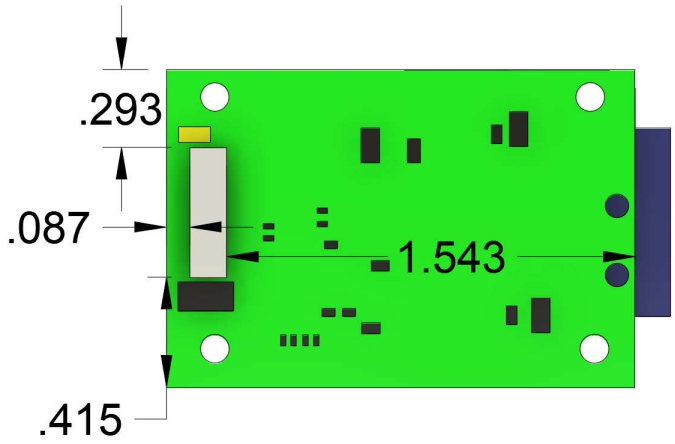

Figure 2-9. DF40GB Connector Mounting Position

2.7.3 Mounting Holes

The DP83TG720-EVM-AM2 is designed with mounting holes to securely attach to the main Sitara AM2x MCU EVM. The compatible Sitara AM2x EVMs are designed to have matching mounting holes for an Ethernet Add-on Board to connect to. Screws and spacers can be inserted into the mounting holes for a more permanent configuration. Figure 2-10 shows the positions of the mounting holes on the DP83TG720-EVM-AM2.

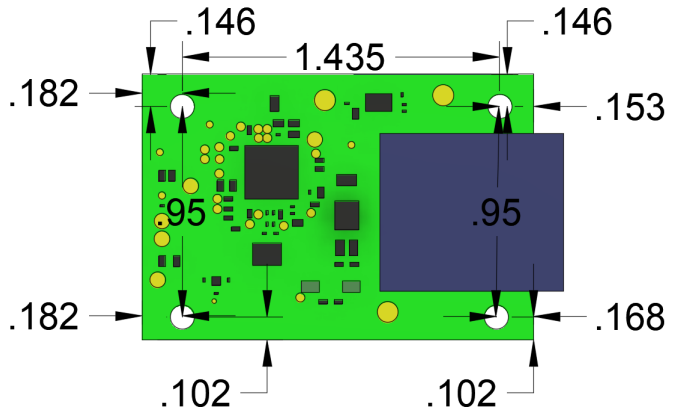

Figure 2-10. Mounting Hole Positions

2.7.4 MATEnet Ethernet Connector

The DP83TG720-EVM-AM2 has a MATEnet Ethernet Connector for sending and receiving signals from the DP83TG720S-Q1 Ethernet PHY. Different Automotive Ethernet PHYs utilize the same connector, and must be used on custom Automotive Ethernet PHY Add-on Boards. Figure 2-11 shows the position of the MATEnet connector on the DP83TG720-EVM-AM2.

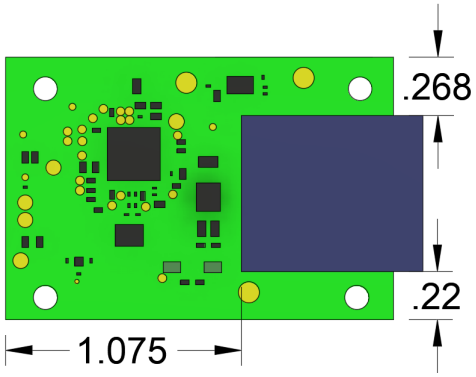

Figure 2-11. MATEnet Connector Position

3 Hardware Design Files

To download the zip file containing the latest design files for the EVM, go to the product folder DP83TG720-EVM-AM2.

4 Additional Information

4.1 Trademarks

Sitara™ and E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

5 References

5.1 Reference Documents

In addition to this document, the following references are available for download at www.ti.com.

- *AM263P controlCARD Evaluation Module Tool Folder*
- *AM263P controlCARD Evaluation Module User's Guide*
- *Texas Instruments Code Composer Studio*

5.2 Compatible Sitara™ MCU AM2x EVMs

This Ethernet add-on board is compatible with the following EVMs:

- *TMDSCNCD263P*

5.3 Other TI Components Used in This Design

This Ethernet Add-on board uses various other TI components for the functions. A consolidated list of these components with links to the TI product pages is shown below.

- *TPD2E2U06-Q1 Automotive Dual 1.5-pF, 5.5-V, ±25-kV ESD protection diode for USB & High Speed Interfaces*
- *TLV755P 500-mA high-PSRR low-IQ low-dropout voltage regulator with enable*

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from January 1, 2024 to October 30, 2024 (from Revision * (January 2024) to Revision A (October 2024))	Page
• [Header Information] Updated DF40GB header pinout to match Rev A design	6
• [Test Points] updated TP list for Rev A design	7

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