User's Guide

TMS320F2837x, TMS320F2838x, TMS320F28P65x Migration to TMS320F29H85x

ABSTRACT

This migration guide describes the hardware and software differences to consider when moving between F2837x, F2838x, F28P65x and F29H85x C2000™ MCUs, where F28P65x is used as the example of a Gen 3 device in individual sections. While the CPU system from C28x to C29x has improved, the block diagram is not shown between the two MCUs as a visual representation on what blocks are similar or different. As there will be huge differences, there is a section sharing the improvement on the architecture in C29x. It also highlights the features that are unique between the devices for all available packages in a device comparison table. To facilitate application and hardware migration between Gen3 and Gen4 devices, the new PCB hardware section provides guidance on how to proceed with the new design for F29H85x. As there are many new features being offered on this device, there are sections showing the new changes that have been made and what value each feature adds. This serves as a reference for hardware design and signal routing when considering a move between the devices.

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1 Feature Differences Between F2837x, F2838x, F28P65x and F29H85x

Drop-in pin compatibility is not supported when migrating from Gen 3 devices to F29H85x. Users are expected to map the pin resources accordingly when migrating to F29H85x.

Note

This comparison guide focuses on the superset devices: F2837x, F2838x, F28P65x and F29H85X as other part numbers in these product series have reduced feature support. For details specific to certain part numbers, see the device-specific data sheet.

1.1 F28x to F29x Feature Change Overview

The Figure 1-1, shows the new CPU sub-system and associated peripherals. The feature comparison of the superset part numbers for F2837x, F2838x, F28P65x and F29H85x devices is shown in Table 1-1.

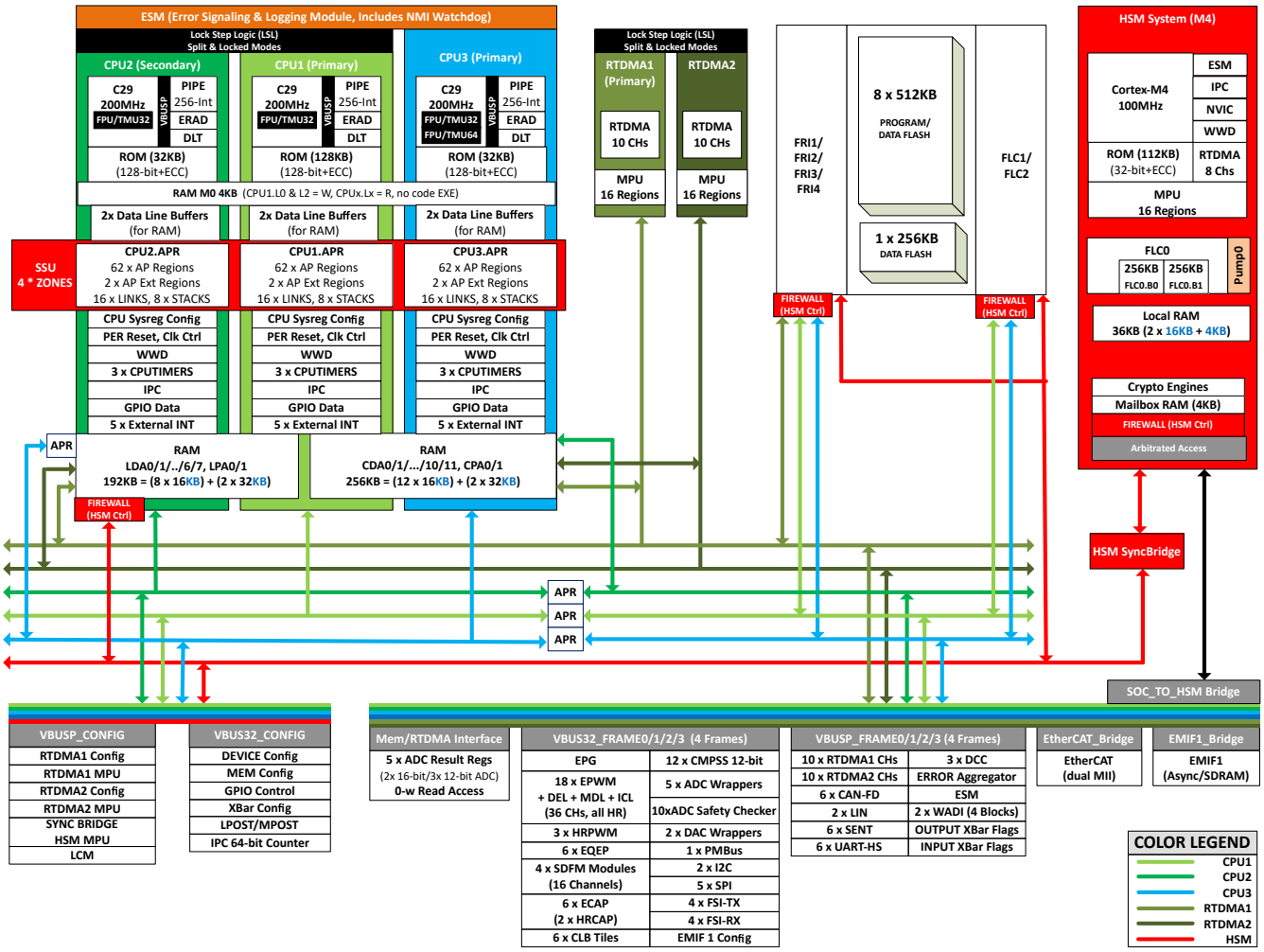

Figure 1-1. F29H85x Block Diagram

Table 1-1. IP Differences

Feature		F2837x	F2838x	F28P65x	F29H85x
C2000 CPU Subsystem					
CPU Type		C28x	C28x	C28x	C29x
Number of CPU		2	2	2	3
CPU Frequency (MHz)		200	200	200	200
32-bit and 64-bit Floating-Point Unit (FPU)		Yes	Yes	Yes	Yes (CPU1/2 - 32-bit, CPU3 - 32-bit & 64-bit)
CPU Lockstep		No	No	Yes (Lockstep between CPU2 and Shadow-CPU2)	Yes (CPU1/CPU2 are Lockstep capable)
Relative Performance					
Signal Chain Performance		-			3x faster
FFT Performance		-			5x faster
Interrupt Response		-			4x faster
General Purpose Code		-			3x faster
Memory					
Flash		1MB	1MB	1.28MB	4MB + 256KB (Data Bank)
RAM		204KB	216KB	248KB	452KB
System					
CLA		2	2	1 (CPU1 only)	No
External Memory Interface (EMIF)		2	2	1	1
DMA		1 per CPU (6 channels)	1 per CPU (6 channels)	1 per CPU (6 channels)	2 - Real-time DMA (10 channels each)
Data Logger and Trace (DLT)		No	No	No	Yes
Embedded Pattern Generator (EPG)		No	No	Yes	Yes
Enhanced Real-time Analysis and Diagnostic (ERAD)		No	Yes	1 per CPU (Type 2)	1 per CPU (Type 5)
CPU Timer		3 per CPU	3 per CPU	3 per CPU	3 per CPU
Analog Peripherals					
ADC 16/12-bit	Number of ADCs	4	4	3	2
	16-bit MSPS	1.1	1.1	1.19	1.19
	16-bit Conversion Time (ns)	915	915	840	840
	12-bit MSPS	3.5	3.5	3.92	3.92
	12-bit Conversion Time (ns)	280	280	255	255
ADC 12-bit	Number of ADCs	No	No	No	3
	MSPS	-	-	-	3.92
	Conversion Time (ns)	-	-	-	255
Temperature Sensor		1	1	1	1
Buffered DAC - Type 2		3	3	2	2
CMPSS - Type 6		8	8	11	12
Control Peripherals					
eCAP - Type 3	Total Modules	6 - Type 0	7 - Type 2	7	6
	HRCAP Capable	0	2 (eCAP6, eCAP7)	2 (eCAP6, eCAP7)	2 (eCAP5, eCAP6)
ePWM - Type 5	Total Channels	24 - Type 4	32 - Type 4	36	36
	HRPWM Capable	16	16	36	36
eQEP - Type 2		3	3	6	6
Configurable Logic Block (CLB) - Type 3		4 tiles	8 tiles	6 tiles	6 tiles

Table 1-1. IP Differences (continued)

Feature	F2837x	F2838x	F28P65x	F29H85x
Sigma-Delta Filter Module (SDFM) Channels - Type 2	8 - Type 0	8	16 Channels (4 SDFM Modules)	16 Channels (4 SDFM Modules)
Communication Peripherals				
Ethernet for Control Automation Technology (EtherCAT)	No	Yes	Yes	Yes
Controller Area Network (CAN) 2.0B - Type 0	2	2	1	No
CAN with Flexible Data-Rate (CAN-FD) - Type 2	0	1	2	6
Fast Serial Interface (FSI) RX - Type 2	0	8 - Type 1	4	4
Fast Serial Interface (FSI) TX - Type 2	0	2 - Type 1	2	4
Inter-Integrated Circuit (I2C)	2 (Type 0)	2 (Type 0)	2 (Type 1)	2 (Type 2)
Local Interconnect Network (LIN) - Type 1	0	0	2	2
Power Management Bus (PMBus) 1.1 - Type 0	0	1	1	1
High Speed UART (HS-UART) - Type 1	0	1 (CM)	2	6
Single Edge Nibble Transmission (SENT) - Type 1	0	0	No	6
Serial Peripheral Interface (SPI) - Type 2	3	4	4	5
Serial Communications Interface (SCI) - Type 0	4	4	2 - UART Compatible	No
Universal Serial Bus (USB) - Type 0	1	1	1	No
Safety and Security				
Dual-zone Code Security Module (DCSM)	No	Yes	Yes	No
Error Signaling Module (ESM)	No	No	No	Yes
Hardware Security Module (HSM)	No	No	No	Yes
Logic Power-on Self-test (LPOST)	No	No	No	Yes
Memory Power-on Self-test (MPOST)	No	No	No	Yes
Safety and Security (SSU) Module	No	No	No	Yes
Waveform Analysis and Diagnostics (WADI)	No	No	No	Yes
Functional Safety	ASIL B/SIL 2	ASIL B/SIL2	ASIL B/SIL2	ASIL D/SIL3

Table 1-2. 100-pin IO and Analog Channel Counts

IO Type	F2837x	F2838x	F28P65x	F29H85x
Digital				
AIO (analog with digital inputs)	41	-	13	16
AGPIO (analog with digital inputs and outputs)		-	11	8
Additional GPIO		-	4 (2 from JTAG and 2 from X1/X2)	5 (ERRORSTS, TDI, TDO, X1, X2)
Standard GPIO		-	49	41
Total GPIO		-	60	46
Total GPIO + AIO		-	73	70
Analog				
ADC Channels (single-ended, all modules)	24	-	24	24

Table 1-2. 100-pin IO and Analog Channel Counts (continued)

IO Type	F2837x	F2838x	F28P65x	F29H85x
ADC Channels (differential, ADC AB)	12	-	11	6

Table 1-3. 176-pin IO and Analog Channel Counts

IO Type	F2837x	F2838x	F28P65x	F29H85x
Digital				
AIO (analog with digital inputs)	97	97	14	28
AGPIO (analog with digital inputs and outputs)			22	26
Additional GPIO			4 (2 from JTAG and 2 from X1/X2)	5 (ERRORSTS, TDI, TDO, X1, X2)
Standard GPIO			106	81
Total GPIO			128	86
Total GPIO + AIO			142	140
Analog				
ADC Channels (single-ended, all modules)	20	20	36	54
ADC Channels (differential, ADC AB)	9	9	18	13

Table 1-4. 256-pin IO and Analog Channel Counts

IO Type	F2837x	F2838x	F28P65x	F29H85x
Digital				
AIO (analog with digital inputs)	-	-	18	54
AGPIO (analog with digital inputs and outputs)	-	-	22	26
Additional GPIO	-	-	4 (2 from JTAG and 2 from X1/X2)	5 (ERRORSTS, TDI, TDO, X1, X2)
Standard GPIO	-	-	163	105
Total GPIO	-	-	185	110
Total GPIO + AIO	-	-	203	190
Analog				
ADC Channels (single-ended, all modules)	-	-	40	80
ADC Channels (differential, ADC AB)	-	-	19	16

2 C29x Architecture

With the solid basis of the real-time feature and fast-signal chain, the C28x core is evolving to a new generation C29x core. This change in C29x helps improve the overall performance and increase the market share of all kinds of real-time applications. This section shows the new architecture of C29x, and an overview of the new features that have been added and improved from C28x.

2.1 C29x Architecture Overview

The C29 CPU is an enhanced VLIW (Very Long Instruction Word) architecture with a fully protected pipeline. C29 supports multiple instruction sizes (16, 32, and 48 bits) and a variable instruction packet size which contains instructions that execute in parallel. This is enabled by multiple functional units inside the CPU which can execute concurrently. A total of 64 working registers support the parallel operations in the CPU. In addition to the working registers, the CPU contains multiple status registers which maintain different execution and interrupt context related information. The major features in C29x are specified in Table 2-1.

Table 2-1. C29 Major Feature

Feature	Comment
Ease of Use	• Byte addressable CPU • Linear and unified memory map with 4GB address range • Fully protected pipeline • Deterministic execution without cached memories
Improved Parallelism	• Execute 1 to 8 instructions in parallel • Execute fixed-point, floating point, and addressing operations in parallel • Specialized instructions for decision making code and real-time control (example: if-then-else statements, trigonometric and multiphase vector translation operations)
Improved Bus Throughput	• Capable of fetching up to 128-bit instruction word every cycle • Capable of performing 8, 16, 32, 64-bit dual reads and single writes per cycle • Improved addressing modes which reduce overhead in accessing memory and peripheral resources
Code Efficiency	• Supports variable length instruction set (16-bit, 32-bit, and 48-bit) • Critical operations are encoded as 16-bit and 32-bit opcodes for improving the code density • Rich instruction set optimizes operations in smallest instructions
ASIL-D Safety Capability	• Support for both Lockstep and split lock modes • Integrated ECC logic enables end to end safe interconnect • Separate code threads can be fully isolated including stack using SSU • Zero CPU overhead switching from one thread to other in HW automatically enabled best real-time performance
Multi-zone Security	• Run time content protection and IP protection of code • Individual passwords for each zone to control access
Enhanced Debug and Trace Capabilities	• Specialized data logging and code flow trace instructions • Trace data capable of being logged in on-chip RAM or exported through serial communication peripherals

Besides from the C29x's feature improvement, there are several new IPs that is used for faster signal chain and safer environment around the CPU.

2.1.1 Peripheral Interrupt Priority and Expansion (PIPE)

In C28x, the primary interrupt controller was the Peripheral Interrupt Expansion (PIE). In C29x, the primary interrupt controller is the Peripheral Interrupt Priority and Expansion (PIPE). The PIPE module arbitrates peripheral interrupts across the device. All asserted interrupts are arbitrated each clock cycle, with the highest priority interrupt asserted to the appropriate CPU interrupt line (NMI, RTINT, or INT). The PIPE module is responsible for providing vector addresses to the CPU for NMI, RTINT, INT and RESET. The PIPE is capable custom ordering of interrupts and hardware nesting. For more information, see the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual*.

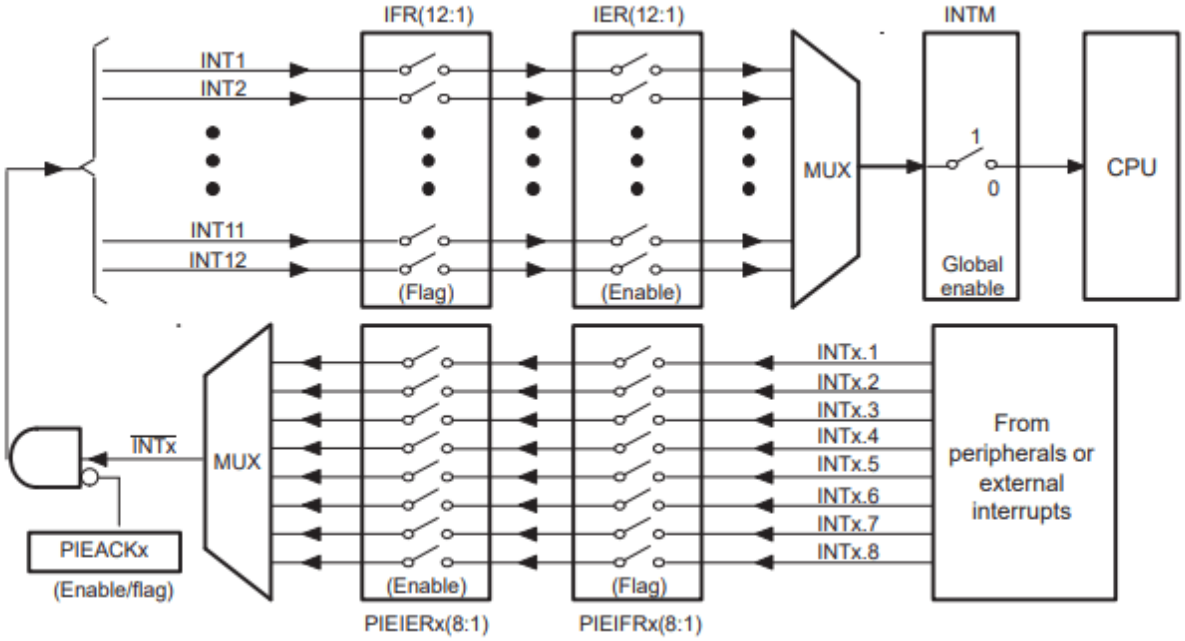

Figure 2-1. PIE Architecture

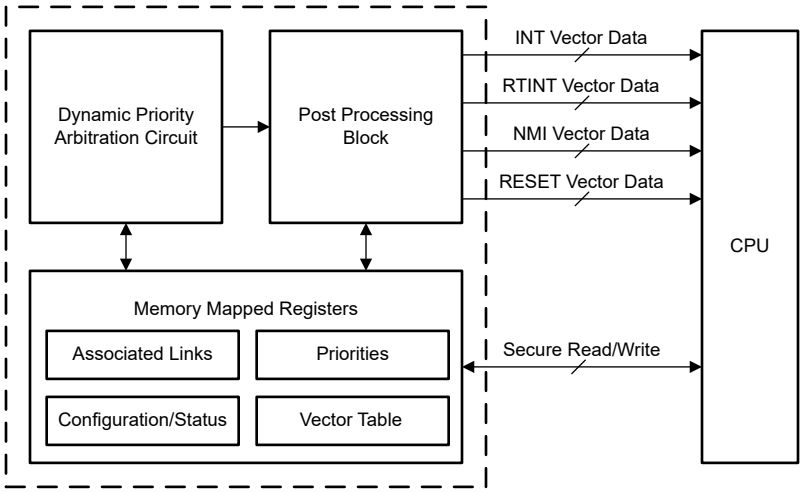

Figure 2-2. PIPE Architecture

Table 2-2. PIE vs PIPE

Feature	C28x PIE	C29x PIPE
Hardware Prioritization	No (Software only)	Yes
Hardware Arbitration	No (Software only)	Yes
Hardware Nesting	No	Yes (can block using groups)
Peripheral Interrupt Type	1	2 (RTINT/INT)
Stack Overflow Tracking	No	Yes
Peripheral Interrupt Count	192 (on most devices)	256

2.1.2 Safety and Security Module (SSU)

The Safety and Security Unit (SSU) acts as a firewall between the C29 CPUs and the memory and peripherals. The primary role of the SSU is to enforce run-time safety and security protections during every CPU access to peripherals and memory on the chip. In addition, the SSU governs debug access and flash controller operations on the device.

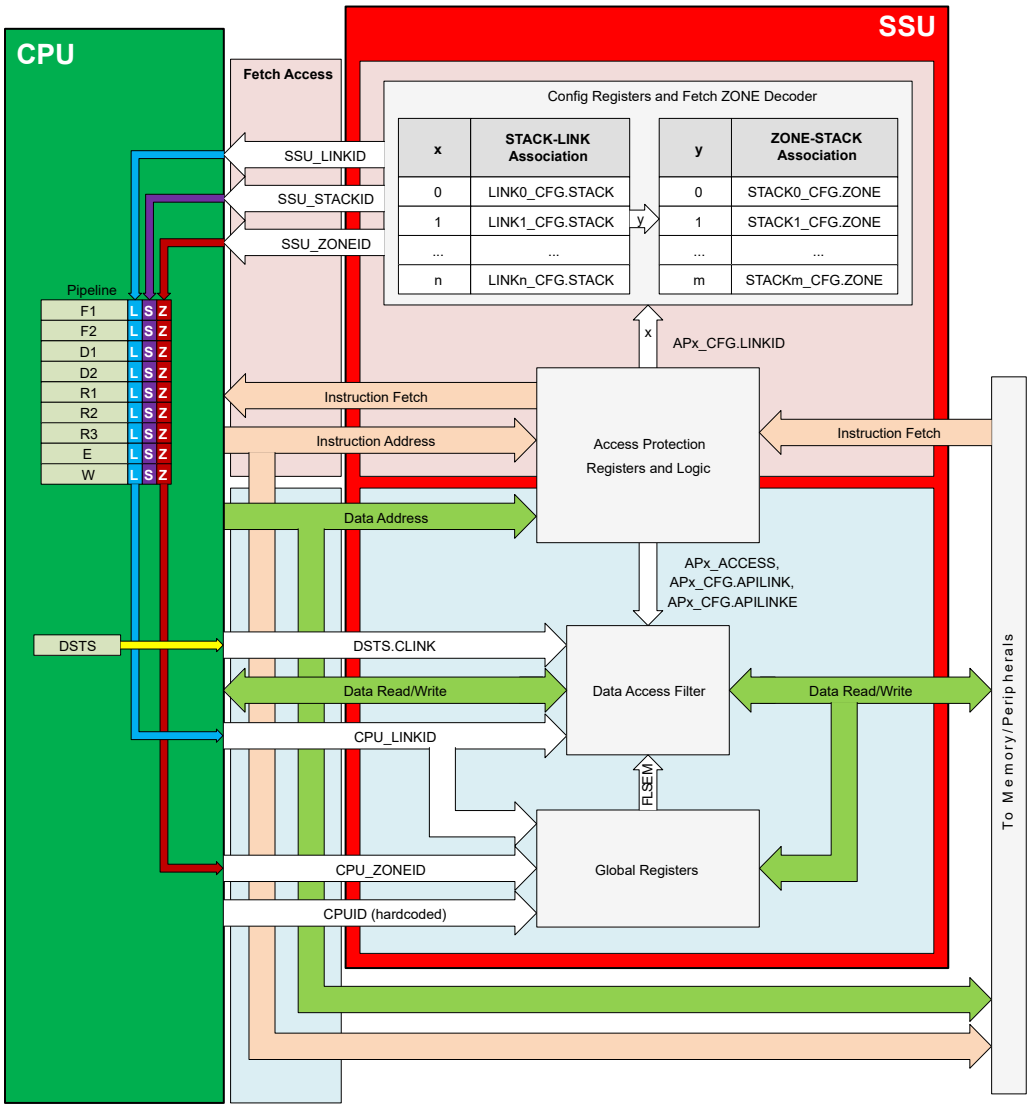

Figure 2-3. SSU-CPU Coupled Interface

2.1.3 Real-Time DMA (RTDMA)

The Real-Time (RTDMA) provides a hardware method of transferring data between peripherals and memory without intervention from the CPU in real time. Each of the (2) F29H85x RTDMA modules has ten independent, user-configurable RTDMA channels with an corresponding PIPE vector mapped interrupt to inform the CPU when a RTDMA transfer has either started or completed. All ten channels can be configured at one of four priority levels with one selected channel at a higher priority than the others. Table 2-3 shows the differences between the C28x DMA and the new C29x RTDMA. For more information, see the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual*.

Table 2-3. DMA vs RTDMA

Feature	C28x DMA	C29x RTDMA
Number of channels	(6) channels with fixed priority level	(10) channels with (4) software configurable priority levels
Burst Mode	No	Yes (for data transfer through EMIF)
Data Transfer Size	16 and 32-bit data transfers	8, 16, 32, and 64-bit data transfers
Read/Write Interface	(1) Read/Write bus – 3 cycles/word without arbitration	(2) Independent Read/Write busses – 1 cycle/word without arbitration
Trigger Source	System Level Only	System Level, Internal channel to channel linking
Safety	N/A	Integrated Memory Protection Unit configured by system level Safety and Security Unit (SSU)
Security	N/A	Integrated channel specific secure zones
Transfer Control	Linear and Circular Addressing Mode (One Shot, Continuous, Channel Interrupt)	
Level/Edge Triggers	Triggered by the edge on the trigger inputs	

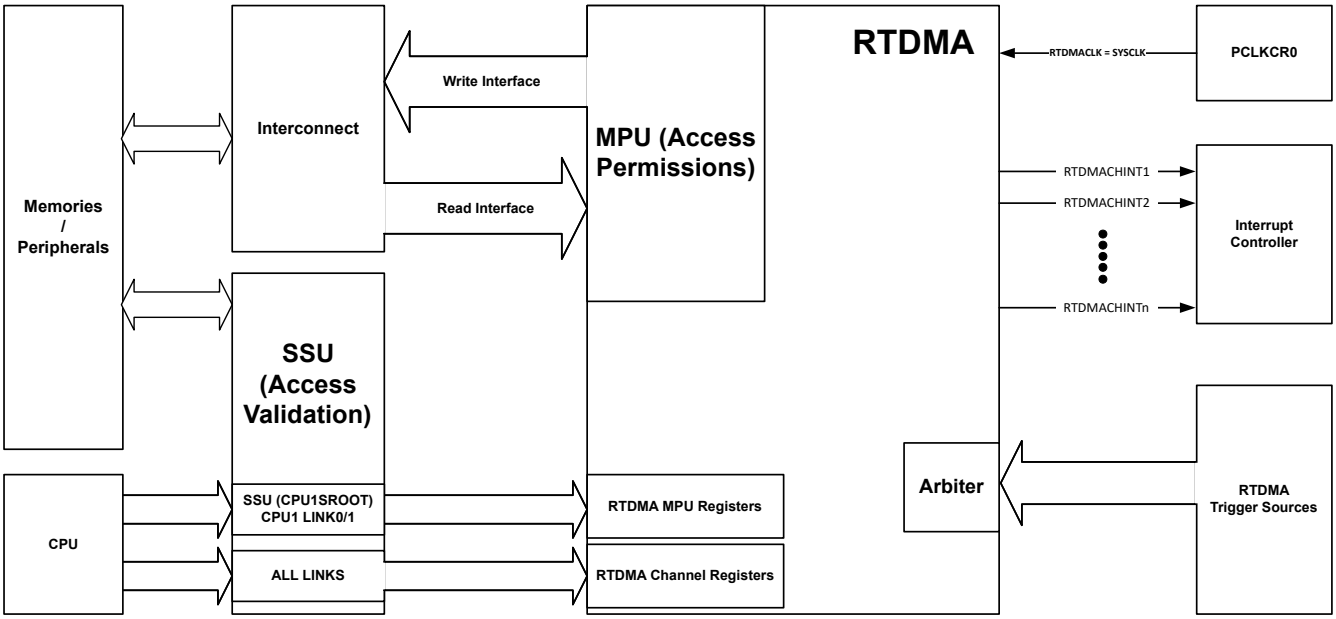

Figure 2-4. RTDMA Block Diagram

2.1.4 Lock-step Compare Module (LCM)

CPU1 and CPU2 instances, including the integrated PIPE and RTDMA will be supported by lock-step mode configuration to detect permanent and transient faults for safety-critical applications. The CPU can be configured as single module (CPU2 not present on the device) or lockstep (CPU1 and CPU2 in lockstep mode) or dual module (CPU1 and CPU2 operating as independent cores, also known as split-lock mode). The lock-step feature is only available on certain device variants. For the device variants that can support lock-step, see the *Device Comparison* table in the device-specific data sheet. For the full details of the *Lock-step Comparator Module* section, see the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual*.

There are several IPs that are covered by LCM:

- C29 CPU Subsystem (Includes C29x CPUs, PIPE, Timer, ERAD, and DLT)
- RTDMA

Table 2-4. Lockstep Module CPU Configuration

CPU1 and CPU2	CPU1	CPU2
Single Core	Available	Clock Gated
SL (Split-lock)	Independent Core	Independent Core
LS (Lock-step)	Cores operate as single CPU1 in Lock-step Mode	

2.2 C28x vs C29x Architecture Overview

C29x as a new generation CPU, there are several improvements made in architectures, which has enhanced on the efficiency and the overall performance when executing instructions. Table 2-5 shows the organized improvement in C29x. For more detailed CPU information, please refer to C2000 C29x CPU and Instruction Set.

Table 2-5. C29x Improvement

Category	C28x	C29x
Architecture	• 16-bit addressable • FPU32, FPU64 • TMU32 • NLPID • Fast Integer Division • 1x 32-bit program bus • 1x 32-bit read bus • 1x 32-bit write bus	• Very Long Instruction Word architecture (VLIW) • Byte-addressable • FPU32, FPU64 (CPU3 only) • TMU32, TMU64 (CPU3 only) • NLPID • Fast Integer Division • 1x 128-bit program bus • 2x 64-bit read bus • 1x 64-bit write bus
Parallelism	• 1 instruction per cycle • Protected pipeline (not extended to co-processors)	• Up to 8 instructions per cycle • Fully protected pipeline
Performance	-	CPU running at same frequency: • 2x to 3x signal chain performance increase (motor control, power control) • 5x faster FFT performance (system diagnostics, system tuning, arc detection) • 4x faster interrupt response and reduced latency (support for real time interrupts) • 2x to 3x improvement in general purpose code (if then else, command processing)
Interrupt	• Peripheral Interrupt Expansion (PIE) • INT, NMI • Real time interrupt latency: 40+ cycles	• Peripheral Interrupt Priority and Expansion (PIPE) • INT, RTINT, NMI • Interrupt latency: 11 cycles • Dedicated HW stack for real-time interrupt – HW saves/restores the context
Security	• Dual Code Security Module (DCSM)	• Safety and Security Unit (SSU) • Hardware Security Module (HSM)
Safety	• ASIL B • MPOST	• ASIL D • MPOST, LPOST • ECC / Parity protection for bus and registers • MPU-like SSU enables freedom from interference enabled

3 PCB Design Consideration

F29H85x has four package types (256ZEX, 176 PTS, 144RFS, and 100PZS). Due to the various enhancements in the F29H85x device series, there is no compatibility between the PCB designs. The following sections include recommendations on how to start designing a new PCB, in general.

3.1 VSSOSC

In F28P65x, the VSSOSC is used for connections for the crystal oscillator (X1 and X2) ground. If an external crystal is not used, the VSSOSC can be connected to the board ground, but is not required.

In F29H85x, the VSSOSC must be grounded, so that VSSOSC and VSS are on the same plane, for proper device operation.

3.2 JTAG

The JTAG architecture from F28P65x to F29H85x remains the same except for one functional difference. Both devices support the same 4-wire (JTAG protocol). For 2-wire mode, F29H85x only supports the Serial Wire Debug (SWD) Protocol while F28P65x only supports cJTAG (compact JTAG).

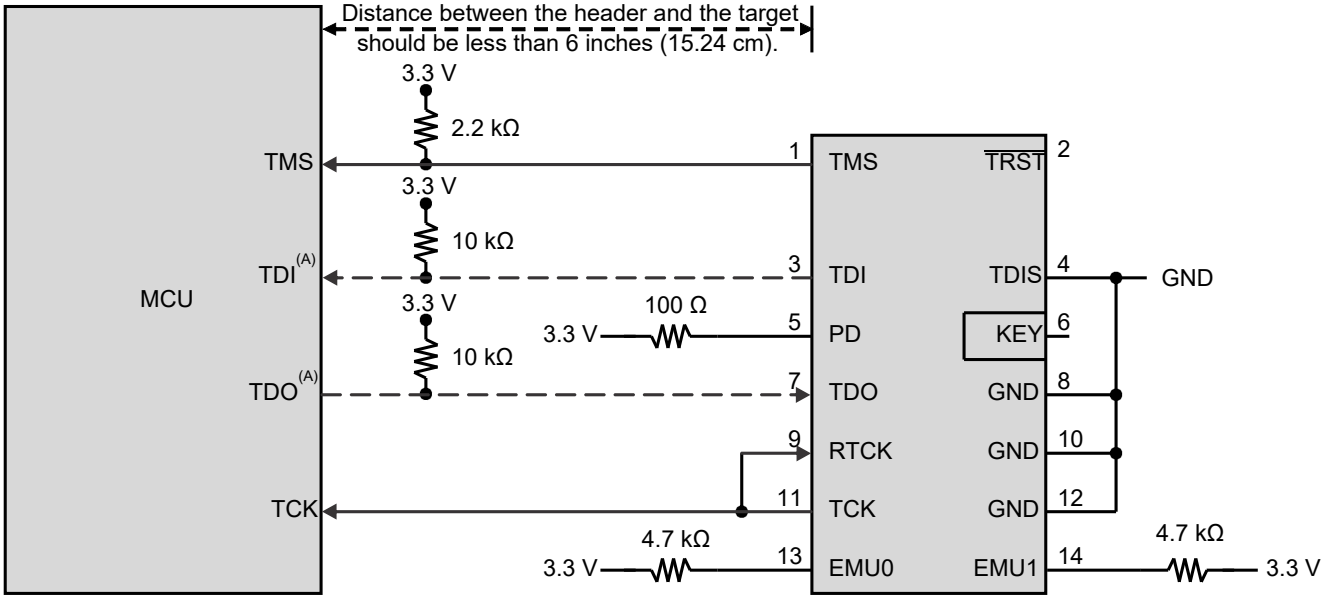

Figure 3-1. JTAG Connection Diagram (Connecting to 14-Pin JTAG Header)

3.3 VREF

F29H85x has two dedicated VREFHI pins. One is for both ADCA and ADCB (12-bit/16-bit ADCs) and the other is for ADCC, ADCD, and ADCE (12-bit ADCs). These VREFHI pins should not be tied together but instead be supplied independently to minimize coupling between the different ADC types and modes of operation to achieve optimum performance.

In addition, it is important to keep low inductance connections in the reference path allows the reference driving circuit to remain stable and settled during the conversion phase.

4 Feature Differences for System Consideration

This section showcases the similarities and differences in features when moving between the F28P65x and F29H85x devices.

Table 4-1. Main Changes in F29H85x

Category	Peripheral Information
CPU Subsystem	C29x CPU Section 2.1
Memory	RAM Section 4.6
	FLASH Section 4.6
System	Peripheral Interrupt Priority and Expansion (PIPE) Section 2.1.1
	Data Logger and Trace (DLT) Section 4.1.2
	Real-Time DMA (RTDMA) Section 2.1.3
	BOOTROM Section 4.1.6
	Enhanced Real-Time Analysis and Diagnostic (ERAD) Section 4.1.7
	Crossbar (XBAR) Section 4.1.8
Analog	Analog Subsystem Section 4.1.1
Control	Enhanced Pulse Width Modulator (EPWM) Section 4.1.5
Communication	Single Edge Nibble Transmission (SENT) Section 4.1.3
Safety and Security	Waveform Analyzer Diagnostics (WADI) Section 4.1.4
	Error Signaling Module (ESM) Section 4.1.9
	Safety and Security Module (SSU) Section 2.1.2
	Hardware Security Module (HSM) Section 4.1.11
	Cryptographic Accelerators Section 4.1.11.1: • Symmetric Cryptography • Asymmetric Cryptography • Hashing Function
	Safe Interconnect End-to-End Safing Section 4.1.12
	MMR Safing with Parity Section 4.1.13
	Logic Power-On Self-Test (LPOST) Section 4.1.14

4.1 New Features in F29H85x

This section outlines new features introduced in the F29H85x device series. For more information, see the *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual*..

4.1.1 Analog Subsystem

From F28P65x to F29H85x, the number of ADCs has increased from 3 to 5 along with the SOC doubling from 16 to 32. Within these 5 ADCs, two of them are 12-bit and 16-bit selectable, and three of them are 12-bit only. The ADC has been enhanced with capability of hardware oversampling and undersampling.

The PPB block has also been updated with aggregation features in hardware to support data processing for oversampling and undersampling which would otherwise require software running in lengthy repetitive loops. When the PPB delta is enabled, the ADC automatically calculates the delta between the current conversion and the last conversion for that SOC. This can speed up control loop computations in certain cases. PPB digital filter is a windowed filter can now be configured for the limit compare and zero-crossing logic in the PPB. This filter works just like the digital filter in the CMPSS, to prevent false events. Limit compare/zero-crossing can be used to generate events e.g. to trip the PWM.

4.1.2 Data Logger and Trace (DLT)

The Data Logger and Trace (DLT) module has the ability to control what data gets logged, when to start data-logging, and how much data to data-log for critical CPU run-time content. Critical run-time content can include any information that needs to be monitored as the content is computed. When data-logging, the DLT is non-intrusive meaning there is no impact to run-time or CPU core behavior. The ability to view intermediate values of computation in a critical task, such as a control loop, can help users fine-tune the loop. The DLT module can generate interrupts to the interrupt controller, issue DMA transfer requests, and interact with ERAD event triggers. The DLT makes it possible to collect, time-stamp, pre-filter, export, and do real-time and post analysis of data.

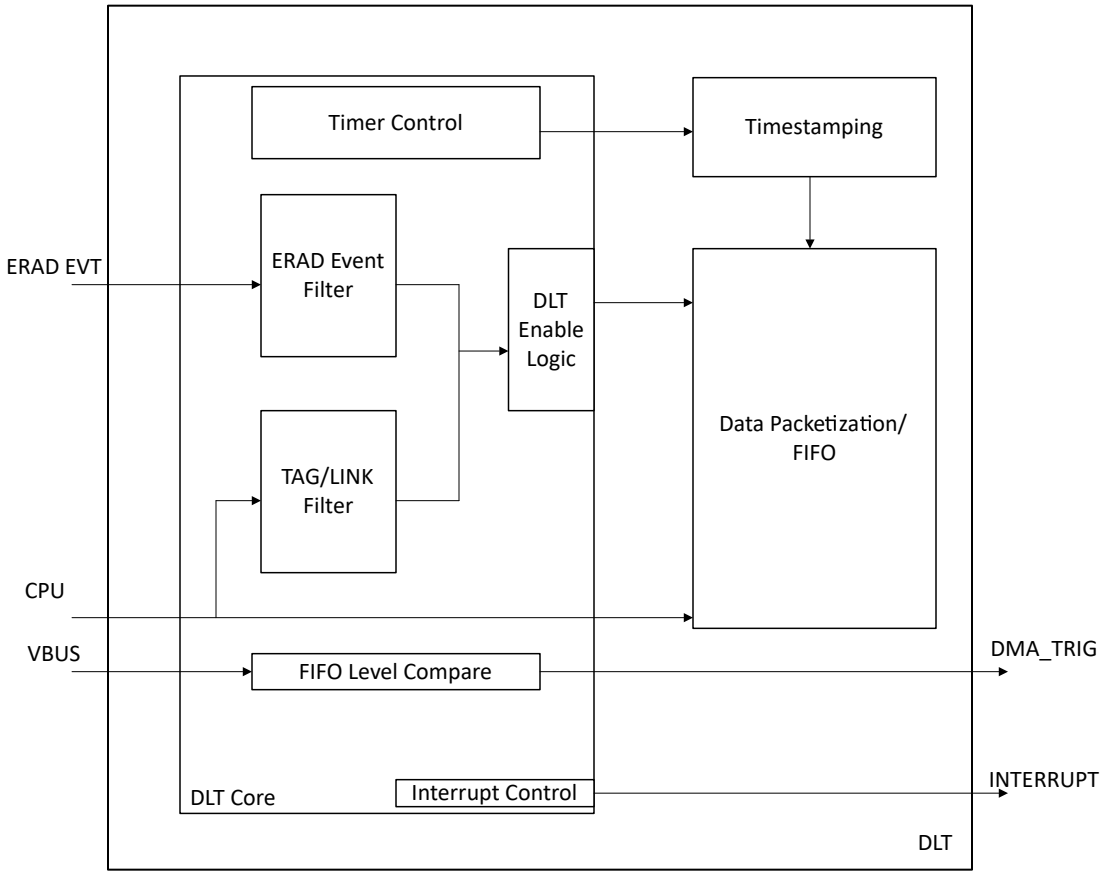

Figure 4-1. DLT Block Diagram

4.1.3 Single Edge Nibble Transmission (SENT)

In F29H85x, SENT module for communication has been added. The SENT protocol is unidirectional and uses single wire between two or more points to transmit signals from one or more sensors to a controller. SENT uses an open standard SAE J2716 released by the Society of Automotive Engineers (SAE), and is mainly used for automotive applications. This protocol can transmit high resolution data at a low cost to the system. The SENT module utilizes a Master Trigger Pulse Generator to control and receive data from one or more sensors, using a configurable pulse signal. The received data can be stored directly into memory or a FIFO and read by the CPU or DMA.

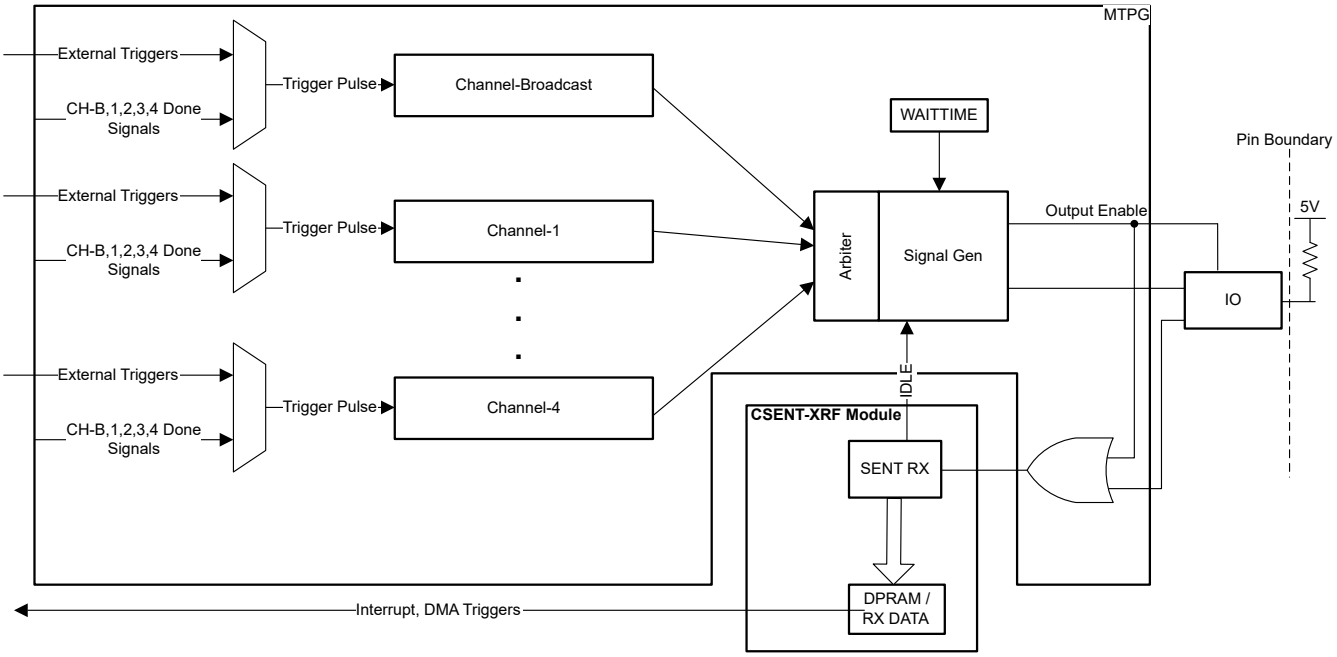

Figure 4-2. SENT Block Diagram

4.1.4 Waveform Analyzer Diagnostic (WADI)

The WADI blocks analyze signal waveforms and characterize pulse width, frequency, dead-band, phase shift. If the signal waveforms are analyzed to be incorrect, it creates a sequence of events to drive the signals to a safe state. WADI is primarily used for safety applications, where deviant waveforms applied to power switches can be detected and corresponding course of action can be either taken by WADI or MCU subsystem. Each WADI block can perform comparison between two signals and have the override capabilities of the signals. Safety mechanisms of WADI can be tuned with appropriate Safe State Sequencer (SSS) configurations. SSS creates a safe sequence of chained events depending on the signals. Both the fail operational as well as fail safe solutions can be implemented as per application need and available resources.

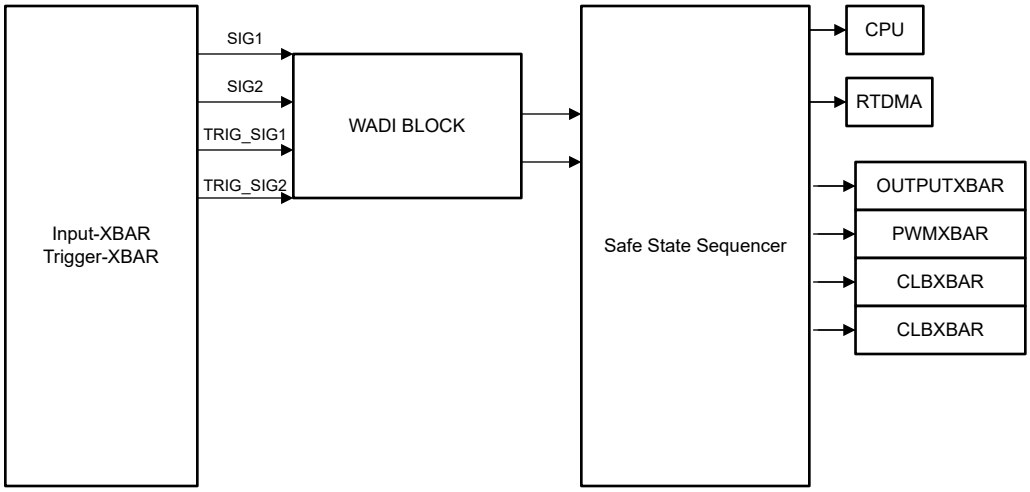

Figure 4-3. WADI Block Diagram

4.1.5 EPWM

There is now a dedicated XLINK region in the memory map to support writes to any of the ePWM registers to reflect in other ePWM instances

In addition, the HRPWM's resolution in F28P65x has been with 150ps delay-line, and now in F29H85x, that is being supported with 75ps delay-line.

4.1.6 Bootrom

For bootrom differences between F28P65x and F29H85x see Table 4-2.

Table 4-2. Bootrom Comparison

Module	F28P65x	F29H85x
ROM Memory	Standard and secure bootrom	Start at 0x00000000 and is divided into Reset vector, NMI vector, LINK0, User tables and LINK1
Security Module	DCSM initialization done through dummy reads	SSU initialization, no dummy reads
MPOST	Can execute at 150MHz, 75MHz PLL output clock as well as INTOSC clock	MPOST and LPOST are performed by HSM and not by CPU1
PLL	Option to enable/disable PLL during bootrom execution	PLL is enabled by HSM, and CPU1 runs at PLL clock
Watchdog Timer	Disabled by default	Enabled by default
Error Status Pin	GPIO configured as Error Status Pin	GPIO configured as Error Status Pin and ESM configuration to influence error status pin
Peripheral Bootloaders	Executed at bypass clock	Executed at PLL clock

Table 4-2. Bootrom Comparison (continued)

Module	F28P65x	F29H85x
Peripheral Boot Modes Supported	CAN, MCAN, I2C, SPI, SCI, USB, GPIO	CAN, MCAN, I2C, SPI, UART-HS, GPIO
Critical Trim Loading Method	Bootrom loads	Hardware CTL module loads
Bootload Image Format	Key followed by image data organized into blocks	X509 certificate followed by the image data
Boot Process	Involves downloading of image from peripheral	Involves handshaking with HSM for X509 certificate and image sharing with HSM for integrity check or authentication
IPC	IPC is based on C2000 IPC interface	IPC between CPU1 and HSM is heterogeneous involving C2000 IPC interface on CPU1 and Mailbox based interface on HSM
NMI	NMI is enabled at a later point in the boot flow	NMI is enabled by default throughout the boot flow
OTP	Single user OTP available	Dual SECCFG sectors are available
Lockstep	Lockstep is disabled during boot flow	Lockstep is enabled during boot flow

4.1.7 ERAD

C29 Embedded Real-time analysis and Diagnostics (ERAD) block is mainly comprised of two major blocks to aid with debug and system analysis capabilities. This is primarily tied to the C29 CPU and these capabilities can be used either with the debugger connected or as part of real-time application too. The two main components are the enhanced bus comparator (EBC) and the system event counter block (SEC), with an optional PC trace module.

ERAD can generate hardware breakpoints, watch points, interrupts or just a trigger output to be used by other resources like profiling counters and configurable logic block (CLB).

ERAD can be used for various types of system scenarios like counting of system events (like interrupts, critical system events and so forth), measuring minimum and maximum time taken between a pair of events measured over multiple iterations, and so forth.

Program Counter trace block helps keep track of PC discontinuity/jumps, which can in turn help track the complete sequence of software that got executed at any given point of time.

4.1.8 XBAR

The crossbars (XBAR) provide flexibility to connect device inputs, outputs, and internal resources in a variety of configurations. F29H85x contains several XBARs, including Input X-BAR, Output X-BAR, CLB X-BAR, ePWM X-BAR, MINDB X-BAR, and ICL X-BAR. In F29H85x, there is an architectural improvement compared to F28 family. Figure 4-4 shows that the input signals are directed into a MUX, where users can only choose one input within the same MUX. However, Figure 4-5 shows that the inputs are grouped (G0...Gx) instead of muxed, which solves the scenario when users want to select multiple inputs within the same group. Now, they can enable any combination of inputs, even if they are within the same group, to be ORed together to produce the output signal of the X-BAR. This architecture is used across all XBAR modules with the exception of Input X-BAR, which has the same architecture as C28 Input X-BAR.

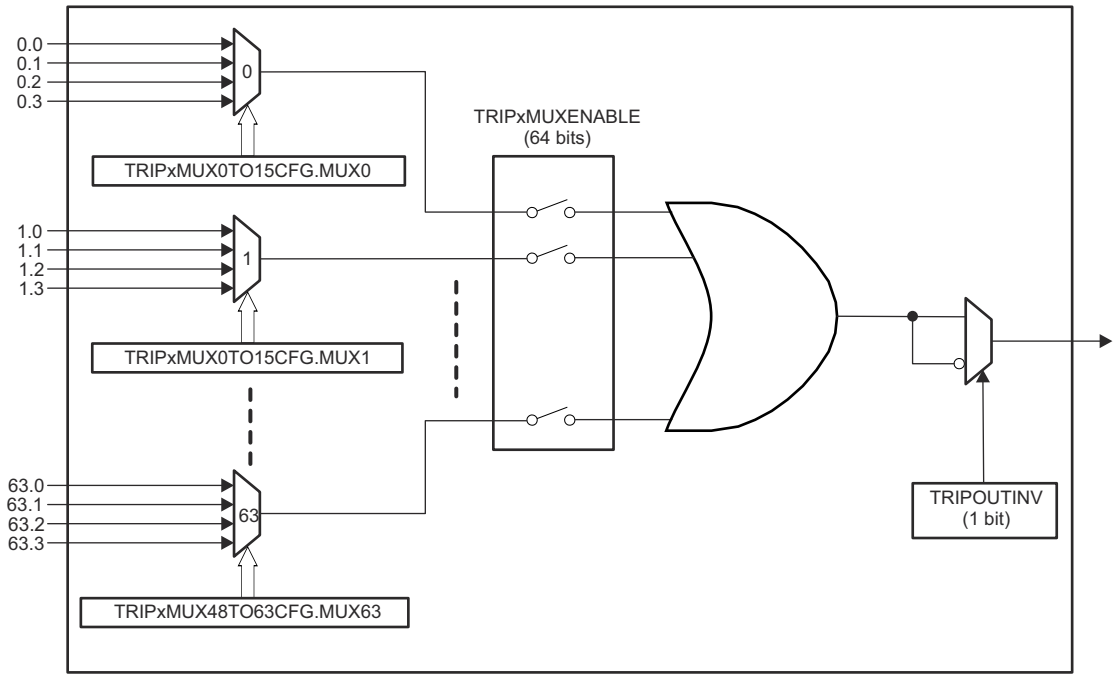

Figure 4-4. F28P65x ePWM X-BAR Architecture

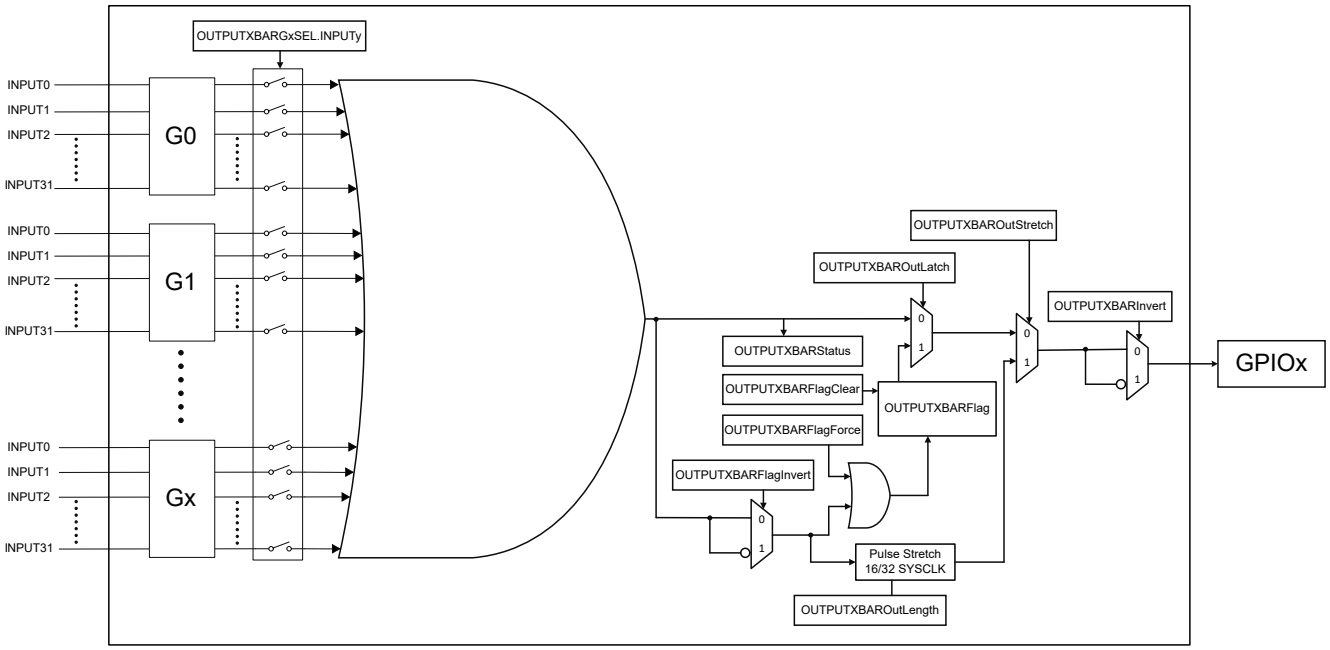

Figure 4-5. F29H85x ePWM X-BAR Architecture

4.1.9 Error Signaling Module (ESM)

The Error Signaling Module (ESM) provides a systematic consolidation of responses to error events throughout the device into one location. The error classification in the ESM is determined by programmed configuration for each individual error input. The module can signal high or low priority interrupts to the processor to respond to an error event and/or manipulate an I/O error pin to signal an external hardware that an error has occurred. This external controller is then able to reset the device and/or keep the system in a safe, known state.

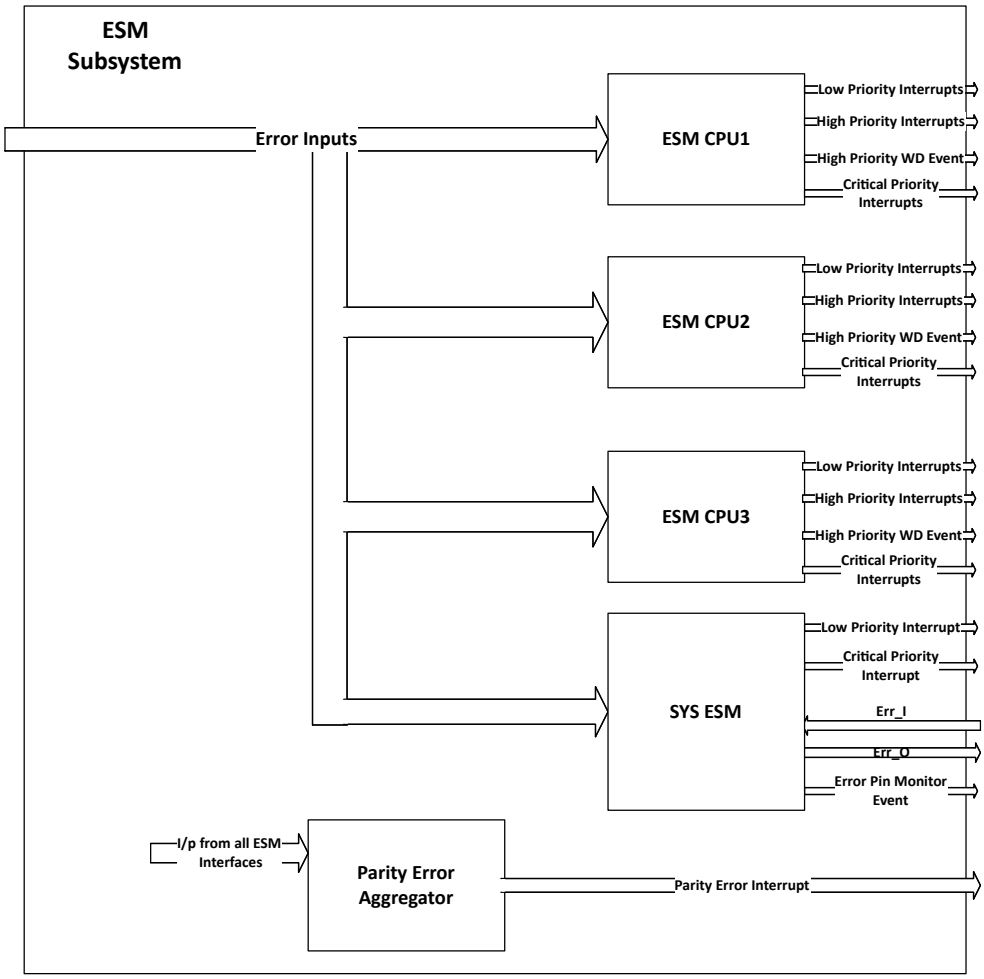

Figure 4-6. ESM-SS Block Diagram

4.1.10 Error Aggregator

The error aggregator is an interface module between certain peripherals that generate specific errors including the C29, RTDMA, Memory controllers, Peripheral bridges, Read Interfaces and ESM. Main purpose of the Error Aggregator is to accumulate various errors from various sources and provide aggregated error output to ESM module. The module also logs the error status, error address and error type information while segregating high priority errors and low priority errors for ESM to generate appropriate action to alert CPU.

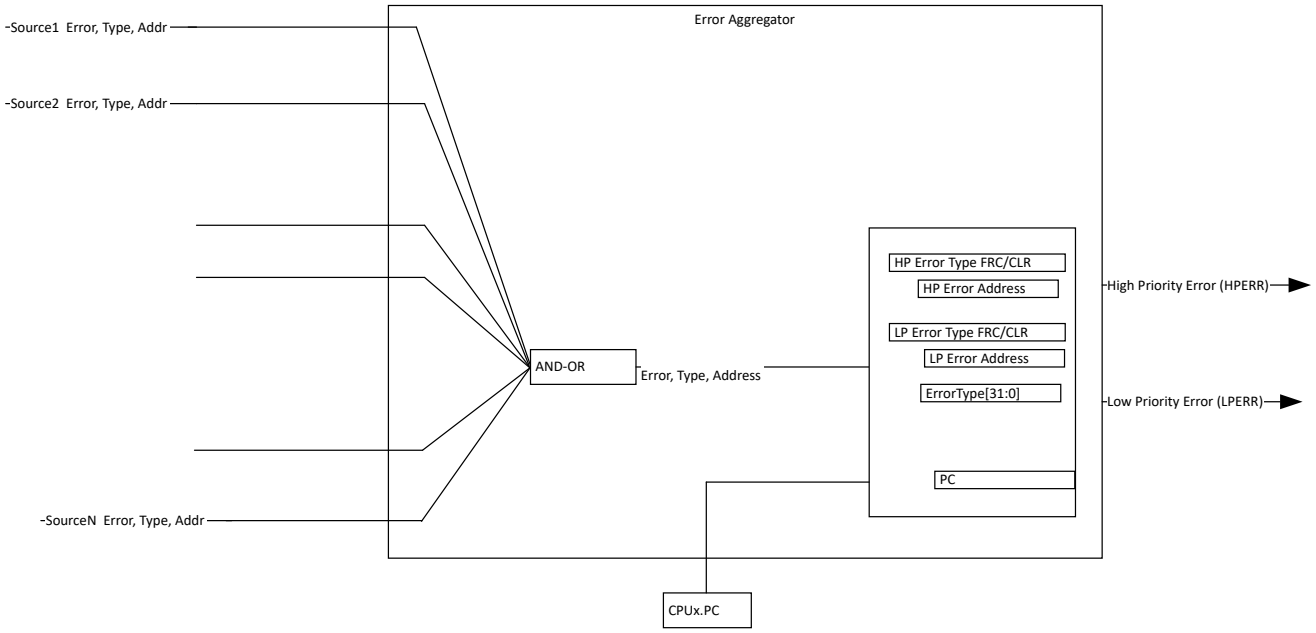

Figure 4-7. Error Aggregator Block Diagram

4.1.11 Hardware Security Module (HSM)

The Hardware Security Module (HSM) is a self-contained subsystem within the device that provides security and cryptographic functions. The host C29 subsystem interfaces with the HSM subsystem to perform the cryptographic operations required for code authentication, secure boot, secure firmware upgrades, secure debug, and encrypted run-time communications. The HSM also includes several hardware accelerators to efficiently execute key cryptographic algorithms. These engines are described in the Table 4-3.

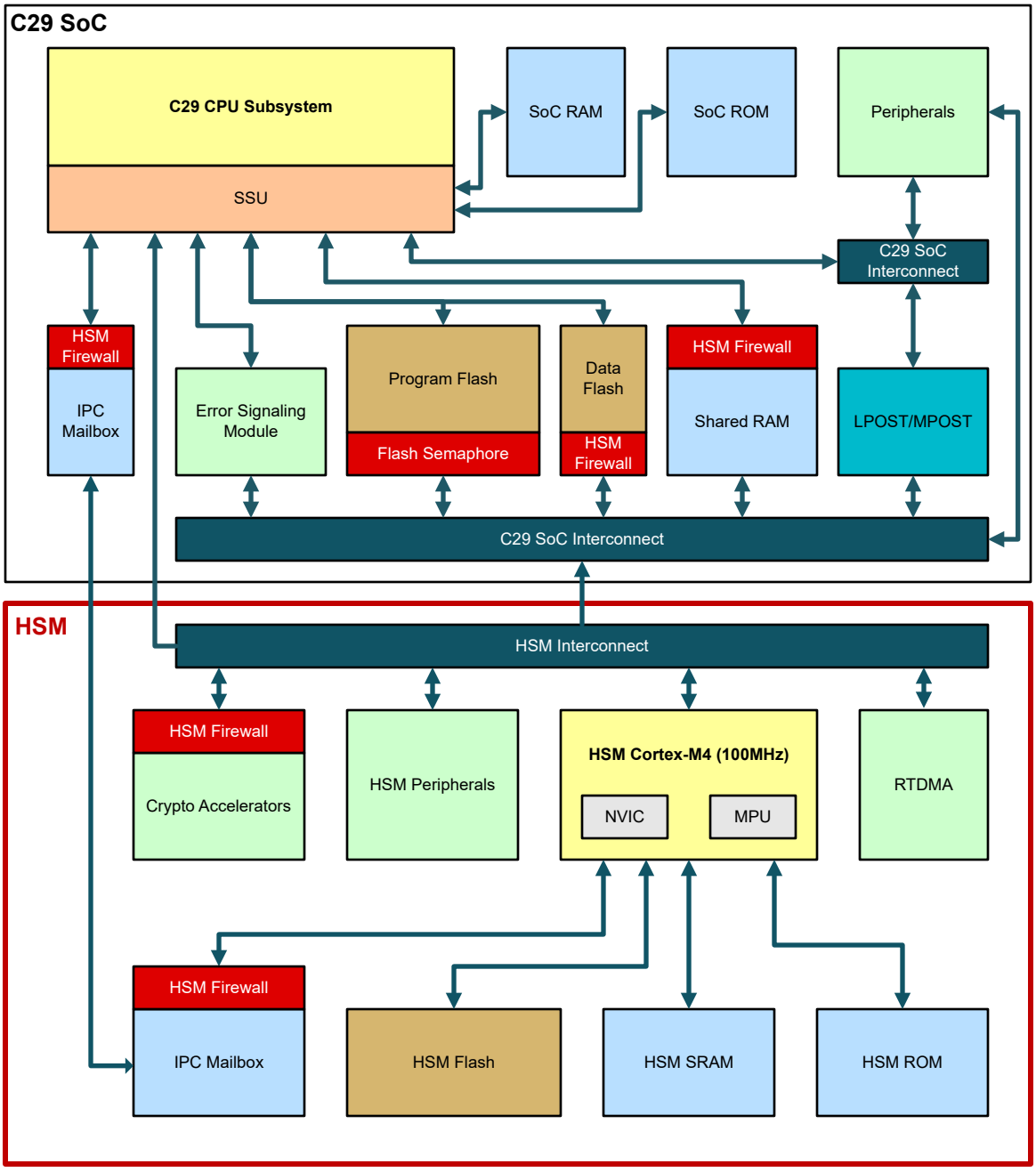

Figure 4-8. Device High-Level Block Diagram

4.1.11.1 Cryptographic Accelerators

Table 4-3. List of Cryptographic Accelerator Engines

Type of Cryptography	Cryptographic Engine	Feature Supported	
Symmetric Cryptography	AES	Symmetric Algorithms: AES-128, AES-192, AES-256 Cipher Modes: ECB, CTR, CBC, GCM Authentication: CBC-MAC, CMAC	
	SM4	Symmetric Algorithms: SM4	
Asymmetric Cryptography	PKE	High-performance PKE (Public Key Engine) for large-vector math/modulus operation Asymmetric Algorithms: RSA-2048, RSA-3092, RSA-4096, ECC (Curve25519, X25519, SecP256r1, SecP256k1, SecP384k1, Brain Pool, and more), SM2 Side-channel protection (DPA, FIA)	
Hashing Function	Hashing Engine	HMAC	Hash Algorithms: SHA-256, SHA-384, SHA-512 Keyed Hashing: HMAC-SHA256, HMAC-SHA512
		SHA	
		MD5	
	SM3	Hash Algorithms: SM3 (256 bits, 384 bits, 512 bits)	

4.1.12 Safe Interconnect End-to-End (E2E) Safing

The Safe Interconnect mechanism detects any faults that occur in the bus interconnect on the F29H85x. The bus interconnect includes C29 buses (control and data), address decodes, memory controllers, and peripheral bridges. Any data corruption in memory is detected and this is achieved by storing ECC along with data in memory. To achieve safe interconnect, there are checks that are implemented inside and outside the CPU.

4.1.13 Critical MMR Safing With Parity

Parity detection identifies single bit errors in a read access. The parity circuitry sets the parity bits when the location of the byte is written and verifies that there are no single bit errors in the word when it is read back. This is done during each read and write cycles, so no CPU overhead is involved. When the parity circuitry identify an error, it generates a high priority interrupt to the CPU.

The IPs covered by MMR Safing with Parity include the following:

- ADC
- Analog Subsystem
- ESM
- Error Aggregator
- Flash
- LCM
- LPOST
- PIPE
- SYSCTRL
- WADI

4.1.14 LPOST

F29H85x introduces the Logic Power-On Self-Test (LPOST) which addresses the start-up logic self-test requirements for functional safety applications. Coverage is configurable (60%, 80%, 90%) based on the application requirements. The higher the coverage required, the higher will be the impact on boot time. The LPOST test is triggered through software on power-up and/or during functional operation. Once the test is initiated, the device will enter scan test mode, perform the logic self-test, logs the status of the test, enter functional mode and issue a chip to reset. The reset issued after LPOST clears up any random data shifted in by the scan operation.

For power-on self-test, application code does not need to invoke the test. The test will be invoked by the Boot-ROM based on the OTP configuration. Upon completion of the boot process and test status, the application needs to take the appropriate safety action.

Note

All analog modules (except the ones required for the POST execution) shall be powered down during test.

4.2 Communication Module Changes

Communication module changes between the F28P65x and F29H85x devices affect the number of modules and migration. Module functionality is mostly maintained between both devices. Table 4-4 shows the module instances and major register differences which should be considered when migrating applications between F28P65x and F29H85x.

Table 4-4. Communication Module Instances

Module	Category	F28P65x	F29H85x	Notes
SCI	Number	2 - SCIA, SCIB	Not Present	
I2C	Number	2 - I2CA, I2CB		
LIN	Number	2 - LINA, LINB		
CAN	Number	1 - CANA	Not Present	
CAN-FD	Number	2 - MCANA, MCANB	6 - MCANA, MCANB, MCANC, MCAND, MCANE, MCANF	
SPI	Number	4 - SPIA, SPIB, SPIC, SPID	5 - SPIA, SPIB, SPIC, SPID, SPIE	
PMBUS	Number	1 - PMBUSA		
EMIF	Number	1 - EMIF1		
USB	Number	1 - USBA	Not Present	
ECAT	Number	1- ECATA		
SENT	Number	Not Present	6 - SENTA, SENTB, SENTC, SENTD, SENTE, SENTF	
UART	Number	2 - UARTA, UARTB	6 - UARTA, UARTB, UARTC, UARTD, UARTE, UARTF	
	Registers	-	GLB_INT_CLR	UART Global Interrupt Clear Register
		-	GLB_INT_EN	UART Global Interrupt Flag Register
		-	GLB_INT_FLG	UART Global Interrupt Flag Register
FSI	Number	4 - FSIRXA..D,2 - FSITXA, FSITXB		

4.3 Control Module Changes

There are changes in the control modules between the F28P65x and F29H85x devices. The biggest changes come from the EPWM and ECAP on the F29H85x device. Table 4-5 shows the module instances differences that should be considered when migrating applications between F28P65x and F29H85x.

Table 4-5. Control Module Differences

Module	Category	F28P65x	F29H85x	Notes
SDFM	Number	16 - SD1_D1C1..D4C4, SD2_D1C1..D4C4, SD3_D1C1..D4C4,SD4_D1C1..D4C4		
	Registers	-	SDINTMODE	SD Interrupt Mode register
eQEP	Number	6 - EQEP1..6		
eCAP	Number	7 - ECAP1..7	6 - ECAP1.. 6	
	Registers	-	HRCALPRD	High-Res Calibration Period Register
		-	HRCLKCAP	High-Res Calibration HRCLK Capture Register
		-	HRCLKCTR	High-Res Calibration HRCLK Counter Register
		-	HRCLR	High-Res Calibration Interrupt Clear Register
		-	HRCTL	High-Res Control Register
		-	HRFLG	High-Res Calibration Interrupt Flag Register
		-	HRFRC	High-Res Calibration Interrupt Force Register
		-	HRINTEN	High-Res Calibration Interrupt Enable Register
		-	HRSYSCLKCAP	High-Res Calibration SYSCLK Capture Register
		-	HRSYSCLKCTR	High-Res Calibration SYSCLK Counter Register
HRCAP	Number	2 - HRCAP6, HRCAP7	2 - HRCAP5, HRCAP6	
ePWM	Number	18 - EPWM1..18		
	Registers	XLINK	-	EPWMx Link Register (Present in SysCtl registers in F29H85x)
		XLINK2	-	EPWMx Link 2 Register (Present in SysCtl registers in F29H85x)
HRPWM	Number	18 - HRPWM1..18		

4.4 Analog Module Differences

This section outlines the analog differences between F28P65x and F29H85x. The ADC on F29H85x has a lot of new features compared to the ADC on F28P65x. Table 4-6 shows the differences.

Table 4-6. Analog Module Differences

Module	Category	F28P65x	F29H85x	Notes
ADC	Number	3 - ADCA to ADCC	5 - ADCA to ADCE	
	Registers	-	PPBTRIP1FILCLKCTL	ADCEVT1 Trip High Filter Prescale Control
		-	PPBTRIP1FILCTL	ADCEVT1 Trip High Filter Control Register
		-	PPBTRIP2FILCLKCTL	ADCEVT2 Trip High Filter Prescale Control
		-	PPBTRIP2FILCTL	ADCEVT2 Trip High Filter Control Register
		-	PPBTRIP3FILCLKCTL	ADCEVT3 Trip High Filter Prescale Control
		-	PPBTRIP3FILCTL	ADCEVT3 Trip High Filter Control Register
		-	PPBTRIP4FILCLKCTL	ADCEVT4 Trip High Filter Prescale Control
		-	PPBTRIP4FILCTL	ADCEVT4 Trip High Filter Control Register
		-	RESULT16	ADC Result 16 Register
		-	RESULT17	ADC Result 17 Register
		-	RESULT18	ADC Result 18 Register
		-	RESULT19	ADC Result 19 Register
		-	RESULT20	ADC Result 20 Register
		-	RESULT21	ADC Result 21 Register
		-	RESULT22	ADC Result 22 Register
		-	RESULT23	ADC Result 23 Register
		-	RESULT24	ADC Result 24 Register
		-	RESULT25	ADC Result 25 Register
		-	RESULT26	ADC Result 26 Register
		-	RESULT27	ADC Result 27 Register
		-	RESULT28	ADC Result 28 Register
		-	RESULT29	ADC Result 29 Register
		-	RESULT30	ADC Result 30 Register
		-	RESULT31	ADC Result 31 Register
		-	SAFECHECKRESEN2	ADC Safe Check Result Enable 2 Register
		-	SOC16CTL	ADC SOC16 Control Register
		-	SOC17CTL	ADC SOC17 Control Register
		-	SOC18CTL	ADC SOC18 Control Register
		-	SOC19CTL	ADC SOC19 Control Register
		-	SOC20CTL	ADC SOC20 Control Register
		-	SOC21CTL	ADC SOC21 Control Register
		-	SOC22CTL	ADC SOC22 Control Register
		-	SOC23CTL	ADC SOC23 Control Register
		-	SOC24CTL	ADC SOC24 Control Register
		-	SOC25CTL	ADC SOC25 Control Register
		-	SOC26CTL	ADC SOC26 Control Register
		-	SOC27CTL	ADC SOC27 Control Register
		-	SOC28CTL	ADC SOC28 Control Register
		-	SOC29CTL	ADC SOC29 Control Register
		-	SOC30CTL	ADC SOC30 Control Register
		-	SOC31CTL	ADC SOC31 Control Register

Table 4-6. Analog Module Differences (continued)

Module	Category	F28P65x	F29H85x	Notes
Analog Subsystem	Register	-	AGPIOCTRLH	AGPIO Control Register
		-	CTLTRIMSTS	HWCTL TRIM Error Status register
		-	CTLTRIMSTSCLR	HWCTL TRIM Error Status CLEAR register
		-	INTERNALTESTCTL	INTERNALTEST Node Control Register
		-	IODRVSEL	5V FS IO Drive strength select register
		-	IOMODESEL	PMBUS IO Mode select register
		-	PARITY_TEST	Enables parity test
		-	PARITY_TEST_ALT1	Enables parity test
		-	PMMVREGTRIM	Power Management Module VREG Trim Register
		-	REFBUFCONFIGCDE	Config register for analog reference CDE
		-	VREGCTL	Voltage Regulator Control Register
		ADCACLOOPBACK	-	Enable loopback from DAC to ADCs
		AGPIOCTRLG	-	AGPIO Control Register
		GPIOINENACTRL	-	GPIOINENACTRL Control Register
DAC	Number	2 - GPDACA, GPDACC		
CMPSS	Number	11 - CMPSS1 to CMPSS11	12 - CMPSS1 to CMPSS12	
Temp Sensor	Number	1 - (in ADCB ch 18)	1	

4.5 Power Management

F28P65x has two options to supply power to the device. All packages can operate with a dual-rail supply (3.3 V and 1.2 V) or single-rail supply (3.3 V) with the internal LDO VREG enabled.

In F29H85x, all pin packages support dual-rail supply (3.3 V and 1.25 V), but only the 100-pin package supports the single-rail supply (3.3 V) with the internal LDO VREG enabled.

This section describes the power management differences and similarities between the two devices.

4.5.1 VREGENZ

Only the F29H85x 100-pin package supports the VREG mode where power is internally generated from the single-rail supply rail. For other package types, the dual-rail supply is required to power up the device.

Note

In general, the Internal and External VREG power sequencing detailed in the device-specific data sheet needs to be followed to start up the device properly.

4.5.2 Power Consumption

Total power for F28H85x is 1.8W where as F28P65x was 1.15kW. Power consumption is higher on F29H85x due to increased amount of resources on this devices such as CPUs (1-3 C29x depending on the package, Cortex M4) as well as larger memory which consume more current.

4.6 Memory Module Changes

As the whole architecture, RAM and FLASH memories have changed from F28P65x and F29H85x. Table 4-7 summarizes the memory features including error-checking and security assignment, and the different modes in flash.

Table 4-7. RAM and Flash Memory Changes

Memory	F28P65x			F29H85x		
RAM and Flash	**Size**	**Parity/ECC**	**Secured**	**Size**	**Parity/ECC**	**Secured**
Dedicated RAM	104KB	Parity		4K	ECC	
Local Shared RAM	64KB	Parity		N/A		
Global Shared RAM	80KB	Parity				
Program Memory (LPAx, CPAx)	N/A			128KB	ECC	
Data Memory (LDAx, CDAx)				320KB	ECC	
Message RAM (CPU1,2,CM,CLA,& DMA)	5KB	Parity		N/A		
Total RAM	**249KB**			**452KB**		
Per CPU Bank	256KB (5 banks mappable between 2 C28 CPUs)	ECC	DCSM-controlled	512KB (8 banks mappable between 3 CPUs)	ECC	
Data Bank	N/A			256KB	ECC	
HSM Firmware				2*256KB	ECC	
Total Flash	**1.28MB**			**4.75MB**		

In F29H85x, the architecture of the memory has changed. Every memory can be accessed by every CPU, but there are categorized and optimized sections of the RAM for better efficiency. There are program-optimized sections, LPAx and CPAx, while LPAx is optimized for CPU1/CPU2 and CPAx is optimized for CPU1/CPU3. Similarly, there are data-optimized sections with CPU1/CPU2 optimized (LDAx) and CPU1/CPU3 optimized (CDAx). In F28P65x, there is message RAM, and you do not see message RAM in F29H85x, but any memory can be used as CPU message RAM in our new device. It can be created out of the RAMS along with SSU.

The 128-bit memory controller enables zero wait states on program accesses. This allows data accesses, providing the ability to copy code, download code, and insert software breakpoints, which also utilize maximum parallelism of the CPU. The 64-bit LDx and CDx memory controller is similar to the 128-bit LPx and CPx memory controller, but the 64-bit memory controller has zero wait states on data access and one wait state on program access. Furthermore, RTDMA is connected through a slow access port, so all accesses are minimum one wait state. With RTDMA burst support, RTDMA supports local address generation within the MEMSS memory controller. This enables performance close to zero wait states.

Table 4-8. Memory Configuration

RAM Section	Interleaved	CPU1	CPU2	CPU3	HSM	RTDMA1	RTDMA2
LPAx RAM	Yes	0WS program 1WS data	0WS program 1WS data 1WS data	3WS data		1WS	1WS
LDAx RAM	Yes	1WS program 0WS data	1WS program 0WS data	3WS data	2WS	1WS	1WS
M0 RAM	Yes	1WS program 0WS data	1WS program 0WS data	3WS data		1WS	1WS
CPAx RAM	Yes	0WS program 1WS data	3WS data	0WS program 1WS data		1WS	1WS
CDAx RAM	Yes	1WS program 0WS data	3WS data	1WS program 0WS data		1WS	1WS
CPU1 ROM	Yes	1WS program 1WS data					
CPU2 ROM	Yes		1WS program 1WS data				
CPU3 ROM	Yes			1WS program 1WS data			

The atomic operations support in memory module is also an main improvement in F29H85x. Atomic operation executes a protected sequence of memory operations while preventing other memory initiators from interrupting. This sequence can involve reading and updating shared variables in memory, where there is a need to protect these variables from updates by other initiators, which means in multiple sequences, you need to set as atomic so that they can finish the access first and cannot be interrupted. Note that all RAMs have ECC protection with a 32-bit granularity. This means that every 32 bits has 7 bits of ECC.

In flash, there are 4 modes that you can choose from. It depends on how you want to allocate the flash with difference CPUS and whether you will need FOTA. Table 4-9 shows the different modes and how each of the solutions could be used.

Table 4-9. Flash Mode for F29H85x

Flash Mode	CPU1	CPU3
0	4MB	-
1	4MB (with FOTA)	-
2	2MB	2MB
3	2MB (with FOTA)	2MB (with FOTA)

Table 4-10. Memory Module Differences

Module	Category	F28P65x	F29H85x	Notes
Flash	Registers	-	1_INTF_CLR	Flash Read Interface 1 Clear Register
		-	1_INTF_CTRL	Flash Read Interface 1 Control Register
		-	1_INTF_CTRL_COMMIT	Flash Read Interface 1 Control Commit Register
		-	1_INTF_CTRL_LOCK	Flash Read Interface 1 Control Lock Register
		-	2_INTF_CLR	Flash Read Interface 2 Clear Register
		-	2_INTF_CTRL	Flash Read Interface 2 Control Register
		-	2_INTF_CTRL_COMMIT	Flash Read Interface 2 Control Commit Register
		-	2_INTF_CTRL_LOCK	Flash Read Interface 2 Control Lock Register
		-	3_INTF_CLR	Flash Read Interface 3 Clear Register
		-	3_INTF_CTRL	Flash Read Interface 3 Control Register
		-	3_INTF_CTRL_COMMIT	Flash Read Interface 3 Control Commit Register
			3_INTF_CTRL_LOCK	Flash Read Interface 3 Control Lock Register
		-	4_INTF_CLR	Flash Read Interface 4 Clear Register
		-	4_INTF_CTRL	Flash Read Interface 4 Control Register
		-	4_INTF_CTRL_COMMIT	Flash Read Interface 4 Control Commit Register
		-	4_INTF_CTRL_LOCK	Flash Read Interface 4 Control Lock Register
		-	FRDCNTL_COMMIT	Flash Read Control Commit Register
		-	FRDCNTL_LOCK	Flash Read Control Lock Register
		-	PARITY_TEST_COMMIT	Parity Test Commit Register
		-	PARITY_TEST_LOCK	Parity Test Lock Register
		ECC_ENABLE	-	ECC Enable
		FECC_CTRL	-	ECC Control
		FLPROT	-	Flash program/erase protect register
		FRD_INTF_CTRL	-	Flash Read Interface Control Register

4.7 GPIO Multiplexing Changes

As the GPIO multiplexing scheme has changed with the introduction of new peripherals and IOs, refer to the device-specific data sheet and the new SysConfig PinMux tool for implementing the PinMux configuration.

5 Software Development with F29H85x

The following section describes code changes when migrating from F28P65x to F29H85x.

Each Gen 4 device, starting with F29H85x, has an individual set of foundational and application SDKs as opposed to one C2000WARE for all devices. To get started with F29x software, see this page.

Note

Code Composer Studio™ (CCS) Eclipse does not have support for Gen 4 devices. Moving forward, CCS Theia and CCS 20 should be used for software development. To learn more and download this IDE, see this page.

5.1 Migration Report Generation Tool

Users can refer to migration guides released for two specific devices within similar class. Considering the ease of use and different customer needs, the Migration Report Generation Tool was created to assist in migrating between any two C2000 C28x/C29x devices. To try it out, please refer to this tool.

6 References

- Texas Instruments: *F29H85x and F29P58x Real-Time Microcontrollers Technical Reference Manual*
- Texas Instruments: *F29H85x and F29P58x Real-Time Microcontrollers Data Sheet*
- Texas Instruments: *C29x CPU Reference Guide*
- Texas Instruments: *Migration Between TMS320C28x and TMS320C29x Platform User's Guide*
- Texas Instruments: C28/CLA to C29 Software Migration Guide (Hosted within F29H85x SDK)
- Texas Instruments: *C2000 Real-Time Microcontrollers Peripherals Reference Guide*
- Texas Instruments: C29X-ACADEMY

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