AM62P SK Evaluation Module



Description

The SK-AM62P-LP starter kit (SK) evaluation module (EVM) is built around our AM62P display processor, which includes scalable Arm® Cortex®-A53 performance and embedded features, such as: triple high-definition display support, high-performance 3D-GPU, 4K video acceleration, and extensive peripherals. SK-AM62P-LP is an excellent choice for those looking to develop automotive and industrial applications, including automotive digital instrumentation, automotive displays, industrial HMI, and more.

SK-AM62P-LP includes multiple display connectors that enable supporting up to three screens, a mobile industry processor interface (MIPI®) CSI-2 camera connector, an M.2 connector for Wi-Fi® and Bluetooth® modules, two Gigabit Ethernet ports, UART-to-USB circuit for debug output, and two temperature sensors for monitoring SoC and LPDDR4 thermal monitoring.

Get Started

- 1. Order the EVM at SK-AM62P-LP.
- 2. Download the EVM Design Files.
- Download the software from SK-AM62P-LP.
- 4. Read this EVM User's Guide.

Features

- USB-C powered standalone mode of operation
- Power-optimized Power Management Integrated Circuit (PMIC) based power management
- Onboard XDS110 JTAG interface with USB connectivity for code development and debugging
- Onboard 32GB eMMC memory and 512Mb Octal Serial Peripheral Interface (OSPI) NOR flash
- 40-pin FPC connector for Open LVDS Display Interface (OLDI)
- 22-pin FPC connector for Display Serial Interface (DSI)
- Onboard High-Definition Multimedia Interface (HDMI®) connector to interface with external display
- 2 × RGMII RJ45 connectors
- 2 × USB 2.0 on Type A and Type-C connectors
- Test automation interface through XDS110
- Expansion connectors to access the low-speed interfaces
- Microcontroller (MCU) connector to access MCU interfaces
- General Purpose Memory Controller (GPMC) connector for external GPMC NAND interface
- M.2 connector for Wi-Fi/BT module





This design incorporates HDMI® technology.



Table of Contents

Description	1
Get Started	1
Features	
1 Evaluation Module Overview	4
1.1 Introduction	
1.2 Kit Contents	4
1.3 Device Information	4
1.4 EVM Revisions and Assembly Variants	4
1.5 Specification	5
2 Hardware	6
2.1 Additional Images	
2.2 Key Features	
2.3 Interface Mapping	
2.4 Power ON/OFF Procedure	
2.5 Clocking	
2.6 Reset	
2.7 Camera Serial Interface (CSI)	
2.8 Open LVDS Display Interface (OLDI)	
2.9 Display Serial Interface (DSI)	
2.10 Audio Codec Interface	
2.11 HDMI Display	
2.13 Test Automation Header	
2.14 UART Interface	
2.15 USB Interface	
2.16 Memory Interfaces	
2.17 Ethernet Interface.	
2.18 GPIO Port Expander	
2.19 GPIO Mapping	
2.20 Power	
2.21 EVM User Setup/Configuration.	
2.22 Expansion Headers	
2.23 Interrupt	
2.24 I2C Address Mapping	
3 Hardware Design Files	
4 Compliance Information	56
4.1 Compliance and Certifications	<u>5</u> 6
5 Additional Information	
5.1 Known Hardware or Software Issues	
5.2 Trademarks	
6 Revision History	59
List of Figures	
Figure 1-1. Functional Block Diagram of AM62P SK EVM	5
Figure 2-1. EVM Top Side	6
Figure 2-2. EVM Bottom Side	
Figure 2-3. Example Boot Mode (MMCSD Boot)	9
Figure 2-4. Clock Architecture	
Figure 2-5. SoC WKUP Domain Clock	
Figure 2-6. Reset Architecture	
Figure 2-7. CSI	
Figure 2-8. OLDI	
Figure 2-9. DSI	
Figure 2-10. Audio Codec Interface	
Figure 2-11. HDMI	
Figure 2-12. JTAG Interface	
Figure 2-13. Test Automation Interface	
Figure 2-14. UART Interface	
Figure 2-15. USB 2.0 Type A Interface	
Figure 2-16. USB 2.0 Type C® Interface	21

Table of Contents

Figure 2-17. LPDDR4 Interface	
Figure 2-18. OPSI	
Figure 2-19. eMMC Interface	
Figure 2-20. uSD Interface	
Figure 2-21. M.2 Interface	
Figure 2-22. Board ID EEPROM Interface	
Figure 2-24. Power InputFigure 2-25. Power Architecture	
Figure 2-26. Power Sequence	
Figure 2-27. Boot Mode Switch (MMCSD Boot)	
Figure 2-28. MCU Connector Interface	
Figure 2-29. I2C Interface	
Figure 5-1. Disconnect Pre-reg Enable Pin	
Figure 5-2. Connect the Pre-reg Enable Pin	
Figure 5-3. Supply the Test Automation With the TYPE-C PD LDO-3V3	59
List of Tables	
Table 1-1. EVM PCB Design Revisions, and Assembly Variants	4
Table 2-1. Interface Mapping	8
Table 2-2. Test Points	
Table 2-3. Clock Table	12
Table 2-4. CSI Camera Connector (J6) Pinout	14
Table 2-5. OLDI Display Connector (J27) Pinout	
Table 2-6. DSI Display Connector (J25) Pinout	17
Table 2-7. JTAG Connector (J23) Pinout	
Table 2-8. Test Automation Connector (J29) Pinout	<mark>2</mark> 4
Table 2-9. UART Port Interface	<mark>24</mark>
Table 2-10. IO Expander 1 Signal Details	
Table 2-11. IO Expander 2 Signal Details	
Table 2-12. GPIO Mapping	
Table 2-13. Type C Port Power Roles	
Table 2-14. Recommended External Power Supply	
Table 2-15. SoC Power Supplies	
Table 2-16. INA I2C Device Address	
Table 2-17. Boot Mode Pin Mapping	
Table 2-18. PLL Reference Clock Selection BOOTMODE[2:0]	
Table 2-19. Boot Device Selection BOOTMODE[6:3]	
Table 2-20. Backup Boot Mode Selection BOOTMODE[12:10]	
Table 2-21. Primary Boot Media Configuration BOOTMODE[9:7]	
Table 2-22. Serial NAND Configuration Fields	
Table 2-23. OSPI Boot Configuration Fields	
Table 2-24. QSPI Boot Configuration Fields	
Table 2-25. SPI Boot Configuration Fields	
Table 2-27. Ethernet RMII Boot Configuration Fields	
Table 2-28. Ethernet RMII Clocking	
Table 2-29. Ethernet Backup Boot Configuration Field	
Table 2-30. I2C Boot Configuration Fields	
Table 2-31. SD Card Boot Configuration Fields	
Table 2-32. eMMC Boot Configuration Fields	
Table 2-33. USB Boot Configuration Fields	
Table 2-34. xSPI Boot Configuration Fields	
Table 2-35. User Test LEDs.	
Table 2-36. User Expansion Connector (J4).	
Table 2-37. MCU Connector (J11)	
Table 2-38. GPMC NAND (x8) Connector (J14)	
Table 2-39. EVM Push Buttons	
Table 2-40. I2C Mapping Table	
Table 5-1. AM62P SK EVM Known Issues and Modifications	

Evaluation Module Overview www.ti.com

1 Evaluation Module Overview

1.1 Introduction

The starter kit allows the user to experience high resolution display features through HDMI (over DPI), dual-port Low-Voltage Differential Signaling (LVDS) and MIPI DSI, as well as industrial communication designs using serial, Ethernet, USB, and other interfaces. The SK EVM can communicate with other processors or systems, and act as a communication gateway. In addition, the SK EVM can directly operate as a standard remote I/O system or simple sensor connected to an industrial communication network. The embedded emulation logic allows for emulation and debugging using standard development tools, such as Code Composer Studio™ from TI.

This technical user's guide describes the hardware architecture of the AM62P SK EVM, a low-cost, low-power starter kit built around the TI's AM62P system-on-chip (SoC). The AM62P SoC is comprised of a quad-core 64-bit Arm® Cortex®-A53 microprocessor, and a single-core Arm® Cortex®-R5F microcontroller (MCU).

1.2 Kit Contents

- SK-AM62P-LP EVM
- · EVM user guide pamphlet
- EVM disclaimer and standard terms

1.3 Device Information

Furthermore, the SK-AM62P-LP supports Linux® and Android development with a feature-rich software development kit (SDK). On-chip emulation logic allows for emulation and debugging using standard development tools such as the Code Composer Studio integrated development environment (IDE) (CCSTUDIO) as well as an intuitive out-of-box user's guide to quickly start design evaluation.

1.4 EVM Revisions and Assembly Variants

The various AM62P EVM PCB design revisions, and assembly variants are listed in Table 1-1. The specific PCB revision is indicated in silkscreen on the PCB and the specific assembly variant is indicated with an additional sticker label. All the revision changes are captured in the change list available in the design file package.

Table 1-1. EVM PCB Design Revisions, and Assembly Variants

OPN	PCB Revision	Assembly Variant	Revision and Assembly Variant Description	
SK-AM62P- LP	E1	N/A (Single variant produced)	First prototype, early release revision of the AM62P EVM.	
SK-AM62P- LP	E1-1	N/A	Second prototype, early release revision of the AM62P EVM. Implements a number of changes and bug fixes.	
SK-AM62P- LP	E2	N/A	Third prototype, early release revision of the AM62P EVM Implements a number of changes, including updating to AM62P SR1.2.	



1.5 Specification

The figure below shows the functional block diagram of the AM62P SK EVM.

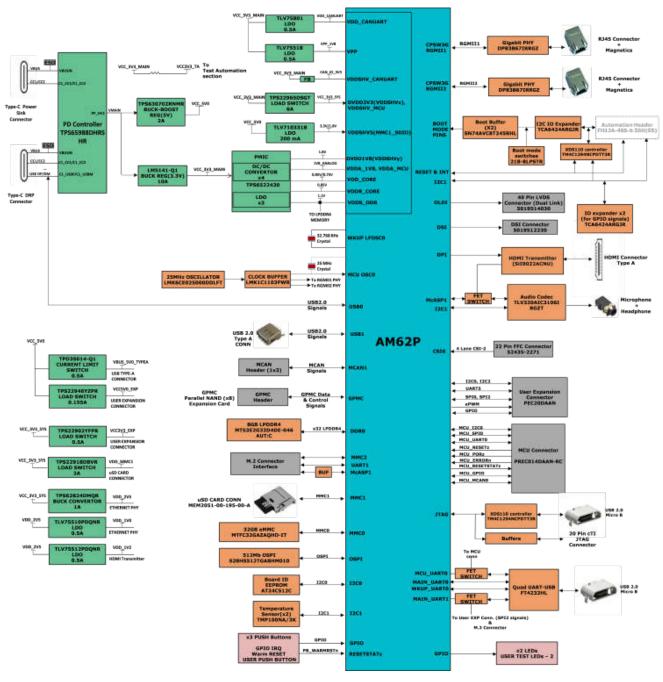


Figure 1-1. Functional Block Diagram of AM62P SK EVM

Hardware www.ti.com

2 Hardware

2.1 Additional Images

This section shows the EVM pictures and location of various blocks on the board.

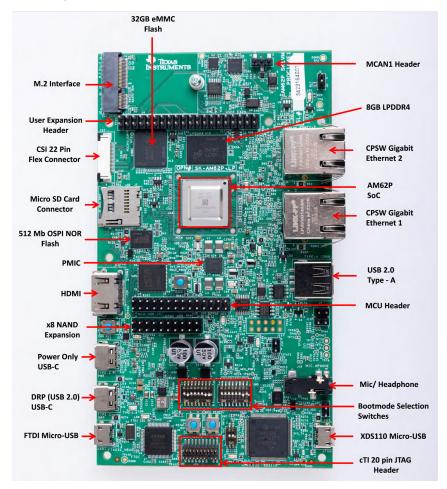


Figure 2-1. EVM Top Side

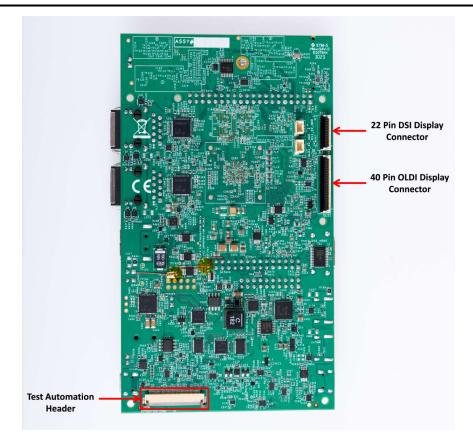


Figure 2-2. EVM Bottom Side

2.2 Key Features

The AM62P SK EVM is a high performance, standalone development platform that enables users to evaluate and develop industrial applications for the Texas Instrument's AM62P System-on-Chip (SoC).

The following sections discuss the key features of the SK EVM.

2.2.1 Processor

AM62P SoC, 17mm x 17mm, 466-pin BGA

2.2.2 Power Supply

- Two USB Type-C[®] ports (5V–15 V input range)
- · Optimized power designs with PMIC, discrete regulators and LDOs for the processor and peripherals

2.2.3 Memory

- 8GB LPDDR4 supporting data rate up to 3200Mb/s per pin
- · Micro SD card slot with UHS-1 support
- 512Mbit Octal Serial Peripheral Interface (OSPI) NOR flash memory
- 512Kbit Inter-Integrated Circuit (I2C) board ID EEPROM
- · 32GB embedded MultiMediaCard (eMMC) flash

2.2.4 JTAG/Emulator

- XDS110 onboard emulator
- Supports 20-pin JTAG connection from external emulator

Hardware Www.ti.com

2.2.5 Supported Interfaces and Peripherals

- 1 × USB 2.0 Type-C® interface, supporting DFP and UFP modes (Data) and DRP mode (Power)
- 1 × USB 2.0 host interfaces, Type A
- 1 × HDMI
- Audio line in and MIC + headphone out
- M.2 Key E interface support for both Wi-Fi and Bluetooth modules
- 2 × Gigabit Ethernet port supporting 10/100/1000Mbps data rate on RJ45 connector
- · Quad port UART to USB circuit over micro-B USB connector
- User test LEDs
- INA devices for SoC power monitoring
- 2 × temperature sensors near SoC and LPDDR4 for thermal monitoring

2.2.6 Expansion Connectors/Headers

- · CSI Camera connector
- DSI Display connector
- · LVDS Display connector
- User Expansion connector
- MCU header
- GPMC NAND (x8) header
- MCAN1 header

2.3 Interface Mapping

Table 2-1. Interface Mapping

Interface Name	Port on SoC	Device Part Number
Memory – LPDDR4	DDR0	MT53E2G32D4DE-046 AUT:C
Memory – OSPI	OSPI0	S28HS512TGABHM010
Memory – Micro SD socket	MMC1	MEM2051-00-195-00-A
Memory – eMMC	MMC0	MTFC32GAZAQHD-IT
Memory – Board ID EEPROM	SoC_I2C0	AT24C512C-MAHM-T
Ethernet 1 – RGMII	SoC_RGMII1	DP83867IRRGZ
Ethernet 2 – RGMII	SoC_RGMII2	DP83867IRRGZ
GPIO port expander 1	SoC_I2C1	TCA6424ARGJR
User expansion connector – 2x20 HDR	SPI0, SPI2, UART5, SoC_I2C0, SoC_I2C2, McASP1 and GPIOs	PEC20DAAN
MCU header – 2x14 HDR	MCU MCU_UART0, MCU_MCAN0, MCU_SPI0, MCU_I2C0 and MCU GPIOs	PREC014DAAN-RC
GPMC NAND (x8) HDR	G GPMC	PREC010DAAN-RC
USB- 2.0 Type C	USB0	2012670005
USB- 2.0 Type A	USB1	629104151021
CSI	CSI0-RX	52435-2271
DSI	DSI0-TX	5019512230
OLDI	OLDI	5019514030
MCAN1 interface	MCAN1	TSM-103-02-T-SV
HDMI	VOUT0, McASP1and SoC_I2C1	Sil9022ACNU + TPD12S016PWR + DC04S019JA1R600
Audio codec	McASP1 and SoC_I2C1	TLV320AIC3106IRGZT+ SJ-43514-SM
GPIO port expander 2	SoC_I2C1	TCA6424ARGJR
UART terminal (UART-to-USB)	SoC_UAR SoC_UART[1:0], WKUP_UART0 and MCU_UART0	FT4232HL + 629105150521
Test automation header	SoC_I2C1	FH12A-40S-0.5SH
Temperature sensors	SoC_I2C1	TMP100NA/3K

Table 2-1. Interface Mapping (continued)

Interface Name	Port on SoC	Device Part Number	
Current monitors	SoC_I2C1	INA228AIDGSR	
Connectivity– M.2 Key E	MMC2, McASP1 and SoC_UART1	2199119-4	

2.4 Power ON/OFF Procedure

Power to the EVM is provided through an external power supply with PD capability to either of the two USB Type-C Ports.

Note

The maximum length of the I/O cables shall not exceed 3 meters.

2.4.1 Power ON Procedure

- 1. Place the SK EVM boot switch selectors (SW4, SW5) into selected boot mode. Example boot-mode for SD card is shown below.
- 2. Connect your boot media (if applicable).
- 3. Attach the PD capable USB Type-C® cable to the SK EVM Type-C (J17 or J19) connector.
- 4. Connect the other end of the USB Type-C cable to the source, either AC Power Adapter, or USB Type C source device (such as a laptop computer).
- 5. Visually inspect that either LD4 or LD6 LED is illuminated.
- 6. XDS110 JTAG and UART debug console outputs are routed to micro-USB ports J22 and J21, respectively.





Figure 2-3. Example Boot Mode (MMCSD Boot)

2.4.2 Power OFF Procedure

- 1. Disconnect AC power from AC/DC converter.
- 2. Remove the USB Type-C cable from the SK EVM.

Hardware INSTRUMENTS

www.ti.com

2.4.3 Test Points

Test points for each power output on the board are mentioned in Table 2-2.

Table 2-2. Test Points

SL. No.	Power Supply	Test Points Test Point	Voltage
1	VCC5V0_EXP	TP10	5
2	VDD CANUART	TP11	0.85
3	VCC3V3_EXP	TP12	3.3
4	VDD_1V0	TP23	1
5	VDD_1V2	TP24	1.2
6	VDDSHV_SDIO	TP33	3.3/1.8
7	VPP_1V8	TP35	1.8
8	VDD_2V5	TP36	2.5
9	VDD_CORE	TP42	0.85/0.75
10	VDDR_CORE	TP43	0.85
11	VCC1V8_SYS	TP54	1.8
12	VDDA_1V8	TP55	1.8
13	VDD_LPDDR4	TP56	1.1
14	VCC_3V3_SYS	TP61	3.3
15	VCC_3V3_MAIN	TP68	3.3
16	VMAIN	TP82	12
17	VCC_5V0	TP85	5
18	VCC3V3_XDS	TP90	3.3
19	XDS_USB_VBUS	TP98	5
20	VCC3V3_TA	TP201	3.3
21	VBUS_5V0_TYPEA	TP203	5
22	VBUS_TYPEC1	TP204	12
23	VBUS_TYPEC2	TP205	12
24	FT4232_USB_VBUS	TP206	5
25	LDO_3V3	U30.8	3.3
26	VCC_3V3_FT4232	C153.2	3.3
27	VDD_MMC1_SD	TP202	3.3
28	VCC_5V0_HDMICONN	TP207	5

2.5 Clocking

Figure 2-4 shows the clock architecture of the AM62P SK EVM.

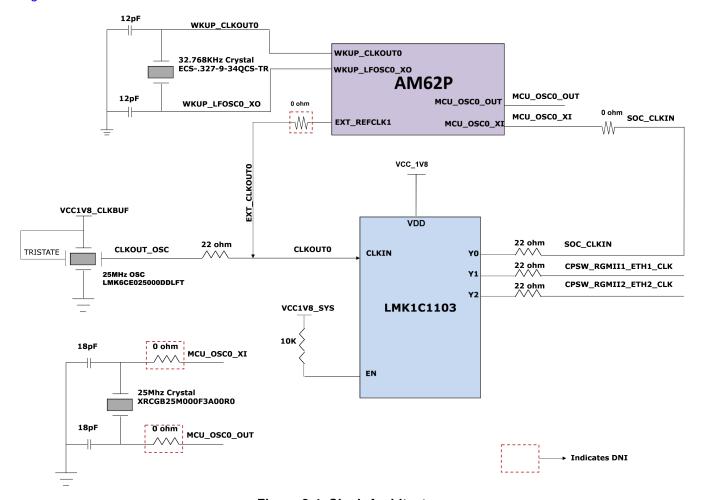


Figure 2-4. Clock Architecture

A clock buffer of part number LMK1C1103PWR is used to drive the 25MHz clock to the SoC and the two Ethernet PHYs. LMK1C1103PWR is a 1:3 LVCMOS clock buffer, which takes the 25MHz crystal/LVCMOS reference input and provides three 25MHz LVCMOS clock outputs. The source for the clock buffer shall be either the CLKOUT0 pin from the SoC or a 25MHz oscillator, the selection of which is made using a set of resistors. By default, an oscillator is used as an input to the clock buffer on the AM62P SK EVM. Outputs Y1 and Y2 of the clock buffer are used as reference clock inputs for the two Gigabit Ethernet PHYs.

There is one external crystal (32.768KHz) attached to the AM62P SoC to provide clock to the WKUP domain.

Hardware www.ti.com

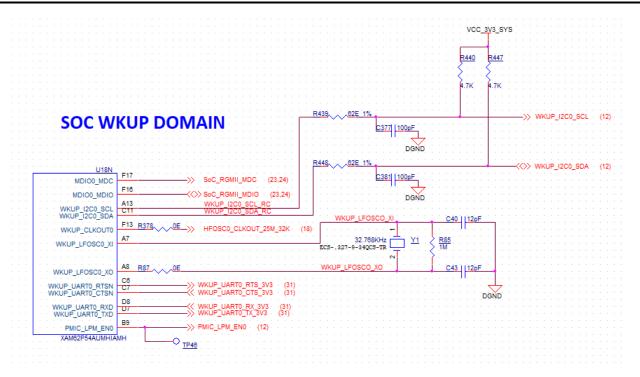


Figure 2-5. SoC WKUP Domain Clock

2.5.1 Peripheral Ref Clock

Clock inputs required for peripherals such as XDS110, FT4232, M.2 Interface, HDMI Framer and Audio Codec are generated locally using separate crystals or oscillators. Table 2-3 shows the crystals or oscillators used to provide the reference clocks to the EVM peripherals.

Peripheral Mfr. Part # Description Frequency XRCGB16M000FXN01R0 CRY 16.000MHz 8pF SMD XDS110 emulator (Y3) 16.000MHz FT4232 Bridge (Y4) 445I23D12M00000 CRY 12.000MHz 18pF SMD 12.000MHz M.2 Interface (U45) ECS-327MVATX-2-CN-TR OSC 32.768KHz CMOS SMD 32.768KHz Audio Codec (U98) LMK6CE012288CDLFT OSC 12.288MHz CMOS SMD 12.288MHz HDMI Framer (U23) LMK6CE012288CDLFT OSC 12.288MHz CMOS SMD 12.288MHz

Table 2-3. Clock Table

The clock required by the HDMI Transmitter can be provided by either the onboard oscillator or the AUDIO_EXT_REFCLK1 of the SoC, which can be selected through a resistor multiplexer. The EXT_REFCLK1 of the SoC is used to provide clock to the User Expansion Connector on the SK EVM. The 32.768KHz clock to the M.2 module is provided by default from WKUP_CLKOUT0 ball of AM62P SoC.

2.6 Reset

The reset architecture of the AM62P SK EVM is shown below. The SoC has the following resets.

- RESETSTATz is the Main domain warm reset status output.
- PORz_OUT is the Main domain power ON reset status output.
- RESET_REQz is the Main domain warm reset input.
- MCU_PORz is the MCU domain power ON/Cold Reset input.
- MCU_RESETz is the MCU domain warm reset input.
- MCU RESETSTATz is the MCU domain warm reset status output.

Upon power on reset, all peripheral devices connected to the main domain get reset by RESETSTATz.

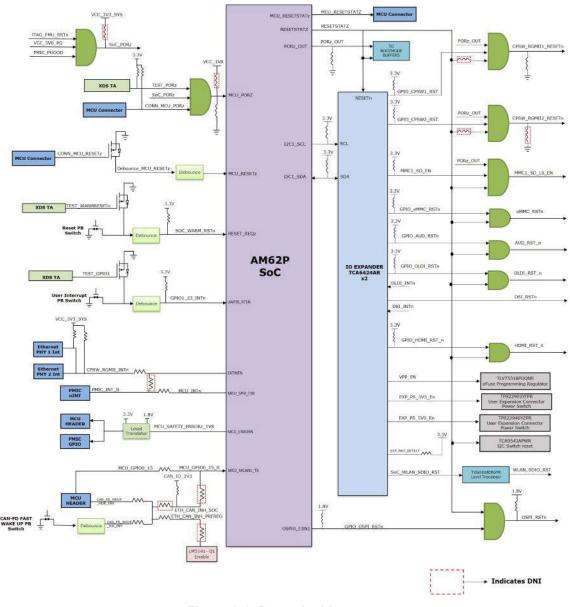


Figure 2-6. Reset Architecture

Hardware Vincom

Vinco

2.7 Camera Serial Interface (CSI)

The CSI-2 signals from the AM62P SoC are terminated to a 22-pin FFC connector 52435-2271 to interface with commercially available of the shelf CSI-2 standard Camera Card/Modules. All four CSI RX lanes are pinned out on the SK EVM along with SOC_I2C2 instance and a couple of GPIOs from the I2C1 controlled GPIO Port Expander.

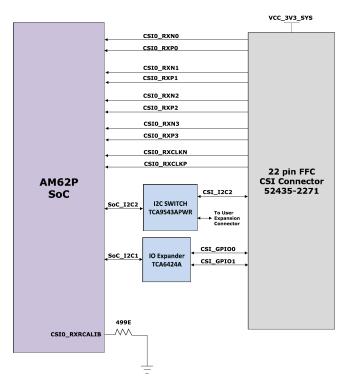


Figure 2-7. CSI

Table 2-4. CSI Camera Connector (J6) Pinout

Pin No	Pin Description		
1	DGND		
2	CSI0_RXN0		
3	CSI0_RXP0		
4	DGND		
5	CSI0_RXN1		
6	CSI0_RXP1		
7	DGND		
8	CSI0_RXCLKN		
9	CSI0_RXCLKP		
10	DGND		
11	CSI0_RXN2		
12	CSI0_RXP2		
13	DGND		
14	CSI0_RXN3		
15	CSI0_RXP3		
16	DGND		
17	CSI_GPIO0		
18	CSI_GPIO1		
19	DGND		

Table 2-4. CSI Camera Connector (J6) Pinout (continued)

Pin No	Pin Description
20	CSI_I2C2_SCL
21	CSI_I2C2_SDA
22	VCC_3V3_SYS

2.8 Open LVDS Display Interface (OLDI)

The OLDI0 display interface of the AM62P is connected to a 40-pin LVDS display connector (J27) manufacturer part number 5019514030 from Molex®. The AM62P SK EVM supports dual-channel 8-bit LVDS output with resolutions up to 3840 × 1080p. Apart from the dual-channel LVDS signals, the 40-pin connector is provided with a 3.3V supply with sourcing capability until 500mA, I2C0 for any pre-initializations and two GPIOs for handling interrupt and reset to the interfacing display.

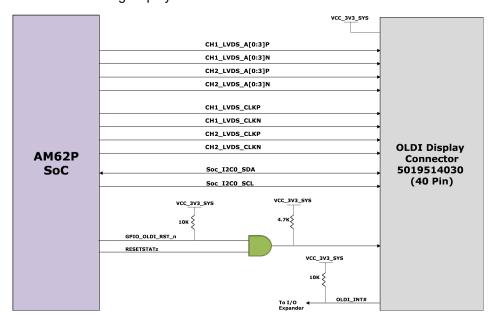


Figure 2-8. OLDI



Hardware www.ti.com

Table 2-5. OLDI Display Connector (J27) Pinout

Table 2-3. OLDI Display Golffiector (327) I mout				
Pin No.	Signal	Pin No.	Signal	
1	DGND	21	CH1_LVDS_A2N	
2	CH2_LVDS_A3P	22	DGND	
3	CH2_LVDS_A3N	23	CH1_LVDS_CLKP	
4	DGND	24	CH1_LVDS_CLKN	
5	CH2_LVDS_A2P	25	DGND	
6	CH2_LVDS_A2N	26	CH1_LVDS_A1P	
7	DGND	27	CH1_LVDS_A1N	
8	CH2_LVDS_CLKP	28	DGND	
9	CH2_LVDS_CLKN	29	CH1_LVDS_A0P	
10	DGND	30	CH1_LVDS_A0N	
11	CH2_LVDS_A1P	31	DGND	
12	CH2_LVDS_A1N	32	OLDI_INT#	
13	DGND	33	OLDI_RESETN	
14	CH2_LVDS_A0P	34	DGND	
15	CH2_LVDS_A0N	35	DGND	
16	DGND	36	NC	
17	CH1_LVDS_A3P	37	NC	
18	CH1_LVDS_A3N	38	SOC_I2C0_SDA	
19	DGND	39	SOC_I2C0_SCL	
20	CH1_LVDS_A2P	40	VCC_3V3_SYS_CONN	

2.9 Display Serial Interface (DSI)

The DSI of the AM62P is connected to a 22-pin display connector (J25) manufacturer part number 5019512230 from Molex. The AM62P SK EVM supports four DSI-TX lanes for high-speed video link and low power command link with resolutions up to 3840 × 1080p. Apart from these four lanes, the 22-pin connector is provided with a 3.3V supply with sourcing capability until 500mA, I2C0 for any pre-initializations and two GPIOs for handling interrupt and reset to the interfacing display.

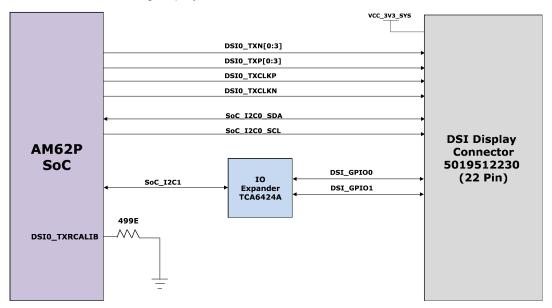


Figure 2-9. DSI

Table 2-6. DSI Display Connector (J25) Pinout

	. ,
Pin No.	Signal
1	VCC_3V3_SYS
2	SOC_I2C0_SDA
3	SOC_I2C0_SCL
4	DGND
5	DSI_INTN#
6	DSI_RESETN
7	DGND
8	DSI_TX3_P
9	DSI_TX3_N
10	DGND
11	DSI_TX2_P
12	DSI_TX2_N
13	DGND
14	DSI_TXCLK_P
15	DSI_TXCLK_N
16	DGND
17	DSI_TX1_P
18	DSI_TX1_N
19	DGND
20	DSI_TX0_P
21	DSI_TX0_N
22	DGND

STRUMENTS Hardware www.ti.com

2.10 Audio Codec Interface

AM62P SK EVM houses TI's TLV320AIC3106 Stereo Audio Codec to interface with AM62P through McASP1 group of signals.

TLV320AIC3106 is a low-power stereo audio codec with stereo headphone amplifier, as well as multiple inputs and outputs programmable in single-ended or fully differential configurations. The record path of the TLV320AIC3106 contains integrated microphone bias, digitally controlled stereo microphone preamplifier and Automatic gain control (AGC) with mix/MUX capability among the multiple analog inputs. The stereo audio DAC supports sampling rates from 8kHz to 96kHz.

One standard 3.5mm TRRS audio jack connector (J18) manufacturer part number SJ-43514 is provided for MIC IN and Headphone output. Audio codec line inputs are terminated to test points. The codec can be configured over I2C with device address set to 0x1B.

The controller clock input, MCLK to the audio codec is provided through a 12.288MHz oscillator. Audio serial data bus bit clock (BCLK) and audio serial data bus input and output (DIN and DOUT) are connected to SOCs MCASP1 instance through a MUX/DEMUX. An AND output of RESETSTATz and a GPIO sourced through IO expander is used to reset the Audio codec.

The TLV320AIC3106 is powered by an analog supply of 3.3V, a digital core supply of 1.8V, and a digital I/O supply of 3.3V.

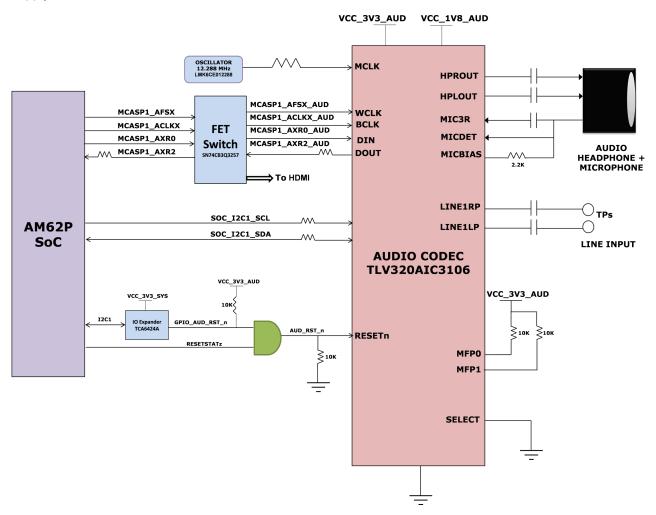


Figure 2-10. Audio Codec Interface

2.11 HDMI Display

The Display Subsystem (DSS) from AM62P SoC is used on the SK EVM to provide an HDMI through a standard Type-A connector. The SK EVM features a Sil9022A HDMI transmitter from Lattice Semiconductor Corporation[®] to convert the 24-bit parallel RGB DSS output stream as well as McASP1 signals to an HDMI-compliant digital audio and video signal.

To use Sil9022A, the SoC needs to set up the device. This is done through the I2C1 interface between the SoC and the Sil9022A. SoC_I2C1 instance connected to the HDMI transmitter accesses the compatible mode registers, the TPI registers, and the CPI registers. Audio data is sent from the SoC to the HDMI transmitter through the McASP1 instance. HDMI I2C bus accesses the EDID and HDCP data on an attached sink device.

TMDS differential data pairs along with the differential clock signals from the transmitter are connected to the HDMI connector through HDMI ESD device manufacturer part number TPD12S016PWR which also acts as a load switch to limit current supplied to the HDMI connector from onboard 5V supply.

The HDMI framer is powered using 3.3V board I/O supply and 1.2V for the AVCC and DVCC supply by a dedicated LDO manufacturer part number TLV75512PDQNR.

Hardware Superior INSTRUMENTS

www.ti.com

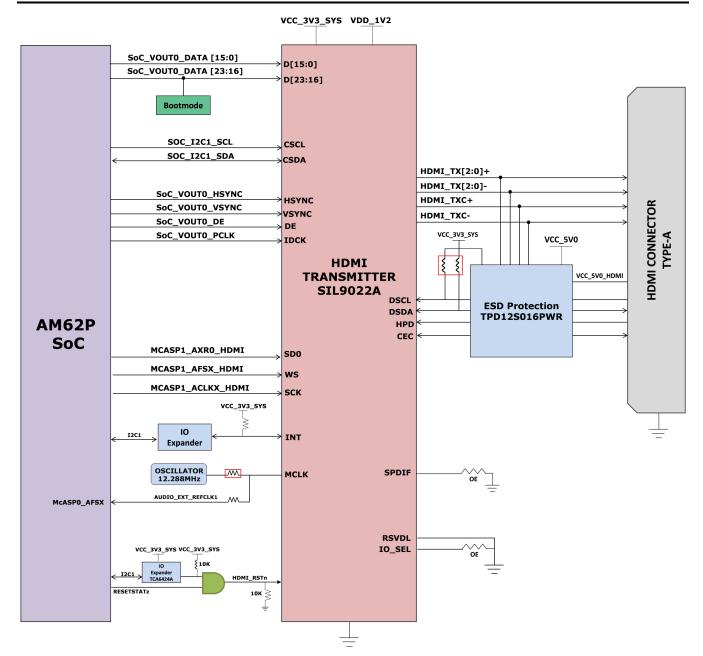


Figure 2-11. HDMI

2.12 JTAG Interface

AM62P SK EVM includes XDS110 class onboard emulation. The connection for this emulator uses a standard USB 2.0 micro-B connector and the circuit acts as a bus powered USB device. The VBUS power from the connector is used to power the emulation circuit such that connection to the emulator is not lost when the power to the SKEVM is removed. Voltage translation buffers are used to isolate the XDS110 circuit from the rest of the SK EVM.

Optionally, a JTAG interface on SK EVM is also provided through a 20-pin standard JTAG cTI header J23. This allows the user to connect an external JTAG emulator cable. Voltage translation buffers are used to isolate the JTAG signals of cTI header from rest of the SK EVM. The output of the voltage translators from XDS110 section and cTI header section are multiplexed and connected to the AM62P JTAG interface. If a connection to the cTI 20-pin JTAG connector is sensed using an auto presence detect circuit, the MUX routes the 20-pin signals from the cTI connector to the AM62P SoC in place of the onboard emulation circuit.

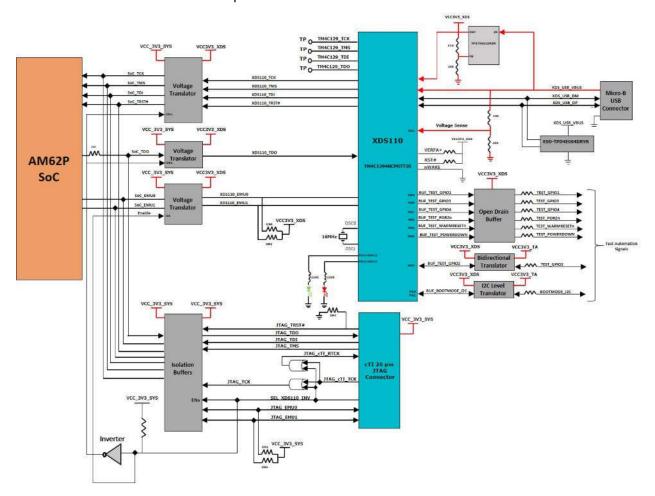


Figure 2-12. JTAG Interface



Hardware www.ti.com

The pinouts of the cTI 20-pin JTAG connector are given in Table 2-7. A ESD protection part number TPD4E004 is provided on USB signals to steer ESD current pulses to VCC or GND. TPD4E004 protects against ESD pulses up to ±15kV Human-Body Model (HBM) as specified in IEC 61000-4-2 and provides ±8kV contact discharge and ±12kV air-gap discharge.

Table 2-7. JTAG Connector (J23) Pinout

Pin Number	Signal
1	JTAG_TMS
2	JTAG_TRST#
3	JTAG_TDI
4	JTAG_TDIS
5	VCC_3V3_SYS
6	NC
7	JTAG_TDO
8	SEL_XDS110_INV
9	JTAG_cTI_RTCK
10	DGND
11	JTAG_cTI_TCK
12	DGND
13	JTAG_EMU0
14	JTAG_EMU1
15	JTAG_EMU_RSTn
16	DGND
17	NC
18	NC
19	NC
20	DGND

2.13 Test Automation Header

AM62P SK EVM has an optional 40-pin test automation header (FH12A-40S-0.5SH) to allow any external controller to manipulate some basic operations like Power Down, POR, Warm Reset, and Boot Mode control.

The Test Automation Circuit is powered by the 3.3V supply generated by an Always On regulator manufacturer part number LM5141QRGETQ1. The SoCs I2C1 instance is connected to the test automation header. Another I2C instance (BOOTMODE_I2C) from the Test Automation Header is connected to the 24-bit I2C boot mode IO Expander of manufacturer part number TCA6424ARGJR to allow control of the boot modes for the AM62P SoC.

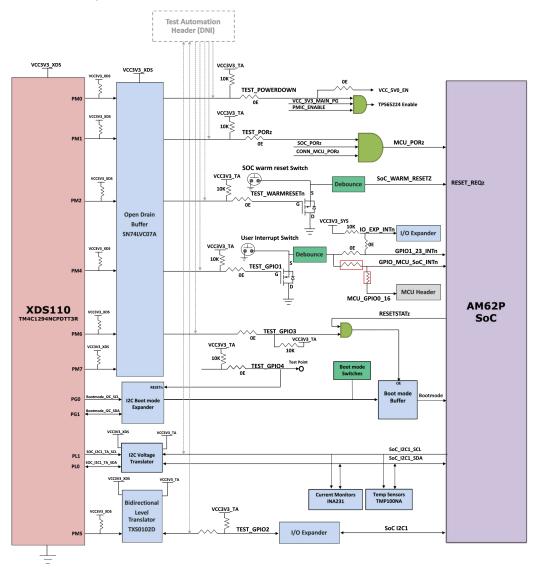


Figure 2-13. Test Automation Interface

The test automation has voltage translation circuits so that the controller is isolated from the I/O voltages used by the AM62P. Boot mode for the AM62P can be user controlled by either using DIP Switches or the test automation header through the I2C I/O Expander. Boot Mode Buffers are used to isolate the Boot Mode controls driven through DIP Switches or I2C I/O Expander. The boot mode can also be set using two 8-bit DIP switches on the board, which connects a pull-up resistor to the output of a buffer when the switch is set to the ON position and to a weaker pulldown resistor when set to OFF position. The outputs of the buffer are connected to the boot mode pins on the AM62P SoC and the output is only enabled when the boot mode is needed during a reset cycle.

Hardware www.ti.com

When boot mode is to be set through Test Automation header, the required switch values are set at the I2C I/O expander output, which overwrites the DIP switch values to give the desired boot values to the SoC. The pins used for boot mode also have other functions which are automatically isolated by disabling the boot mode buffer during normal operation.

The power down signal from the Test automation header instructs the SK EVM to power down all the rails except for dedicated power supplies on the board. Similarly, PORZn signal provides a hard reset to the SoC and WARM RESETn for a warm reset to the SoC.

Table 2-8. Test Automation Connector (J29) Pinout

Pin no.	Signal	IO Direction	Pin no.	Signal	IO Direction
1	VCC3V3_TA	Power	21	NC	NA
2	VCC3V3_TA	Power	22	NC	NA
3	VCC3V3_TA	Power	23	NC	NA
4	NC	NA	24	NC	NA
5	NC	NA	25	DGND	Power
6	NC	NA	26	TEST_POWERDOW N	Input
7	DGND	Power	27	TEST_PORZn	Input
8	NC	NA	28	TEST_WARMRESET n	Input
9	NC	NA	29	NC	NA
10	NC	NA	30	TEST_GPIO1	Input
11	NC	NA	31	TEST_GPIO2	Bidirectional
12	NC	NA	32	TEST_GPIO3	Input
13	NC	NA	33	TEST_GPIO4	Input
14	NC	NA	34	DGND	Power
15	NC	NA	35	NC	NA
16	DGND	Power	36	SoC_I2C1_TA_SCL	Bidirectional
17	NC	NA	37	BOOTMODE_I2C_S CL	Bidirectional
18	NC	NA	38	SoC_I2C1_TA_SDA	Bidirectional
19	NC	NA	39	BOOTMODE_I2C_S DA	Bidirectional
20	NC	NA	40	DGND	Power

2.14 UART Interface

The four UART ports of the SoC (MCU UART0, WKUP UART0, SOC UART0 and SOC UART1) are interfaced with an FTDI Bridge FT4232HL for UART-to-USB functionality and then terminated on a USB micro-B connector (J21) onboard. When the AM62P SK EVM is connected to a host using USB cable, the computer can establish a Virtual COM Port which can be used with any terminal emulation application. Since FT4232HL device is bus powered the connection to the COM port is not be lost when the SK EVM power is removed.

Table 2-9. UART Port Interface

UART PORT	USB to UART Bridge	USB Connector	COM Port
SOC_UART0	FT4232HL	J21	COM1
SOC_UART1			COM2
WKUP_UART0			COM3
MCU_UART0			COM4

The FT4232 chip is configured to operate in 'Single chip USB to four channel UART' mode using the configuration file from an external SPI EEPROM connected. The EEPROM (93LC46B) supports 1 Mbit/s clockrate. The EEPROM is programmable in-circuit over USB using a utility program called FT_PROG available from the FTDI web site. The FT_PROG is also used for programming the board serial number for users to identify the connected COM port with board serial number when one or more boards are connected to the computer.

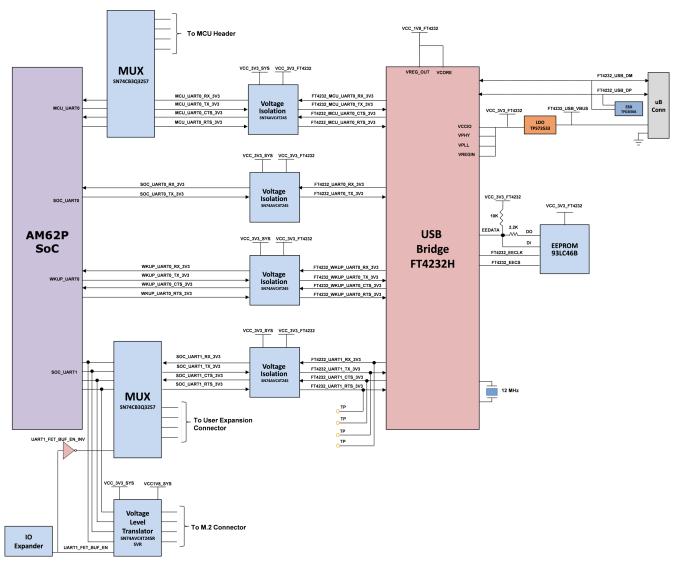


Figure 2-14. UART Interface

Hardware www.ti.com

2.15 USB Interface

2.15.1 USB 2.0 Type A Interface

USB 2.0 data lines DP and DM from Type A connector J9 are connected to the USB1 interface of the AM62P SoC to provide USB high-speed and full-speed communication. USB1 VBUS to the SoC is provided through a resistor divider network to support (5V-30V) VBUS operation. USB1 DRVVBUS from SoC controls the enable pin of a 500mA current limited load switch manufacturer part number TPS2051BD to allow onboard 5V supply to power the VBUS. This load switch has an overcurrent indication pin connected to I2C-based GPIO expander on the SK EVM.

A common mode choke of manufacturer part number DLW21SZ900HQ2B is provided on USB Data lines for EMI/EMC reduction along with ESD protection manufacturer part number TPD4S012DRYR to suppress any transient voltages.

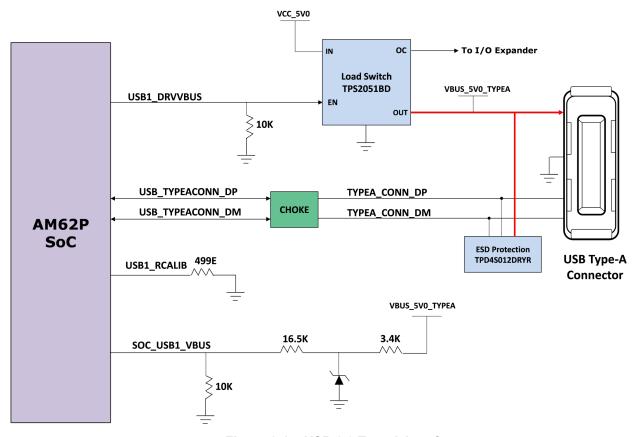


Figure 2-15. USB 2.0 Type A Interface

2.15.2 USB 2.0 Type-C® Interface

On the SK EVM, a USB 2.0 interface is offered through USB Type-C connector J19 manufacturer part number 2012670005 which supports data rate up to 480Mbps. J19 can be used for data communication and as a power connector sourcing supply to the SK EVM. J19 is configured as DRP port using PD controller TPS65988DHRSHR IC. So, J19 can act as either a host or device. The role of the port depends on the type of device getting connected on the connector and the ability to either sink or source. When the port is acting as DFP, DFP can source up to 5V at 500mA.

USB 2.0 data lines DP and DM from J19 are provided with a choke and an ESD protection device. USB0_VBUS to the SoC is provided through a resistor divider network to support (5V–30V) VBUS operation.

A common-mode choke of manufacturer part number DLW21SZ900HQ2B is provided on USB data lines for EMI/ EMC reduction. ESD protection devices of part number ESD122DMXR are included to dissipate any ESD strikes on USB 2.0 DP/DM signals. An ESD protection device of part number TPD1E01B04DPLT is included on CC signals and TVS2200DRVR IC is included on VBUS rail of Type-C connector J19 to dissipate ESD strikes.

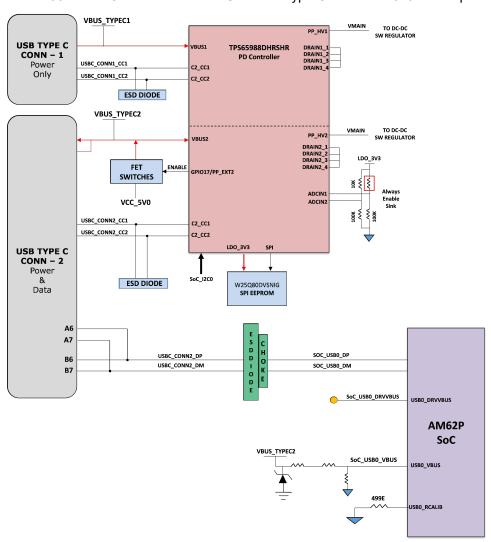


Figure 2-16. USB 2.0 Type C® Interface

Hardware Very Instruments

www.ti.com

2.16 Memory Interfaces

2.16.1 LPDDR4 Interface

AM62P SK EVM houses Micron's (MT53E2G32D4DE-046 AUT:C) dual Rank dual Die 8GB, 32-bit wide LPDDR4 memory supporting data rates up to 3200 Mb/s per pin. The LPDDR4 memory is placed routed to the DDR0 group of SoC to support point to point communication.

The LPDDR4 memory requires 1.8V for the core supply, thus reducing power demand. The I/Os are supplied from a 1.1V supply output from the PMIC. LPDDR4 reset (active low) controlled by the AM62P SoC is pulled down to set the default active state. The provision for mounting a pullup resistor is also provided.

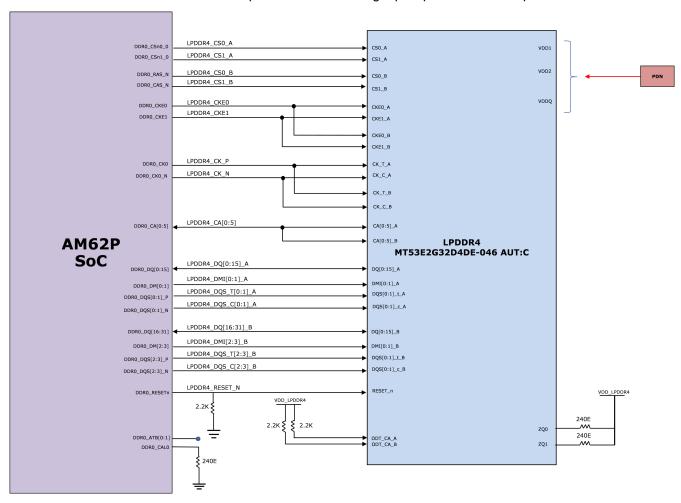


Figure 2-17. LPDDR4 Interface

2.16.2 Octal Serial Peripheral Interface (OSPI)

AM62P SK EVM board features a 512Mb OSPI memory device from Cypress Part# S28HS512TGABHM010 connected to the OSPI0 interface of the AM62P SoC. The OSPI memory supports single and double data rates with memory speeds up to 200MBps SDR and 400MBps DDR (200MHz clock speed).

OSPI and QSPI implementation: 0Ω resistors are provided for DATA[7:0], DQS, INT# and CLK signals. External pullup resistors are provided on DATA[7:0] to prevent bus floating. The footprint for the OSPI memory also allows the installation of either a QSPI memory or an OSPI memory. The 0Ω series resistors provided for pins OSPI_DQ[4:7] can be removed if a QSPI Flash is to be mounted.

Reset: The reset for the OSPI flash is connected to a circuit that ANDs the RESETSTATz from the AM62P with the signal GPIO_OSPI_RSTn from the SoC GPIO. A pull-up resistor is provided on GPIO_OSPI_RSTn to set the default active state.

Power: Both VCC and VCCQ pins of the OSPI Flash memory is supplied through an onboard 1.8V system power. The OSPI I/O group is powered by the VDDSHV1 domain of SoC sourced from the same 1.8V system power.

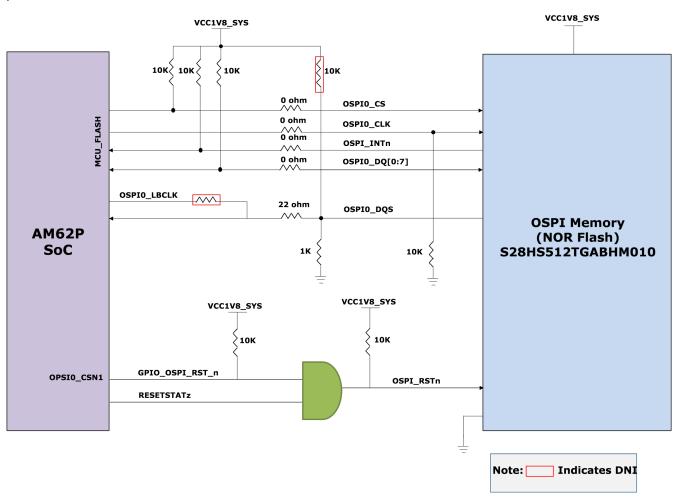


Figure 2-18. OPSI

2.16.3 MMC Interfaces

AM62P SoC features three MMC ports (MMC0, MMC1 and MMC2). MMC0 is connected to eMMC, MMC1 is interfaced with a Micro SD Card connector and MMC2 is terminated to a M.2 Key E expansion connector for Wi-Fi and BT Module Interface.

Hardware Very INSTRUMENTS

www.ti.com

2.16.3.1 MMC0 - eMMC Interface

The SK EVM board contains 32GB of eMMC flash memory from Micron part number MTFC32GAZAQHD-IT connected to the MMC0 port of AM62P SoC.

The data bus from the flash memory is connected to the 8 data bits of the MMC0 interface supporting HS400 double data rates up to 200MHz. The Micron eMMC is a communication and mass data storage device that includes a Multimedia Card (MMC) interface and a NAND Flash component. Option to mount external pullup resistors are provided on DAT[7:1] to prevent bus floating and series resistor is provided for CLK signal close to SoC pad to match the characteristic impedance.

The eMMC device requires two power supplies, 3.3V for NAND memory and 1.8V for the eMMC interface. The MMC0 I/Os of the SoC are powered by VDDS_MMC0 supplied from an fixed 1.8V supply.

eMMC device requires active low reset from host. By default, the RST_n signal is temporarily disabled in the device. The host must set ECSD register byte 162, bits[1:0] to 0x1 to enable this functionality before the host can use. The External Reset is provided by ANDing RESETSTATz from SoC and a GPIO from IO Expander. A pullup is provided on GPIO pin to set the default active state.

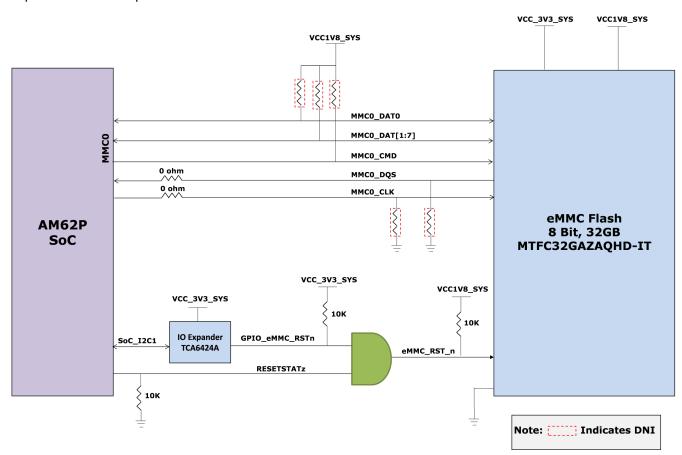


Figure 2-19. eMMC Interface

2.16.3.2 MMC1 - Micro SD Interface

The SK EVM provides a micro SD card socket of manufacturer part number MEM2051-00-195-00-A connected to the MMC1 port of AM62P SoC. This supports UHS1 operation including I/O operations at both 1.8V and 3.3V. The Micro SD card interface is set to operate in SD mode by default. For high-speed cards, the ROM Code of the SoC attempts to find the fastest speed that the card and controller can support and then have a transition to 1.8V through a VSEL SD SOC signal from the SoC.

The SD Card connector power is provided using a load switch of manufacturer part number TPS22918DBVR, which is controlled by ANDing the output of RESETSTATZ, PORZ_OUT and a GPIO from IO Expander.

An ESD protection device of part number TPD6E001RSE is provided for data, clock, and command signals. TPD6E001RSE is a line termination device with integrated TVS diodes providing system-level IEC 61000-4-2 ESD protection, ± 8-kV contact discharge and ± 15kV air-gap discharge.

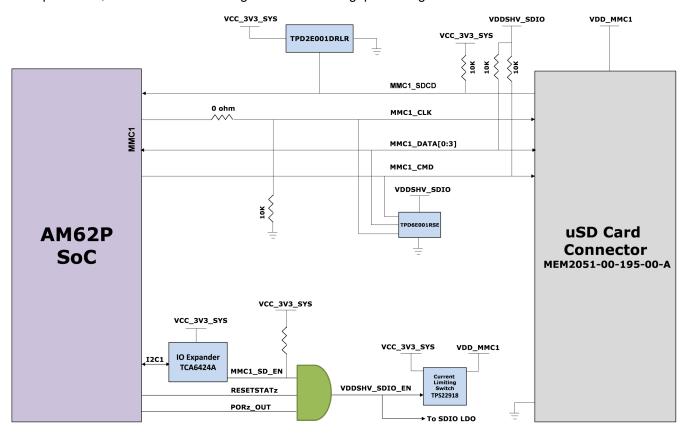


Figure 2-20. uSD Interface

Hardware Very Instruments

Www.ti.com

2.16.3.3 MMC2 - M.2 Key E Interface

AM62P SK EVM has a M.2 Key E expansion for connecting Wi-Fi/BT modules to MMC2, UART2 and McASP1 interface through buffers. This can be used to interface with a Wi-Fi, dual-band, 2.4 and 5GHz module with antennas supporting Industrial temperature grade. The M.2 is provided with 4-bit I/Os of the MMC2 interface supporting IEEE standard 802.11a/b/g/n data. The M.2 connector can be interfaced with modules that can offer high throughput and extended range along with Wi-Fi and Bluetooth coexistence for a power-optimized design.

The M.2 Connector is provided with a 3.3V onboard power supply to meet the power supply requirements of the interfacing modules. The MMC2 interface of the SoC is powered by the VDDSHV6 power domain, which is connected to 1.8V IO supply.

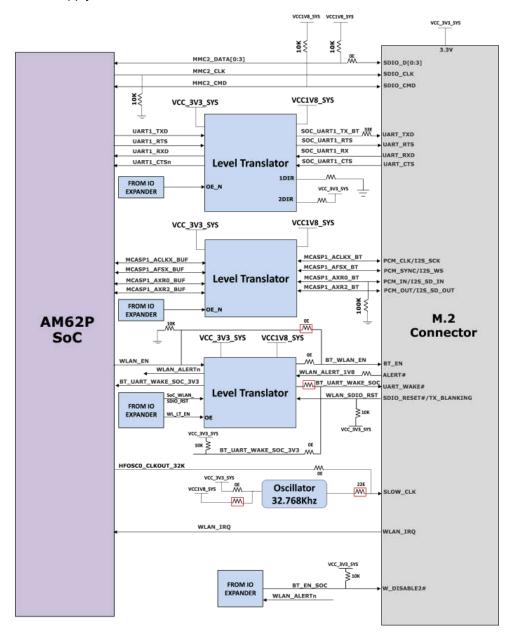


Figure 2-21. M.2 Interface

2.16.4 Board ID EEPROM

AM62P SK- EVM can be identified remotely from the version and serial number data stored on the onboard EEPROM.

Board ID memory AT24C512C-MAHM-T from Microchip is interfaced to the I2C0 port of the SoC and is configured to respond to address 0x51 programmed with the header description. I2C address of the EEPROM can be modified by driving the A0 pin to high and A1, A2 pins to LOW. The first 259 bytes of memory are preprogrammed with identification information for each board. The remaining 65277 bytes are available to the user for data or code storage.

Note

Header J3 must be shorted with a jumper to perform a write operation.

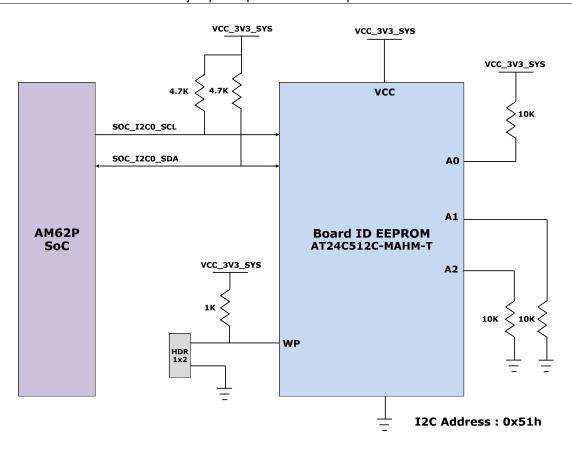


Figure 2-22. Board ID EEPROM Interface



Hardware Vincom

Vinco

2.17 Ethernet Interface

The AM62P SK EVM offers two Ethernet Ports of 1 Gigabit Speed for external communication. Two channels of RGMII Gigabit Ethernet CPSW ports from AM62P SoC are connected to separate Gigabit Ethernet PHY Transceivers DP83867, which are finally terminated on two RJ45 connectors with integrated magnetics.

The 48-pin version of the PHY DP83867 is configured to advertise 1Gb operation with the TX and RX clock skew set to accommodate the internal delay inside the AM62P. CPSW_RGMII1 and CPSW_RGMII2 ports share a common MDIO bus to communicate with the external PHY transceiver.

Two single-port RJ45 connectors manufacturer part number LPJG16314A4NL from Link-PP are used on the board for Ethernet 10/100/1000Mbps connectivity. RJ45 connectors have integrated magnetics and LEDs for indicating 1000BASE-T link as well as receive or transmit activity.

I/O supply to the Ethernet PHY is set 3.3V IO level.

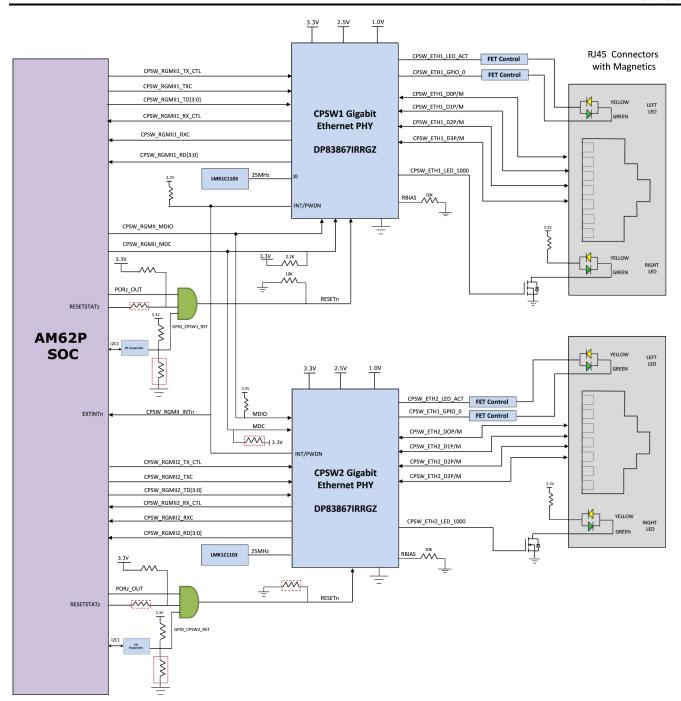


Figure 2-23. Ethernet Interface



Hardware Very INSTRUMENTS

www.ti.com

2.17.1 CPSW Ethernet PHY Strapping

The default configuration of the DP83867 is determined using several resistor pullup and pulldown values on specific pins of the PHY. Depending on the values installed, each of the configuration pins can be set to one of four modes. The AM62P SK EVM uses the 48-pin QFN package which supports the RGMII interface.

The DP83867 PHY uses four level configurations based on resistor strapping which generate four distinct voltage ranges. The resistors are connected to the RX data and control pins which are normally driven by the PHY and are inputs to the processor. The voltage range for each mode is shown below:

- Mode1 0V to 0.3V
- Mode 2 0.462V to 0.6303V
- Mode3 0.7425V to 0.9372V
- Mode4 2.2902V to 2.9304V

Footprint for both pullup and pulldown is provided on all the strapping pins except LED_0. LED_0 is for mirror enable, which is set to mode 1 by default, Mode 4 is not applicable, and Mode 2 and Mode 3 option is not desired.

2.17.2 CPSW Ethernet PHY1 Default Configuration

PHY ADDR: 00000 Auto_neg: Enabled

ANG_SEL: 10/100/1000 RGMII TXCLK skew: 0ns RGMII RXCLK skew: 2ns

2.17.3 CPSW Ethernet PHY2 Default Configuration

PHY ADDR: 00001 Auto_neg: Enabled

ANG_SEL: 10/100/1000 RGMII TXCLK skew: 0ns RGMII RXCLK skew: 2ns

2.18 GPIO Port Expander

The I/O Expanders used in the AM62P SK EVM are 24-bit I2C based I/O Expander which is used for daughter cards plug-in detection and for generating resets and enable signals to various peripheral devices connected onboard. The SoC_I2C1 bus of the AM62P SoC is used to interface with the I/O Expanders. The I2C device addresses of the I/O Expanders are 0x21 and 0x23. See the following tables for the list of signals being controlled by the expanders.

Table 2-10. IO Expander 1 Signal Details

Pin No.	Signal	Direction	Purpose
P00	OLDI_INT#	INPUT	Interrupt from OLDI display
P01	x8_NAND_DETECT	INPUT	x8 NAND Card Presence Detect
P02	UART1_FET_SEL	OUTPUT	UART1 FET selection
P03	MMC1_SD_EN	OUTPUT	SD Card Load Switch Enable
P04	VPP_EN	OUTPUT	SoC eFuse Voltage (VPP=1.8V) Regulator Enable
P05	EXP_PS_3V3_EN	OUTPUT	EXP CONN 3.3V Power Switch Enable
P06	UART1_FET_BUF_EN	OUTPUT	SoC UART1 MUX Select
P07	EXP_HAT_DETECT	INPUT	EXP CONN HAT Board Detection
P10	DSI_GPIO0	BIDIRECTIONAL	DSI Display GPIO0
P11	DSI_GPIO1	BIDIRECTIONAL	DSI Display GPIO1
P12	OLDI_EDID	INPUT	OLDI to HDMI Card Device ID interrupt
P13	BT_UART_WAKE_SOC_3V3	INPUT	BT UART WKUP Signal
P14	USB_TYPEA_OC_INDICATION	INPUT	USB Type A overcurrent indicator
P15	CSI_GPIO0	BIDIRECTIONAL	CSI Camera GPIO1
P16	CSI_GPIO1	BIDIRECTIONAL	CSI Camera GPIO2
P17	WLAN_ALERTn	INPUT	M.2 Module WLAN Alert Input
P20	HDMI_INTN	INPUT	HDMI Interrupt
P21	TEST_GPIO2	BIDIRECTIONAL	TEST GPIO2 from Test Automation Connector
P22	MCASP1_FET_EN	OUTPUT	MCASP1 Enable and Direction
P23	MCASP1_BUF_BT_EN	OUTPUT	Control
P24	MCASP1_FET_SEL	OUTPUT	
P25	DSI_EDID	INPUT	DSI to HDMI Card Device ID interrupt
P26	PD_I2C_IRQ	INPUT	Interrupt Request from PD Controller
P27	IO_EXP_TEST_LED	OUTPUT	User Test LED 2



Hardware Www.ti.com

Table 2-11. IO Expander 2 Signal Details

Pin No.	Signal	Direction	Device	
P00	BT_EN_SOC	OUTPUT	M.2 module Bluetooth LDO Enable	
P01	EXP_PS_5V0_EN	OUTPUT	EXP CONN 5V power switch enable	
P10	WL_LT_EN	OUTPUT	M.2 interface level translator enable	
P20	SoC_I2C2_MCAN_SEL	OUTPUT	SoC I2C2 and MCAN MUX selection	
P21	GPIO_HDMI_RSTn	OUTPUT	HDMI transmitter reset control GPIO	
P22	GPIO_CPSW1_RST	OUTPUT	CPSW Ethernet PHY-1 reset control GPIO	
P23	GPIO_CPSW2_RST	OUTPUT	CPSW Ethernet PHY-2 reset control GPIO	
P24	GPIO_OLDI_RSTn	OUTPUT	OLDI display reset control GPIO	
P25	GPIO_AUD_RSTn	OUTPUT	Audio codec reset control GPIO	
P26	GPIO_eMMC_RSTn	OUTPUT	eMMC Reset control GPIO	
P27	SOC_WLAN_SDIO_RST	OUTPUT	M.2 Module WLAN/SDIO Reset	

www.ti.com

2.19 GPIO Mapping

Table 2-12 describes the detailed GPIO mapping of AM62P SoC with AM62P SK EVM peripherals.

Table 2-12. GPIO Mapping

					or to mapping					
SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAINON SoC SIDE	VOLTAGE RAIL CONNECTED ON SKEVM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	WLAN_IRQ	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	MCU Interrupt	MCU_INTn	INTERRUPT	MCU_GPIO0_0	MCU_SPI0_CS0	INPUT	HIGH	LOW	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	OSPI Interrupt	OSPI_INTn	INTERRUPT	GPIO0_13	OSPI0_CSn2	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
7	MCU Header GPIO0_16	MCU_GPIO0_16	GPIO	MCU_GPIO0_16	MCU_MCAN1_RX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
8	MCU Header GPIO0_15	MCU_GPIO0_15	GPIO	MCU_GPIO0_15	MCU_MCAN1_TX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
9	PMIC Interrupt	PMIC_INTn	INTERRUPT	GPIO0_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
10	CAN-FD fast wake up signal from switch	CAN_FD_WKUP_SW_IN H	INTERRUPT	MCU_GPIO0_15	MOU MOANA TV	INPUT	HIGH	LOW	VPPOUN CANHART	0444 10 0040
11	CAN-FD fast wake signal from MCU header	CAN_FD_WKUP_HDR_I NH			MCU_MCAN1_TX				VDDSHV_CANUART	CAN_IO_3V3
12	User test LED control signal	SOC_GPIO1_49	ENABLE	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	IO Expander Interrupt	GPIO1_23_INTn	INTERRUPT	GPIO1_23	LIADTO DIC-	INPUT	HIGH	LOW	VDDSHV0	CaC DVDD2V2
14	User Interrupt				UART0_RTSn				VDDSHVU	SoC_DVDD3V3
15	Low power mode enable	PMIC_LPM_EN0	ENABLE	_E MCU_GPIO0_22 F	PMIC_LPM_EN0	OUTPUT	HIGH LOV	LOW	VDDSHV_CANUART	CAN_IO_3V3
16	SD Card I/O Voltage Selection	VSEL_SD_SOC	SELECTION	GPIO0_31	GPMC0_CLK	OUTPUT	NA	NA	VDDSHV2	SoC_DVDD3V3
				IO EXF	ANDER - 01					
1	Interrupt from OLDI display	OLDI_INT#	INTERRUPT	IO EXPANDER-P00		INPUT	HIGH	LOW		VCC_3V3_SYS
2	x8 NAND Card Presence Detect	x8_NAND_DETECT	DETECTION	IO EXPANDER-P01		INPUT	HIGH	LOW		VCC_3V3_SYS
3	UART1 FET selection control	UART1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P02		OUTPUT	HIGH	-		VCC_3V3_SYS
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
5	SoC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_EN	ENABLE	IO EXPANDER-P04		OUTPUT	NA	HIGH		VCC_3V3_SYS
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER-P05		OUTPUT	LOW	HIGH		VCC_3V3_SYS
7	SoC UART1 MUX Select	UART1_FET_BUF_EN	ENABLE	IO EXPANDER-P06		OUTPUT	HIGH	LOW		VCC_3V3_SYS
8	EXP CONN HAT Board Detection	EXP_HAT_DETECT	DETECTION	IO EXPANDER-P07		INPUT	HIGH	LOW		VCC_3V3_SYS
9	DSI Display GPIO0	DSI_GPIO0	GPIO	IO EXPANDER-P10		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
10	DSI Display GPIO1	DSI_GPIO1	GPIO	IO EXPANDER-P11		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
11	OLDI to HDMI Card Device ID interrupt	OLDI_EDID	INTERRUPT	IO EXPANDER-P12		INPUT	HIGH	LOW		VCC_3V3_SYS
12	BT UART WKUP Signal	BT_UART_WAKE_SOC_ 3V3	INTERRUPT	IO EXPANDER-P13		INPUT	HIGH	LOW		VCC_3V3_SYS
13	USB Type A overcurrent indicator	USB_TYPEA_OC_INDIC ATION	INTERRUPT	IO EXPANDER-P14		INPUT	HIGH	LOW		VCC_3V3_SYS

Hardware



Table 2-12. GPIO Mapping (continued)

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAINON SoC SIDE	VOLTAGE RAIL CONNECTED ON SKEVM
14	Raspberry Pi Camera CSI0 GPIO1	CSI_GPIO0	INPUT/OUTPUT	IO EXPANDER-P15		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
15	Raspberry Pi Camera CSI0 GPIO2	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER-P16		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
16	WLAN Alert Interrupt	WLAN_ALERTn	INTERRUPT	IO EXPANDER-P17		INPUT	HIGH	LOW		VCC_3V3_SYS
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER-P20		INPUT	HIGH	LOW		VCC_3V3_SYS
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO	IO EXPANDER-P21		NA	HIGH	NA		VCC_3V3_SYS
19	MCASP1 Enable and Direction	MCASP1_FET_EN	ENABLE	IO EXPANDER-P22		OUTPUT	LOW	LOW		VCC_3V3_SYS
20	Control	MCASP1_BUF_BT_EN	ENABLE	IO EXPANDER-P23		OUTPUT	LOW	HIGH		VCC_3V3_SYS
21		MCASP1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P24		OUTPUT	HIGH	-		VCC_3V3_SYS
22	DSI to HDMI Card Device ID interrupt	DSI_EDID	INTERRUPT	IO EXPANDER-P25		INPUT	HIGH	LOW		VCC_3V3_SYS
23	Power Delivery I2C Interrupt Request	PD_I2C_IRQ	INTERRUPT	IO EXPANDER-P26		INPUT	HIGH	LOW		VCC_3V3_SYS
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER-P27		OUTPUT	LOW	HIGH		VCC_3V3_SYS
				IO EXP	ANDER - 02					
1	M.2 module Bluetooth LDO Enable	BT_EN_SOC	ENABLE	IO EXPANDER-P00		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
2	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER-P01		OUTPUT	LOW	HIGH		VCC_3V3_SYS
3	M.2 Interface Level Translator Enable	WL_LT_EN	ENABLE	IO EXPANDER-P10		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
4	SoC I2C2 & MCAN MUX Selection	SoC_I2C2_MCAN_SEL	CONTROL	IO EXPANDER-P20		OUTPUT	HIGH	-		VCC_3V3_SYS
5	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER-P21		OUTPUT	HIGH	LOW		VCC_3V3_SYS
6	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER-P22		OUTPUT	HIGH	LOW		VCC_3V3_SYS
7	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER-P23		OUTPUT	HIGH	LOW		VCC_3V3_SYS
8	OLDI display Reset control GPIO	GPIO_OLDI_RSTn	RESET	T IO EXPANDER-P24		OUTPUT	HIGH	LOW		VCC_3V3_SYS
9	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	RESET	IO EXPANDER-P25		OUTPUT	HIGH	LOW		VCC_3V3_SYS
10	eMMC Reset control GPIO	GPIO_EMMC_RSTn	RESET	IO EXPANDER-P26		OUTPUT	HIGH	LOW		VCC_3V3_SYS
11	WLAN Reset control GPIO	SOC_WLAN_SDIO_RST	RESET	IO EXPANDER-P27		OUTPUT	HIGH	LOW		VCC_3V3_SYS

2.20 Power

2.20.1 Power Requirement

AM62P SK EVM can be powered through either of the two USB Type-C connectors:

- Connector1 (J17) Power role SINK, No Data role
- Connector2 (J19) Power role DRP, Data role USB 2.0 DFP or UFP

The AM62P SK EVM supports voltage input ranges of 5V–15V and 3A of current. A USB PD controller manufacturer part number TPS65988DHRSHR is used for PD negotiation upon cable detection to get necessary power required for the board. Connector 1 is configured to be an UFP Port and has no Data role. Connector 2 is configured as a DRP port, and can act as DFP only when the board is being powered by Connector 1. When both the connectors are connected to external power supply, the port with highest PD power contract are selected to power the board.

Table 2-13. Type C Port Power Roles

J17 (UFP)	J19 (DRP)	Board Power	Remarks		
Plugged in	NC	ON - J17	J17 are UFP and only sinks power and J19 can act as DFP if a peripheral is connected.		
NC	Plugged in	ON - J19	J19 is UFP and can only sink power.		
Plugged in	ged in Plugged in		Board is powered by the port with highest PD power contract.		

The PD IC uses an SPI EEPROM to load the necessary configuration on power up so SPI EEPROM can negotiate a power contract with a compatible power source.

The configuration file is loaded to the EEPROM using header J15. Once the EEPROM is programmed the PD obtains the configuration files through SPI communication. Upon loading the configuration file, the PD negotiates with the source to obtain the necessary power requirement.

Note

The EEPROM is pre-programmed with the configuration file for the operation of the PD controller.

Power indication LEDs are provided for both the USB Type-C connectors for the user to identify which connector is powering the SK EVM board. An external power supply (USB Type-C output) can be used to power the EVM but is not included as part of the SK EVM kit.

The external power supply requirements (USB Type-C) are:

Table 2-14. Recommended External Power Supply

DigiKey Part #	Manufacturer	Manufacturer Part #		
1939-1794-ND	GlobTek, Inc.	TR9CZ3000USBCG2R6BF2		
Q1251-ND	Qualtek	QADC-65-20-08CB		

Note

Minimum voltage: 5VDC, Recommended minimum current: 3000mA, maximum voltage: 15VDC, maximum current: 5000mA. Since SK-AM62P-LP implements USB PD for power, the device can negotiate to the highest voltage and current combination supported by both the device and power adapter. Therefore, if the power supply exceeds the maximum voltage and current requirements listed above, then the power supply is acceptable as long as the power adapter is compliant with the USB-C PD specification.

Hardware INSTRUMENTS

www.ti.com

2.20.2 Power Input

Both USB Type-C Connectors (VBUS and CC lines) are connected to a dual PD controller manufacturer part number TPS65988. The TPS65988 is a stand-alone USB Type-C and Power Delivery (PD) controller providing cable plug and orientation detection for two USB Type-C Connectors. Upon cable detection, the TPS65988 communicates on the CC wire using the USB PD protocol. When cable detection and USB PD negotiation are complete, the TPS65988 enables the appropriate power path. The two internal power paths of TPS65988 are configured as sink paths for the two Type-C ports and an external FET path is provided for Type-C CONN 2 to source 5V when acting as DFP. The external FET path is controlled by GPIO17/PP_EXT2 pin of the PD controller along with a resistor option to also enable using USB0 DRVVBUS from AM62P SoC.

TPS65988 PD controller can provide an output of 3A (15V maximum) through CC negotiation. The VBUS pins from both the Type C connectors are connected to the VBUS pins of the PD controller. The output of the PD is VMAIN which is supplied to onboard buck-boost and buck regulators to generate fixed 5V and 3.3V supply for the SK EVM.

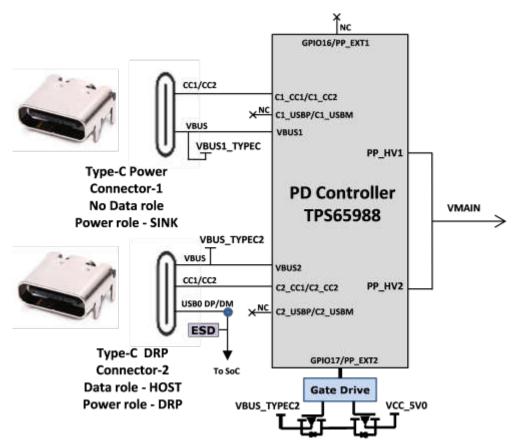


Figure 2-24. Power Input

2.20.3 Power Supply

AM62P SK EVM utilizes an array of DC-DC converters to supply the various memories, clocks, SoC, and other components and peripherals on the board with the necessary voltage and the power required.

Figure 2-25 shows the various discrete regulators, PMIC, and LDOs used to source power rails for each peripheral on AM62P SK EVM.

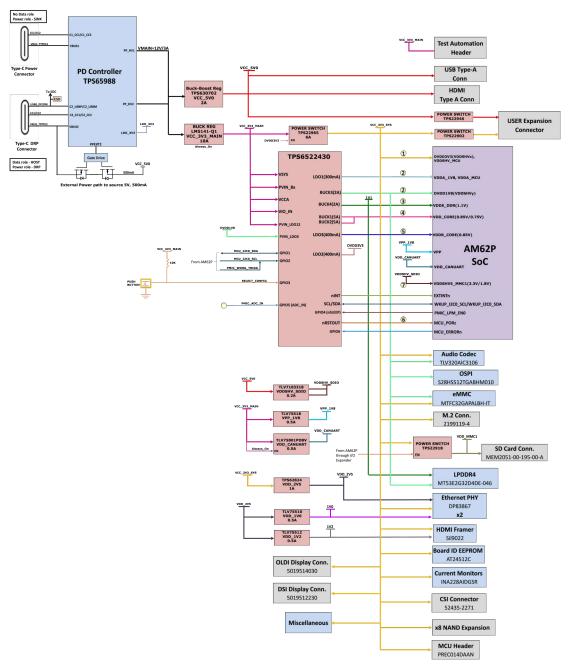


Figure 2-25. Power Architecture

The following sections describe the power distribution network topology that supplies the SK EVM board, supporting components and reference voltages.

The AM62P SK EVM includes a power design based on discrete power supply components. The initial stage of the power supply is VBUS voltage from either of the two USB Type-C connectors J17 and J19. USB Type-C dual

Hardware Superior INSTRUMENTS

www.ti.com

PD controller of manufacturer part number TPS65988DHRSHR is used for negotiation of the required power to the system.

Buck-boost controller TPS630702RNMR and buck converter LM5141-Q1 are used for the generation of 5V and 3.3V, respectively, and the input to the regulators is the PD output, VMAIN. These 3.3V and 5V are the primary voltages for the AM62P SK EVM board power resources. The 3.3V supply generated from the buck regulator LM5141-Q1 is the input supply to the PMIC, various SoC regulators and LDOs. The 5V supply generated from the buck-boost regulator TPS630702RNMR is used for powering the onboard peripherals.

Discrete regulators and LDOs used onboard are:

- TPS62824DMQR

 To generate VDD_2V5 rail for Ethernet PHYs
- TLV75510PDQNR

 To generate VDD_1V0 for Ethernet PHYs
- TLV75512PDQNR- To generate VDD 1V2 for HDMI Framer
- PTPS6522430RAHRQ1 (PMIC) To generate various SoC and Peripheral supplies
- TLV75801PDBVT LDO VDD CANUART power of SoC
- TPS79601LDO XDS110 Onboard emulator
- TPS73533LDO FT4232 UART to USB Bridge
- TLV7103318 LDO To generate VDDSHV5_MMC1 (SD interface) supply for SoC
- TLV75518 LDO eFuse programming of SoC

Additionally,GPIO (TEST_POWERDOWN) is connected to the ENABLE pin of PMIC to control ON/OFF of the SK EVM through XDS110/Test automation. GPIO also disables the VCC_5V0 output of TPS630702RNMR from which several other power supplies are derived.

2.20.4 Power Sequencing

The following image shows the Power Up sequence of the AM62P SoC power supplies.

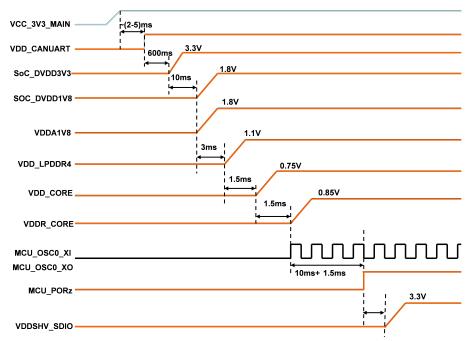


Figure 2-26. Power Sequence

2.20.5 AM62P SoC Power

The core voltage of the AM62P SoC can be 0.75V or 0.85V based on the PMIC Configuration and on the power optimization requirement. By default, the PMIC is configured to supply VDD_CORE at 0.85V, however the PMIC can be changed to 0.75V by removing R157. Current monitors are provided on all the SoC Power rails.

The SoC has different I/O groups. Each I/O group is powered by specific power supplies as listed in Table 2-15.

Table 2-15. SoC Power Supplies

SL. No.	Power Supply	SoC Supply Rail	IO Power Group	Voltage
		VDD_CORE	CORE	
		VDDA_CORE_CSI_DSI	CSI & DSI	
1	VDD_CORE	VDDA_CORE_DSI_CLK	DSI	0.75/0.85
		VDDA_DDR_PLL0	DDR PLL	
		VDDA_CORE_USB	USB	
2	VDD_CANUART (Always ON)	VDD_CANUART	CANUART	0.75/0.85
		VDDR_CORE	CORE	
3	VDDR_CORE	VDD_MMC0	MMC0	0.85
		VDDS_DLL_MMC0	MMC0	
		VDDA_1P8_CSI_DSI	CSI & DSI	
		VDDA_1P8_OLDI0	OLDI	
		VDDA_MCU	MCU	
4	VDDA_1V8	VDDS_OSC0	OSC0	1.8
		VDDA_PLL[0:4]	PLL	
		VDDA_TEMP[0:2]	TEMP	
		VDDA_1P8_USB	USB	
5	VDD_LPDDR4	VDDS_DDR	DDR0	1.1
J	VDD_LI DDIN4	VDDS_DDR_C	ВЫКО	1.1
6	CAN_IO_3V3 (Always ON)	VDDSHV_CANUART	CANUART	3.3
7	VPP_1V8	VPP_1V8		1.8
8	SOC_VDDSHV5_SDIO	VDDSHV5	MMC1	3.3/1.8
		VDDSHV1	OSPI	
9	SOC_DVDD1V8	VDDS_MMC0	MMC0	1.8
9	300_000100	VDDSHV6	MMC2	1.0
		VMON_1P8_SOC		
		VDDSHV0	GENERAL	
		VDDSHV2	GEMAC	
10	SOC_DVDD3V3	VDDSHV3	GPMC	3.3
10	300_0,000303	VDDSHV_MCU	MCU GENERAL	
		VMON_3P3_SOC		
		VDDA_3P3_USB	USB	

2.20.6 Current Monitoring

INA228 power monitor devices are used to monitor current and voltage of various power rails of AM62P SoC. The INA228 interfaces to the AM62P SoC through I2C interface (SoC_I2C1). Four terminal, high-precision shunt resistors are provided to measure load current.

Note

The design supports current/voltage measurements using either INA228 or INA231. INA228 is only populated on the SK (Implemented through stacked PCB footprint).

Table 2-16. INA I2C Device Address

Source	Supply Net	Device Address	Value of the Shunt
VCC_CORE	VDD_CORE	0x40	1 mΩ ± 1%
VDD_CORE_0V85	VDDR_CORE	0x41	10 mΩ ± 1%
VCC_3V3_SYS	SoC_DVDD3V3	0x4C	10 mΩ ± 1%

Hardware www.ti.com

Table 2-16. INA I2C Device Address (continued)

Source	Supply Net	Device Address	Value of the Shunt
VCC1V8_SYS	SoC_DVDD1V8	0x45	10 mΩ ± 1%
VDDA1V8	VDDA_1V8	0x4D	10 mΩ ± 1%
VCC1V1	VDD_LPDDR4	0x47	1 mΩ ± 1%

2.21 EVM User Setup/Configuration

2.21.1 DIP Switches

AM62P SK EVM has two 8-position DIP switches to set the desired SoC Boot mode.

2.21.2 Boot Modes

The boot mode for the SK EVM is defined by two banks of switches SW4 and SW5 or by the I2C buffer connected to the Test automation (XDS110 and Header). This allows for AM62P SoC Boot mode control by either the user (DIP Switch Control) or by the Test Automation.

All the bits of switch (SW4 and SW5) have a weak pulldown resistor and a strong pullup resistor. Note that OFF setting provides a low logic level ('0') and an ON setting provide a high logic level ('1').



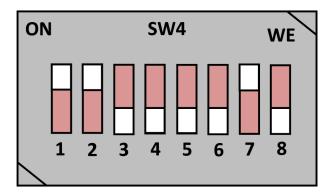


Figure 2-27. Boot Mode Switch (MMCSD Boot)

The boot mode pins of the SoC have associated alternate functions during normal operation. Hence isolation is provided using Buffer ICs to cater for alternate pin functionality. The output of the buffer is connected to the boot mode pins on the AM62P SoC and the output is enabled only when the boot mode is needed during a reset cycle.

The input to the buffer is connected to the DIP switch circuit and to the output of an I2C IO Expander set by the test automation circuit. If the test automation circuit controls the boot mode, then all the switches are manually set to the OFF position. The boot mode buffer is powered by an always ON power supply to make sure that the boot mode remains present even if the SoC is power cycled.

Switch SW4 and SW5 bits [15:0] are used to set the SoC Boot mode.

The switch map to the boot mode functions is provided in the tables below.

Table 2-17. Boot Mode Pin Mapping

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	Reserved	Backup boot mode configuration	Backup b	oot mode		Primary b			Primary b	oot mode			PLL confi	guration	

- BOOTMODE[2:0]— Denote system clock frequency for PLL configuration.
- The following table gives the details of PLL reference clock selection.

Table 2-18. PLL Reference Clock Selection BOOTMODE[2:0]

SW4.3	SW4.2	SW4.1	PLL REF CLK (MHz)
OFF	OFF	OFF	19.2
OFF	OFF	ON	20



Table 2-18. PLL Reference Clock Selection BOOTMODE[2:0] (continued)

SW4.3	SW4.2	PLL REF CLK (MHz)	
OFF	ON	OFF	24
OFF	ON	ON	25
ON	OFF	OFF	26
ON	OFF	ON	27
ON	ON ON		RSVD
ON	ON	ON	RSVD

 BOOTMODE[6:3] – This provides primary boot mode configuration to select the requested boot mode after POR, that is, the peripheral/memory to boot from primary boot device selection details.

Table 2-19. Boot Device Selection BOOTMODE[6:3]

SW4.7	SW4.6	SW4.5	SW4.4	Primary Boot Device Selected
OFF	OFF	OFF	OFF	Serial NAND
OFF	OFF	OFF	ON	OSPI
OFF	OFF	ON	OFF	QSPI
OFF	OFF	ON	ON	SPI
OFF	ON	OFF	OFF	Ethernet RGMII
OFF	ON	OFF	ON	Ethernet RMII
OFF	ON	ON	OFF	I2C
OFF	ON	ON	ON	UART
ON	OFF	OFF	OFF	MMC/SD card
ON	OFF	OFF	ON	eMMC
ON	OFF	ON	OFF	USB0
ON	OFF	ON	ON	GPMC NAND
ON	ON	OFF	OFF	GPMC NOR
ON	ON	OFF	ON	Rsvd
ON	ON	ON	OFF	xSPI
ON	ON	ON	ON	No boot/Dev Boot

• BOOTMODE[12:10] – Select the backup boot mode, that is, the peripheral/memory to boot from, if primary boot device failed.

Table 2-20. Backup Boot Mode Selection BOOTMODE[12:10]

SW5.5	SW5.4	SW5.3	Backup Boot Device Selected			
OFF	OFF	OFF	None (No backup mode)			
OFF	OFF	ON	USB			
OFF	ON	OFF	Reserved			
OFF	ON	ON	UART			
ON	OFF	OFF	Ethernet			
ON	OFF	ON	MMC/SD			
ON	ON	OFF	SPI			
ON	ON	ON	I2C			

 BOOTMODE[9:7] – These pins provide optional settings and are used in conjunction with the primary boot device selected.

Table 2-21. Primary Boot Media Configuration BOOTMODE[9:7]

:							
SW5.2	SW5.1	SW4.8	Boot Device				
Reserved	Read Mode 2	Read Mode 1	Serial NAND				
Reserved	Reserved	Csel	OSPI				
Reserved	Reserved	Csel	QSPI				

Hardware www.ti.com

Table 2-21. Primary Boot Media Configuration BOOTMODE[9:7] (continued)

SW5.2	SW5.1	SW4.8	Boot Device
Reserved	Mode	Csel	SPI
Clkout	0	Link Info	Ethernet RGMII
Clkout	Clk src	0	Ethernet RMII
Bus Reset	Reserved	Addr	I2C
Reserved	Reserved	Reserved	UART
1	Reserved	Fs/raw	MMC/ SD card
Reserved	Reserved	Reserved	eMMC
Core Volt	Mode	Lane swap	USB0
Reserved	Reserved	Reserved	GPMC NAND
Reserved	Reserved	Reserved	GPMC NOR
Reserved	Reserved	Reserved	Reserved
SFPD	Read Cmd	Mode	xSPI
Reserved	ARM/Thumb	No/Dev	No boot/Dev Boot

- BOOTMODE[13] These pins provide optional settings and are used in conjunction with the backup boot device devices. Switch SW 5.6 when ON sets 1 and sets 0 if OFF, see the device specific TRM.
- BOOT-MODE[15:14] Reserved. Provides backup boot media configuration options.

Table 2-22. Serial NAND Configuration Fields

BOOTMODE Pins	Field	Value	Description	
8 [SW5.1]	Read Mode 2	0	Reserved (Read mode is taken from Read Mode 1	
		1	SPI/ 1-1-1 mode (Read mode is taken from Read Mode 2 and Read Mode 1 is ignored)	
7 [SW4.8]	Read Mode 1	0	OSPI/ 1-1-8 Mode (valid only when Read Mode 2 is 0)	
		1	OSPI/ 1-1-4 Mode (valid only when Read Mode 2 is 0)	

Table 2-23. OSPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description		
7 [SW4.8]	Csel	0	Boot Flash is on CS 0		
		1	Boot Flash is on CS 1		

Table 2-24, QSPI Boot Configuration Fields

	Table 2 24. Qor i Boot Gornigaration i lotae				
BOOTMODE Pins	Field	Value	Description		
7 [SW4.8]	Csel	0	Boot Flash is on CS 0		
		1	Boot Flash is on CS 1		

Table 2-25. SPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
8 [SW5.1]	Mode	0	SPI Mode 0
		1	SPI Mode 3
7 [SW4.8]	Csel	0	Boot Flash is on CS 0
		1	Boot Flash is on CS 1

Table 2-26. Ethernet RGMII Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description	
9 [SW5.2]	Clkout	0	Must be set to 0 to choose external clock	
		1	Reserved	
8 [SW5.1]	Delay	0	Must be set to 0 for RGMII with internal Tx delay	
		1	Reserved	

Table 2-26. Ethernet RGMII Boot Configuration Fields (continued)

BOOTMODE Pins	Field	Value	Description
7 [SW4.8]	Link info	0	MDIO PHY scan used for link parameters
		1	Link parameters programmed by the ROM

Table 2-27. Ethernet RMII Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW5.2]	Clkout	0	50MHz clock not generated on CLKOUT0
		1	50MHz clock generated on CLKOUT0
8 [SW5.1]	Clk src	0	External clock source for RMII1_REF_CLK
		1	Internal clock source for RMII1_REF_CLK
7 [SW4.8]	RMII	0	This bit must be set to 0
		1	Reserved

Table 2-28. Ethernet RMII Clocking

DE Pin 9	BOOTMO DE Pin 8 (Clk src)	Description
0		50MHz external source to RMII_REF_CLK and to external Ethernet PHY input clock (CLKOUT0 is unused) These are the recommended settings
0	1	Not a valid configuration
1	0	CLKOUT0 is configured to 50 MHz and connect to both RMII1_REF_CLK and to external Ethernet PHY input clock
1	1	Not a valid configuration

Table 2-29. Ethernet Backup Boot Configuration Field

BOOTMODE Pins	Field	Value	Description
13 [SW5.2]	Interface	0 RGMII with internal TX delay	
	1		RMII with external clock source

Table 2-30. I2C Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW5.2]	Bus reset	0 Hung bus reset attempt after 1 ms	
		1	No hung bus reset attempted
7 [SW4.8]	Address	0 The address of the EEPROM is 0x50	
		1	The address of the EEPROM is 0x51

Table 2-31. SD Card Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW5.2]	Port	0	Reserved
13 [SW5.2] ⁽¹⁾		1	MMC Port 1 (4 bit width). This bit must be set to 1
7 [SW4.8]	FS/Raw	0	Filesystem mode
		1	Raw Mode

(1) When MMCSD is the backup mode.

Table 2-32. eMMC Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW5.2]	Port	0	MMCSD Port 0 (8 bit width). This bit must be set to 0
13 [SW5.2] ⁽¹⁾		1	Reserved
7 [SW4.8]	FS/Raw	0 Filesystem mode	
		1	Raw Mode

(1) When MMCSD is the backup mode.

Hardware Www.ti.com

Table 2-33. USB Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW5.2]	Core Voltage	0	0.85V core voltage
		1	0.75V core voltage
8 [SW5.1]	Mode	0	DFU (USB device firmware upgrade)
13 [SW5.2] ⁽¹⁾		1	Host (MSC boot)
7 [SW4.8]	Lane Swap 0 D+/D- lines are not swapped		D+/D- lines are not swapped
		1	D+/D- lines are swapped

(1) When USB is the backup mode.

Table 2-34. xSPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW5.2]	SFDP	0	SFDP disabled
		1	SFDP enabled
8 [SW5.1]	Read cmd	0	0x0B Read Command
		1	0xEE Read Command
7 [SW4.8]	Mode	Mode 0 1S-1S-1S mode at 50MHz	
		1	8D-8D-8D mode at 25MHz

2.21.3 User Test LEDs

The AM62P SK EVM consists of two LEDs for user defined functions.

Table 2-35 indicates the User test LEDs and the associated GPIOs used to control.

Table 2-35. User Test LEDs

SL.No.	LED	GPIO used	SCH Net Names
1	LD2	GPIO1_49	SOC_GPIO1_49
2	LD5	U105.24(P27)	IO_EXP_TEST_LED

2.22 Expansion Headers

AM62P SK EVM features three expansion Headers, a 40 pin User expansion connector, a 20 pin GPMC NAND (x8) connector and a 28 pin MCU Header.

2.22.1 User Expansion Connector

The AM62P SK EVM supports RPi expansion interface using a 40-pin user expansion connector manufacturer part number PEC20DAAN. Three mounting holes are oriented with the connector to allow for connection of any generic HAT boards.

The following interfaces and IOs are included on to the 40-pin user expansion connector:

- 2 × SPI: SPI0 with 2 CS and SPI2 with 3 CS
- 2 x I2C: SoC I2C0 and SoC I2C2
- 1 × UART: UART5
- 2 × PWM: EHRPWM0 A, EHRPWM1 B
- 1 × CLK: CLKOUT0
- 10 × GPI0: GPIOs from main domain
- 5Vand 3.3V supply (current limited to 155mA and 500mA)

Each of the power supplies 5V and 3.3V are current limited to 155mA and 500mA, respectively. This is achieved by using two individual load switch TPS22902YFPR and TPS22946YZPR. Enable for the load switches are controllable by an I2C-based GPIO port expander.

Table 2-36 lists the signals routed from the user expansion connector.

Table 2-36. User Expansion Connector (J4)

Table 2-36. User Expansion Connector (J4)			
Pin No.	SoC Ball	Net Name	
1	-	VCC3V3_EXP	
2	-	VCC5V0_EXP	
3	U25	EXP_I2C2_SDA	
4	-	VCC5V0_EXP	
5	T22	EXP_I2C2_SCL	
6	-	DGND	
7	C25	EXP_CLKOUT0	
8	F20	EXP_UART5_TXD	
9	-	DGND	
10	B23	EXP_UART5_RXD	
11	F24	EXP_SPI2_CS1	
12	G20	EXP_SPI2_CLK	
13	U23	EXP_GPIO0_42	
14	-	DGND	
15	A23	EXP_GPIO1_22	
16	AD24	EXP_GPIO0_38	
17	-	VCC3V3_EXP	
18	P24	EXP_GPIO0_39	
19	B20	EXP_SPI0_D0	
20	-	DGND	
21	C21	EXP_SPI0_D1	
22	L23	EXP_GPIO0_14	
23	B21	EXP_SPI0_CLK	
24	D20	EXP_SPI0_CS0	
25	-	DGND	
26	E20	EXP_SPI0_CS1	
27	A24	SOC_I2C0_SDA	
28	B25	SOC_I2C0_SCL	
29	T24	EXP_GPIO0_36	
30	R25	EXP_GPIO0_32	
31	R24	EXP_GPIO0_33	
32	P25	EXP_GPIO0_40/PR0_ECAP0_IN_APWM_OUT	
33	F23	EXP_EHRPWM1_B	
34	-	DGND	
35	G23	EXP_SPI2_CS0/EHRPWM0_A	
36	E24	EXP_SPI2_CS2	
37	T23	EXP_GPIO0_41	
38	E25	EXP_SPI2_D1/ECAP2_IN_APWM_OUT	
39	-	EXP_HAT_DETECT	
40	D25	EXP_SPI2_D0	
	1		

2.22.2 MCU Connector

AM62P SK EVM has a 14 × 2 standard 0.1" spaced MCU connector which includes signals connected to the MCU Domain of the SoC. The connected signals include MCU_I2C0, MCU_UART0 (with flow control), MCU_SPI0 and MCU_MCAN0 signals. Additional control signals connected on the header includes CONN_MCU_RESETz, CONN_MCU_PORz, MCU_RESETSTATz, MCU_SAFETY_ERRORn, 3.3V IO supply and GND. MCU_UART0 signals from AM62P SoC are connected to both MCU Header and FT4232 Bridge

Hardware www.ti.com

through a MUX manufacturer part number SN74CB3Q3257PWR. The MCU Header does not include the Board ID memory interface. The allowed current limit is 100mA on 3.3V rail.

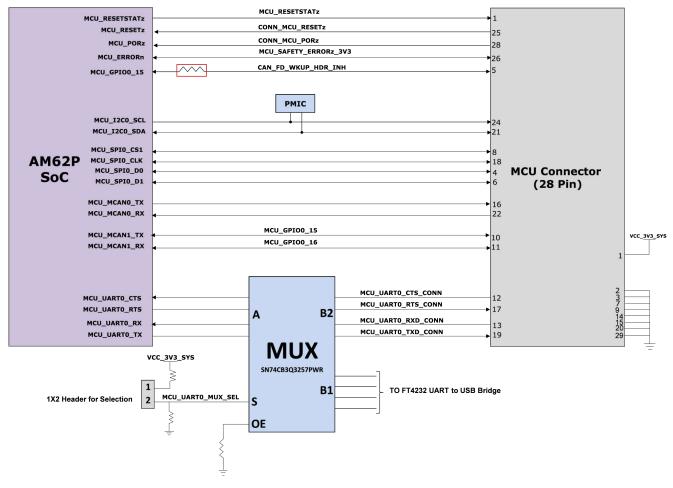


Figure 2-28. MCU Connector Interface

Table 2-37, MCU Connector (J11)

Table 2-37. MCO Confilector (311)				
Pin No.	SoC Ball No.	Net Name		
1	-	VCC_3V3_SYS		
2	-	DGND		
3	-	DGND		
4	D10	MCU_SPI0_D1		
5	F8	CAN_FD_WKUP_HDR_INH		
6	B11	MCU_SPI0_D0		
7	-	DGND		
8	E10	MCU_SPI0_CS1		
9	-	DGND		
10	F8	MCU_GPIO0_15		
11	E7	MCU_GPIO0_16		
12	B8	MCU_UART0_CTS_CONN		
13	B6	MCU_UART0_RXD_CONN		
14	-	DGND		
15	-	DGND		
16	E8	MCU_MCAN0_TX		
17	B7	MCU_UART0_RTS_CONN		

Table 2-37. MCU Connector (J11) (continued)

Pin No.	SoC Ball No.	Net Name
18	C10	MCU_SPI0_CLK
19	C8	MCU_UART0_TXD_CONN
20	-	DGND
21	D11	MCU_I2C0_SDA
22	D6	MCU_MCAN0_RX
23	F14	MCU_RESETSTATz
24	E11	MCU_I2C0_SCL
25	F11	CONN_MCU_RESETz
26	G6	MCU_SAFETY_ERRORz_3V3
27	-	DGND
28	H6	CONN_MCU_PORz

2.22.3 GPMC NAND (x8) Connector

The AM62P SK EVM supports GPMC NAND(x8) interface using a 20-pin standard 0.1" spaced connector manufacturer part number PREC010DAAN-RC. This connector includes GPMC_AD[0:7] signals which on power up executes prominent boot mode functions. The other control signals GPMC0_WEn, GPMC0_WAIT0 and GPMC0_BE0N_CLE can be routed to this connector by mounting RA5 and removing RA1. This connector is provided with a 3.3V supply to power any x8 NAND expansion card.

Note

User expansion connector and MCU Header can be used in conjunction with the GPMC NAND (x8) connector to expand number of control signals (for example, GPIO's & I2C) that can be required for the operation of a NAND memory device.

Table 2-38. GPMC NAND (x8) Connector (J14)

Pin No.	SoC Ball No.	Netname
1	-	VCC_3V3_SYS
2	-	DGND
3	-	x8_NAND_DETECT
4	-	NC
5	-	NC
6	-	NC
7	T25	GPMC0_WEn
8	-	NC
9	AA24	GPMC0_WAIT0
10	-	NC
11	U24	GPMC0_BE0N_CLE
12	-	NC
13	U22	GPMC0_AD0
14	U21	GPMC0_AD1
15	U20	GPMC0_AD2
16	V25	GPMC0_AD3
17	T20	GPMC0_AD4
18	T21	GPMC0_AD5
19	V24	GPMC0_AD6
20	W25	GPMC0_AD7

Hardware Www.ti.com

2.23 Interrupt

AM62P SK EVM supports two push buttons for providing reset input and a user generated interrupt to the AM62P SOC. These push buttons are placed on the Top side of the Board and are listed in Table 2-39.

Table 2-39. EVM Push Buttons

SL. No.	Push Buttons	Signal	Function
1	SW6	SoC_WARM_RESETZ	Main domain Warm Reset input
2	SW7	_	Generates interrupt on GPIO1_23 (UART0_RTSn)

2.24 I2C Address Mapping

There are five AM62P I2C instances communicating with the various peripherals in the SKEVM.

- SoC_I2C0 Interface: SoC I2C[0] is connected to Board ID EEPROM, User Expansion Connector, USB PD controller, OLDI display connector and DSI display connector.
- SOC_I2C1 Interface: SoC I2C[1] is connected to Test Automation Header, Current Monitors (x6), Temperature Sensors (x2), Audio Codec, HDMI Transmitter & GPIO Port Expander (x2).
- SOC I2C2 Interface: SoC I2C[2] is connected to the User Expansion Connector and CSI Camera connector.
- MCU I2C0 Interface: MCU I2C[0] is connected to the MCU Header & PMIC.
- WKUP_I2C0 Interface: WKUP I2C[0] is only connected to the PMIC.

Figure 2-29 depicts the I2C tree, and Table 2-40 provides the complete I2C address mapping details present on the AM62P SK EVM.

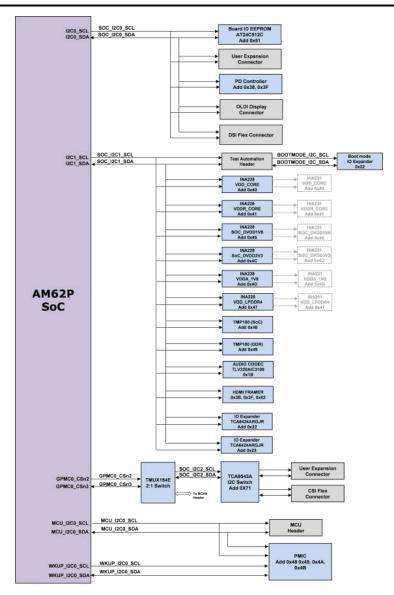


Figure 2-29. I2C Interface

Table 2-40. I2C Mapping Table

I2C Port	Device/Function	Part #	I2C Address
SoC_I2C0	Board ID EEPROM	AT24C512C-MAHM-T	0x51
	User Expansion Connector	<connector interface=""></connector>	
	USB PD Controller	TPS65988DHRSHR	0x38, 0x3F
	OLDI Display Connector	<connector interface=""></connector>	
	DSI Display Connector	<connector interface=""></connector>	
SoC_I2C1	Test Automation Header	<connector interface=""></connector>	
	Current Monitors	INA228AIDGSR	0x40, 0x41, 0x4C, 0x45, 0x4D and 0x47
	Temperature Sensors	TMP100NA/3K	0x48, 0x49
	Audio Codec	TLV320AIC3106IRGZT	0x1B
	HDMI Transmitter	Sil9022ACNU	0x3B, 0x3F, 0x62
	GPIO Port Expander	TCA6424ARGJR	0x22, 0x23
SoC_I2C2	CSI Camera Connector	<connector interface=""></connector>	
	User Expansion Connector	<connector interface=""></connector>	



Hardware Design Files www.ti.com

Table 2-40. I2C Mapping Table (continued)

I2C Port	Device/Function	Part #	I2C Address		
MCU_I2C0	MCU Header	<connector interface=""></connector>			
WKUP_I2C0	PMIC	PTPS6522430RAHRQ1	0x48, 0x49, 0x4A, 0x4B		
Others					
BOOTMODE_I2C	I2C Bootmode Buffer	TCA6424ARGJR	0x22		
	Test Automation Header	<connector interface=""></connector>			

3 Hardware Design Files

The hardware design files such as schematics, BOM, PCB Layout, Assembly Files and Gerber files are available in the link below.

Design Files

4 Compliance Information

4.1 Compliance and Certifications

EMC, EMI and ESD Compliance

Components installed on the product are sensitive to Electric Static Discharge (ESD). TI recommends this product be used in an ESD controlled environment. This can include a temperature or a humidity controlled environment to limit the buildup of ESD. TI also recommends to use ESD protection such as wrist straps and ESD mats when interfacing with the product.

The product is used in the basic electromagnetic environment as in laboratory conditions, and the applied standard is as per EN IEC 61326-1:2021.

ww.ti.com Additional Information

5 Additional Information

5.1 Known Hardware or Software Issues

This section describes the currently known issues on each EVM revision and applicable workarounds. Issues that are patched have modification labels attached to the EVM assembly.

Table 5-1. AM62P SK EVM Known Issues and Modifications

Issue Number	Issue Title	Issue Description	Variants Affected
1	Watchdog reset	PMIC Watchdog reset happens around 10 seconds.	E1
2	Power down sequence	PMIC not able to complete proper power down sequence	E1
3	Power cycling failure using TIVA	EVM experiencing issues with power cycling when in low power modes	E1, E1-1, E2

5.1.1 Issue 1 - Watchdog Reset

Applicable EVM Revisions: E1

Issue Description: Due to incorrect pull-up voltage on the PMIC watchdog disable pin (R124), the EVM is getting reset after around 10 seconds.

Fix: The pull-up voltage for R124 needs to be changed from VCC_3V3_SYS to VCC_3V3_MAIN. Change R131 pull-up voltage from VCC_1V8_SYS to VCC_3V3_SYS.

5.1.2 Issue 2 - Power Down Sequence

Applicable EVM Revisions: E1

Issue Description: Due to incorrect voltage (excessive capacitance) connection to the PMIC VSENSE pin, PMIC cannot able to complete the power down sequence before VCCA goes below threshold level.

Fix: The VSENSE pin input voltage are changed from VMAIN to dual voltage VBUS_TYPEC1 and VBUS_TYPEC2 through ORing diodes.

5.1.3 Issue 3 - Power Cycling Failure Using TIVA

Applicable EVM Revisions: E1, E1-1, E2

Issue Description: The EVM (Evaluation Module) was experiencing issues with power cycling when in low power modes (Active, DeepSleep, MCU Only, and Partial I/O) using the TIVA firmware. The board was unable to be turned on and off successfully in these states.

Fix:

Disconnect pre-reg enable pin from the 5V VMAIN supply by Removing R499. See Figure 5-1.

Connect the pre-reg enable pin to TEST_POWERDOWN by Connecting R75 (PAD: EN_LM5141_ON) to R246 (PAD: TEST_POWERDOWN). See Figure 5-2.

Disconnect the test automation supply from the pre-reg output by Removing R480. See Figure 5-1.

Supply the test automation with the TYPE-C DUAL PD CONTROLLER LDO-3V3 by Connecting TP201 to C115. See Figure 5-3.

Additional Information www.ti.com

PCBA Bottom

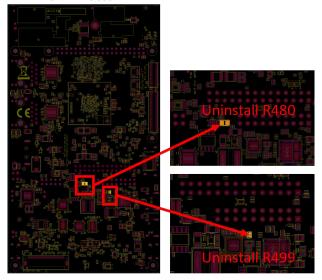


Figure 5-1. Disconnect Pre-reg Enable Pin

PCBA Top

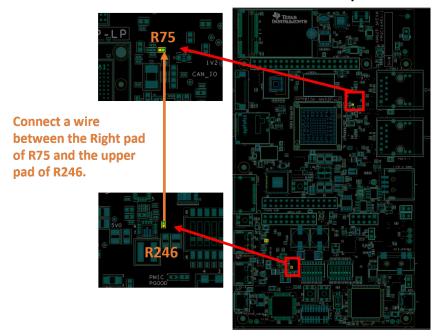


Figure 5-2. Connect the Pre-reg Enable Pin

www.ti.com Additional Information

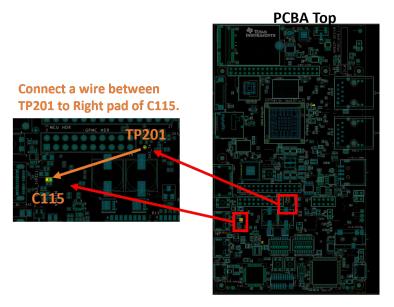


Figure 5-3. Supply the Test Automation With the TYPE-C PD LDO-3V3

5.2 Trademarks

Code Composer Studio™ is a trademark of Texas Instruments.

Arm® and Cortex® are registered trademarks of Arm Limited.

MIPI® is a registered trademark of MIPI Alliance, Inc.

Wi-Fi® is a registered trademark of Wi-Fi Alliance.

Bluetooth® is a registered trademark of Bluetooth SIG.

HDMI® is a registered trademark of HDMI Licensing LLC.

USB Type-C® and USB 2.0 Type-C® are registered trademarks of USB Implementers Forum, Inc.

is a registered trademark of USB Implementers Forum.

Molex® is a registered trademark of Molex, LLC.

Lattice Semiconductor Corporation® is a registered trademark of Lattice Semiconductor Corporation.

All trademarks are the property of their respective owners.

The terms HDMI, HDMI High-Definition Multimedia Interface, HDMI trade dress, and the HDMI Logos are trademarks or registered trademarks of HDMI Licensing Administrator Inc.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2023) to Revision A (October 2025)	Page
Changed starter kit name from SK-AM62A-LP to SK-AM62P-LP	
Updated Design Files link	1
Updated to single-core Arm Cortex-R5F MCU	
Added EVM PCB Design Revisions, and Assembly Variants table.	4
Added tables: Table 2-22 through Table 2-34	46
Changed SW5.1 for OSPI and QSPI to Reserved in Table 2-21	46
Updated footnote 1 to say Switch 5.6	46
Updated Design Files link	56
Added Issue 3 to Table 5-1	57

STANDARD TERMS FOR EVALUATION MODULES

- Delivery: TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or
 documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance
 with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.
 - 1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM ("Software") shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software
 - 1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.
- 2 Limited Warranty and Related Remedies/Disclaimers:
 - 2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.
 - 2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after the defect has been detected.
 - 2.3 Tl's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. Tl's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by Tl and that are determined by Tl not to conform to such warranty. If Tl elects to repair or replace such EVM, Tl shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI's recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI's recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI's instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 Regulatory Notices:

3.1 United States

3.1.1 Notice applicable to EVMs not FCC-Approved:

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- · Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types lated in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 Japan

- 3.3.1 Notice for EVMs delivered in Japan: Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
 - https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html
- 3.3.2 Notice for Users of EVMs Considered "Radio Frequency Products" in Japan: EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

- 1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
- 2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
- 3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above. User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの 措置を取っていただく必要がありますのでご注意ください。

- 1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用 いただく。
- 2. 実験局の免許を取得後ご使用いただく。
- 3. 技術基準適合証明を取得後ご使用いただく。
- なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。 上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・イ

ンスツルメンツ株式会社

東京都新宿区西新宿6丁目24番1号

西新宿三井ビル

- 3.3.3 Notice for EVMs for Power Line Communication: Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page 電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html
- 3.4 European Union
 - 3.4.1 For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

- 4 EVM Use Restrictions and Warnings:
 - 4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.
 - 4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.
 - 4.3 Safety-Related Warnings and Restrictions:
 - 4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.
 - 4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.
 - 4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.
- 5. Accuracy of Information: To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. Disclaimers:

- 6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.
- 6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.
- 7. USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS. USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

- 8. Limitations on Damages and Liability:
 - 8.1 General Limitations. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS, REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TIMORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.
 - 8.2 Specific Limitations. IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.
- 9. Return Policy. Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.
- 10. Governing Law: These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2023, Texas Instruments Incorporated

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025