User's Guide

J721S2, TDA4VE, TDA4AL, TDA4VL, AM68 Power Estimation Tool

ABSTRACT

The Excel-based J721S2 Power Estimation tool allows users to estimate thermal power based on specified loadings for different components (compute cores and peripherals) of the system-on-chip (SoC). The tool allows the user to pre-populate the various fields (which components are used, and utilization of the major components) from a set of representative use cases. This gives a starting point from which a new use case can be customized to judge the power and loadings of their own use case. The tool provides a breakdown of thermal power at the junction temperature (T_j) entered, and also provides a table of power delivery network (PDN) currents computed for this defined use case at T_j = 125°C or 105°C. The J721S2 Power Estimation tool supports the SOCs (e.g. J721S2, TDA4VE, TDA4AL, TDA4VL, AM68) in the J721S2 family.

The tool gives two power estimates:

1. Thermal power estimate: The time constant for heating or cooling an SoC is on the order of seconds or minutes. Because this is the primary use for the tool, the loadings represent the average activity over a duration of seconds or minutes.
2. Peak / PDN estimate: The time constant for peak current (power) is on the order of a microsecond. Though a use case (on average) can utilize a given component for say 70%, for windows of time that component is at 100% utilization. The tool's calculation for Peak / Power Delivery Network (PDN) estimates automatically increases the loading on key intellectual property (IP) that is enabled in order to create the PDN requirements.

Download the tool described in this document from https://www.ti.com/lit/zip/SPRUJ91A.

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Trademarks

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1 Contributions to Power

The SoC power is typically considered to have two different components – dynamic power and leakage.

The dynamic power is computed based upon two numbers for the IP – max power and idle power (both scaled to the voltage). The dynamic power is computed as the weighted average of the max and idle power:

$$P_{dyn} = P_{max} \times Utilization + P_{idle} \times (1 - Utilization) \quad (1)$$

- Dynamic power is typically computed as fCV. Consider a clock signal on a pcb that is driven from a CMOS output to a CMOS input. Dynamic power is computed based upon the (a) frequency of the signal – f; (b) the capacitance of the input load and the pcb trace capacitance – C; and (c) the voltage swing of the signal – V.
- Within the tool, the user can select the frequency for some IP as well as the IP's utilization. The frequency and utilization are obviously linked; as the frequency decreases, the utilization needs to increase to maintain *the same activity*. Therefore, a function that requires 40% loading on an IP has nearly the same power if the frequency is cut in half and the utilization doubles to 80%.

The leakage power is computed based on voltage, junction temperature, and manufacturing process variation. While the process and voltage have strong effects on the leakage power, the leakage power increases exponentially with T_j

- A CMOS transistor is considered to have two states: (a) ON in which the channel between source and drain is conducting; and (b) OFF in which the channel is non-conductive between the source and the drain. Leakage power arises because the OFF state can allow a trickle of current to cross the channel.

Note

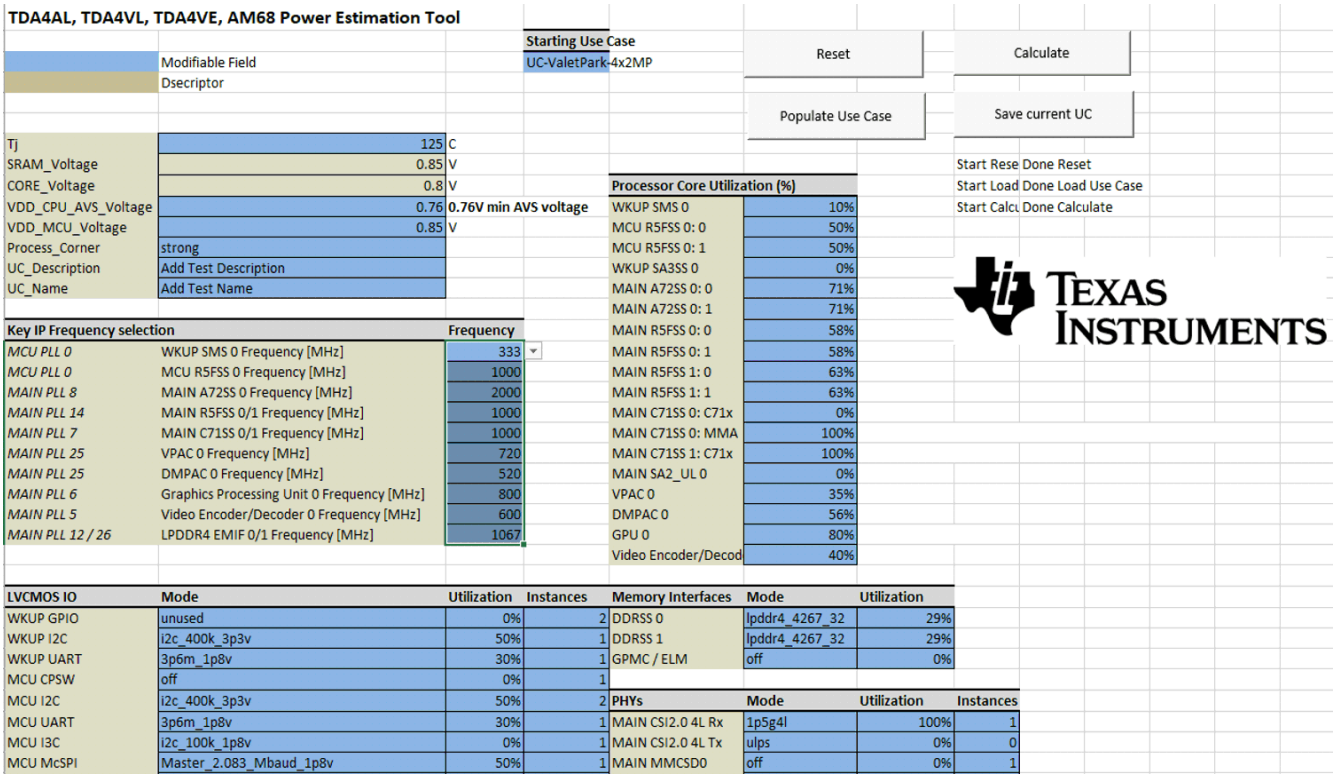
Analog / Bias Currents – There is a third component of the SoC power – analog or bias currents. These currents are not considered in this tool because in almost all cases the power contributed from these sources is negligible to the overall power.

2 How to Use the Tool

The tool has two pages:

- Use Case contains many different components that the user can configure to represent their use case; the use case is shown in Figure 2-1. (The individual largest contributors to the power are in column E.) This sheet also contains 4 buttons that initialize different phases of the estimate.
- Results is a blank sheet into which the results are populated.

Figure 2-1. Top of Use Case Tab of J721S2PowerEstimationTool_v0p2.xlsm



TDA4AL, TDA4VL, TDA4VE, AM68 Power Estimation Tool

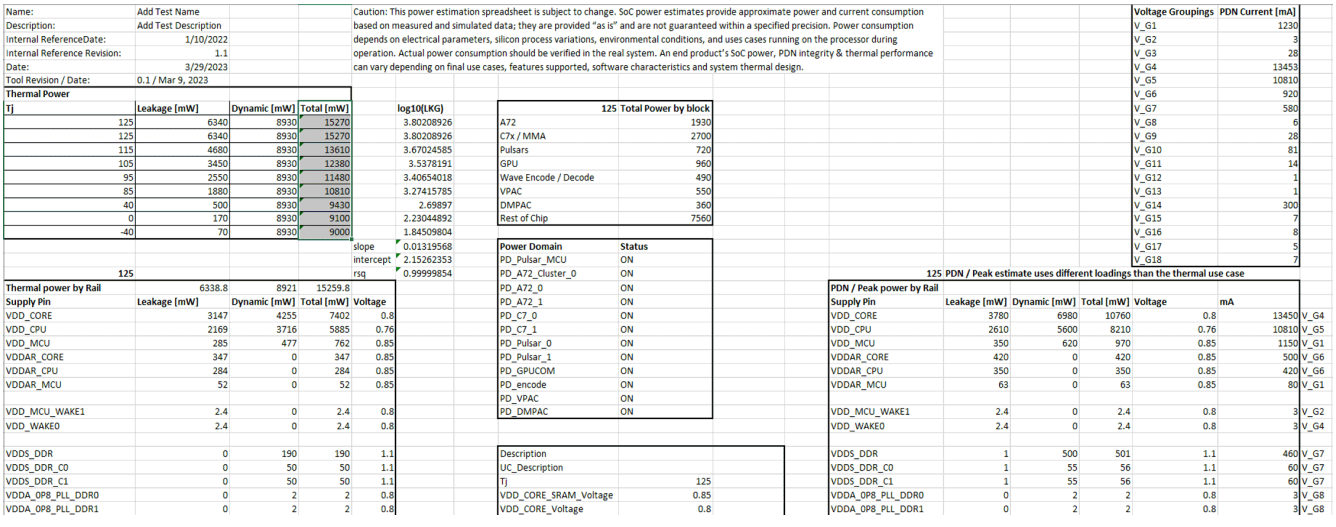
			Starting Use Case	Reset	Calculate	
	Modifiable Field		UC-ValetPark-4x2MP			
	Dsecriptor			Populate Use Case	Save current UC	
Tj	125	C				
SRAM_Voltage	0.85	V			Start Rese	Done Reset
CORE_Voltage	0.8	V		Processor Core Utilization (%)	Start Load	Done Load Use Case
VDD_CPU_AVS_Voltage	0.76	0.76V min AVS voltage		WKUP SMS 0 10%	Start Calcu	Done Calculate
VDD_MCU_Voltage	0.85	V		MCU R5FSS 0: 0 50%		
Process_Corner	strong			MCU R5FSS 0: 1 50%		
UC_Description	Add Test Description			WKUP SA3SS 0 0%		
UC_Name	Add Test Name			MAIN A72SS 0: 0 71%		
				MAIN A72SS 0: 1 71%		
Key IP Frequency selection		Frequency		MAIN R5FSS 0: 0 58%		
MCU PLL 0	WKUP SMS 0 Frequency [MHz]	333		MAIN R5FSS 0: 1 58%		
MCU PLL 0	MCU R5FSS 0 Frequency [MHz]	1000		MAIN R5FSS 1: 0 63%		
MAIN PLL 8	MAIN A72SS 0 Frequency [MHz]	2000		MAIN R5FSS 1: 1 63%		
MAIN PLL 14	MAIN R5FSS 0/1 Frequency [MHz]	1000		MAIN C71SS 0: C71x 0%		
MAIN PLL 7	MAIN C71SS 0/1 Frequency [MHz]	1000		MAIN C71SS 0: MMA 100%		
MAIN PLL 25	VPAC 0 Frequency [MHz]	720		MAIN C71SS 1: C71x 100%		
MAIN PLL 25	DMPAC 0 Frequency [MHz]	520		MAIN SA2_UL 0 0%		
MAIN PLL 6	Graphics Processing Unit 0 Frequency [MHz]	800		VPAC 0 35%		
MAIN PLL 5	Video Encoder/Decoder 0 Frequency [MHz]	600		DMPAC 0 56%		
MAIN PLL 12 / 26	LPDDR4 EMIF 0/1 Frequency [MHz]	1067		GPU 0 80%		
				Video Encoder/Decod 40%		

LVCMOS IO	Mode	Utilization	Instances
WKUP GPIO	unused	0%	2
WKUP I2C	i2c_400k_3p3v	50%	1
WKUP UART	3p6m_1p8v	30%	1
MCU CPSW	off	0%	1
MCU I2C	i2c_400k_3p3v	50%	2
MCU UART	3p6m_1p8v	30%	1
MCU I3C	i2c_100k_1p8v	0%	1
MCU McSPI	Master_2.083_Mbaud_1p8v	50%	1

Memory Interfaces	Mode	Utilization
DDRSS 0	lpddr4_4267_32	29%
DDRSS 1	lpddr4_4267_32	29%
GPMC / ELM	off	0%

PHYs	Mode	Utilization	Instances
MAIN CSI2.0 4L Rx	1p5g4l	100%	1
MAIN CSI2.0 4L Tx	ulps	0%	0
MAIN MMCSD0	off	0%	1

Figure 2-2. Top of Results Tab of J721S2PowerEstimationTool_v0p2.xlsm



Name:	Add Test Name
Description:	Add Test Description
Internal ReferenceDate:	1/10/2022
Internal Reference Revision:	1.1
Date:	3/29/2023
Tool Revision / Date:	0.1 / Mar 9, 2023

Caution: This power estimation spreadsheet is subject to change. SoC power estimates provide approximate power and current consumption based on measured and simulated data; they are provided "as is" and are not guaranteed within a specified precision. Power consumption depends on electrical parameters, silicon process variations, environmental conditions, and uses cases running on the processor during operation. Actual power consumption should be verified in the real system. An end product's SoC power, PDN integrity & thermal performance can vary depending on final use cases, features supported, software characteristics and system thermal design.

Thermal Power

Tj	Leakage [mW]	Dynamic [mW]	Total [mW]	log10(LKG)
125	6340	8930	15270	3.80208926
125	6340	8930	15270	3.80208926
115	4680	8930	13610	3.67024585
105	3450	8930	12380	3.5378191
95	2550	8930	11480	3.40654018
85	1880	8930	10810	3.27415785
40	500	8930	9430	2.69897
0	170	8930	9100	2.23044892
-40	70	8930	9000	1.84509804
			slope	0.01319568
			intercept	2.15262353
125			rsq	0.99999854

125 Total Power by block	
A72	1930
C7x / MMA	2700
Pulsars	720
GPU	960
Wave Encode / Decode	490
VPAC	550
DMPAC	360
Rest of Chip	7560

Power Domain	Status
PD_Pulsar_MCU	ON
PD_A72_Cluster_0	ON
PD_A72_0	ON
PD_A72_1	ON
PD_C7_0	ON
PD_C7_1	ON
PD_Pulsar_0	ON
PD_Pulsar_1	ON
PD_GPUCOM	ON
PD_encode	ON
PD_VPAC	ON
PD_DMPAC	ON

Thermal power by Rail				
Supply Pin	Leakage [mW]	Dynamic [mW]	Total [mW]	Voltage
VDD_CORE	3147	4255	7402	0.8
VDD_CPU	2169	3716	5885	0.76
VDD_MCU	285	477	762	0.85
VDDAR_CORE	347	0	347	0.85
VDDAR_CPU	284	0	284	0.85
VDDAR_MCU	52	0	52	0.85
VDD_MCU_WAKE1	2.4	0	2.4	0.8
VDD_WAKE0	2.4	0	2.4	0.8
VDDS_DDR	0	190	190	1.1
VDDS_DDR_C0	0	50	50	1.1
VDDS_DDR_C1	0	50	50	1.1
VDDA_0P8_PLL_DDR0	0	2	2	0.8
VDDA_0P8_PLL_DDR1	0	2	2	0.8

Description	
UC_Description	
Tj	125
VDD_CORE_SRAM_Voltage	0.85
VDD_CORE_Voltage	0.8

Voltage Groupings	PDN Current [mA]
V_G1	1230
V_G2	3
V_G3	28
V_G4	13453
V_G5	10810
V_G6	920
V_G7	580
V_G8	6
V_G9	28
V_G10	81
V_G11	14
V_G12	1
V_G13	1
V_G14	300
V_G15	7
V_G16	8
V_G17	5
V_G18	7

125 PDN / Peak estimate uses different loadings than the thermal use case

PDN / Peak power by Rail					
Supply Pin	Leakage [mW]	Dynamic [mW]	Total [mW]	Voltage	mA
VDD_CORE	3780	6980	10760	0.8	13450 V_G4
VDD_CPU	2610	5600	8210	0.76	10810 V_G5
VDD_MCU	350	620	970	0.85	1150 V_G1
VDDAR_CORE	420	0	420	0.85	500 V_G6
VDDAR_CPU	350	0	350	0.85	420 V_G6
VDDAR_MCU	63	0	63	0.85	80 V_G1
VDD_MCU_WAKE1	2.4	0	2.4	0.8	3 V_G2
VDD_WAKE0	2.4	0	2.4	0.8	3 V_G4
VDDS_DDR	1	500	501	1.1	460 V_G7
VDDS_DDR_C0	1	55	56	1.1	60 V_G7
VDDS_DDR_C1	1	55	56	1.1	60 V_G7
VDDA_0P8_PLL_DDR0	0	2	2	0.8	3 V_G8
VDDA_0P8_PLL_DDR1	0	2	2	0.8	3 V_G8

3 Use Case

3.1 Core Processor Utilization

This block allows the user to assign a utilization to each major core IP.

WKUP domain:

- SMS 0 – Arm Cortex-M4F based Security Management Subsystem
- SA3SS 0 – a collection of essential hardware accelerators supporting cryptography

MCU domain:

- Dual-R5F MCU Subsystem

Main domain:

- Dual-A72 MPU Subsystem
- 2x Dual-R5F MCU Subsystems
- C71x DSP Subsystem that includes a Matrix Multiplication Accelerator (MMA)
- C71x DSP Subsystem (standalone)
- SA2_UL is a collection of hardware accelerators supporting cryptography
- Vision Preprocessing Accelerator (VPAC)
- Depth and Motion Processing Accelerator (DMPAC)
- Graphics Processing Unit (GPU)
- Combination Video Encoder and Decoder

Processor Core Utilization (%)	
WKUP SMS 0	10%
MCU R5FSS 0: 0	50%
MCU R5FSS 0: 1	50%
WKUP SA3SS 0	0%
MAIN A72SS 0: 0	71%
MAIN A72SS 0: 1	71%
MAIN R5FSS 0: 0	58%
MAIN R5FSS 0: 1	58%
MAIN R5FSS 1: 0	63%
MAIN R5FSS 1: 1	63%
MAIN C71SS 0: C71x	0%
MAIN C71SS 0: MMA	100%
MAIN C71SS 1: C71x	100%
MAIN SA2_UL 0	0%
VPAC 0	35%
DMPAC 0	56%
GPU 0	80%
Video Encoder/Decod	40%

3.2 Key IP Frequency Selection

This block allows the user to select the frequency for the key blocks in the core utilization block (+DDR).

Note

VPAC / DMPAC – An important note on PLL25. Since the internal frequency of the PLL is limited to -3 GHz, the VPAC and DMPAC cannot simultaneously run at the highest frequency (720 MHz and 520 MHz, respectively) for both IPs.

Key IP Frequency selection		Frequency
MCU PLL 0	WKUP SMS 0 Frequency [MHz]	333
MCU PLL 0	MCU R5FSS 0 Frequency [MHz]	1000
MAIN PLL 8	MAIN A72SS 0 Frequency [MHz]	2000
MAIN PLL 14	MAIN R5FSS 0/1 Frequency [MHz]	1000
MAIN PLL 7	MAIN C71SS 0/1 Frequency [MHz]	1000
MAIN PLL 25	VPAC 0 Frequency [MHz]	720
MAIN PLL 25	DMPAC 0 Frequency [MHz]	520
MAIN PLL 6	Graphics Processing Unit 0 Frequency [MHz]	800
MAIN PLL 5	Video Encoder/Decoder 0 Frequency [MHz]	600
MAIN PLL 12 / 26	LPDDR4 EMIF 0/1 Frequency [MHz]	1067

3.3 Memory Interfaces

The J721S2 device family has 2 Double Data Rate (DDR) SDRAM controllers and associated physical layer interfaces (PHYs) as well as a General-Purpose Memory Controller (GPMC) with Error Location Module (ELM).

Memory Interfaces	Mode	Utilization
DDRSS 0	lpddr4_4267_32	29%
DDRSS 1	lpddr4_4267_32	29%
GPMC / ELM	off	0%

3.4 PHYs

The J721S2 device family has several PHYs; for the PHYs with multiple instances, in addition to the mode and the utilization, the user can also select how many of the instances are used:

- 2x Camera Stream Interface (CSI) 2.0 Receive PHYs each with 4 Lanes
- 2x CSI2.0 Transmit PHYs each with 4 Lanes
- Multi Media Card Interface (MMC) for eMMC only
- 2x Display Subsystem Display Serial Interface (DSI) Transmit interface (using the CSI2.0 Tx PHY)
- Universal Serial Bus (USB) 2.0 PHY

PHYs	Mode	Utilization	Instances
MAIN CSI2.0 4L Rx	1p5g4l	100%	1
MAIN CSI2.0 4L Tx	ulps	0%	0
MAIN MMCSD0	off	0%	1
MAIN DSS 0: DSI Tx	ulps	0%	2
USB2.0	sleep	0%	1

3.5 High Speed Serial Interface

There is one high speed serializing / deserializing (SerDes) interface on this device. The SerDes has 4 lanes for which the mode, utilization and IP is selected.

Note

The loading for the core portion of the IP is determined based upon the selected IP. The user defines what IP is driving the various lanes of the SerDes.

High Speed Serial Int	Mode	Utilization	IP	*(eDP, PCIe and USB share 1 4 lane SerDes)*
Lane0	disable	0%	none	
Lane1	disable	0%	none	
Lane2	disable	0%	none	
Lane3	disable	0%	none	

3.6 Environmental

The environmental section allows the user to define junction temperature (Tj), VDD_CPU_AVS voltage, VDD_MCU voltage, the process corner, and a use case name and description.

- the PDN / Peak estimate runs with Strong silicon and at either 105°C or 125°C.
- To save the use case, the user must supply a name for the use case.

Tj	125	C	
SRAM_Voltage	0.85	V	
CORE_Voltage	0.8	V	
VDD_CPU_AVS_Voltage	0.76	**0.76V min AVS voltage**	
VDD_MCU_Voltage	0.85	V	
Process_Corner	strong		
UC_Description	Add Test Description		
UC_Name	Add Test Name		

Note

Impact of User Selected Tj – If the user selects a junction temperature less than or equal to 105°C, the Peak / PDN estimate is computed for 105°C. If the user-selected junction temperature is greater than 105°C, then the Peak / PDN estimate is carried out at 125°C.

3.7 LVCMOS IOs

Like the PHY section, the user enters mode, utilization, and instances for each LVCMOS. There is only one mode and utilization allowed per IP (customization is not supported since the corresponding IP blocks do not contribute significantly to the overall power). If a system uses multiple modes for an IP type, the highest power mode is used.

LVCMOS IO	Mode	Utilization	Instances
WKUP GPIO	unused	0%	2
WKUP I2C	i2c_400k_3p3v	50%	1
WKUP UART	3p6m_1p8v	30%	1
MCU CPSW	off	0%	1
MCU I2C	i2c_400k_3p3v	50%	2
MCU UART	3p6m_1p8v	30%	1
MCU I3C	i2c_100k_1p8v	0%	1
MCU McSPI	Master_2.083_Mbaud_1p8v	50%	1
MCU MCAN	12mbs_3p3v	10%	2
MCU ADC	on		2
MCU FSS 0: OSPI0 / Hype	unused	0%	1
MCU FSS OSPI1 (QSPI)	unused	0%	1

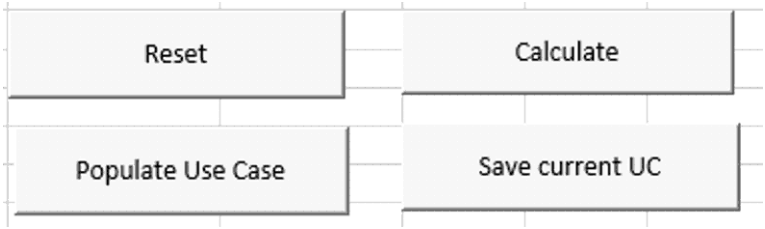
LVCMOS IO	Mode	Utilization	Instances
MAIN GPIO	unused	0%	0
MAIN I2C	i2c_400k_3p3v	50%	1
MAIN UART	3p6m_1p8v	30%	1
MAIN CPSW	off	0%	1
MAIN McSPI	Master_2.083_Mbaud_1p8v	50%	2
MAIN McASP	unused	0%	0
MAIN ECAP	unused	0%	0
MAIN EPWM	unused	0%	0
MAIN EQEP	unused	0%	0
MAIN MCAN	12mbs_3p3v	10%	2
MAIN MMCSD1	off	0%	1
MAIN DSS 0: DPI	off	0%	1

3.8 Buttons

The buttons initialize different phases of the power estimation.

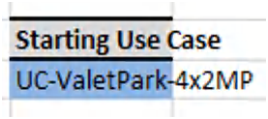
- Reset clears and resets the form as well as clearing results.
- Populate Use Case – Start any power estimate by using one of the pre-configured representative use cases. This helps to highlight how the tool can be used in a reasonable way (i.e., do not enter 100% for all of the IP on the SoC).
- Calculate – once the form is completed, calculate to populate data into the results sheet.
- Save current UC – once the user gets a test case competed, the case can be saved if a UC Name has been supplied. Once saved with a unique name, the case is part of the “Starting Use Case” list and is re-populated with the populate use case button. One particular note about re-populating use cases involves the SerDes and Display Sub-System. A SerDes bandwidth cannot map to the driving IP. As an example, an 8G Lane can be driven by the DSS or PCIe GEN 3. The user must, therefore, configure the SerDes IP and define what outputs the DSS is using. The tool applies loading to the IP designated by the SerDes and the DSS based upon these manual changes.

When each button is pushed, the cells underneath the button (H8:I11) record the start and stop times.



3.9 Starting Use Case

This drop down selects the use case to pre-populate. This set of use cases is supplemented when the user saves the current UC (with the buttons described prevously). The pre-populated use cases are intended to provide TI-generated starting points for the customer’s use case.



4 Results Sheet

The Results sheet gives information based upon the use case entered.

4.1 Thermal Power Estimate

- The primary output of the estimation is shown in cells A7 to D17; this table gives the total power of the device at various temperatures.
- Since the leakage power is exponential, the leakage component can be computed at any temperature. The cells in F8:F20 allow this computation; the leakage power is:

$$P_{LKG} = 10^{mT_j + b} \quad (2)$$

- Cells A1 to B6 contain reference information about the tool and the use case.
- The power can be broken down by rail. Those results are provided in cell A21 to E91.
- Cells H3 to J86 provide information (utilization and frequencies) on the use case estimated.
- Cells H18 to I30 show how the device's power domains have been configured.
  - When possible, the tool powers OFF the power domain. If the user wants to keep the domain ON, load IP utilization within the domain at 0.1%.
  - Configure the software to match the expectations defined in the power estimate.
- Cells H8 to I16 show a breakdown of power by block. This table shows that significant power is present in the back-plane of the device.

Note

Voltage Domains, Power Domains, and Local Power Sleep Controllers – In the Environmental section of the Use Case tab, the user selects the voltage for configurable voltage domains. Within a voltage domain (e.g. VDD_CPU_AVS), some circuitry is placed within a power domain (e.g. C7x_0 and MMA are within PD_C7_0); the power domain can break the connection to the voltage domain if-and-only-if all of the IP within the power domain is unused. Circuitry within an off power domain, do not contribute power – leakage or dynamic – to the power budget. Within the power domain, IP is controlled by a local power sleep controller (LPSC) which controls the clock and reset to the IP. IP which is not clocked does not contribute dynamic power to the overall device power, but contributes leakage power unless the IP resides in an unpowered power domain.

Note that a voltage domain typically has some IP that is within a power domain and other IP that is not within a power domain.

4.2 Peak / PDN Power Estimate

- Cells L20 to R93 contain the by-rail Peak / PDN estimate. This estimate is derived from the entered use case.
  - Column R creates a label V_G1 through V_G18 (e.g. voltage group.) These labels can be modified by the user.
  - The same labels are present in cells P2-P19. If the user modifies the labels in column R, the labels can also be modified in this range. Cells Q2-Q19 sum the current for this voltage group.

5 Three Specific Pre-Loaded Use Case Results

The following three use cases are intended to span the expected range of thermal power for this device. A use case can fall outside of this range (Peak / PDN power falls outside of this range.)

Table 5-1. 125°C Thermal Power

Use Case	Leakage [mW]	Dynamic [mW]	Total [mW]
ARM only	4720	3950	8670
Superset	6340	10910	17250
Valet Park	6340	9270	15610

Table 5-2. 105°C Thermal Power

Use Case	Leakage [mW]	Dynamic [mW]	Total [mW]
ARM only	2570	3950	6520
Superset	3450	10910	14360
Valet Park	3450	9270	12720

Note

Leakage Power – Because all of the power domains are enabled in both Superset and Valet Park use cases, the leakage is the same in both these cases.

As noted, the exponential behavior of the leakage with junction temperature causes a significant decrease in leakage between 125°C and 105°C.

5.1 ARM Only

A minimum use case for this class of processors relies upon using the A72 cores and the PCIe and ethernet switch; in this case, the A72 cores are reduced from 2 GHz to 1 GHz.

In this configuration, many of the power domains are disabled:

Table 5-3. ARM-Only Power Domain Status

Power Domain	Status
PD_Pulsar_MCU	ON
PD_A72_Cluster_0	ON
PD_A72_0	ON
PD_A72_1	ON
PD_C7_0	OFF
PD_C7_1	OFF
PD_Pulsar_0	OFF
PD_Pulsar_1	OFF
PD_GPUCOM	OFF
PD_encode	OFF
PD_VPAC	OFF
PD_DMPAC	OFF

The device loading is:

Table 5-4. ARM-Only Device Configuration

Description		
UC_Description		
Tj	125	
VDD_CORE_SRAM_Voltage	0.85	
VDD_CORE_Voltage	0.8	
VDD_CPU_SRAM_Voltage	0.85	
VDD_CPU_Voltage	0.76	
VDD_MCU_SRAM_Voltage	0.85	
VDD_MCU_Voltage	0.85	
Process_Corner	strong	
A72 CPU	70%	1000
A72 CPU	70%	1000
Pulsar Main J7AEP	0%	1000
Pulsar Main J7AEP	0%	1000
C711 512k 1.1	0%	1000
C711 512k 1.1	0%	1000
MMA2	0%	1000
Pulsar MCU J7am	50%	1000
DSS7L_eDP_DSI J7AEP	0%	0
CSI_3RX_2TX	0%	0
DPHY 1.2 RX - 4L	0%	0
DPHY 1.2 RX - 4L	0%	ulps
DPHY 1.2 TX - 4L	0%	ulps
DPHY 1.2 TX - 4L	0%	ulps
GPU BXS4-64-256KB DUST	0%	800
GPU BXS4-64-256KB Rascal	0%	800
GPU BXS4-64-256KB Wrap	0%	800

Table 5-4. ARM-Only Device Configuration (continued)

Description		
DMPAC J7AEP	0%	520
VPAC3	0%	720
WAVE521CL Video Codec	0%	600
CPSW2X eAVB	80%	0
Hyperlink x2	0%	0
PCIE_G3 4L J7AM	20%	0
USB3P0TCx1 J7AEP	0%	0
EMMC 4 J7AEP	0%	0
EMMC 8 J7AEP	10%	0
LPDDR4-32 EMIF J7AEP EW	35%	1067
lpddr4-32 IO 4267	39%	lpddr4_4267_32
LPDDR4-32 EMIF J7AEP NS	0%	1067
lpddr4-32 IO 4267	0%	sleep
SerDes 10G Common	100%	1pll
SerDes 10G Lane	20%	8g
SerDes 10G Lane	20%	8g
SerDes 10G Lane	20%	8g
SerDes 10G Lane	20%	8g
SDIO - 1 bit	0%	off
Arasan HS400 8 bit	10%	hs400

And the thermal power for the device is:

Table 5-5. ARM-Only Thermal Power

Tj	Leakage [mW]	Dynamic [mW]	Total [mW]
125	4720	3950	8670
115	3480	3950	7430
105	2570	3950	6520
95	1900	3950	5850
85	1410	3950	5360
40	380	3950	4330
0	130	3950	4080
-40	60	3950	4010

5.2 Superset

A superset use case is when A72s, Pulsars, C71x and MMAs, GPU, DMPAC and VPAC are effectively maximized. In this example, the SerDes is also loaded.

In this configuration, note of the power domains are disabled.

Table 5-6. Superset Power Domain Status

Power Domain	Status
PD_Pulsar_MCU	ON
PD_A72_Cluster_0	ON
PD_A72_0	ON
PD_A72_1	ON
PD_C7_0	ON
PD_C7_1	ON
PD_Pulsar_0	ON
PD_Pulsar_1	ON

Table 5-6. Superset Power Domain Status (continued)

Power Domain	Status
PD_GPUCOM	ON
PD_encode	ON
PD_VPAC	ON
PD_DMPAC	ON

The device loading is:

Table 5-7. Superset Device Configuration

Description		
UC_Description		
Tj	125	
VDD_CORE_SRAM_Voltage	0.85	
VDD_CORE_Voltage	0.8	
VDD_CPU_SRAM_Voltage	0.85	
VDD_CPU_Voltage	0.76	
VDD_MCU_SRAM_Voltage	0.85	
VDD_MCU_Voltage	0.85	
Process_Corner	strong	
A72 CPU	80%	2000
A72 CPU	80%	2000
Pulsar Main J7AEP	71%	1000
Pulsar Main J7AEP	71%	1000
C711 512k 1.1	0%	1000
C711 512k 1.1	100%	1000
MMA2	100%	1000
Pulsar MCU J7am	50%	1000
DSS7L_eDP_DSI J7AEP	35%	0
CSI_3RX_2TX	25%	0
DPHY 1.2 RX - 4L	50%	2p5g4l
DPHY 1.2 RX - 4L	50%	2p5g4l
DPHY 1.2 TX - 4L	50%	2p5g4l
DPHY 1.2 TX - 4L	50%	2p5g4l
GPU BXS4-64-256KB DUST	80%	800
GPU BXS4-64-256KB Rascal	80%	800
GPU BXS4-64-256KB Wrap	80%	800
DMPAC J7AEP	100%	520
VPAC3	90%	720
WAVE521CL Video Codec	50%	600
CPSW2X eAVB	80%	0
Hyperlink x2	0%	0
PCIE_G3 4L J7AM	25%	0
USB3P0TCx1 J7AEP	40%	0
EMMC 4 J7AEP	0%	0
EMMC 8 J7AEP	20%	0
LPDDR4-32 EMIF J7AEP EW	35%	1067
lpddr4-32 IO 4267	39%	lpddr4_4267_32
LPDDR4-32 EMIF J7AEP NS	35%	1067
lpddr4-32 IO 4267	39%	lpddr4_4267_32

Table 5-7. Superset Device Configuration (continued)

Description		
SerDes 10G Common	100%	2pll
SerDes 10G Lane	50%	8g
SerDes 10G Lane	50%	8g
SerDes 10G Lane	0%	disable
SerDes 10G Lane	40%	5g
SDIO - 1 bit	0%	off
Arasan HS400 8 bit	20%	hs400

And the thermal power for the device is:

Table 5-8. Superset Thermal Power

Tj	Leakage [mW]	Dynamic [mW]	Total [mW]
125	6340	10910	17250
115	4680	10910	15590
105	3450	10910	14360
95	2550	10910	13460
85	1880	10910	12790
40	500	10910	11410
0	170	10910	11080
-40	70	10910	10980

5.3 Valet Park

A use case representative of the vision analytics features of the device – a surround view and valet park example.

In this configuration, none of the power domains are disabled:

Table 5-9. Valet Park Power Domain Status

Power Domain	Status
PD_Pulsar_MCU	ON
PD_A72_Cluster_0	ON
PD_A72_0	ON
PD_A72_1	ON
PD_C7_0	ON
PD_C7_1	ON
PD_Pulsar_0	ON
PD_Pulsar_1	ON
PD_GPUCOM	ON
PD_encode	ON
PD_VPAC	ON
PD_DMPAC	ON

The device loading is:

Table 5-10. Valet Park Device Configuration

Description		
UC_Description		
Tj	125	
VDD_CORE_SRAM_Voltage	0.85	
VDD_CORE_Voltage	0.8	
VDD_CPU_SRAM_Voltage	0.85	
VDD_CPU_Voltage	0.76	
VDD_MCU_SRAM_Voltage	0.85	
VDD_MCU_Voltage	0.85	
Process_Corner	strong	
A72 CPU	71%	2000
A72 CPU	71%	2000
Pulsar Main J7AEP	58%	1000
Pulsar Main J7AEP	63%	1000
C711 512k 1.1	0%	1000
C711 512k 1.1	100%	1000
MMA2	100%	1000
Pulsar MCU J7am	50%	1000
DSS7L_eDP_DSI J7AEP	70%	0
CSI_3RX_2TX	25%	0
DPHY 1.2 RX - 4L	100%	1p5g4l
DPHY 1.2 RX - 4L	0%	ulps
DPHY 1.2 TX - 4L	100%	2p5g4l
DPHY 1.2 TX - 4L	100%	2p5g4l
GPU BXS4-64-256KB DUST	80%	800
GPU BXS4-64-256KB Rascal	80%	800
GPU BXS4-64-256KB Wrap	80%	800

Table 5-10. Valet Park Device Configuration (continued)

Description		
DMPAC J7AEP	56%	520
VPAC3	35%	720
WAVE521CL Video Codec	40%	600
CPSW2X eAVB	0%	0
Hyperlink x2	0%	0
PCIE_G3 4L J7AM	0%	0
USB3P0TCx1 J7AEP	0%	0
EMMC 4 J7AEP	0%	0
EMMC 8 J7AEP	0%	0
LPDDR4-32 EMIF J7AEP EW	29%	1067
lpddr4-32 IO 4267	32%	lpddr4_4267_32
LPDDR4-32 EMIF J7AEP NS	29%	1067
lpddr4-32 IO 4267	32%	lpddr4_4267_32
SerDes 10G Common	0%	disable
SerDes 10G Lane	0%	disable
SerDes 10G Lane	0%	disable
SerDes 10G Lane	0%	disable
SerDes 10G Lane	0%	disable
SDIO - 1 bit	0%	off
Arasan HS400 8 bit	0%	off

And the thermal power for the device is:

Table 5-11. Valet Park Thermal Power

Tj	Leakage [mW]	Dynamic [mW]	Total [mW]
125	6340	9270	15610
115	4680	9270	13950
105	3450	9270	12720
95	2550	9270	11820
85	1880	9270	11150
40	500	9270	9770
0	170	9270	9440
-40	70	9270	9340

6 Summary of Power for Pre-Populated Use Cases

The following table summarizes the power for the pre-populated use cases. The ARM only, Superset, and Valet Park use cases align to the use cases in the previous section. The MCU only use case uses only a small portion of the device while the remainder is un-powered and is a special case. (The compute core and peripheral loadings can be viewed within the tool.)

Table 6-1. Thermal Power at 125°C

Use Case	Tj	Leakage [mW]	Dynamic [mW]	Total [mW]	Comments
ARM only	125	4720	3950	8670	Assign SerDes IP PCIe on all channels.
ARM + GPU + Display	125	5100	5520	10620	Set MAIN DSS 0: DSI TX to 2p5g4l; 90% on 2 PHYs. Assign SerDes IP PCIe on all channels.
ARM + VPAC + Deep Learning	125	5540	7120	12660	Assign SrDes IP to PCIe.
Front Camera (2.5MPix, Edge)	125	5630	5560	11190	
Front Camera (5MPix, Edge)	125	5960	6190	12150	
Front Camera (8MPix, Edge)	125	5960	6400	12360	
8MP (front) + 3MP (rear)	125	6060	6330	12390	Set MAIN DSS 0: DSI TX 2p5g4l; 70%; 2 PHYs.
Valet Park	125	6340	9270	15610	Set MAIN DSS 0: DSI TX set to 2p5g4l; 100%; 2 PHYs.
Superset	125	6340	10910	17250	Set MAIN DSS 0: DSI TX 2p5g4l; 50%, 2 PHYs; assign SerDes IP with PCIe (8G) and USB (5G).
MCU only	125	370	760	1130	Set SRAM Voltage, CORE Voltage and CPU voltage to 0 V.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from April 4, 2023 to May 17, 2023 (from Revision * (Apr 2023) to Revision A (May 2023)) Page

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