User's Guide

AM263Px LaunchPad User Guide

Description

The AM263Px LaunchPad™ development kit is a simple and inexpensive hardware evaluation module (EVM) for the Texas Instruments™ Sitara™ AM263Px series of microcontrollers (MCUs). This EVM provides an easy way to start developing on the AM263Px MCUs with onboard emulation for programming and debugging as well as buttons and LEDs for a simple user interface. The LaunchPad also features two independent BoosterPack XL expansion connectors, onboard Controller Area Network (CAN) transceiver, two RJ45 Ethernet ports, and an onboard XDS110 debug probe.

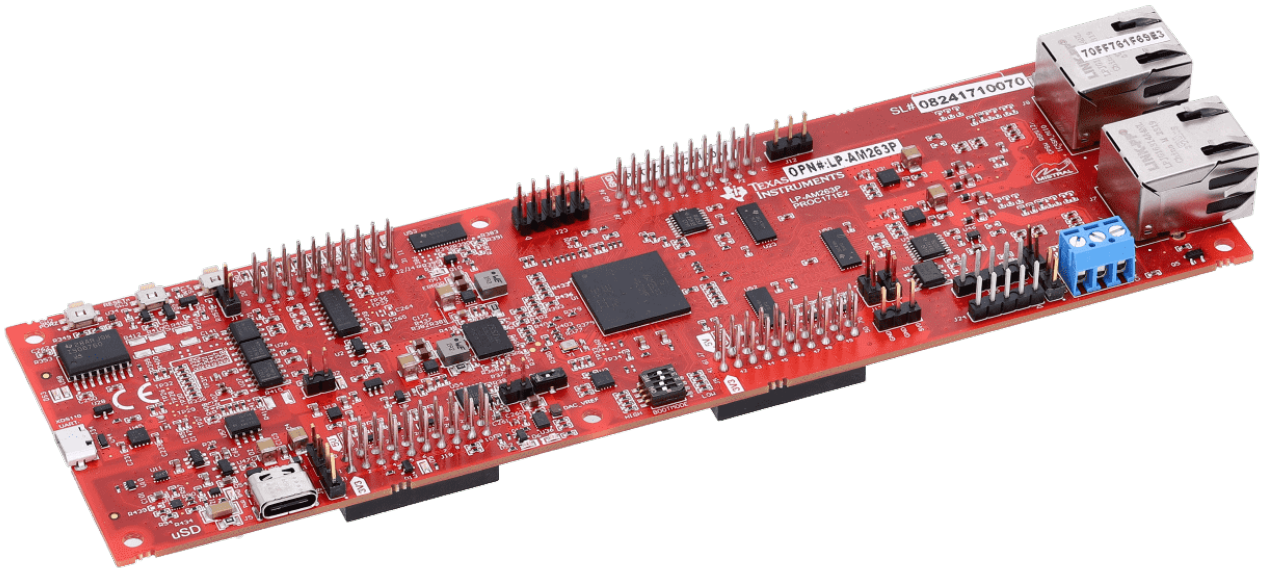

Table of Contents

List of Figures

List of Tables

1 Key Features

The AM263Px LaunchPad has the following features:

- PCB dimensions: 195.56mm X 58.42mm
- Powered through 5V, 3A USB type-C input
- Two RJ45 Ethernet ports capable of 1Gbps speeds
- Onboard XDS110 debug probe
- Three push buttons:
  - PORz
  - User interrupt
  - RESETz
- LEDs for:
  - Power status
  - Power NOT Good
  - User testing
  - Ethernet connection
  - I2C driven array
- CAN connectivity with onboard CAN transceiver
- Dedicated FSI connector
- Discrete DC-DC buck regulators and LDOs that generate the required supplies with an additional option of Vpp LDO 1.7 (TLV75801PDRVR) as DNP
- TI Test Automation Header
- TIVA Test Automation Header
- MMC interface to micro SD card connector. Also a footprint option for users to mount eMMC, like MTFC8GAMALBH-AT. Currently the eMMC is made DNP.
- Two independent Enhanced Quadrature Encoder Pulse (EQEP) based encoder connectors
- Two independent BoosterPack XL (40 pin) standard connectors featuring stackable headers to maximize expansion through the BoosterPack ecosystem
- Onboard memory:
  - 256 Mb OSPI Flash
  - 1 Mb I2C Board ID EEPROM

2 LaunchPad Module Overview

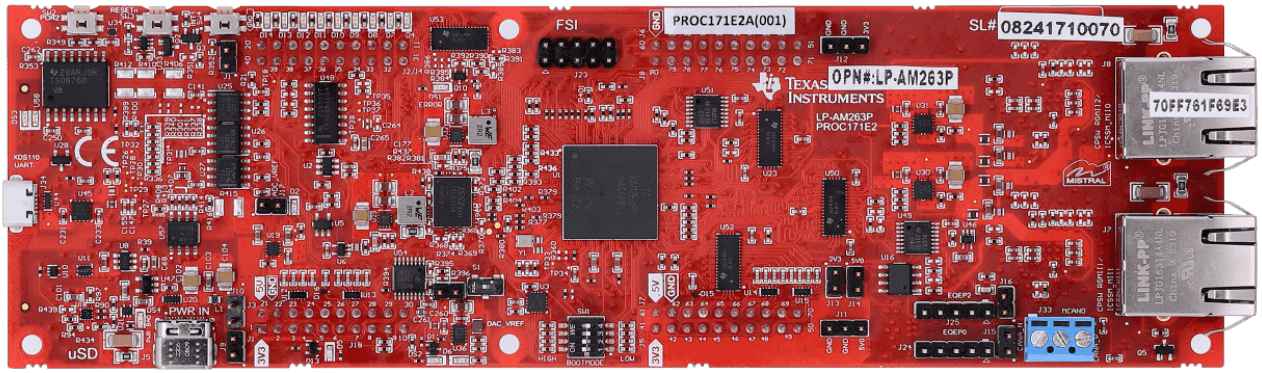

Figure 2-1. AM263Px LaunchPad Board

2.1 Introduction

This user's guide details the design of the EVM and how to properly use each interface. The user's guide also details many important aspects of the board including but not limited to power requirements, boot mode selections, and mux/switch signal routing.

2.2 Preface: Read This First

2.2.1 If You Need Assistance

If you have any feedback or questions, support for the Sitara MCUs and the AM263Px LaunchPad development kit is provided by the TI Product Information Center (PIC) and the TI E2E™ Forum. Contact information for the PIC can be found on the TI website. Additional device-specific information can be found in the Reference Documents.

2.2.2 Important Usage Notes

Caution	Caution Hot surface. Contact may cause burns. Do not touch!

Note

The AM263Px LaunchPad requires a 5V, 3A power supply to function. A 5V, 3A power supply is not included in the kit and must be ordered separately. The *Belkin USB-C Wall Charger* is known to work with the LaunchPad and supplied type-C cable. For more information on power requirements refer to Power Requirements. If there is an insufficient power input then the red LED (DS1) will glow. For more information on power status LEDs refer to Power Status LEDs.

Note

External Power Supply or Power Accessory Requirements:

- Nominal output voltage: 5VDC
- Max output current: 3000mA
- Power Delivery

Note

TI recommends using an external power supply or accessory which complies with applicable regional safety standards such as (by example) UL, CSA, VDE,CCC,PSE, etc.

2.3 Kit Contents

The Sitara AM263Px Series LaunchPad Development Kit contains the following items:

- AM263Px Sitara Series LaunchPad development board
- USB micro-B cable
- Micro SD card
- CAT5 Ethernet cable

The kit does not include:

- USB type-C 5V/3A AC/DC supply
- USB type-C cable

2.4 Device Information

2.4.1 System Architecture Overview

The below image shows the overall top level architecture of the AM263Px LaunchPad.

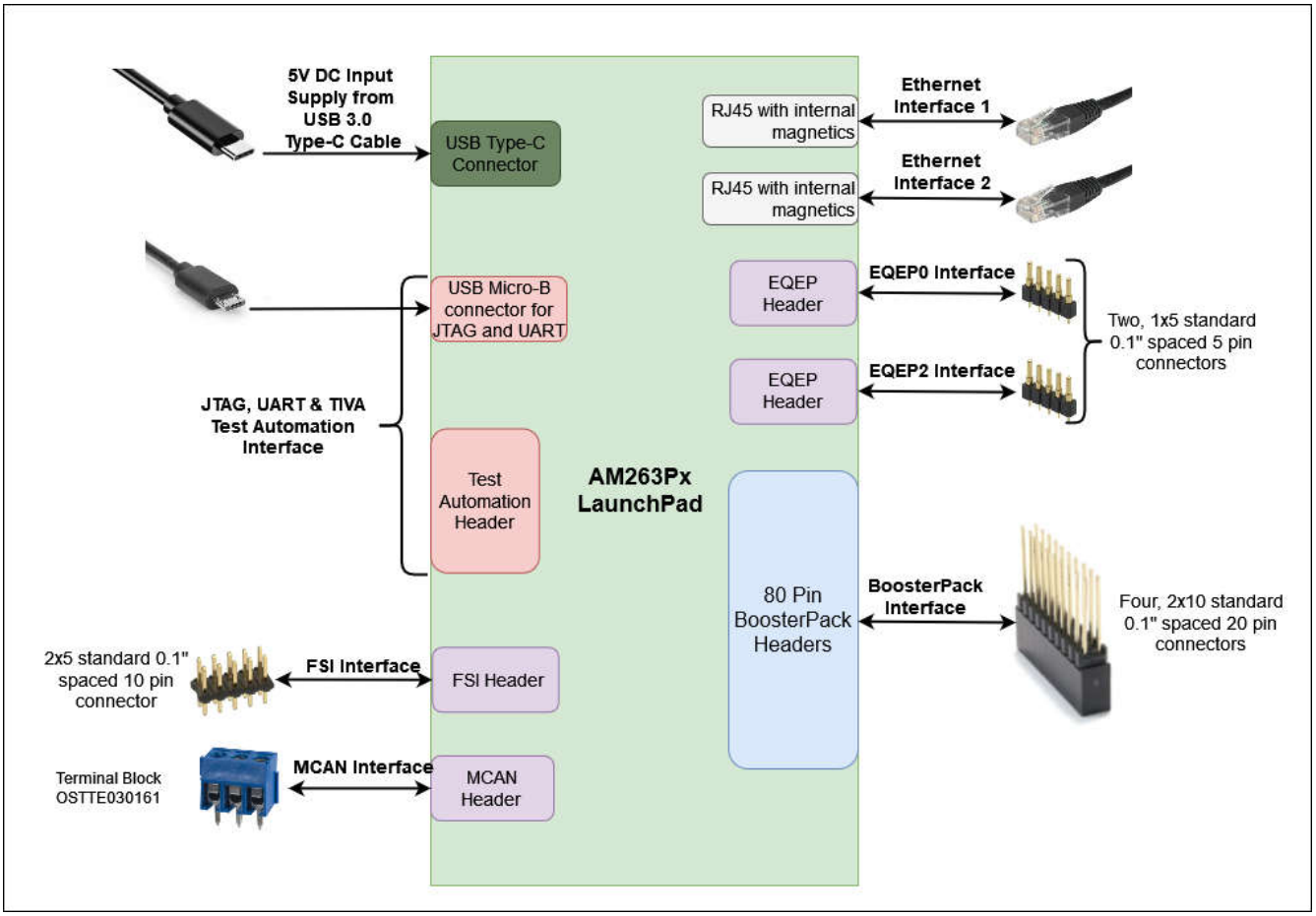

Figure 2-2. System Architecture

2.4.2 Security

The AM263Px LaunchPad features a High Security, Field Securable (HS-FS) device. An HS-FS device has the ability to use a one time programming to convert the device from HS-FS to High Security, Security Enforced (HS-SE) device.

The AM263Px device leaves the TI factory in an HS-FS state where customer keys are not programmed and has the following attributes:

- Does not enforce the secure boot process
- M4 JTAG port is closed
- R5 JTAG port is open
- Security Subsystem firewalls are closed
- SoC Firewalls are open
- ROM Boot expects a TI signed binary (encryption is optional)
- TIFS-MCU binary is signed by the TI private key

The One Time Programmable (OTP) keywriter converts the secure device from HS-FS to HS-SE. The OTP keywriter programs customer keys into the device efuses to enforce secure boot and establish a root of trust. The secure boot requires an image to be encrypted (optional) and signed using customer keys, which will be verified by the SoC. A secure device in the HS-SE state has the following attributes:

- M4, R5 JTAG ports are both closed
- Security Subsystems and SoC Firewalls are both closed
- TIFS-MCU and SBL need to be signed with active customer key

2.4.3 Compliance

All components selected meet RoHS compliance.

2.4.4 BoosterPacks

The AM263Px LaunchPad development kit provides an easy and inexpensive way to develop applications with the AM263Px Series microcontroller. BoosterPacks are add-on boards that follow a pin-out standard created by Texas Instruments. The TI and third-party ecosystem of BoosterPacks greatly expands the peripherals and potential applications that you can easily explore with the AM263Px LaunchPad. For a detailed diagram on the pin-out of the AM263Px LaunchPad, refer to BoosterPack Headers.

You can also build your own BoosterPack by following the design guidelines on TI's website. Texas Instruments even helps you promote your BoosterPack to other members of the community. TI offers a variety of avenues for you to reach potential customers with your solutions.

2.4.5 Component Identification

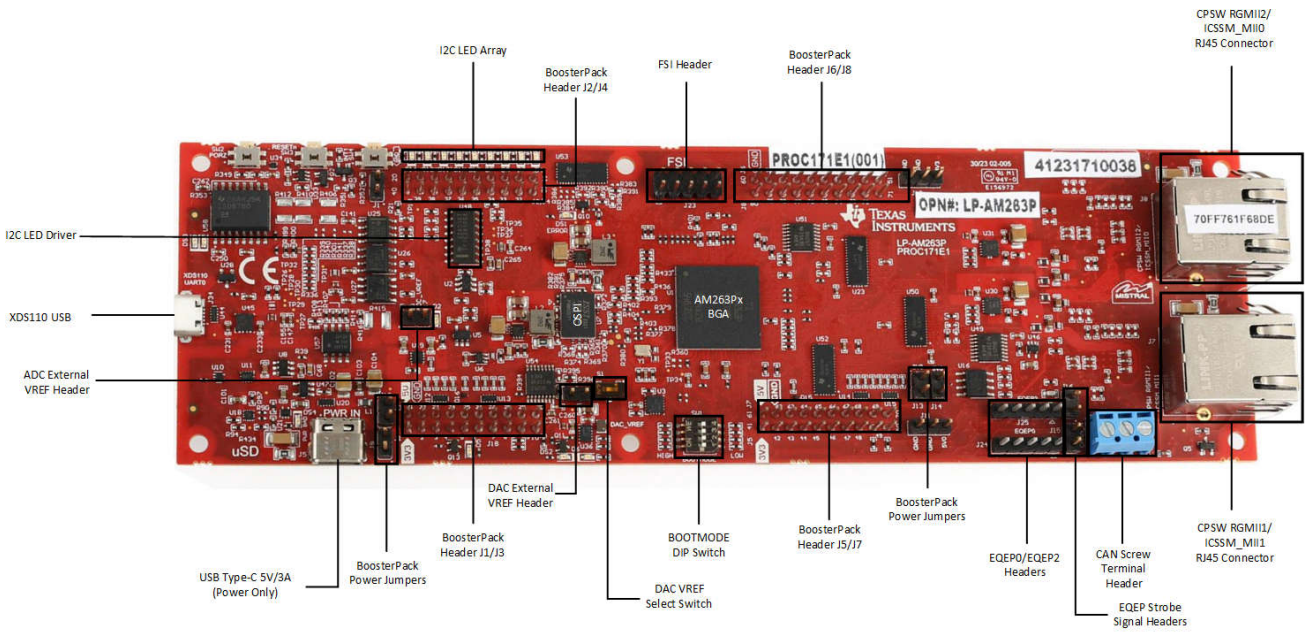

Figure 2-3. AM263Px LaunchPad Top Components Identification

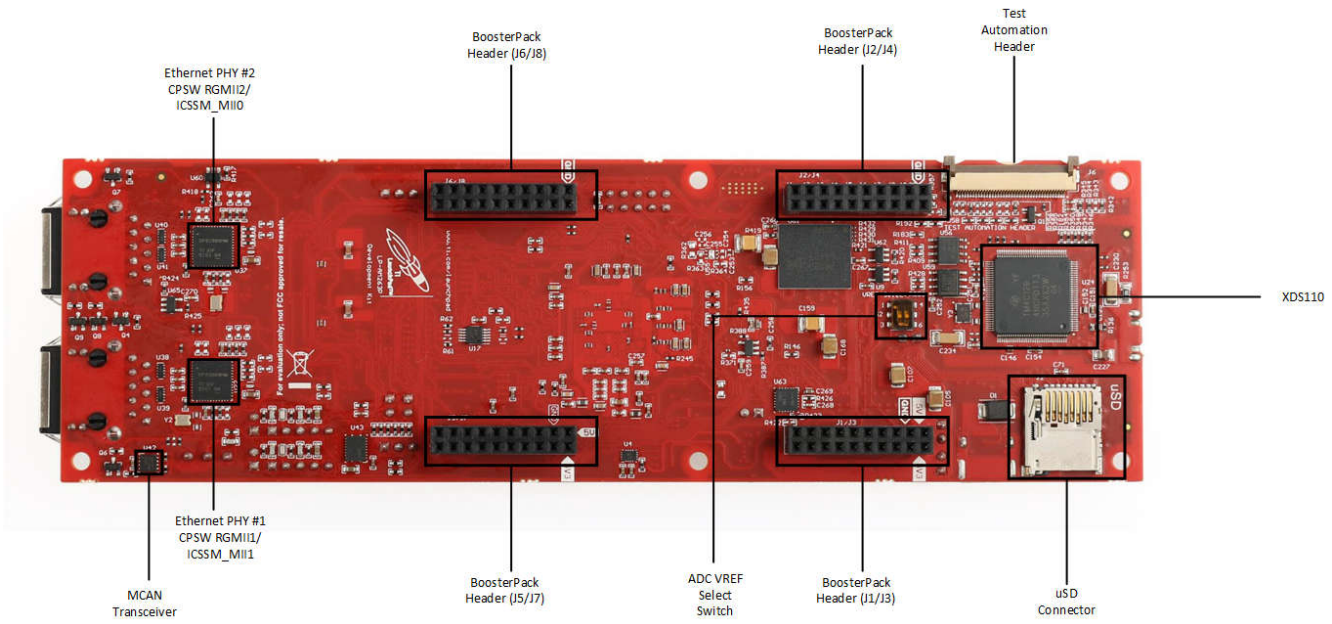

Figure 2-4. AM263Px LaunchPad Bottom Components Identification

3 Hardware Description

3.1 Board Setup

3.1.1 Power Requirements

The AM263Px LaunchPad is powered from a 5V, 3A USB type-C input. The following sections describe the power distribution network topology that supply the AM263Px LaunchPad, supporting components and the reference voltages.

Power supply solutions that are compatible with the AM263Px LaunchPad:

- When using the USB type-C input:
  - 5V, 3A power adapter with USB-C receptacle
  - 5V, 3A power adapter with captive USB-C cable
  - PC USB type-C port that has Power Delivery classification
    - Thunderbolt
    - Battery behind USB logo

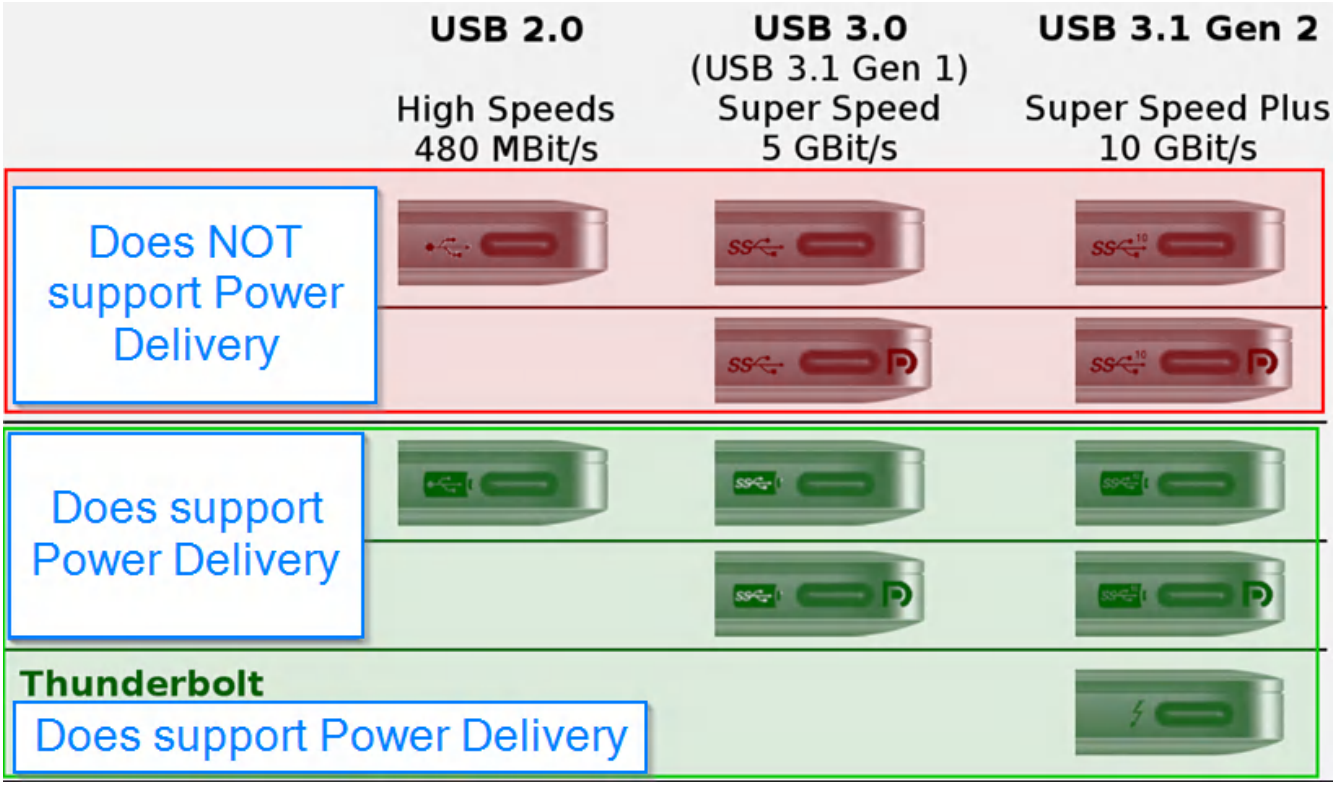

Figure 3-1. USB Type-C Power Delivery Classification

Power supply solutions that are **NOT** compatible with the AM263Px LaunchPad:

- When using USB type-C input:
  - Any USB adapter cables such as:
    - Type-A to type-C
    - micro-B to type-C
    - DC barrel jack to type-C
  - 5V, 1.5A power adapter with USB-C captive cable or receptacle
  - PC USB type-C port not capable of 3A

3.1.1.1 Power Input Using USB Type-C Connector

The AM263Px LaunchPad is powered through a USB type-C connection. The USB Type-C source should be capable of providing 3A at 5V and should advertise the current sourcing capability through CC1 and CC2 signals. On AM263Px LaunchPad, the CC1 and CC2 from USB type-C connector are interfaced to the port controller IC (TUSB320). This device uses the CC pins to determine port attach and detach, cable orientation, role detection, and port control for Type-C current mode. The CC logic detects the Type-C current mode as default, medium, or high depending on the role detected.

The Port pin is pulled down to ground with a resistor to configure it as upward facing port (UFP) mode. VBUS detection is implemented to determine a successful attach in UFP mode. The OUT1 and OUT2 pins are connected to a NOR gate. Active low on both the OUT1 and OUT2 pins advertises high current (3A) in the attached state which enables the VUSB_5V0 power switch to provide the VSYS_5V0 supply which powers other regulators and LDOs.

In UFP mode, the port controller IC constantly presents pull down resistors on both CC pins. The port controller IC also monitors the CC pins for the voltage level corresponding to the Type-C mode current advertisement by the connected DFP. The port controller IC de-bounces the CC pins and waits for VBUS detection before successfully attaching. As a UFP, the port controller device detects and communicates the advertised current level of the DFP to the system through the OUT1 and OUT2 GPIOs.

The AM263Px LaunchPad power requirement is 5V at 3A and if the source is not capable of providing the required power, the output at the NOR gate becomes low that disables the VUSB_5V0 power switch. Therefore, if the power requirement is not met, all power supplies except VCC3V3_TA remains in the off state. The board gets powered on completely only when the source can provide 5V at 3A.

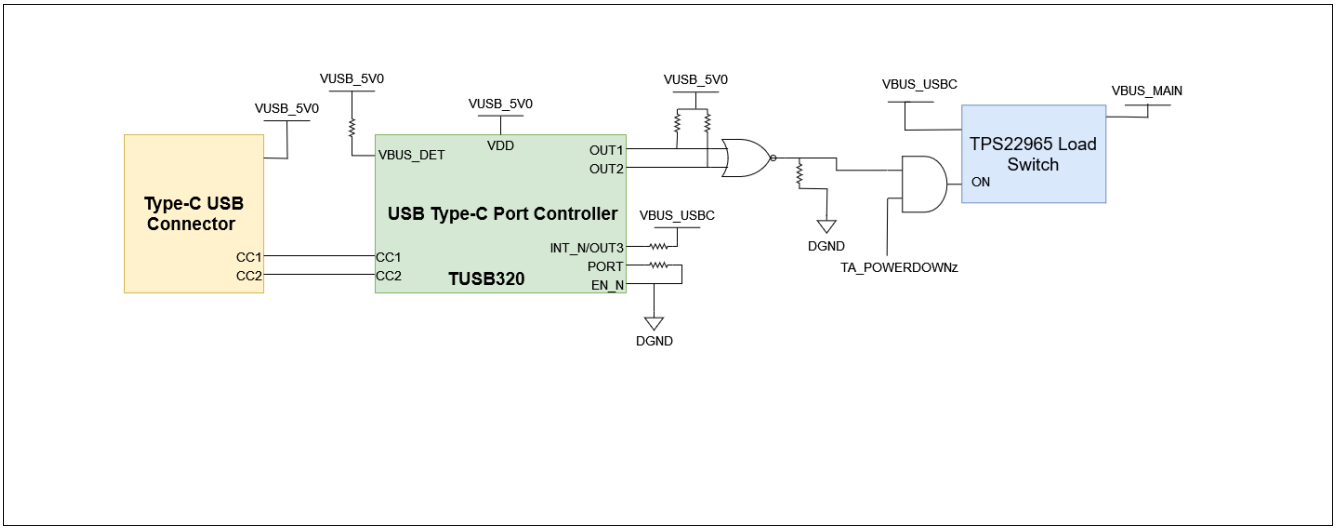

Figure 3-2. Type-C CC Configuration

Table 3-1. Current Sourcing Capability and State of USB Type-C Cable

OUT1	OUT2	Advertisement
H	H	Default current in unattached state
H	L	Default current in attached state
L	H	Medium current (1.5A) in attached state
L	L	High current (3.0A) in attached state

The AM263Px LaunchPad includes a power solution based on discrete regulators for each of the power rails. During the initial stage of the power supply, 5V supplied by the type-C USB connector is used to generate all of the necessary voltages required by the LaunchPad.

Discrete DC-DC buck regulators and LDOs are used to generate the supplies required for the AM263Px system on a chip (SoC) and other peripherals.

Table 3-2. Voltage Rail Generation

Component	Reference Designator	Function	Voltage In	Voltage Out
TPS62913	U29	AM263Px Core Digital 1.2V	5.0V	1.2V
TPS74801	U32	System 3.3V	5.0V	3.3V
TSP74801	U30	Ethernet PHY 2.5V	5.0V	2.5V
TPS74801	U31	Ethernet PHY 1.1V	5.0V	1.1V
TPS62177	U36	Test Automation Header 3.3V	5.0V	3.3V

3.1.1.2 Power Status LEDs

Multiple power-indication LEDs are provided onboard to indicate to users the output status of major supplies. The LEDs indicate power across various domains.

Table 3-3. Power Status LEDs

Name	Default Status	Operation	Function
D2	ON	VSYS_5V0	Power indicator for generated 5V voltage
D4	ON	VSYS_3V3	Power indicator for generated 3.3V voltage
D5	ON	PG_VDD_1V2	Power indicator for generated 1.2V power-good voltage
D6	ON	VSYS_TA_3V3	Power indicator for voltage going to the Test Automation Header
DS1	OFF	SAFETY_ERROR	Power error indication for voltage - VUSB_5V0
D3	OFF	XDS_PROGSTAZ1	LED will glow after micro-B connection is made
DS3	OFF	XDS_PROGSTAZ2	LED will glow to indicate communication over JTAG
DS4	OFF	VUSB_5V0	Power NOT Good (Power Bad)

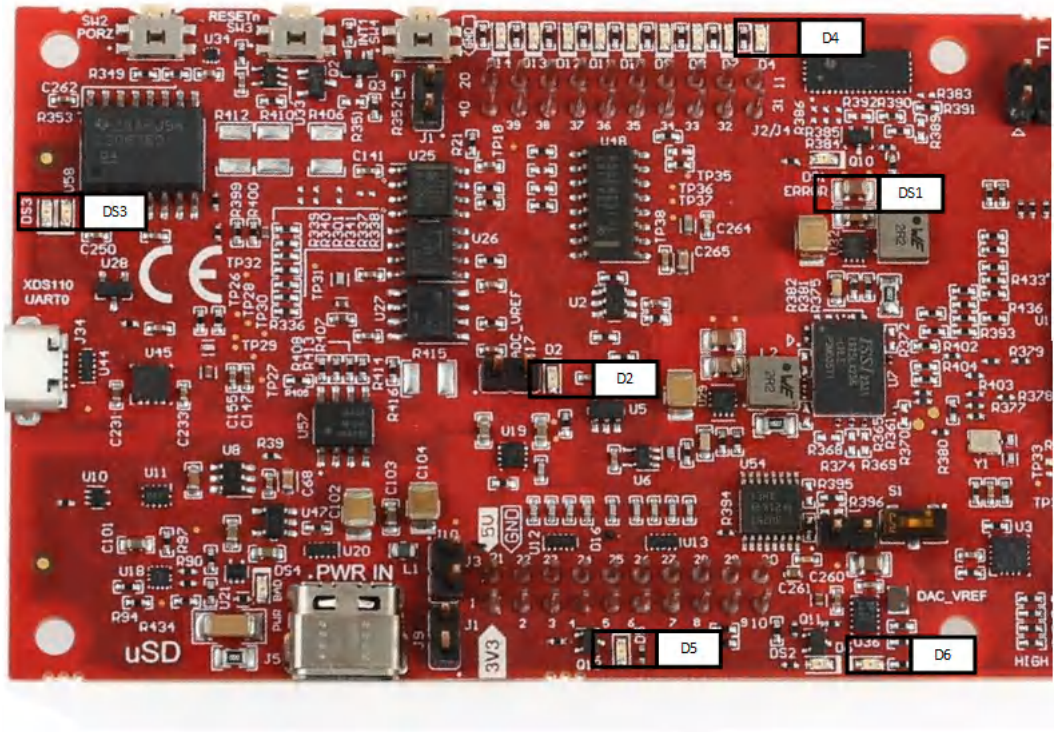

Figure 3-3. Power Status LEDs

3.1.1.3 Power Tree

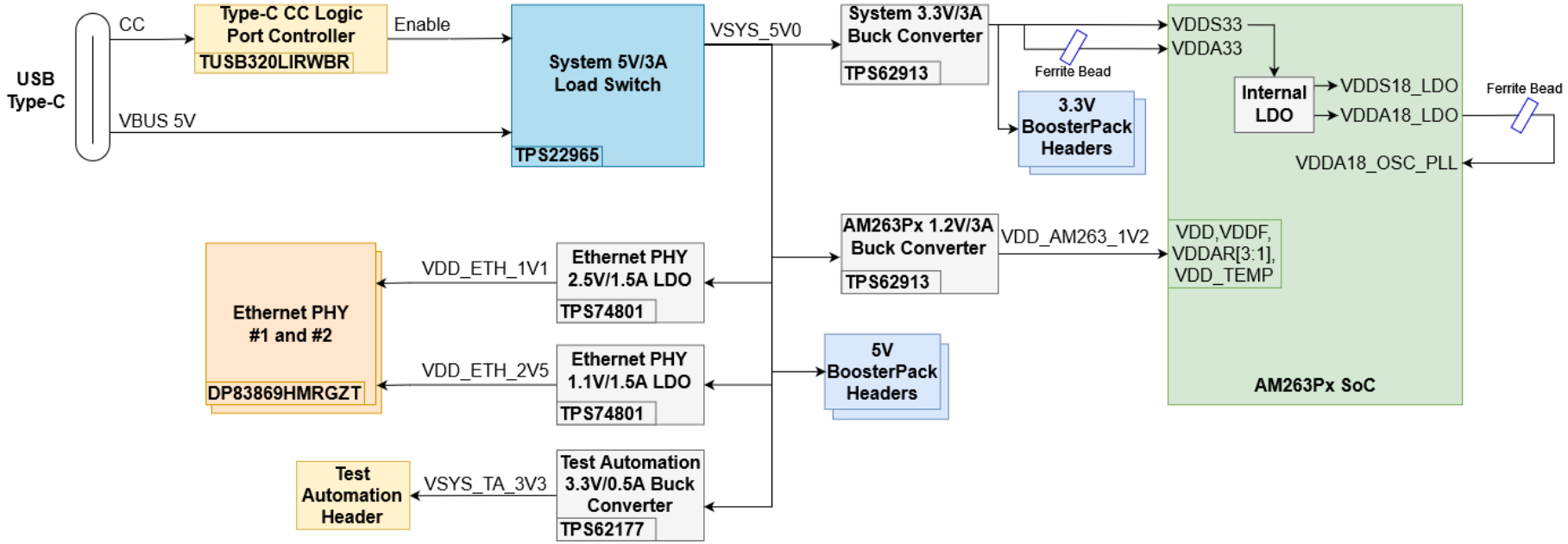

Figure 3-4. Power Tree Diagram of AM263Px LaunchPad

3.1.2 Push Buttons

The LaunchPad supports multiple user push buttons that provide reset inputs and user interrupts to the AM263Px SoC.

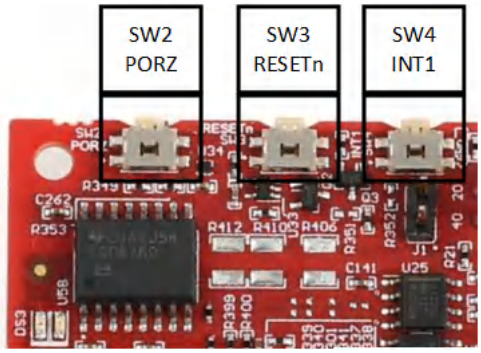

Figure 3-5. Push Buttons

Table 3-4 lists the push buttons that are placed on the top side of the AM263Px LaunchPad.

Table 3-4. LaunchPad Push Buttons

Push Button	Signal	Function
SW2	PORz	SoC PORz reset input
SW3	RESETz	SoC warm reset input
SW4	INT1	User Interrupt Signal

3.1.3 Boot mode Selection

The boot mode for the AM263Px is selected by a DIP (Dual In-Line Package) switch (SW1) or the test automation header. The test automation header uses an I2C expansion buffer to drive the boot mode when PORz is toggled. The supported boot modes are shown in Table 3-6. The DIP Switch configurations for each boot mode are shown in Table 3-5.

Note

As seen in the schematic, enabling(toggling to ON state) a switch pulls the respective SOP pin to GND through a 1kΩ resistor. Thus the Boot mode selection switches' logic table below is logical invert of the corresponding SOP logic levels for a given boot mode, as seen in AM263P Technical Reference Manual.

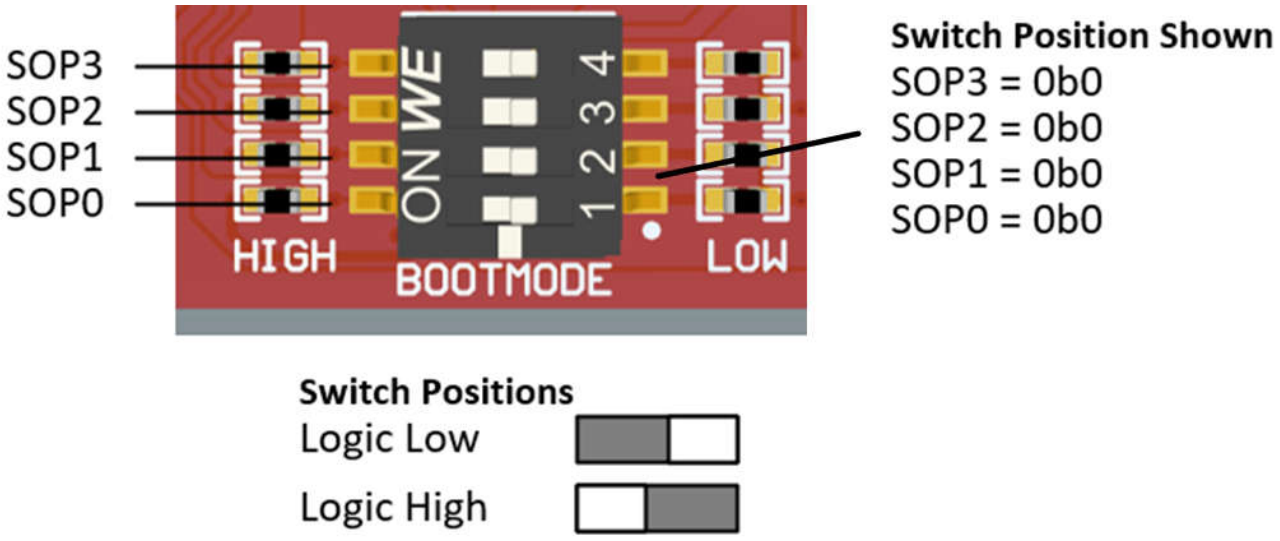

Figure 3-6. Boot mode DIP Switch Positions - LP AM263Px E2 SW1 SOP Switches

Table 3-5. Boot mode Selection

Boot mode	SPI0_D0_pad (SOP3 - SW1.4)	SPI0_CLK_pad (SOP2 - SW1.3)	QSPI_D1 (SOP1 - SW1.2)	QSPI_D0 (SOP0 - SW1.1)
OSPI (4S) - Quad Read Mode	1	1	1	1
UART	1	1	1	0
OSPI (1S) - Single Read Mode	1	1	0	1
OSPI (8S) - Octal Read Mode	1	1	0	0
DevBoot	0	1	0	0
xSPI 8D (SFDP)	0	0	1	1
Unsupported boot mode	All other combinations not defined above			

Table 3-6. Supported Boot modes

Boot mode/Peripheral	Boot Media/Host	Notes
OSPI (4S) - Quad Read Mode	OSPI Flash	Download and boot SBL from OSPI flash in quad read mode. Attempt Primary SBL, followed by Secondary SBL if primary loading fails.
UART	External Host	Download and boot SBL from UART interface via XMODEM protocol at 115200bps BaudRate.
OSPI (1S) - Single Read Mode	OSPI Flash	Download and boot SBL from OSPI flash in single read mode. Attempt Primary SBL, followed by Secondary SBL if primary loading fails.
OSPI (8S) - Octal Read Mode	OSPI Flash	Download and boot SBL from OSPI flash in octal read mode. Attempt Primary SBL, followed by Secondary SBL if primary loading fails.
xSPI 8D (SFDP)	OSPI Flash	Read SFDP table for read command, download and boot SBL from OSPI flash in 8D mode. Attempt Primary SBL, followed by Secondary SBL if primary loading fails.
DevBoot	N/A	No SBL. Used for development purposes only.

3.1.4 IO Expander

AM263Px LaunchPad has an TCA6416ARTWR IO Expander, that provides general-purpose remote I/O expansion and bidirectional voltage translation for processors through I2C communication, an interface consisting of serial clock (SCL), and serial data (SDA) signals.

The TCA6416A's digital core consists of eight 8-bit data registers: two Configuration registers (input or output selection), two Input Port registers, two Output Port registers, and two Polarity Inversion registers. At power on or after a reset, the I/Os are configured as inputs. However, the system controller can configure the I/Os as either inputs or outputs by writing to the Configuration registers. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system controller. In AM263P SoC, the communication with IO Expander is done through I2C1 bus. The signals that are coming out of the IO Expander shown in IO Expander. Please refer to TCA6416ARTWR-Datasheet for programming guide of TCA6416ARTWR.

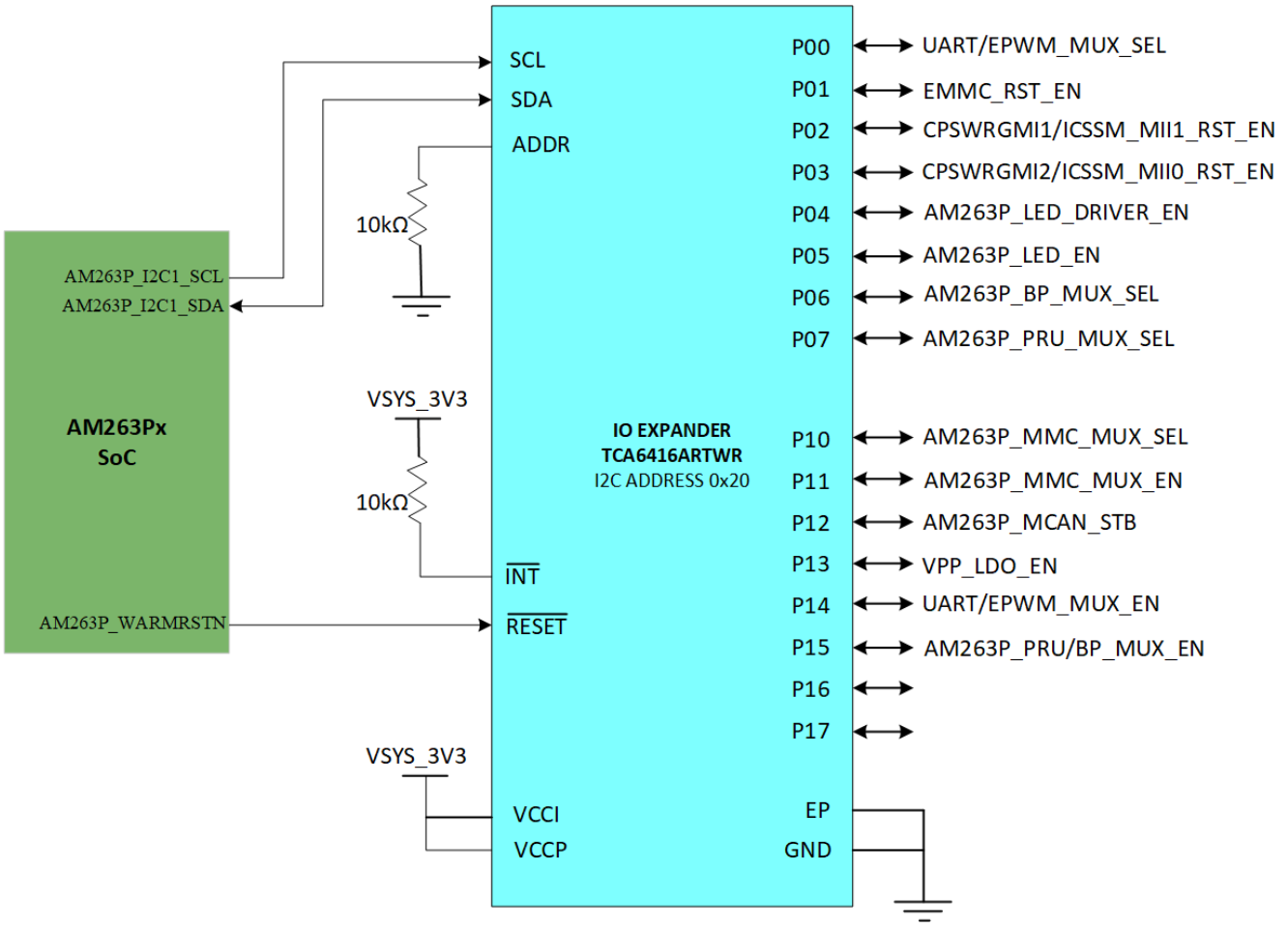

Figure 3-7. IO Expander

3.2 Functional Block Diagram

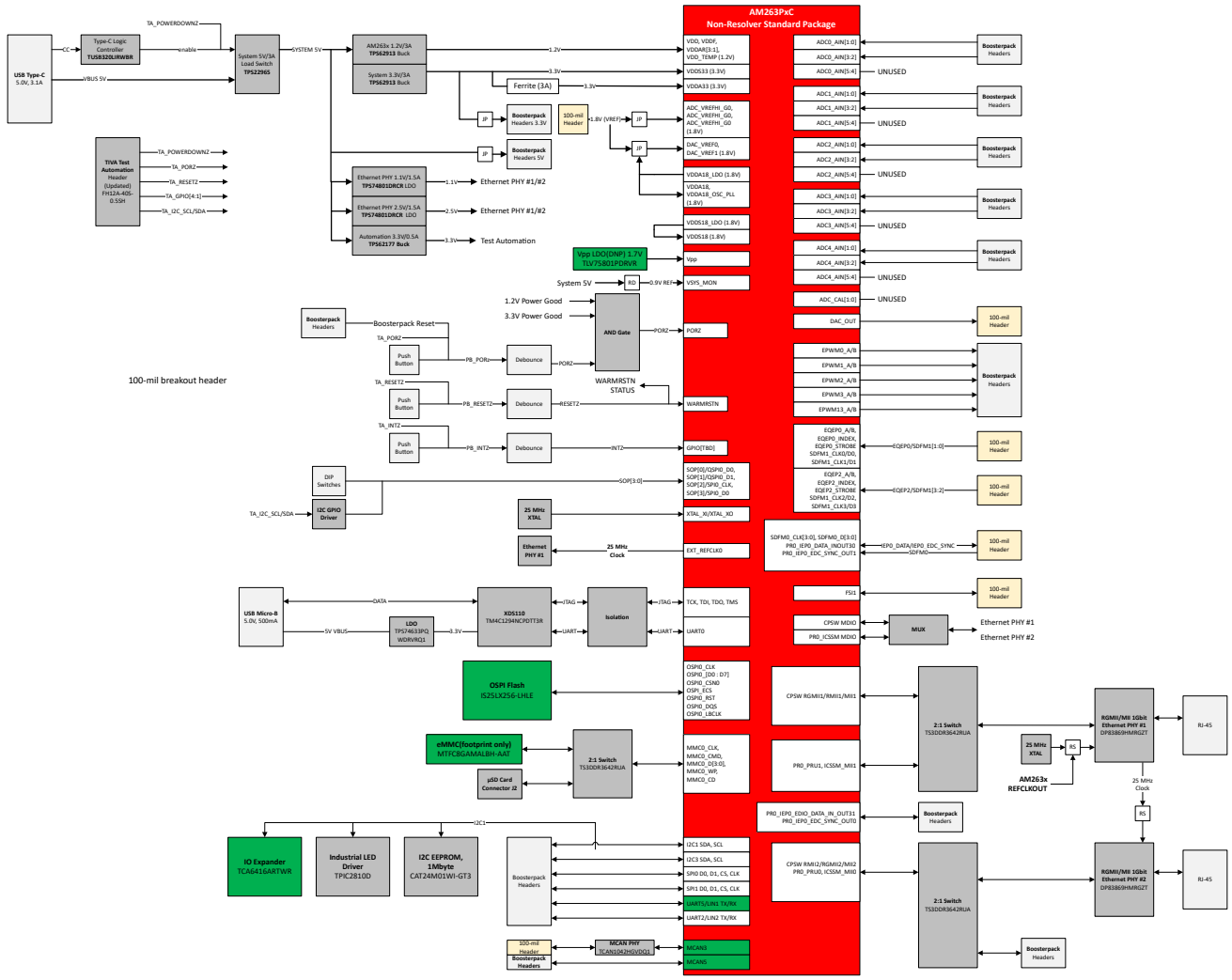

Figure 3-8. AM263Px LaunchPad Functional Block Diagram

3.3 GPIO Mapping

Table 3-7. GPIO Mapping Table

GPIO Description	GPIO	Functionality	Net Name	Active Status
CPSW RGMII1/MII1 MUX select	GPIO105	GPIO	RGMII1_ICSSM_MUX_SEL_GPIO105	LOW
SD Card Load Switch Enable	GPIO122	GPIO	AM263P_SD_ENABLE_GPIO122	LOW
Interrupt To SoC	GPIO123	Interrupt	AM263P_INT1_PB_GPIO123	LOW

3.4 Reset

Figure 3-9 shows the reset architecture of the AM263Px LaunchPad

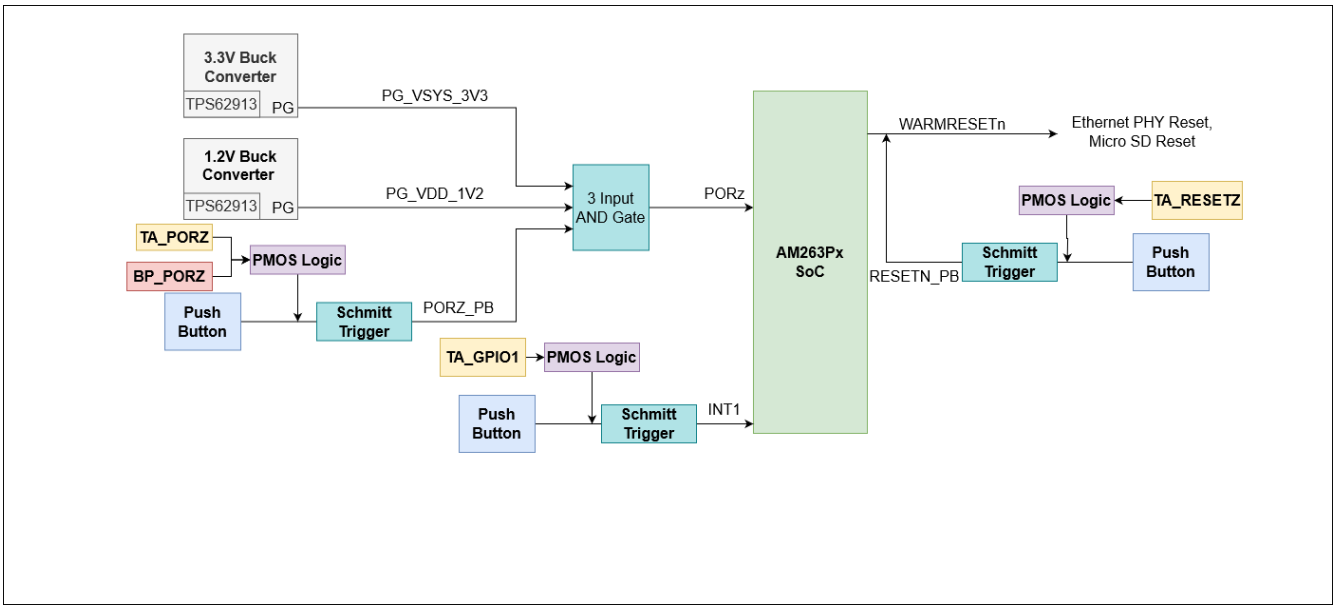

Figure 3-9. Reset Architecture

The AM263Px LaunchPad has the following resets:

- PORz is the Power On Reset
- WARMRESETn is the warm reset

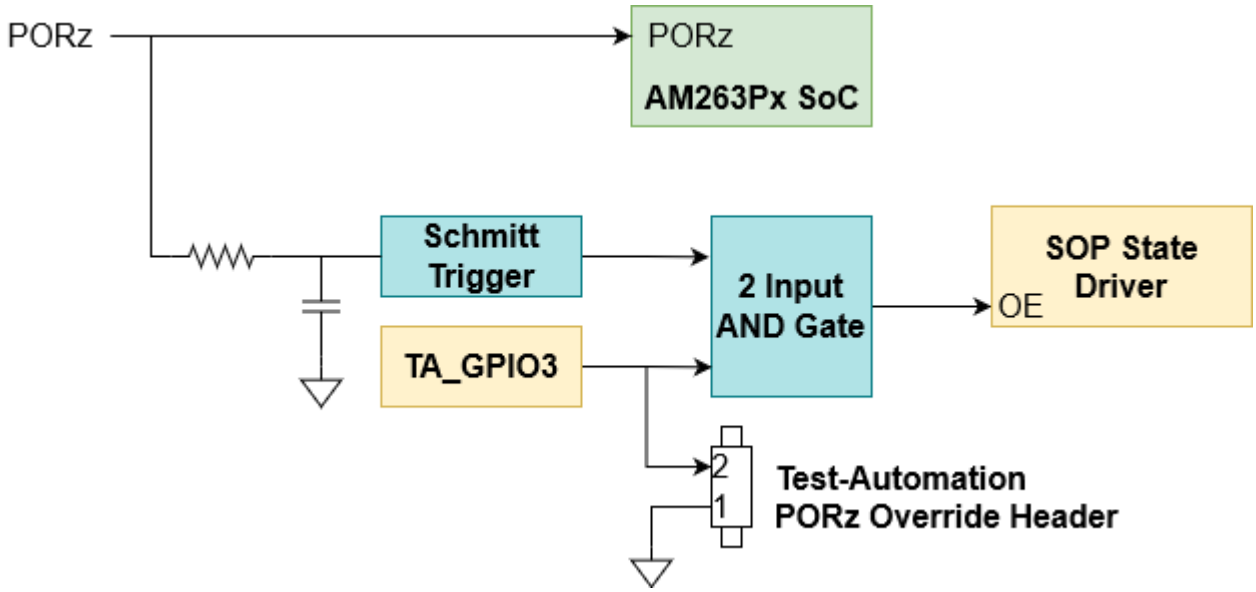

Figure 3-10. PORZ Reset Signal Tree

The PORz signal is driven by a 3-input AND gate that generates a power on reset for the MAIN domain when:

- The 3.3V buck converter (TPS62913) power good output is driven low by having an output voltage that is below the power-good threshold.
- The 1.2V buck converter (TPS62913) power good output is driven low by having an output voltage that is below the power-good threshold.
- The user push button (SW2) is pressed.

- A P-Channel MOSFET gate's signal is logic LOW which causes V_{GS} of the PMOS to be less than zero and so the PORz signal connects to the PMOS drain which is tied directly to ground. The signals that can create the logic LOW input to the PMOS gate are:
  - TA_PORZ output from the Test Automation header
  - BP_PORZ output from either of the BoosterPack sites.

The PORz signal is tied to:

- AM263Px SoC PORz input
- Boot mode State Driver(U4)'s output enable input
  - There is an RC filter to create a 1ms delay from GND to 3.0V such that the SOP State Driver's output enable input is low longer than the required SOP hold time following a PORz de-assertion.

There is a Test-Automation PORz Override header that enables the ability to hold TA_GPIO3 low when a jumper is installed. This enables the boot mode Control from the Test Automation Header.

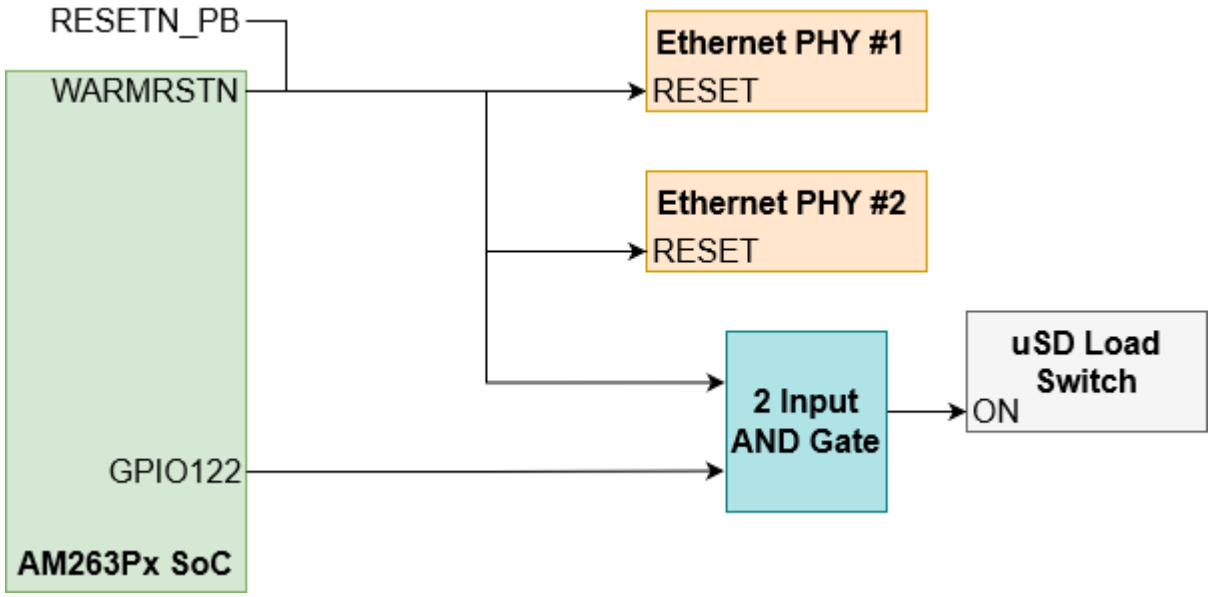

Figure 3-11. WARMRESETn Reset Signal Tree

The WARMRESETn signal creates a warm reset to the MAIN domain when:

- The user push button (SW3) is pressed.
- The Test Automation Header outputs a logic LOW signal (TA_RESETz) to a P-Channel MOSFET gate which causes V_{GS} of the PMOS to be less than zero and so the RESETz signal connects to the PMOS drain which is tied directly to ground.

The WARMRESETn signal is tied to:

- AM263Px SoC WARMRESETN output
- RESETN_PB signal that is created from push button + PMOS logic
- Micro SD Load Switch control input via a 2 input AND Gate with an AM263Px SoC driven GPIO signal (GPIO122)
- Both Ethernet PHY's reset input

The AM263Px LaunchPad also has an external interrupt to the SoC , INT1, that occurs when:

- The user push button (SW4) is pressed.
- The Test Automation Header outputs a logic LOW signal (TA_GPIO1) to a P-Channel MOSFET gate which causes V_{GS} of the PMOS to be less than zero and so the INTn signal connects to the PMOS drain which is tied directly to ground.

3.5 Clock

The AM263Px SoC requires a 25MHz clock input for XTAL_XI. The AM263Px LaunchPad uses a 25MHz crystal for the SoC clock source. The LaunchPad also has two 25MHz Crystals onboard for the Ethernet PHY clocking. The SoC clock signal output CLKOUT0 can be used as a clock source for Ethernet PHY #1 by removing the resistors mounted for XTAL_XI and XTAL_XO from the 25MHz Ethernet PHY #1 Crystal and mounting the appropriate resistor for the CLKOUT0 signal to be routed to the XI pin of the Ethernet PHY.

The Ethernet PHY #1 clock signal output ETH1_CLKOUT can be used as a clock source for Ethernet PHY #2 by removing the resistors mounted for XTAL_XI and XTAL_XO from the 25MHz Ethernet PHY #2 Crystal and mounting the appropriate resistor for the ETH1_CLKOUT signal to be routed to the XI pin of Ethernet PHY #2.

The LaunchPad also requires a 16MHz clock source for the XDS110 for UART-USB JTAG support.

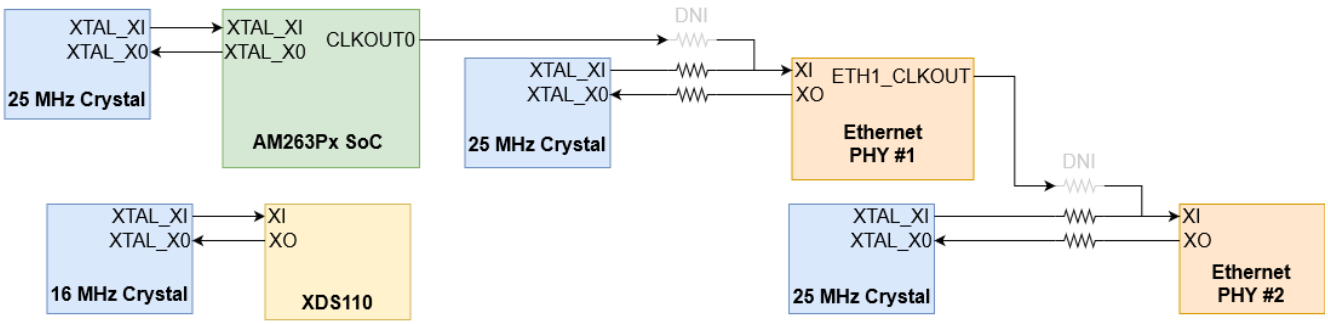

Figure 3-12. AM263Px LaunchPad Clock Tree

3.6 Memory Interfaces

3.6.1 OSPI

The AM263Px LaunchPad has a 256 Mb OSPI Flash memory device (IS25LX256-LHLE), which is connected to the OSPI0 interface of the AM263Px SoC. The OSPI supports single data rates and double data rates with memory speeds up to 133MHz. The OSPI flash is powered by the 3.3V system supply.

The OSPI0_D0/D1 signals are also used for boot mode control logic. There are 10KΩ resistors used to isolate the boot mode control logic after the value is latched.

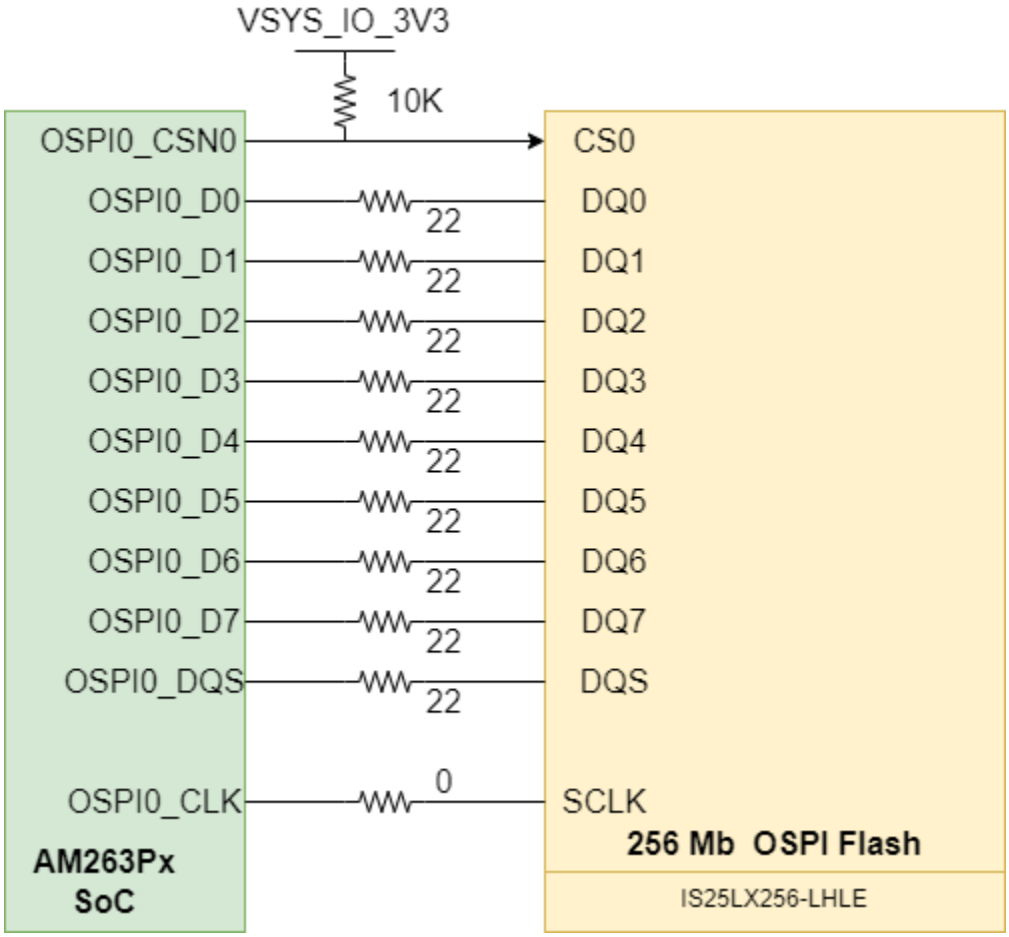

Figure 3-13. OSPI Flash Interface

Note

AM263P_OSPI0_DQS(UART1_RXD) and AM263P_OSPI0_LBCLK(UART1_TXD) net names are wrongly swapped in the schematics. As per datasheet OSPI0_DQS must be connected to M3 ball pin and OSPI0_LBCLKO must be connected to L3 Ball pin.

Refer to OSPI DQS and LBCLK nets swap for more details.

3.6.2 MMC

The AM263Px LaunchPad provides a micro SD card interface that is mapped to the MMC0 instance of the AM263Px SoC.

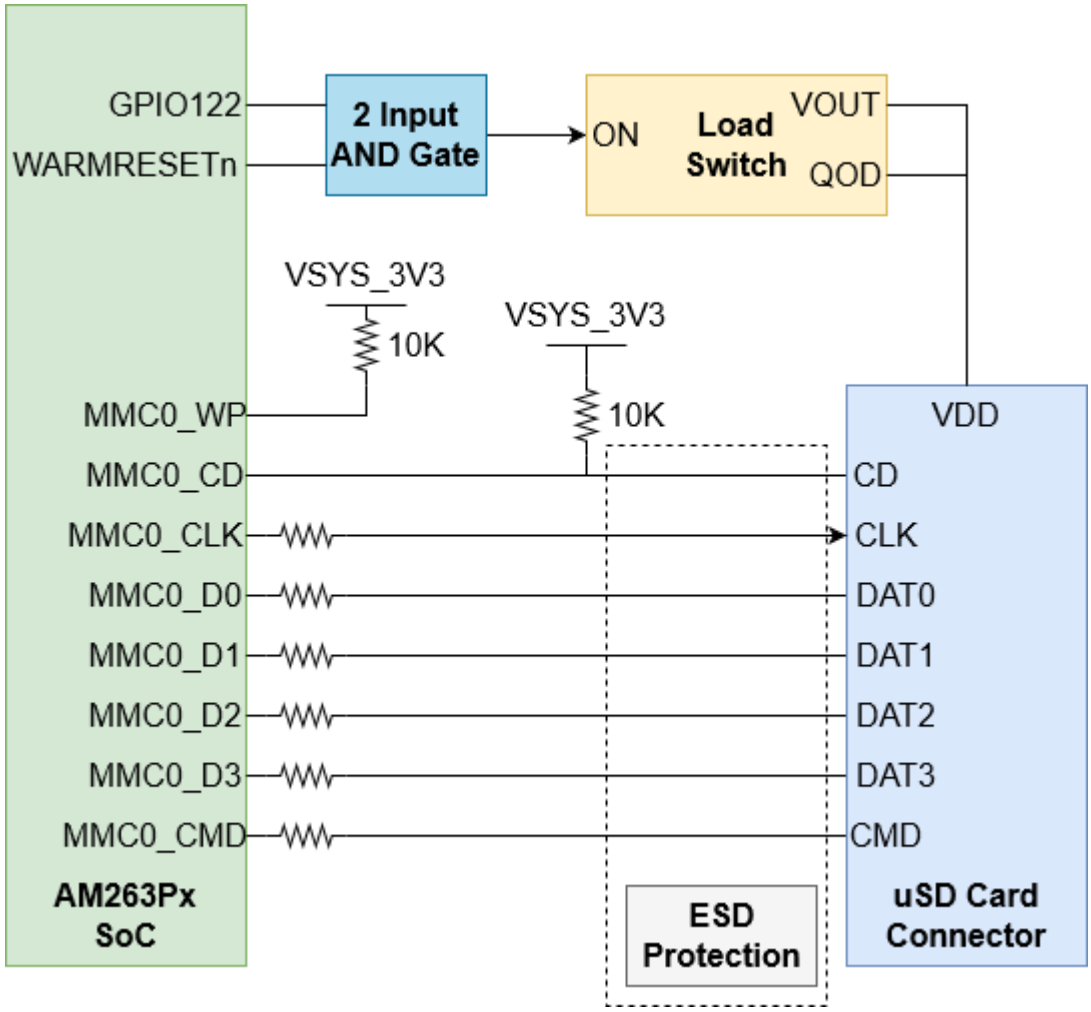

Figure 3-14. Micro SD Card Connector

A load switch (TPS22918TDBVTQ1) is used to power the micro SD card connector. The load switch is driven by the output of a 2-input AND gate between WARMRESETn and the SD Card enable GPIO (GPIO122) to power cycle the card upon reset. The load switch uses quick output discharge (QOD) to make sure that the supply voltage reaches <10% of nominal value during reset.

Inline ESD protection is provided for the MMC signals in the form of a six channel transient voltage suppressor device (TPD6E001RSER) and two channel transient voltage suppressor device (TPD2E001DRLR).

The Write Protect (WP) and Card Detect (CD) signals of the SD card connector are pulled up to the 3.3V System voltage supply.

A series termination resistor is provided for all MMC signals besides CD.

3.6.3 eMMC

The AM263Px LaunchPad has a eMMC footprint that is mapped to the MMC0 instance of the AM263Px SoC, muxed through U53 MUX. The current eMMC footprint is considering the eMMC part MTFC8GAMALBH-AAT. Users can mount the same part, or pin compatible ones for evaluating the eMMC interface.

Note

The current eMMC footprint on the LP-AM263P board has a mismatch of the AM263P_EMMC0_CLK_MUX and AM263P_EMMC0_CMD_MUX nets, where in they are swapped with each other wrongly. This needs to be fixed through a hardware modification of the board, before evaluating eMMC. Please refer to eMMC CMD and CLK nets swap for more details.

3.6.4 Board ID EEPROM

The AM263Px LaunchPad has a I2C based 1Mbit EEPROM (CAT24M01WI-GT3) to store board configuration details. The Board ID EEPROM is connected to the I2C1 interface of the AM263Px SoC. The default I2C address of the EEPROM is set to 0x52 by pulling up the address pin A1 and pulling down the address pin A2 to ground. The Write Protect pin for the EEPROM is by default pulled down to ground and therefore Write Protect is disabled.

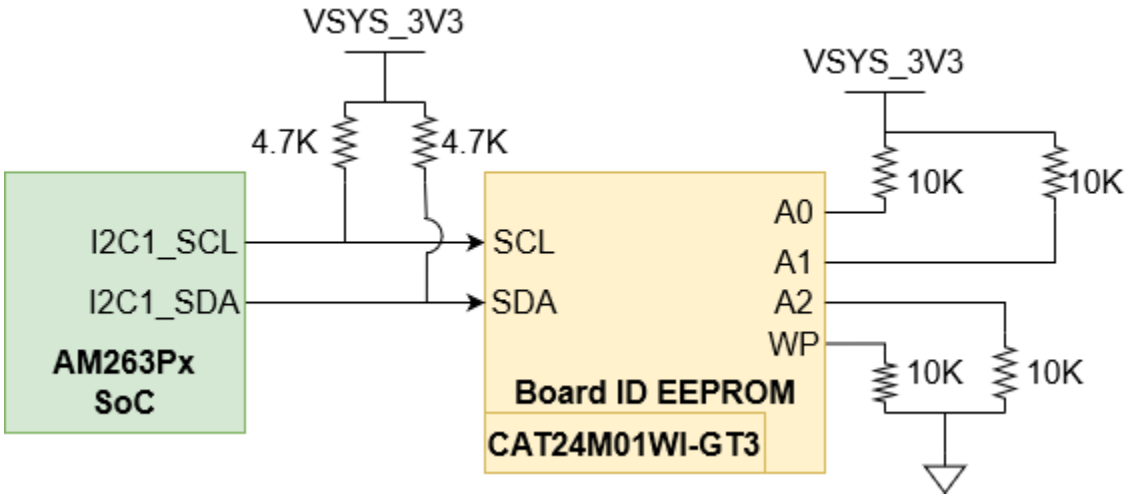

Figure 3-15. Board ID EEPROM

3.7 Ethernet Interface

3.7.1 Ethernet PHY #1 - CPSW RGMII/ICSSM

Note

The PRU internal pinmux mapping provided in the TRM is part of the original hardware definition of the PRU. However, due to the flexibility provided by the IP and associated firmware configurations, this is not necessarily a hard requirement. The first PRU implementation for AM65x had the MII TX pins swapped during initial SOC integration and this convention as maintained for subsequent PRU revisions to enable firmware reuse. To make use of the SDK firmware, use the SYSCONFIG generated PRU pin mapping.

The AM263Px LaunchPad utilizes a 48-pin Ethernet PHY (DP83869HMRGZT) connected to either CPSW RGMII or one on-die Programmable Real-time Unit and Industrial Communication Sub System (PRU-ICSS). There is a 2:1 mux that selects between the RGMII or PRU-ICSS signals. The PHY is configured to advertise 1-Gb operation. The Ethernet data signals of the PHY are terminated to an RJ45 connector. The RJ45 connector is used on the board for Ethernet 10/100/1000Mbps connectivity with integrated magnetics and LEDs for link and activity indication.

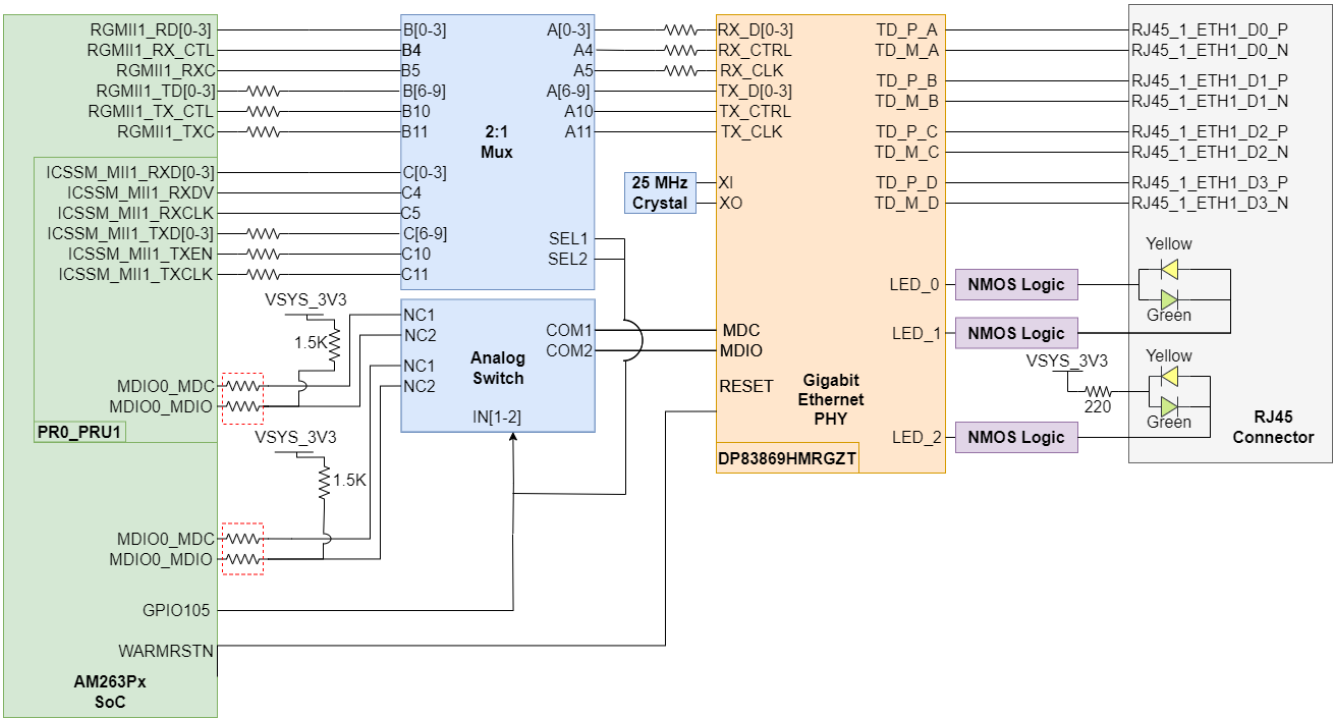

Figure 3-16. Ethernet PHY #1

The Ethernet PHY requires three separate power sources. VDDIO is the 3.3V, system generated supply. There are dedicated LDO's for the 1.1V and 2.5V supplies for the Ethernet PHY.

There are series termination resistors on the transmit clock and data signals located near the SoC. There are series termination resistors on the receive clock and data signals near the Ethernet PHY.

The MDIO signal from the SoC to the PHY require 1.5kΩ pullup resistors to the 3.3V system supply voltage for proper operation. There is an analog switch (TS5A23159DGSR) that selects between the CPSW MDIO/MDC and the ICSSM MDIO/MDC signals to be routed to the Ethernet PHY.

Both the 2:1 mux and analog switch are controlled by a GPIO signal that selects between CPSW RGMII and ICSSM signals.

Table 3-8. Ethernet PHY #1 CPSW/ICSSM Select

GPIO105	Condition	Function of Mux
LOW	RGMII CPSW Selected	Port A ↔ Port B
HIGH	ICSSM Selected	Port A ↔ Port C

The reset input for the Ethernet PHY is controlled by the WARMRESET AM263Px SoC output signal.

The Ethernet PHY uses many functional pins as strap option to place the device into specific modes of operation.

Table 3-9. Ethernet PHY #1 Strapping Resistors

Functional Pin	Default Mode	Mode in LaunchPad	Function
RX_D0	0	3	PHY address: 0011
RX_D1	0	0	
JTAG_TDO/GPIO_1	0	0	RGMII to Copper
RX_D3	0	0	
RX_D2	0	0	
LED_0	0	0	Auto-negotiation, 1000/100/10 advertised, auto MDI-X
RX_ER	0	0	
LED_2	0	0	
RX_DV	0	0	Port Mirroring Disabled

Note

Each strap pin has an internal pull down resistance of 2.49kΩ

Note

RX_D0 and RX_D1 are on a 4-level strap resistor mode scheme. All other signals are 2-level strap resistor modes.

3.7.2 Ethernet PHY #2 - CPSW RGMII/ICSSM

Note

The PRU internal pinmux mapping provided in the TRM is part of the original hardware definition of the PRU. However, due to the flexibility provided by the IP and associated firmware configurations, this is not necessarily a hard requirement. The first PRU implementation for AM65x had the MII TX pins swapped during initial SOC integration and this convention was maintained for subsequent PRU revisions to enable firmware reuse. To make use of the SDK firmware, use the SYSCONFIG generated PRU pin mapping.

The AM263Px LaunchPad utilizes a 48-pin Ethernet PHY (DP83869HMRGZT) connected to either CPSW RGMII or one on-die Programmable Real-time Unit and Industrial Communication Sub System (PRU-ICSS). The RGMII CPSW port and ICSSM are internally pinmuxed on the AM263Px SoC. For more information on the internal muxing of signals refer to Pinmux Mapping. The PHY is configured to advertise 1-Gb operation. The Ethernet data signals of the PHY are terminated to an RJ45 connector. The RJ45 connector is used on the board for Ethernet 10/100/1000Mbps connectivity with integrated magnetics and LEDs for link and activity indication.

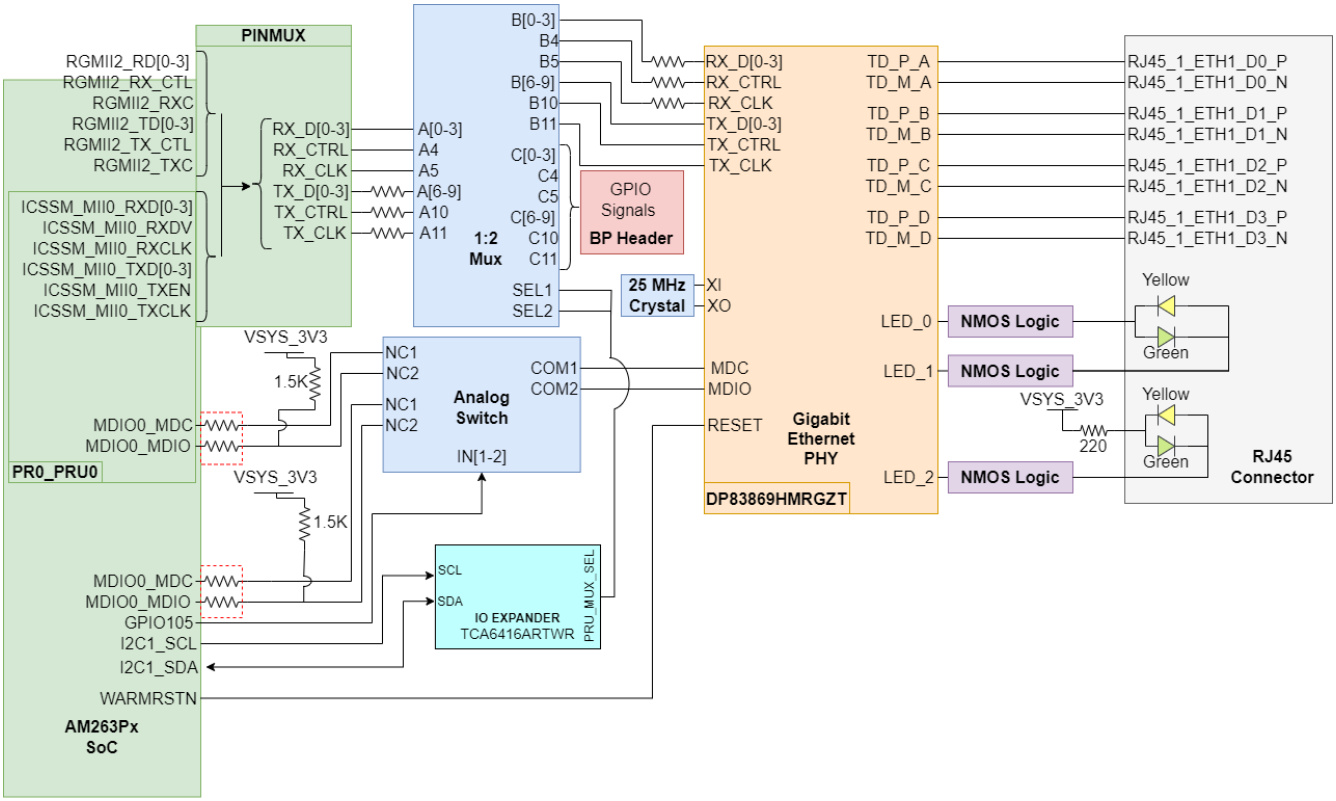

Figure 3-17. Ethernet PHY #2

The Ethernet PHY requires three separate power sources. VDDIO is the 3.3V, system generated supply. There are dedicated LDO's for the 1.1V and 2.5V supplies for the Ethernet PHY.

There are series termination resistors on the transmit clock and data signals located near the SoC. There are series termination resistors on the receive clock and data signals near the Ethernet PHY.

The MDIO signal from the SoC to the PHY require 1.5kΩ pullup resistors to the 3.3V system supply voltage for proper operation. There is an analog switch (TS5A23159DGSR) that selects between the CPSW MDIO/MDC and the ICSSM MDIO/MDC signals to be routed to the Ethernet PHY.

AM263Px internal Pinmux is used to select between CPSW RGMII and ICSSM signals. The signals are then routed to a 1:2 mux (TS3DDR3812RUAR) that selects between mapping the signals to the Ethernet PHY or the BP headers in the case that the PRU GPIO signals are being used in a BoosterPack application. There is an AM263Px SoC GPIO select signal that drives the 1:2 mux.

Table 3-10. Ethernet PHY #2 CPSW/ICSSM Select

PRU_MUX_SEL	Condition	Function of Mux
LOW	Ethernet PHY Selected	Port A ↔ Port B
HIGH	BoosterPack header Selected	Port A ↔ Port C

The reset input for the Ethernet PHY is controlled by the WARMRESET AM263Px SoC output signal.

The Ethernet PHY uses many functional pins as strap option to place the device into specific modes of operation.

Table 3-11. Ethernet PHY #2 Strapping Resistors

Functional Pin	Default Mode	Mode in LP	Function
RX_D0	0	0	PHY address: 1100
RX_D1	0	3	
JTAG_TDO/GPIO_1	0	0	RGMII to Copper
RX_D3	0	0	
RX_D2	0	0	
LED_0	0	0	Auto-negotiation, 1000/100/10 advertised, auto MDI-X
RX_ER	0	0	
LED_2	0	0	
RX_DV	0	0	Port Mirroring Disabled

Note

Each strap pin has an internal pull down resistance of 2.49kΩ

Note

RX_D0 and RX_D1 are on a 4-level strap resistor mode scheme. All other signals are 2-level strap resistor modes.

3.7.3 LED Indication in RJ45 Connector

The AM263Px LaunchPad has two RJ45 network ports for the CPSW RGMII and ICSSM signals of the AM263Px SoC. Each RJ45 connector contains two bi-color LEDs that are used to indicate link and activity.

RJ45 Connector LED indication for the Ethernet PHY #1:

Table 3-12. Ethernet PHY #1 RJ45 Connector LED indication

LED	Color	Indication
Right LED	Green	Ethernet PHY power established
	Yellow	Transmit or Receive activity
Left LED	Green	Link OK
	Yellow	1000BT link is up

RJ45 Connector LED indication for the Ethernet PHY #2:

Table 3-13. Ethernet PHY #2 RJ45 Connector LED indication

LED	Color	Indication
Right LED	Green	Ethernet PHY power established
	Yellow	Transmit or Receive activity
Left LED	Green	Link OK
	Yellow	1000BT link is up

3.8 I2C

The AM263Px LaunchPad uses two AM263Px SoC inter-integrated circuit (I2C) ports to operate as a controller for various targets. I2C data and clock lines needs to be pulled up to the 3.3V system voltage supply to enable communication.

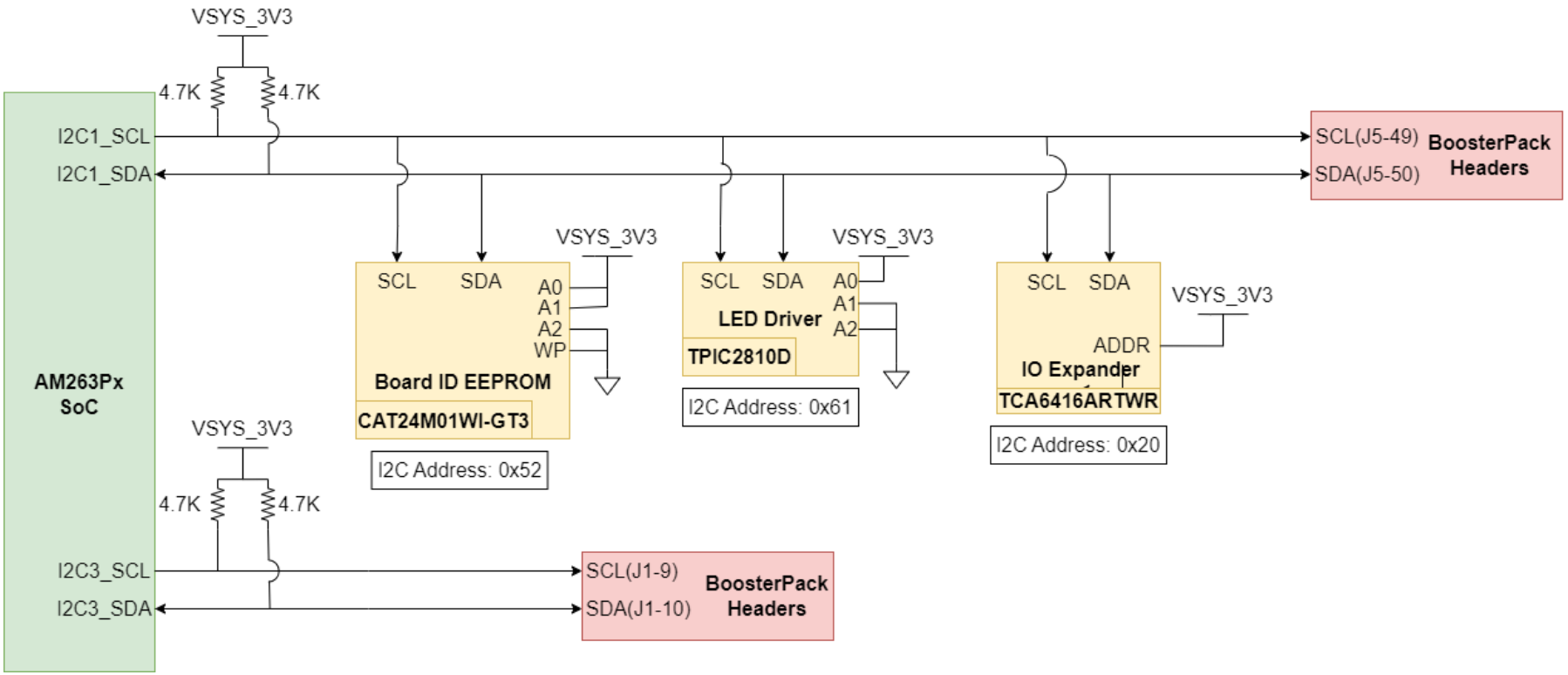

Figure 3-18. I2C Targets

Table 3-14. I2C Addressing

Target	I2C Instance	I2C Addres Bit Description	Device Addressing	LaunchPad Config.	I2C Address
Board ID EEPROM	I2C1	The first 4 bits of the device address are set to 1010, the next two are set by the A2 and A1 pins, the seventh bit, a16, is the most significant internal address bit	0b10110[A2][A1][a16] A1 is connected to 3.3V supply A2 is connected to ground	0b1010010	0x52
LED Driver	I2C1	The first four bits of the target address are 1100, the following three are determined by A2, A1, and A0	0b1100[A2][A1][A0] A2/A1 are connected to ground A0 is connected to 3.3V supply	0b1100001	0x61
BoosterPack Headers	I2C1, I2C3	Dependent on target			

Table 3-14. I2C Addressing (continued)

Target	I2C Instance	I2C Addres Bit Description	Device Addressing	LaunchPad Config.	I2C Address
Boot mode IO Expander	I2C1	The first 6 bits of the target address are set to 010000, the next bit is determined by the addr pin of the IO expander	IO_ADDR pin connected to 3.3V supply	0b0100001	0x21
IO Expander	I2C1	The first 6 bits of the target address are set to 010000, the next bit is determined by the addr pin of the IO expander	IO_ADDR pin connected to 3.3V supply	0b0100001	0x20

Note

Underlined address bits are fixed based on the device addressing and cannot be configured.

3.9 Industrial Application LEDs

The AM263Px LaunchPad has an LED Driver (TPIC2810D) that is used for Industrial Communication LEDs. The driver is connected to eight green LEDs, and the driver has an I2C address of 0x61.

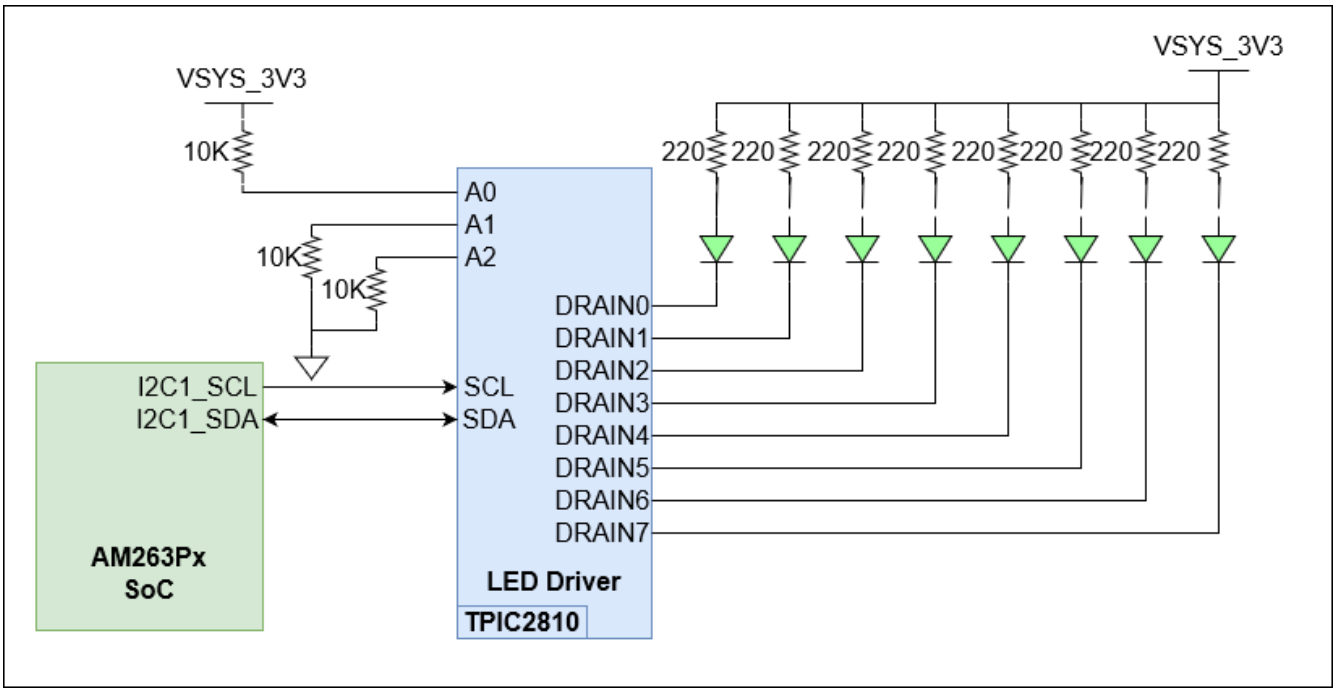

Figure 3-19. Industrial Application I2C LED Array

3.10 SPI

The AM263Px LaunchPad maps two SPI instances (SPI0, SPI1) from the AM263Px SoC to the BoosterPack Headers. Series termination resistors are placed near the SoC for each SPI clock and SPI D0 signal. There is a 2:1 mux (SN74CB3Q3257PWR) that is responsible for selecting SPI signals for proper function. The mux is driven by two GPIO signals that are generated from the AM263Px SoC.

Table 3-15. SPI Mux

Output Enable (OE)	Select (S)	Input/Output	Function
Low	Low	A ↔ B1	A port = B1 port
Low	High	A ↔ B2	A port = B2 port
High	X	Hi-Z	Disconnect

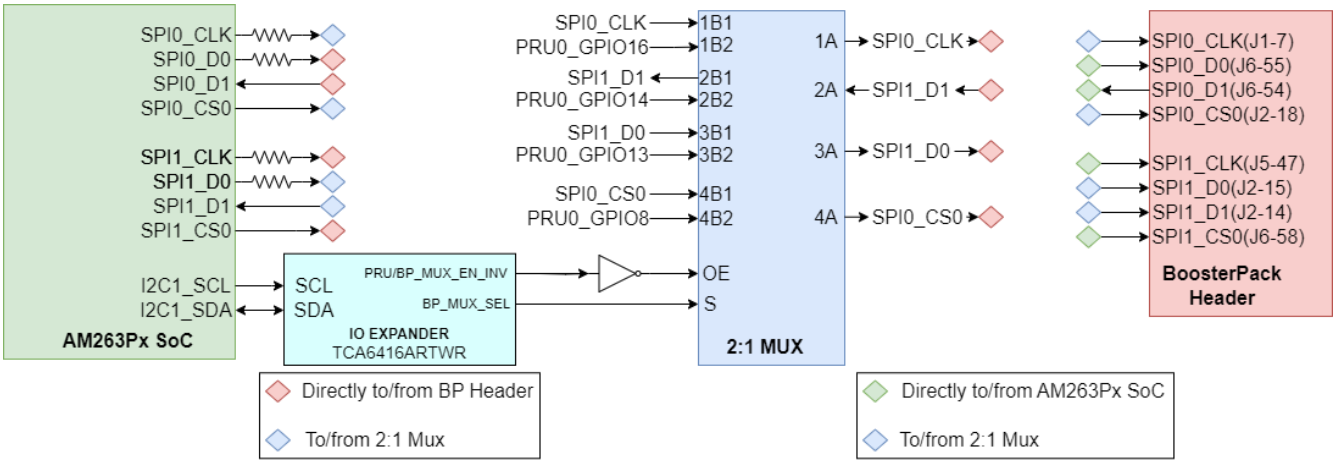

Figure 3-20. SoC SPI to BoosterPack

3.11 UART

The AM263Px LaunchPad uses the XDS110 as a USB2.0 to UART bridge for terminal access. UART0 transmit and receive signals of the AM263Px SoC are mapped to the XDS110 with a dual channel isolation buffer (ISO7721DR) for translating from the 3.3V IO voltage supply to the 3.3V XDS supply. The XDS110 is connected to a micro-B USB connector for the USB 2.0 signals. ESD protection is provided to the USB 2.0 signals by a transient voltage suppression device (TPD4E02B04DQAR). The micro-B USB connector's VBUS 5V power is mapped to a low dropout regulator (TPS79601DRBR) to generate the 3.3V XDS110 supply. A separate 3.3V supply for the XDS110 allows for the emulator to maintain a connection when power to the LaunchPad is removed.

Separate UART instances (UART2 & UART5) are mapped directly to the BoosterPack header.

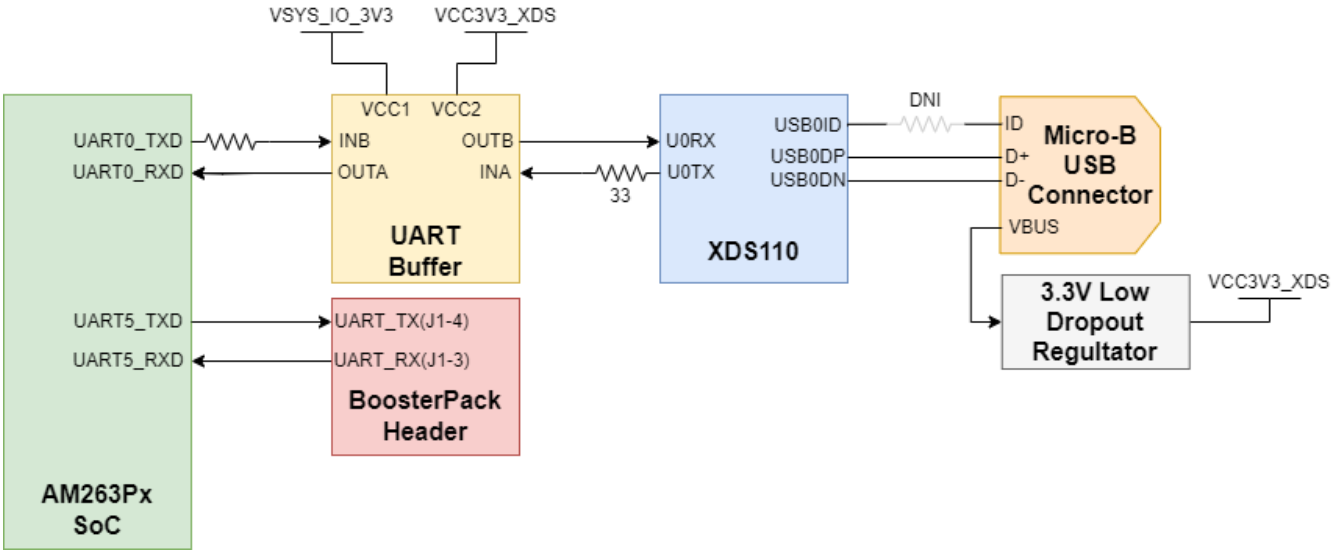

Figure 3-21. UART

3.12 MCAN

The LaunchPad is equipped with a single MCAN Transceiver (TCAN1044VDRBTQ1) that is connected to the MCAN3 interface of the AM263Px SoC. The MCAN Transceiver has two power inputs, VIO is the transceiver 3.3V system level shifting supply voltage and VCC is the transceiver 5V supply voltage. The SoC CAN data transmit data input is mapped to TXD of the transceiver and the CAN receive data output of the transceiver is mapped to the MCAN RX signal of the SoC.

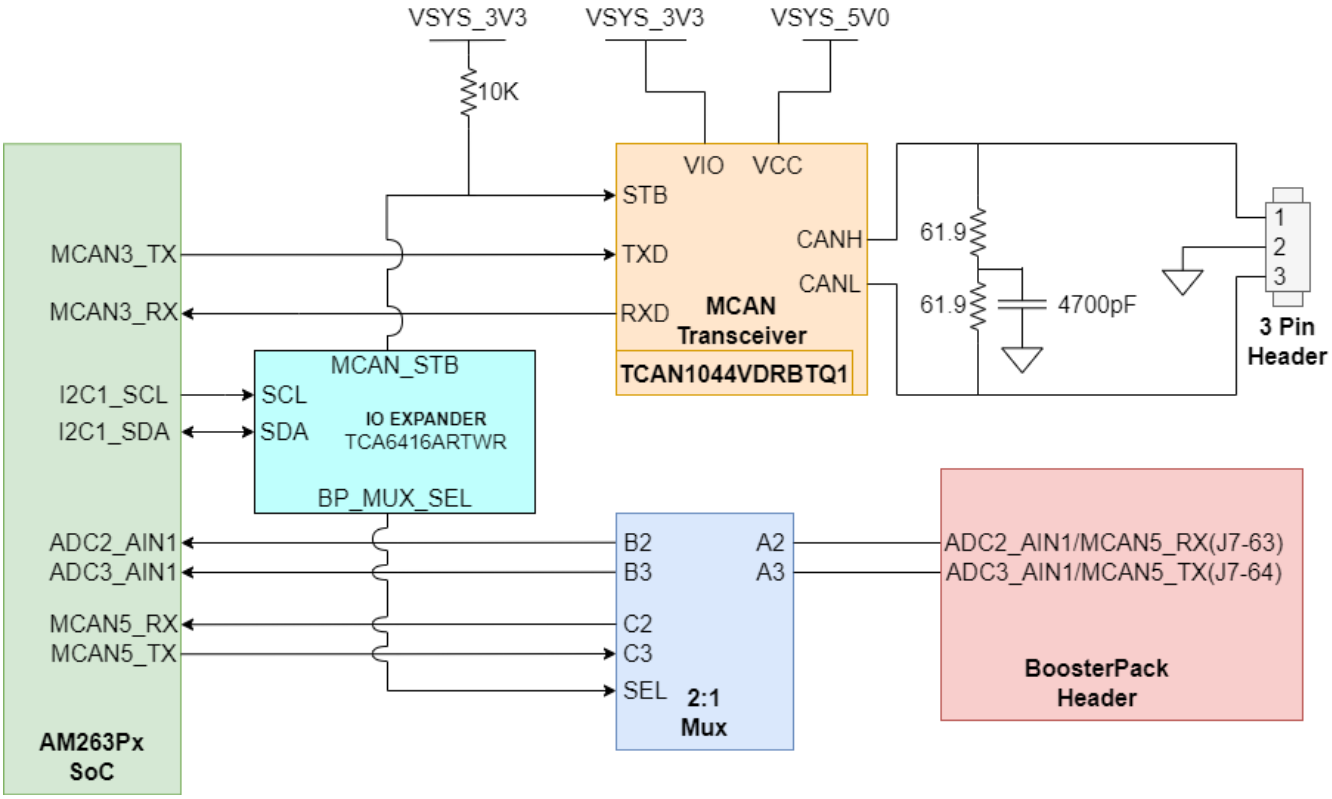

Figure 3-22. MCAN Transceiver and BoosterPack Header

The system has a 120Ω split termination on the CANH and CANL signals to improve EMI performance. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

The low and high level CAN bus input output lines are terminated to a three pin header.

The standby control signal is an AM263Px SoC GPIO signal. The STB control input has a pullup resistor that is used to have the transceiver be in low-power standby mode to prevent excessive system power. Below is a table that shows the operating modes of the MCAN transceiver based on the STB control input logic.

Table 3-16. MCAN Transceiver Operating Modes

STB	Device Mode	Driver	Receiver	RXD Pin
High	Low current standby mode with bus wake-up	Disabled	Low-power receiver and bus monitor enable	High (recessive) until valid WUP is received
Low	Normal Mode	Enabled	Enabled	Mirrors bus state

MCAN5 is routed to the BoosterPack Header via a 2:1 mux. The mux selects whether ADC inputs or MCAN signals are mapped to the BoosterPack Header.

Table 3-17. MCAN BoosterPack Mux

BP_MUX_SEL	Condition	Function of Mux
LOW	ADC Inputs Selected	Port A ↔ Port B
HIGH	MCAN TX/RX Selected	Port A ↔ Port C

3.13 FSI

The AM263Px LaunchPad supports a fast serial interface by terminating the SoC signals to a 10-pin header. The interface has two lines of data and a clock line for both the receive and transmit signals. The 10-pin header is connected to the 3.3V System voltage supply.

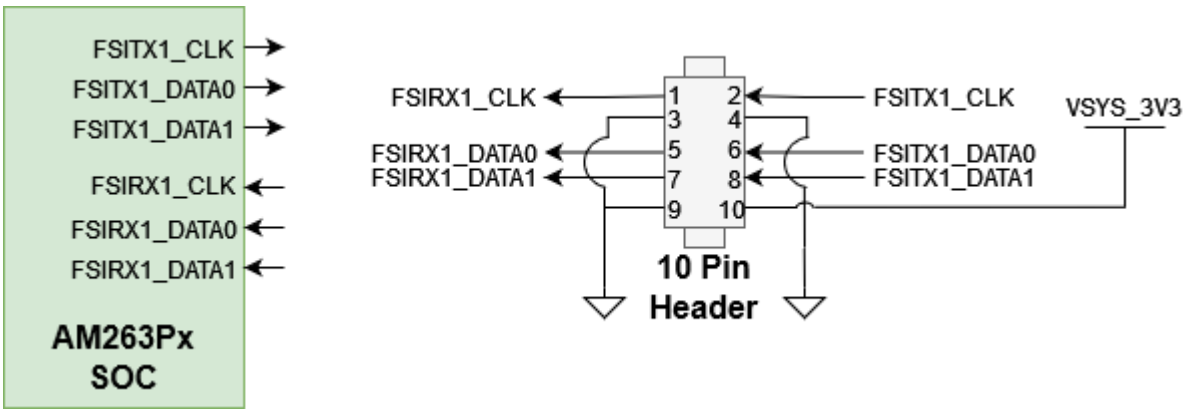

Figure 3-23. FSI 10-Pin Header

3.14 JTAG

The AM263Px LaunchPad includes an XDS110 class onboard emulator. The LaunchPad includes all circuitry needed for XDS110 emulation. The emulator uses a USB 2.0 micro-b connector to interface the USB 2.0 signals that are created from the UART-USB bridge. The VBUS power from the connector is used to power the emulator circuit so that the connection to the emulator is not lost when power to the LaunchPad is removed. For more information on the XDS110 and the UART-USB bridge refer to UART

The XDS110 controls two power status LEDs. For more information on the Power Status LEDs refer to Power Status LEDs

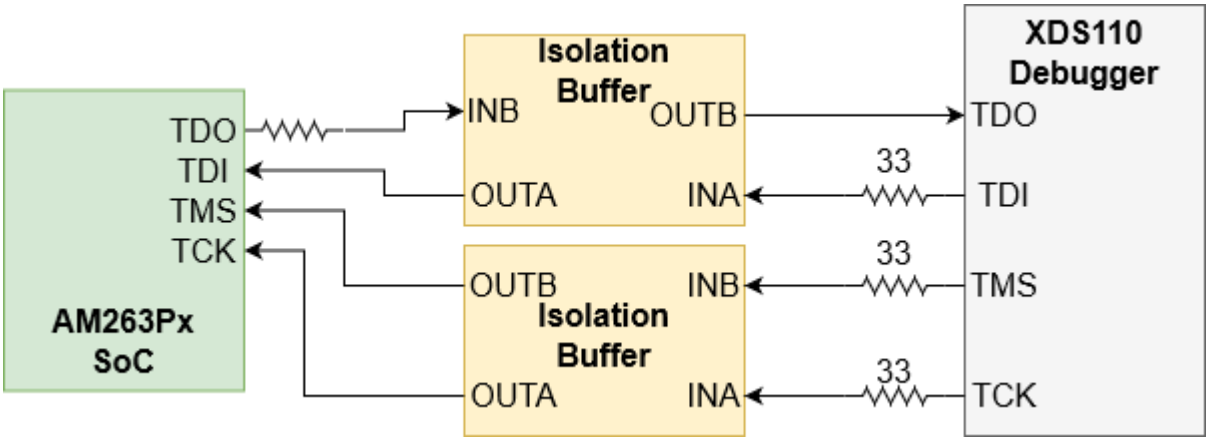

Figure 3-24. JTAG Interface to XDS110

3.15 TIVA and Test Automation Header

The board supports two test automation features:

- A USB-based virtual COM port, using the TIVA Test Automation Header.
  - The header allows an external controller to manipulate basic operations such as power down, PORz, warm reset, and boot mode control.
  - The AM263Px SOC I2C instance is connected to the TIVA Test Automation Header - FH12A-402-0.55H.
- A 40 pin test automation header that allows an external controller to manipulate basic operations such as power down, PORz, warm reset, and boot mode control.

– The Test Automation Circuit is powered by a dedicated 3.3V power supply (VSYS_TA_3V3) which is generated by a 5V to 3.3V buck regulator (TPS62177DQCR).
– The AM263Px SoC I2C3 instance is connected to both the Test Automation Header and the boot mode IO expander (TCA6408ARGTR).

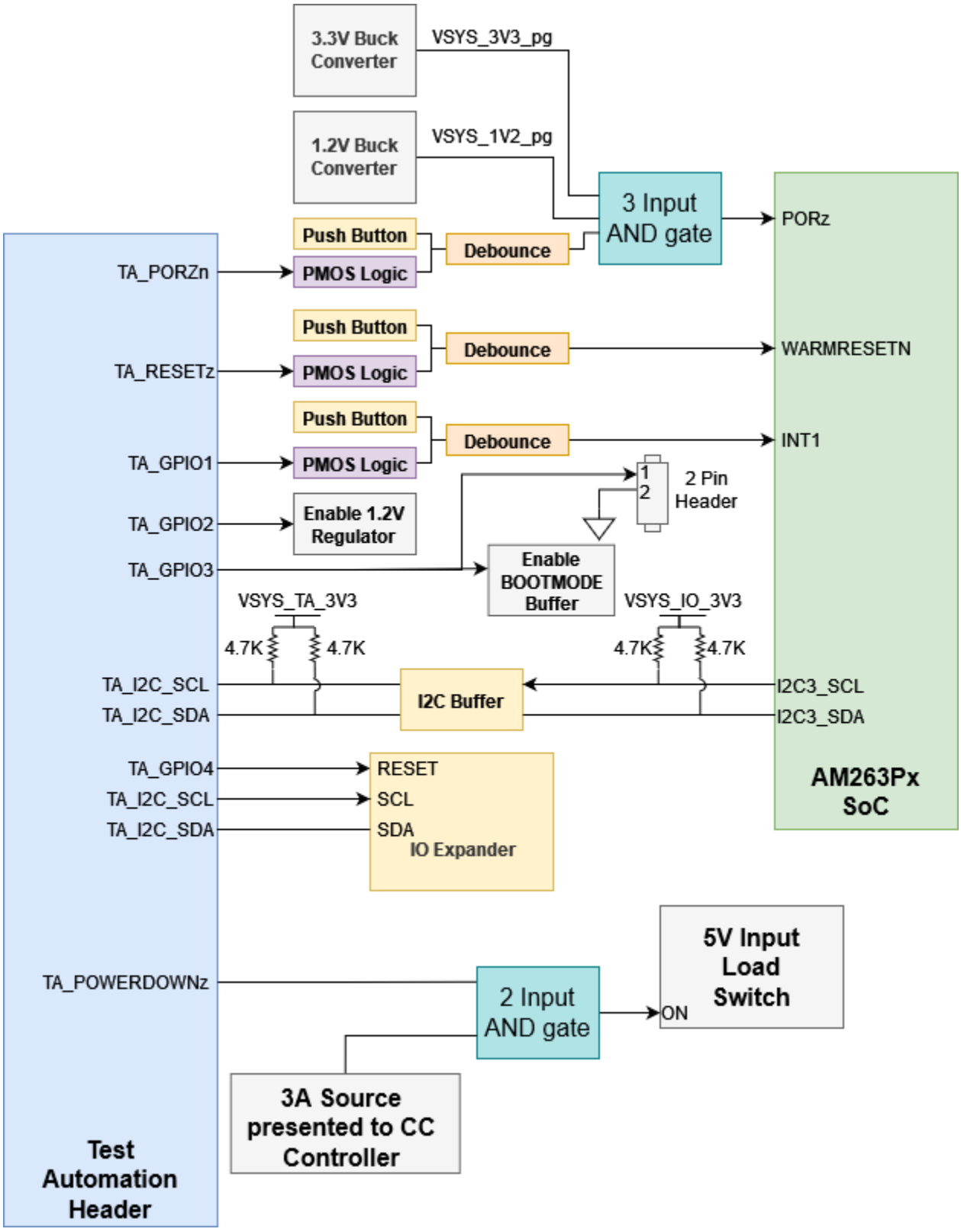

Figure 3-25. Test Automation Header

The following table details the Test Automation mapping.

Table 3-18. Test Automation GPIO and I2C Mapping

Signal Name	Description	Direction
TA_POWERDOWNZ	When logic low, disables the 3.3V buck regulator that is used in the first stage of DC/DC conversion	Output
TA_PORZ	When logic low, connects the PORz signal to ground due to PMOS V_{GS} being less than zero creating a power on reset to the MAIN domain	Output
TA_RESETZ	When logic low, connects the WARM RESETn signal to ground due to PMOS V_{GS} being less than zero creating a warm reset to the MAIN domain	Output
TA_GPIO1	When logic low, connects the INTn signal to ground due to PMOS V_{GS} being less than zero creating an interrupt to SoC	Output
TA_GPIO3	When logic low, disables the boot mode buffer output enable	Output
TA_GPIO4	Reset signal for boot mode IO Expander	Output
TA_I2C_SCL	I2C Clock signal used to communicate with bootmode IO expander to change the boot modes.	Output
TA_I2C_SDA	I2C Data signal used to communicate with bootmode IO expander to change the boot modes.	Output

3.16 LIN

The AM263Px LaunchPad supports Local Interconnect Network communication with two LIN instances mapped to the BoosterPack header.

Note

The AM263Px does **not** have an onboard LIN Transceiver

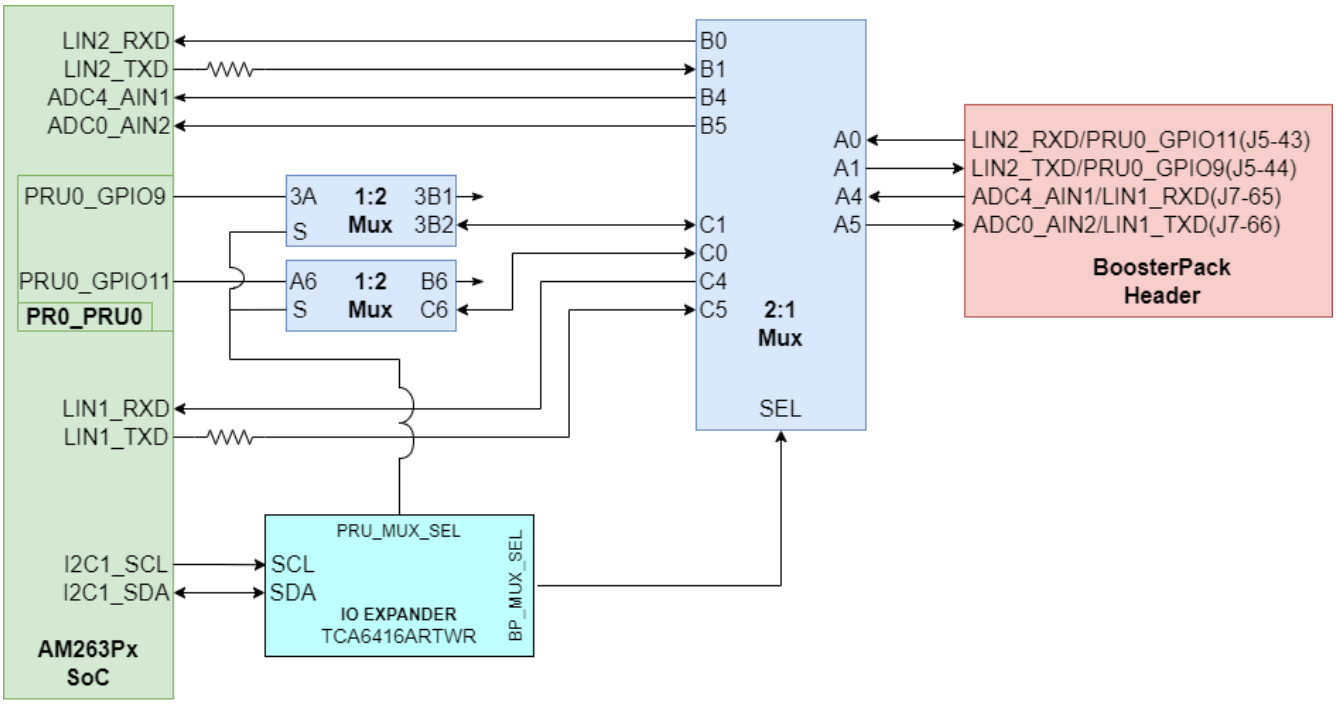

Figure 3-26. LIN Instances to BoosterPack Header

Both LIN instances are mapped to the alternate BoosterPack function 2:1 mux. The alternate BoosterPack function mux also has mappings for ADC inputs and PRU0 GPIO signals.

Table 3-19. LIN 2:1 Mux

PRU_MUX_SEL	BP_MUX_SEL	Function of 2:1 Mux	Signals to BP Header
HIGH	LOW	Port A ↔ Port B	LIN2TX/RX, ADC4_AIN1, ADC0_AIN2
HIGH	HIGH	Port A ↔ Port C	PRU GPIO11/9, LIN1TX/RX
LOW	LOW	Port A ↔ Port B	LIN2TX/RX, ADC4_AIN1, ADC0_AIN2
LOW	HIGH	Port A ↔ Port C	NC, NC, LIN1 TX/RX

3.17 ADC and DAC

The AM263Px LaunchPad maps 20 ADC inputs to the BoosterPack header. All of the ADC inputs that are used in the LaunchPad are ESD protected.

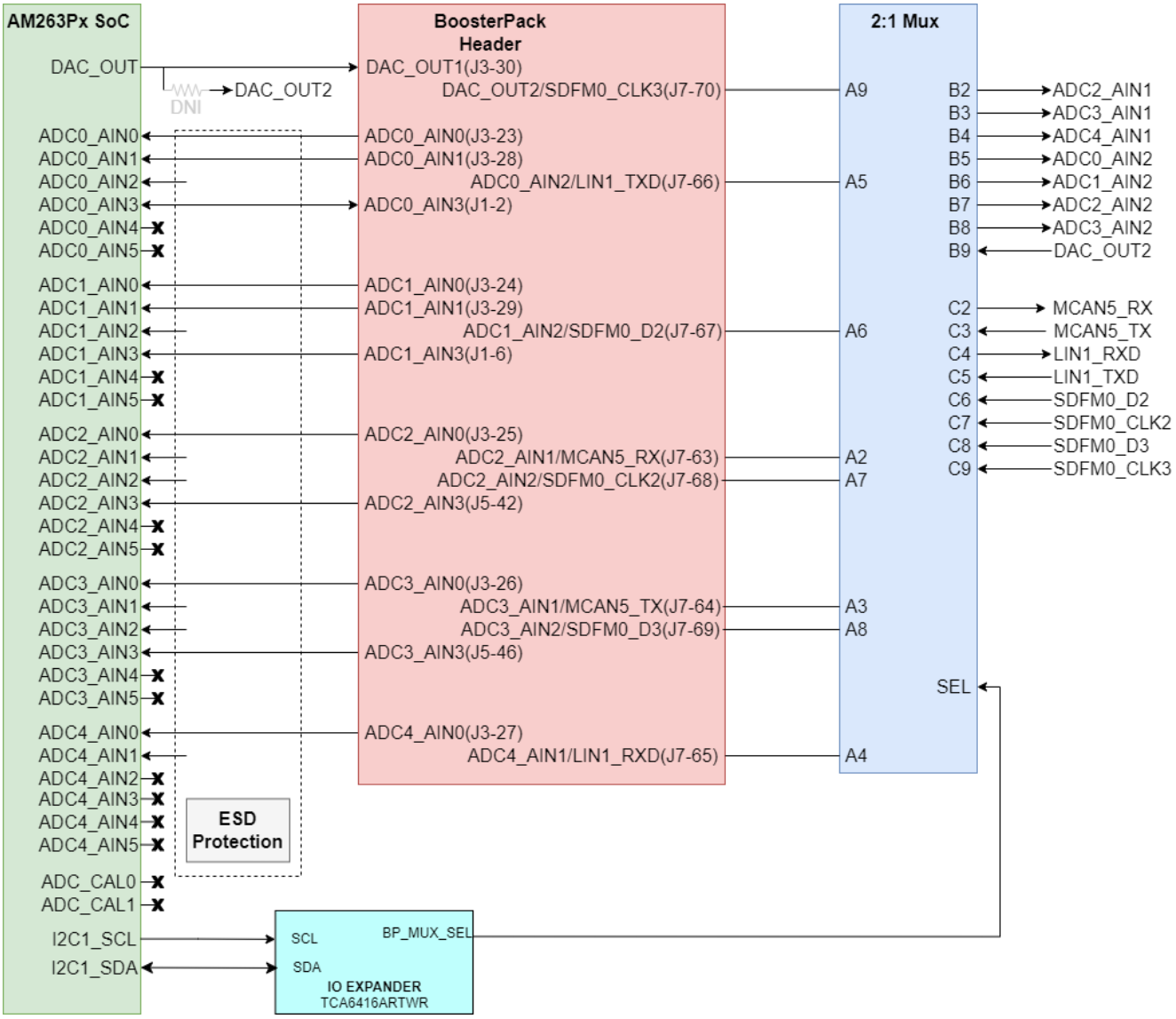

Figure 3-27. ADC/DAC Signal Pathing

Seven of the ADC inputs and one instance of the DAC_OUT signal is routed to a 2:1 mux (TS3DDR3812RUAR) to offer alternate BoosterPack functionality. The select line of the mux is driven by an AM263Px SoC GPIO signal.

Table 3-20. ADC BoosterPack Mux

BP_MUX_SEL	Condition	Funciton of Mux
LOW	ADC input/DAC_OUT Selected	Port A ↔ Port B
HIGH	Alternate BP functionality Selected	Port A ↔ Port C

The ADC and DAC require a voltage reference. The AM263Px LaunchPad has two switches that allow the user to switch between the DAC and ADC VREF source.

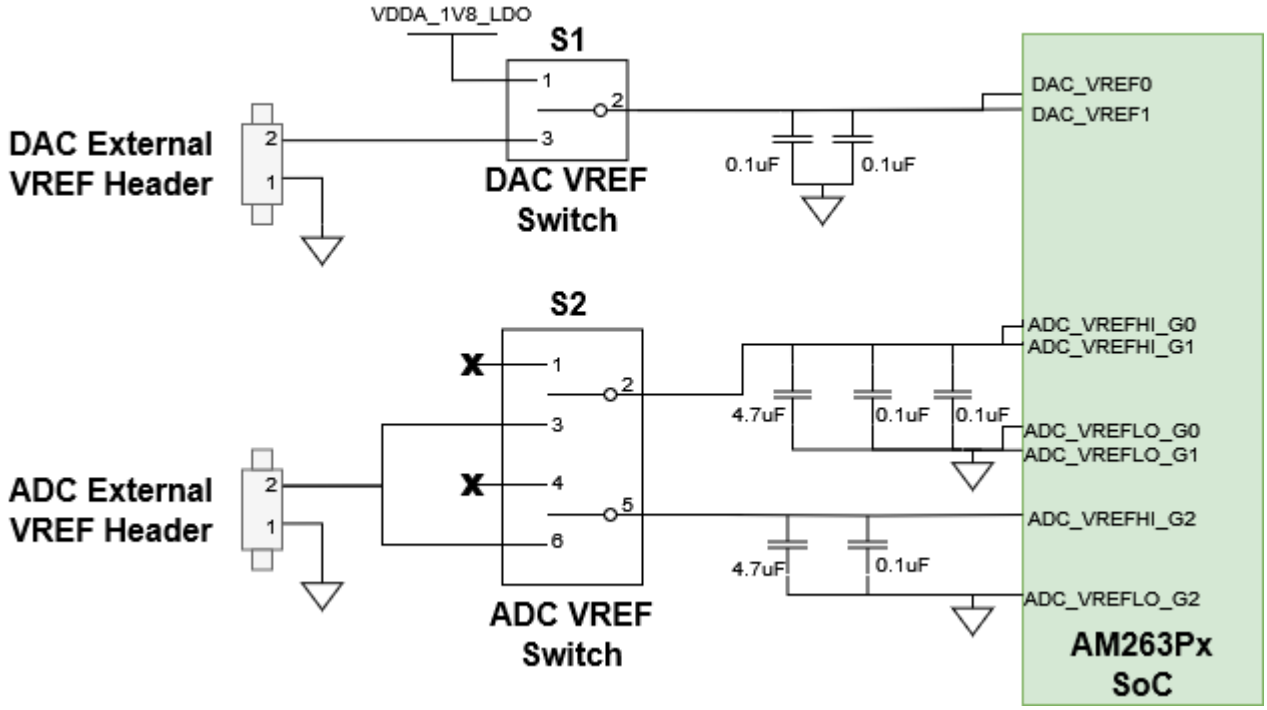

Figure 3-28. ADC and DAC VREF Switches

The DAC VREF Switch (S1) is a single pole double throw switch that controls the input of the ADC VREF inputs of the AM263Px SoC.

Table 3-21. DAC VREF Switch

DAC VREF Switch Position	Reference Selection
Pin 1-2	AM263Px on-die LDO
Pin 2-3	External DAC VREF Header

The ADC VREF Switch (S2) contains two single pole double throw switches that controls the input of the ADC VREF inputs of the AM263Px SoC.

Table 3-22. ADC VREF Switch

ADC VREF Switch Position	Reference Selection
Pin 1-2	OPEN - Allow for reference to be AM263Px on-die LDO reference
Pin 2-3	External ADC VREF Header
Pin 4-5	OPEN - Allow for reference to be AM263Px on-die LDO reference
Pin 5-6	External ADC VREF Header

3.18 EQEP and SDFM

The AM263Px LaunchPad internally muxes the eQEP and SDFM signals. The eQEP0 and SDFM1 instances of the AM263Px are terminated to two headers (J24, J15). The eQEP2 and SDFM2 instances of the AM263Px are terminated to two headers (J25, J16).

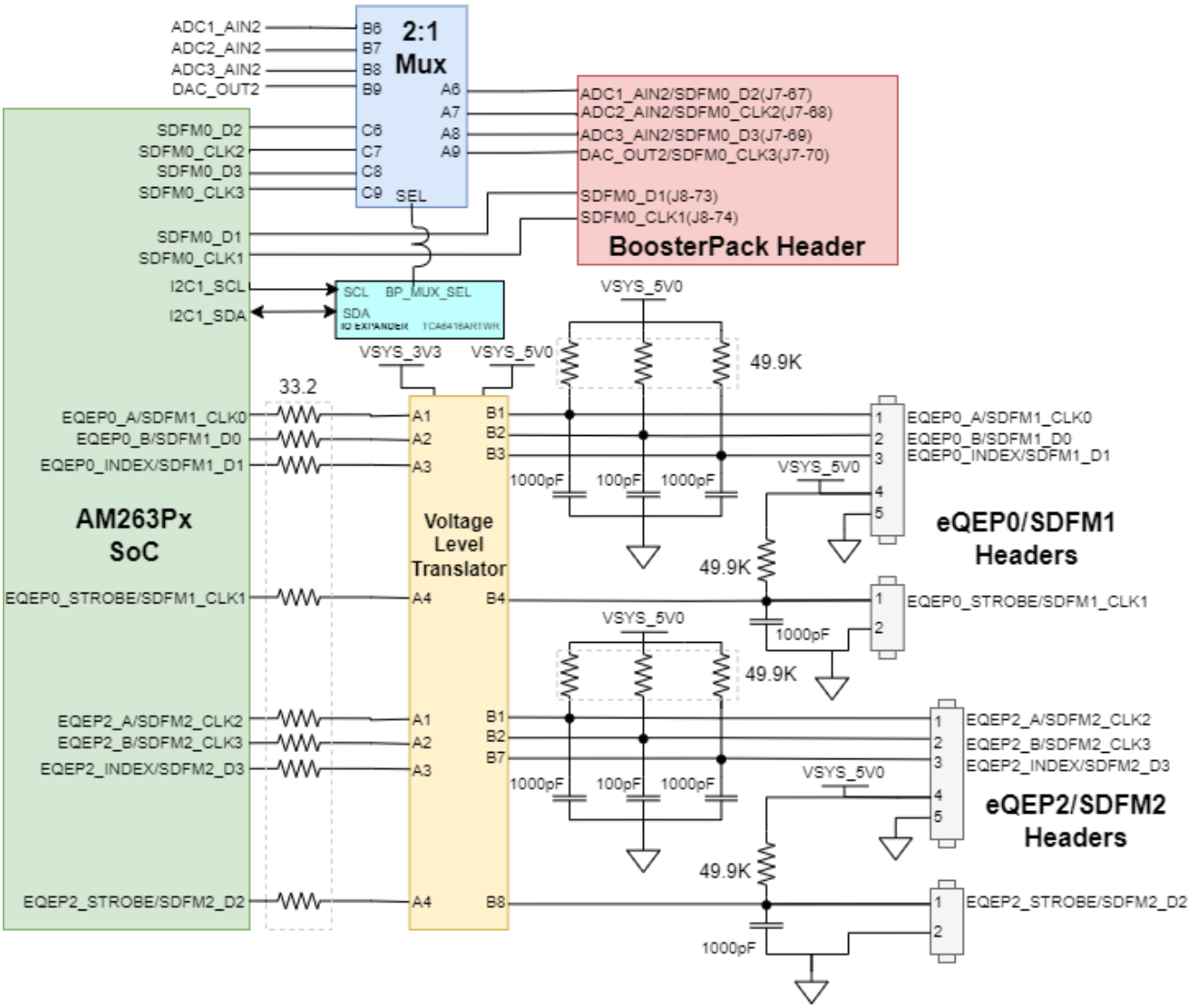

Figure 3-29. EQEP and SDFM Signal Mapping

All eQEP signals have series termination resistors between the AM263Px SoC and the Voltage Level Translator (TXB0108RGYR). The voltage level shifter is responsible for translating the 3.3V to 5V.

SDFM0 is mapped to the BoosterPack Header rather than an independent header. Four of the SDFM0 signals are routed through a 2:1 mux to offer alternate BoosterPack functionality. The select line of the mux is driven by an AM263Px SoC GPIO signal.

Table 3-23. SDFM0 Mux

BP_MUX_SEL	Condition	Function of Mux
LOW	Alternate BP functionality Selected	Port A ↔ Port B
HIGH	SDFM0 Selected	Port A ↔ Port C

3.19 EPWM

The AM263Px LaunchPad maps 20 PWM channels (10 PWM_A/B pairs) to the BoosterPack Header. Each EPWM signal has a series termination resistor. For the mapping of each EPWM signal refer to Pinmux Mapping.

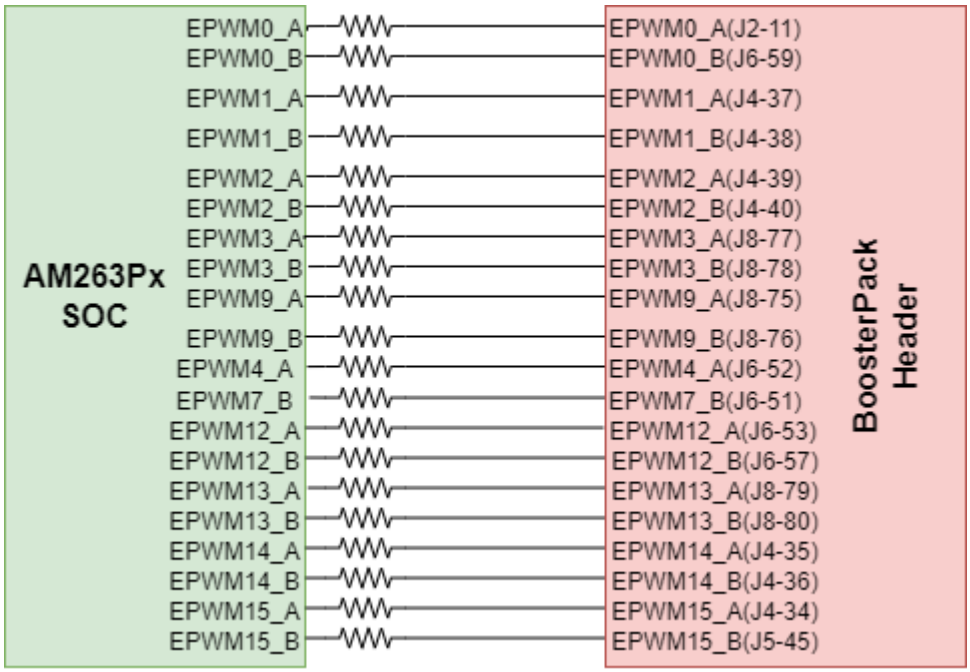

Figure 3-30. EPWM Signal Mapping to BoosterPack Header

3.20 BoosterPack Headers

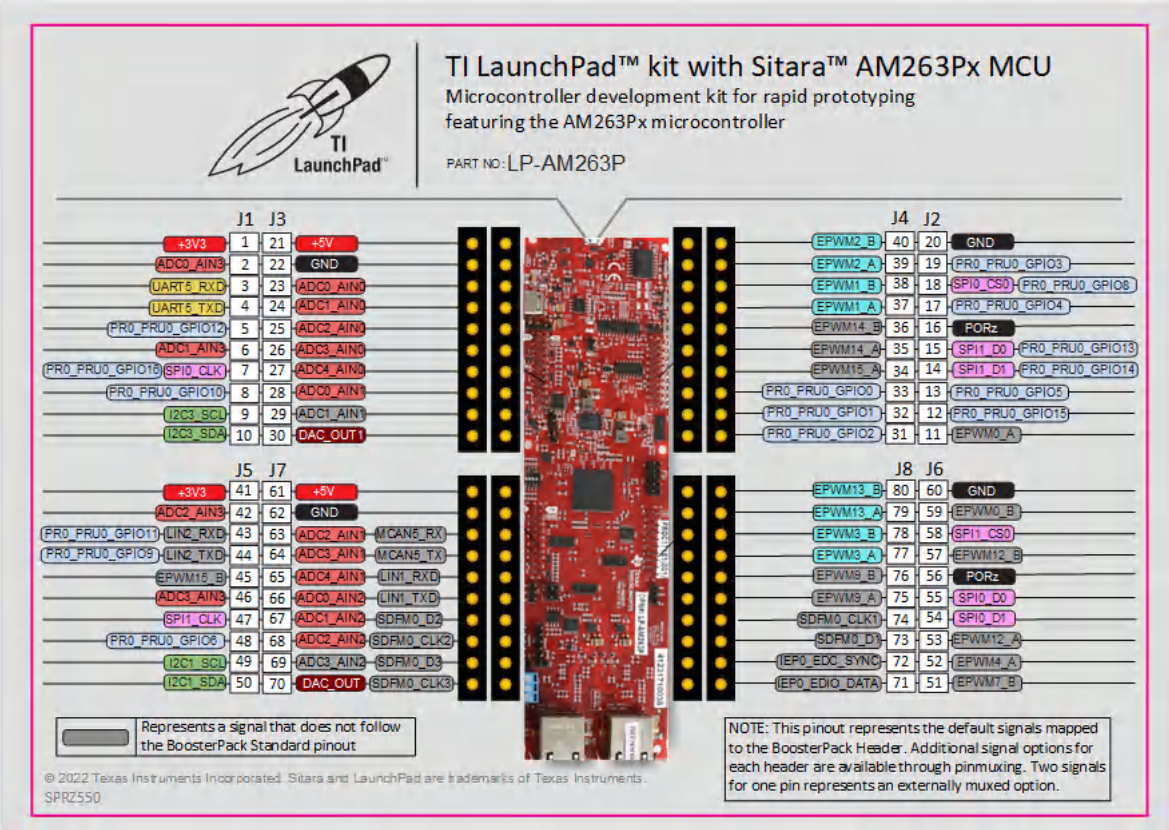

Figure 3-31. AM263Px LaunchPad BoosterPack Pinout

Note

This pinout represents the default signals mapped to the BoosterPack Header. Additional signal options for each header are available through Pinmux Mapping. Two signals for one pin represents an externally muxed option

The AM263Px LaunchPad supports two fully independent BoosterPack XL connectors. BoosterPack site #1 (J1/J3, J2/J4) is located in between the SoC and the micro-B USB Connector. BoosterPack site #2 (J5/J7, J6/J8) is located in between the SoC and the RJ45 connectors. Each GPIO has multiple functions available through the GPIO mux. The signals connected from the SoC to the BoosterPack headers include:

- Various ADC inputs
- DAC outouts
- UART5
- Various GPIO signals
- SPI0 and SPI1
- I2C1 and I2C3
- Various EPWM channels
- LIN1 and LIN2
- MCAN1
- SDFM0

3.21 Pinmux Mapping

The various pinmux options for the BoosterPack connector pins are given below.

Table 3-24. Pinmux Legend

Default signal for BP Header	Muxed alternative signal	External MUX for alternate signal options

Table 3-25. Pinmux Options for J1

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode 10
J1.1	3V3										
J1.2	ADC0_AIN3										
J1.3	EPWM15_B	UART5_RXD	MII1_CRS	MCAN7_TX				GPIO74		CHANNEL5	EPWM15_B
J1.4	EPWM15_A	UART5_TXD	MII1_COL	MCAN7_RX				GPIO73		CHANNEL4	EPWM15_A
J1.5	PR0_PRU0_GPIO12		RMII2_TXD1	RGMII2_TD1	MII2_TXD1	EPWM28_B		GPIO100			EPWM28_B
J1.6	ADC1_AIN3										
J1.7	SPI0_CLK	UART3_TXD	LIN3_TXD				FSITX0_CLK	GPIO12		CHANNEL1	
	PR0_PRU0_GPIO16			RGMII2_TXC	MII2_TXCLK	EPWM27_A		GPIO97			EPWM27_A
J1.8	PR0_PRU0_GPIO10		RMII2_CRS_DV	PR0_UART0_RTSn	MII2_CRS	EPWM23_A		GPIO89			EPWM22_B
J1.9	EPWM8_B	UART4_RXD	I2C3_SCL	SPI6_D1			FSITX2_D0	GPIO60			EPWM9_B
J1.10	EPWM8_A	UART4_TXD	I2C3_SDA	SPI6_D0			FSITX2_CLK	GPIO59			EPWM8_A

Table 3-26. Pinmux Options for J2

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10
J2.11	EPWM0_A							GPIO43			EPWM0_A
J2.12	PR0_PRU0_GPIO15		RMII2_TX_EN	RGMII2_TX_CTL	MII2_TX_EN	EPWM27_B		GPIO98			
J2.13	PR0_PRU0_GPIO5		RMII2_RX_ER		MII2_RX_ER	EPWM22_A		GPIO87			EPWM22_A
J2.14	SPI1_D1	UART5_RXD				XBAROUT4	FSIRX0_D1	GPIO18		CHANNEL7	
	PR0_PRU0_GPIO14			RGMII2_TD3	MII2_TXD3	EPWM29_B		GPIO102			EPWM27_B
J2.15	SPI1_D0	UART5_TXD				XBAROUT3	FSIRX0_D0	GPIO17		CHANNEL8	
	PR0_PRU0_GPIO13			RGMII2_TD2	MII2_TXD2	EPWM29_A		GPIO101			EPWM27_B
J2.16	PORz										
J2.17	PR0_PRU0_GPIO4			RGMII2_RX_CTL	MII2_RXDV	EPWM24_B		GPIO92			EPWM24_B
J2.18	SPI0_CS0	UART3_RXD	LIN3_RXD					GPIO11		CHANNEL0	
	PR0_PRU0_GPIO8					EPWM23_B		GPIO90			EPWM29_A
J2.19	PR0_PRU0_GPIO3			RGMII2_RD3	MII2_RXD3	EPWM26_B		GPIO96			EPWM26_B
J2.20	GND										

Table 3-27. Pinmux Options for J3

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9
J3.21	5V									
J3.22	GND									
J3.23	ADC0_AIN0									
J3.24	ADC1_AIN0									
J3.25	ADC2_AIN0									
J3.26	ADC3_AIN0									
J3.27	ADC4_AIN0									
J3.28	ADC0_AIN1									
J3.29	ADC1_AIN1									
J3.30	DAC_OUT1									

Table 3-28. Pinmux Options for J4

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10
J4.31	PR0_PRU0_GPIO2			RGMII2_RD2	MII2_RXD2	EPWM26_A		GPIO95			EPWM26_A
J4.32	PR0_PRU0_GPIO1		RMII2_RXD1	RGMII2_RD1	MII2_RXD1	EPWM25_B		GPIO94			EPWM25_B
J4.33	PR0_PRU0_GPIO0		RMII2_RXD0	RGMII2_RD0	MII2_RXD0	EPWM25_A		GPIO93			EPWM25_A
J4.34	EPWM15_A	UART5_TXD	MII1_COL	MCAN7_RX				GPIO73		CHANNEL4	EPWM15_A
J4.35	EPWM14_A	UART1_DSRn	SPI7_D1	MCAN6_RX				GPIO71			EPWM14_A
J4.36	EPWM14_B		MII1_RX_ER					GPIO72			EPWM14_B
J4.37	EPWM1_A							GPIO45			EPWM1_A
J4.38	EPWM1_B							GPIO46			EPWM4_B
J4.39	EPWM2_A							GPIO47			EPWM2_A
J4.40	EPWM2_B							GPIO48			EPWM2_B

Table 3-29. Pinmux Options for J5

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10
J5.41	3V3										
J5.42	ADC2_AIN3										
J5.43	LIN2_RXD	UART2_RXD	SPI2_D0					GPIO21			
	PR0_PRU0_GPIO11		RMII2_TXD0	RGMII2_TD0	MII2_TXD0	EPWM28_A		GPIO99			EPWM28_A
J5.44	LIN2_TXD	UART2_TXD	SPI2_D1					GPIO22			
	PR0_PRU0_GPIO9			PR0_UART0_CTSn	MII2_COL	EPWM22_B		GPIO88			
J5.45	EPWM15_B	UART5_RXD	MII1_CRS	MCAN7_TX				GPIO74		CHANNEL5	EPWM15_B
J5.46	ADC3_AIN3										
J5.47	SPI1_CLK	UART4_RXD	LIN4_RXD			XBAROUT2	FSIRX0_CLK	GPIO16		CHANNEL5	
J5.48	PR0_PRU0_GPIO6		RMII2_REF_CLK	RGMII2_RXC	MII2_RXCLK	EPWM24_A		GPIO91			EPWM24_A
J5.49	I2C1_SCL		SPI3_CS0			XBAROUT7		GPIO23			

Table 3-29. Pinmux Options for J5 (continued)

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10
J5.50	I2C1_SDA		SPI3_CLK			XBAROUT8		GPIO24			

Table 3-30. Pinmux Options for J6

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10
J6.51	EPWM7_B			SPI6_CLK				GPIO58			EPWM5_B
J6.52	EPWM4_A							GPIO51			EPWM4_A
J6.53	EPWM12_A	UART3_CTSn	SPI4_CS1		MCAN7_RX		OSPI_D5	GPIO67			EPWM12_A
J6.54	SPI0_D1						FSITX0_D1	GPIO14		CHANNEL3	
J6.55	SPI0_D0						FSITX0_D0	GPIO13		CHANNEL2	
J6.56	PORz										
J6.57	EPWM12_B	UART1_DCDn	SPI7_CS0		MCAN7_TX		OSPI_D7	GPIO68			EPWM10_A
J6.58	SPI1_CS0	UART4_TXD	LIN4_TXD			XBAROUT1		GPIO15		CHANNEL4	
J6.59	EPWM0_B							GPIO44			EPWM0_B
J6.60	GND										

Table 3-31. Pinmux Options for J7

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9
J7.61	5V									
J7.62	GND									
J7.63	ADC2_AIN1									
	PR0_PRU1_GPIO16	MCAN5_RX		FSITX3_CLK	TRC_DATA10			GPIO113		
J7.64	ADC3_AIN1									
	PR0_PRU1_GPIO15	MCAN5_TX		FSITX3_D0	TRC_DATA11			GPIO114		
J7.65	ADC4_AIN1									
	LIN1_RXD	UART1_RXD	SPI2_CS0	OSPI_ECC_FAIL		XBAROUT5		GPIO19	OSPI_RESET_OUT1	
J7.66	ADC0_AIN2									
	LIN1_TXD	UART1_TXD	SPI2_CLK	OSPI_RESET_OUT0		XBAROUT6		GPIO20		
J7.67	ADC1_AIN2									
	UART5_RXD							GPIO127	SDFM0_D2	CHANNEL0
J7.68	ADC2_AIN2									
	UART5_TXD					I2C3_SCL		GPIO126	SDFM0_CLK2	CHANNEL8
J7.69	ADC3_AIN2									
	MCAN3_RX							GPIO129	SDFM0_D3	CHANNEL1
J7.70	DAC_OUT									
	MCAN3_TX	UART5_RXD						GPIO128	SDFM0_CLK3	CHANNEL9

Table 3-32. Pinmux Options for J8

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10
J8.71	PR0_PRU1_GPIO18		UART3_TXD	PR0_IEP0_EDIO_DATA_IN_OUT31	TRC_CTL	XBAROUT14		GPIO120		EQEP1_B	
J8.72	PR0_PRU1_GPIO19		UART3_RXD	PR0_IEP0_EDC_SYNC_OUT0	TRC_CLK	XBAROUT13		GPIO119		EQEP1_A	
J8.73	PR0_PRU1_GPIO17		UART5_CTSn	PR0_IEP0_EDIO_DATA_IN_OUT30				GPIO125	SDFM0_D1		
J8.74	PR0_PRU1_GPIO7	CPTS0_TS_SYNC	UART5_RTSn	PR0_IEP0_EDC_SYNC_OUT1		I2C3_SDA		GPIO124	SDFM0_CLK1		
J8.75	EPWM9_A			SPI7_CS0	MCAN4_RX		FSITX2_DATA1	GPIO61			EPWM9_A
J8.76	EPWM9_B	UART1_RTSn		SPI7_CLK	MCAN4_TX		FSIRX2_CLK	GPIO62			EPWM11_B
J8.77	EPWM3_A							GPIO49			EPWM3_A
J8.78	EPWM3_B							GPIO50			EPWM6_A
J8.79	EPWM13_A	UART1_RIn	SPI7_CLK				OSPI_D3	GPIO69			EPWM13_A
J8.80	EPWM13_B	UART1_DTRn	SPI7_D0				OSPI_ECC_FAIL	GPIO70			EPWM13_B

Table 3-33. Pinmux Legend

Default signal for BP Header	Muxed alternative signal	External MUX for alternate signal options

4 Additional Information

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4.1 Sitara MCU+ Academy

TI offers the *MCU+ Academy* as a resource for designing with the MCU+ software and tools on supported devices. The MCU+ Academy features easy-to-use training modules that range from the basics of getting started to advanced development topics.

4.2 Known Board Changes/Issues

The below sections capture all the known issues/observations on the board and solutions/fixes for the same. Please note that some of these are already fixed on boards ordered from ti.com, as mentioned in respective sections.

4.2.1 OSPI DQS and LBCLK nets swap

In AM263P the ball pins for OSPI DQS and LBCLK are as per below

- OSPI0_DQS is from Ball pin M3
- OSPI0_LBCLKO is from Ball pin L3

But as seen in the below image from LP-AM263P Schematics, the nets are wrongly swapped.

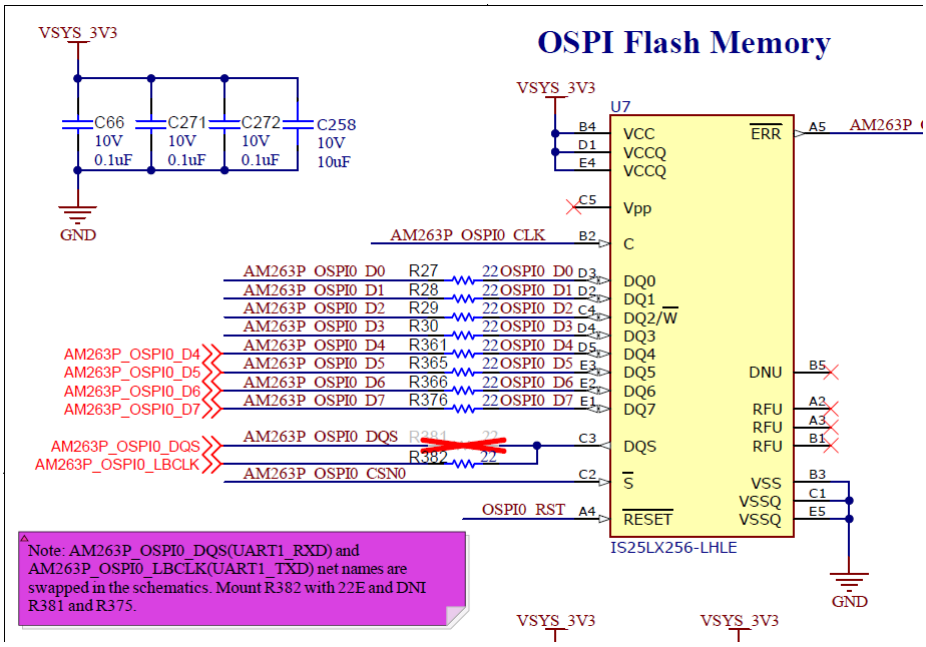

Figure 4-1. OSPI DQS and LBCLK nets caution note in LP-AM263P Schematic

Hence to rectify this, as mentioned in the same schematic the resistor R381 is unmounted and the resistor R382 is mounted with 22Ω resistor. Also the resistor R375 is unmounted.

All boards ordered from ti.com already have this change made.

4.2.2 XDS110 Debugger Bricking Issue

It has been found that few EVMs when connected to the PC and connect through Code Composer Studio(CCS), the user is prompted to update the firmware as per below window. Upon clicking on Update button, the update is unsuccessful and CCS just disconnects from the board and the board is no longer detected by CCS. This has been mostly observed with CCS versions 12.4 and above.

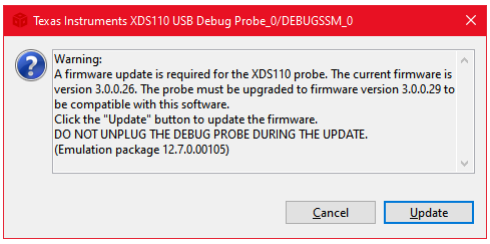

Figure 4-2. CCS prompt to update firmware

The below are the steps of recovering a board when CCS fails to detect the board as mentioned above.

The failure to detect the board is mostly attributed to the wrong firmware version on the XDS110 debugger on the board. Thus the XDS110 debugger would need to be re-flashed with the latest firmware available with the CCS on the user's PC. Follow the below steps to do the same.

1. Disconnect all cables connected to LP-AM263P.
2. Short pins 64 and 97(shown in below image) of the U24 component(TM4C being the XDS110 debugger) and connect back the USB Micro-B debugger cable to LP-AM263P and PC, while pins 64 and 97 are shorted. Now the XDS110 debugger will be in DFU mode.

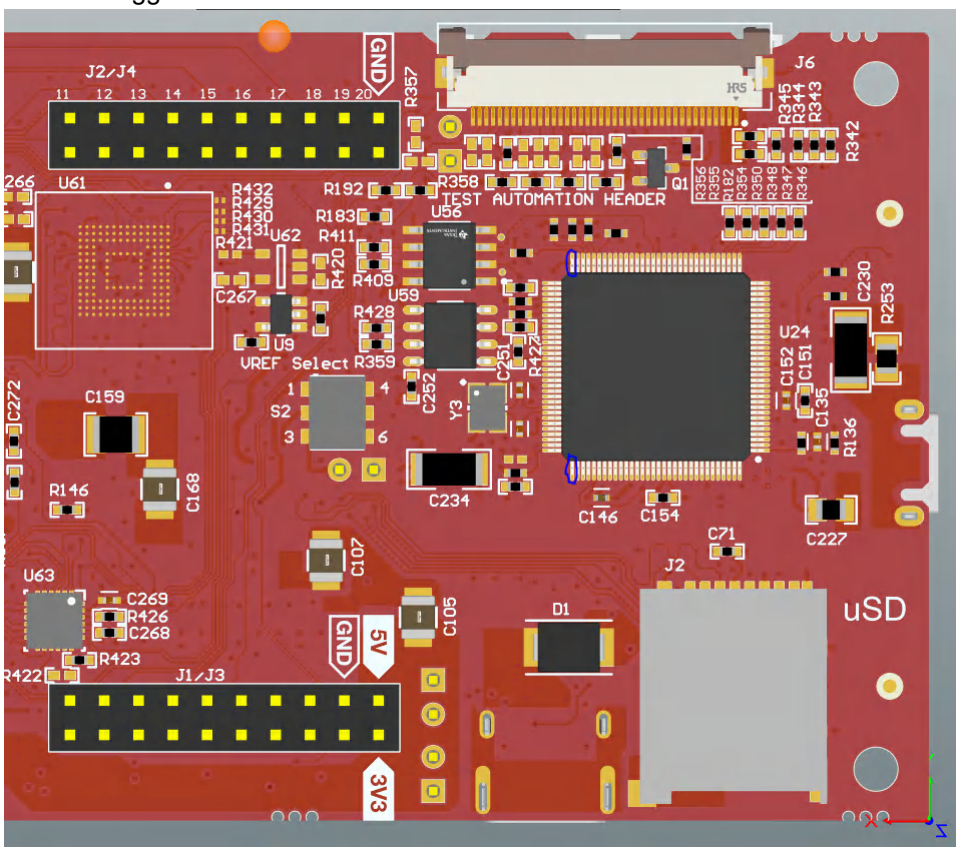

Figure 4-3. Location of Pins 64 and 97 on U24

3. Open Command Prompt on your Windows PC and navigate to C:\ti\ccs12XX\ccs\ccs_base\common\uscif\xds110, where 12XX corresponds to the CCS version on the PC.
4. Run command "xdsdfu -e" and the device must be reported with Mode as "DFU". If not, please repeat Steps 1 to 3 ensuring the pin shorting is done properly.
5. After the debugger is in DFU mode, run command "xdsdfu -f firmware_3.0.0.XX.bin -r" where 3.0.0.XX is the corresponding XDS firmware version found in "C:\ti\ccs12XX\ccs\ccs_base\common\uscif\xds110" path. This starts the firmware upgrade utility and flashes the mentioned firmware to the XDS110 debugger.
6. Once step 5 is complete, run command "xdsdfu -e" once more to see that the XDS110 debugger is detected by the PC as shown in below image with all the above steps.

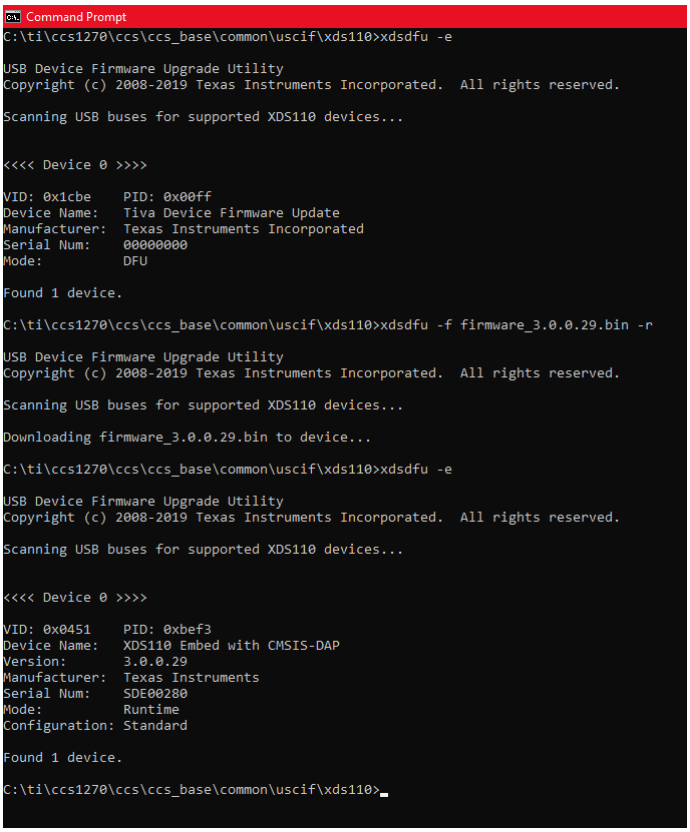

Figure 4-4. XDS110 Firmware update commands in Command Prompt

Post the above steps are complete, CCS should be able to detect and connect to the XDS110 debugger on LP-AM263P.

More details about XDS110 firmware and updating it can be found in *https://software-dl.ti.com/ccs/esd/documents/xdsdebugprobes/emu_xds110.html#manual-update*

4.2.3 eMMC CMD and CLK nets swap

The LP-AM263P has an eMMC footprint on board, for the part MTFC8GAMALBH-AAT. But it is seen that the CMD and CLK nets are wrongly swapped. The correct nets should be connected as per below

- U61 Pin M6 should be connected to AM263P_EMMC0_CLK_MUX net
- U61 Pin M5 should be connected to AM263P_EMMC0_CMD_MUX net

Users are suggested to do board re-work before using this eMMC footprint. Please raise an e2e ticket for details on this.

5 References

5.1 Reference Documents

In addition to this document, the following references are available for download at www.ti.com.

- *AM263P4 Sitara™ Microcontrollers*
- *AM263Px Sitara™ Microcontrollers Data Sheet*
- *AM263Px Sitara™ Microcontrollers Technical Reference Manual*
- *AM263Px Sitara™ Microcontrollers Silicon Errata*
- *Texas Instruments Code Composer Studio*
- *Updating XDS110 Firmware*
  - To find the serial number, only follow steps 1 and 2 of updating XDS110 firmware

5.2 Other TI Components Used in This Design

This LaunchPad uses various other TI components for its functions. A consolidated list of these components with links to their TI data sheets is shown below.

- *TUSB320USB Type-C Configuration Channel Logic and Port Controller*
- *TPD4E02B04 4-Channel ESD Protection Diode for USB Type-C*
- *TPS22965x-Q1 5.5-V, 4-A, 16-mΩ On-Resistance Load Switch*
- *TPS6291x 3-V to 17-V, 2-A/3-A Low Noise and Low Ripple Buck Converter*
- *TPS748 1.5-A Low-Dropout Linear Regulator*
- *TCA6408A Low-Voltage 8-Bit I 2C and SMBus I/O Expander*
- *SN74AVC4T245 Dual-Bit Bus Transceiver with Configurable Voltage Translation*
- *TPS22918-Q1, 5.5-V, 2-A, 52-mΩ On-Resistance Load Switch*
- *TPD6E001 Low-Capacitance 6-Channel ESD-Protection for High-Speed Data Interfaces*
- *XDS110 JTAG Debug Probe*
- *TS5A23159 1-Ω 2-Channel SPDT Analog Switch*
- *TCAN1044V-Q1 Automotive Fault-Protected CAN FD Transceiver*
- *DP83869HM High Immunity 10/100/1000 Ethernet Physical Layer Transceiver*
- *TS3DDR3812 12-Channel, 1:2 MUX/DEMUX Switch for DDR3 Applications*
- *TCA9617B Level-Translating I2C Bus Repeater*
- *SN74CB3Q3257 4-Bit 1-of-2 FET Multiplexer/Demultiplexer*
- *TPIC2810 8-Bit LED Driver with I2C Interface*
- *TPS796xx 1-A Low-Dropout Linear Regulators*
- *TXB0108 8-Bit Bidirectional Voltage-Level Translator with Auto-Direction Sensing*
- TCA6416ARTWR 16-bit translating 1.65- to 5.5-V I2C/SMBus I/O expander

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2024) to Revision A (August 2024)	Page
• Added a note on Boot mode selection SOP switches	16
• Added section on Known Board Changes/Issues	53

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