User's Guide

AM62Ax/AM62Dx Escape Routing for PCB Design

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1 Introduction

The AM62Ax/AM62Dx are based on the Cortex-A53 microprocessor, M4F microcontroller with dedicated peripherals, 3D graphics acceleration, dual display interfaces, and extensive peripheral and networking options for a variety of embedded applications. The AM62Ax is available in a 18-mm × 18-mm FBGA package with a 0.8-mm ball pitch. The package BGA design is built leveraging TI Flip Chip BGA Technology (FC-BGA) technology. The AM62Dx is available in a 18-mm × 18-mm FCCSP package with a 0.8-mm ball pitch. Device-specific data sheets should be referenced to document specific features and package availability.

This document is intended to provide a reference for escape routing on the AM62Ax and AM62Dx device. Care must be taken to route signals with special requirements such as DDR, high speed interfaces. for more information, see the *High-Speed Interface Layout Guidelines* and *DDR Routing Guidelines*. Details on Power Delivery Network are provided in *Sitara Processor Power Distribution Networks: Implementation and Analysis* and any routing and layout requirements specified in those documents supersede the generic requirements provided here.

2 Width/Spacing Proposal for Escapes

The AM62Ax/AM62Dx has been designed to support the following. The AM62Ax/AM62Dx package supports a similar feature set as several other competing solutions with smaller package area and wider line width. This solution reduces PCB foot print and utilizes lower cost PCB rules, enabling compact and low-cost systems.

Table 2-1. Width/Spacing Proposal for Escapes

PCB Feature	PCB Routing Requirements	Comments
Minimum via diameter	18 mils	Via pads dia - 18Mils Via hole dia - 8Mils
Via hole size	8 mils	
Minimum trace width/spacing required in the BGA breakout (Inner Layer)	Trace width – 3.5mils Spacing – 3.49mils	
Minimum trace width/spacing required in the BGA breakout (External Layer)	Trace width – 3.5mils Spacing – 4mils	
Number of layers used for escape	8	• Top (1 Layer) • Signal (3 Layer) • Power (3 Layer) • Bottom (1 Layer)
BGA land pad size	18mils	
Package Size	18mm × 18mm	
PCB layers (signal routing, total) recommended		• Top (1 Layer) • Signal (3 Layer) • Power (3 Layer) • Ground (4 Layer) • Bottom (1 Layer)

3 Stackup

PCB stack-up is one of the first and most important considerations in realizing a successful PCB. The AM62Ax/AM62Dx device supports a BGA array of 22x22 with a 0.8-mm pitch and a body size of 18mm. Due to the number of rows of signal balls around the periphery, TI recommends three signal routing layers. PDN compliance and robustness is critical to meet all the performance objectives of the device and associated peripherals. To enable this, TI recommends allocating three layers for power planes. Ground planes must be added adjacent to the power planes and adjacent to the outer layers for shielding and controlled impedance routing. High speed interfaces such as DDR, CSI, and USB require ground planes for impedance matching. Additionally, to meet the higher DDR interface speeds, ground layers both above and below the DDR signals are recommended. The escapes and routing on the AM62Ax/AM62Dx board design was achieved with 12 layers as shown in Table 3-1.

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Table 3-1. Example PCB Layer Stack-up

PCB Layer	Layer Routing, Planes or Pours
Layer 1	Component pads, ground, and signal escapes
Layer 2	Ground
Layer 3	Signal Routing
Layer 4	Ground
Layer 5	Signal Routing
Layer 6	Power/Ground ref for DDR
Layer 7	Power
Layer 8	Power
Layer 9	Ground
Layer 10	Signal Routing
Layer 11	Ground
Layer 12	Component pads, power, and ground routes

An example 12-layer board stack-up for AM62Ax/AM62Dx is described above. This board is designed for optimum signal integrity on the high-speed interfaces while limiting the board size. The AM62Ax/AM62Dx board is implemented without High Density Interconnect (HDI) and does not use micro vias, which are both intended to save board cost. All vias on the AM62Ax/AM62Dx board are Plated Through Hole (PTH) and pass completely through the board. Proper analysis shall be performed to validate both signal and power integrity, if further optimizations are required to reduce PCB stack-up and/or routing rules illustrated in this document.

4 Via Sharing

The FC-BGA pattern implemented on the AM62Ax/AM62Dx design offers opportunities for via sharing. Vias are shared across BGA pins. Figure 4-1 and Figure 4-2 show the via sharing opportunities for VDD_LDDR4 and VSS power supplies, respectively. Via sharing across BGA pins provides for easier escape routing and also robust electrical connection by connecting multiple pins.

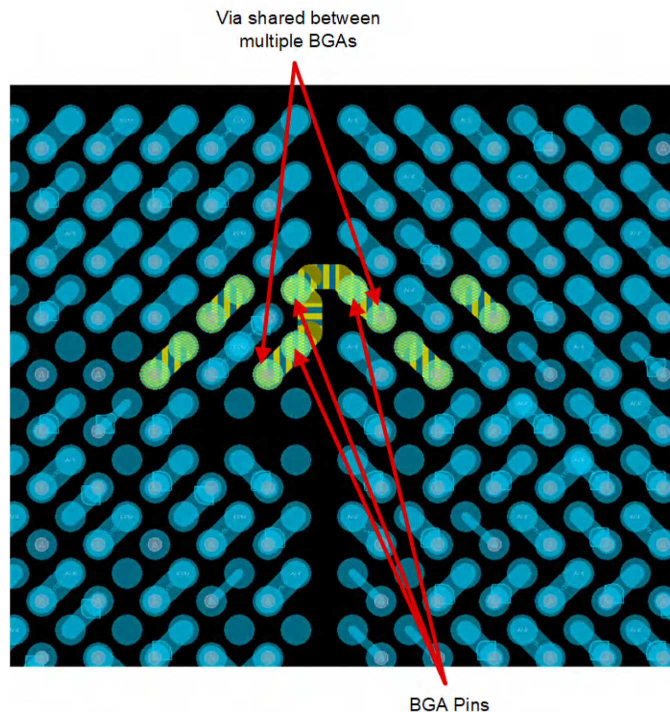

Figure 4-1. Via Sharing for VDD_LPDDR4 Domain

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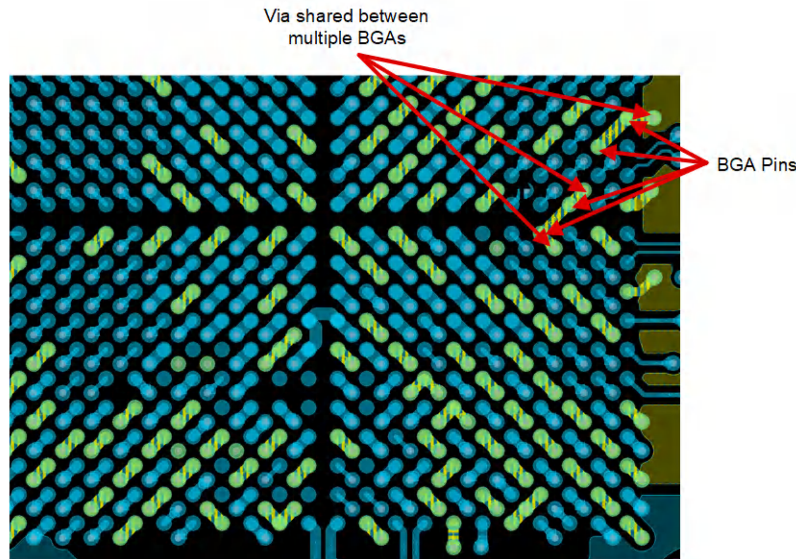

Figure 4-2. Via Sharing for VSS

5 Floorplan Component Placement

Careful analysis is required to analyze the locations of the interfaces used on the device and the associated components and connectors. Optimum trace routing has routes as short as possible with a minimum cross-over. The AM62Ax/AM62Dx offers interface selection flexibility through pin-mux choices. Pin-muxing enables the same interface function made available on multiple pins and is selectable through a pin mux option. Favorable pin-mux options that ease PCB routing and component placement can be fully utilized to further optimize the PCB design. The figure below shows the arrangement of the signal balls and the power and ground balls. Priority is given to component placements without pin-mux options, such as DDR, CSI, USB, and so forth.

VSS	RGMII2_RD2	RGMII2_RD3	RGMII2_TXC	VSS	RGMII1_TXC	RGMII1_RD0	VSS	CSI0_RXCLKN	CSI0_RXCLKP	VSS	CSI0_RXN3	CSI0_RXP3	VSS	MMC0_DAT7	MMC0_CLK	MMC0_DAT1	VSS	DDR0_DQ31	VSS	VDDS_DDR	VSS
VOUT0_PCLK	RGMII2_RD0	RGMII2_RXC	RGMII2_TD0	RGMII2_TD2	RGMII1_TD3	RGMII1_RXC	RGMII1_RX_CTL	VSS	CSI0_RXN2	CSI0_RXP2	VSS	USB0_DM	USB0_DP	VSS	MMC0_DAT3	MMC0_DAT0	DDR0_DQ30	VSS	DDR0_DQ29	VSS	VDDS_DDR
VOUT0_DATA15	VOUT0_DATA14	RGMII2_RD1	RGMII2_TX_CTL	RGMII2_TD1	RGMII1_TD0	RGMII1_TD2	VSS	CSI0_RXP1	CSI0_RXN1	VSS	USB1_DM	USB1_DP	VSS	MMC0_DAT4	MMC0_DAT2	MMC0_CMD	VSS	DDR0_DQ28	VSS	DDR0_DQ24	DDR0_DQS3_N
VOUT0_DATA10	VOUT0_DATA11	VOUT0_DATA12	VOUT0_DATA13	RGMII2_RX_CTL	RGMII2_TD3	RGMII1_TX_CTL	RGMII1_RD2	VSS	CSI0_RXP0	CSI0_RXN0	VSS	USB0_RCALIB	MMC0_DAT6	VSS	MMC0_DAT5	VSS	DDR0_DQ27	VSS	DDR0_DM3	VSS	DDR0_DQS3
VOUT0_DATA6	VOUT0_DATA7	VSS	VOUT0_DATA8	VOUT0_DATA9	VOUT0_VSYNC	RGMII1_TD1	RGMII1_RD1	RGMII1_RD3	MDIO0_MDIO	MDIO0_MDC	CSI0_ATB_0_H	CSI0_RXRCALIB	VSS	USB0_VBUS	VSS	USB1_VBUS	VSS	DDR0_DQ26	VSS	DDR0_DQ25	VSS
VOUT0_DATA0	VOUT0_DATA1	VOUT0_DATA2	VOUT0_DATA3	VOUT0_DATA5	VOUT0_DE	VSS	VDD_CORE	VSS	VDDSHV2	VSS	CSI0_ATB_1_H	VDDA_3P3_USB	VSS	VDDSHV4	USB1_RCALIB	VSS	DDR0_DQ18	VSS	DDR0_DQ23	VSS	DDR0_DM2
GPMC0_AD12	GPMC0_AD15	GPMC0_AD14	VOUT0_DATA4	VOUT0_HSYNC	VSS	VDD_CORE	VSS	CAP_VDDS2	VDDSHV2	VDDA_1P8_CSIRX0	VDDA_CORE_CSIRX0	VDDA_1P8_USB	VDDA_CORE_USB	VDDSHV4	VSS	DDR0_DQ16	VSS	DDR0_DQ17	VSS	DDR0_DQ22	VSS
GPMC0_AD11	GPMC0_AD13	GPMC0_AD10	GPMC0_AD9	GPMC0_WAIT0	GPMC0_WAIT1	VSS	VDD_CORE	VSS	VDDSHV2	VSS	VDDA_PLL1	VSS	VDD_CORE	CAP_VDDS4	DDR0_BG1	VSS	DDR0_DQ19	VSS	DDR0_DQ21	VSS	DDR0_DQS2
GPMC0_AD8	GPMC0_AD7	VSS	GPMC0_AD6	GPMC0_AD5	VSS	VDDA_TEMP0	VSS	VDD_CORE	VSS	VDDR_CORE	VSS	VDD_CORE	VDDR_CORE	VDDS_DDR	VSS	DDR0_RESET0_N	DDR0_CKE1	DDR0_BG0	DDR0_CKE0	DDR0_DQ20	DDR0_DQS2_N
GPMC0_CLK	GPMC0_AD0	GPMC0_AD1	GPMC0_AD2	GPMC0_AD3	GPMC0_AD4	VSS	VDDSHV3	VSS	VDD_CORE	VSS	VDD_CORE	VSS	VDDA_PLL0	VSS	VDDS_DDR	DDR0_WE_N	DDR0_ACT_N	DDR0_CS1_N	DDR0_ODT1	DDR0_PAR	VSS
GPMC0_CSN2	GPMC0_CSN1	GPMC0_CSN3	GPMC0_CSN0	GPMC0_BE1N	VSS	CAP_VDDS3	VDDSHV3	VDDR_CORE	VDDA_PLL2	VDD_CORE	VSS	VDDR_CORE	VDDA_DDR_PLL0	VDDS_DDR	VSS	DDR0_RAS_N	DDR0_CAS_N	VSS	DDR0_A12	DDR0_A13	DDR0_CK0
OSPI0_CLK	OSPI0_DQS	VSS	GPMC0_BE0N_CLE	GPMC0_ADVN_ALE	GPMC0_OEN_REN	VDDSHV1	VDDSHV3	VSS	VDD_CORE	VSS	VDD_CORE	VDDA_TEMP2	VDD_CORE	VDDS_DDR_C	VDDS_DDR	DDR0_A8	DDR0_A11	DDR0_A3	VSS	DDR0_A9	DDR0_CK0_N
OSPI0_LBCLKO	OSPI0_D4	OSPI0_CSN2	GPMC0_WEN	GPMC0_DIR	GPMC0_WPN	CAP_VDDS1	VDDSHV1	VDD_CORE	VDDA_PLL3	VDDR_CORE	VSS	VDDA_PLL4	VSS	VDDS_DDR	VSS	DDR0_BA0	DDR0_A5	VSS	DDR0_A6	DDR0_A10	VSS
OSPI0_D7	OSPI0_D0	OSPI0_D6	OSPI0_D2	OSPI0_D1	VSS	CAP_VDDS6	VDD_CORE	VDDR_CORE	VDD_CORE	VSS	VDD_CORE	VDDA_MCU	VDD_CORE	VDDS_OSC0	VDDS_DDR	DDR0_CS0_N	DDR0_A0	DDR0_A2	VSS	DDR0_A1	DDR0_A4
MMC2_CLK	OSPI0_CSN0	VSS	OSPI0_D5	OSPI0_D3	VDDSHV6	VDDSHV6	VDDSHV5	VSS	VDDSHV0	VMON_ER_VSYS	VSS	VDDSHV_MCU	VDD_CANUART	VDDSHV_CANUART	DDR0_ALERT_N	DDR0_CAL0	DDR0_ODT0	VSS	DDR0_BA1	DDR0_A7	VSS
MMC2_CMD	MMC2_DAT3	OSPI0_CSN3	OSPI0_CSN1	VDDA_TEMP1	VSS	VDDSHV5	CAP_VDDS5	VDDSHV0	CAP_VDDS0	VSS	VDDSHV_MCU	CAP_VDDS_MCU	VSS	CAP_VDDS_CANUART	DDR0_ATB0	DDR0_DQ12	VSS	DDR0_DQ13	VSS	DDR0_DQ11	DDR0_DQS1
MMC2_SDCD	MMC2_DAT1	MMC2_DAT2	RESETSTATZ	PORZ_OUT	EXTINTN	VSS	TRSTN	UART0_CTSN	VSS	VMON_1P8_SOC	VSS	TEMP_DIODE_P	VMON_3P3_SOC	MCU_UART0_TXD	VPP	DDR0_ATB1	DDR0_DQ9	VSS	DDR0_DM1	VSS	DDR0_DQS1_N
MMC1_CLK	MMC2_SDWP	MMC2_DAT0	RESET_REQZ	MMC1_SDCD	I2C1_SDA	I2C0_SDA	SPI0_D1	UART0_RXD	WKUP_I2C0_SDA	MCU_I2C0_SCL	MCU_SPI0_CS0	EMU1	WKUP_UART0_TXD	MCU_MCAN0_RX	ATEST0	DDR0_DQ10	VSS	DDR0_DQ14	VSS	DDR0_DQ8	VSS
MMC1_DAT3	MMC1_DAT1	VSS	USB1_DRVVBUS	MMC1_SDWP	I2C0_SCL	SPI0_CS0	UART0_TXD	MCU_RESETSTATZ	WKUP_I2C0_SCL	PMIC_LPM_EN0	VSS	MCU_UART0_RTSN	MCU_I2C0_SDA	MCU_UART0_RXD	MCU_MCAN1_TX	VSENSE	DDR0_DQ3	VSS	DDR0_DQ15	VSS	DDR0_DQS0
MMC1_DAT2	MMC1_CMD	USB0_DRVVBUS	MCASP0_AXR3	MCAN0_RX	I2C1_SCL	SPI0_CS1	UART0_RTSN	TDO	EMU0	MCU_RESETZ	MCU_SPI0_CS1	WKUP_UART0_CTSN	WKUP_UART0_RXD	WKUP_UART0_RTSN	MCU_MCAN0_TX	IFORCE	DDR0_DQ4	VSS	DDR0_DQ5	DDR0_DM0	DDR0_DQS0_N
MMC1_DAT0	MCASP0_AFSR	MCASP0_AXR0	MCASP0_AXR2	MCASP0_AXR1	MCAN0_TX	EXT_REFCLK1	SPI0_D0	TMS	MCU_SPI0_CLK	MCU_SPI0_D1	MCU_UART0_CTSN	WKUP_CLKOUT0	MCU_MCAN1_RX	MCU_ERRORN	VSS	DDR0_DQ2	VSS	DDR0_DQ1	VSS	DDR0_DQ6	VDDS_DDR
VSS	MCASP0_ACLKR	MCASP0_AFSX	MCASP0_ACLKX	VSS	SPI0_CLK	TDI	MCU_SPI0_D0	TCK	VSS	MCU_OSC0_XI	MCU_OSC0_XO	VSS	WKUP_LFOSC0_XO	WKUP_LFOSC0_XI	MCU_PORZ	VSS	DDR0_DQ0	VSS	DDR0_DQ7	VDDS_DDR	VSS

DDR3
DDR2
DDR Addr
DDR1
DDR0
MCU
GENERAL
GPMC
I2C
MCAN
MCASP
MMC0
MMC1
MMC2
GPMC
VOUT
OSPI
RGMII2
RGMII1
CSI
VDD_CORE
VDDR_CORE
VDDSHV
WKUP_MCU

Figure 5-1. AM62Ax/AM62Dx Floorplan

6 Critical Interfaces Impact Placement

Placement of the AM62Ax/AM62Dx device and some of the component and/or connectors is also dictated by some of the highest performance interfaces, such as DDR, CSI, USB, and so forth. Additionally, due to the PCB losses at multi-gigabit rates, there are routing distance limits that may also limit component placement.

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7 Routing Priority

As indicated above, critical interfaces affect component placement options. The next step in PCB design is to prioritize routing to these critical interfaces. Those with higher priority must be completed before implementing those of lower priority. It is imperative to route interfaces with the higher priority first. PCB layout teams often end up in a time intense, iterative process with sub optimal results when routing priorities are not established.

Table 7-1 lists a recommended priority order for interfaces contained on the AM62Ax/AM62Dx family of devices. Individual design requirements may drive a need for adjustment of the priorities but this serves as a good baseline and has been used for the board example illustrated in this document.

Table 7-1. Routing Priority

Interface	Routing Priority
DDR4/LPDDR4	10 (Highest Priority)
CSI	9
OSC	8
USB2, OSPI	8
Power distribution	7
RGMII	6
eMMC	5
Clocks	5
MII / RMII	4
SPI	4
Motor control	4
Analog	3
GPMC	2
GPIO	1
UART/CANUART	1
I2C/Temp Diode	1 (Lowest Priority)

The multi-gigabit DDR (dual data-rate) interface is the most critical due to its data rate and loss concerns. DDR is at the top of the priority list because it is very sensitive to PCB losses. Additionally, being single ended in nature makes it highly susceptible to signal integrity issues such as crosstalk, especially at the high speeds targeted in this design. Next in the priority list is the CSI (Camera Serial) interface. The limited length for these routes might affect the PCB placement of the CSI connector and theAM62Ax/AM62Dx device. CSI signals are found on the outer layers of the BGA footprint allowing some of the CSI traces to escape from the BGA without vias.

The asynchronous and low speed interfaces are at the bottom. This leaves the synchronous and source-synchronous interfaces on the top ordered by data rate. The one surprise may be power distribution. If left to last, it results in poor decoupling performance or current starvation and excessive power supply noise due to insufficient copper to carry the power and ground currents. **Space for copper and decoupling must be allocated before routing the middle and low priority interfaces.**

8 SerDes Interfaces

The package BGA ball map is also arranged to support routing the high priority interfaces first. Therefore, the SerDes CSI interfaces are located close to the outer rings. The lanes located on the outermost row of BGAs can be escaped on the top layer. The lanes located on inner BGA rows require vias to escape as a differential pair on the bottom or on an interior layer. The BGA map facilitates this for inner rows. Figure 8-1 shows an example of the SerDes signals on the AM62Ax/AM62Dx board on the top layer and on an inner layer. Wide traces can limit the signal loss but could violate the impedance requirements. For more detailed information on routing Serdes signals, see the *High-Speed Interface Layout Guidelines*.

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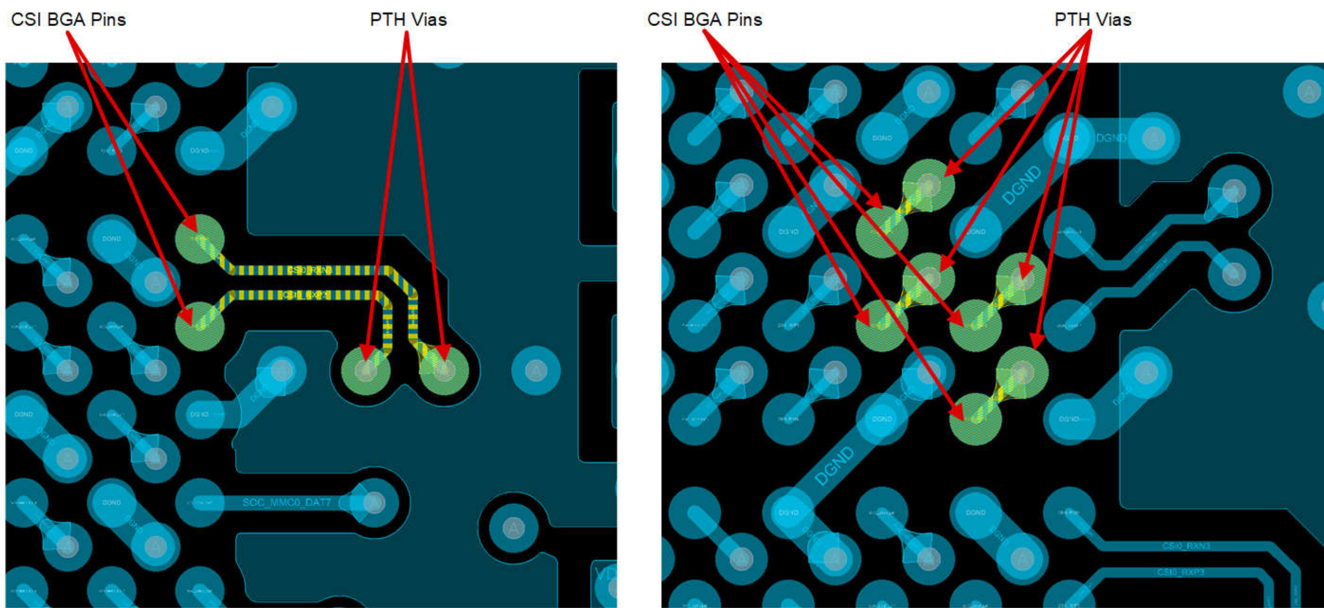

Figure 8-1. Serdes CSI Escapes for Top Layer (Left) and Inner Layer (Right)

9 DDR Interfaces

The AM62Ax/AM62Dx SoC supports connection to an LPDDR4 device. The DDR signals must be routed at the highest priority, as noted in Table 7-1. For detailed recommendations for DDR routing, see the *DDR Routing Guidelines*. The images below show the BGA breakout for the DDR interface on the AM62Ax/AM62Dx

The DDR SDRAM memory devices are normally arranged so that the data group balls are closest to the AM62Ax/AM62Dx device. The Package BGA ball map has been carefully planned to place the DDR address and command signals between data byte lanes 0 and 1 and data byte lanes 2 and 3.

Figure 9-1 and Figure 9-2 illustrate how to escape the DDR byte lanes 0 and 1, respectively. Similarly, Figure 9-3 and Figure 9-4 illustrate the escape of DDR byte lanes 2 and 3, respectively. The use of Plated Through Hole (PTH) vias make the routing of these signals between the SoC and SDRAM possible on any layer.

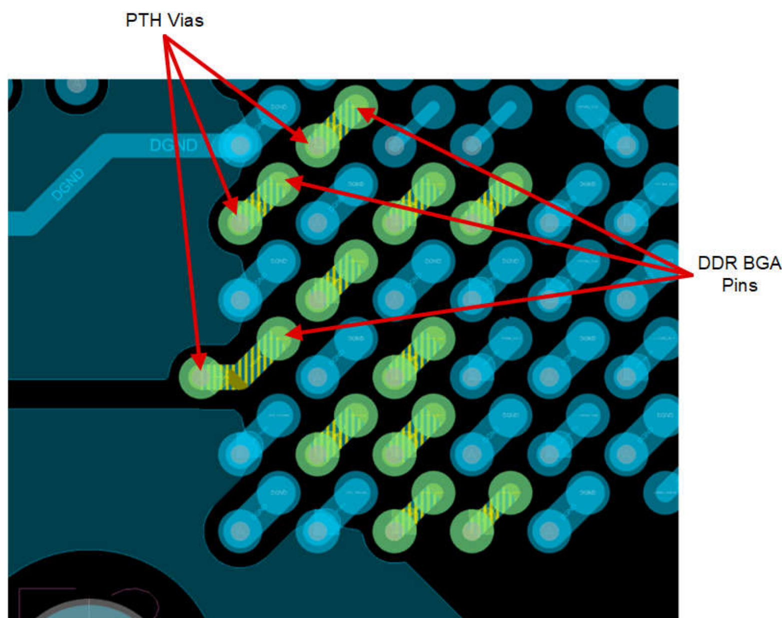

Figure 9-1. DDR Byte Lane0 Escape

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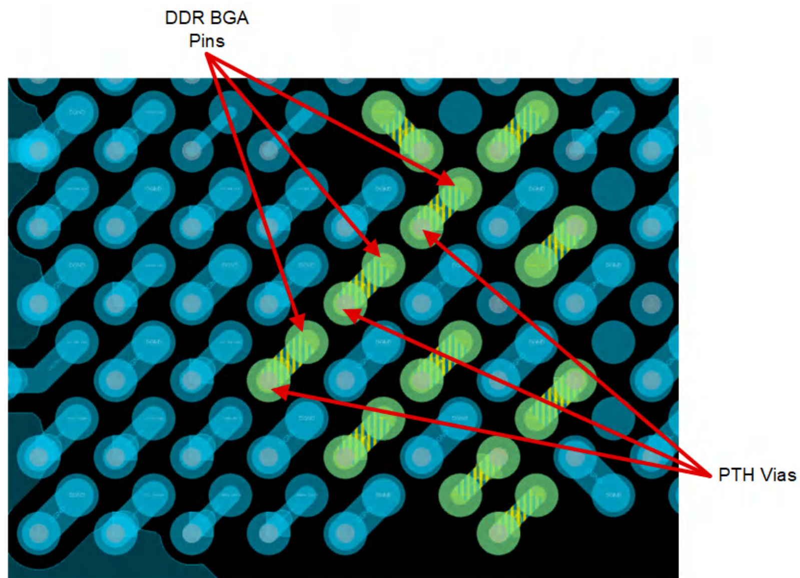

Figure 9-2. DDR Byte Lane1 Escape

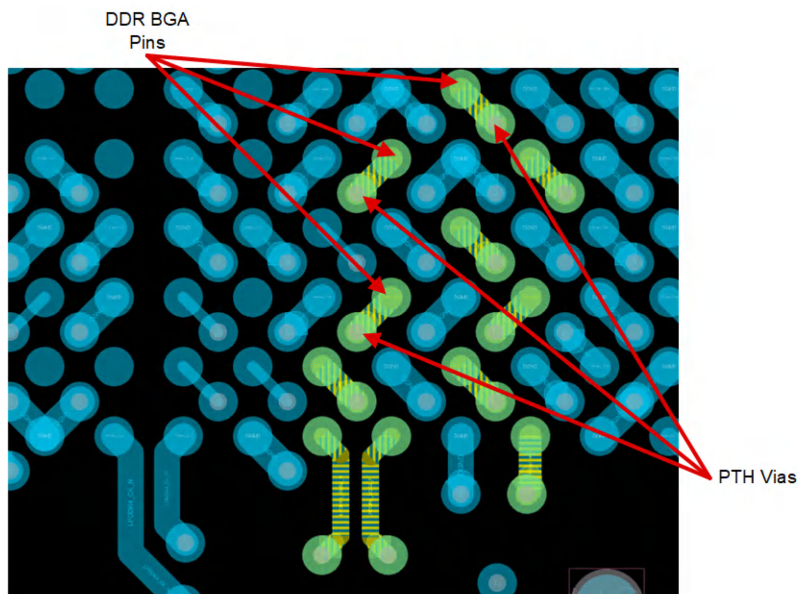

Figure 9-3. DDR Byte Lane 2 Escape

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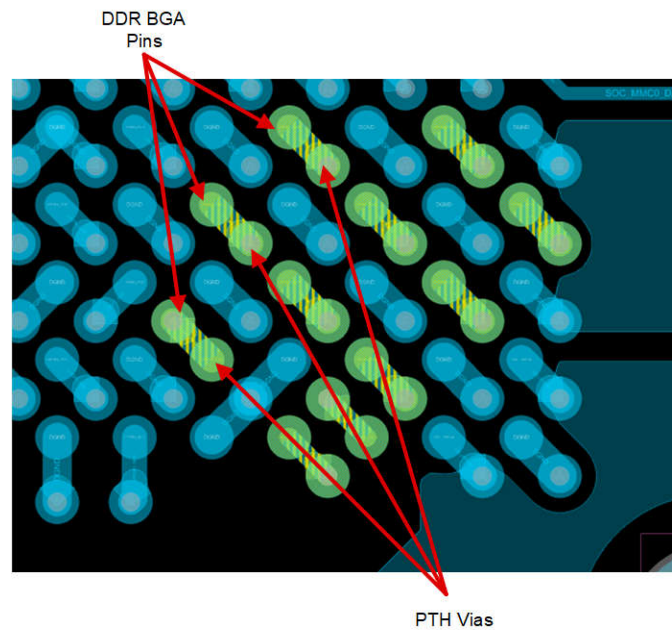

Figure 9-4. DDR Byte Lane 3 Escape

The address, command, and clock signals are routed directly to the memory device.

The top and inner layers are used to escape and route the address and command signals. The traces must be length matched to ensure that the signals arrive at the memory at the same time. Length matching must be from the SoC to memory pin individually, and must include the stub to the memory pad and all via lengths. For detailed recommendations for DDR routing, see the *DDR Routing Guidelines*.

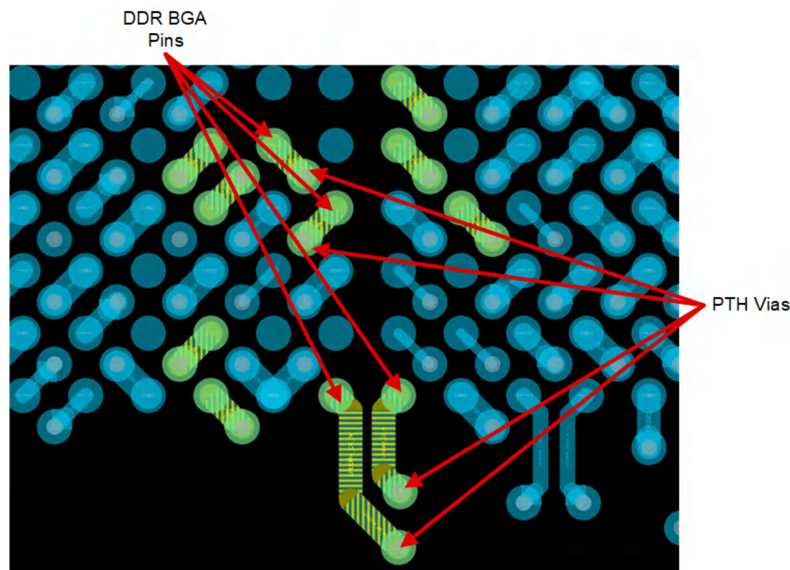

Figure 9-5. DDR Address/Cmd Escape

The escapes of the address and command signals for an LPDDR4 interface on these layers are shown above in Figure 9-5.

Address signals are routed directly from the SoC to the via next to the associated pad for the memory device. This requires that the address signals escape in the correct order. It is required to have the same number of vias for each of the address and command signals. The use of Plated Through Hole (PTH) vias allows the flexibility of routing the address/cmd signals on any layer.

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10 Power Decoupling

The middle priority interfaces and the power distribution planes and pours are routed next after the SerDes and DDR interfaces. TI recommends completing all SerDes and DDR routing before continuing with other interfaces. The power distribution planes and pours and all of the decoupling must be placed before PCB simulations are executed for the SerDes and DDR routes, as these can influence the return currents for the high-speed interfaces. The highest speed source-synchronous interfaces, such as RGMII and QSPI, may also require simulation, so these may also need to be completed at this time.

Special care is needed for the 1-uF output capacitors connected to the CAP_VDDS* BGA pins on the AM62Ax/AM62Dx device. These capacitors should be placed as close to the pin as possible, and a low inductance path should be present between the CAP_VDDS BGA pin and the supply pad on the capacitor. The layout used on the CAP_VDDS0, CAP_VDDS1, CAP_VDDS5, and CAP_VDDS6 nets on the AM62Ax/AM62Dx board is shown below in Figure 10-1. Note the sharing of the GND pad of the capacitors with other capacitors in the vicinity, which allows saving routing resources. Also, it is important to keep the PTH vias for the capacitor power and GND pad connections as close to each other as possible to minimize the loop inductance.

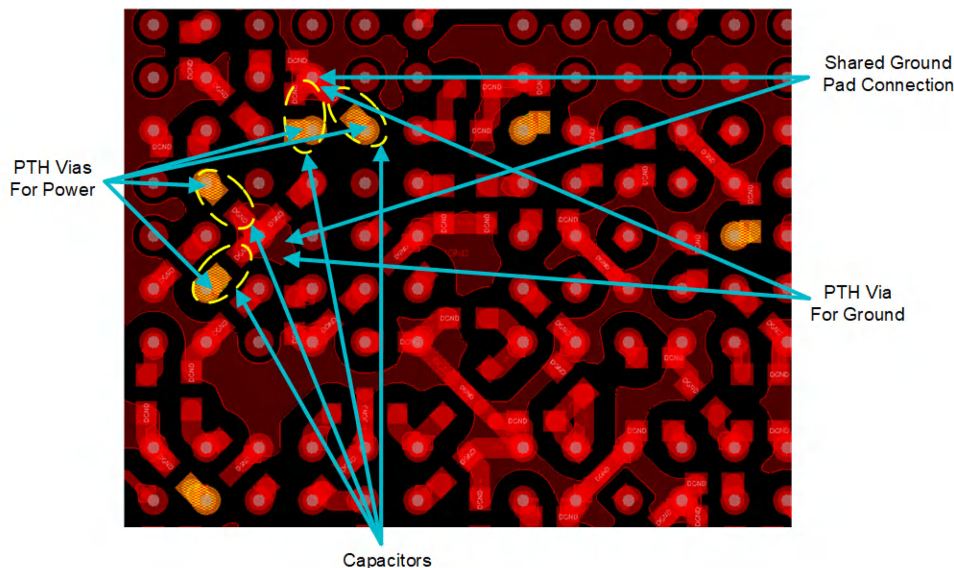

Figure 10-1. Output Capacitor Placement for CAP_VDDS Nets

This placement can be improved if the capacitors can be placed directly under the SoC. The decoupling capacitors for the VDD_CORE and VDDS_DDR supplies should also receive the same priority as those on the CAP_VDDS* pins and should be placed under the socket, with minimum inductance connections to the respective BGA pins on the AM62Ax/AM62Dx device.

11 Route Lowest Priority Interfaces Last

When the length matching and simulations for high speed interfaces and DDR have been completed for the highest priority interfaces and the Power Distribution Network (PDN) analysis has been completed, then the layout can continue with the medium and then the lower priority interfaces.

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12 Summary

A picture with the AM62Ax/AM62Dx with all signals and power escaped is shown in Figure 12-1.

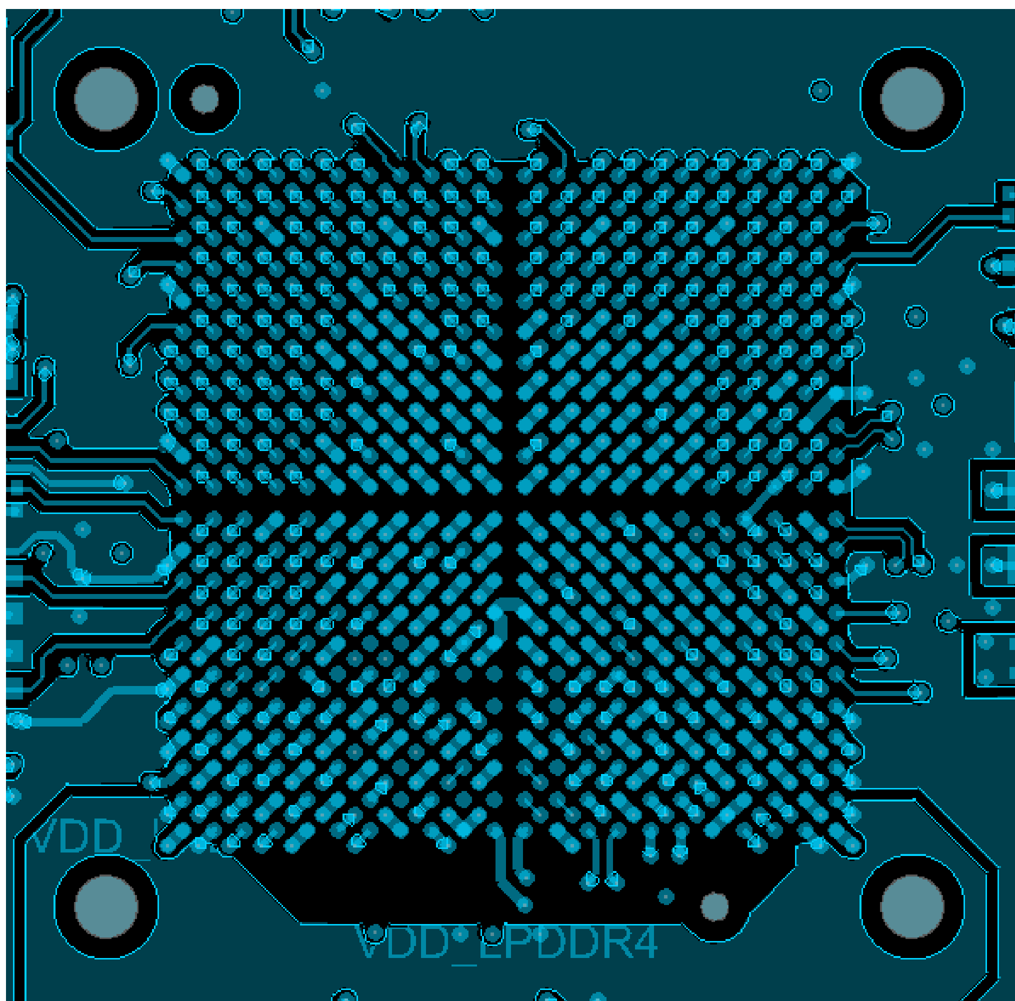

Figure 12-1. AM62Ax with Complete Signal and Power Escapes

13 References

- Texas Instruments: *High-Speed Interface Layout Guidelines*
- Texas Instruments: *DDR Routing Guidelines*
- Texas Instruments: *Sitara Processor Power Distribution Networks: Implementation and Analysis*

14 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2023) to Revision A (January 2025)	Page
• Added AM62Dx Support to document	2
• Removed reference to DDR4 as unsupported	6

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