User's Guide

SK-TDA4VM User's Guide

ABSTRACT

This document provides the SK-TDA4VM capabilities and interface details.

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Trademarks

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1 Introduction

1.1 Inside the Box

The SK-TDA4VM kit includes:

- SK-TDA4VM
- Micro-SD Card
- USB Cable (Type-A to Micro-B) for serial terminal/logging
- Paper Card with Start-up Link/Support Information

The EVM is powered from a Type-C power supply, but is NOT INCLUDED. For more information on the types of supplies recommended with the EVM, see Table 2-1.

1.2 Key Features and Interfaces

- Processor
  - Texas Instruments Jacinto TDA4VM
- Optimized Power Management Solution
  - Dynamic Voltage Scaling
  - Multiple Clock and Power Domains
- Memory
  - 4GByte LPDDR4 DRAM (2133 MHz)
  - 512 Mb Non-Volatile Flash, Octal-SPI NOR
  - Multimedia Card (MMC)/Secure Digital Card (Micro SD) Cage, UHS-I
- USB
  - USB3.1 (Gen1) Hub to 3x Type A (Host)
  - USB3.1 (Gen1) Type C (DFP and UFP modes)
  - USB2.0 Micro B (for Quad UART-over-USB Transceiver)
- Display
  - VESA Display Port (v1.4), supports 4K UHD with MST support
  - DVI (v1.0) via HDMI Type A, supports 1080p
- Wired Network
  - Gigabit Ethernet (RJ45 Connector)
  - 4x CAN-FD Headers (1x3)
- Camera Interfaces
  - 2x 15-Pin Flex Cable Interface (CSI-2L)
  - 40-pin High Speed Connector (dual CSI-4L, I2C, GPIO, and so forth)
- Expansion/Add-on
  - M.2 Key E Interface (PCIe/Gen3 x 1 Lane, USB2.0, SDIO, I2S, UART, I2C)
  - M.2 Key M Interface (PCIe/Gen3 x 2 Lane)
  - 40-pin Header (2x20) (I2C, SPI, UART, I2S, GPIO, PWM, and so forth)
  - Fan Header (5V)
- User Control/Indication
  - Pushbuttons (Reset, Power/User Defined)
  - LEDs (Power, User Defined, Serial Port)
  - User Configuration (Boot Mode, USB Mode)
  - External JTAG/Emulator Support (20-pin Header)
- REACH and RoHS Compliant
- EMI/EMC Radiation Compliant

1.3 Thermal Compliance

There is elevated heat on the processor/heatsink, use caution particularly at elevated ambient temperatures! Although the processor/heatsink is not a burn hazard, caution should be used when handling the EVM due to increased heat in the area of the heatsink

	Caution	Caution Hot surface. Contact may cause burns. Do not touch!

1.4 EMC, EMI, and ESD Compliance

Components installed on the product are sensitive to Electrostatic Discharge (ESD). It is recommended this product be used in an ESD controlled environment. This may include a temperature and/or humidity controlled environment to limit the buildup of ESD. It is also recommended to use ESD protection such as wrist straps and ESD mats when interfacing with the product.

The product is used in the basic electromagnetic environment as in laboratory condition and the applied standard will be as per EN IEC 61326-1:2021.

2 User Interfaces

Figure 2-1 and Figure 2-2 identify the key user interfaces on the EVM (top and bottom view)

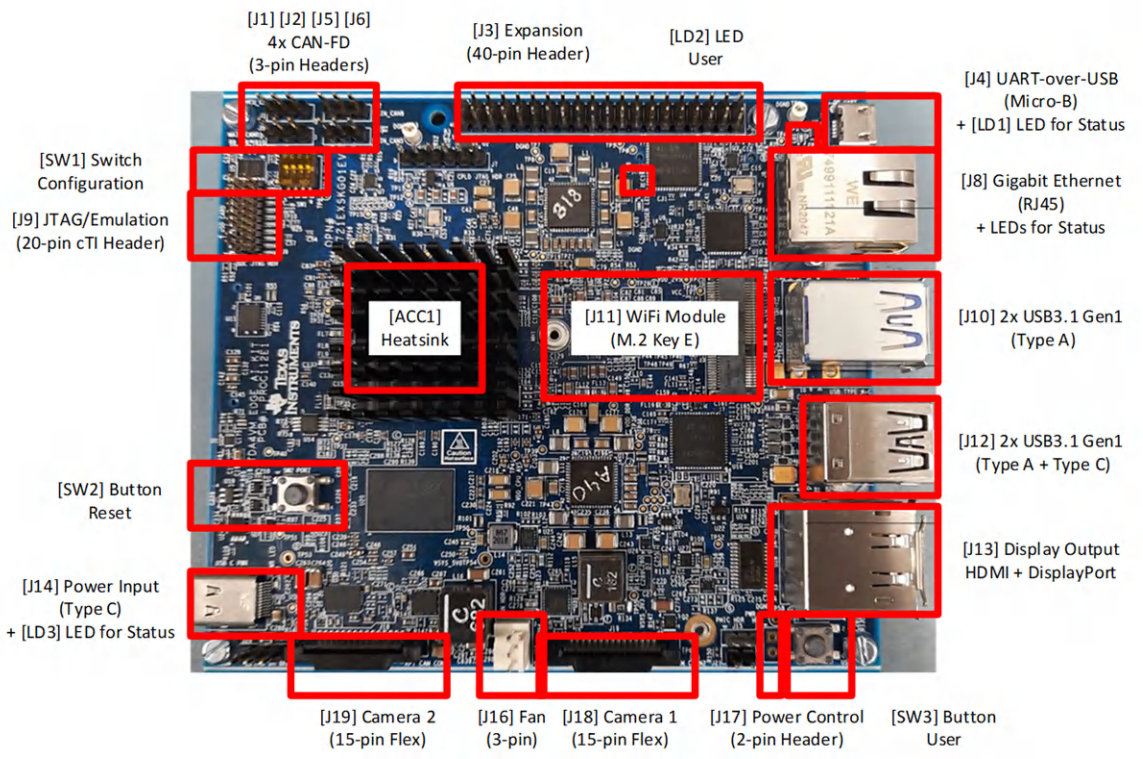

Figure 2-1. User Interfaces (Top)

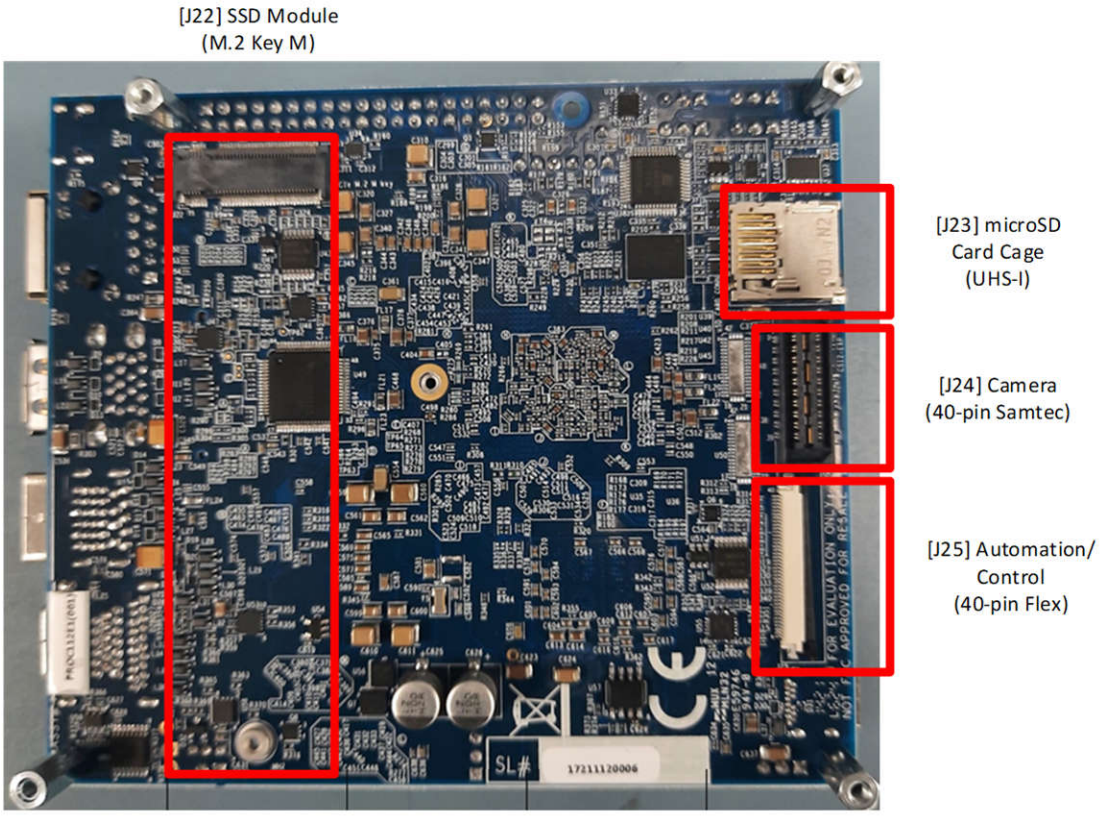

Figure 2-2. User Interfaces (Bottom)

2.1 Power Input

A power supply is not included with the EVM and must be purchased separately.

External Power Supply or Power Accessory Requirements:

- Nominal Output Voltage: 5-20VDC
- Maximum Output Current: 5000 mA
- Efficiency Level V

Note

TI recommends using an external power supply or power accessory that complies with applicable regional safety standards such as (by example) UL, CSA, VDE, CCC, PSE, and so forth.

2.1.1 Power Input [J14] With LED for Status [LD3]

The dedicated power input connector is a USB Type C connector [J14] with Power Delivery 3.0 support. The input can accept wide range of input voltages (5V to 20V). The exact power required for the EVM is largely dependent on the application and the connected peripherals. The recommended supplies are listed in Table 2-1. These supplies are 20V Type C supplies capable of supplying up to 60W of power (20VDC at 3A). The minimum supply required is 15W supply (5VDC at 3A). However, a 5V supply may limit available processing with TDA4VM as well as limit some of the available peripherals. USB peripherals require VBUS and depending on their power needs, may have too much voltage drop from a 5V input supply. This is a reason higher voltage supply is recommended.

There are many USB Type C power supply manufactures and models available in the market, and it is not possible to test the EVM with every combination.

Table 2-1 lists a few recommended supplies the EVM has tested.

Table 2-1. Recommended External Power Supply

Manufacturer	Part #	Digikey #
GlobTek, Inc.	TR9CZ3000USBCG2R6BF2	1939-1794-ND
Qualtek	QADC-65-20-08CB	Q1251-ND

The EVM is designed to power up automatically upon insertion of power. A red power led [LD3] will be illuminated when a valid power source is connected.

2.1.2 Power Budget Considerations

The exact power required for the EVM is largely dependent on the application, usage of the on-board peripherals, and power needs of add-on devices. Table 2-2 shows the designs power allocations. (Again, the input supply must be capable of supplying the power needs for your application.)

Table 2-2. Power Supply Allocation

Function	Power	Description
Processor Core	Up to 15W	Processor, Memory
On-board Peripherals	Up to 3W	SD Card, Ethernet, Logic, and so forth
USB Port(s)	Up to 19W	USB Hub Type A Ports (2.8A at 5V) Type C Ports (0.9A at 5V)
Camera Ports	Up to 2W	Cam Ports (0.5A at 3.3V)
Expansion Interface(s)	Up to 20W	M.2 Type E (1A at 3.3V) M2 Type M (1A at 3.3V) 40p Expansion (2A at 3.3V, 1.5A at 4V)
Display(s)	Up to 3W	HDMI Transceiver HDMI Panel (55mA at 5V) DP Panel (0.5A at 3.3V)

2.2 User Inputs

The EVM supports several mechanisms for the user to configure, control, and provide input to the system.

2.2.1 Board Configuration Settings [SW1]

Dip Switch [SW1] is used to configure different options available on the EVM, including processor boot mode and USB mode for the Type C interface.

Table 2-3. Processor Boot Mode Settings [SW1 Switch 1-3]

TDA4VM Boot Source	SW1.1	SW1.2	SW1.3
MicroSD Card [J23]	OFF	OFF	OFF
Non-Volatile Flash (xSPI)	OFF	OFF	ON
USB3.1 Type A [J10][J12]	ON	ON	OFF
USB Type C (DFP) [J12] (1)	OFF	ON	OFF
M.2 Key M [J22]	OFF	ON	ON
UART (for Flashing)	ON	OFF	ON
No Boot (JTAG/Emulator)	ON	OFF	OFF

(1) For USB booting from Type C, requires mode be set to DFP.

Table 2-4. USB Type C Mode Setting [SW1 Switch 4]

USB3.1 Type C Mode	SW1.4
Downstream Facing Peripheral (DFP)	OFF
Upstream Facing Peripheral (UFP)	ON

2.2.2 Reset Pushbutton [SW2]

When pressed [SW2], the EVM is issued a Power-On (Cold) Reset, and is held in reset until the button is released.

2.2.3 User Pushbutton [SW3] With User LED Indication [LD2]

The pushbutton [SW3] can be used for several different functions.

Function 1: System Wake from Shutdown. After software-initiated power down (using GPIO0_55), pressing pushbutton [SW3] will re-enable and boot the EVM.

Function 2: Power Management Input/Interrupt. The pushbutton [SW3] is connected with Power Management IC (IO4), and can be programmed for different power related functions (ex. Wake from Sleep).

Function 3: User Defined Input/Interrupt. The pushbutton [SW3] is connected with the TDA4VM processor (GPIO0_4), and can be programmed for variety of user input/interrupt needs.

A red LED [LD2] is available as user indicator, and is controlled via the TDA4VM processor (GPIO0_64)

2.3 Standard Interfaces

The EVM provides industry standard interfaces/connectors to connect a wide variety of peripherals. As these interfaces are standard, specific pin information is not provided in this document.

2.3.1 Uart-Over-USB [J4] With LED for Status [LD1]

Four UART ports of the TDA4VM are interfaced with UART-over-USB transceiver. When the EVM's USB micro-B connector (J4) is connected to a Host-PC using supplied USB cable (Type-A to Micro-B), the computer can establish Virtual Com Port(s) which can be used with any terminal emulation application. Virtual Com Port drivers for the transceiver (CP2108-B02-GM) can be obtained from https://www.silabs.com/developers/usb-to-uart-bridge-vcp-drivers.

Once installed, the Host-PC will create four Virtual Com Ports. Depending on the other Host-PC resources available - the Virtual COM Ports not be located at COM1-4. However, they will remain in the same numerical order.

Table 2-5. UART to COM Port Mapping

TDA4VM UART	Host-PC COM Port
WKUP_UART0	COM 1
MCU_UART0	COM 2
UART0	COM 3
UART1	COM 4

The circuit is powered through BUS power and therefore the COM connection not be lost when the EVM power is removed. An LED [LD1] is used to indicate an active COM connection with Host-PC.

2.3.2 Gigabit Ethernet [J8] With Integrated LEDs for Status

A wired Ethernet network is supported via RJ45 cable interface [J8], and is compatible with IEEE 802.3 10BASE-Te, 100BASE-TX, and 1000BASE-T specifications. The connector includes status indicators for link and activity.

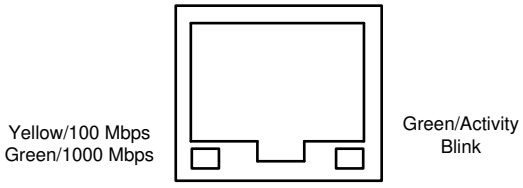

Figure 2-3. RJ45 LED Indicators [J8]

Power-Over-Ethernet (PoE) is not supported.

2.3.3 JTAG/Emulation Interface [J9]

The EVM supports JTAG emulation/debugger through a dedicated emulation connector [J9]. The connector is aligned with the Texas Instrument 20-pin CTI header standard (2x20, 1.27mm pitch), and is compatible with Texas Instruments modules (XDS110, XDS200, XDS560v2) and 3rd party modules.

Table 2-6. Expansion Header Pin Definition [J3]

Pin #	Pin Name	Description (TDA4VM Pin #)	Dir
1	TMS	Test Mode Select (TMS)	Input
2	TRSTn	Test Reset	Input
3	TDI	Test Data Input	Input
4	TDIS	Target Disconnect	Output
5	Vref	Target Voltage Detect, 3.3V	Output
6	<No Pin>	No Pin/Key	
7	TDO	Test Data Output	Output
8	GND	Ground	
9	RTCK	Test Clock Return	Output
10	GND	Ground	
11	TCK	Test Clock	Input
12	GND	Ground	
13	EMU0	Emulation Pin 0	Bi-Dir
14	EMU1	Emulation Pin 1	Bi-Dir
15	RESETz	Target Reset	Input
16	GND	Ground	
17		Open	
18		Open	
19		Open	
20	GND	Ground	

Note

In the DIR column, output is to the JTAG module, input is from the JTAG module. Bi-Dir signals can be configured as either input or output.

2.3.4 USB3.1 Gen1 Interfaces [J10] [J12]

The EVM supports three USB3.1 Gen1 Type A ports [J10][J12], which operate in Host mode. The combined VBUS output for these ports is limited to 2.8A.

Also supported is one USB3.1 Gen1 Type C interface [J12], which can function as either a DFP or UFP. For details on how to select USB mode, see Section 2.2.1. The VBUS output for this port is limited to 0.9A. When operating as UFP, the EVM cannot be powered from this port.

Note

The USB2.0 Micro-B connector [J4] is discussed in Uart-over-USB section.

Note

The VBUS power output capability assumes the selected input supply is capable of supply power for both EVM and connected peripherals.

Note

An example optional add-on USB Camera module for this interface is the Logitech USB C270.

Note

The maximum length for the IO cables are required to be less than 3 meters.

2.3.5 M.2 Key E Connector [J11] for Wi-Fi Networking Modules

The EVM supports a Mini-PCIe M.2, Key E slot (2230) for expansion modules [J11]. This expansion interface is primarily used for BT/Wi-Fi modules, and supports the following interfaces: PCI Express (PCIe) (1x), USB2.0, secure data/secure digital IO (SDIO), universal asynchronous receiver/transmitter (UART), inter-IC sound (I2S), and inter-integrated circuit (I2C).

Note

An example optional add-on Wireless Network module for this interface is the Intel M.2 Type E Wi-Fi/ 9260NGW.

2.3.6 Stacked DisplayPort and HDMI Type A [J13]

The EVM supports DisplayPort panel via standard DP cable interface [J13]. The interface supports resolutions to 4K UHD (3840x2160) including MST (Mutli-Stream Transport) for supporting multiple panels. A second display interface is supported via HDMI connector [J13], and supports resolutions up to 1080p (1920x1080). The interface is DVI, and therefor does not support the integrated audio. Both DisplayPort and HDMI interfaces can be used simultaneous.

2.3.7 M.2 Key M Connector [J22] for SSD Modules

The EVM supports a Mini-PCIe M.2, Key M slot (2280) for expansion modules [J22]. This expansion interface is primarily used for Solid State Drives (SSD), and supports the following interfaces: PCIe (2x) and I2C.

2.3.8 MicroSD Card Cage [J23]

The EVM supports a micro-SD card cage. It supports UHS-1 class memory cards, including SDHC and SXDC. The connector is a PUSH-PUSH connector, meaning you push to insert the card and push again to remove the card.

A MicroSD Card is included with the EVM kit.

2.4 Expansion Interfaces

The EVM supports expansion interfaces that have non-standard/custom pinouts. Each of those interfaces are introduced and specific pin information is provided.

2.4.1 Heatsink [ACC1] With [J16] Fan Header

The heatsink supports cooling of the device at ambient temperatures. If your environment or use case requires additional cooling, a fan can be added to the Heatsink.

The fan connector is a 3-pin header (WURTH ELEKTRONIK, Part number 61900311121).

Table 2-7. Fan Header Pin Definition [J16]

Pin #	Pin Name	Description	Direction
1	<open>	Unconnected	n/a
2	5V	Main 5V Supply	Output
3	GND	Ground	

2.4.2 CAN-FD Connector(s) [J1] [J2] [J5] [J6]

The EVM supports four (4x) CAN Bus interfaces.

Table 2-8. CAN-FD Interface Assignment

Connector Ref	TDA4VM Resource
J1	MCU CAN0
J2	CAN9
J5	CAN0
J6	CAN5

Each Controller Area Network (CAN) Bus interface is supported on a 3-pin, 2.54 mm pitch header. The interface meets ISO 11898-2 and ISO 11898-5 physical standards, and supports CAN and optimized CAN-FD performance up to 8 Mbps. Each includes CAN Bus end-point termination. If the EVM is included in a network with more than two nodes, the termination my need to be adjusted.

Table 2-9. CAN-FD Header Pin Definition [J1][J2][J5][J6]

Pin #	Pin Name	Description	Direction
1	CAN-H	High-Level CAN Bus Line	Bi-Dir
2	GND	Ground	
3	CAN-L	Low-Level CAN Bus Line	Bi-Dir

2.4.3 Expansion Header [J3]

The EVM includes a 40-pin (2x20, 2.54mm pitch) expansion interface [J3]. The expansion connector supports variety of interfaces including: I2C, serial peripheral interface (SPI), I2S with Audio clock, UART, pulse width modulator (PWM), and GPIO. All signals on the interfaces are 3.3V levels.

Table 2-10. Expansion Header Pin Definition [J3]

Pin #	Pin Name	Description (TDA4VM Pin #)	Dir
1	Power	Power, 3.3V	Output
2	Power	Power, 5.0V	Output
3	I2C_SDA	I2C Bus #5, Data (AA27)	Bi-Dir
4	Power	Power, 5.0V	Output
5	I2C_SCL	I2C Bus #5, Clock (Y26)	Bi-Dir
6	GND	Ground	
7	GP_CLK/GPIO	REFCLK0/GPIO0 #7 (AD22)	Bi-Dir
8	UART_TXD	UART #2 Transmit (AA24)	Output
9	GND	Ground	
10	UART_RXD	UART #2 Receive (AA26)	Input
11	GPIO	GPIO0 #71 (AA28)	Bi-Dir
12	I2S_SCLK	McASP #6 ACLKX (AC23)	Bi-Dir
13	GPIO	GPIO0 #82 (AA29)	Bi-Dir
14	GND	Ground	
15	GPIO	GPIO0 #11 (AD21)	Bi-Dir
16	GPIO	GPIO0 #5 (AH23)	Bi-Dir
17	Power	Power, 3.3V	Output
18	GPIO	GPIO1 #12 (U3)	Bi-Dir
19	SPI_MOSI	SPI #5 Data 0 (V25)	Bi-Dir
20	GND	Ground	
21	SPI_MISO	SPI #5 Data 1 (W24)	Bi-Dir
22	GPIO	GPIO0 #8 (AE20)	Bi-Dir
23	SPI_SCLK	SPI #5 Clock (W29)	Bi-Dir

Table 2-10. Expansion Header Pin Definition [J3] (continued)

Pin #	Pin Name	Description (TDA4VM Pin #)	Dir
24	SPI_CS0	SPI #5 Chip Select 0 (W27)	Bi-Dir
25	GND	Ground	
26	SPI_CS1	SPI #5 Chip Select 1 (W25)	Bi-Dir
27	ID_SDA	Wkup I2C Data (H24)	Bi-Dir
28	ID_SCL	Wkup I2C Clock (J25)	Bi-Dir
29	GPIO	GPIO0 #93 (U27)	Bi-Dir
30	GND	Ground	
31	GPIO	GPIO0 #94 (U24)	Bi-Dir
32	PWM0	PWM3_A (V23)	Output
33	PWM1	PWM3_B (W23)	Output
34	GND	Ground	
35	I2S_FS	McASP #6 FSX (AG22)	Bi-Dir
36	GPIO	GPIO0_97 (Y28)	Bi-Dir
37	GPIO	GPIO0_115 (AA3)	Bi-Dir
38	I2S_DIN	McASP #6 (AF22)	Bi-Dir
39	GND	Ground	
40	I2S_DOUT	McASP #6 (AJ23)	Bi-Dir

Note

In the DIR column, output is to the expansion module, input is from the expansion module. Bi-Dir signals can be configured as either input or output.

Note

All the signals on the Expansion connector can support other functions including GPIO. For full list of functions available on each pin, see the *TDA4VM Jacinto™ Processors for ADAS and Autonomous Vehicles Silicon Revisions 1.0 and 1.1*. Functions like UART and PWM set as INPUT or OUTPUT can be Bi-Dir when configured as GPIO.

2.4.4 Camera Interface, 15-Pin Flex Connectors [J18] [J19]

The EVM supports two (2) 15-pin flex (1.0mm pitch) connectors [J18][J19] for interfacing with camera modules. Each camera interface provides MIPI CSI-2 interface (2Lane), Clock/Control signals, and power (3.3V) to the camera.

To enable camera modules with same addressing to be used simultaneously, I2C mux is used to select each camera. The voltage level for Clock/Control signals is selectable between 1.8V/3.3V.

Table 2-11. Camera 1 Flex Pin Definition [J18]

Pin #	Pin Name	Description	Dir
1 / 1A	GND	Ground	
3 / 2A	CSI0_D0_N	CSI Port 0 Data Lane 0	Input
5 / 3A	CSI0_D0_P	CSI Port 0 Data Lane 0	Input
7 / 4A	GND	Ground	
9 / 5A	CSI0_D1_N	CSI Port 0 Data Lane 1	Input
11 / 6A	CSI0_D1_P	CSI Port 0 Data Lane 1	Input
13 / 7A	GND	Ground	
15 / 8A	CSI0_CLK_N	CSI Port 0 CLK	Input
17 / 9A	CSI0_CLK_P	CSI Port 0 CLK	Input
19 / 10A	GND	Ground	
21 / 11A	CAM1_PWDN	Pwr-Dwn (GPIO0-116)	Output

Table 2-11. Camera 1 Flex Pin Definition [J18] (continued)

Pin #	Pin Name	Description	Dir
23 / 12A	CAM1_AUX	AUX (GPIO0-117)	Bi-Dir
25 / 13A	I2C_SCL	I2C Clock #3, Mux 0	Output
27 / 14A	I2C_SDA	I2C Data # 3, Mux 0	Bi-Dir
29 / 15A	Power	Power, 3.3V	Output

Table 2-12. Camera 2 Flex Pin Definition [J19]

Pin #	Pin Name	Description	Dir
1 / 1A	GND	Ground	
3 / 2A	CSI1_D0_N	CSI Port 1 Data Lane 0	Input
5 / 3A	CSI1_D0_P	CSI Port 1 Data Lane 0	Input
7 / 4A	GND	Ground	
9 / 5A	CSI1_D1_N	CSI Port 1 Data Lane 1	Input
11 / 6A	CSI1_D1_P	CSI Port 1 Data Lane 1	Input
13 / 7A	GND	Ground	
15 / 8A	CSI1_CLK_N	CSI Port 1 CLK	Input
17 / 9A	CSI1_CLK_P	CSI Port 1 CLK	Input
19 / 10A	GND	Ground	
21 / 11A	CAM2_PWDN	Pwr-Dwn (GPIO0-119)	Output
23 / 12A	CAM2_AUX	AUX (GPIO0-120)	Bi-Dir
25 / 13A	I2C_SCL	I2C Clock #3, Mux 1	Output
27 / 14A	I2C_SDA	I2C Data # 3, Mux 1	Bi-Dir
29 / 15A	Power	Power, 3.3V	Output

Note

In the DIR/Level column, output is to the camera module, input is from the camera module. Bi-Dir signals can be configured as either input or output.

2.4.5 Camera Interface, 40-Pin High Speed [J24]

The EVM includes a 40-pin (2x20, 2.54 mm pitch) high speed camera interface [J24]. The expansion connector supports two CSI-2 (4 Lanes each), power, and control signals (I2C, GPIO, and so forth): All control signals are configurable for 3.3V or 1.8V voltage levels.

Table 2-13. Camera IO Voltage Control

GPIO0 #118 (Pin Y1)	Camera IO Level
Low or ‘0’	1.8V (Default)
High or ‘1’	3.3V

Table 2-14. 40-Pin High-Speed Camera Expansion Pin Definition [J24]

Pin #	Pin Name	Description (TDA4VM Pin #)	Dir
1	Power		Output
2	I2C_SCL	I2C Bus #3, Clock (T26)	Bi-Dir
3	Power		Output
4	I2C_SDA	I2C Bus #3, Data (T25)	Bi-Dir
5	CSI0_CLK_P	CSI Port 0 Clock	Input
6	GPIO/PWMA	GPIO0 #74 (AG26)	Bi-Dir
7	CSI0_CLK_N	CSI Port 0 Clock	Input
8	GPIO/PWMB	GPIO0 #75 (AF27)	Bi-Dir
9	CSI0_D0_P	CSI Port 0 Data Lane 0	Input
10	REFCLK	REFCLK2 (W26)	Bi-Dir

Table 2-14. 40-Pin High-Speed Camera Expansion Pin Definition [J24] (continued)

Pin #	Pin Name	Description (TDA4VM Pin #)	Dir
11	CSI0_D0_N	CSI Port 0 Data Lane 0	Input
12	GND	Ground	
13	CSI0_D1_P	CSI Port 0 Data Lane 1	Input
14	RESETz	GPIO0 #79 (AG29)	Output
15	CSI0_D1_N	CSI Port 0 Data Lane 1	Input
16	GND	Ground	
17	CSI0_D2_P	CSI Port 0 Data Lane 2	Input
18	GPIO	GPIO0 #76 (AF26)	Bi-Dir
19	CSI0_D2_N	CSI Port 0 Data Lane 2	Input
20	GPIO	GPIO0 #77 (AE25)	Bi-Dir
21	CSI0_D3_P	CSI Port 0 Data Lane 3	Input
22	GPIO	GPIO0 #78 (AF29)	Bi-Dir
23	CSI0_D3_N	CSI Port 0 Data Lane 3	Input
24	GND	Ground	
25	CSI1_CLK_P	CSI Port 1 Clock	Input
26	CSI1_D3_P	CSI Port 1 Data Lane 3	Input
27	CSI1_CLK_N	CSI Port 1 Clock	Input
28	CSI1_D3_N	CSI Port 1 Data Lane 3	Input
29	CSI1_D0_P	CSI Port 1 Data Lane 0	Input
30	Power	Power, 3.3V	Output
31	CSI1_D0_N	CSI Port 1 Data Lane 0	Input
32	Power	Power, 3.3V	Output
33	CSI1_D1_P	CSI Port 1 Data Lane 1	Input
34	Power	Power, 3.3V	Output
35	CSI1_D1_N	CSI Port 1 Data Lane 1	Input
36	Power	Power, 3.3V	Output
37	CSI1_D2_P	CSI Port 1 Data Lane 2	Input
38	Power	Power, IO Level (1.8 or 3.3V)	Output
39	CSI1_D2_N	CSI Port 1 Data Lane 2	Input
40	Power	Power, IO Level (1.8 or 3.3V)	Output

Note

In the DIR column, output is to the expansion module, input is from the expansion module. Bi-Dir signals can be configured as either input or output.

2.4.6 Automation and Control Connector [J25]

The EVM supports an interface to allow for automated control of the system, including functions like on/off, reset, and boot mode settings.

Table 2-15. Test Automation Interface Pin Definition [J25]

Pin	Pin Name	Description (TDA4VM Pin #)	Dir
1	Power	Power, 3.3V	Output
2	Power	Power, 3.3V	Output
3	Power	Power, 3.3V	Output
4	<open>		N/A
5	<open>		N/A
6	<open>		N/A

Table 2-15. Test Automation Interface Pin Definition [J25] (continued)

Pin	Pin Name	Description (TDA4VM Pin #)	Dir
7	GND	Ground	
8	<open>		N/A
9	<open>		N/A
10	<open>		N/A
11	<open>		N/A
12	<open>		N/A
13	<open>		N/A
14	<open>		N/A
15	<open>		N/A
16	GND	Ground	
17	<open>		N/A
18	<open>		N/A
19	<open>		N/A
20	<open>		N/A
21	<open>		N/A
22	<open>		N/A
23	<open>		N/A
24	<open>		N/A
25	GND	Ground	
26	POWERDOWNz	EVM Power Down	Input
27	PORz	EVM Power-On/Cold Reset	Input
28	RESETz	EVM Warm Reset	Input
29	<open>		N/A
30	INT1z	EXTINTN (AC18)	Input
31	INT2z	WKUP_GPIO0 #5 (F29)	Bi-Dir
32	<open>		N/A
33	BOOTMODE_RSTz	Bootmode Buffer Reset	Input
34	GND	Ground	
35	<open>		N/A
36	I2C_SCL	I2C Bus #2, Clock (AA1)	Bi-Dir
37	BOOTMODE_SCL	Bootmode Buffer I2C Clock	Input
38	I2C_SDA	I2C Bus #2, Data (AA3)	Bi-Dir
39	BOOTMODE_SDA	Bootmode Buffer I2C Data	Bi-Dir
40	GND	Ground	
41	GND	Ground	
42	GND	Ground	

Note

In the DIR/Level column, output is to the camera module, input is from the camera module. Bi-Dir signals can be configured as either input or output.

Note

The signal polarity is identified with a trailing 'z' in the Pin Name, which indicates the signal is active LOW. For example, POWERDOWNz is an active low signal, meaning '0' = EVM is Powered Down, '1' = EVM is NOT Powered Down.

3 Mechanicals

This section has yet to be completed.

4 Circuit Details

This sections provides additional details on the EVM design and processor connections.

4.1 Top Level Diagram

Figure 4-1 shows the functional block diagram of the EVM Board.

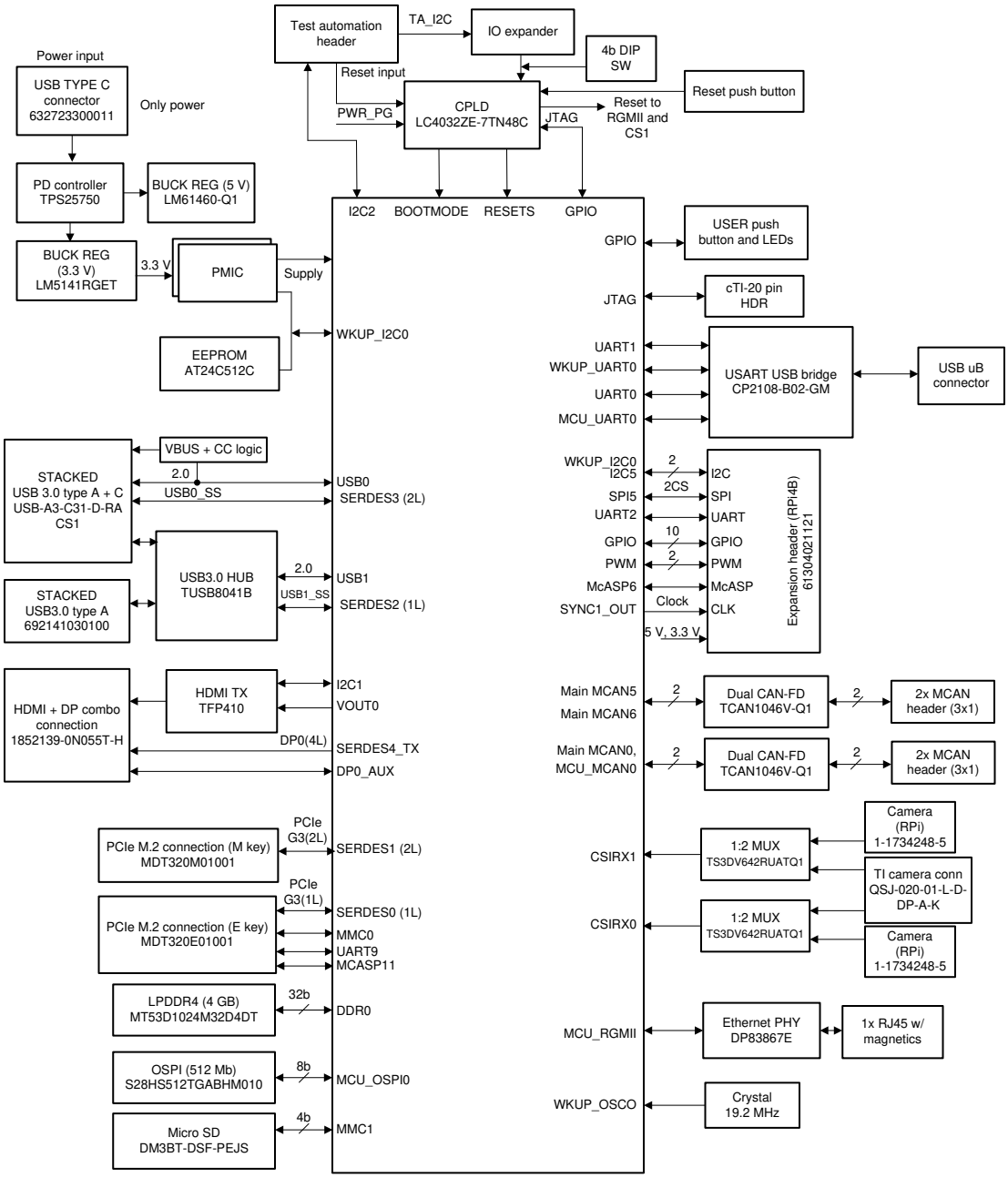

Figure 4-1. SK-TDA4VM Functional Block Diagram

4.2 Interface Mapping

The TDA4VM Interface Mapping table is provided in Table 4-1.

Table 4-1. Interface Mapping Table

Connected Peripheral	TDA4VM Resources	Components / Part Numbers
Memory, LPDDR4 DRAM	DDR0	Micron MT53D1024M32D4DT
Memory, xSPI NOR Flash	MCU_OSPI0	Cypress S28HS512TGABHM010
Micro-SD Card Cage	MMC1	
EEPROM, Board Identification	WKUP_I2C0	Microchip Tech AT24C512C
Wired Ethernet	MCU_RGMII1, MCU_MDIO	Texas Instruments DP83867E
USB Type C + CC Controller	USB0 (SERDES3)	Texas Instruments TUSB321
USB Type A (3x)	USB1 (SERDES2)	Texas Instruments TUSB8041
HDMI	DPI0, I2C1	Texas Instruments TFP410
Display Port	DP0 (SERDES4)	
PCIe – M.2 Socket (E-Key 2230)	PCIe0 (SERDES0), USB1, MMC0, McASP11, UART9, I2C0	
PCIe – M.2 Socket (M-Key 2280)	PCIe1 (SERDES1), I2C0	
CSI Rx Interface	CSI0, CSI1, I2C3	
UART Terminal (UART-to-USB)	WKUP_UART0, MCU_UART0, UART0, UART1	Silicon Labs CP2108
CAN (4x)	MCU_MCAN0, MCAN0, MCAN5, MCAN9	Texas Instruments TCAN1046V
Expansion Header (40-pin)	McASP6, SPI5, UART2, I2C5	
Test Automation Header	I2C2	

4.3 I2C Address Mapping

Table 4-2 provides the complete I2C address mapping details for the EVM.

Table 4-2. I2C Mapping Table

Connected Peripheral	TDA4VM Resources		Components / Part Numbers
	I2C Port	I2C Address	
Power Management IC	WKUP_I2C0	0x48-4B	Texas Instruments PTPS65941213
Power Management IC	WKUP_I2C0	0x4C-4F	Texas Instruments PTPS65941111
EEPROM, Board Id	WKUP_I2C0	0x51	Microchip Tech AT24C512C
Expansion Header (40p)	WKUP_I2C0	Add-on	
Power Management IC	MCU_I2C0	0x12	Texas Instruments PTPS65941213
Input PD Controller	I2C0	0x20	Texas Instruments TPS25750
PCIe M.2 Key E/M	I2C0	0x71, Add-on	Texas Instruments TCA9543A
HDMI DDC	I2C1	Add-on	
Camera Expansion	I2C3	0x70, Add-on	Texas Instruments TCA9543A
Expansion Header (40p)	I2C5	Add-On	

4.4 GPIO Mapping

The General Purpose IOs (GPIO) of TDA4VM SoC are broken into two major groups, WKUP and MAIN. For this design, there is not much functional difference between the IOs. Table 4-3 describes the GPIO mapping of TDA4VM SoC with the EVM peripherals and provides the default settings.

Table 4-3. GPIO Mapping Table

TDA4VM Pin Name	GPIO	Function	Dir/Level	Remarks
WKUP_GPIO0_3	WKUP_GPIO0_3	MCU CAN Bus #0 Stand-by	Output	'0' – Normal Mode '1' – Standby Mode (default)
WKUP_GPIO0_4	WKUP_GPIO0_4	SW3 Pushbutton	Input	'0' – SW3 is Pressed '1' – SW2 is NOT Pressed (default)
WKUP_GPIO0_5	WKUP_GPIO0_5	EEPROM Write Protect	Output	'0' – EEPROM is NOT Write Protected (default) '1' – EEPROM is Write Protected
WKUP_GPIO0_6	WKUP_GPIO0_6	Test Automation Interrupt #2	Input	'0' - To Be Defined by User '1' - To Be Defined by User (default)
WKUP_GPIO0_7	WKUP_GPIO0_7	Power Management IC Interrupt	Input	'0' – Active Interrupt Request '1' – No Interrupt Request (default)
WKUP_GPIO0_8	WKUP_GPIO0_8	SD Card Power Enable	Output	'0' – SD Card Power Disabled '1' – SD Card Power Enable (default)
WKUP_GPIO0_9	WKUP_GPIO0_9	SD Card IO Voltage Selection	Output	'0' – SD Card IO Voltage is 1.8V '1' – SD Card IO Voltage is 3.3V (default)
WKUP_GPIO0_10	WKUP_GPIO0_10	Ethernet PHY Reset	Output	'0' – Ethernet is Reset '1' – Ethernet is NOT Reset (default)
WKUP_GPIO0_11	WKUP_GPIO0_11	M.2 Key M Interface Signal (RSTz)	Output	RSTz, See M.2 Key M specification for more details. (Default = '0')
MCU_OSPI1_DQS	WKUP_GPIO0_31	Flash Memory Interrupt	Input	'0' – Active Interrupt Request '1' – No Interrupt Request (default)
MCU_OSPI1_CSN0	WKUP_GPIO0_36	M.2 Key E Interface Signal (SDIO_RESET#)	Output	SDIO_RESET#, See M.2 Key E specification for more details. (Default = '0')
MCU_OSPI1_CSN1	WKUP_GPIO0_37	M.2 Key E Interface Signal (SDIO_WAKE#)	Output	SDIO_WAKE#, See M.2 Key E specification for more details. (Default = '1')
MCU_SPI0_CS0	WKUP_GPIO0_55	System Power Down	Output	'0' - Normal Operation (default) '1' - System Power Down/Off
PMIC_POWER_EN0	WKUP_GPIO0_66	Ethernet PHY Interrupt	Input	'0' – Active Interrupt Request '1' – No Interrupt Request (default)
PRG1_PRU0_GPO4	GPIO0_5	40-pin Expansion Header Signal (GPIO)	Bi-Dir	Expansion Board Specific (Pin 16)
PRG1_PRU0_GPO6	GPIO0_7	40-pin Expansion Header Signal (REFCLK0/GPIO)	Bi-Dir	Expansion Board Specific (Pin 7)
PRG1_PRU0_GPO7	GPIO0_8	40-pin Expansion Header Signal (GPIO)	Bi-Dir	Expansion Board Specific (Pin 22)
PRG1_PRU0_GPO10	GPIO0_11	40-pin Expansion Header Signal (GPIO)	Bi-Dir	Expansion Board Specific (Pin 15)
PRG0_PRU0_GPO18	GPIO0_61	M.2 Key E Interface Signal (W_DISABLE1#)	Output	W_DISABLE1#, See M.2 Key E specification for more details. (Default = '1')
PRG0_PRU0_GPO19	GPIO0_62	M.2 Key E Interface Signal (W_DISABLE2#)	Output	W_DISABLE2#, See M.2 Key E specification for more details. (Default = '1')
PRG0_PRU1_GPO1	GPIO0_64	User LED (LD2)	Output	'0' – LED [LD2] is OFF (default) '1' – LED [LD2] is ON

Table 4-3. GPIO Mapping Table (continued)

TDA4VM Pin Name	GPIO	Function	Dir/Level	Remarks
PRG0_PRU1_GPO2	GPIO0_65	CAN Bus #0 Stand-by	Output	'0' – Normal Mode '1' – Standby Mode (default)
PRG0_PRU1_GPO3	GPIO0_66	CAN Bus #5 Stand-by	Output	'0' – Normal Mode '1' – Standby Mode (default)
PRG0_PRU1_GPO4	GPIO0_67	CAN Bus #9 Stand-by	Output	'0' – Normal Mode '1' – Standby Mode (default)
PRG0_PRU1_GPO8	GPIO0_71	40-pin Expansion Header Signal (GPIO)	Bi-Dir	Expansion Board Specific (Pin 11)
PRG0_PRU1_GPO9	GPIO0_72	M.2 Key E Interface Signal (RTSz)	Output	RSTz, See M.2 Key E specification for more details. (Default = '0')
PRG0_PRU1_GPO11	GPIO0_74	CSI Expansion Signal (GPIO)	Bi-Dir	CSI2 Expansion Board Specific (Pin 6)
PRG0_PRU1_GPO12	GPIO0_75	CSI Expansion Signal (GPIO)	Bi-Dir	CSI2 Expansion Board Specific (Pin 8)
PRG0_PRU1_GPO13	GPIO0_76	CSI Expansion Signal (GPIO)	Bi-Dir	CSI2 Expansion Board Specific (Pin 18)
PRG0_PRU1_GPO14	GPIO0_77	CSI Expansion Signal (GPIO)	Bi-Dir	CSI2 Expansion Board Specific (Pin 20)
PRG0_PRU1_GPO15	GPIO0_78	CSI Expansion Signal (GPIO)	Bi-Dir	CSI2 Expansion Board Specific (Pin 22)
PRG0_PRU1_GPO16	GPIO0_79	CSI Expansion Signal (RESETz)	Output	'0' – CSI Board is Reset (Default) '1' – CSI Board is NOT Reset
PRG0_PRU1_GPO19	GPIO0_82	40-pin Expansion Header Signal (GPIO)	Bi-Dir	Expansion Board Specific (Pin 13)
RGMII5_TX3	GPIO0_87	HDMI Monitor Enable	Output	'0' – Power Down '1' – Normal Operation (default)
RGMII5_TD2	GPIO0_88	CSI Expansion Interface Selection	Output	CSI I2C MUX select '0' – Camera/Flex Selected (default) '1' – 40-pin Camera Expansion Selected
RGMII5_RD3	GPIO0_93	40-pin Expansion Header Signal (GPIO)	Bi-Dir	Expansion Board Specific (Pin 29)
RGMII5_RD2	GPIO0_94	40-pin Expansion Header Signal (GPIO)	Bi-Dir	Expansion Board Specific (Pin 31)
RGMII5_RD1	GPIO0_95	M.2 Key E Interface Signal (UART_WAKE#)	Output	UART_WAKE#, See M.2 Key E specification for more details. (Default = '1')
RGMII6_TX_CTL	GPIO0_97	40-pin Expansion Header Signal (GPIO)	Bi-Dir	Expansion Board Specific (Pin 36)
SPI0_CS0	GPIO0_111	Display Port Monitor Enable	Output	'0' – Monitor is Disabled (default) '1' – Monitor is Enabled
SPI0_D1	GPIO0_115	40-pin Expansion Header Signal (GPIO)	Bi-Dir	Expansion Board Specific (Pin 37)
SPI1_CS0	GPIO0_116	Camera #0 Flex Signal (PwrDwn)	Output	Camera Specific (Pin 11a) '0' – Normal Operation (default) '1' – Power Down
SPI1_CS1	GPIO0_117	Camera #0 Flex Signal (GPIO)	Bi-Dir	Camera Specific (Pin 12a)
SPI1_CLK	GPIO0_118	CSI I2C/GPIO Voltage Selection	Output	'0' – 1.8 V IO (default) '1' – 3.3 V IO
SPI1_D0	GPIO0_119	Camera #1 Flex Signal (PwrDwn)	Output	Camera Specific (Pin 11a) '0' – Normal Operation (default) '1' – Power Down
SPI1_D1	GPIO0_120	Camera #1 Flex Signal (GPIO)	Bi-Dir	Camera Specific (Pin 12a)

Table 4-3. GPIO Mapping Table (continued)

TDA4VM Pin Name	GPIO	Function	Dir/Level	Remarks
UART1_CTSN	GPIO0_127	HDMI Transceiver Enable	Output	'0' – Power Down (default) '1' – Normal Operation
UART1_RTSN	GPIO1_0	HDMI Monitor Detect	Input	'0' – No Monitor Detected (default) '1' – Monitor Detected
MCAN1_RX	GPIO1_3	USB Type C Cable Orientation	Input	'0' – Low Position Detected (default) '1' – High Position Detected
EXT_REFCLK1	GPIO1_12	40-pin Expansion Header Signal (GPIO)	Bi-Dir	Expansion Board Specific (Pin 18)

Note

In the DIR/Level column, output is to the peripheral/module, input is from the peripheral/module. Bi-Dir signals can be configured as either input or output.

4.5 Identification EEPROM

The SK-TDA4VM board identified and revision information are stored in an on-board EEPROM. The first 259 bytes of memory are pre-programmed with EVM identification information. The format of that data is provided in Table 4-4. The remaining 32509 bytes are available for data or code storage.

The EEPROM is accessible from WKUP I2C0 port of TDA4VM processor at address 0x51.

Table 4-4. Board ID Information

Field Name	Offset / Size	Value	Comments
MAGIC	0000 / 4B	0xEE3355AA	Header Identifier
M_TYPE	0004 /1B	0x1	Fixed length and variable position board ID header
M_LENGTH	0005 /2B	0x37	Size of payload
B_TYPE	0007 /1B	0x10	Payload type
B_LENGTH	0008 /2B	0x2E	Offset to next header
B_NAME	000A /16B	J721EX-EAIK	Name of the board
DESIGN_REV	001A /2B	E2	Revision number of the design
PROC_NBR	001C /4B	112	PROC number
VARIANT	0020 /2B	1	Design variant number
PCB_REV	0022 /2B	E2	Revision number of the PCB
SCHBOM_REV	0024 /2B	0	Revision number of the schematic
SWR_REV	0026 /2B	1	First software release number
VENDORID	0028 /2B	1	
BUILD_WK	002A /2B		Week of the year of production
BUILD_YR	002C /2B		Year of production
BOARDID	002E /6B	0	
SERIAL_NBR	0034 /4B		Incrementing board number
DDR_INFO	TYPE	1	
	Length	2	Offset to next header
	DDR control	2	DDR Control Word
MAC_ADDR	TYPE	1	Payload type
	Length	2	Size of payload
	MAC control	2	MAC header control word
	MAC_adrs	192	
END_LIST	TYPE	1	End Marker

5 Usage Notes and Advisories

5.1 Usage Notes

i001: The board can reset during boot and/or normal use.

Details: This can be due to insufficient power supply providing power to the SK (via the Type C connector). Make sure the external supply meets the requirements detailed in Section 2 of this document. If the supply has multiple output options and/or connections, make sure the correct option is selected that enables the input supply to negotiate to the recommended voltage (20V). Operating from a 5V input will likely limit the available processing power and could be a cause of the board resetting under boot/normal conditions.

5.2 Advisories

i002: The processor can reset due to over-heating when operating at higher loading and/or environment with elevated temperatures.

Details: At the time of creating this advisory, the default SDK does not include thermal monitoring/management. When operating the processor at higher loading, the temperature can become elevated and eventually exceed its maximum device temperature causing the processor to reset. The included heatsink does help with thermal dissipation, but additional thermal management may be needed for some applications.

Workaround(s): Adding a fan to the heatsink or increasing air-flow across the SK will help reduce the temperature of the processor and will eliminate the thermal reset condition in most circumstances.

Quantity	Description	Manufacturer	Part Number
1	DC Fan, 5 Volt, 25 mm x 25 mm(1)	CUI Devices	CFM-2510b-0130-275(3)
2	Screw	TBD	TBD
1	Connector Housing, 3 Pos, Female, 2.54 mm(2)	Wurth Elektronik	61900311621
2	Connector Socket, 22-28AWG, Crimp	Wurth Elektronik	61900113722DEC

(1) TBD Fan direction (blow downward or upward)
(2) Attach fan's black wire to housing connector position 2 (middle), red wire to position 3 (away from board edge). Pin 1 is open (board edge)
(3) Manufacture part numbers are included as reference. They can be replaced with compatible components from other manufactures.

i003: The board can reset when using SSD drives and/or higher processor loading.

Details: For Revision A and previous versions only. Version A1 and later revisions have updated design to resolve this item. The power regulator supplying power to the processor and PCIe M.2 slots is under-sized, and some applications can cause the regulator to reset when higher loading occurs. Operating the SK at elevated temperatures can also cause the application to draw additional power also causing the regulator to be over-loaded.

Workaround(s): Keeping the processor/SK at lower temperatures with a fan or other means will reduce the required power. The circuit components can be updated to increase the power capacity of on-board regulator. See below of a list of components to be updated.

Reference	Description	Manufacturer	Part Number
L15	Power Inductor, 1.2uH, 21.6 A, 20%	Coilcraft	XAL7070-122MEC
R134	Resistor, 1m-Ohm, 0.5W, 1206 package	STACKPOLE ELECTRONICS	CSNL1206FT1L00(1)
R123	Resistor, 649-Ohms, 0.1W, 0402 package	PANASONIC-ECG	ERJ-2RKF6490X(1)
C268	Capacitor, Ceramic, 0.047uF, 25V, 0402 package	Murata	GRM155R71E473JA88D(1)
C272	Capacitor, Ceramic, 1000pF, 16V, 0402 package	Kemet	C0402C102M4REC7867(1)

(1) Manufacture part numbers are included as reference. They can be replaced with compatible components from other manufactures.

6 References

- CP210x USB to UART Bridge VCP Drivers
- Texas Instruments: *TDA4VM Jacinto™ Processors for ADAS and Autonomous Vehicles Silicon Revisions 1.0 and 1.1 Data Sheet*

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2021) to Revision B (February 2022)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	2
• Updates were made in Section 1.1	2
• Added new Section 1.4	3

Changes from Revision B (February 2022) to Revision C (October 2022)	Page
• Updated Section 1.4	3
• Added Usage Notes and Advisories sections	19

Changes from Revision C (October 2022) to Revision D (February 2024)	Page
• Updated Section 2.3.4	7

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