EVM User's Guide:
AM263x LaunchPad User Guide

Description

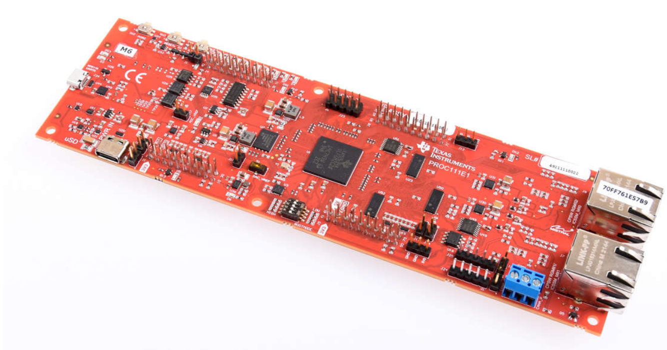
LP-AM263 is a cost-optimized development board for Sitara™ high-performance microcontrollers (MCUs) from the AM263x series. This board is designed for initial evaluation and prototyping as the board provides a standardized and easy-to-use platform to develop your next application.

LP-AM263 is equipped with a Sitara AM2634 processor, along with additional components, allowing the user to make use of various device interfaces, including industrial Ethernet (IE), standard Ethernet, fast serial interface (FSI) and others to easily create prototypes. AM2634 supports a variety of IE protocols, such as EtherCAT, Ethernet/IP and PROFINET®.

This extended LaunchPad™ XL development kit offers additional I/O pins for development and supports connection of up to two BoosterPack™ plug-in modules. LP-AM263 also features an intuitive out-of-box user's guide to quickly start design evaluation.

Features

- AM263x quad-core Arm® Cortex®-R5F MCU
  - 2MB optimized custom static random access memory (OCSRAM)
  - 16MB quad Serial Peripheral Interface (SPI) flash memory, 128-byte Inter-Integrated Circuit (I^2C) electrically erasable programmable read-only memory (EEPROM)
  - 20 analog-to-digital converter (ADC) input channels; one digital-to-analog converter (DAC) output channel
  - 10 enhanced pulse-width modulator (ePWM) output channels, two enhanced quadrature encoder pulse (eQEP), two special frequency-division multiplexing (SFDM), four frequency-shifted interferometry (FSI)
  - Two universal asynchronous receiver transceivers (UARTs), two SPI, two I^2C interfaces
  - Two Reduced Gigabit Media Independent Interface (RGMII), Reduced MII (RMII) and MII industrial Ethernet
  - Two programmable real-time units (PRUs) supporting multiple industrial and automotive network and sensor protocols
- More peripherals supported with AM263x I/O multiplexer (MUX) and onboard MUX options
- Multiple industrial and automotive networking protocols supported through programmable real-time unit (PRU), modular controller area network (MCAN), local interconnect network (LIN), RGMII, RMII and MII interfaces
- microSD card slot for extended storage
- Onboard XDS110 JTAG debugger



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1 Preface: Read This First

1.1 Sitara MCU+ Academy

TI offers the *MCU+ Academy* as a resource for designing with the MCU+ software and tools on supported devices. The MCU+ Academy features easy-to-use training modules that range from the basics of getting started to advanced development topics.

1.2 If You Need Assistance

If you have any feedback or questions, support for the Sitara MCUs and the AM263x LaunchPad development kit is provided by the TI Product Information Center (PIC) and the TI E2E™ Forum. Contact information for the PIC can be found on the TI website. Additional device-specific information can be found in the Reference Documents.

1.3 Important Usage Notes

	Caution	Caution Hot surface. Contact may cause burns. Do not touch!

Note

The AM263x LaunchPad requires a 5 V, 3A power supply in order to function. While a USB type-C cable is included, A 5 V, 3A power supply is not included in the kit and must be ordered separately. The *Belkin USB-C Wall Charger* is known to work with the LaunchPad and supplied type-C cable. For more information on power requirements refer to Power Requirements . If there is an insufficient power input then the red LED (DS1) will glow. For more information on power status LEDs refer to Power Status LEDs.

Note

External Power Supply or Power Accessory Requirements:

- Nominal output voltage: 5VDC
- Max output current: 3000 mA
- Power Delivery

Note

TI recommends using an external power supply or accessory which complies with applicable regional safety standards such as (by example) UL, CSA, VDE,CCC,PSE, etc.

2 Kit Overview

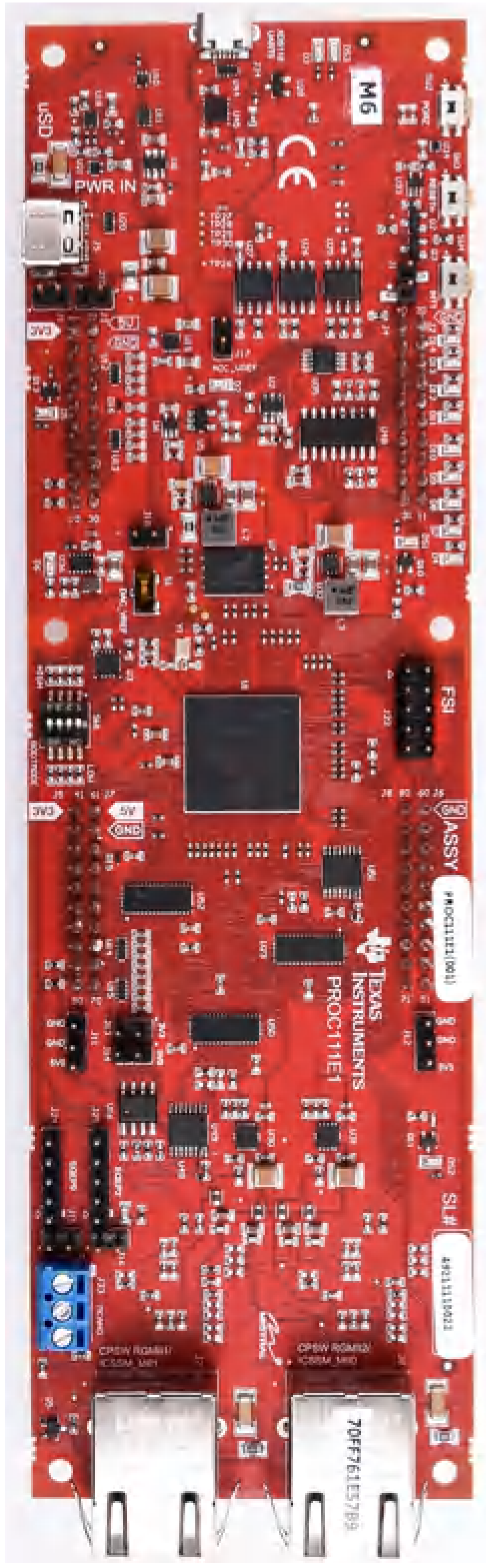

Figure 2-1. AM263x LaunchPad Board

Figure 2-2 Shows the overall top level architecture of the AM263x LaunchPad.

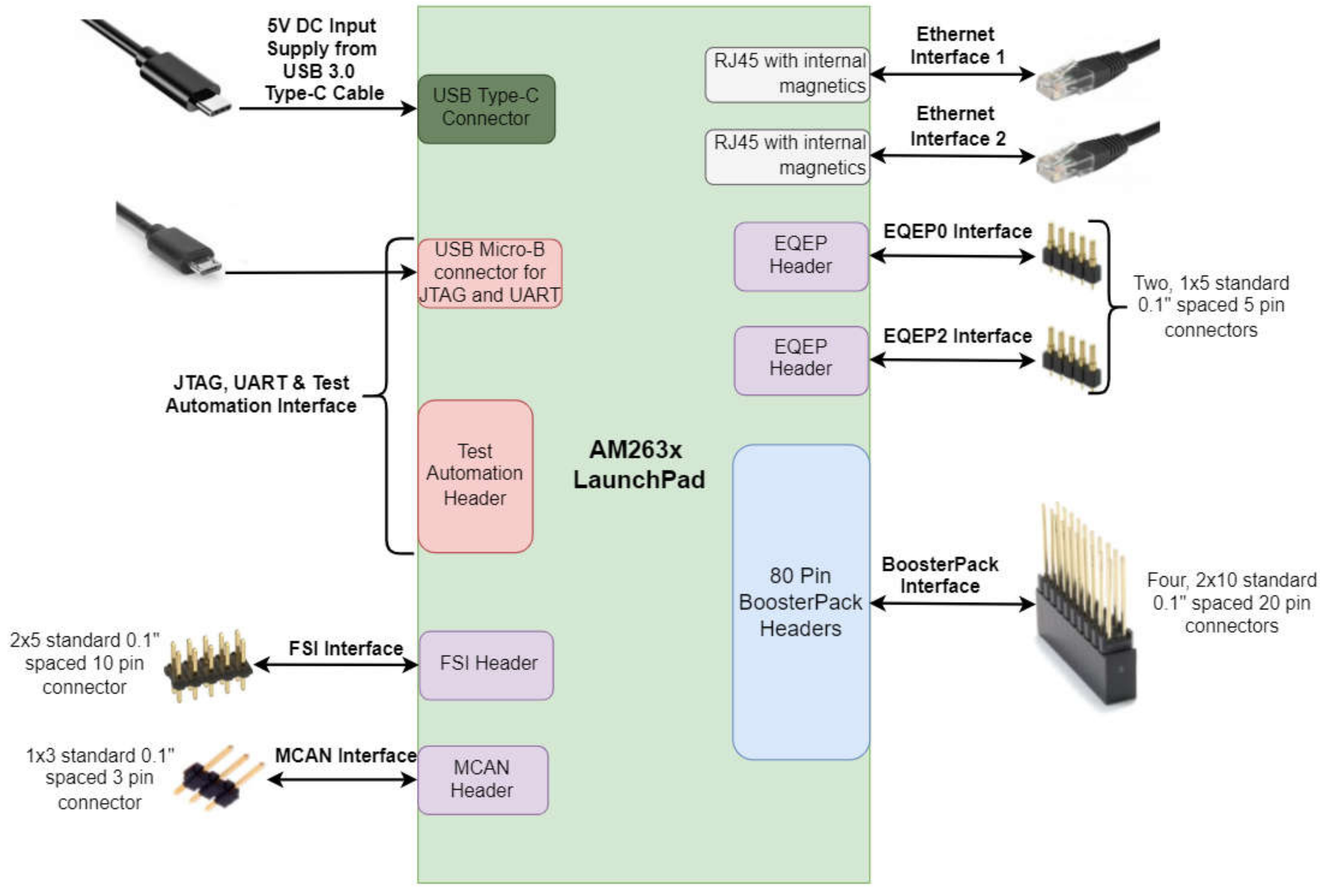

Figure 2-2. System Architecture

2.1 Introduction

The AM263x LaunchPad™ development kit is a simple and inexpensive hardware evaluation module (EVM) for the Texas Instruments™ Sitara™ AM263x series of microcontrollers (MCUs). This EVM provides an easy way to start developing on the AM263x MCUs with on-board emulation for programming and debugging as well as buttons and LEDs for a simple user interface. The LaunchPad also features two independent BoosterPack XL expansion connectors, on-board Controller Area Network (CAN) transceiver, two RJ45 Ethernet ports, and an on-board XDS110 debug probe.

2.2 Kit Contents

The Sitara AM263x Series LaunchPad Development Kit contains the following items:

- AM263x Sitara Series LaunchPad development board
- USB Micro-B cable
- Micro SD card
- CAT5 Ethernet cable

The kit does not include:

- USB Type-C 5V/3A AC/DC supply
- USB Type-C cable

2.3 Specification

2.3.1 Key Features

The AM263x LaunchPad has the following features:

- PCB dimensions:
- Powered through 5V, 3A USB Type-C input
- Two RJ45 Ethernet ports capable of 1Gb or 100Mb speeds
- On-board XDS110 debug probe
- Three push buttons:
  - PORz
  - User interrupt
  - RESETz
- LEDs for:
  - Power status
  - User testing
  - Ethernet connection
  - I2C driven array
- CAN connectivity with on-board CAN transceiver
- Dedicated FSI connector
- TI Test Automation Header
- MMC interface to micro SD card connector
- Two independent Enhanced Quadrature Encoder Pulse (EQEP) based encoder connectors
- Two independent BoosterPack XL (40 pin) standard connectors featuring stackable headers to maximize expansion through the BoosterPack ecosystem
- On-Board memory:
  - 128Mbyte QSPI Flash
  - 1Mbyte I2C Board ID EEPROM

2.3.2 Component Identification

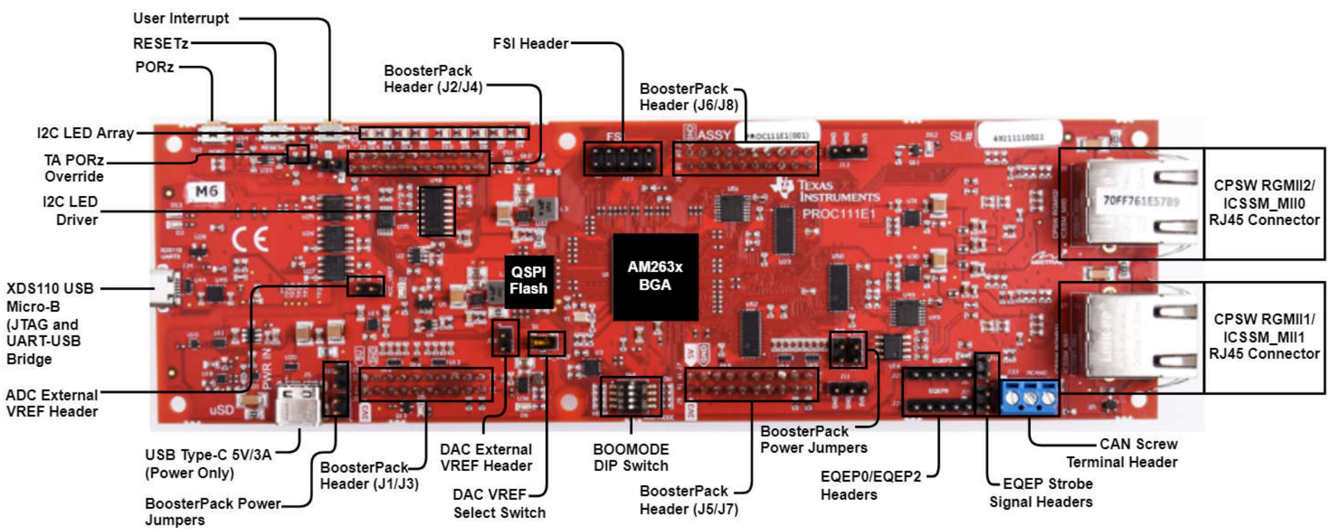

Figure 2-3. AM263x LaunchPad Top Component Identification

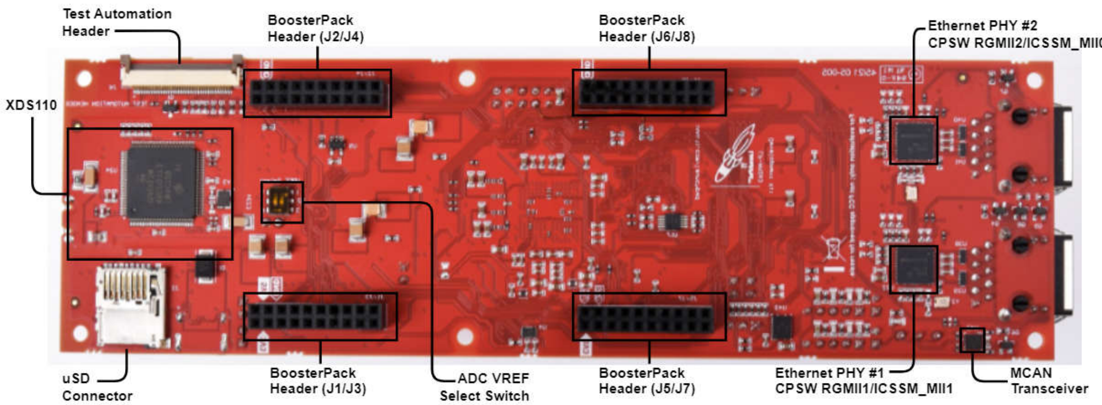

Figure 2-4. AM263x LaunchPad Bottom Component Identification

2.3.3 Functional Block Diagram

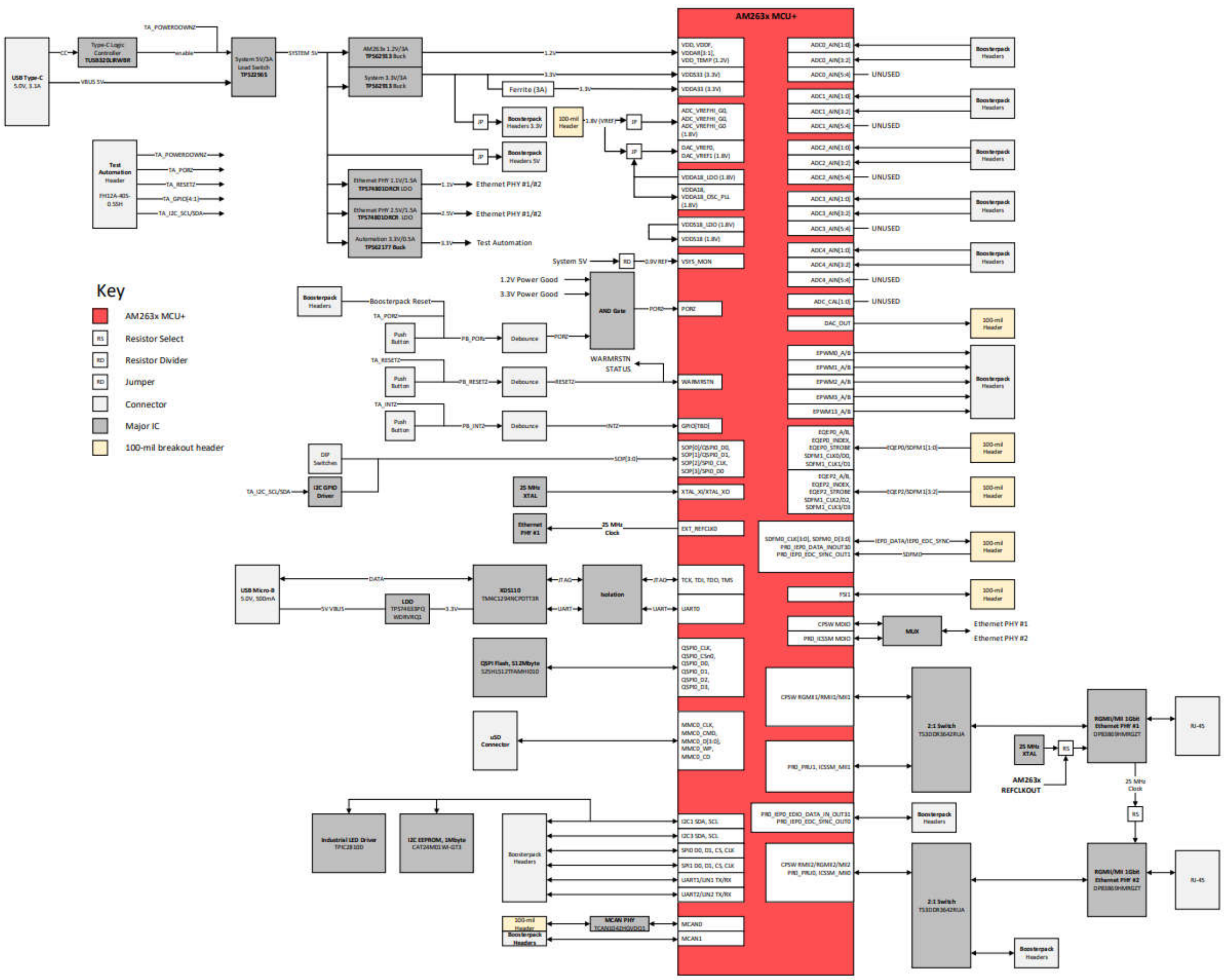

Figure 2-5. AM263x LaunchPad Functional Block Diagram

2.4 Device Information

The AM263x Sitara™ Arm® Microcontrollers are built to meet the complex real-time processing needs of next generation industrial and automotive embedded products. The AM263x MCU family consists of multiple pin-to-pin compatible devices with up to four 400MHz Arm® Cortex®-R5F cores. As an option, the Arm® R5F subsystem can be programmed to run in lockstep or dual-core mode for a multiple functional safety configurations. The industrial communications subsystem (PRU-ICSS) enables integrated industrial Ethernet communication protocols such as PROFINET®, TSN, Ethernet/IP®, EtherCAT® (among many others), standard Ethernet connectivity, and even custom I/O interfaces. The family is designed for the future of motor control and digital power applications with advanced analog sensing and digital actuation modules.

The multiple R5F cores are arranged in cluster subsystems with 256KB of shared tightly coupled memory (TCM) along with 2MB of shared SRAM, greatly reducing the need for external memory. Extensive ECC is included for on-chip memories, peripherals, and interconnects for enhanced reliability. Granular firewalls managed by the Hardware Security Manager (HSM) enable developers to implement stringent security-minded system design requirements. Cryptographic acceleration and secure boot are also available on AM263x devices.

TI provides a complete set of microcontroller software and development tools for the AM263x family of microcontrollers.

2.5 BoosterPacks

The AM263x LaunchPad development kit provides an easy and inexpensive way to develop applications with the AM263x Series microcontroller. BoosterPacks are add-on boards that follow a pin-out standard created by Texas Instruments. The TI and third-party ecosystem of BoosterPacks greatly expands the peripherals and potential applications that you can easily explore with the AM263x LaunchPad. For a detailed diagram on the pin-out of the AM263x LaunchPad, refer to BoosterPack Headers

You can also build your own BoosterPack by following the design guidelines on TI's website. Texas Instruments even helps you promote your BoosterPack to other members of the community. TI offers a variety of avenues for you to reach potential customers.

2.6 Compliance

All components selected meet *RoHS compliance* .

2.7 Security

The AM263x LaunchPad features a High Security, Field Securable (HS-FS) device. An HS-FS device has the ability to use a one time programming to convert the device from HS-FS to High Security, Security Enforced (HS-SE).

The AM263x device leaves the TI factory in an HS-FS state where customer keys are not programmed and has the following attributes:

- Does not enforce the secure boot process
- M4 JTAG port is closed
- R5 JTAG port is open
- Security Subsystem firewalls are closed
- SoC Firewalls are open
- ROM Boot expects a TI signed binary (encryption is optional)
- TIFS-MCU binary is signed by the TI private key

The One Time Programmable (OTP) keywriter converts the secure device from HS-FS to HS-SE. The OTP keywriter programs customer keys into the device eFuses to enforce secure boot and establish a root of trust. The secure boot requires an image to be encrypted (optional) and signed using customer keys, which are verified by the SoC. A secure device in the HS-SE state has the following attributes:

- M4, R5 JTAG ports are both closed
- Security Subsystems and SoC Firewalls are both closed
- TIFS-MCU and SBL need to be signed with active customer key

3 Board Setup

3.1 Power Requirements

The AM263x LaunchPad is powered from a 5V, 3A USB Type-C input. The following sections describe the power distribution network topology that supply the AM263x LaunchPad, supporting components and the reference voltages.

Power supply options that are compatible with the AM263x LaunchPad:

- When using the USB Type-C input:
  - 5V, 3A power adapter with USB-C receptacle
  - 5V, 3A power adapter with captive USB-C cable
  - PC USB Type-C port that has Power Delivery classification
    - Thunderbolt
    - Battery behind USB logo

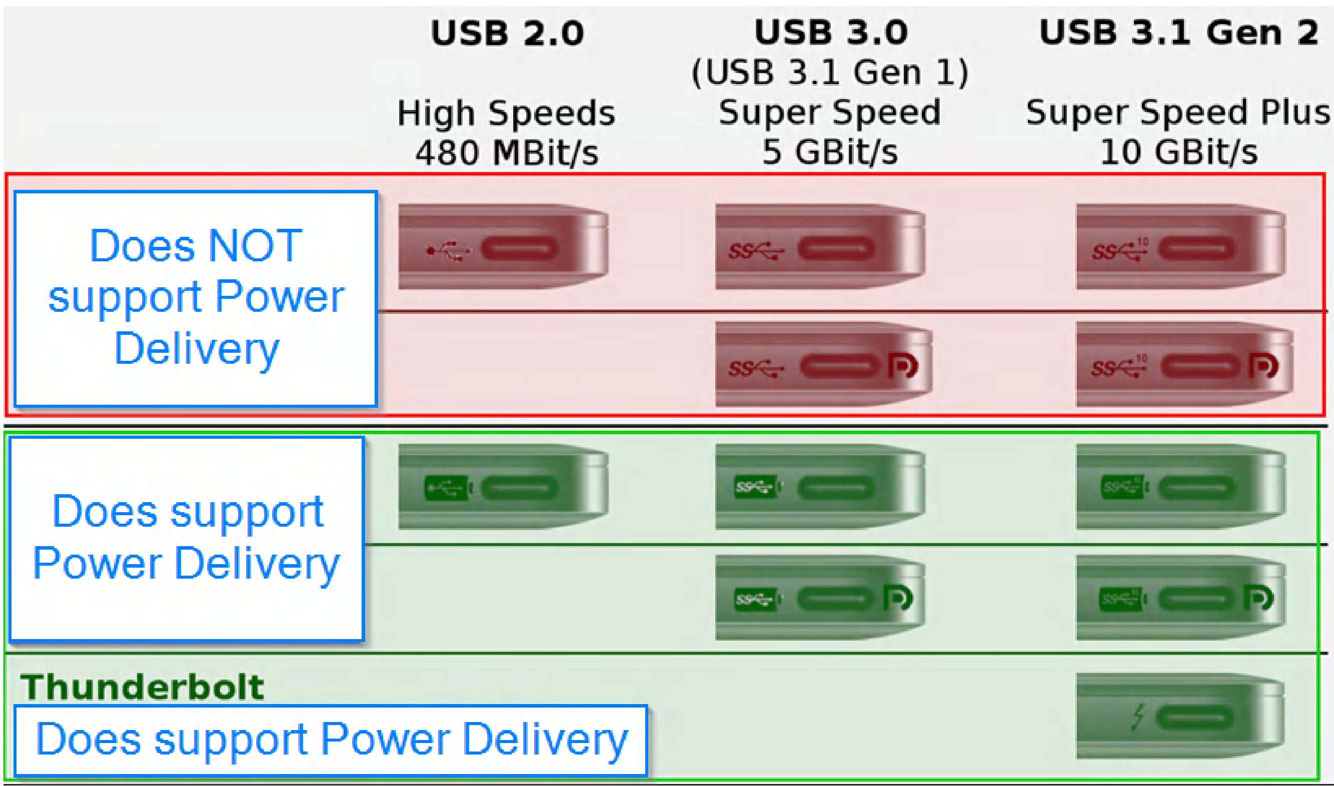

Figure 3-1. USB Type-C Power Delivery Classification

Power supply options that are **NOT** compatible with the AM263x LaunchPad:

- When using USB Type-C input:
  - Any USB adapter cables such as:
    - Type-A to Type-C
    - Micro-B to Type-C
    - DC barrel jack to Type-C
  - 5V, 1.5A power adapter with USB-C captive cable or receptacle
  - PC USB Type-C port not capable of 3A

3.1.1 Power Input Using USB Type-C Connector

The AM263x LaunchPad is powered through a USB Type-C connection. The USB Type-C source is capable of providing 3A at 5V and advertises the current sourcing capability through CC1 and CC2 signals. On AM263x LP, the CC1 and CC2 from USB Type-C connector are interfaced to the port controller IC (TUSB320). This device uses the CC pins to determine port attach and detach, cable orientation, role detection, and port control for Type-C current mode. The CC logic detects the Type-C current mode as default, medium, or high depending on the role detected.

The Port pin is pulled down to ground with a resistor to configure it as upward facing port (UFP) mode. VBUS detection is implemented to determine a successful attach in UFP mode. The OUT1 and OUT2 pins are connected to a NOR gate. Active low on both the OUT1 and OUT2 pins advertises high current (3A) in the attached state which enables the VUSB_5V0 power switch to provide the VSYS_5V0 supply which powers other regulators and LDOs.

In UFP mode, the port controller IC constantly presents pull-down resistors on both CC pins. The port controller IC also monitors the CC pins for the voltage level corresponding to the Type-C mode current advertisement by the connected DFP. The port controller IC de-bounces the CC pins and waits for VBUS detection before successfully attaching. As a UFP, the port controller device detects and communicates the advertised current level of the DFP to the system through the OUT1 and OUT2 GPIOs.

The AM263x LP power requirement is 5V at 3A and if the source is not capable of providing the required power, the output at the NOR gate becomes low and disables the VUSB_5V0 power switch. Therefore, if the power requirement is not met, all power supplies except VCC3V3_TA remain in the off state. The board gets powered on completely only when the source can provide 5V at 3A.

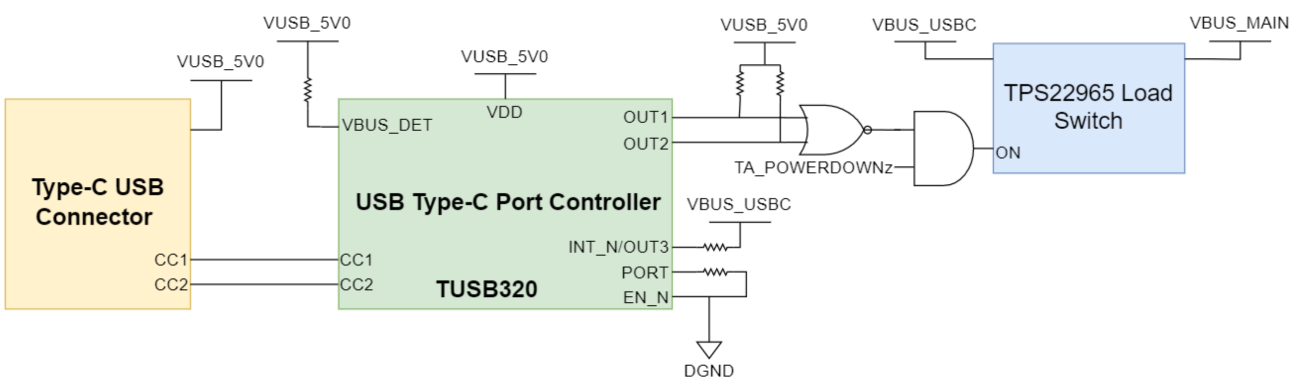

Figure 3-2. Type-C CC Configuration

Table 3-1. Current Sourcing Capability and State of USB Type-C Cable

OUT1	OUT2	Advertisement
H	H	Default current in unattached state
H	L	Default current in attached state
L	H	Medium current (1.5A) in attached state
L	L	High current (3.0A) in attached state

The AM263x LaunchPad includes a power option based on discrete regulators for each of the power rails. During the initial stage of the power supply, the 5V supplied by the Type-C USB connector is used to generate all of the necessary voltages required by the LaunchPad.

Discrete DC-DC buck regulators and LDOs are used to generate the supplies required for the AM263x system on a chip (SoC) and other peripherals.

Table 3-2. Voltage Rail Generation

Component	Function	Voltage In	Voltage Out
TPS62913	AM263x Core Digital 1.2 V	5.0 V	1.2 V
TPS74801	System 3.3 V	5.0 V	3.3 V
TSP74801	Ethernet PHY 2.5 V	5.0 V	2.5 V
TPS74801	Ethernet PHY 1.1 V	5.0 V	1.1 V
TPS62177	Test Automation Header 3.3 V	5.0V	3.3 V

3.1.2 Power Status LEDs

Multiple power-indication LEDs are provided on-board to indicate to users the output status of major supplies. The LEDs indicate power across various domains.

Table 3-3. Power Status LEDs

Name	Default Status	Operation	Function
D2	ON	VSYS_5V0	Power indicator for voltage
D4	ON	VSYS_3V3	Power indicator for voltage
D5	ON	PG_VDD_1V2	Power indicator for voltage
D6	ON	VSYS_TA_3V3	Power indicator for voltage
DS1	OFF	SAFETY_ERROR	Power error indication for voltage - VUSB_5V0
D3	OFF	XDS_PROGSTAZ1	LED will glow after micro-B connection is made
DS3	OFF	XDS_PROGSTAZ2	LED will glow to indicate communication over JTAG

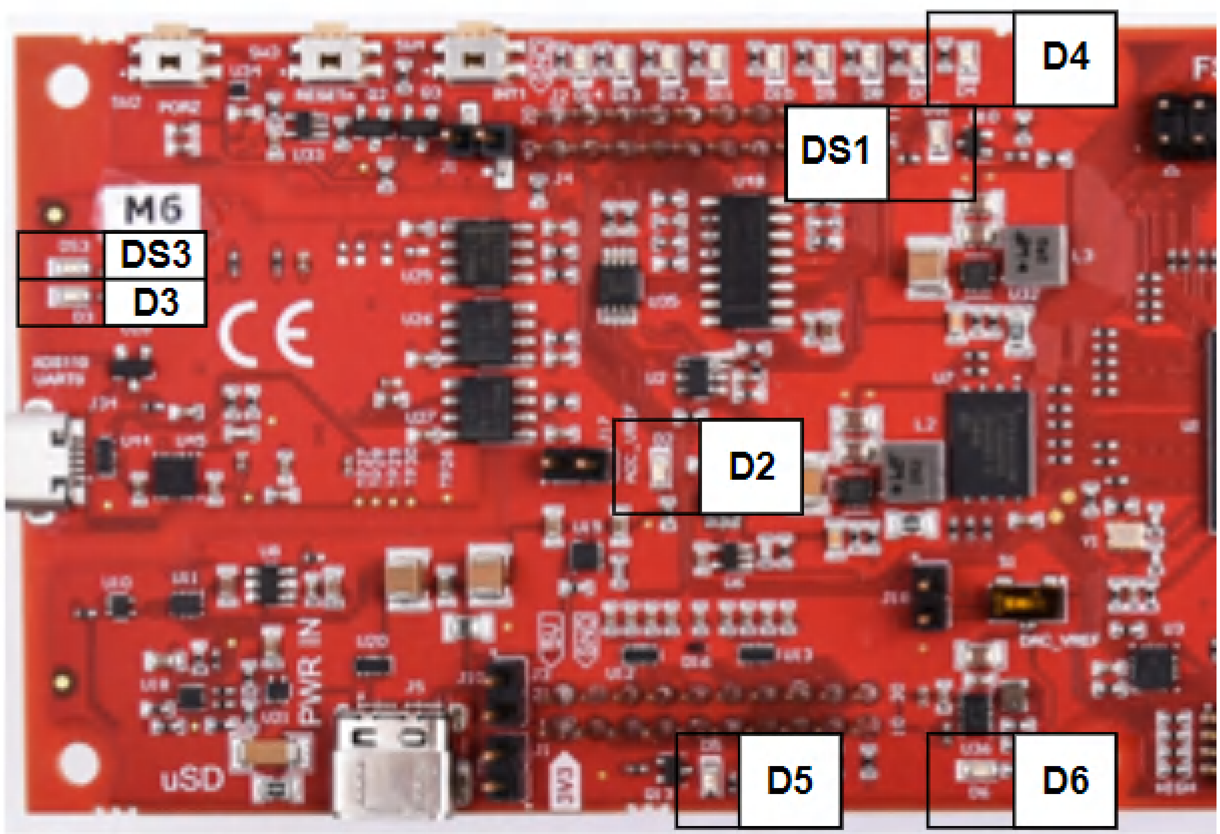

Figure 3-3. Power Status LEDs

3.1.3 Power Tree

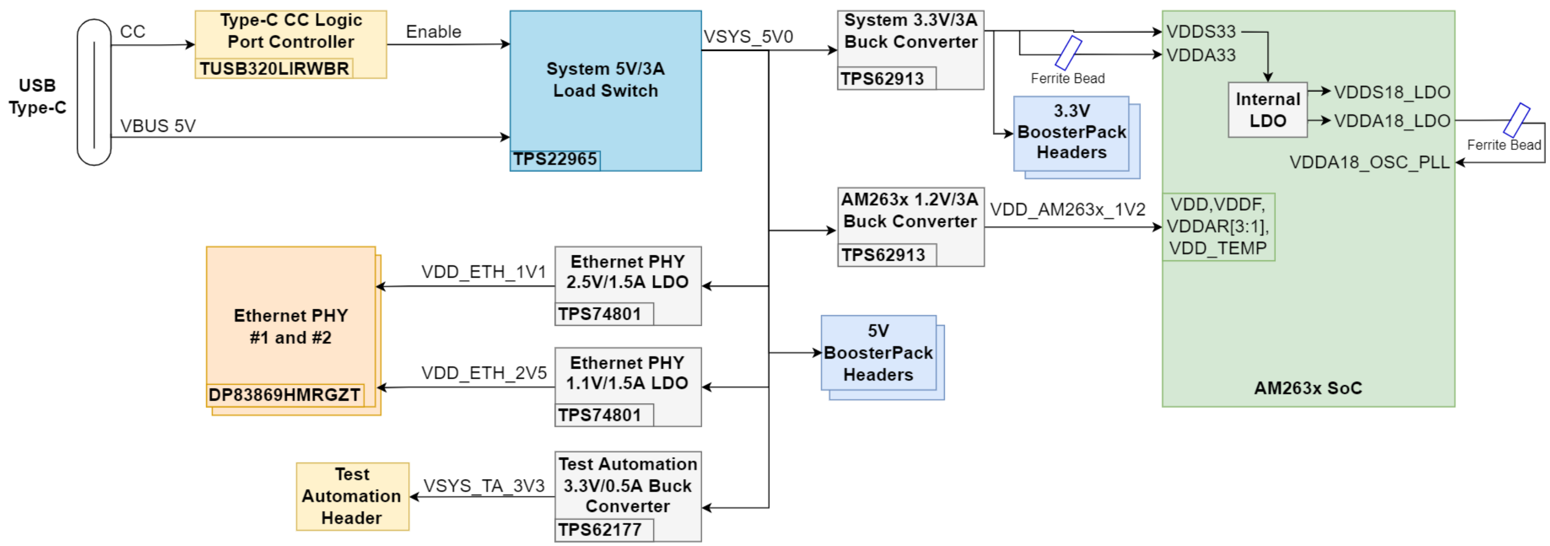

Figure 3-4. Power Tree Diagram of AM263x LaunchPad

3.2 Push Buttons

The LaunchPad supports multiple user push buttons that provide reset inputs and user interrupts to the AM263x SoC.

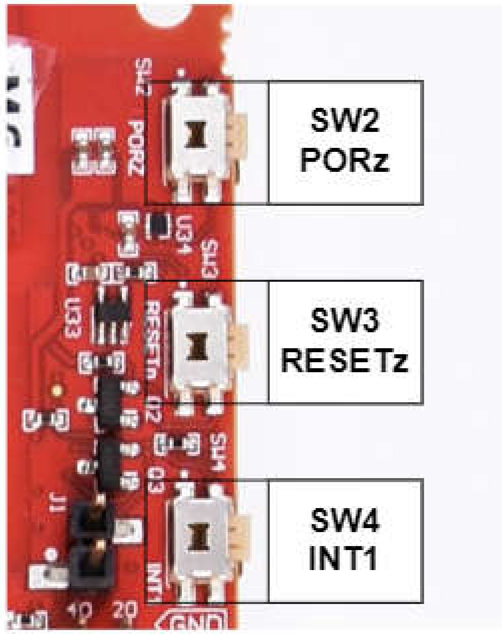

Figure 3-5. Push Buttons

Table 3-4 lists the push buttons that are placed on the top side of the AM263x LaunchPad.

Table 3-4. LaunchPad Push Buttons

Push Button	Signal	Function
SW2	PORz	SoC PORz reset input
SW3	RESETz	SoC warm reset input
SW4	INT1	User Interrupt Signal

3.3 Boot Mode Selection

The bootmode for the AM263x is selected by a DIP switch (SW1) or the test automation header. The test automation header uses an I2C expansion buffer to drive the bootmode when PORz is toggled. The supported boot modes are shown in Table 3-6. The DIP Switch configurations for each bootmode are shown in Table 3-5.

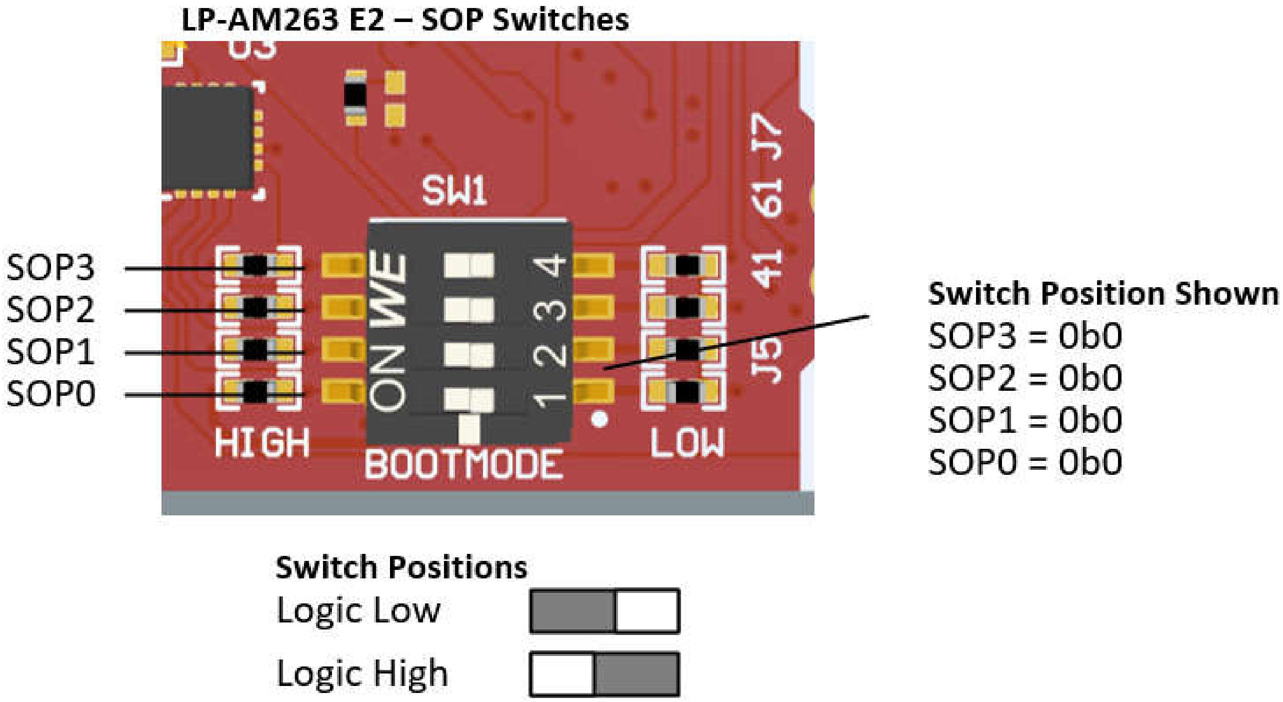

Figure 3-6. Bootmode DIP Switch Positions

Table 3-5. Boot-Mode Selection

Boot Mode	SPI0_D0_pad (SOP3)	SPI0_CLK_pad (SOP2)	QSPI_D1 (SOP1)	QSPI_D0 (SOP0)
QSPI (4S) - Quad Read Mode	1	1	1	1
UART	1	1	1	0
QSPI (1S) - Single Read Mode	1	1	0	1
QSPI (4S) - Quad Read UART Fallback Mode	1	0	1	1
QSPI (1S) - Single Read UART Fallback Mode	1	0	1	0
DevBoot	0	1	0	0
Unsupported Boot Mode	All other combinations not defined above			

Table 3-6. Supported Boot Modes

Boot Mode/Peripheral	Boot Media/Host	Notes
QSPI (4S) - Quad Read Mode	QSPI Flash	Download and boot SBL from QSPI flash in quad read mode. Attempt Primary SBL, followed by Secondary SBL if primary loading fails.
UART	External Host	Download and boot SBL from UART. Device is expected to get SBL from UART. Device supports the XMODEM protocol for download over UART.
QSPI (1S) - Single Read Mode	QSPI Flash	Download and boot SBL from QSPI flash in single read mode. Attempt Primary SBL,followed by Secondary SBL if primary loading fails.
QSPI (4S) - Quad Read UART Fallback Mode	QSPI Flash / External Host	Download and boot SBL from QSPI flash in quad read mode. Attempt Primary SBL, followed by Secondary SBL if primary loading fails. If Secondary SBL also fails then boot from external host via UART interface.
QSPI (1S) - Single Read UART Fallback Mode	QSPI Flash / External Host	Download and boot SBL from QSPI flash in single read mode. Attempt Primary SBL, followed by Secondary SBL if primary loading fails. If Secondary SBL also fails then boot from external host via UART interface.
DevBoot	N/A	No SBL. Used for development purposes only.

4 Hardware Description

4.1 Functional Block Diagram

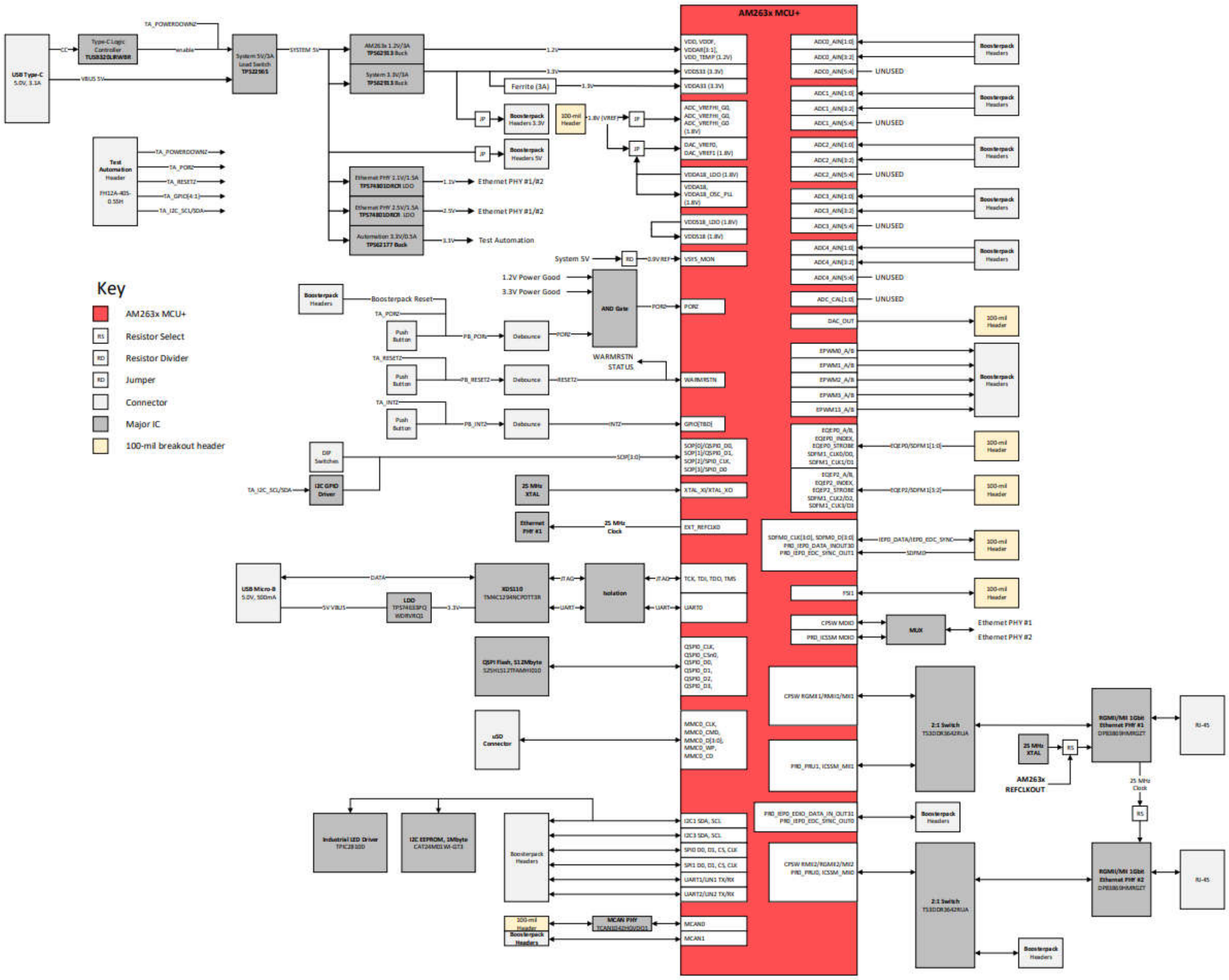

Figure 4-1. AM263x LaunchPad Functional Block Diagram

4.2 GPIO Mapping

Table 4-1. GPIO Mapping Table

GPIO Description	GPIO	Functionality	Net Name	Active Status
Enable control to CPSW RGMII1/MII1 Mux	GPIO1	GPIO	RGMII1_ICSSM_MUX_EN_GPIO1	LOW
Industrial LED Driver Enable	GPIO25	GPIO	AM263_LED_ENABLE_GP25	LOW
User Defined LED	GPIO26	GPIO	AM263_LED_GPIO26	LOW
Standby input to CAN Transceiver	GPIO51	GPIO	AM263_CAN_STB_GPIO51	HIGH
MUX Enable	GPIO58	GPIO	AM263_MUX_EN_GPIO58	HIGH
Select line for BP Mux	GPIO63	GPIO	AM263_BP_MUX_SEL_GPIO63	LOW
Select line for PRU MUX	GPIO64	GPIO	AM263_PRU_MUX_SEL_GPIO64	LOW
Select line for CPSW RGMII1/MII1 MUX	GPIO105	GPIO	RGMII1_ICSSM_MUX_SEL_GPIO105	LOW
SD Card Load Switch Enable	GPIO122	GPIO	AM263_SD_ENABLE_GPIO122	LOW
Interrupt To SoC	GPIO123	Interrupt	AM263_INT1_PB_GPIO123	LOW

4.3 Reset

Figure 4-2 shows the reset architecture of the AM263x LaunchPad

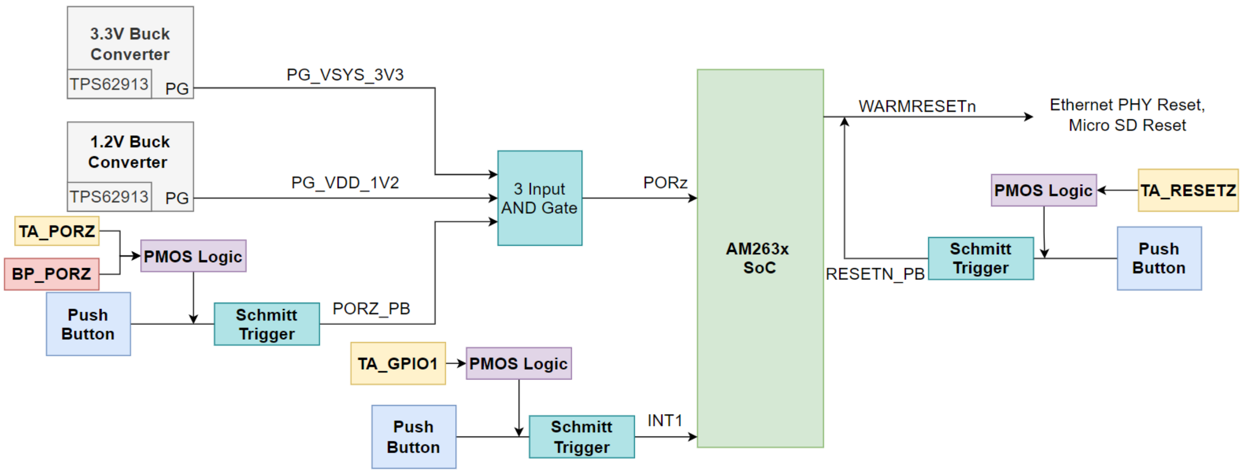

Figure 4-2. Reset Architecture

The AM263x LaunchPad has the following resets:

- PORz is the Power On Reset
- WARMRESETn is the warm reset

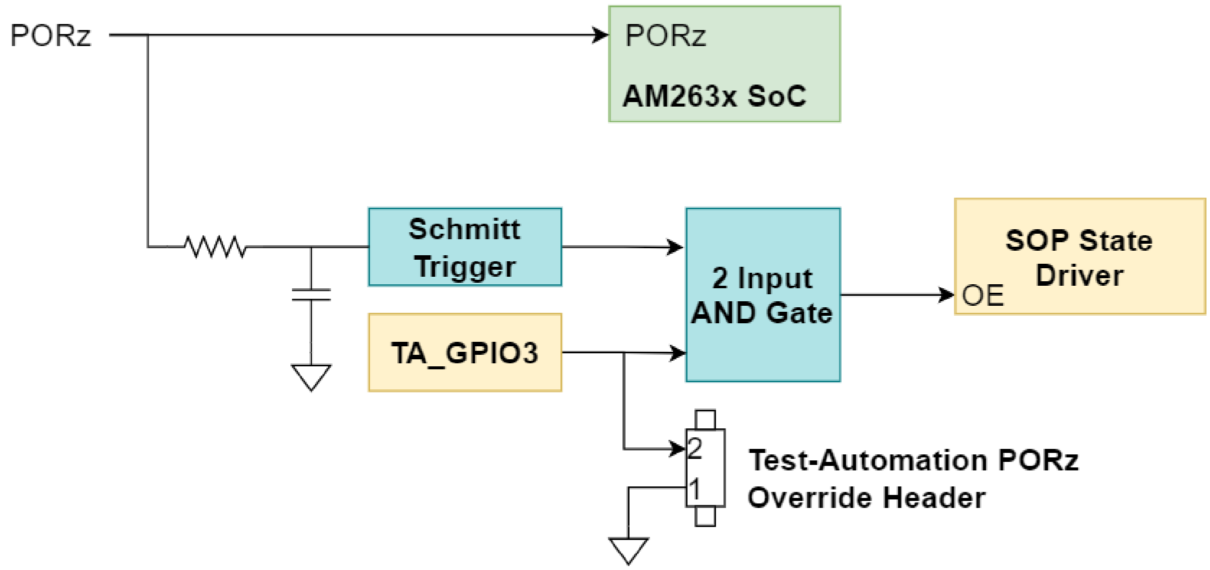

Figure 4-3. PORz Reset Signal Tree

The PORz signal is driven by a 3-input AND gate that generates a power on reset for the MAIN domain when:

- The 3.3V buck converter (TPS62913) power good output is driven low by having an output voltage that is below the power-good threshold.
- The 1.2V buck converter (TPS62912) power good output is driven low by having an output voltage that is below the power-good threshold.
- The user push button (SW2) is pressed.
- A P-Channel MOSFET gate's signal is logic LOW which causes V_GS of the PMOS to be less than zero and so the PORz signal connects to the PMOS drain which is tied directly to ground. The signals that can create the logic LOW input to the PMOS gate are:
  - TA_PORZ output from the Test Automation header
  - BP_PORZ output from either of the BoosterPack sites.

The PORz signal is tied to:

- AM263x SoC PORz input
- BOOTMODE State Driver's output enable input
  - There is an RC filter to create a 1ms delay from GND to 3.0V such that the SOP State Driver's output enable input is low longer than the required SOP hold time following a PORz de-assertion.

There is a Test-Automation PORz Override header that enables the ability to hold TA_GPIO3 low when a jumper is installed. This enables the BOOTMODE Control from the Test Automation Header.

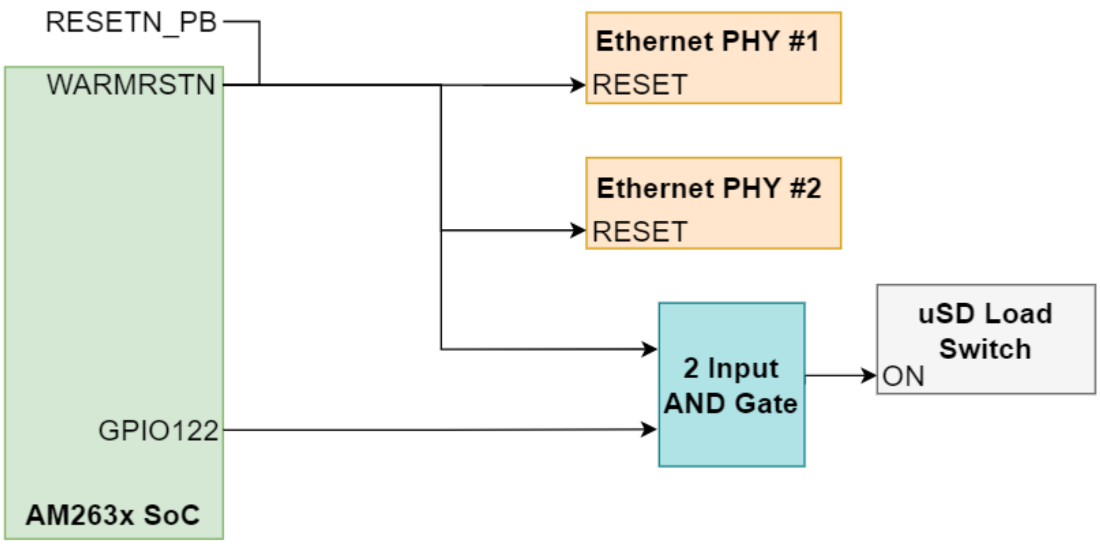

Figure 4-4. WARMRESETn Reset Signal Tree

The WARMRESETn signal creates a warm reset to the MAIN domain when:

- The user push button (SW3) is pressed.
- The Test Automation Header outputs a logic LOW signal (TA_RESETz) to a P-Channel MOSFET gate which causes V_GS of the PMOS to be less than zero and so the RESETz signal connects to the PMOS drain which is tied directly to ground.

The WARMRESETn signal is tied to:

- AM263x SoC WARMRESETN output
- RESETN_PB signal that is created from push button + PMOS logic
- Micro SD Load Switch control input via a 2 input AND Gate with an AM263x SoC driven GPIO signal (GPIO122)
- Both Ethernet PHY's reset input

The AM263x LaunchPad also has an external interrupt to the SoC , INT1, that occurs when:

- The user push button (SW4) is pressed.
- The Test Automation Header outputs a logic LOW signal (TA_GPIO1) to a P-Channel MOSFET gate which causes V_GS of the PMOS to be less than zero and so the INTn signal connects to the PMOS drain which is tied directly to ground.

4.4 Clock

The AM263x SoC requires a 25MHz clock input for XTAL_XI. The AM263x LaunchPad uses a 25MHz crystal for the SoC clock source. The LaunchPad also has two 25MHz Crystals on-board for the Ethernet PHY clocking. The SoC clock signal output CLKOUT0 can be used as a clock source for Ethernet PHY #1 by removing the resistors mounted for XTAL_XI and XTAL_XO from the 25MHz Ethernet PHY #1 Crystal and mounting the appropriate resistor for the CLKOUT0 signal to be routed to the XI pin of the Ethernet PHY.

The Ethernet PHY #1 clock signal output ETH1_CLKOUT can be used as a clock source for Ethernet PHY #2 by removing the resistors mounted for XTAL_XI and XTAL_XO from the 25MHz Ethernet PHY #2 Crystal and mounting the appropriate resistor for the ETH1_CLKOUT signal to be routed to the XI pin of Ethernet PHY #2.

The LaunchPad also requires a 16 MHz clock source for the XDS110 for UART-USB JTAG support.

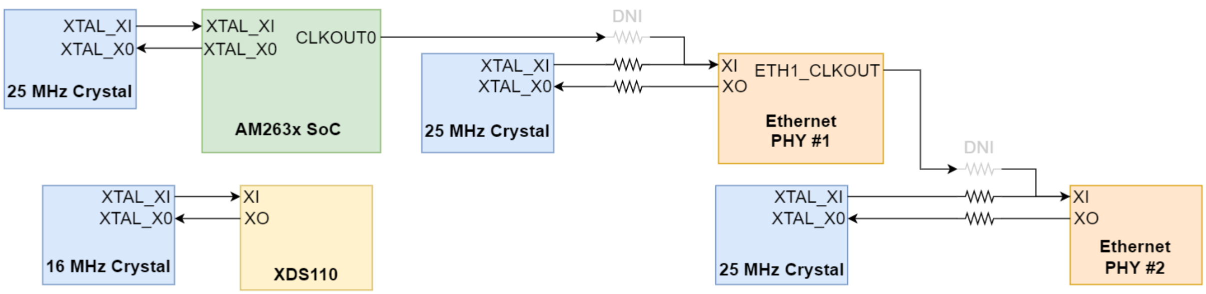

Figure 4-5. AM263x LaunchPad Clock Tree

4.5 Memory Interface

4.5.1 QSPI

The AM263x LaunchPad has a 128Mbit QSPI Flash memory device (S25FL128SAGNFI000), which is connected to the QSPI0 interface of the AM263x SoC. The QSPI interface supports single data rates with memory speeds up to 104MHz. The QSPI flash is powered by the 3.3V system supply.

Note

There is typically a reset pin for Flash memory. The Reset pin is not present in the WSON flash package that is used in the LaunchPad

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The QSPI0_D0/D1 signals are also used for BOOTMODE control logic. There are 10KΩ resistors used to isolate the BOOTMODE control logic after the value is latched.

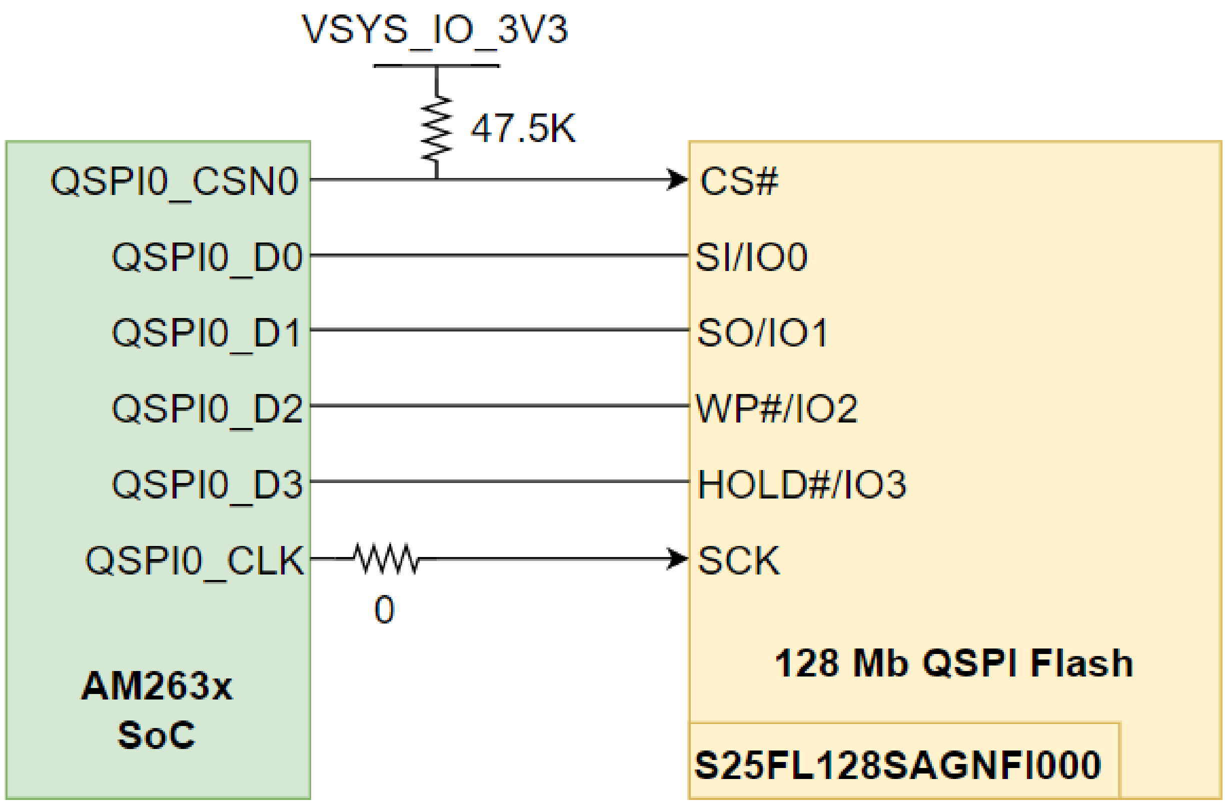


Figure 4-6. QSPI Flash Interface

4.5.2 Board ID EEPROM

The AM263x LaunchPad has a I2C based 1Mbit EEPROM (CAT23M01WI-GT3) to store board configuration details. The Board ID EEPROM is connected to the I2C1 interface of the AM263x SoC. The default I2C address of the EEPROM is set to 0x52 by pulling up the address pin A1 and pulling down the address pin A2 to ground. The Write Protect pin for the EEPROM is by default pulled down to ground and therefore Write Protect is disabled.

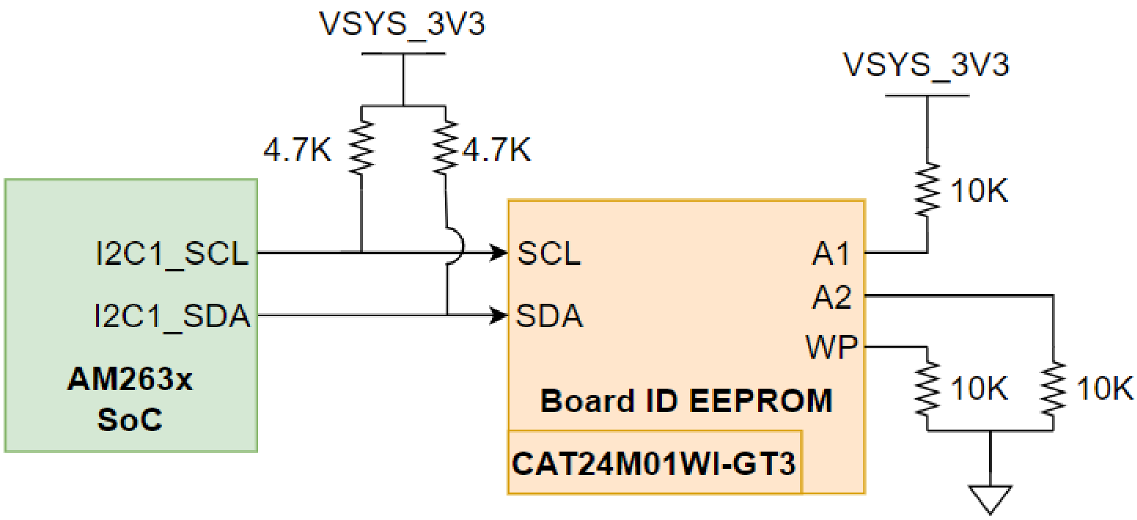


Figure 4-7. Board ID EEPROM

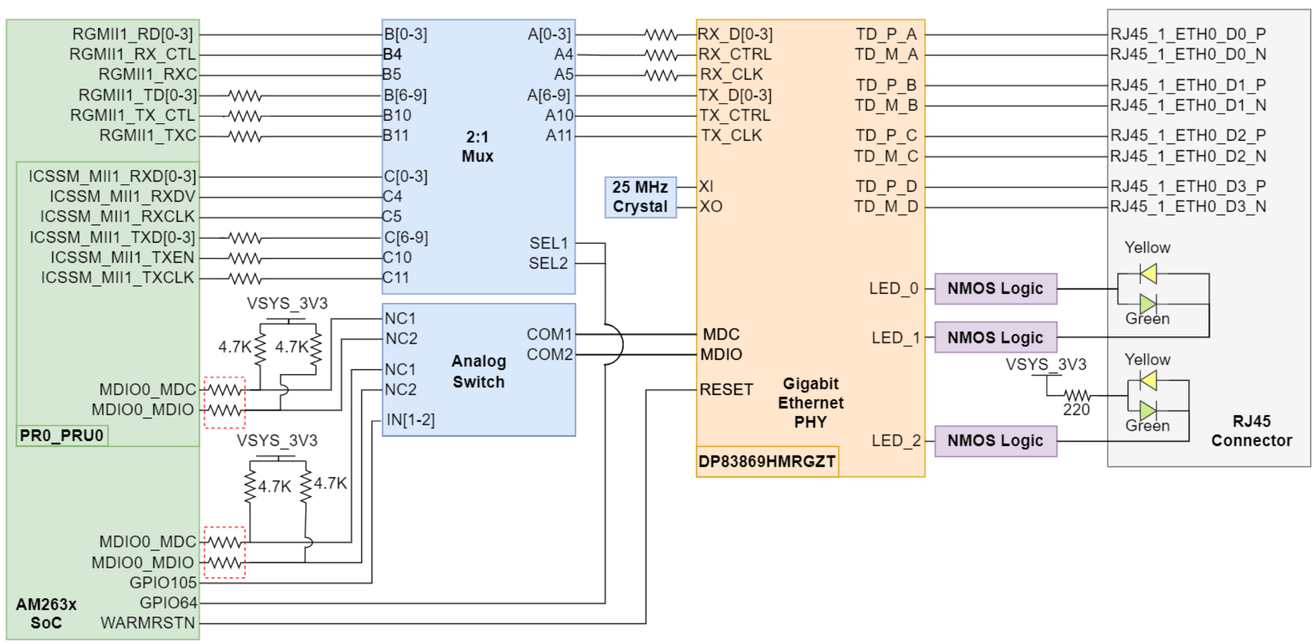
4.6 Ethernet Interface

4.6.1 Ethernet PHY #1 - CPSW RGMII/ICSSM

Note

The PRU internal pinmux mapping provided in the TRM is part of the original hardware definition of the PRU. However, due to the flexibility provided by the IP and associated firmware configurations, this is not necessarily a hard requirement. The first PRU implementation for AM65x had the MII TX pins swapped during initial SoC integration and this convention was maintained for subsequent PRU revisions to enable firmware reuse. To make use of the SDK firmware, use the SYSCONFIG generated PRU pin mapping.

The AM263x LaunchPad utilizes a 48-pin Ethernet PHY (DP83869HMRGZT) connected to either CPSW RGMII or one on-die programmable real-time unit and industrial communication subsystem (PRU-ICSS). There is a 2:1 mux that selects between the RGMII or PRU-ICSS signals. The PHY is configured to advertise 1-Gb operation. The Ethernet data signals of the PHY are terminated to an RJ45 connector. The RJ45 connector is used on the board for Ethernet 10/100/1000 Mbps connectivity with integrated magnetics and LEDs for link and activity indication.



A. The series termination resistors that are outlined with a red dotted box were updated from 0Ω to 33Ω to improve signal integrity between the AM263x MCU MDIO pins and the attached PHY pins. The modification is signified by an "M1" sticker on the top side of the LaunchPad near the PORz push button.

Figure 4-8. Ethernet PHY #1

The Ethernet PHY requires three separate power sources. VDDIO is the 3.3V, system generated supply. There are dedicated LDO's for the 1.1V and 2.5V supplies for the Ethernet PHY.

There are series termination resistors on the transmit clock and data signals located near the SoC. There are series termination resistors on the receive clock and data signals near the Ethernet PHY.

The MDC and MDIO signals from the SoC to the PHY require 4.7KΩ pull up resistors to the 3.3 V system supply voltage for proper operation. There is an analog switch (TS5A23159DGSR) that selects between the CPSW MDIO/MDC and the ICSSM MDIO/MDC signals to be routed to the Ethernet PHY.

Both the 2:1 Mux and analog switch are controlled by a GPIO signal that selects between CPSW RGMII and ICSSM signals.

Table 4-2. Ethernet PHY #1 CPSW/ICSSM Select

GPIO105	Condition	Function of Mux
LOW	RGMII CPSW Selected	Port A ↔ Port B
HIGH	ICSSM Selected	Port A ↔ Port C

The reset input for the Ethernet PHY is controlled by the WARMRESET AM263x SoC output signal.

The Ethernet PHY uses many functional pins as strap option to place the device into specific modes of operation.

Table 4-3. Ethernet PHY #1 Strapping Resistors

Functional Pin	Default Mode	Mode in LP	Function
RX_D0	0	3	PHY address: 0011
RX_D1	0	0	
JTAG_TDO/GPIO_1	0	0	RGMII to Copper
RX_D3	0	0	
RX_D2	0	0	
LED_0	0	0	Auto-negotiation, 1000/100/10 advertised, auto MDI-X
RX_ER	0	0	
LED_2	0	0	
RX_DV	0	0	Port Mirroring Disabled

Note

Each strap pin has an internal pull down resistance of 9KΩ

Note

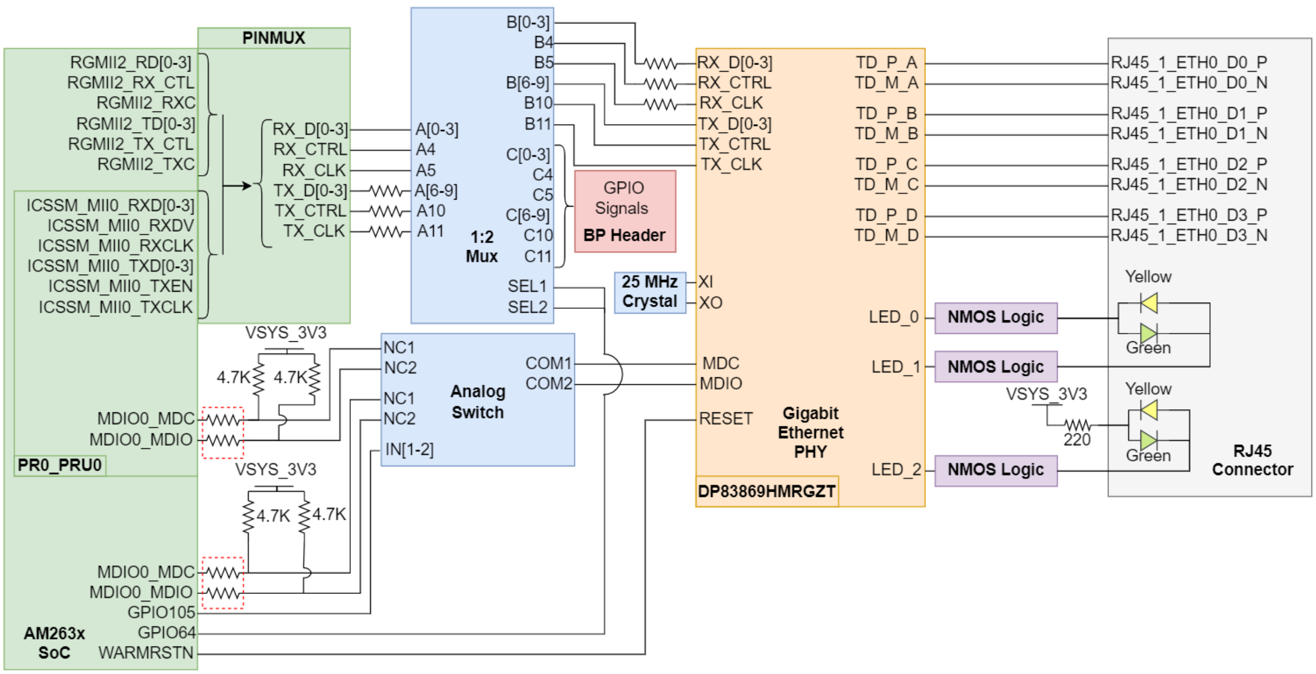
RX_D0 and RX_D1 are on a 4-level strap resistor mode scheme. All other signals are 2-level strap resistor modes.

4.6.2 Ethernet PHY #2: CPSW RGMII/ICSSM

Note

The PRU internal pinmux mapping provided in the TRM is part of the original hardware definition of the PRU. However, due to the flexibility provided by the IP and associated firmware configurations, this is not necessarily a hard requirement. The first PRU implementation for AM65x had the MII TX pins swapped during initial SoC integration and this convention was maintained for subsequent PRU revisions to enable firmware reuse. To make use of the SDK firmware, use the SYSCONFIG generated PRU pin mapping.

The AM263x LaunchPad utilizes a 48-pin Ethernet PHY (DP83869HMRGZT) connected to either CPSW RGMII or one on-die programmable real-time unit and industrial communication subsystem (PRU-ICSS). The RGMII CPSW port and ICSSM are internally pinmuxed on the AM263x SoC. For more information on the internal muxing of signals refer to Pinmux Mapping. The PHY is configured to advertise 1-Gb operation. The Ethernet data signals of the PHY are terminated to an RJ45 connector. The RJ45 connector is used on the board for Ethernet 10/100/1000 Mbps connectivity with integrated magnetics and LEDs for link and activity indication.



A. The series termination resistors that are outlined with a red dotted box were updated from 0Ω to 33Ω to improve signal integrity between the AM263x MCU MDIO pins and the attached PHY pins. The modification is signified by an "M1" sticker on the top side of the LaunchPad near the PORz push button.

Figure 4-9. Ethernet PHY #2

The Ethernet PHY requires three separate power sources. VDDIO is the 3.3V, system generated supply. There are dedicated LDO's for the 1.1V and 2.5V supplies for the Ethernet PHY.

There are series termination resistors on the transmit clock and data signals located near the SoC. There are series termination resistors on the receive clock and data signals near the Ethernet PHY.

The MDC and MDIO signals from the SoC to the PHY require 4.7KΩ pull up resistors to the 3.3 V system supply voltage for proper operation. There is an analog switch (TS5A23159DGSR) that selects between the CPSW MDIO/MDC and the ICSSM MDIO/MDC signals to be routed to the Ethernet PHY.

AM263x internal Pinmux is used to select between CPSW RGMII and ICSSM signals. The signals are then routed to a 1:2 Mux (TS3DDR3812RUAR) that selects between mapping the signals to the Ethernet PHY or the BP headers in the case that the PRU GPIO signals are being used in a BoosterPack application. There is an AM263x SoC GPIO select signal that drives the 1:2 mux.

Table 4-4. Ethernet PHY #2 CPSW/ICSSM Select

GPIO64	Condition	Function of Mux
LOW	Ethernet PHY Selected	Port A ↔ Port B
HIGH	BoosterPack header Selected	Port A ↔ Port C

The reset input for the Ethernet PHY is controlled by the WARMRESET AM263x SoC output signal.

The Ethernet PHY uses many functional pins as strap option to place the device into specific modes of operation.

Table 4-5. Ethernet PHY #2 Strapping Resistors

Functional Pin	Default Mode	Mode in LP	Function
RX_D0	0	0	PHY address: 1100
RX_D1	0	3	
JTAG_TDO/GPIO_1	0	0	RGMII to Copper
RX_D3	0	0	
RX_D2	0	0	
LED_0	0	0	Auto-negotiation, 1000/100/10 advertised, auto MDI-X
RX_ER	0	0	
LED_2	0	0	
RX_DV	0	0	Port Mirroring Disabled

Note

Each strap pin has an internal pull down resistance of 9KΩ

Note

RX_D0 and RX_D1 are on a 4-level strap resistor mode scheme. All other signals are 2-level strap resistor modes.

4.6.3 LED Indication in RJ45 Connector

The AM263x LaunchPad has two RJ45 network ports for the CPSW RGMII and ICSSM signals of the AM263x SoC. Each RJ45 connector contains two bi-color LEDs that are used to indicate link and activity.

RJ45 Connector LED indication for the Ethernet PHY #1:

Table 4-6. Ethernet PHY #1 RJ45 Connector LED indication

LED	Color	Indication
Right LED	Green	Ethernet PHY power established
	Yellow	Transmit or Receive activity
Left LED	Green	Link OK
	Yellow	1000BT link is up

RJ45 Connector LED indication for the Ethernet PHY #2:

Table 4-7. Ethernet PHY #2 RJ45 Connector LED indication

LED	Color	Indication
Right LED	Green	Ethernet PHY power established
	Yellow	Transmit or Receive activity
Left LED	Green	Link OK
	Yellow	1000BT link is up

4.7 I2C

The AM263x LaunchPad uses two AM263x SoC inter-integrated circuit (I2C) ports to operate as a controller for various targets. It is important that all I2C data and clock lines are pulled up to the 3.3V system voltage supply to enable communication.

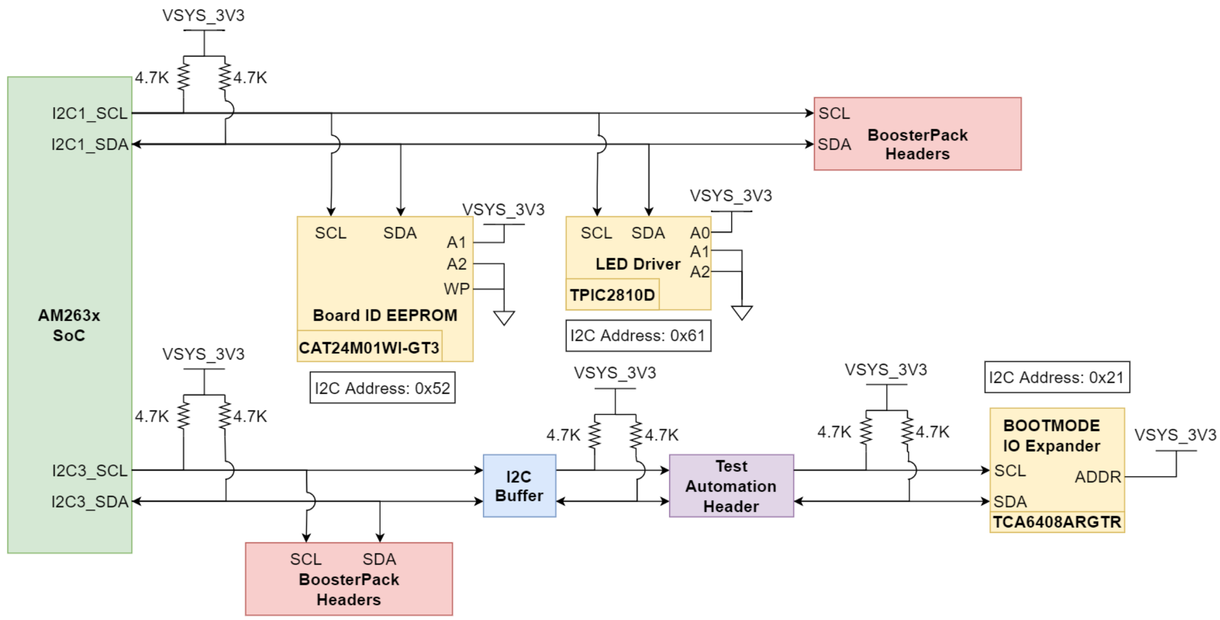


Figure 4-10. I2C Targets

Table 4-8. I2C Addressing

Target	I2C Instance	I2C Addres Bit Description	Device Addressing	LaunchPad Config.	I2C Address
Board ID EEPROM	I2C1	The first 4 bits of the device address are set to 1010, the next two are set by the A2 and A1 pins, the seventh bit, a16, is the most significant internal address bit	0b10110[A2][A1][a16] A1 is connected to 3.3V supply A2 is connected to ground	0b1010010	0x52
LED Driver	I2C1	The first four bits of the target address are 1100, the following three are determined by A2, A1, and A0	0b1100[A2][A1][A0] A2/A1 are connected to ground A0 is connected to 3.3V supply	0b1100001	0x61
BoosterPack Headers	I2C1	Dependent on target			
BOOTMODE IO Expander	I2C3/TA_I2C	The first 6 bits of the target address are set to 010000, the next bit is determined by the addr pin of the IO expander	0b010000[ADDR] ADDR pin connected 3.3V supply	0b0100001	0x21
BoosterPack Headers	I2C3	Dependent on target			

Note

Underlined address bits are fixed based on the device addressing and cannot be configured.

4.8 Industrial Application LEDs

The AM263x LaunchPad has an LED Driver (TPIC2810D) that is used for Industrial Communication LEDs. The driver is connected to eight green LEDs and it has an I2C address of 0x61.

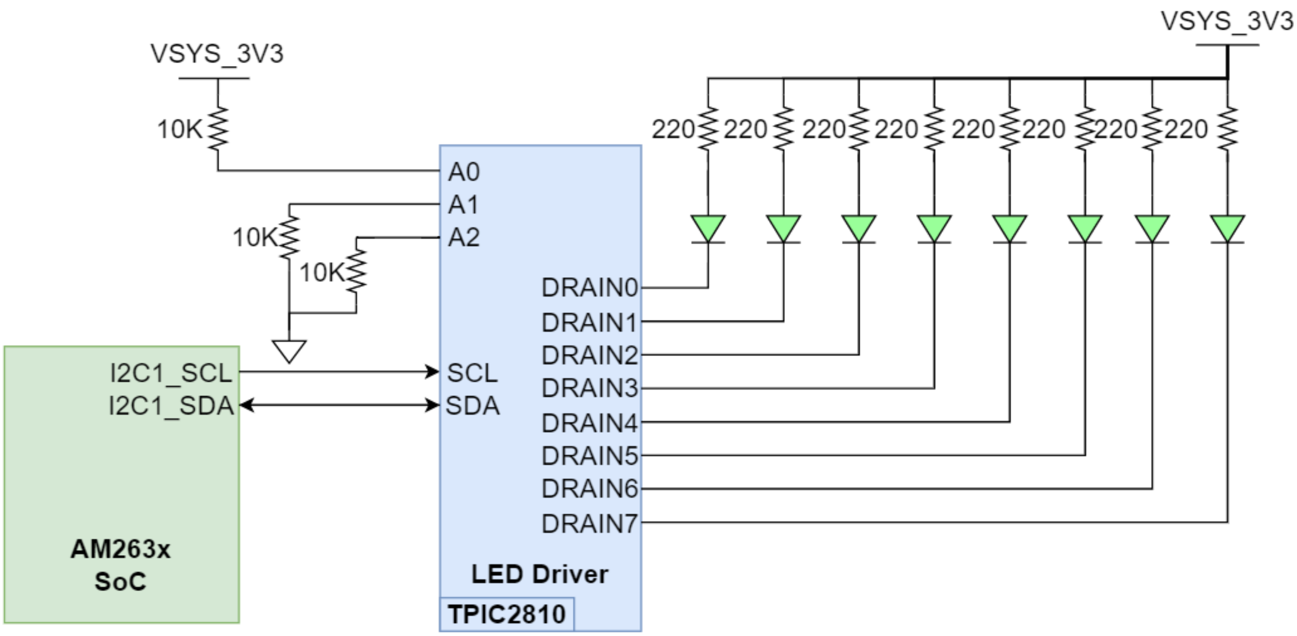


Figure 4-11. Industrial Application I2C LED Array

4.9 SPI

The AM263x LaunchPad maps two SPI instances (SPI0,SPI1) from the AM263x SoC to the BoosterPack Headers. Series termination resistors are placed near the SoC for each SPI clock and SPI D0 signal. There is a 2:1 Mux (SN74CB3Q3257PWR) that is responsible for selecting SPI signals for proper function. The Mux is driven by two GPIO signals that are generated from the AM263x SoC.

Table 4-9. SPI MUX

Output Enable (OE)	Select (S)	Input/Output	Function
Low	Low	A ↔ B1	A port = B1 port
Low	High	A ↔ B2	A port = B2 port
High	X	Hi-Z	Disconnect

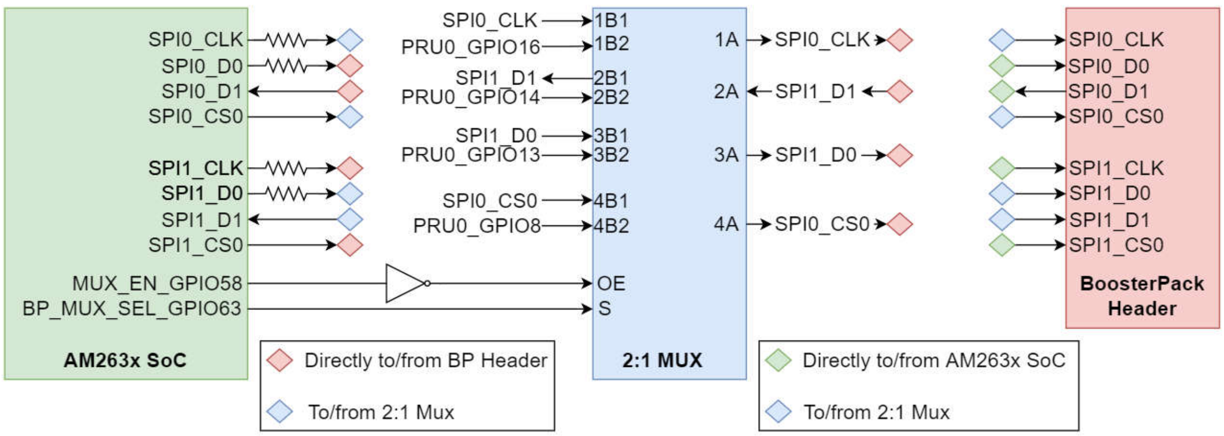


Figure 4-12. SoC SPI to BoosterPack

4.10 UART

The AM263x LaunchPad uses the XDS110 as a USB2.0 to UART bridge for terminal access. UART0 transmit and receive signals of the AM263x SoC are mapped to the XDS110 with a dual channel isolation buffer (ISO7221DR) for translating from the 3.3V IO voltage supply to the 3.3V XDS supply. The XDS110 is connected to a micro-B USB connector for the USB 2.0 signals. ESD protection is provided to the USB 2.0 signals by a transient voltage suppression device (TPD4E004DRYR). The micro-B USB connector's VBUS 5V power is mapped to a low dropout regulator (TPS79601DRBR) to generate the 3.3V XDS110 supply. A separate 3.3V supply for the XDS110 allows for the emulator to maintain a connection when power to the LaunchPad is removed.

A separate UART instance is mapped directly to the BoosterPack header.

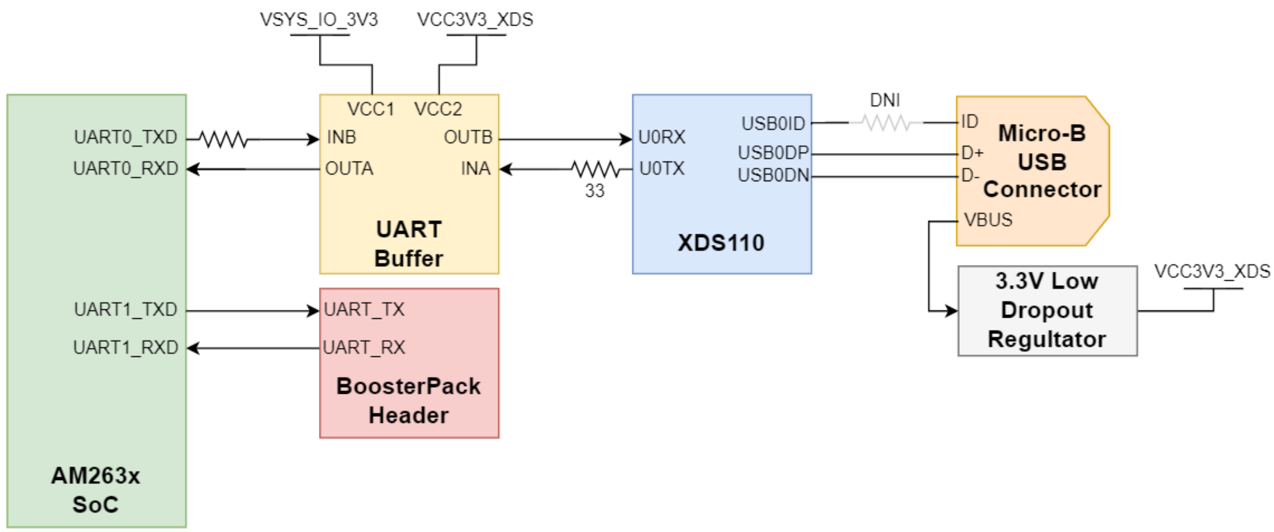


Figure 4-13. UART

4.11 MCAN

The LaunchPad is equipped with a single MCAN Transceiver (TCAN1044VDRBTQ1) that is connected to the MCAN0 interface of the AM263x SoC. The MCAN Transceiver has two power inputs, VIO is the transceiver 3.3V system level shifting supply voltage and VCC is the transceiver 5 V supply voltage. The SoC CAN data transmit data input is mapped to TXD of the transceiver and the CAN receive data output of the transceiver is mapped to the MCAN RX signal of the SoC.

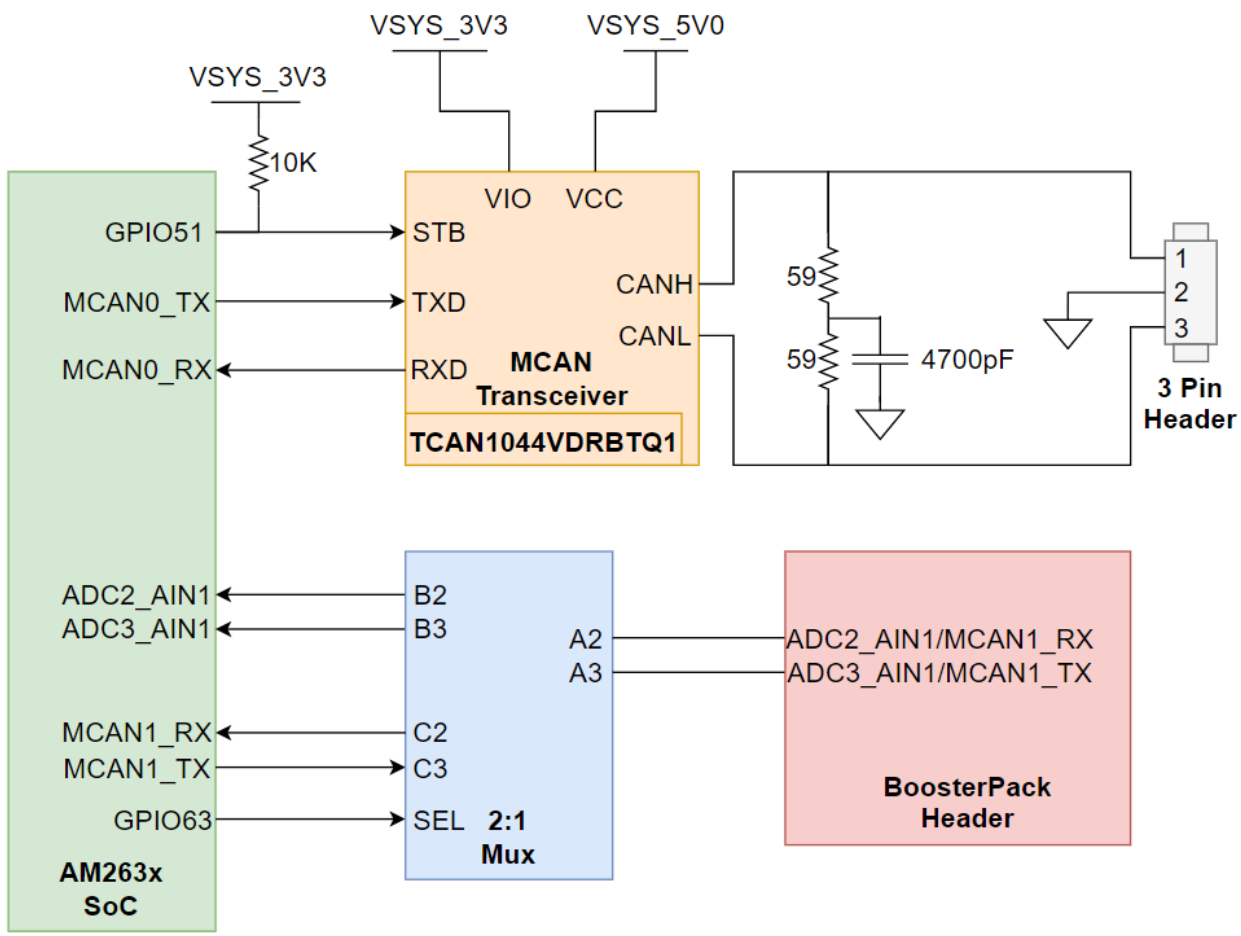


Figure 4-14. MCAN Transceiver and BoosterPack Header

The system has a 120Ω split termination on the CANH and CANL signals to improve EMI performance. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

The low and high level CAN bus input output lines are terminated to a three pin header.

The standby control signal is an AM263x SoC GPIO signal. The STB control input has a pull up resistor that is used to have the transceiver be in low-power standby mode to prevent excessive system power. Below is a table that shows the operating modes of the MCAN transceiver based on the STB control input logic.

Table 4-10. MCAN Transceiver Operating Modes

STB	Device Mode	Driver	Receiver	RXD Pin
High	Low current standby mode with bus wake-up	Disabled	Low-power receiver and bus monitor enable	High (recessive) until valid WUP is received
Low	Normal Mode	Enabled	Enabled	Mirrors bus state

There is a separate MCAN1 interface that is not connected to a transceiver. MCAN1 is routed to the BoosterPack Header via a 2:1 Mux. The Mux selects whether ADC inputs or MCAN signals are mapped to the BoosterPack Header.

Table 4-11. MCAN BoosterPack Mux

GPIO63	Condition	Function of Mux
LOW	ADC Inputs Selected	Port A ↔ Port B
HIGH	MCAN TX/RX Selected	Port A ↔ Port C

4.12 FSI

The AM263x LaunchPad supports a fast serial interface by terminating the SoC signals to a 10 pin header. The interface has two lines of data and a clock line for both the receive and transmit signals. The 10 pin header is connected to the 3.3V System voltage supply.

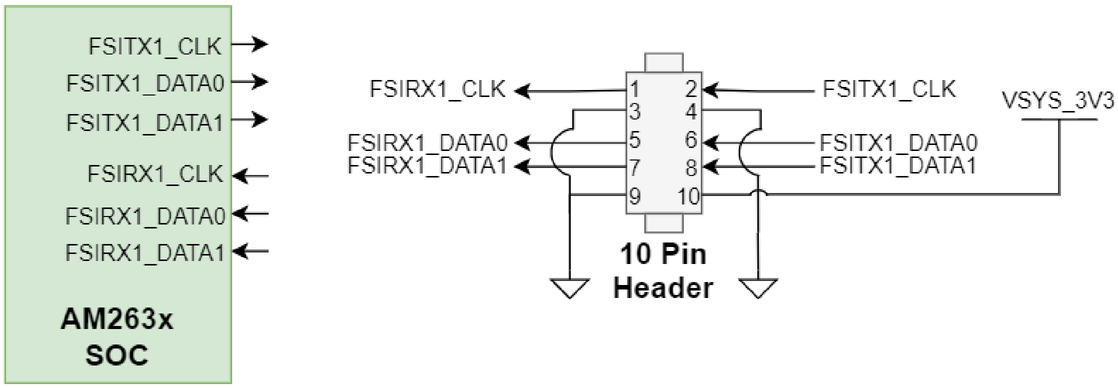


Figure 4-15. FSI 10 Pin Header

4.13 JTAG

The AM263x LaunchPad includes an XDS110 class on-board emulator. The LaunchPad includes all circuitry needed for XDS110 emulation. The emulator uses a USB2.0 micro-b connector to interface the USB 2.0 signals that are created from the UART-USB bridge. The VBUS power from the connector is used to power the emulator circuit so that the connection to the emulator is not lost when power to the LaunchPad is removed. For more information on the XDS110 and the UART-USB bridge refer to UART.

The XDS110 controls two power status LEDs. For more information on the Power Status LEDs refer to Power Status LEDs

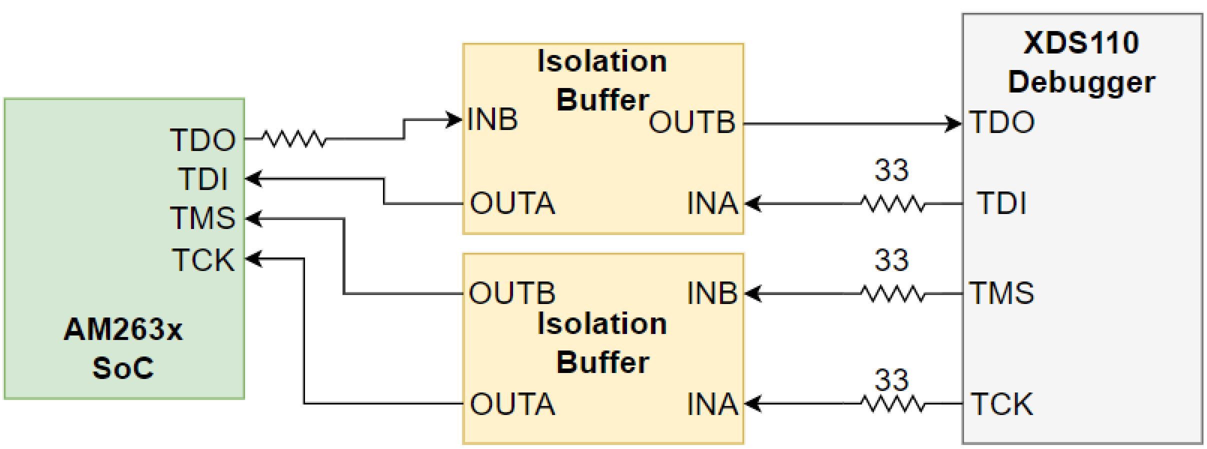


Figure 4-16. JTAG Interface to XDS110

4.14 Test Automation Header

The AM263x LaunchPad supports a 40 pin test automation header that allows an external controller to manipulate basic operations such as power down, PORz, warm reset, and bootmode control.

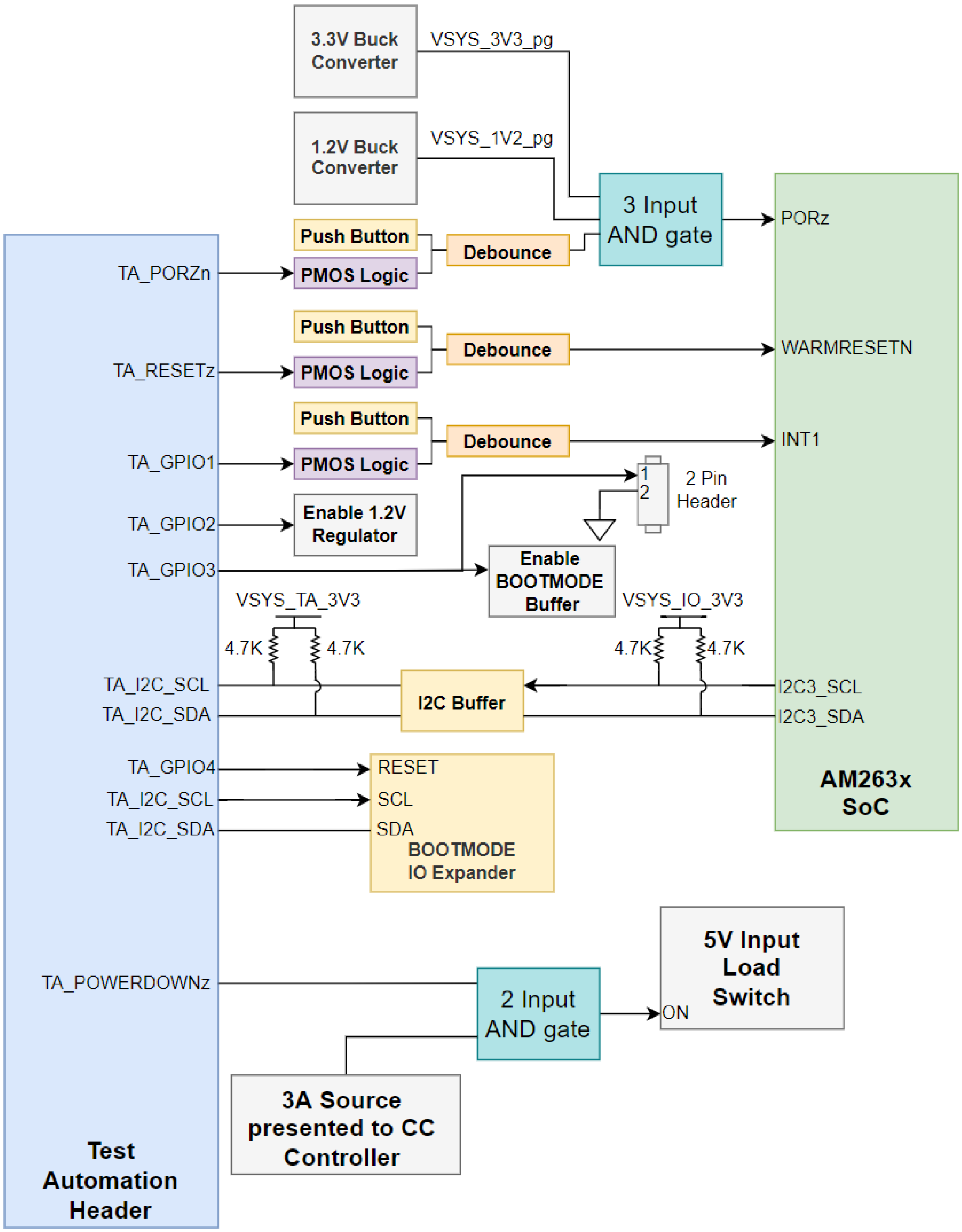


Figure 4-17. Test Automation Header

The Test Automation Circuit is powered by a dedicated 3.3V power supply (VSYS_TA_3V3) which is generated by a 5V to 3.3V buck regulator (TPS62177DQCR).

The AM263x SoC I2C3 instance is connected to both the Test Automation Header and the bootmode IO expander (TCA6408ARGTR).

The following table details the Test Automation GPIO mapping:

Table 4-12. Test Automation GPIO Mapping

Signal Name	Description	Direction
TA_POWERDOWN	when logic low, disables the 3.3V buck regulator (TPS62913RPUR) that is used in the first stage of DC/DC conversion	Output
TA_PORZn	when logic low, connects the PORz signal to ground due to the PMOS V_GS being less than zero creating a power on reset to the MAIN domain	Output
TA_RESETz	when logic low, connects the WARMRESETn signal to ground due to the PMOS V_GS being less than zero creating a warm reset to the MAIN domain	Output
TA_GPIO1	when logic low, connects the INTn signal to ground due to the PMOS V_GS being less than zero creating an interrupt to the SoC	Output
TA_GPIO2	when logic low, disables the 1.2V buck regulator (TPS62913RPUR)	Output
TA_GPIO3	when logic low, disables the bootmode buffer output enable	Output
TA_GPIO4	Reset signal for Bootmode IO Expander (TCA6408ARGTR)	Output

4.15 LIN

The AM263x LaunchPad supports Local Interconnect Network communication with two LIN instances mapped to the BoosterPack header.

Note

The AM263x does **not** have an on-board LIN Transceiver

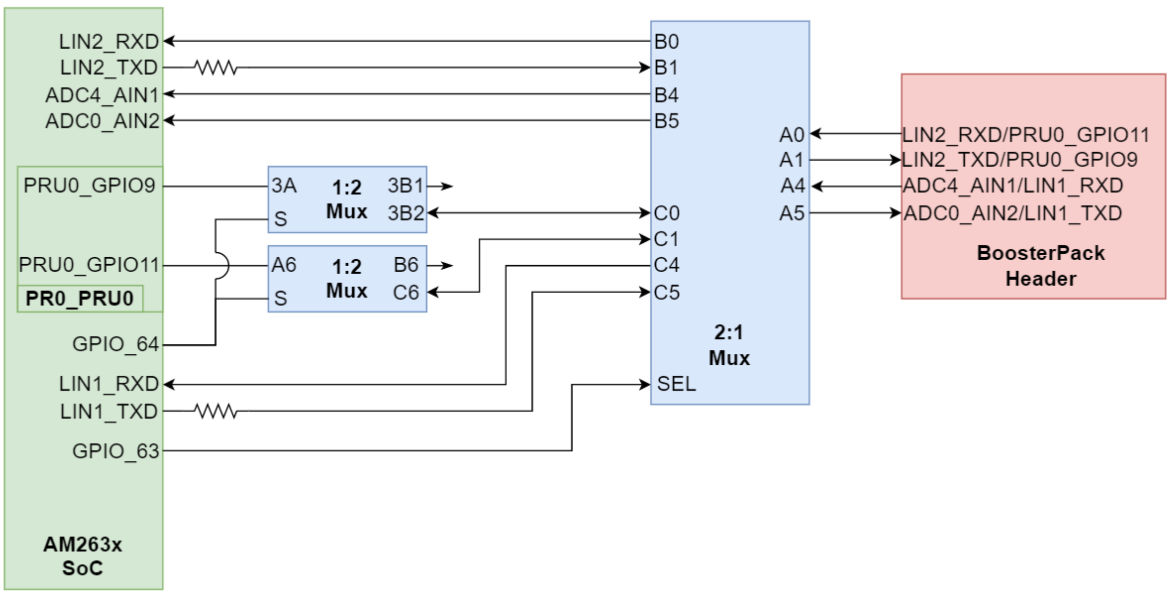


Figure 4-18. LIN Instances to BoosterPack Header

Both LIN instances are mapped to the alternate BoosterPack function 2:1 Mux. The alternate BoosterPack function mux also has mappings for ADC inputs and PRU0 GPIO signals.

Table 4-13. LIN 2:1 Mux

GPIO_64	GPIO_63	Function of 2:1 Mux	Signals to BP Header
HIGH	LOW	Port A ↔ Port B	LIN2TX/RX, ADC4_AIN1, ADC0_AIN2
HIGH	HIGH	Port A ↔ Port C	PRU GPIO11/9, LIN1TX/RX
LOW	LOW	Port A ↔ Port B	LIN2TX/RX, ADC4_AIN1, ADC0_AIN2
LOW	HIGH	Port A ↔ Port C	NC, NC, LIN1 TX/RX

4.16 MMC

The AM263x LaunchPad provides a micro SD card interface that is mapped to the MMC0 instance of the AM263x SoC.

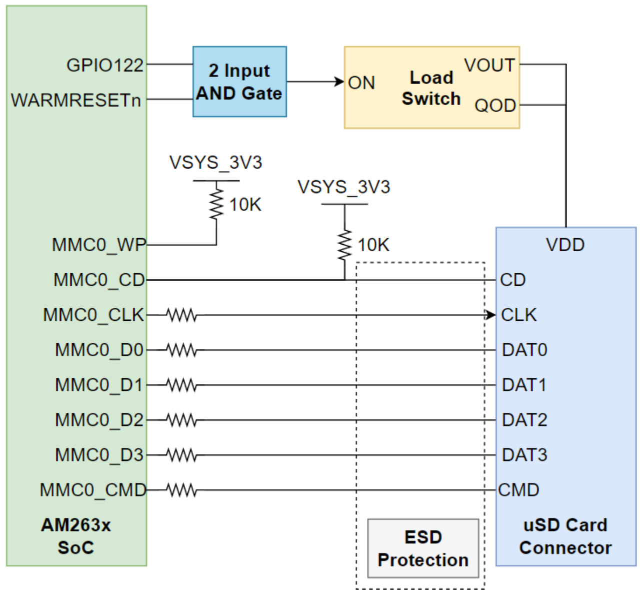


Figure 4-19. Micro SD Card Connector

A load switch (TPS22918DBVR) is used to power the micro SD card connector. The load switch is driven by the output of a 2-input AND gate between WARMRESETn and the SD Card enable GPIO (GPIO122) in order to power cycle the card upon reset. The load switch uses quick output discharge (QOD) to ensure that the supply voltage reaches <10% of nominal value during reset.

Inline ESD protection is provided for the MMC signals in the form of a six channel transient voltage suppressor device (TPD6E001RSER) and two channel transient voltage suppressor device (TPD2E001DRLR).

The Write Protect (WP) and Card Detect (CD) signals of the SD card connector are pulled up to the 3.3V System voltage supply.

A series termination resistor is provided for all MMC signals besides CD.

4.17 ADC and DAC

The AM263x LaunchPad maps 18 ADC inputs to the BoosterPack header. All of the ADC inputs that are used in the LaunchPad are ESD protected.

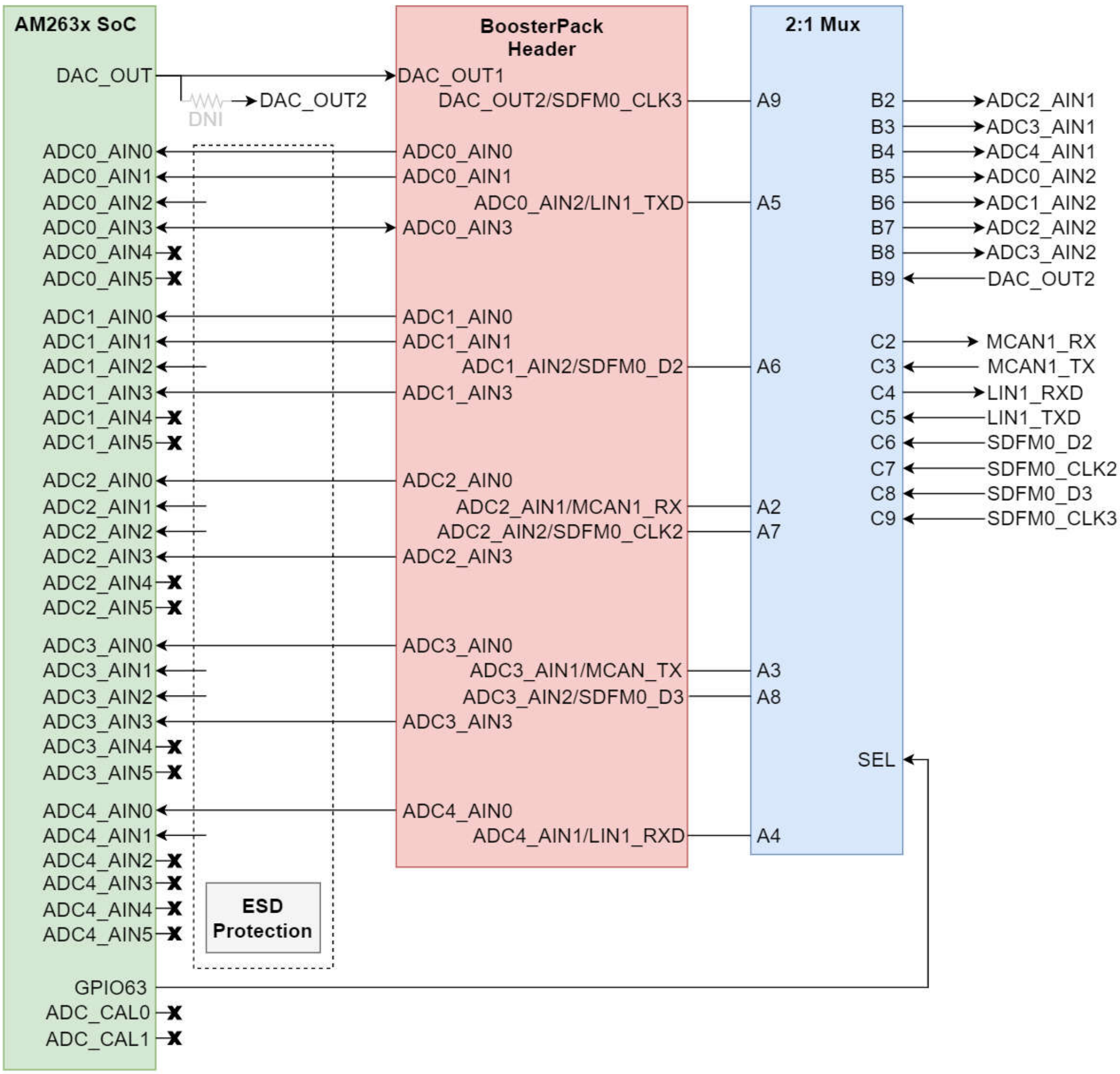


Figure 4-20. ADC/DAC Signal Pathing

Seven of the ADC inputs and one instance of the DAC_OUT signal is routed to a 2:1 mux (TS3DDR3812RUAR) to offer alternate BoosterPack functionality. The select line of the mux is driven by an AM263x SoC GPIO signal.

Table 4-14. ADC BoosterPack Mux

GPIO63	Condition	Funciton of Mux
LOW	ADC input/DAC_OUT Selected	Port A ↔ Port B
HIGH	Alternate BP functionality Selected	Port A ↔ Port C

The ADC and DAC require a voltage reference. The AM263x LaunchPad has two switches that allow the user to switch between the DAC and ADC VREF source.

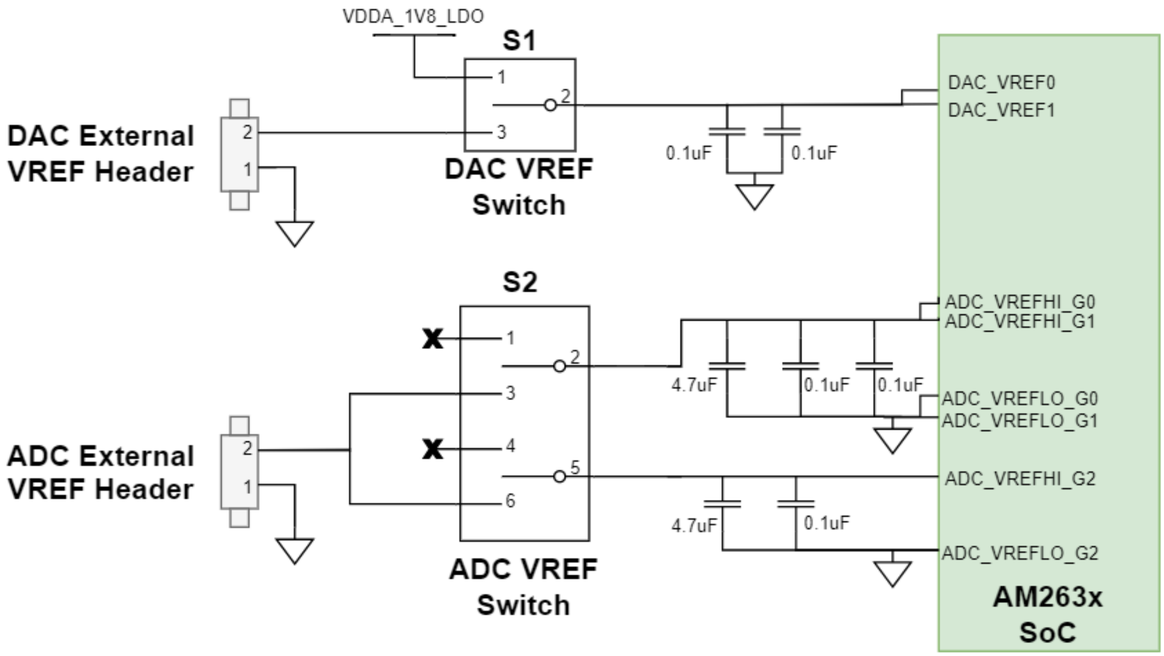


Figure 4-21. ADC and DAC VREF Switches

The DAC VREF Switch (S1) is a single pole double throw switch that controls the input of the ADC VREF inputs of the AM263x SoC.

Table 4-15. DAC VREF Switch

DAC VREF Switch Position	Reference Selection
Pin 1-2	AM263x on-die LDO
Pin 2-3	External DAC VREF Header

The ADC VREF Switch (S2) contains two single pole double throw switch that controls the input of the ADC VREF inputs of the AM263x SoC.

Table 4-16. ADC VREF Switch

ADC VREF Switch Position	Reference Selection
Pin 1-2	OPEN- Allow for reference to be AM263x on-die LDO reference
Pin 2-3	External ADC VREF Header
Pin 4-5	OPEN- Allow for reference to be AM263x on-die LDO reference
Pin 5-6	External ADC VREF Header

4.18 EQEP and SDFM

The AM263x LaunchPad internally muxes the eQEP and SDFM signals. The eQEP0 and SDFM1 instances of the AM263x are terminated to two headers (J24, J15). The eQEP2 and SDFM2 instances of the AM263x are terminated to two headers (J25, J16).

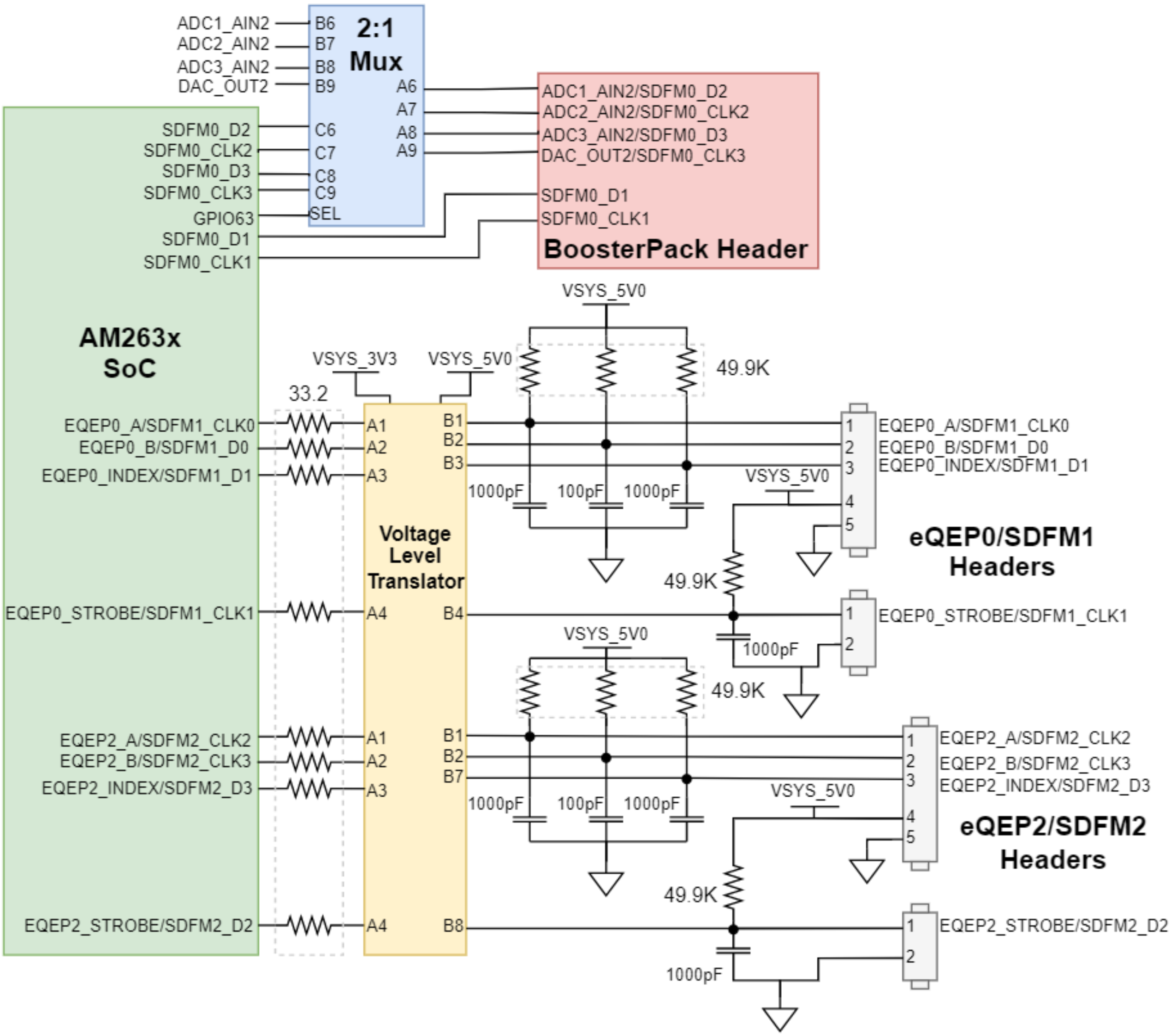


Figure 4-22. EQEP and SDFM Signal Mapping

All eQEP signals have series termination resistors between the AM263x SoC and the Voltage Level Translator (TXB0108RGYR). The voltage level shifter is responsible for translating the 3.3 V to 5 V.

SDFM0 is mapped to the BoosterPack Header rather than an independent header. Four of the SDFM0 signals are routed through a 2:1 Mux to offer alternate BoosterPack functionality. The select line of the mux is driven by an AM263x SoC GPIO signal.

Table 4-17. SDFM0 Mux

GPIO63	Condition	Function of Mux
LOW	Alternate BP functionality Selected	Port A ↔ Port B
HIGH	SDFM0 Selected	Port A ↔ Port C

4.19 EPWM

The AM263x LaunchPad maps 20 PWM channels (10 PWM_A/B pairs) to the BoosterPack Header. Each EPWM signal has a series termination resistor. For the mapping of each EPWM signal refer to Pinmux Mapping

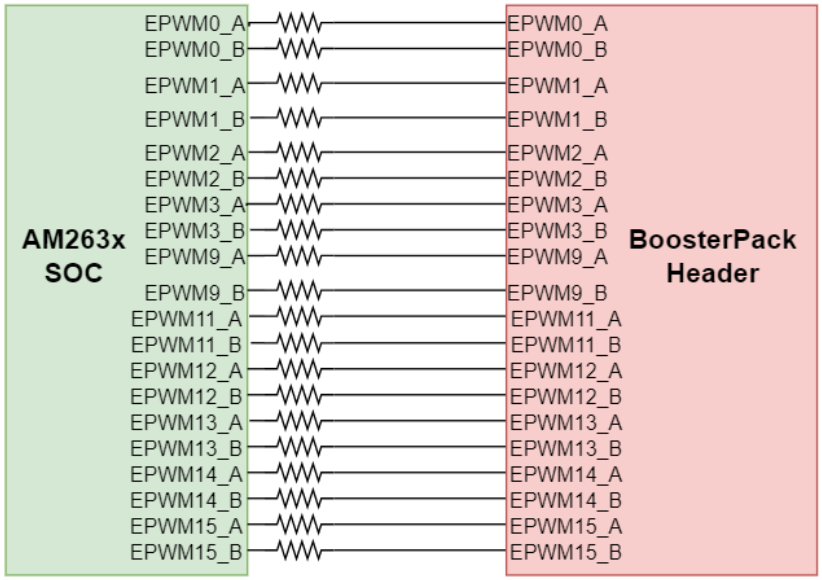


Figure 4-23. EPWM Signal Mapping to BoosterPack Header

4.20 BoosterPack Headers

Note

Confirm which EVM revision is in use before checking the BoosterPack pinout. There are slight differences between Rev E2 and A, which are detailed in Section 5.1.

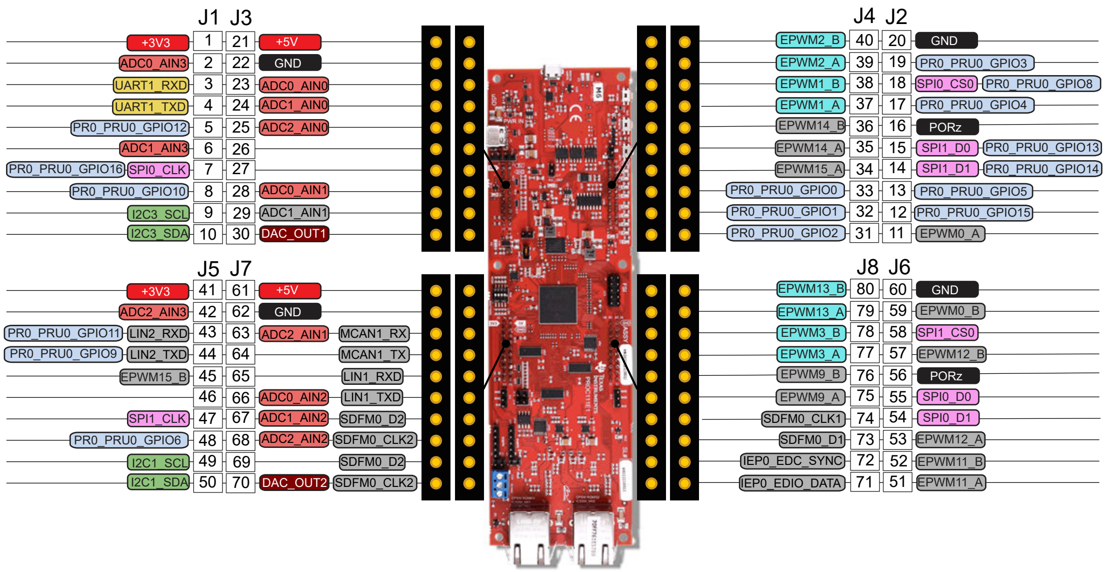


Figure 4-24. AM263x LaunchPad - Rev E2 BoosterPack Pinout

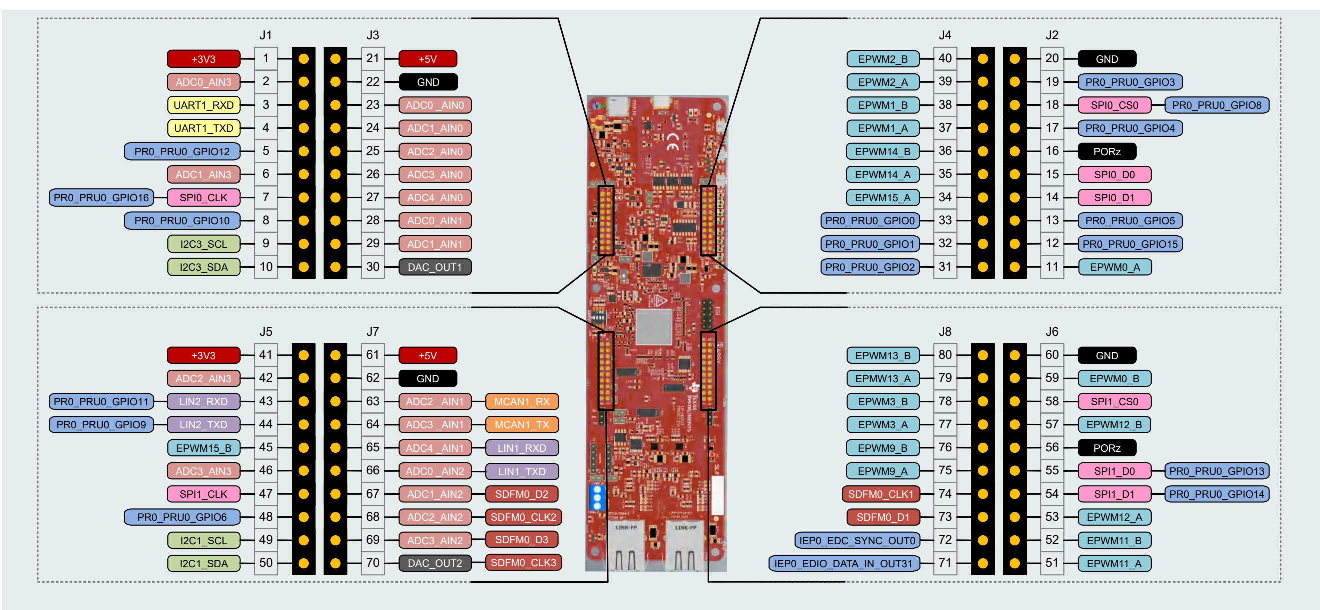


Figure 4-25. AM263x LaunchPad - Rev A BoosterPack Pinout

Note

This pinout represents the default signals mapped to the BoosterPack Header. Additional signal options for each header are available through Pinmuxing. Two signals for one pin represents an externally muxed option

Note

A gray background for a signal on the pinout shows that the signal does not follow the BoosterPack Standard pinout.

The AM263x LaunchPad supports two fully independent BoosterPack XL connectors. BoosterPack site #1 (J1/J3, J2/J4) is located in between the SoC and the micro-B USB Connector. BoosterPack site #2 (J5/J7, J6/J8) is located in between the SoC and the RJ45 connectors. Each GPIO has multiple functions available through the GPIO mux. The signals connected from the SoC to the BoosterPack headers include:

- Various ADC inputs
- DAC Out
- UART1
- Various GPIO signals
- SPI0 and SPI1
- I2C1 and I2C3
- Various EPWM Channels
- LIN1 and LIN2
- MCAN1
- SDFM0

4.21 Pinmux Mapping

The various pinmux options for the BoosterPack connector pins are given below.

Note

The signals on pins J2.14, J2.15, J6.54, J6.55 are dependent on the EVM revision

Table 4-18. Pinmux Legend

Default signal for BP Header	Muxed alternative signal	External MUX for alternate signal options

Table 4-19. Pinmux Options for J1

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9
J1.1	3V3									
J1.2	ADC0_AIN3									
J1.3	UART1_RXD	LIN1_RXD				EPWM16_A	GPMC0_AD6	GPIO75		
J1.4	UART1_TXD	LIN1_TXD				EPWM16_B	GPMC0_AD7	GPIO76		
J1.5	PR0_PRU0_GPIO12		RMII2_TXD1	RGMII2_TD1	MII2_TXD1	EPWM28_B	GPMC0_A8	GPIO100		
J1.6	ADC1_AIN3									
J1.7	SPI0_CLK	UART3_TXD	LIN3_TXD				FSITX0_CLK	GPIO12		
	PR0_PRU0_GPIO16			RGMII2_TXC	MII2_TXCLK	EPWM27_A	GPMC0_A5	GPIO97		
J1.8	PR0_PRU0_GPIO10		RMII2_CRS_DV	PR0_UART0_RTSn	MII2_CRS	EPWM23_A	GPMC0_WAIT0	GPIO89		
J1.9	EPWM8_B	UART4_RXD	I2C3_SCL				FSITX2_DATA0	GPIO60		
J1.10	EPWM8_A	UART4_TXD	I2C3_SDA				FSITX2_CLK	GPIO59		

Table 4-20. Pinmux Options for J2

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9
J2.11	EPWM0_A							GPIO43		
J2.12	PR0_PRU0_GPIO15		RMII2_TX_EN	RGMII2_TX_CTL	MII2_TX_EN	EPWM27_B	GPMC0_A6	GPIO98		
J2.13	PR0_PRU0_GPIO5		RMII2_RX_ER		MII2_RX_ER	EPWM22_A	GPMC0_DIR	GPIO87		
J2.14 Rev A	SPI0_D1						FSITX0_DATA1	GPIO14		
J2.14 Rev E1/E2	SPI1_D1	UART5_RXD				XBAROUT4	FSIRX0_DATA1	GPIO18		
	PR0_PRU0_GPIO14			RGMII2_TD3	MII2_TXD3	EPWM29_B	GPMC0_A10	GPIO102		
J2.15 Rev A	SPI0_D0						FSITX0_DATA0	GPIO13		
J2.15 Rev E1/E2	SPI1_D0	UART5_TXD				XBAROUT3	FSIRX0_DATA0	GPIO17		
	PR0_PRU0_GPIO13			RGMII2_TD2	MII2_TXD2	EPWM29_A	GPMC0_A9	GPIO101		
J2.16	PORz									
J2.17	PR0_PRU0_GPIO4			RGMII2_RX_CTL	MII2_RXDV	EPWM24_B	GPMC0_A0	GPIO92		
J2.18	SPI0_CS0	UART3_RXD	LIN3_RXD					GPIO11		
	PR0_PRU0_GPIO8					EPWM23_B	GPMC0_WPn	GPIO90		
J2.19	PR0_PRU0_GPIO3			RGMII2_RD3	MII2_RXD3	EPWM26_B	GPMC0_A4	GPIO96		
J2.20	GND									

Table 4-21. Pinmux Options for J3

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9
J3.21	5V									
J3.22	GND									
J3.23	ADC0_AIN0									
J3.24	ADC1_AIN0									
J3.25	ADC2_AIN0									
J3.26	ADC3_AIN0									
J3.27	ADC4_AIN0									
J3.28	ADC0_AIN1									
J3.29	ADC1_AIN1									
J3.30	DAC_OUT									

Table 4-22. Pinmux Options for J4

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9
J4.31	PR0_PRU0_GPIO2			RGMII2_RD2	MII2_RXD2	EPWM26_A	GPMC0_A3	GPIO95		
J4.32	PR0_PRU0_GPIO1		RMII2_RXD1	RGMII2_RD1	MII2_RXD1	EPWM25_B	GPMC0_A2	GPIO94		
J4.33	PR0_PRU0_GPIO0		RMII2_RXD0	RGMII2_RD0	MII2_RXD0	EPWM25_A	GPMC0_A1	GPIO93		
J4.34	EPWM15_A	UART5_TXD	MII1_COL				GPMC0_AD4	GPIO73		
J4.35	EPWM14_A	UART1_DSRn					GPMC0_AD2	GPIO71		
J4.36	EPWM14_B		MII1_RX_ER				GPMC0_AD3	GPIO72		
J4.37	EPWM1_A							GPIO45		
J4.38	EPWM1_B							GPIO46		
J4.39	EPWM2_A							GPIO47		
J4.40	EPWM2_B							GPIO48		

Table 4-23. Pinmux Options for J5

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9
J5.41	3V3									
J5.42	ADC2_AIN3									
J5.43	LIN2_RXD	UART2_RXD	SPI2_D0					GPIO21		
	PR0_PRU0_GPIO11		RMII2_TXD0	RGMII2_TD0	MII2_TXD0	EPWM28_A	GPMC0_A7	GPIO99		
J5.44	LIN2_TXD	UART2_TXD	SPI2_D1					GPIO22		
	PR0_PRU0_GPIO9			PR0_UART0_CTSn	MII2_COL	EPWM22_B	GPMC0_CLK	GPIO88		
J5.45	EPWM15_B	UART5_RXD	MII1_CRS				GPMC0_AD5	GPIO74		
J5.46	ADC3_AIN3									
J5.47	SPI1_CLK	UART4_RXD	LIN4_RXD			XBAROUT2	FSIRX0_CLK	GPIO16		
J5.48	PR0_PRU0_GPIO6		RMII2_REF_CLK	RGMII2_RXC	MII2_RXCLK	EPWM24_A	GPMC0_CSn1	GPIO91		
J5.49	I2C1_SCL		SPI3_CS0			XBAROUT7		GPIO23		
J5.50	I2C1_SDA		SPI3_CLK			XBAROUT8		GPIO24		

Table 4-24. Pinmux Options for J6

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9
J6.51	EPWM11_A	UART2_CTSn					GPMC0_CLKLB	GPIO65		
J6.52	EPWM11_B	UART3_RTSn					GPMC0_OEn_REn	GPIO66		
J6.53	EPWM12_A	UART3_CTSn	SPI4_CS1				GPMC0_WEn	GPIO67		
J6.54 Rev A	SPI1_D1	UART5_RXD				XBAROUT4	FSIRX0_DATA1	GPIO18		
	PR0_PRU0_GPIO14			RGMII2_TD3	MII2_TXD3	EPWM29_B	GPMC0_A10	GPIO102		
J6.54 Rev E1/E2	SPI0_D1						FSITX0_DATA1	GPIO14		
J6.55 Rev A	SPI1_D0	UART5_TXD				XBAROUT3	FSIRX0_DATA0	GPIO17		
	PR0_PRU0_GPIO13			RGMII2_TD2	MII2_TXD2	EPWM29_A	GPMC0_A9	GPIO101		
J6.55 Rev E1/E2	SPI0_D0						FSITX0_DATA0	GPIO13		
J6.56	PORz									
J6.57	EPWM12_B	UART1_DCDn					GPMC0_CSn0	GPIO68		
J6.58	SPI1_CS0	UART4_TXD	LIN4_TXD			XBAROUT1		GPIO15		
J6.59	EPWM0_B							GPIO44		
J6.60	GND									

Table 4-25. Pinmux Options for J7

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9
J7.61	5V									
J7.62	GND									
J7.63	ADC2_AIN1									
	MCAN1_RX	SPI4_D0						GPIO9		
J7.64	ADC3_AIN1									
	MCAN1_TX	SPI4_D1						GPIO10		
J7.65	ADC4_AIN1									
	LIN1_RXD	UART1_RXD	SPI2_CS0			XBAROUT5		GPIO19		
J7.66	ADC0_AIN2									
	LIN1_TXD	UART1_TXD	SPI2_CLK			XBAROUT6		GPIO20		
J7.67	ADC1_AIN2									
	UART5_RXD							GPIO127	SDFM0_D2	
J7.68	ADC2_AIN2									
	UART5_TXD					I2C3_SCL	GPMC0_ADVn_ALE	GPIO126	SDFM0_CLK2	
J7.69	ADC3_AIN2									
	MCAN3_RX							GPIO129	SDFM0_D3	
J7.70	DAC_OUT									
	MCAN3_TX	UART5_RXD						GPIO128	SDFM0_CLK3	

Table 4-26. Pinmux Options for J8

Pin#	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9
J8.71	PR0_PRU1_GPIO18		UART3_TXD	PR0_IEP0_EDIO_DATA_IN_OUT31	TRC_CTL	XBAROUT14	GPMC0_WAIT1	GPIO120		EQEP1_B
J8.72	PR0_PRU1_GPIO19		UART3_RXD	PR0_IEP0_EDC_SYNC_OUT0	TRC_CLK	XBAROUT13		GPIO119		EQEP1_A
J8.73	PR0_PRU1_GPIO17		UART5_CTSn	PR0_IEP0_EDIO_DATA_IN_OUT30				GPIO125	SDFM0_D1	
J8.74	PR0_PRU1_GPIO7	CPTS0_TS_SYNC	UART5_RTSn	PR0_IEP0_EDC_SYNC_OUT1		I2C3_SDA		GPIO124	SDFM0_CLK1	
J8.75	EPWM9_A						FSITX2_DATA1	GPIO61		
J8.76	EPWM9_B	UART1_RTSn					FSIRX2_CLK	GPIO62		
J8.77	EPWM3_A							GPIO49		
J8.78	EPWM3_B							GPIO50		
J8.79	EPWM13_A	UART1_RIn					GPMC0_AD0	GPIO69		
J8.80	EPWM13_B	UART1_DTRn					GPMC0_AD1	GPIO70		

Table 4-27. Pinmux Legend

Default signal for BP Header	Muxed alternative signal	External MUX for alternate signal options

5 EVM Revision Design Changes

5.1 Rev A Design Changes

The LP-AM263 design changes between Revision E2 → A are detailed below:

1. BoosterPack Header Changes

Table 5-1. LP-AM263 Rev E2 → A BoosterPack Pinout Comparison

BoosterPack Header Pin	Rev E2	Rev A
J2.15	SPI1_D0 / PR0_PRU0_GPIO13	SPI0_D0
J2.14	SPI1_D1 / PR0_PRU0_GPIO14	SPI0_D1
J6.55	SPI0_D0	SPI1_D0 / PR0_PRU0_GPIO13
J6.54	SPI0_D1	SPI1_D1 / PR0_PRU0_GPIO14

2. VPP FET Switch Support
    a. LDO U53 added to supply 1V7 to AM2634 VPP pin for E-fusing
3. ADC Filter Capacitors
    a. ADC input capacitor values changed from 0.1uF to 330pF
    b. Capacitors moved to ADC side of muxed ADC/MCAN signals

6 Hardware Design Files

1. Download the zip file containing the latest design files for the EVM, click the following link: https://www.ti.com/lit/zip/sprr452.
2. Included in the zip file are Altium schematics, the PCB layout file, and the BOM.

7 References

7.1 Reference Documents

In addition to this document, the following references are available for download at www.ti.com.

- *AM263P4 Sitara™ Microcontrollers*
- *AM263Px Sitara™ Microcontrollers Data Sheet*
- *AM263Px Sitara™ Microcontrollers Technical Reference Manual*
- *AM263Px Sitara™ Microcontrollers Silicon Errata*
- *Texas Instruments Code Composer Studio*
- *Updating XDS110 Firmware*
  – To find the serial number, only follow steps 1 and 2 of updating XDS110 firmware

7.2 Other TI Components Used in This Design

This LaunchPad uses various other TI components for its functions. A consolidated list of these components with links to their TI data sheets is shown below.

- *TUSB320USB Type-C Configuration Channel Logic and Port Controller*
- *TPD4E02B04 4-Channel ESD Protection Diode for USB Type-C*
- *TPS22965x-Q1 5.5-V, 4-A, 16-mΩ On-Resistance Load Switch*
- *TPS6291x 3-V to 17-V, 2-A/3-A Low Noise and Low Ripple Buck Converter*
- *TPS748 1.5-A Low-Dropout Linear Regulator*
- *TCA6408A Low-Voltage 8-Bit I 2C and SMBus I/O Expander*
- *SN74AVC4T245 Dual-Bit Bus Transceiver with Configurable Voltage Translation*
- *TPS22918-Q1, 5.5-V, 2-A, 52-mΩ On-Resistance Load Switch*
- *TPD6E001 Low-Capacitance 6-Channel ESD-Protection for High-Speed Data Interfaces*
- *XDS110 JTAG Debug Probe*
- *TS5A23159 1-Ω 2-Channel SPDT Analog Switch*
- *TCAN1044V-Q1 Automotive Fault-Protected CAN FD Transceiver*
- *DP83869HM High Immunity 10/100/1000 Ethernet Physical Layer Transceiver*
- *TS3DDR3812 12-Channel, 1:2 MUX/DEMUX Switch for DDR3 Applications*
- *TCA9617B Level-Translating I2C Bus Repeater*
- *SN74CB3Q3257 4-Bit 1-of-2 FET Multiplexer/Demultiplexer*
- *TPIC2810 8-Bit LED Driver with I2C Interface*
- *TPS796xx 1-A Low-Dropout Linear Regulators*
- *TXB0108 8-Bit Bidirectional Voltage-Level Translator with Auto-Direction Sensing*
- TCA6416ARTWR 16-bit translating 1.65- to 5.5-V I2C/SMBus I/O expander

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8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from September 30, 2023 to May 30, 2025 (from Revision D (September 2023) to Revision E (May 2025)) **Page**

- [Important Usage Notes] Removed MDIO M1 sticker note as Rev E1 boards are no longer in circulation....... 4
- [BoosterPack Headers] Added Rev A pinout image...46
- [Pinmux Mapping] Added EVM revision details..48
- Added IO Expander to the list..54