User's Guide
AM64x and AM243x BGA Escape Routing

TEXAS INSTRUMENTS

ABSTRACT

This user's guide provides a sample PCB escape routing for the AM64x and AM243x System-on-Chip (SoC). The SoCs have multiple functions assigned to each pin making it impossible to provide an escape for all permutations of pinmux definitions. The escape presented here is based on the AM64x and AM243x GP EVMs and the pinmux defined for that design.

The strategy provided within is designed to help ensure a successful escape. Care must be taken to escape the signals with the most layout constraints early in the routing process. This document does not include those constraints. For additional information on routing these signals, see the *High-Speed Interface Layout Guidelines*. Care must also be taken to ensure that a robust power delivery network is provided. For additional information, see the *Sitara™ Processor Power Distribution Networks: Implementation and Analysis*.

> **Note**
> Due to package differences, not all interfaces may be available in all form factors, this document is intended to provide a superset overview of escape routing. Consult the processor datasheet for package differences.

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1 Stackup

The PCB layout designer must balance many different requirements when starting a PCB layout. The first is the board stackup. The AM64x and AM243x devices have a 17.2-mm × 17.2-mm package which has a 0.80-mm pitch ball array of 21×21. To minimize cost, this ball grid is a solid array. Due to the number of rows of signal balls around the periphery, designs must have two routing layers, not counting the top and bottom layers, which can also contain some signal routes. Also, due to the number of power supply rails, there must be two layers dedicated for power planes. Ground planes must be added adjacent to the power planes and adjacent to the outer layers for shielding and controlled impedance routing. High-speed interfaces such as the SERDES and the DDR require ground planes for impedance matching. Due to the higher speeds, ground layers both above and below the DDR signals are recommended. The AM64 GP EVM design connected all of the signal balls and included the additional ground planes. The routing was achieved with 10 layers as shown in Table 1-1.

Table 1-1. PCB Layer Stack-up

PCB Layer	Layer Routing, Planes or Pours
Layer 1	Component pads and signal routing
Layer 2	Ground
Layer 3	Signal routing[1]
Layer 4	Ground
Layer 5	Power
Layer 6	Power
Layer 7	Ground
Layer 8	Signal routing[1]
Layer 9	Ground
Layer 10	Component pads (including most decoupling) and signal routing

(1)   Bracketing the signal routing between two ground planes eliminates broadside coupling to prevent crosstalk problems.

A 10-layer stack-up similar to the one above is needed for relatively dense PCBs. Alternately, the layer count can be reduced, assuming one or more of the following exist:

- The PCB is not crowded around the AM64x or AM243x device. This allows for more routing away from the device on the top and bottom layers, which can reduce layer congestion.
- Many of the signal balls are unused. Many designs do not use all of the interfaces, resulting in unused signal balls. This also reduces routing congestion.
- The PCB layout team has time to carefully place the routes. This can be very time consuming.

It is not acceptable to violate routing rules simply to save money on reduced PCB layers or due to limited routing time. All requirements must still be met. Also, creative routing increases design validation time, both in simulation and bench testing. This can be minimized if the layout is similar to one of the AM64x EVM designs.

The AM64x EVM is implemented in a 10-layer stack-up, similar to the one described in Table 1-1. This design has nearly every signal ball routed to circuitry or a connector. This drives the requirement for the full number of layers. Additionally, this board is designed for optimum signal integrity on the high-speed interfaces while limiting the board size. The AM64x EVM is implemented without a High Density Interconnect (HDI) and does not use microvias. All vias on the AM64x EVM pass completely through the board. This complicates the escape from the BGA.

2 Floorplan Component Placement

Optimum trace routing will have routes as short as possible with a minimum of cross-over. This requires careful placement of the components around the SoC. Figure 2-1 shows the default arrangement of the signal balls and the power and ground balls. Some of the interfaces can move to other locations due to pin multiplex choices, and there are other interfaces not listed that are exposed through pin multiplex choices. The PCB layout team must analyze the locations of the interfaces used and the associated components or connectors.
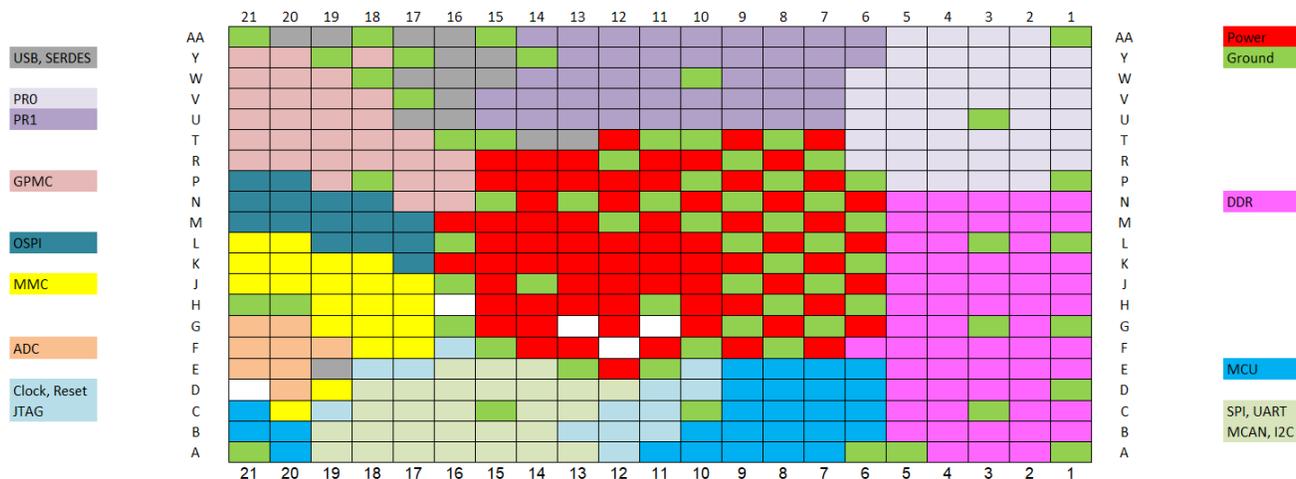
Figure 2-1. AM64x Floorplan

3 Critical Interfaces Impact Placement

Placement of the SoC and some of the components or connectors is also dictated by some of the highest performance interfaces. Additionally, due to the PCB losses at multi-gigabit rates, there are routing distance limits that may also limit component placement.

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4 Route Critical Interfaces First

As indicated above, critical interfaces affect component placement options. When routing begins, these critical interfaces must be routed first. The design team must establish a priority for the different interfaces. Those with higher priority must be completed before implementing those of lower priority. PCB layout teams often waste considerable effort ripping up and re-routing traces for lower priority interfaces when deficiencies are found in the routing of more critical interfaces. Always complete routing for the critical interfaces first.

Table 4-1 lists a recommended priority order for interfaces contained on the AM64x and AM243x families of devices. Individual design requirements may cause this list to change, but this provides a good baseline.

Table 4-1. Routing Priority

| Interface	Routing Priority
PCIe/USB3	10 (Highest Priority)
DDR4/LPDDR4	9
USB2, OSPI	8
Power distribution	7
RGMII	6
QSPI	6
eMMC	5
Clocks	5
MII / RMII	4
SPI	4
Motor control	4
Analog audio	3
GPMC	2
GPIO	1
UART	1
I2C	1 (Lowest Priority)

The placement of most of these should appear obvious. The multi-gigabit SERDES interfaces are the most critical due to their data rate and loss concerns. PCIe is at the top because it is very sensitive to PCB losses. The limited length for these routes might affect the PCB placement of the PCIe connector and the AM64x device. PCIe signals are found on the outer rings of the BGA footprint, allowing the traces to escape from the BGA without vias.

The asynchronous and low-speed interfaces are at the bottom. This leaves the synchronous and source-synchronous interfaces on the top, ordered by data rate. The one surprise may be power distribution. Power distribution is often left to last, but this can then result in poor decoupling performance or current starvation and excessive power supply noise due to insufficient copper to carry the power and ground currents. **Space for copper and decoupling must be allocated before routing the middle and low priority interfaces.**

5 Route SERDES Interfaces First

The previous section highlighted priorities for the PCB routing. The BGA ball map is also arranged to support routing the highest priority interfaces first. You will notice that most of the PCIe/USB3 SERDES interfaces are located on the outer two rings. The transmit pair should be routed away from the SoC on the top layer leaving a gap without blocking vias. The receive pair requires vias to escape as a differential pair on the bottom or on an interior layer. For the routing of the serdes signals on the AM64x EVM on the top layer and on the SIG2 layer, see Figure 5-1. Wide traces can limit the signal loss, but complicate the impedance requirements, which must be met.
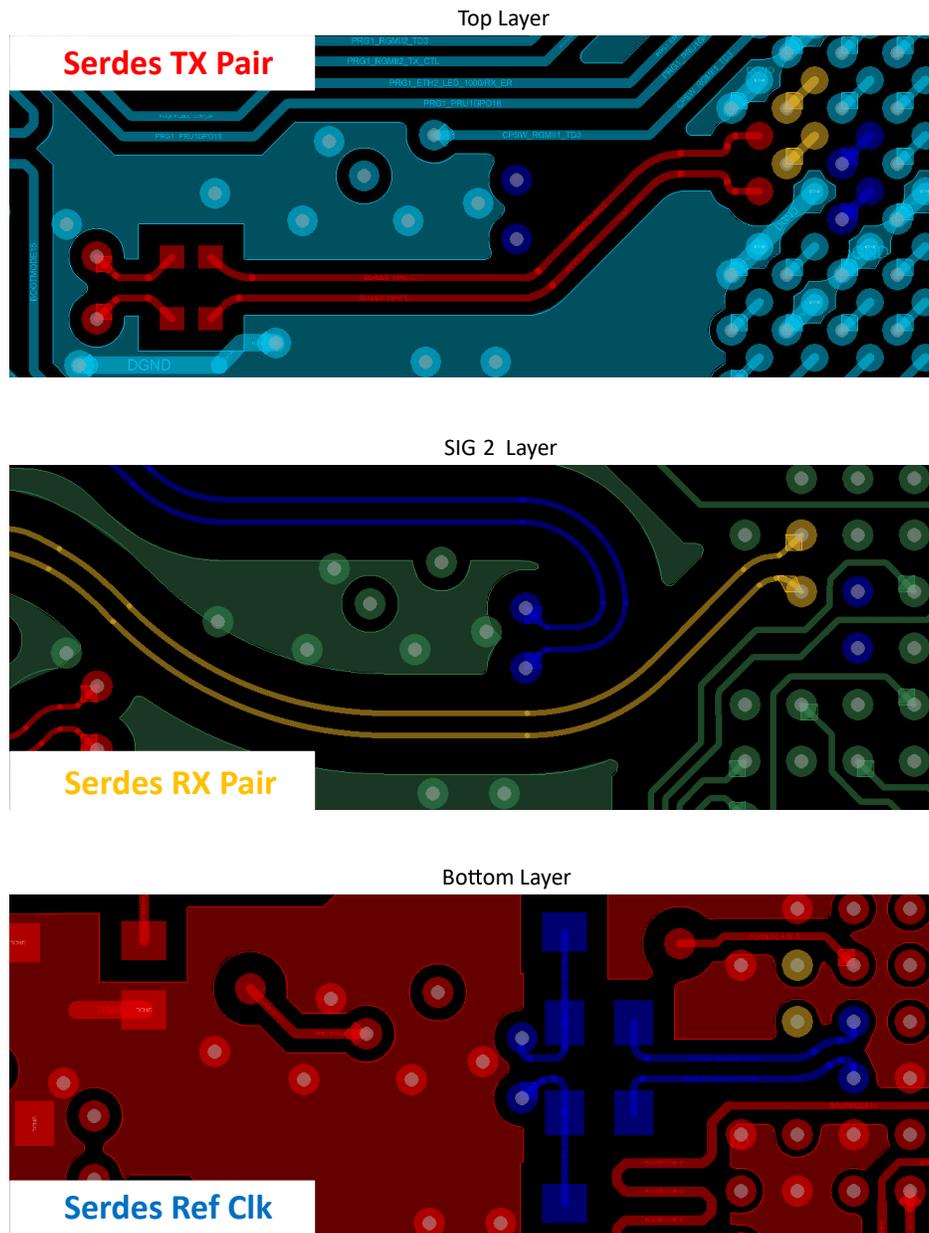
Figure 5-1. Serdes Escapes

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6 Route DDR Signals

The AM64x supports connection to DDR4 and LPDDR4 devices. The DDR signals must be routed next. For detailed recommendations for DDR routing, see the *AM64x DDR Board Design and Layout Guidelines*. Figure 6-1 through Figure 6-3 show the BGA breakout for the DDR4 on the AM64x GP EVM. Routing for LPDDR4 uses a similar escape.

The DDR4 SDRAM memory devices are normally arranged so that the data group balls are closest to the AM64x device. The pin placement of the DDR4 signals on the AM64x places the address and command signals between data byte lane1 and data byte lane0. To achieve an escape on four layers it was necessary to rotate the DDR4 memory and place the address pins closer to the AM64x. Since the EVM uses a single x16-bit DDR4 memory device, the added trace length for the data lines is not significant.
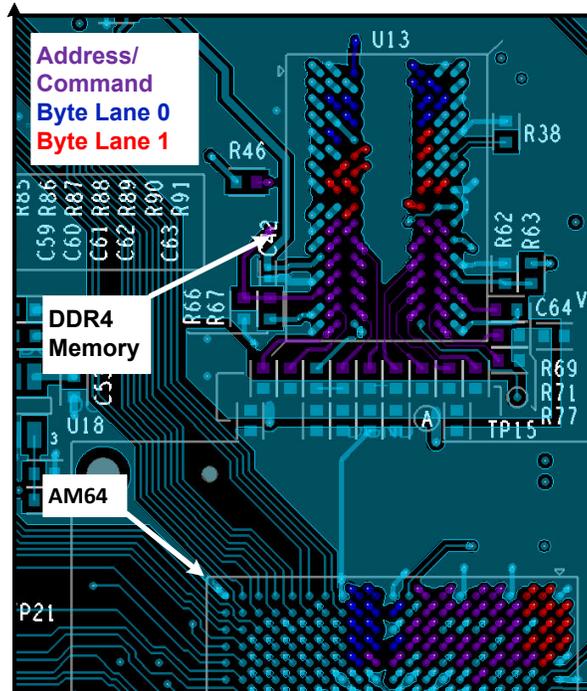
Figure 6-1. DDR4 Address and Data Top Layer
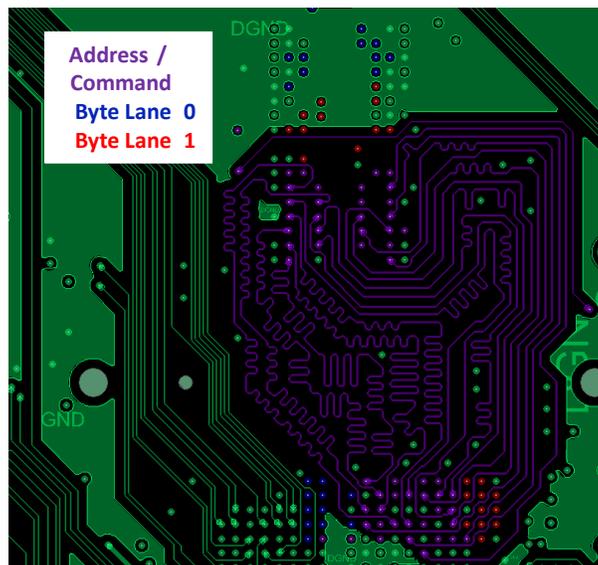
Figure 6-2. DDR4 Address on Sig1 Layer
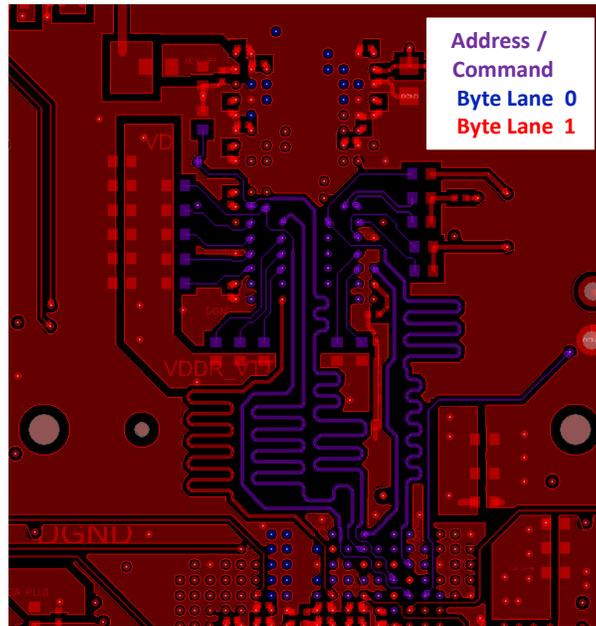
Figure 6-3. DDR4 Address on Bottom Layer

6.1 Address, Command, Control, and Clock Group Routes

The address, command, and clock signals are routed directly to the memory device followed by the VTT termination resistors. The VTT termination is placed at the end of the trace past the connection to the memory. If 8-bit memories are used, the address, command and clock signals should be in a fly-by manner.

The bottom, SIG1 and SIG2 layers are used to escape and route the address and command signals. The traces must be length matched to ensure that the signals arrive at the memory at the same time. Length matching must be from the SoC to memory pin individually including the stub to the memory pad. The trace connection to the VTT termination resistor is not included in this measurement.

The escapes of the address and command signals on these three layers are shown above. Details of the escape are shown in Figure 6-4.

Address signals were routed directly from the SoC to the via next to the associated pad for the memory device. This requires that the address signals escape in the correct order. Some of the signals are routed looped around pins closer to the center of the AM64x to achieve the correct order. Using a third steering via in the trace simplifies the escape but complicates the length matching calculation. It is always best to have the same number of vias for each of the address and command signals.

Placing the address pins of the memory closer to the AM64x allows the address and command signals to be routed without crossing a byte data lane.
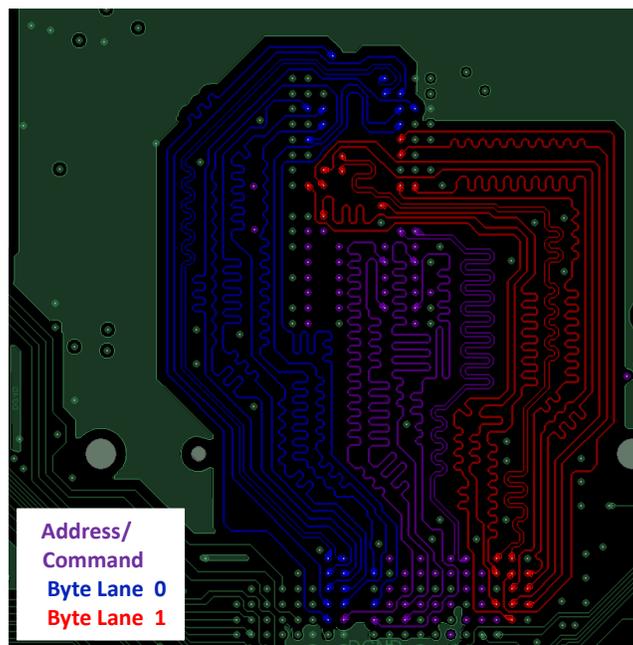

**Figure 6-4. DDR4 Address and Data Sig2 Layer**

6.2 Data Group Routes

The images above show the data group routing for the DDR4 memory. Note that the PCB layout designer grouped all 11 nets for each byte group on a single layer. This is not a requirement but it is strongly recommended as this simplifies the signal length and delay matching requirements.

The DDR4 design for the AM64x GP EVM includes a single 16-bit device for a 16bit data bus. The order of the byte lane connection is determined by the order of the byte lane signals on the AM64x. The routing layers shown in the picture above including the top, the bottom, the SIG1 layer and the SIG2 layer.

Figure 6-5 shows escape of the signals from the BGA of the AM64x. Note that most of the routing is on the internal layers SIG1 and SIG2. All of the DDR signals are connected directly to a via within the BGA footprint. Signals travel through traces routed on the top and bottom layers at a different speed then traces routed on internal layers. This difference must be included in the length matching calculations. Ideally, all DDR4 signals should be routed on internal layers. A second via next to the pads on the DDR4 memory is used to connect to the memory device. Each trace has only two vias.
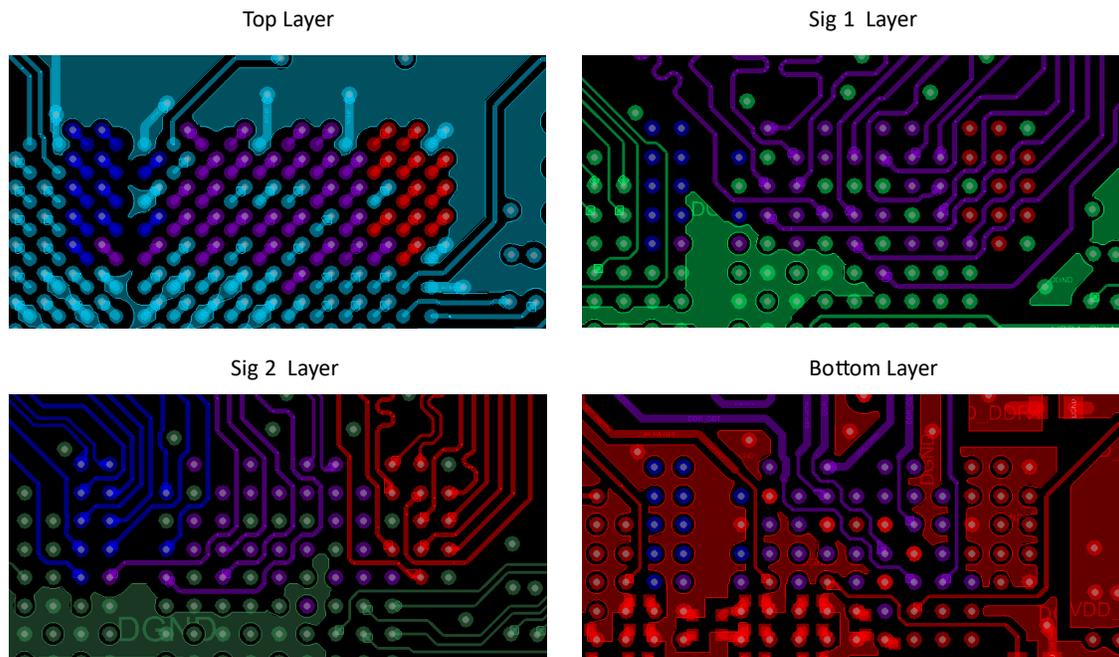
Figure 6-5. DDR4 Signal Escape

7 Complete Power Decoupling

The middle priority interfaces and the power distribution planes and pours are routed after the SERDES and DDR interfaces. TI strongly recommends completing all SERDES and DDR routing before continuing with other interfaces. Note that the power distribution planes and pours and all of the decoupling must be placed before PCB simulations are executed for the SERDES and DDR routes. TI strongly recommends that simulation be performed on the higher speed source-synchronous interfaces, such as RGMII, OSPI, and QSPI. Routing for these interfaces should be completed at this time.

Special care is needed for the 3.3 µF output capacitor connected to the CAP_VDDSHV_MMC1 pin on the SoC. This capacitor should be placed as close to the pin as possible and a low inductance path should be present between the CAP_VDDSHV_MMC1 output and the VDDSHV5 voltage pins for the MMC1 IO voltage. This allows the internal LDO to generate either the 3.3 V or 1.8 V needed for an SD Card. The layout used on the AM64 GP EVM is shown in Figure 7-1.
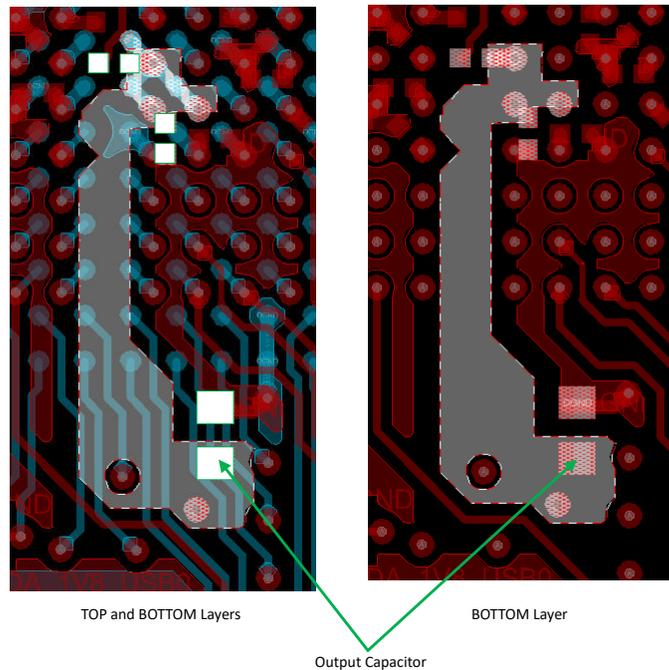
Figure 7-1. AM64 GP EVM Output Capacitor Placement for CAP_VDDSHV_MMC1

This placement can be improved if the capacitor can be placed directly under the SoC. An alternate layout is shown in Figure 7-2.
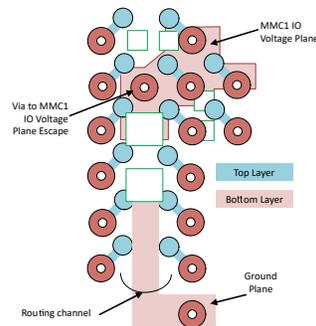
Figure 7-2. Alternate AM64 GP EVM Output Capacitor Placement for CAP_VDDSHV_MMC1

8 Route Lowest Priority Interfaces

When the length matching and simulations have been completed for the highest priority interfaces, and the Power Distribution Network (PDN) analysis has been completed, then the layout can continue with the medium and lower priority interfaces. For additional information, refer to the *Sitara™ Processor Power Distribution Networks: Implementation and Analysis*.

9 References

- *High-Speed Interface Layout Guidelines*
- Sitara™ Processor Power Distribution Networks: Implementation and Analysis
- *AM64x DDR Board Design and Layout Guidelines*

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
	*	Initial Release

Changes from February 1, 2021 to July 30, 2021 (from Revision * (February 2021) to Revision A (July 2021)) **Page**
- Updated with AM243x information...0

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