User's Guide

Migration Between TMS320F28002x and TMS320F28003x

ABSTRACT

This migration guide describes the hardware and software differences to be aware of when moving between F28002x and F28003x C2000™ MCUs. This document shows the block diagram between the two MCUs as a visual representation on what blocks are similar or different. It also highlights the features that are unique between the two devices for all available packages in a device comparison table. The F28002x and F28003x devices have three packages in common; 80-pin, 64-pin and 48-pin so a PCB hardware section has been added to aid in migration between the three common packages. The digital general-purpose input/output (GPIO) and analog multiplex comparison tables show pin functionality between the two MCUs. This is a good reference for hardware design and signal routing when considering a move between the two devices. Lastly, like the F28002x device, the F28003x software support is only in EABI format.

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1 Feature Differences Between F28002x and F28003x

F28003x is a superset of F28002x. They have three packages in common, 48-pin, 64-pin and 80-pin. It is possible to migrate between F28003x and F28002x with the caveats in this document taken into account.

Note

This comparison guide focuses on the super-set devices: F280025 and F280039. Other part numbers in this product family have reduced feature support. For details specific to part numbers, see the device-specific data sheet.

1.1 F28002x and F28003x Feature Comparison

An overlaid block diagram of F28002x and F28003x is shown in Figure 1-1 while feature comparison of the superset part numbers for the F28003x and F28002x devices is shown in Table 1-1.

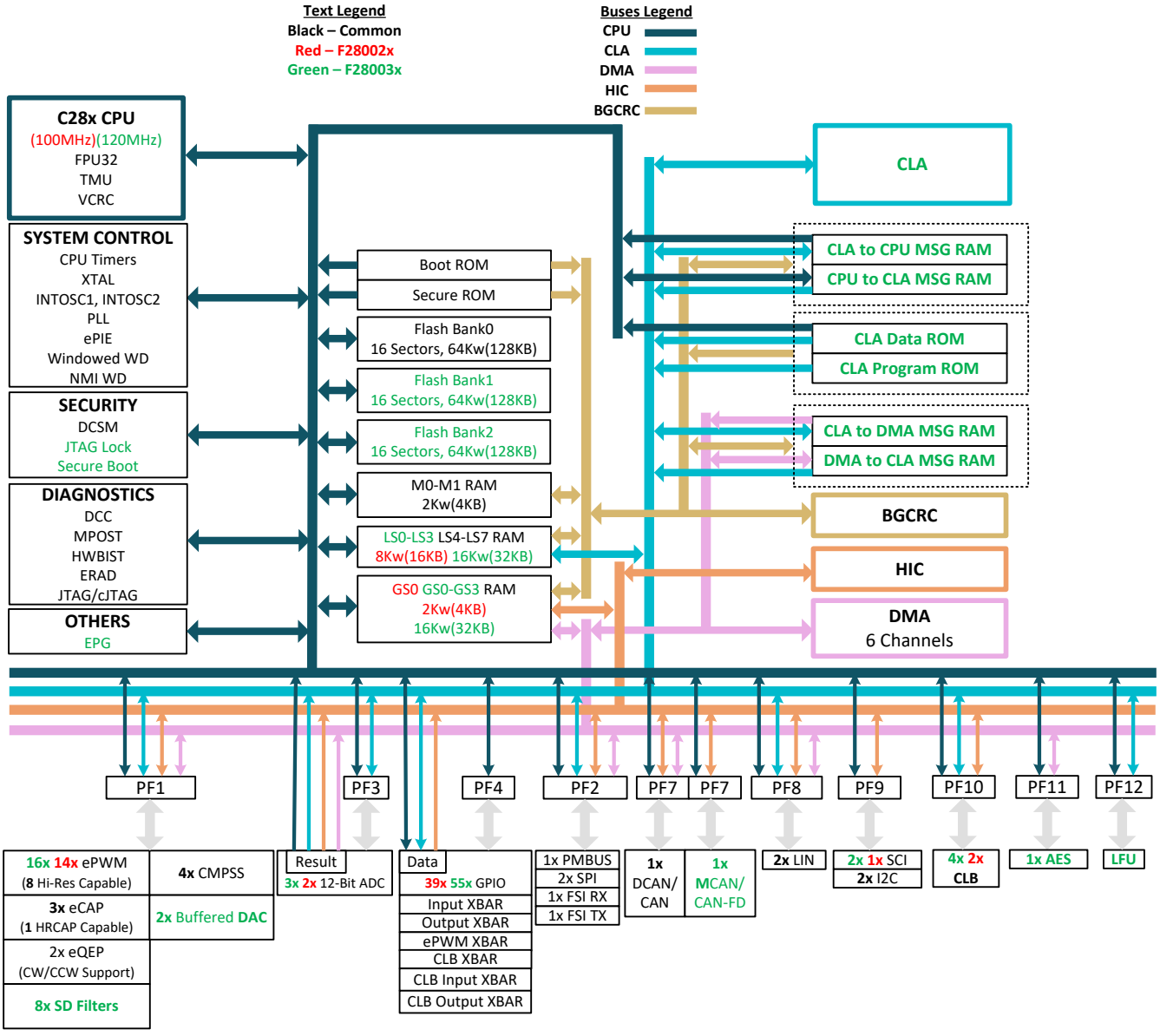


Figure 1-1. F28003x and F28002x Overlaid Functional Block Diagram

Table 1-1. F28002x and F28003x Superset Device Comparison

Feature		F28002x			F28003x			
		80-Pin PN	64-Pin PM	48-Pin PT	100-Pin PZ	80-Pin PN	64-Pin PM	48-Pin PT
Processor and Accelerators								
C28x	Frequency (MHz)	100			120			
	FPU	Yes (instructions for Fast Integer Division)						
	VCRC	Yes						
	TMU	Yes – Type 1 (instructions supporting NLPID)						
CLA – Type 2	Available	No			Yes			
	Frequency (MHz)	-			120			
6–Channel DMA – Type 0		Yes						
External interrupts		5						
Memory								
Flash		128KB (64Kw)			384KB (192Kw)			
RAM	Dedicated	4KB (2Kw)						
	Local Shared	16KB (8Kw)			32KB (16Kw)			
	Message	-			1KB (0.5Kw)			
	Global Shared	4KB (2Kw)			32KB (16Kw)			
	Total	24KB (12Kw)			69KB (34.5Kw)			
Message RAM Types		-			512B (256w) CPU–CLA 512B (256w) CLA–DMA			
ECC		FLASH, Mx, LSx			FLASH, Mx, LSx, GSx, Message RAM			
Parity		GSx, ROM			ROM, CAN RAM			
Code security for on–chip flash and RAM		Yes						
System								
Configurable Logic Block (CLB)		2 Tiles			4 Tiles			
Embedded Pattern Generator (EPG)		-			Yes			
Motor Control Libraries in ROM		Yes						
32–bit CPU timers		3						
Advance Encryption Standard (AES)		–			Yes			
Background CRC (BGCRC)		Yes						
Live Firmware Update (LFU) Support		–			Yes, with enhancements and flash bank erase time improvements			
Secure Boot		–			Yes			
JTAG Lock		–			Yes			
HWBIST		Yes						
Nonmaskable Interrupt Watchdog (NMIWD) timers		1						
Watchdog timers		1						
Crystal oscillator/External clock input		1						
Internal oscillator		2						
Pins and Power Supply								
Internal 3.3v to 1.2v Voltage Regulator	VREG LDO	Yes						
GPIO pins		39	26	14	51	39	26	14
Additional GPIO		4 (2 from cJTAG and 2 from X1/X2)						
AIO (analog with digital inputs)		16	16	14	23	16	16	14
AGPIO (analog with digital inputs and outputs)		-			2	2	-	-

Table 1-1. F28002x and F28003x Superset Device Comparison (continued)

Feature		F28002x			F28003x			
		80-Pin PN	64-Pin PM	48-Pin PT	100-Pin PZ	80-Pin PN	64-Pin PM	48-Pin PT
Analog Peripherals								
ADC 12–bit	Number of ADCs	2			3			
	MSPS	3.45			4			
	Conversion Time (ns)	290			250			
ADC channels (single–ended) - *includes the two gpdac outputs on F28003x*		16	16	14	23	18	16	14
Temperature sensor		1						
Buffered DAC		-			2			
CMPSS (each CMPSS has two comparators and two internal DACs)		4						
Control Peripherals								
eCAP/HRCAP modules		3 (1 with HRCAP capability) – Type 2						
ePWM/HRPWM channels – Type 4		14 (8 with HRPWM)			16 (8 with HRPWM)			
eQEP modules		2 – Type 2						
SDFM channels		-			8 – Type 2			
Communication Peripherals								
CAN (DCAN) – Type 0		1						
CANFD (MCAN) – Type 1		–			1			
FSI		1 (1 RX and 1 TX) – Type 1				1 (1 RX and 1 TX) – Type 2		
I2C – Type 1		2						
LIN – Type 1		2						
HIC		Yes - Type 0			Yes - Type 1			
PMBus – Type 0		1						
SCI – Type 0		1				2		
SPI – Type 2		2						
Package Options, Temperature, and Qualification								
Junction temperature (TJ)		–40°C to 125°C			–40°C to 150°C			
Free-Air temperature (TA)		–40°C to 125°C						
Package Options with AEC-Q100 Qualification available		Yes	Yes	Yes	Yes	–	Yes	Yes

2 PCB Hardware Changes

The F28002x and F28003x devices have three packages in common: 80-pin PN, 64-pin PM and 48-pin PT. The following sections describe the pin migration in detail.

Note

Overall compatibility depends on more than just the pins. Review all of the changes in this document during the migration process.

2.1 PCB Hardware Changes for the 80-Pin PN, 64-Pin PM and 48-Pin PT Packages

This section describes the F28003x and F28002x differences that exist between the 80-Pin PN, 64-Pin PM and 48-Pin PT packages.

80-Pin PN: The Q and non-Q variant for F28002x have the same pinout whereas F28003x has no Q variant for 80-Pin PN. Figure 2-1 outlines the differences.

64-Pin PM: The Q and non-Q variant for F28002x have the same pinout whereas VREGENZ replaces GPIO39 in the Q variant for F28003x. Figure 2-2 and Figure 2-3 outline the differences.

48-Pin PT: The Q and non-Q variant have the same pinout for both devices. Figure 2-4 outlines the differences.

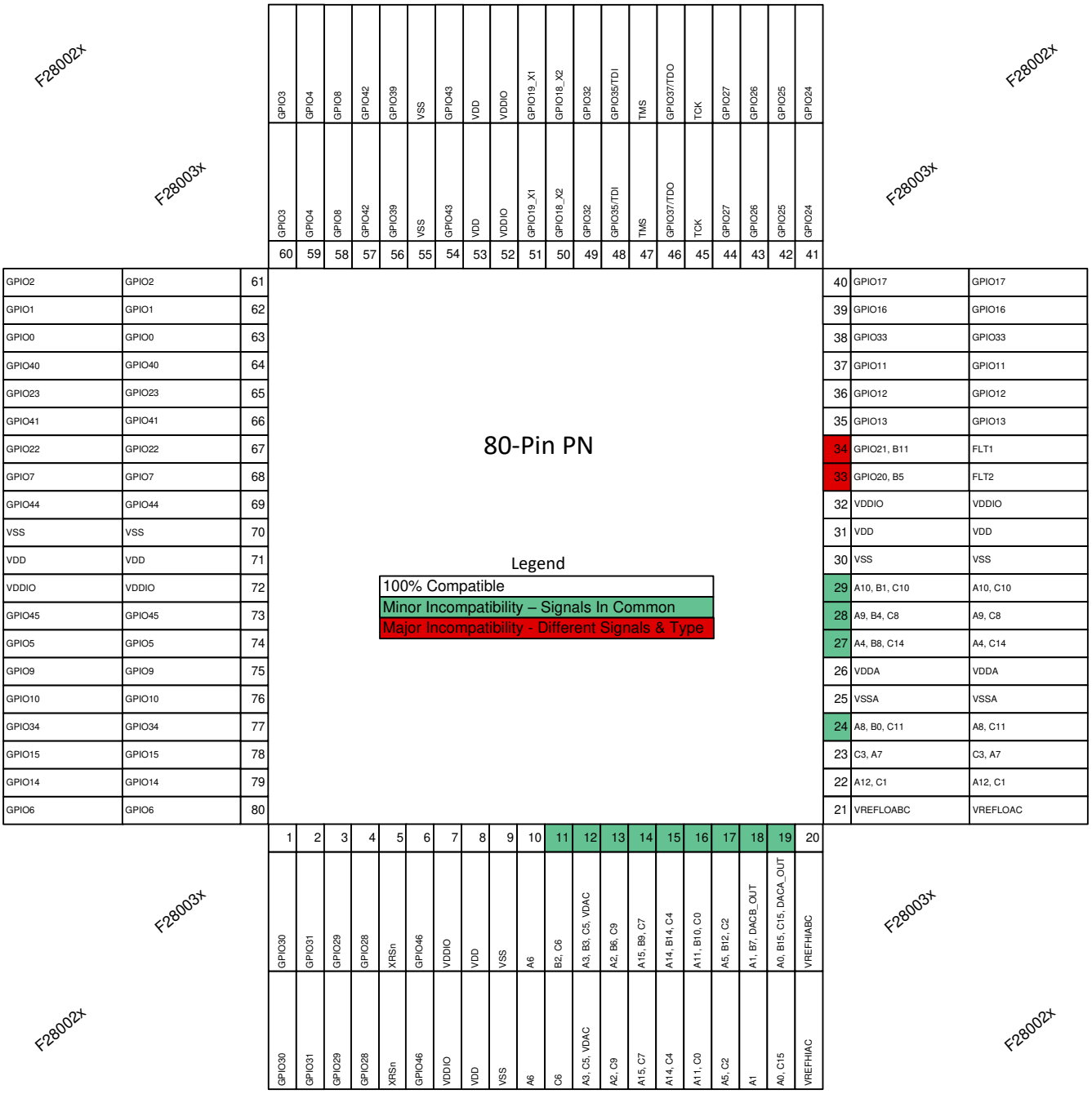
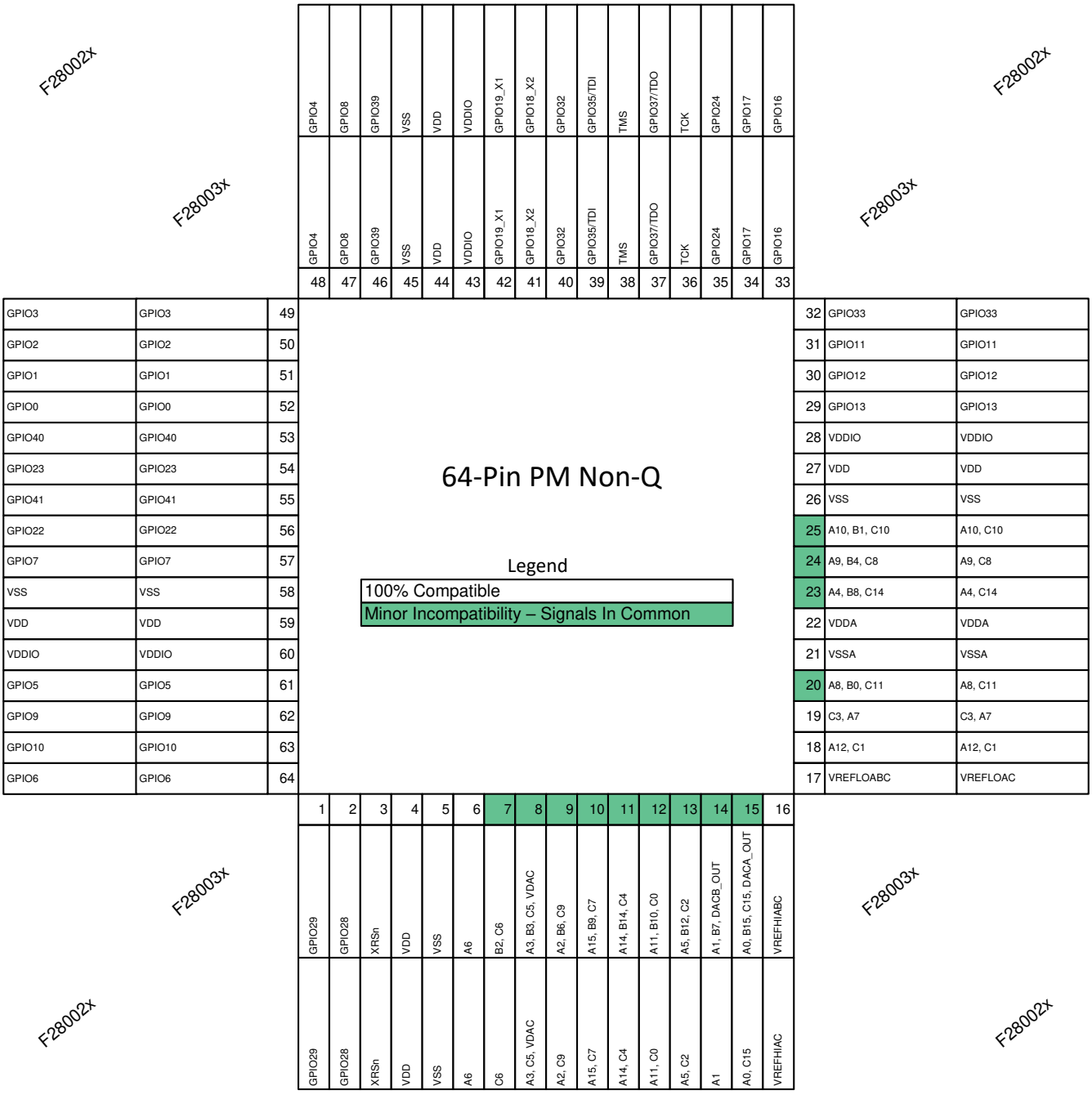


Figure 2-1. 80-Pin PN, F28003x and F28002x Pin-Overlay



GPIO3	GPIO3	49	32	GPIO33	GPIO33
GPIO2	GPIO2	50	31	GPIO11	GPIO11
GPIO1	GPIO1	51	30	GPIO12	GPIO12
GPIO0	GPIO0	52	29	GPIO13	GPIO13
GPIO40	GPIO40	53	28	VDDIO	VDDIO
GPIO23	GPIO23	54	27	VDD	VDD
GPIO41	GPIO41	55	26	VSS	VSS
GPIO22	GPIO22	56	25	A10, B1, C10	A10, C10
GPIO7	GPIO7	57	24	A9, B4, C8	A9, C8
VSS	VSS	58	23	A4, B8, C14	A4, C14
VDD	VDD	59	22	VDDA	VDDA
VDDIO	VDDIO	60	21	VSSA	VSSA
GPIO5	GPIO5	61	20	A8, B0, C11	A8, C11
GPIO9	GPIO9	62	19	C3, A7	C3, A7
GPIO10	GPIO10	63	18	A12, C1	A12, C1
GPIO6	GPIO6	64	17	VREFLOABC	VREFLOAC

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
GPIO29	GPIO28	XRSn	VDD	VSS	A6	B2, C6	A3, B3, C5, VDAC	A2, B6, C9	A15, B9, C7	A14, B14, C4	A11, B10, C0	A5, B12, C2	A1, B7, DACB_OUT	A0, B15, C15, DACA_OUT	VREFHIABC
GPIO29	GPIO28	XRSn	VDD	VSS	A6	C6	A3, C5, VDAC	A2, C9	A15, C7	A14, C4	A11, C0	A5, C2	A1	A0, C15	VREFHIAC

GPIO4	GPIO8	GPIO39	VSS	VDD	VDDIO	GPIO19_X1	GPIO18_X2	GPIO32	GPIO35/TDI	TMS	GPIO37/TDO	TCK	GPIO24	GPIO17	GPIO16
GPIO4	GPIO8	GPIO39	VSS	VDD	VDDIO	GPIO19_X1	GPIO18_X2	GPIO32	GPIO35/TDI	TMS	GPIO37/TDO	TCK	GPIO24	GPIO17	GPIO16
48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33

Figure 2-2. 64-Pin PM Non-Q Variant, F28003x and F28002x Pin-Overlay

Figure 2-3. 64-Pin PM Q Variant, F28003x and F28002x Pin-Overlay

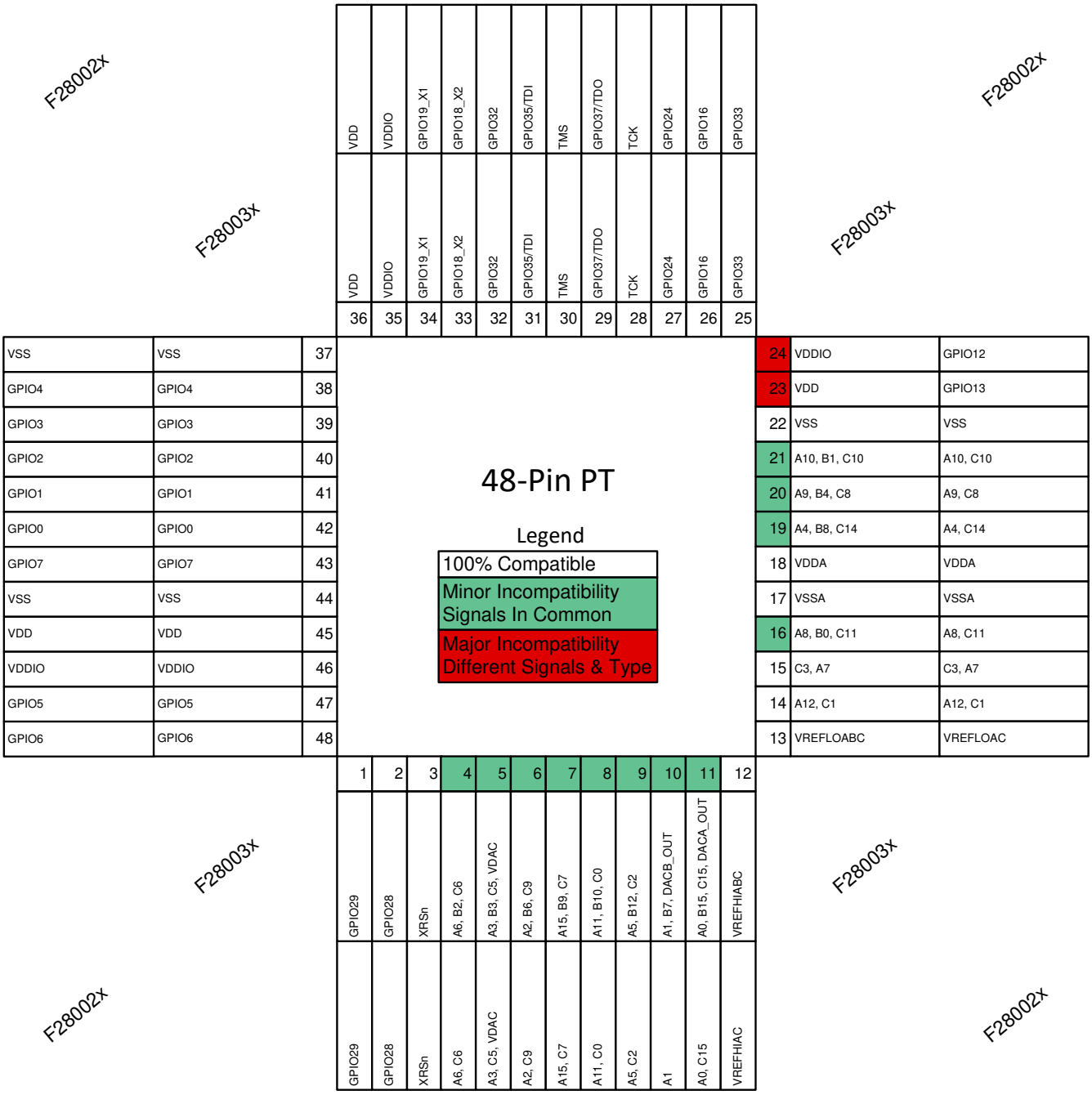


Figure 2-4. 48-Pin PT, F28003x and F28002x Pin-Overlay

2.2 80-Pin PN, 64-Pin PM and 48-Pin PT Migration Between F28002x and F28003x For New and Existing PCB

For the color legend, see Figure 2-1 through Figure 2-4.

Table 2-1. 80-Pin PN, 64-Pin PM and 48-Pin PT Migration Between F28002x and F28003x For New and Existing PCB

Pin No			Pin Name			Action	
80	64	48	F28002x	F28003x	Transition Type	F28003x to F28002x	F28002x to F28003x
Minor Incompatibility - Signals in Common (1)							
10	6	4	A6	A6	Common Analog Channel	Use A6 (No change for 64-Pin and 80-Pin)	
11	7		C6	B2, C6		Use C6	
12	8	5	A3, C5, VDAC	A3, B3, C5 VDAC		Use A3, C5 or VDAC	
13	9	6	A2, C9	A2, B6, C9		Use A2 or C9	
14	10	7	A15, C7	A15, B9, C7		Use A15 or C7	
15	11	-	A14, C4	A14, B14, C4		Use A14 or C4	
16	12	8	A11, C0	A11, B10, C0		Use A11 or C0	
17	13	9	A5, C2	A5, B12, C2		Use A5 or C2	
18	14	10	A1	A1, B7, DACB_OUT		Use A1	
19	15	11	A0, C15	A0, B15, C15, DACA_OUT		Use A0 or C15	
24	20	16	A8, C11	A8, B0, C11		Use A8 or C11	
27	23	19	A4, C14	A4, B8, C14		Use A4 or C14	
28	24	20	A9, C8	A9, B4, C8		Use A9 or C8	
29	25	21	A10, C10	A10, B1, C10		Use A10 or C10	
Major Incompatibility - Different Signals and Types							
33	-	-	FLT2	GPIO20, B5	Flash Test Pins to GPIO/Analog	No connect. Enable internal pull-up for the GPIOs on F28003x	
34	-	-	FLT1	GPIO21, B11			
-	-	23	GPIO13	VDD	Power to GPIO	Tie to VDD through 0-Ohm resistor. Depopulate resistor when using F28002x and enable internal pull-up for the GPIO	
-	-	24	GPIO12	VDDIO		Tie to VDDIO through 0-Ohm resistor. Depopulate resistor when using F28002x and enable internal pull-up for the GPIO	
(Q Variant) Major Incompatibility - Different Signals and Types							
-	46	-	GPIO39	VREGENZ		External VREG not supported. Tie to VSS through 0-Ohm resistor. Depopulate resistor when using F28002x and enable internal pull-up for the GPIO	

(1) Channel to use selected in software.

3 Feature Differences for System Consideration

The differences and similarities that exist when moving between the F28003x and F28002x devices is explored in this section.

3.1 New Features in F28003x

This section outlines features that only exist in the F28003x device. For details on each of these new features, see the *TMS320F28003x Real-Time Microcontrollers Technical Reference Manual* (SPRUIW9).

3.1.1 Advance Encryption Standard (AES)

The AES module on F28003x is a symmetric cipher module that provides hardware-accelerated data encryption and decryption with support for 128-, 192- and 256-bit keys. AES was first introduced in F2838x.

3.1.2 Secure Boot/JTAG Lock

The F28003x device supports secure booting and also has the capability to lock the JTAG to avoid debug access thereby enhancing security. Secure Boot and JTAG Lock were first introduced in F2838x.

3.1.3 Modular Controller Area Network (MCAN)

The MCAN module on F28003x supports CAN FD (CAN with the flexible data-rate) specification which has a higher throughput compared to Classic CAN. It can also operate in Classic CAN mode if needed. MCAN was first introduced in F2838x.

3.1.4 Embedded Pattern Generator (EPG)

The EPG on F28003x is an interface module that can be used to generate waveforms and clocks for other modules on the device. This can be useful for communication module diagnostics and also providing the modulation clock for the SDFM.

3.1.5 Live Firmware Update (LFU)

The F28003x device has in-built hardware to facilitate live firmware updates. It supports fast context switching from the old firmware to the new firmware to minimize application downtime when updating the device firmware.

3.2 Communication Module Changes

Communication module changes between the F28002x and F28003x devices affect the number of modules, addition of CAN-FD and some differences in HIC and FSI. Details are available in Table 3-1.

Table 3-1. Communication Module Instances

Module	Category	F28002x	F28003x	Notes
LIN	Number	2 - LINA, LINB	2 - LINA, LINB	
CAN	Number	1- CANA	1- CANA	
CAN-FD	Number	not present	1 - MCANA	
SCI	Number	1 - SCIA	2 - SCIA, SCIB	
SPI	Number	2 - SPIA, SPIB	2 - SPIA, SPIB	
I2C	Number	2 -I2CA, I2CB	2 -I2CA, I2CB	
PMBUS	Number	1 - PMBUSA	1 - PMBUSA	
FSI	Number	1 - FSIA	1 - FSIA	
	Register	-	TX_OPER_CTRL_LO.SEL_TDM_IN	Transmit TDM Mode Enable bit
		-	TX_DLYLINE_CTRL	Transmit delay line control register
		-	RX_MASTER_CTRL.DATA_FILTER_EN	Data filter enable bit
		-	RX_TRIG_CTRL_0	Receive Trigger Control register 0
		-	RX_TRIG_WIDTH_0	Receive Trigger Wdith register 0
		-	RX_TRIG_CTRL_1	Receive Trigger Control register 1
		-	RX_TRIG_CTRL_2	Receive Trigger Control register 2
		-	RX_TRIG_CTRL_3	Receive Trigger Control register 3
		-	RX_UDATA_FILTER	Receive User Data Filter Control register
HIC	Number	1 - HICA	1 - HICA	
	Register	-	HICCOMMIT	Commit bit for the HICLOCK register

3.3 Control Module Changes

There are minimal changes in the control modules between the F28002x and F28003x devices. The biggest change is the addition of an SDFM module for the F28003x device. Table 3-2 shows the module instances differences which should be considered when migrating applications between F28002x and F28003x.

Table 3-2. Control Module Differences

Module	Category	F28002x	F28003x	Notes
SDFM	Number	-	8 - SD1_D1C1..D4C4, SD2_D1C1..D4C4	
eQEP	Number	2 - EQEP1, EQEP2		
eCAP	Number	3 - ECAP1..3		
HRCAP	Number	1 - HRCAP3		
ePWM	Number	7 - EPWM1..7	8 - EPWM1..8	Blanking window improvements on F28003x
	Registers	DCFCTL.PULSESEL	DCFCTL.PULSESEL	Blank Pulse Mix added as an option for F28003x
HRPWM	Number	4 - HRPWM1..4		

3.4 Analog Module Differences

This section outlines the analog differences between F28003x and F28002x. The GPDAC is not present on the F28002x and the analog mux table is remapped.

Table 3-3. Analog Module Differences

Module	Category	F28002x	F28003x	Notes
ADC(1)	Number	2 - ADCA, ADCC	3 - ADCA, ADCB, ADCC	
	Max Speed	50 MHz	60 MHz	
GPDAC	Number	-	2 - GPDACA, GPDACB	
CMPSS(1)	Number	4 - CMPSS1 to CMPSS4		
	Registers	CTRIPxFILCLKCTL.CLKPRESCALE[9..0]	CTRIPxFILCLKCTL.CLKPRESCALE[15..0]	CMPSS filter prescaling size increased on F28003x
	Other	CMPx_HP has 5 mux input options	CMPx_HP has 6 mux input options	
Temp Sensor	Number	1 - (in ADCC ch 12)		

1. In porting software from F28002x to F28003x (or the other way around), care must be taken to ensure that the correct ADC channels are used because of a difference in channel assignment, see Section 3.9.

3.5 Other Device Changes

This section describes feature differences between F28002x and F28003x that were not covered in the previous sections, as such the changes identified below must be considered when migrating applications between devices.

3.5.1 PLL

The PLL blocks of F28002x and F28003x devices are the same, however the maximum PLL Raw Clock for F28003x is higher to accommodate the SYSCLK frequency requirement of F28003x. Table 3-4 lists the PLL features for both devices for comparison. for more information, consult the TMS320F28003x microcontrollers technical reference manual.

Table 3-4. PLL Features

Feature	F28002x	F28003x
VCO Range	220 - 600 MHz	220 - 600 MHz
PLL Raw Clock Range	6 - 200MHz	6 - 240 MHz
X1 Input Range (PLL enable)	2 - 25 MHz	2 - 25 MHz
REFCLK Divider	Yes[1..32]	Yes[1..32]
PLL Slip Detect	No (use DCC)	No (use DCC)
Fractional PLLMULT	No	No

3.5.2 PIE Channel Mapping

Pie channel mapping between F28002x and F28003x is different due to peripheral module changes between these devices. Table 3-6 summarizes the common and unique pie channel assignments on these two devices.

Table 3-5. Pie Channel Legend

Color	Description
	Pie channel common for both devices
	Pie channel applicable only for F28002x
	Pie channel applicable only for F28003x

Table 3-6. Pie Table Comparison

	INTx.1	INTx.2	INTx.3	INTx.4	INTx.5	INTx.6	INTx.7	INTx.8	INTx.9	INTx.10	INTx.11	INTx.12	INTx.13	INTx.14	INTx.15	INTx.16
INT1.y	ADCA1	ADCB1	ADCC1	XINT1	XINT2	-	TIMER0	WAKE/ WDOG	-	SYS_ER R	-	-	-	-	-	-
INT2.y	EPWM1_ TZ	EPWM2_ TZ	EPWM3_ TZ	EPWM4_ TZ	EPWM5_ TZ	EPWM6_ TZ	EPWM7_ TZ	EPWM8_ TZ	-	-	-	-	-	-	-	-
INT3.y	EPWM1	EPWM2	EPWM3	EPWM4	EPWM5	EPWM6	EPWM7	EPWM8	-	-	-	-	-	-	-	-
INT4.y	ECAP1	ECAP2	ECAP3	-	-	-	-	-	-	-	ECAP3_I NT2	-	-	-	-	-
INT5.y	EQEP1	EQEP2	-	-	CLB1	CLB2	CLB3	CLB4	SDFM1	SDFM2	-	-	SDFM1D R1	SDFM1D R2	SDFM1D R3	SDFM1D R4
INT6.y	SPIA_RX	SPIA_TX	SPIB_RX	SPIB_TX	-	-	-	-	-	-	-	-	SDFM2D R1	SDFM2D R2	SDFM2D R3	SDFM2D R4
INT7.y	DMA_CH 1	DMA_CH 2	DMA_CH 3	DMA_CH 4	DMA_CH 5	DMA_CH 6	-	-	-	-	FSITXA_I NT1	FSITXA_I NT2	FSIRXA_I NT1	FSIRXA_I NT2		DCC0
INT8.y	I2CA	I2CA_FIF O	I2CB	I2CB_FIF O	-	-	-	-	LINA_0	LINA_1	LINB_0	LINB_1	PMBUSA	-	-	DCC1
INT9.y	SCIA_RX	SCIA_TX	SCIB_RX	SCIB_TX	CANA_0	CANA_1	-	-	MCAN_0	MCAN_1	MCAN_E CC	MCAN_W AKE	BGCRC_ CPU	-	-	HICA
INT10.y	ADCA_E VT	ADCA2	ADCA3	ADCA4	ADCB_E VT	ADCB2	ADCB3	ADCB4	ADCC_E VT	ADCC2	ADCC3	ADCC4	-	-	-	-
INT11.y	CLA1_1	CLA1_2	CLA1_3	CLA1_4	CLA1_5	CLA1_6	CLA1_7	CLA1_8	-	-	-	-	-	-	-	-
INT12.y	XINT3	XINT4	XINT5	PBIST(M POST)	FMC	-	FPU_OV ERFLOW	FPU_UN DERFLO W	-	RAM_CO RR_ERR	FLASH_ CORR_E RR	RAM_AC C_VIOL	AES_SIN TREQ	BGCRC_ CLA1	CLA_OV ERFLOW	CLA_UN DERFLO W

3.5.3 Bootrom

For bootrom similarities and differences between F28002x and F28003x see Table 3-8 and Table 3-9.

Table 3-7. Boot options Legend

Color	Description
	Options common for both devices but BOOTDEFx values may differ
	Options applicable only for F28002x
	Options applicable only for F28003x

Table 3-8. Bootloaders and GPIO Assignment Comparison

Bootloader	Option	BOOTDEFx	F28002x	F28003x
Parallel	0	0x00	D0-D7=0 to 7; DSP=16; Host=29	D0-D7=0 to 7; DSP=16; Host=29
	1	0x20	D0-D7=0 to 7; DSP=16; Host=11	D0-D7=0 to 7; DSP=16; Host=11
SCIA	0	0x01	TX=29; RX=28	TX=29; RX=28
	1	0x21	TX=16; RX=17	TX=16; RX=17
	2	0x41	TX=8; RX=9	TX=8; RX=9
	3	0x61	TX=2; RX=3	TX=2; RX=3
	4	0x81	TX=16; RX=3	TX=16; RX=3
CAN	0	0x02	TX=4; RX=5	TX=4; RX=5
	1	0x22	TX=32; RX=33	TX=32; RX=33
	2	0x42	TX=2; RX=3	TX=2; RX=3
	3	0x62	n/a	TX=13; RX=12
MCAN	0	0x08	n/a	TX=4; RX=5
	1	0x28	n/a	TX=1; RX=0
	2	0x48	n/a	TX=13; RX=12
SPI	0	0x06	SIMO=2 SOMI=1; CLK=3; STE=5	SIMO=2 SOMI=1; CLK=3; STE=5
	1	0x26	SIMO=16 SOMI=1; CLK=3; STE=0	SIMO=16 SOMI=1; CLK=3; STE=0
	2	0x46	SIMO=8 SOMI=10; CLK=9 STE=11	SIMO=8 SOMI=10; CLK=9; STE=11
	3	0x66	SIMO=8 SOMI=17; CLK=9; STE=11	SIMO=8 SOMI=17; CLK=9; STE=11

Table 3-8. Bootloaders and GPIO Assignment Comparison (continued)

Bootloader	Option	BOOTDEFx	F28002x	F28003x
I2C	0	0x07	SDA=32 SCL=33	SDA=32; SCL=33
	1	0x27	SDA=0; SCL=1	SDA=0; SCL=1
	2	0x47	SDA=10; SCL=8	SDA=10; SCL=8

Table 3-9. Boot Modes Comparison

Boot Mode	Option	BOOTDEFx	F28002x	F28003x
Flash	0	0x03	Entry=0x00080000' Bank/Sector=0/0	Entry=0x00080000; Bank/Sector=0/0
	1	0x23	Entry=0x00084000; Bank/Sector=0/4	Entry=0x00088000; Bank/Sector=0/8
	2	0x43	Entry=0x00088000; Bank/Sector=0/8	Entry=0x0008FFF0; Bank/Sector=0/15
	3	0x63	Entry=0x0008EFF0; Bank/Sector=0/14	Entry=0x00090000; Bank/Sector=1/0
	4	0x83	-	Entry=0x00097FF0; Bank/Sector=1/7
	5	0xA3	-	Entry=0x0009FFF0; Bank/Sector=1/15
	6	0xC3	-	Entry=0x000A0000; Bank/Sector=2/0
	7	0xE3	-	Entry=0x000AFFF0; Bank/Sector=2/15
LFU Flash	0	0x0B	-	Entry=0x00080000; Bank=0 Entry=0x00090000; Bank=1 Entry=0x000A0000 Bank=2
	1	0x2B	-	Entry=0x00088000; Bank=0 Entry=0x00098000; Bank=1 Entry=0x000A8000 Bank=2
	2	0x4B	-	Entry=0x0008FFF0; Bank=0 Entry=0x0009FFF0; Bank=1 Entry=0x000AFFF0 Bank=2
	3	0x6B	-	Entry=0x00088000; Bank=0 Entry=0x00090000; Bank=1 Entry=0x000A0000 Bank=2
	4	0x8B	-	Entry=0x0008EFF0; Bank=0 Entry=0x00097FF0; Bank=1 Entry=0x000A7FF0 Bank=2

Table 3-9. Boot Modes Comparison (continued)

Boot Mode	Option	BOOTDEFx	F28002x	F28003x
Secure LFU Flash	0	0x0C	-	Entry=0x00080000; Bank=0 Entry=0x00090000; Bank=1 Entry=0x000A0000 Bank=2
	1	0x2C	-	Entry=0x00088000; Bank=0 Entry=0x00098000; Bank=1 Entry=0x000A8000 Bank=2
	2	0x4C	-	Entry=0x0008FFF0; Bank=0 Entry=0x0009FFF0; Bank=1 Entry=0x000AFFF0 Bank=2
	3	0x6C	-	Entry=0x00088000; Bank=0 Entry=0x00090000; Bank=1 Entry=0x000A0000 Bank=2
	4	0x8C	-	Entry=0x0008EFF0; Bank=0 Entry=0x00097FF0; Bank=1 Entry=0x000A7FF0 Bank=2
Wait	0	0x04	Watchdog enabled	Watchdog enabled
	1	0x24	Watchdog disabled	Watchdog disabled
RAM	0	0x05	Entry=0x00000000	Entry=0x00000000

3.5.4 CLB and Motor Control Libraries

There are no functional changes on the Motor Control Libraries in ROM and CLB between F28002x and F28003x.

3.5.5 AGPIO

F28003x has two AGPIO channels that support both normal GPIO and AGPIO (analog) pin functionality. These channels are available on the 100-pin and 80-pin packages. AGPIO functionality is not available on F28002x. See the F28003x data manual for configuration details.

3.6 Power Management

The F28002x and F28003x devices have a few different options for power. F28003x supports dual-rail (3.3 V and 1.2 V) or single-rail (3.3 V) with the internal LDO VREG providing the 1.2 V rail. F28002x only supports single-rail (3.3 V) with the internal LDO VREG providing the 1.2 V rail. This section describes the power management differences and similarities between the two devices.

3.6.1 LDO/VREG

F28003x supports internal and external VREG selectable using the VREGENZ pin. However, not all packages support the external VREG option. For packages that do not support external VREG, the VREGENZ pin is replaced by GPIO39 on the F28003x device. For more details, see the device-specific data manual. F28002x supports only internal VREG and has no VREGENZ pin.

3.6.2 POR/BOR

There are no functional changes for the POR and BOR.

3.6.3 Power Consumption

There is an increase in power consumption on F28003x compared to F28002x.

3.7 Memory Module Changes

RAM and FLASH memories in F28002x and F28003x devices have some similarities and differences. Table 3-10 summarizes the memory features including error-checking and security assignment.

Table 3-10. RAM and FLASH memory changes

Memory		F28002x			F28003x		
		Size	Parity/ ECC	Secured	Size	Parity/ ECC	Secured
RAM	Dedicated(M0,M1)	4KB	ECC	No	4KB	ECC	No
	Local Shared(LS0-LS7)	16KB	DCSM-controlled	Yes	32KB	ECC	DCSM-controlled
	Global Shared(GS0-GS3)	4KB (GS0)	Parity	No	32KB	ECC	No
	Message	-	-	-	512B(CPU-CLA) 512B(CLA-DMA)	ECC	No
	Total RAM	**24KB**			**69KB**		
FLASH	Per Bank	128KB(1 bank)	ECC	DCSM-controlled	128KB(3 banks)	ECC	DCSM-controlled
	Total FLASH	**128KB**			**384KB**		

3.8 GPIO Multiplexing Changes

Table 3-12 outlines the differences and similarities that exist in the GPIO mux between F28002x and F28003x.

Table 3-11. Mux Legend

Color	Description
	mux function common for both devices
	mux function applicable only for F28002x
	mux function applicable only for F28003x

Table 3-12. GPIO Muxed Pins

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO0	EPWM1_A				I2CA_SDA	SPIA_STE	FSIRXA_CLK	MCAN_RX	CLB_OUTPUTXBAR8	EQEP1_INDEX	HIC_D7	HIC_BASESEL1	
GPIO1	EPWM1_B				I2CA_SCL	SPIA_SOMI		MCAN_TX	CLB_OUTPUTXBAR7	HIC_A2	FSITXA_TDM_D1	HIC_D10	
GPIO2	EPWM2_A			OUTPUTXBAR1	PMBUSA_SDA	SPIA_SIMO	SCIA_TX	FSIRXA_D1	I2CB_SDA	HIC_A1	CANA_TX	HIC_D9	
GPIO3	EPWM2_B	OUTPUTXBAR2		OUTPUTXBAR2	PMBUSA_SCL	SPIA_CLK	SCIA_RX	FSIRXA_D0	I2CB_SCL	HIC_NOE	CANA_RX	HIC_D4	
GPIO4	EPWM3_A		MCAN_TX	OUTPUTXBAR3	CANA_TX	SPIB_CLK	EQEP2_STROBE	FSIRXA_CLK	CLB_OUTPUTXBAR6	HIC_BASESEL2		HIC_NWE	
GPIO5	EPWM3_B		OUTPUTXBAR3	MCAN_RX	CANA_RX	SPIA_STE	FSITXA_D1	CLB_OUTPUTXBAR5		HIC_A7	HIC_D4	HIC_D15	
GPIO6	EPWM4_A	OUTPUTXBAR4	SYNCOUT	EQEP1_A		SPIB_SOMI	FSITXA_D0		FSITXA_D1	HIC_NBE1	CLB_OUTPUTXBAR8	HIC_D14	
GPIO7	EPWM4_B		OUTPUTXBAR5	EQEP1_B		SPIB_SIMO	FSITXA_CLK	CLB_OUTPUTXBAR2		HIC_A6		HIC_D14	
GPIO8	EPWM5_A		ADCSOCAO	EQEP1_STROBE	SCIA_TX	SPIA_SIMO	I2CA_SCL	FSITXA_D1	CLB_OUTPUTXBAR5	HIC_A0	FSITXA_TDM_CLK	HIC_D8	
GPIO9	EPWM5_B	SCIB_TX	OUTPUTXBAR6	EQEP1_INDEX	SCIA_RX	SPIA_CLK		FSITXA_D0	LINB_RX	HIC_BASESEL0	I2CB_SCL	HIC_NRDY	
GPIO10	EPWM6_A		ADCSOCBO	EQEP1_A	SCIB_TX	SPIA_SOMI	I2CA_SDA	FSITXA_CLK	LINB_TX	HIC_NWE	FSITXA_TDM_D0	CLB_OUTPUTXBAR4	
GPIO11	EPWM6_B		OUTPUTXBAR7	EQEP1_B	SCIB_RX	SPIA_STE	FSIRXA_D1	LINB_RX	EQEP2_A	SPIA_SIMO	HIC_D6	HIC_NBE0	
GPIO12	EPWM7_A		MCAN_RX	EQEP1_STROBE	SCIB_TX	PMBUSA_CTL	FSIRXA_D0	LINB_TX	SPIA_CLK	CANA_RX	HIC_D13	HIC_INT	
GPIO13	EPWM7_B		MCAN_TX	EQEP1_INDEX	SCIB_RX	PMBUSA_ALERT	FSIRXA_CLK	LINB_RX	SPIA_SOMI	CANA_TX	HIC_D11	HIC_D5	
GPIO14	EPWM8_A	SCIB_TX		I2CB_SDA	OUTPUTXBAR3	PMBUSA_SDA	SPIB_CLK	EQEP2_A	LINB_TX	EPWM3_A	CLB_OUTPUTXBAR7	HIC_D15	
GPIO15	EPWM8_B	SCIB_RX		I2CB_SCL	OUTPUTXBAR4	PMBUSA_SCL	SPIB_STE	EQEP2_B	LINB_RX	EPWM3_B	CLB_OUTPUTXBAR6	HIC_D12	
GPIO16	SPIA_SIMO		OUTPUTXBAR7	EPWM5_A	SCIA_TX	SD1_D1	EQEP1_STROBE	PMBUSA_SCL	XCLKOUT	EQEP2_B	SPIB_SOMI	HIC_D1	
GPIO17	SPIA_SOMI		OUTPUTXBAR8	EPWM5_B	SCIA_RX	SD1_C1	EQEP1_INDEX	PMBUSA_SDA	CANA_TX			HIC_D2	

Table 3-12. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO18_X2	SPIA_CLK	SCIB_TX	CANA_RX	EPWM6_A	I2CA_SCL	SD1_D2	EQEP2_A	PMBUSA_CTL	XCLKOUT	LINB_TX	FSITXA_TDM_CLK	HIC_INT	X2
GPIO19_X1	SPIA_STE	SCIB_RX	CANA_TX	EPWM6_B	I2CA_SDA	SD1_C2	EQEP2_B	PMBUSA_ALERT	CLB_OUTPUTXBAR1	LINB_RX	FSITXA_TDM_D0	HIC_NBE0	X1
GPIO20	EQEP1_A				SPIB_SIMO	SD1_D3	MCAN_TX						
GPIO21	EQEP1_B				SPIB_SOMI	SD1_C3	MCAN_RX						
GPIO22	EQEP1_STROBE		SCIB_TX		SPIB_CLK	SD1_D4	LINA_TX	CLB_OUTPUTXBAR1	LINB_TX	HIC_A5	EPWM4_A	HIC_D13	
GPIO23	EQEP1_INDEX		SCIB_RX		SPIB_STE	SD1_C4	LINA_RX	CLB_OUTPUTXBAR3	LINB_RX	HIC_A3	EPWM4_B	HIC_D11	
GPIO24	OUTPUTXBAR1	EQEP2_A		EPWM8_A	SPIB_SIMO	SD2_D1	LINB_TX	PMBUSA_SCL	SCIA_TX	ERRORSTS		HIC_D3	
GPIO25	OUTPUTXBAR2	EQEP2_B		EQEP1_A	SPIB_SOMI	SD2_C1	FSITXA_D1	PMBUSA_SDA	SCIA_RX		HIC_BASESEL0		
GPIO26	OUTPUTXBAR3	EQEP2_INDEX		OUTPUTXBAR3	SPIB_CLK	SD2_D2	FSITXA_D0	PMBUSA_CTL	I2CA_SDA		HIC_D0	HIC_A1	
GPIO27	OUTPUTXBAR4	EQEP2_STROBE		OUTPUTXBAR4	SPIB_STE	SD2_C2	FSITXA_CLK	PMBUSA_ALERT	I2CA_SCL		HIC_D1	HIC_A4	
GPIO28	SCIA_RX		EPWM7_A	OUTPUTXBAR5	EQEP1_A	SD2_D3	EQEP2_STROBE	LINA_TX	SPIB_CLK	ERRORSTS	I2CB_SDA	HIC_NOE	
GPIO29	SCIA_TX		EPWM7_B	OUTPUTXBAR6	EQEP1_B	SD2_C3	EQEP2_INDEX	LINA_RX	SPIB_STE	ERRORSTS	I2CB_SCL	HIC_NCS	AUXCLKIN
GPIO30	CANA_RX		SPIB_SIMO	OUTPUTXBAR7	EQEP1_STROBE	SD2_D4	FSIRXA_CLK	MCAN_RX	EPWM1_A		HIC_D8		
GPIO31	CANA_TX		SPIB_SOMI	OUTPUTXBAR8	EQEP1_INDEX	SD2_C4	FSIRXA_D1	MCAN_TX	EPWM1_B		HIC_D10		
GPIO32	I2CA_SDA		SPIB_CLK	EPWM8_B	LINA_TX	SD1_D2	FSIRXA_D0	CANA_TX	PMBUSA_SDA	ADCSOCBO		HIC_INT	
GPIO33	I2CA_SCL		SPIB_STE	OUTPUTXBAR4	LINA_RX	SD1_C2	FSIRXA_CLK	CANA_RX	EQEP2_B	ADCSOCAO	SD1_C1	HIC_D0	
GPIO34	OUTPUTXBAR1				PMBUSA_SDA					HIC_NBE1	I2CB_SDA	HIC_D9	
GPIO35	SCIA_RX		I2CA_SDA	CANA_RX	PMBUSA_SCL	LINA_RX	EQEP1_A	PMBUSA_CTL	EPWM5_B	SD2_C1	HIC_NWE	TDI	
GPIO37	OUTPUTXBAR2		I2CA_SCL	SCIA_TX	CANA_TX	LINA_TX	EQEP1_B	PMBUSA_ALERT			HIC_NRDY	TDO	
GPIO39					MCAN_RX	FSIRXA_CLK	EQEP2_INDEX		CLB_OUTPUTXBAR2	SYNCOUT	EQEP1_INDEX	HIC_D7	
GPIO40	SPIB_SIMO			EPWM2_B	PMBUSA_SDA	FSIRXA_D0	SCIB_TX	EQEP1_A	LINB_TX		HIC_NBE1	HIC_D5	
GPIO41				EPWM2_A	PMBUSA_SCL	FSIRXA_D1	SCIB_RX	EQEP1_B	LINB_RX	HIC_A4	SPIB_SOMI	HIC_D12	
GPIO42		LINA_RX	OUTPUTXBAR5	PMBUSA_CTL	I2CA_SDA			EQEP1_STROBE	CLB_OUTPUTXBAR3		HIC_D2	HIC_A6	
GPIO43			OUTPUTXBAR6	PMBUSA_ALERT	I2CA_SCL		PMBUSA_ALERT	EQEP1_INDEX	CLB_OUTPUTXBAR4	SD2_D3	HIC_D3	HIC_A7	
GPIO44			OUTPUTXBAR7	EQEP1_A	PMBUSA_SDA	FSITXA_CLK	PMBUSA_CTL	CLB_OUTPUTXBAR3	FSIRXA_D0	HIC_D7	LINB_TX	HIC_D5	
GPIO45			OUTPUTXBAR8			FSITXA_D0	PMBUSA_ALERT	CLB_OUTPUTXBAR4		SD2_C3		HIC_D6	
GPIO46			LINA_TX	MCAN_TX		FSITXA_D1	PMBUSA_SDA			SD2_C4		HIC_NWE	
GPIO47			LINA_RX	MCAN_RX		CLB_OUTPUTXBAR2	PMBUSA_SCL			SD2_D4	FSITXA_TDM_CLK	HIC_A6	
GPIO48	OUTPUTXBAR3		CANA_TX		SCIA_TX	SD1_D1	PMBUSA_SDA					HIC_A7	
GPIO49	OUTPUTXBAR4		CANA_RX		SCIA_RX	SD1_C1	LINA_RX			SD2_D1	FSITXA_D0	HIC_D2	
GPIO50	EQEP1_A			MCAN_TX	SPIB_SIMO	SD1_D2	I2CB_SDA			SD2_D2	FSITXA_D1	HIC_D3	

Table 3-12. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO51	EQEP1_B			MCAN_RX	SPIB_SOMI	SD1_C2	I2CB_SCL			SD2_D3	FSITXA_CLK	HIC_D6	
GPIO52	EQEP1_STROBE			CLB_OUTPUTXBAR5	SPIB_CLK	SD1_D3	SYNCOUT			SD2_D4	FSIRXA_D0	HIC_NWE	
GPIO53	EQEP1_INDEX			CLB_OUTPUTXBAR6	SPIB_STE	SD1_C3	ADCSOCAO	CANA_RX		SD1_C1	FSIRXA_D1		
GPIO54	SPIA_SIMO			EQEP2_A	OUTPUTXBAR2	SD1_D4	ADCSOCBO	LINB_TX		SD1_C2	FSIRXA_CLK	FSITXA_TDM_D1	
GPIO55	SPIA_SOMI			EQEP2_B	OUTPUTXBAR3	SD1_C4	ERRORSTS	LINB_RX		SD1_C3		HIC_A0	
GPIO56	SPIA_CLK	CLB_OUTPUTXBAR7	MCAN_TX	EQEP2_STROBE	SCIB_TX	SD2_D1	SPIB_SIMO	I2CA_SDA	EQEP1_A	SD1_C4	FSIRXA_D1	HIC_D6	
GPIO57	SPIA_STE	CLB_OUTPUTXBAR8	MCAN_RX	EQEP2_INDEX	SCIB_RX	SD2_C1	SPIB_SOMI	I2CA_SCL	EQEP1_B		FSIRXA_CLK	HIC_D4	
GPIO58				OUTPUTXBAR1	SPIB_CLK	SD2_D2	LINA_TX	CANA_TX	EQEP1_STROBE	SD2_C2	FSIRXA_D0	HIC_NRDY	
GPIO59				OUTPUTXBAR2	SPIB_STE	SD2_C2	LINA_RX	CANA_RX	EQEP1_INDEX	SD2_C3	FSITXA_TDM_D1		
GPIO60			MCAN_TX	OUTPUTXBAR3	SPIB_SIMO	SD2_D3				SD2_C4		HIC_A0	
GPIO61			MCAN_RX	OUTPUTXBAR4	SPIB_SOMI	SD2_C3					CANA_RX		
AIO224		SD2_D3										HIC_A3	
AIO225		SD2_C2										HIC_NWE	
AIO226		SD2_D4										HIC_A1	
AIO227		SD1_C3										HIC_NBE0	
AIO228		SD2_C1										HIC_A0	
AIO230		SD1_C4										HIC_BASESEL2	
AIO231		SD1_C1										HIC_BASESEL1	
AIO232		SD1_D4										HIC_BASESEL0	
AIO233		SD2_D1										HIC_A4	
AIO237		SD1_D2										HIC_A6	
AIO238		SD2_C3										HIC_NCS	
AIO239		SD1_D1										HIC_A5	
AIO240		SD2_C1										HIC_NBE1	
AIO241		SD2_C1										HIC_NBE1	
AIO242		SD2_D2										HIC_A2	
AIO244		SD1_D3										HIC_A7	
AIO245		SD1_C2										HIC_NOE	
AIO252		SD2_C4											

3.9 Analog Multiplexing Changes

Table 3-14 outlines the differences and similarities that exist in the analog mux between F28003x and F28002x for the 80-Pin PN, 64-Pin PM and 48-Pin PT packages. The legend for the table is Table 3-13. The main change is the absence of ADCB in F28002x.

Table 3-13. Mux Legend

Color	Description
	mux function common for both devices
	mux function applicable only for F28002x
	mux function applicable only for F28003x

Table 3-14. F28002x and F28003x 80-Pin PN, 64-Pin PM and 48-Pin PT Analog Mux Table Differences

(F28002x Pin Name)	Package Pin			ADC			Comparator Subsystem (MUX)				
F28003x Pin Name	80 PN	64 PM	48 PT	A	B	C	High Positive	High Negative	Low Positive	Low Negative	AIO Input
VREFHI	20	16	12								
VREFLO	21	17	13	A13		C13					
Analog Group 1							**CMP1**				
(A6) A6	10	6	4	A6	-	-	CMP1 (HPMXSEL=2)		CMP1 (LPMXSEL=2)		AIO228
(A2/C9) A2/B6/C9	13	9	6	A2	B6	C9	CMP1 (HPMXSEL=0)		CMP1 (LPMXSEL=0)		AIO224
(A15/C7) A15/B9/C7	14	10	7	A15	B9	C7	CMP1 (HPMXSEL=3)	CMP1 (HNMXSEL=0)	CMP1 (LPMXSEL=3)	CMP1 (LNMXSEL=0)	AIO233
(A11/C0) A11/B10/C0	16	12	8	A11	B10	C0	CMP1 (HPMXSEL=1)	CMP1 (HNMXSEL=1)	CMP1 (LPMXSEL=1)	CMP1 (LNMXSEL=1)	AIO237
(A1) A1/B7/DACB_OUT	18	14	10	A1	B7	-	CMP1 (HPMXSEL=4)		CMP1 (LPMXSEL=4)		AIO232
Analog Group 2							**CMP2**				
(A10/C10) A10/B1/C10	29	25	21	A10	B1	C10	CMP2 (HPMXSEL=3)	CMP2 (HNMXSEL=0)	CMP2 (LPMXSEL=3)	CMP2 (LNMXSEL=0)	AIO230
Analog Group 3							**CMP3**				
(C6) B2/C6	11	7	4	-	B2	C6	CMP3 (HPMXSEL=0)		CMP3 (LPMXSEL=0)		AIO226
(A3/C5/VDAC) A3/B3/C5/VDAC	12	8	5	A3	B3	C5	CMP3 (HPMXSEL=3) CMP3 (HPMXSEL=5)	CMP3 (HNMXSEL=0)	CMP3 (LPMXSEL=3) CMP3 (LPMXSEL=5)	CMP3 (LNMXSEL=0)	AIO242

Table 3-14. F28002x and F28003x 80-Pin PN, 64-Pin PM and 48-Pin PT Analog Mux Table Differences (continued)

(F28002x Pin Name)	Package Pin			ADC			Comparator Subsystem (MUX)				
F28003x Pin Name	80 PN	64 PM	48 PT	A	B	C	High Positive	High Negative	Low Positive	Low Negative	AIO Input
(A14/C4) A14/B14/C4	15	11	-	A14	B14	C4	CMP3 (HPMXSEL=4)		CMP3 (LPMXSEL=4)		AIO239
(A5/C2) A5/B12/C2	17	13	9	A5	B12	C2	CMP3 (HPMXSEL=1) ***CMP2*** (HPMXSEL=5)	CMP3 (HNMXSEL=1)	CMP3 (LPMXSEL=1) ***CMP2*** (LPMXSEL=5)	CMP3 (LNMXSEL=1)	AIO244
(A0/C15) A0/B15/C15/ DACA_OUT	19	15	11	A0	B15	C15	CMP3 (HPMXSEL=2)		CMP3 (LPMXSEL=2)		AIO231
Analog Group 4							**CMP4**				
(A7/C3) A7/C3	23	19	15	A7	-	C3	CMP4 (HPMXSEL=1)	CMP4 (HNMXSEL=1)	CMP4 (LPMXSEL=1)	CMP4 (LNMXSEL=1)	AIO245
Combined Analog Group 2/4							**CMP2/4**				
(A12/C1) A12/C1	22	18	14	A12	-	C1	CMP2 (HPMXSEL=1) CMP4 (HPMXSEL=2)	CMP2 (HNMXSEL=1)	CMP2 (LPMXSEL=1) CMP4 (LPMXSEL=2)	CMP2 (LNMXSEL=1)	AIO238 AIO248
(A8/C11) A8/B0/C11	24	20	16	A8	B0	C11	CMP2 (HPMXSEL=4) CMP4 (HPMXSEL=4)		CMP2 (LPMXSEL=4) CMP4 (LPMXSEL=4)		AIO241
(A4/C14) A4/B8/C14	27	23	19	A4	B8	C14	CMP2 (HPMXSEL=0) CMP4 (HPMXSEL=3)	CMP4 (HNMXSEL=0)	CMP2 (LPMXSEL=0) CMP4 (LPMXSEL=3)	CMP4 (LNMXSEL=0)	AIO225
(A9/C8) A9/B4/C8	28	24	20	A9	B4	C8	CMP2 (HPMXSEL=2) CMP4 (HPMXSEL=0)		CMP2 (LPMXSEL=2) CMP4 (LPMXSEL=0)		AIO227 AIO236
Other Analog											
B5/GPIO20	33	-	-	-	B5	-	***CMP1*** (HPMXSEL=5)		***CMP1*** (LPMXSEL=5)		
B11/GPIO21	34	-	-	-	B11	-	***CMP4*** (HPMXSEL=5)		***CMP4*** (LPMXSEL=5)		
TempSensor	-	-	-	-		C12					

4 Application Code Migration From F28002x to F28003x

The following section describes code changes when migrating from F28002x to F28003x. Software examples for the new features in F28003x are also discussed in this section.

4.1 C2000Ware Header Files

Header files for both F28003x and F28002x devices are available in C2000Ware under the device_support sub directory.

4.2 Linker Command Files

Linker command files for both F28003x and F28002x devices are available in C2000Ware under the device_support sub directory. Both F28002x and F28003x, have to be compiled to the Embedded Application Binary Interface (EABI) format, section names would also need to conform to the EABI standard.

4.3 C2000Ware Examples

C2000Ware has examples specific for both F28003x and F28002x devices.

5 Specific Use Cases Related to F28003x New Features

This section outlines the new examples in C2000Ware for the F28003x device to support the new features on F28003x that do not exist on F28002x/F28004x.

5.1 AES

C2000Ware has examples that demonstrate the encryption and decryption capabilities of the AES module.

5.2 MCAN

C2000Ware has loopback, transmit and receive examples that illustrate MCAN operation.

5.3 EPG

C2000Ware has examples that demonstrate the functionality of the EPG module.

6 EABI Support

Both F28002x and F28003x devices use the Embedded Application Binary Interface (EABI) format for the binary executable output. All F28002x and F28003x libraries supplied by TI will be released as EABI. Future F28003x libraries created by customers should be generated and compiled as EABI format as well.

6.1 Flash API

F28002x has one Flash bank. F28003x has three Flash banks. Hence, the F28003x Flash API library (FlashAPI_F28003x_FPU32.lib) supports erase, program and verify operations for the Flash Bank0, 1 and 2 address ranges. Compared to the F28002x Flash API library (Flash_API_F28002x_FPU32.lib), the F28003x Flash API is enhanced to return an error when an invalid address is provided for erase, blank-check, program and verify functions. Also, the F28003x Flash API is enhanced to return an error when an invalid programming mode is provided for program operation. Fapi_getLibraryInfo() in FlashAPI_F28003x_FPU32.lib returns the Flash API minor version as 58 (F28002x Flash API returns 57 as the API minor version). Both F28002x and F28003x Flash API library is compiled for EABI format. Note that F28002x and F28003x have the same Bank0 memory map and sector sizes. Also, the Flash wait-state configuration requirement is the same between the two devices. These features are summarized in Table 6-1.

Table 6-1. Flash API Differences

Feature	F28002x	F28003x
Library Name	FlashAPI_F28002x_FPU32.lib	FlashAPI_F28003x_FPU32.lib
Library Executable Output	EABI	EABI
Erase, Blank-check, Program and Verify	Operation on one bank	Operation on three banks
Flash Wait States	Same wait states on both devices	
FlashAPI Minor Version	57	58

7 References

- Texas Instruments: *TMS320F28003x Microcontrollers Technical Reference Manual* (SPRUIW9)
- Texas Instruments: *TMS320F2838x Microcontrollers Technical Reference Manual*
- Texas Instruments: *TMS320F28003x Microcontrollers Data Sheet*

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