User's Guide

Jacinto7 J721E/DRA829/TDA4VM Evaluation Module (EVM)

ABSTRACT

This technical user's guide describes the hardware architecture and configuration options of the J721E/DRA929/TDA4VM EVM.

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Trademarks

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1 Introduction

The Jacinto7 J721E (DRA829/TDA4xM) EVM is a standalone test, development, and evaluation module system that enables developers to write software and develop hardware around Jacinto7 J721E (DRA829/TDA4xM) processor subsystem. The J721E processor is a KeyStone™ III-based Multicore Arm® System-on-Chip (SoC). It is a super-set processor/device and may be available is different configurations targeted for specific markets. This EVM will support development of the super-set device (J721E) as well as the market specific devices (DRA829/TDA4xM). Many features of the J721E system are available on the EVM, which gives developers the basic resources needed for most general-purpose type.

The J721E EVM is comprised of:

- J721E System On Module (SOM) board
- Jacinto7 Common Processor Board (CPB)
- Quad-Port Ethernet board (QPENet)

J721E EVM sub system has been designed to enable customers to evaluate the Processor's performance with flexibility. To have flexibility while developing the system, different interface/expansion boards have been designed. Some examples include:

- Infotainment Expansion Board
- Gateway/Ethernet Switch/Industrial (GESI) Expansion Board
- Fusion CSI2 Expansion Board(s)

1.1 Key Features

The J721E EVM is a high performance, standalone development platform that enables users to evaluate the Texas Instrument's Keystone III System-on-Chip (SoC).

Below are the EVM's key features:

- Processor:
  - J721E (DRA829/TDA4xM), 24 mm x 24 mm, 0.8 mm pitch, 827-pin FCBGA
  - Support for corresponding socket
- Power Supply:
  - 12 V DC nominal input (6 V-28 V input range)
  - Optimized Power Management Solution for Processor
  - Integrated Power Measurement
- Memory:
  - DRAM, LPDDR4-3733, 4GByte total memory, support inline ECC
  - 2x Octal-SPI NOR flash, 512 Mb memory (8 bit) + 512 Mb memory (4 bit)
  - HyperFlash + HyerRAM, 512 Mb flash memory + 256 Mb RAM
  - UFS Flash memory, 32GByte, 2Lane, Gear3
  - eMMC Flash memory, 16 GB memory, v5.1 compliant
  - MicroSD Card Cage, UHS-I
  - Inter-Integrated Circuit (I2C) EEPROM, 1 Mbit
- JTAG/Emulator:
  - Integrated XDS110 Emulator support
  - External emulator through 60pin MIPI Connector
  - Trace Support through 60pin MIPI Connector
  - Includes adapters for 14pin and 20pin CTI

- Supported Interfaces and Peripherals:
  - 4x CAN Interfaces, full CAN-FD support
  - 1x USB3.1 Type C Interface, support DFP, DRP, UFP modes
  - 4x USB2.0 Host Interfaces (2x for external cables)
  - 1x Display Port, up to 4K resolution with MST support
  - 1x FPD-Link Panel Interface, Gen3
  - 1x Audio Codec (PCM3168A), supports 2x Line Inputs, 4x Microphone Inputs, 2x Line Outputs, 6x Headphone Outputs
  - 1x FPD-Link Radio Tuner Interface
  - 2x PCIe Card Slot, 1x PCIe M.2 Slot (M-Key), all Gen3
  - 5x Gbit Ethernet, 1x RGMII/DP83867 + 1x QSGMII/VSC8514
  - 6x Universal Asynchronous Receiver/Transmitter (UART) terminals via 2x USB FTDI (UART-over-USB)
  - 2x I3C headers
  - 1x ADC Header
- Expansion Connectors to support application specific add-on boards
  - MLB, MLBP Expansion Interface
  - Image/Video Capture Expansion Interface
  - Apple Authentication Module Interface
  - General Expansion Interface
- REACH and RoHS Compliant

1.2 Thermal Compliance

There is elevated heat on the processor/heatsink, use caution particularly at elevated ambient temperatures! Although the processor/heatsink is not a burn hazard, caution should be used when handling the EVM due to increased heat in the area of the heatsink.

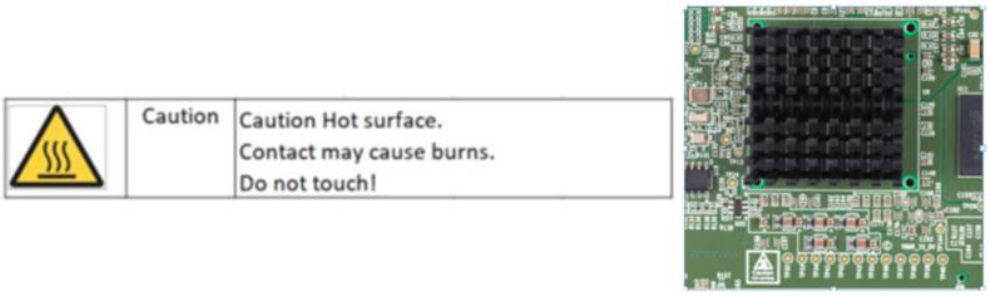


Figure 1-1. Thermal Caution

1.3 REACH Compliance

In compliance with the Article 33 provision of the EU REACH regulation, this EVM includes component(s) containing at least one Substance of Very High Concern (SVHC) above 0.1%. These uses from Texas Instruments do not exceed 1 ton per year. The SVHC's are listed in Table 1-1.

Table 1-1. REACH Compliance

Component Manufacturer	Component type	Component Part Number	SVHC Substance	SVHC CAS (when available)
Tensility	Power Cable	10-02937	Lead	7439-92-1
Rosenberger	FPD Link Connector	D4S20G-400A5-C	Lead	7439-92-1
Littelfuse	Power fuse	0154010.DR	Lead	7439-92-1

1.4 EMC, EMI, and ESD Compliance

Components installed on the product are sensitive to Electrostatic Discharge (ESD). It is recommended this product be used in an ESD controlled environment. This may include a temperature and/or humidity controlled environment to limit the buildup of ESD. It is also recommended to use ESD protection such as wrist straps and ESD mats when interfacing with the product.

The product is used in the basic electromagnetic environment as in laboratory conditions, and the applied standard is as per EN IEC 61326-1:2021.

2 J721E EVM Overview

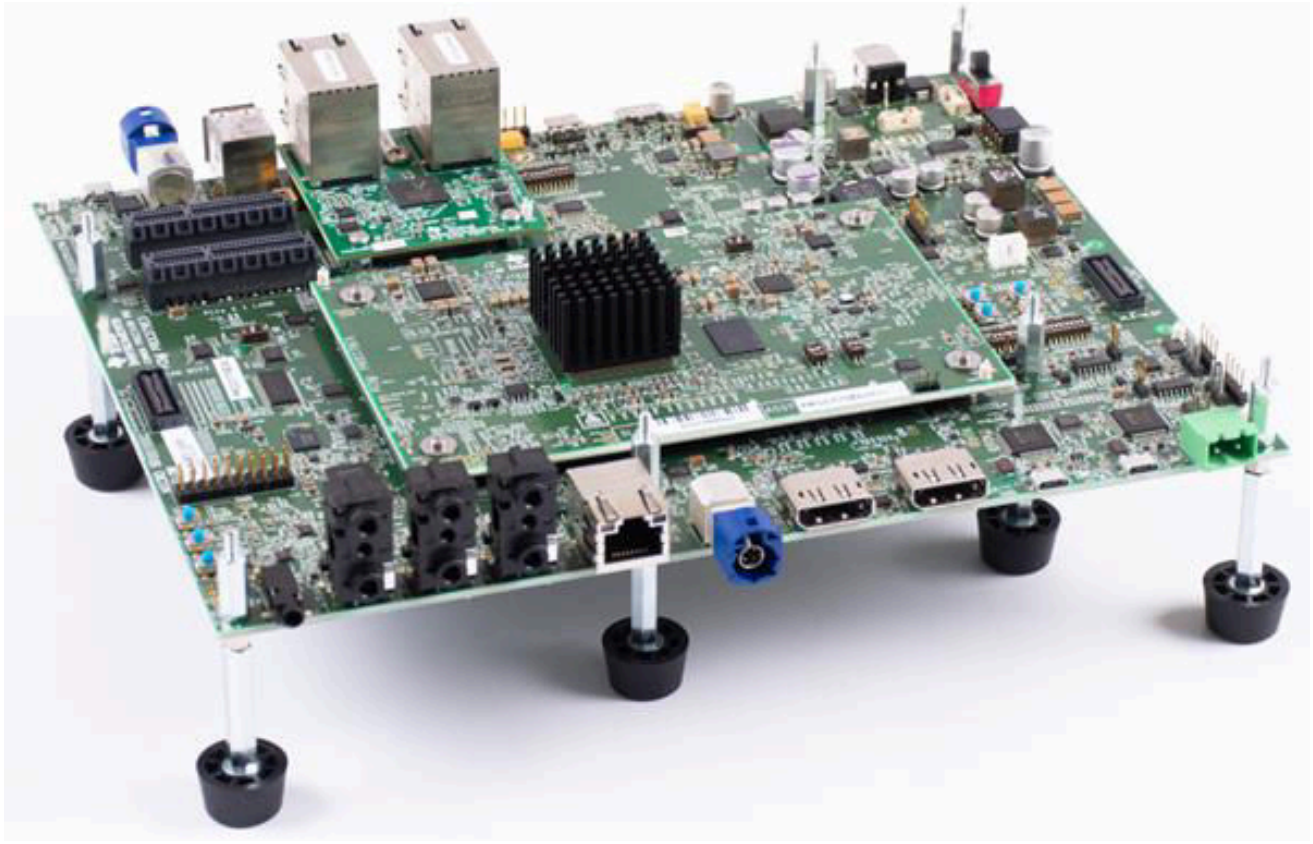
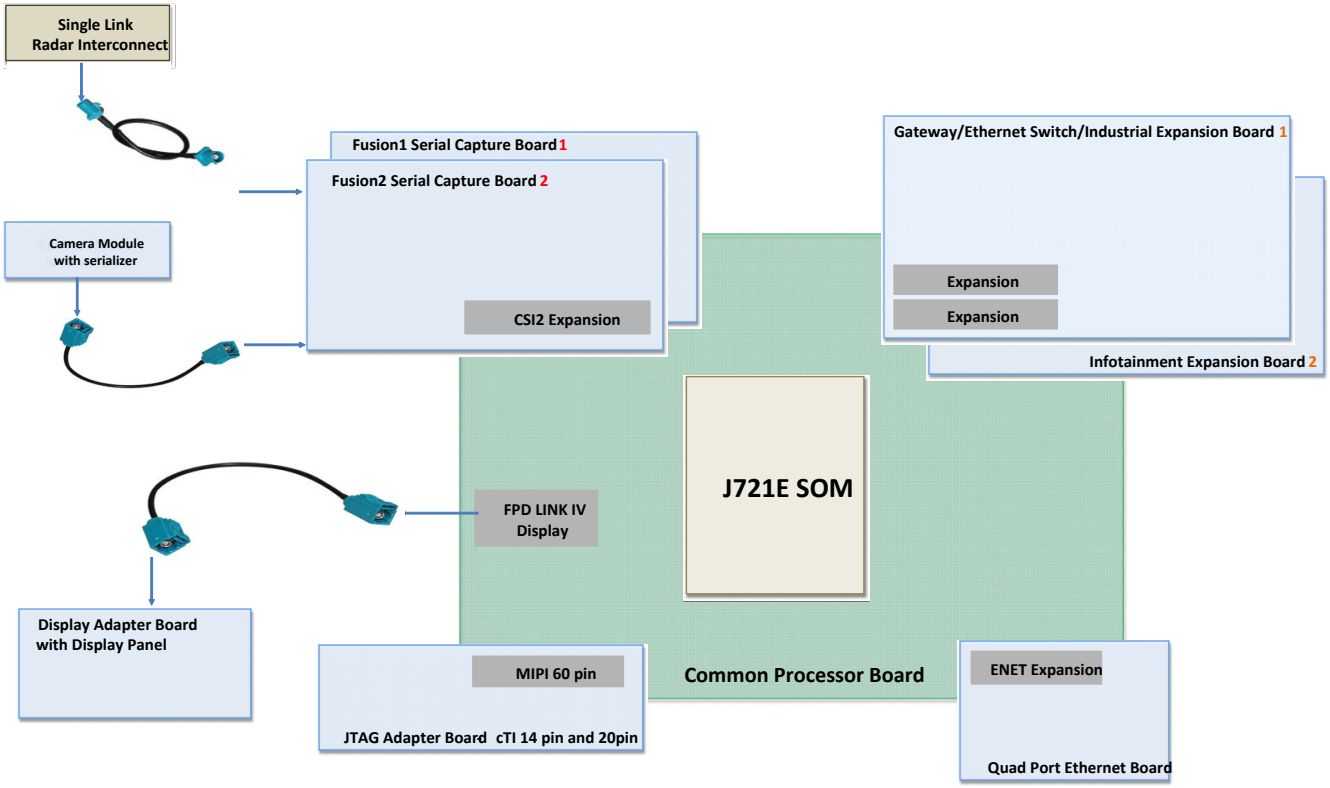


Figure 2-1. J721E EVM Board

Figure 2-2 shows the overall architecture of the J721E EVM.



A. Only one board can be connected to Expansion connector at a time.
B. Only one board can be connected to CSI2 Expansion connector at a time.

Figure 2-2. System Architecture Interface

The J721E EVM System on Module (SoM) board, a Jacinto7 Common Processor board, and Quad-Port Ethernet Board. Detailed descriptions of these cards are explained in the following sections.

2.1 J721E EVM Board Identification

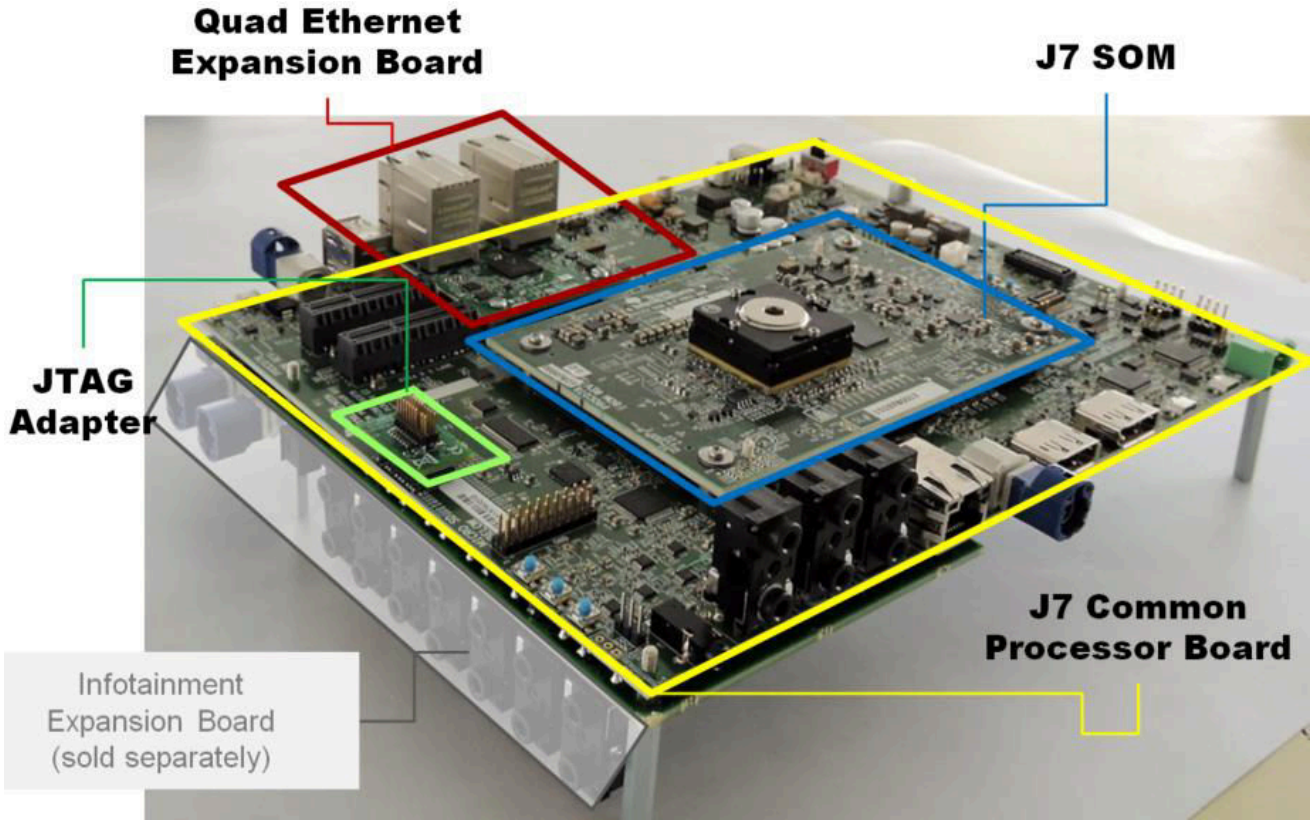


Figure 2-3. J721E EVM Board Identification (SOM, CPB, QP Ethernet)

2.2 J721E SOM Component Identification

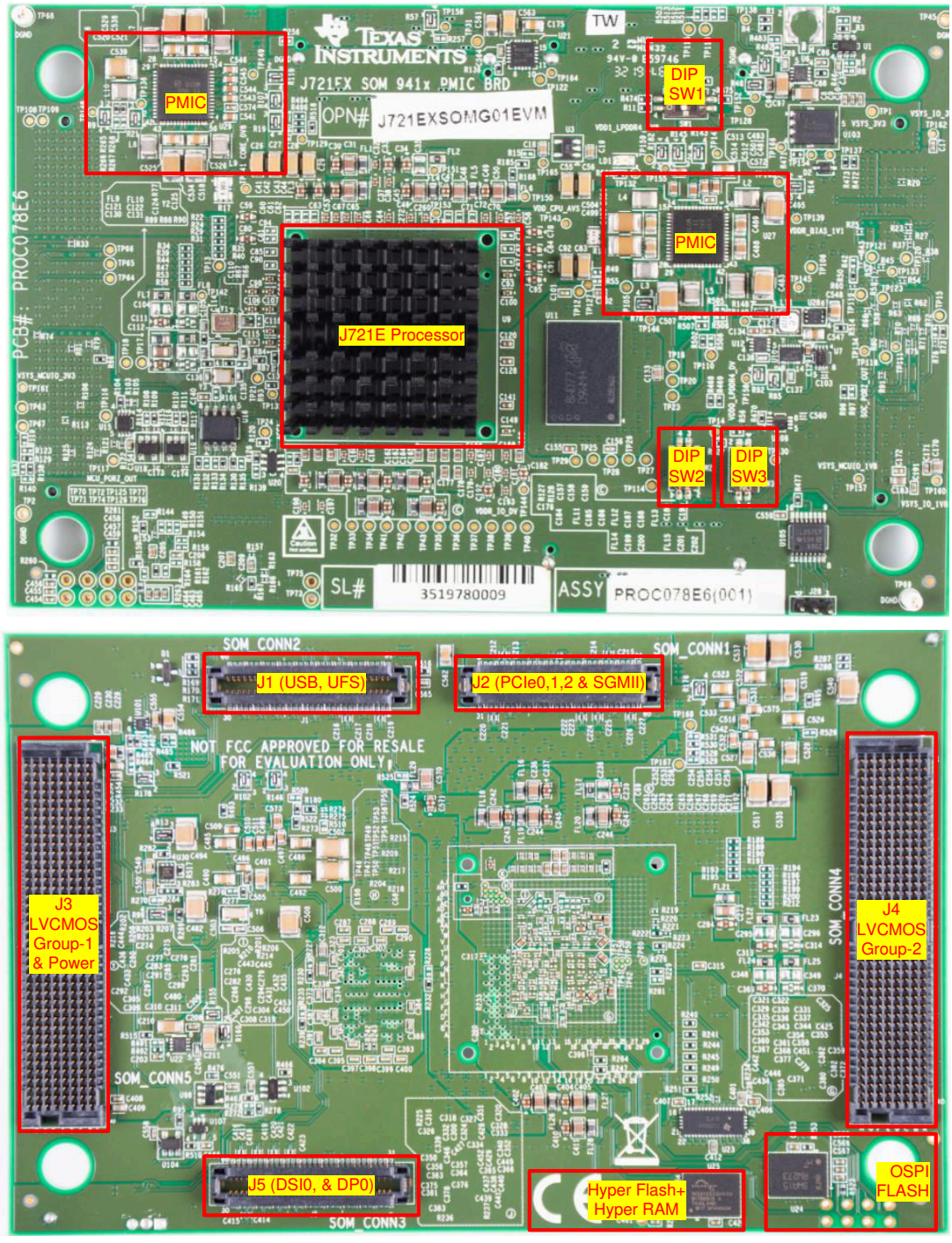


Figure 2-4. J721E SOM Component Identification

2.3 Jacinto7 Common Processor Components Identification

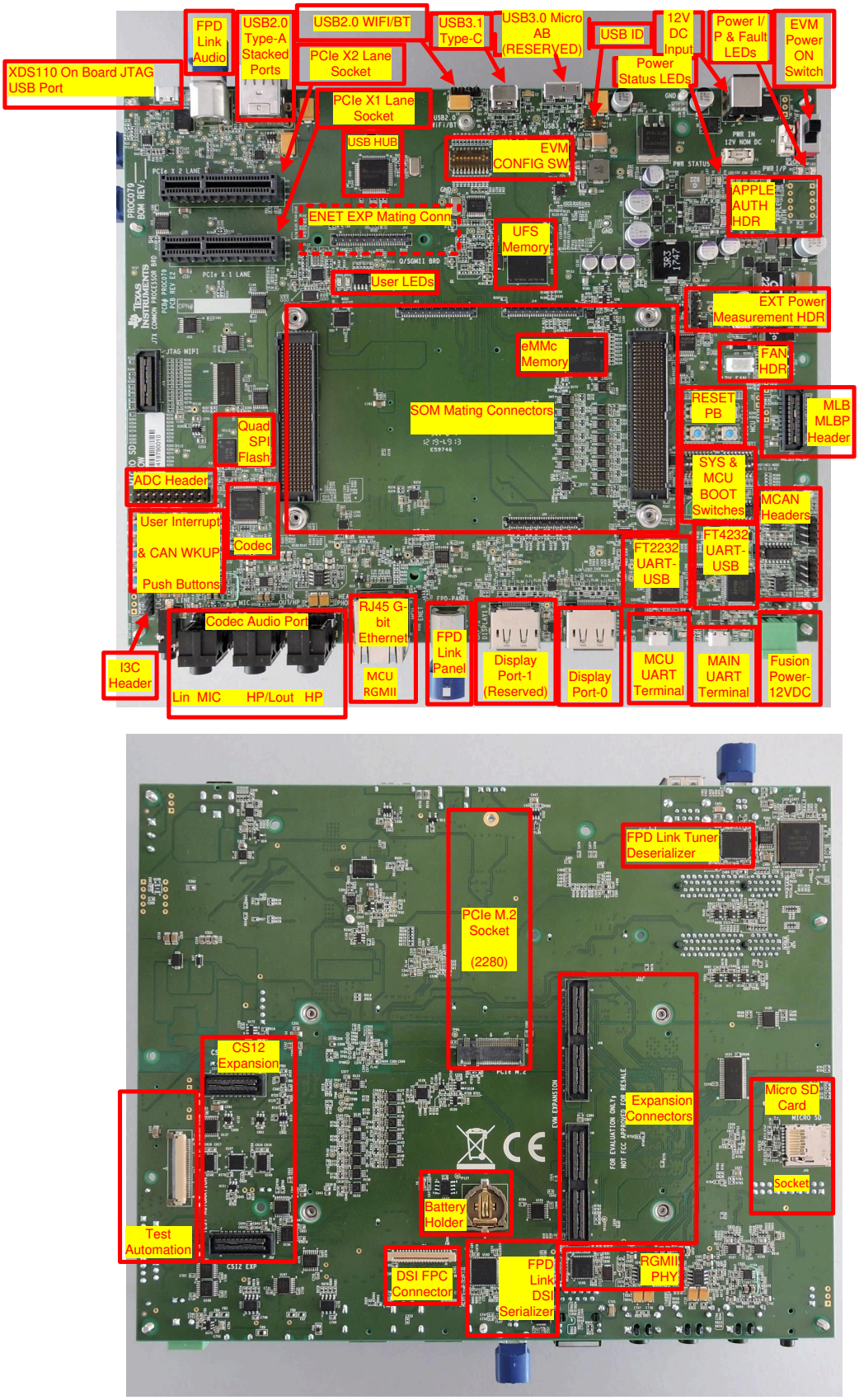


Figure 2-5. Jacinto7 Common Processor Component Identification

Because the Jacinto7 Common Processor board is used with different SOM boards featuring different Jacinto7 processors with different feature sets, some of the board's peripherals/interfaces may not be supported. For the J721E SOM, the following interfaces are not supported:

- USB 3.0 uAB (USB Type C, and 2x USB Type A interfaces are supported)
- 2nd DisplayPort interface (single DisplayPort interface is supported)

These interfaces are identified with a grey color in the component placement pictures (opposed to the yellow color).

2.4 Quad Ethernet Components Identification

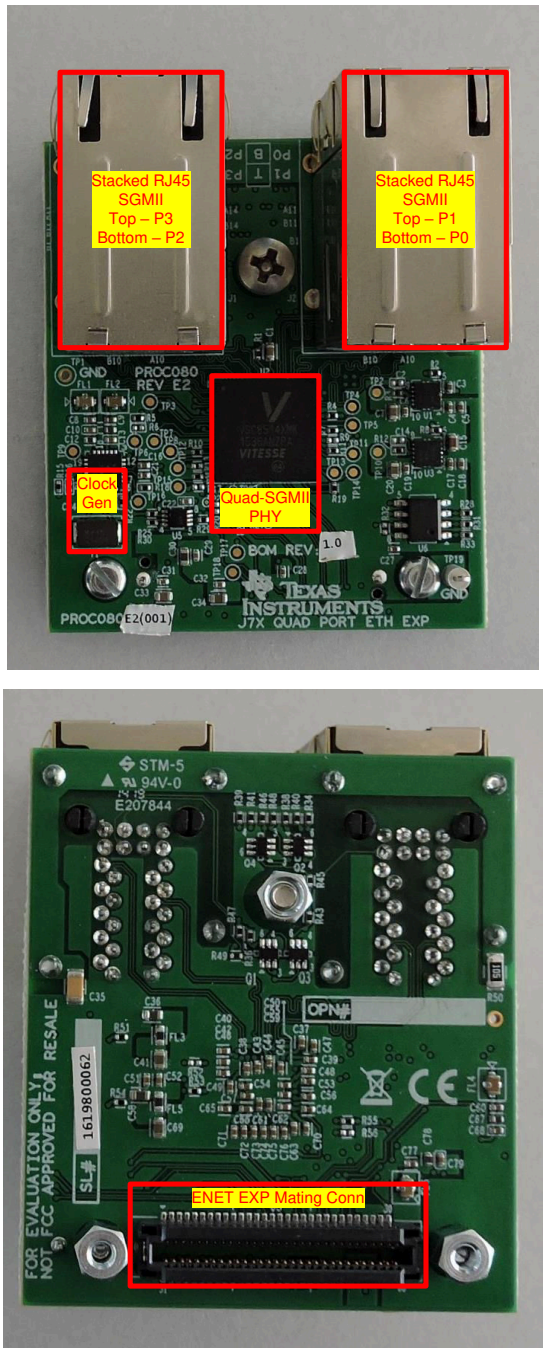


Figure 2-6. Quad Ethernet Component Identification

3 EVM User Setup/Configuration

3.1 Power Requirements

This EVM supports a wide input range of 6 V to 28 V. There is a DC Jack provided for supplying the input power (J7). An external power supply is required to power the EVM but is not included as part of the EVM kit. The external power supply requirements are:

- Power Jack: 2.5 mm ID, 5.5 mm OD
- Nom Voltage: 12 VDC, Recommended Minimum Current: 5000 mA

Table 3-1. Recommended External Power Supply

DigiKey Part No	Manufacturer	Manufacturer Part No
SDI65-12-U-P6-ND	CUI Inc.	SDI65-12-U-P6
SDI65-12-UD-P6-ND	CUI Inc.	SDI65-12-UD-P6

EVM's 2.5 x 5.5-mm DC barrel jack connector (J7) supports 10-A current rating. Polarity outside barrel is Negative/GND, inside post is Positive/PWR.

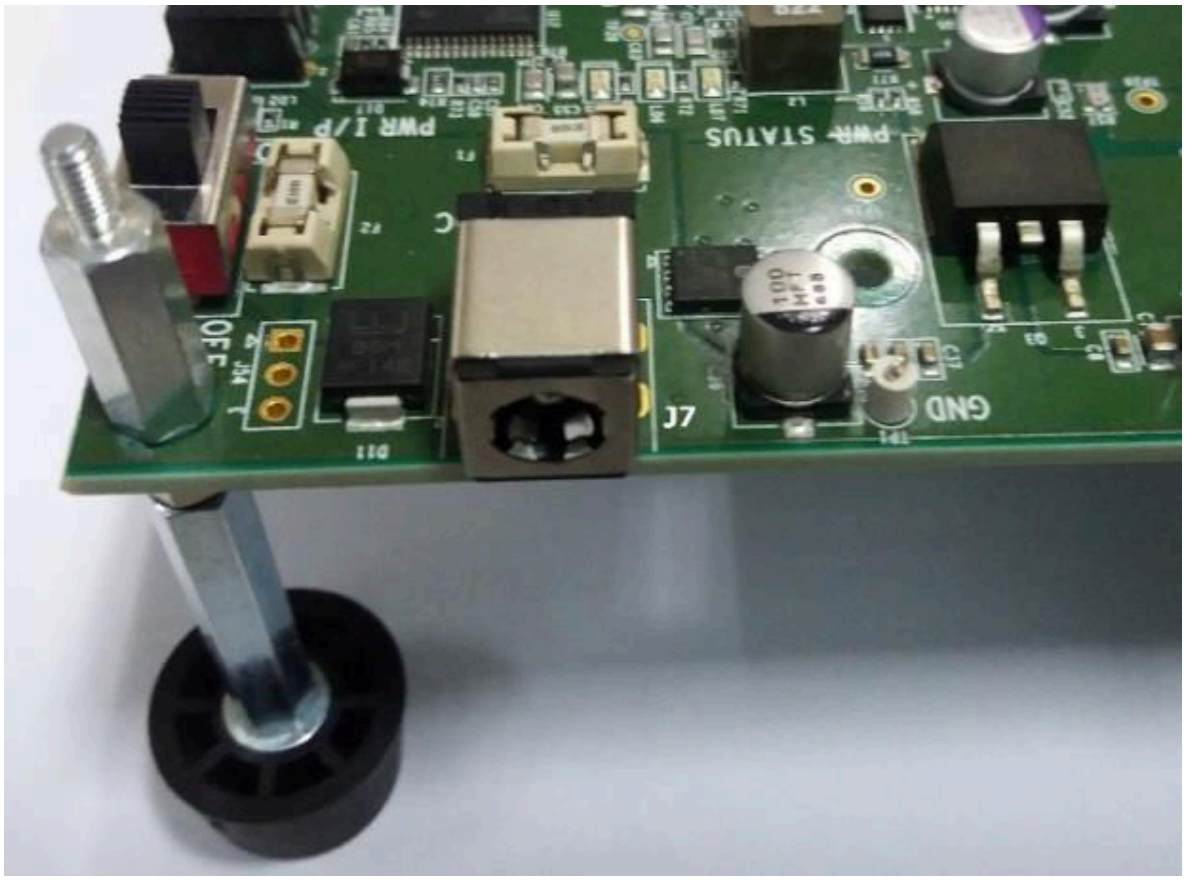


Figure 3-1. Connector Used for Power Input

3.2 Power ON Switch and Power LEDs

The power to the EVM is controlled by the power ON/OFF switch (SW2) on the CPB. To turn the board ON, slide the switch in the direction as shown in Figure 3-2.

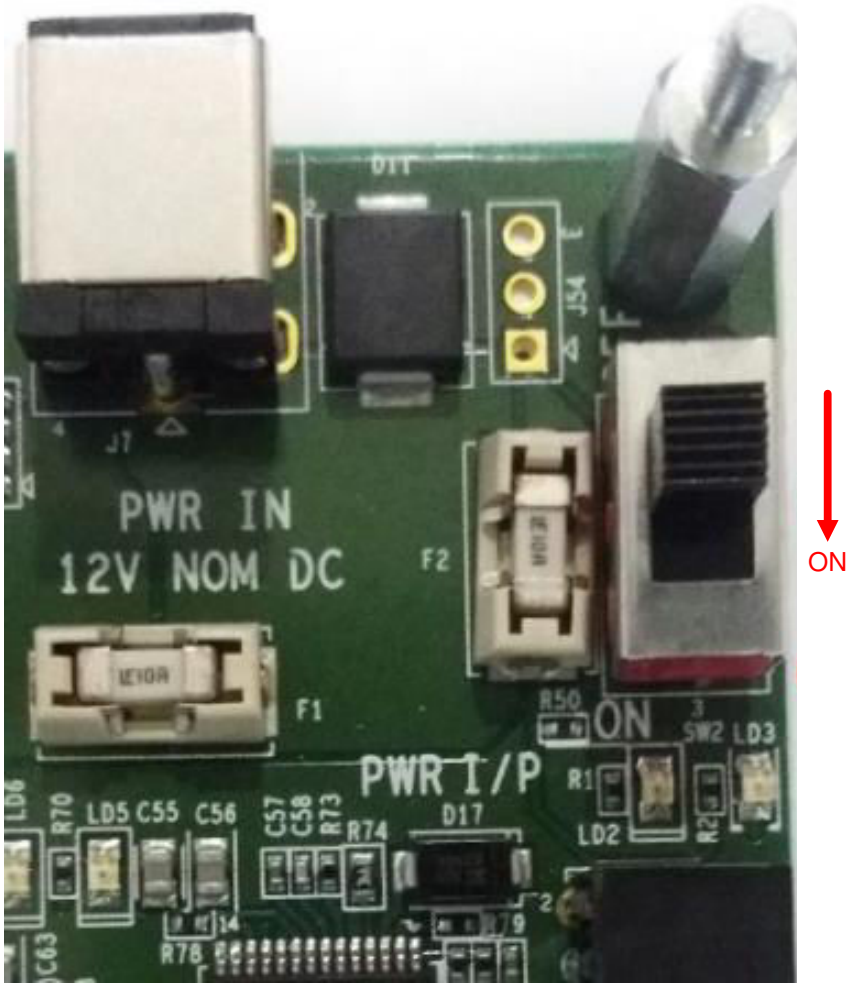


Figure 3-2. Power ON/OFF Switch

3.2.1 Over Voltage and Under Voltage Protection Circuit

The voltage protection circuit on the EVM protects the board from overvoltage, under voltage and transient voltage input cases. The safe operation input voltage range is 6 V to 28 V. A fault indication and power good LEDs are provided to indicate the power status.

Table 3-2. Power LED Status

LED	ON Status	OFF Status
LD2	Board Power on	Board Power off
LD3	Input voltage is >28 V or <6 V	Input voltage is within the limit

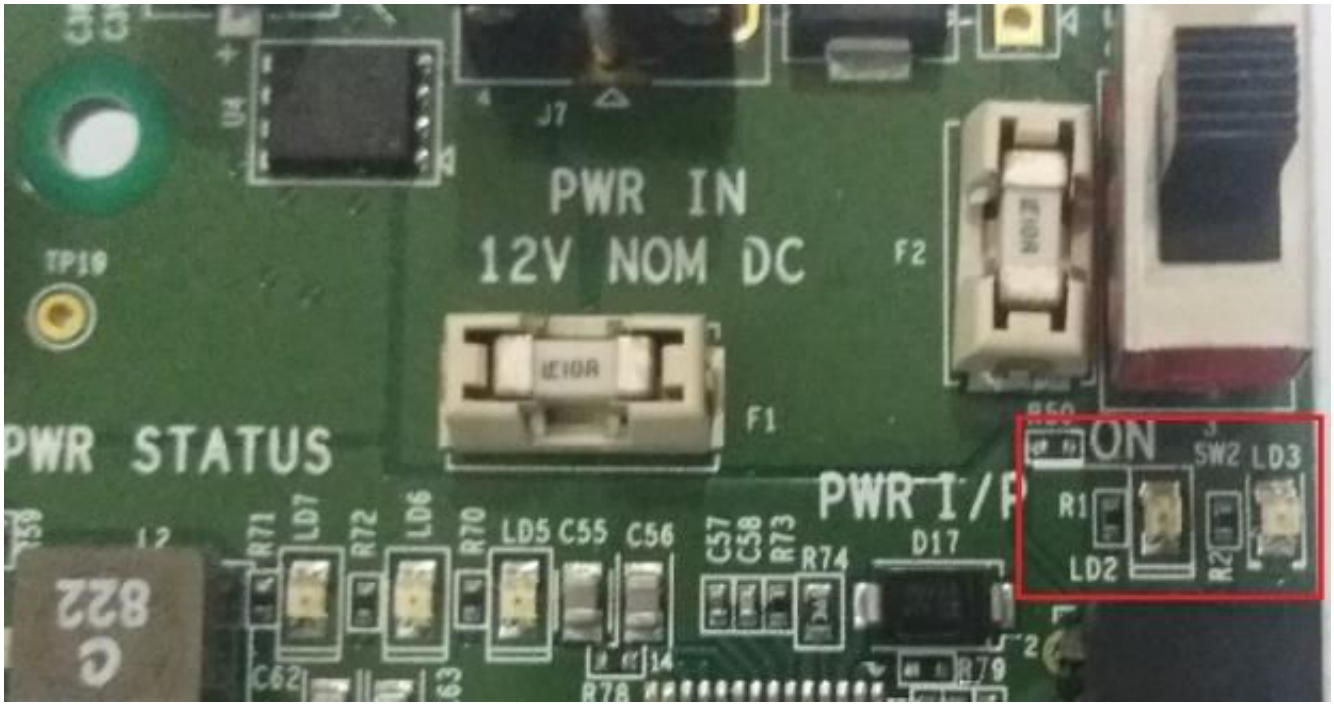


Figure 3-3. Power ON/Fault LEDs

3.2.2 Power Regulators and Power Status LEDs

The processor Card utilizes an array of DC-DC converters to supply the various memories, clocks and other components on the Card with the necessary voltage and the power required.

Dual Buck controller LM5140-Q1 provides the primary stage power conversion (12 V to 5 V / 3.3 V). These 3.3 V and 5 V is the primary voltages for the SoM power management resources.

Buck-Boost controller LM5175 and another Buck controller LM5141 provides 12 V and 3.3 V supplies to the expansion connectors. The power good signals of these power regulators are used to generate the SoC PORz.

Multiple power-indication LEDs are provided on board to give users positive confirmation of the status of output of major supplies. The LEDs indicated power in the various domains.

Table 3-3. Power LEDs

Sl No	LED	Power Status	Sch Net Name
1	LD2	Input Power On/Off	VINPUT
2	LD7	Regulated Power On/Off	VSYS_3V3
3	LD5	SoC Main Domain On/Off	VSYS_IO_3V3
4	LD6	SoC MCU Domain On/Off	VSYS_MCUIO_3V3

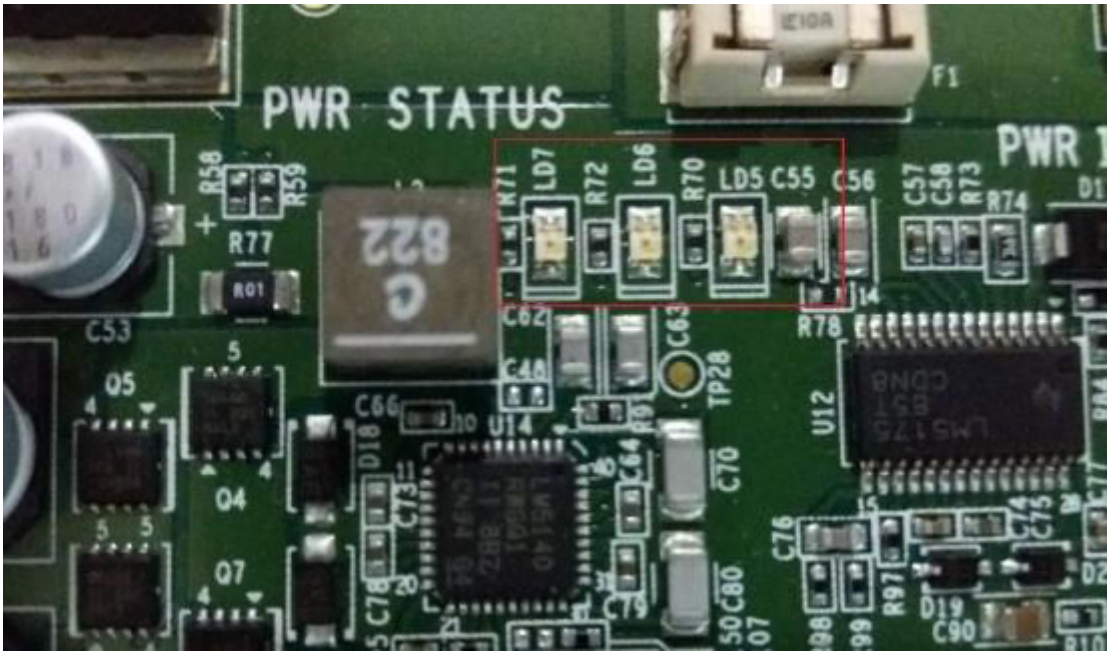


Figure 3-4. Power Status LEDs

Test points for each system power rails are provided on the Common Processor Board (CPB) and are mentioned in Table 3-4. Location for each can be identified by searching the assembly drawing for the test point reference number.

Table 3-4. Power Test Points

Power Supply	Test Point	Nominal Voltage
VINPUT	TP20	12.0V
VSYS_3V3	TP130	3.3V
VCC_12V0	TP39	12.0V
VSYS_5V0	TP26	5.0V
EXP_3V3	TP43	3.3V
VDD_2V5	TP63	2.5V
VDD_1V0	TP59	1.0V
VCC_1V1	TP60	1.1V
VSYS_MCU_5V0	TP117	5.0V
VDD_SD_DV	TP44	3.3V
VSYS_MCUIO_3V3	TP113	3.3V
VSYS_IO_3V3	TP131	3.3V
VSYS_MCUIO_1V8	TP134	1.8V
VSYS_IO_1V8	TP132	1.8V
VDA_MCU_1V8	TP105	1.8V

3.3 EVM Reset/Interrupt Push Buttons

The EVM supports multiple User Push buttons for providing Reset inputs and User Interrupts to the processor.

Table 3-5 lists the Push buttons that are placed on the Top side of the Common Processor Board.

Table 3-5. EVM Push Buttons

Sl No	Push Buttons	Signal	Function
1	SW7	MCU_PORz	MCU domain Power on Reset input
2	SW5	MCU_RESETz	MCU domain Warm Reset input
3	SW4	PORz	Main domain Power on Reset input
4	SW6	RESET_REQz	Main domain Warm Reset input
5	SW10	SOC_EXTINTn	External Interrupt input
6	SW11	SYS_IRQz	System IRQ Interrupt input (also used as SYS_WAKE)
7	SW12	MCAN0_WAKE	CAN Wakeup Input

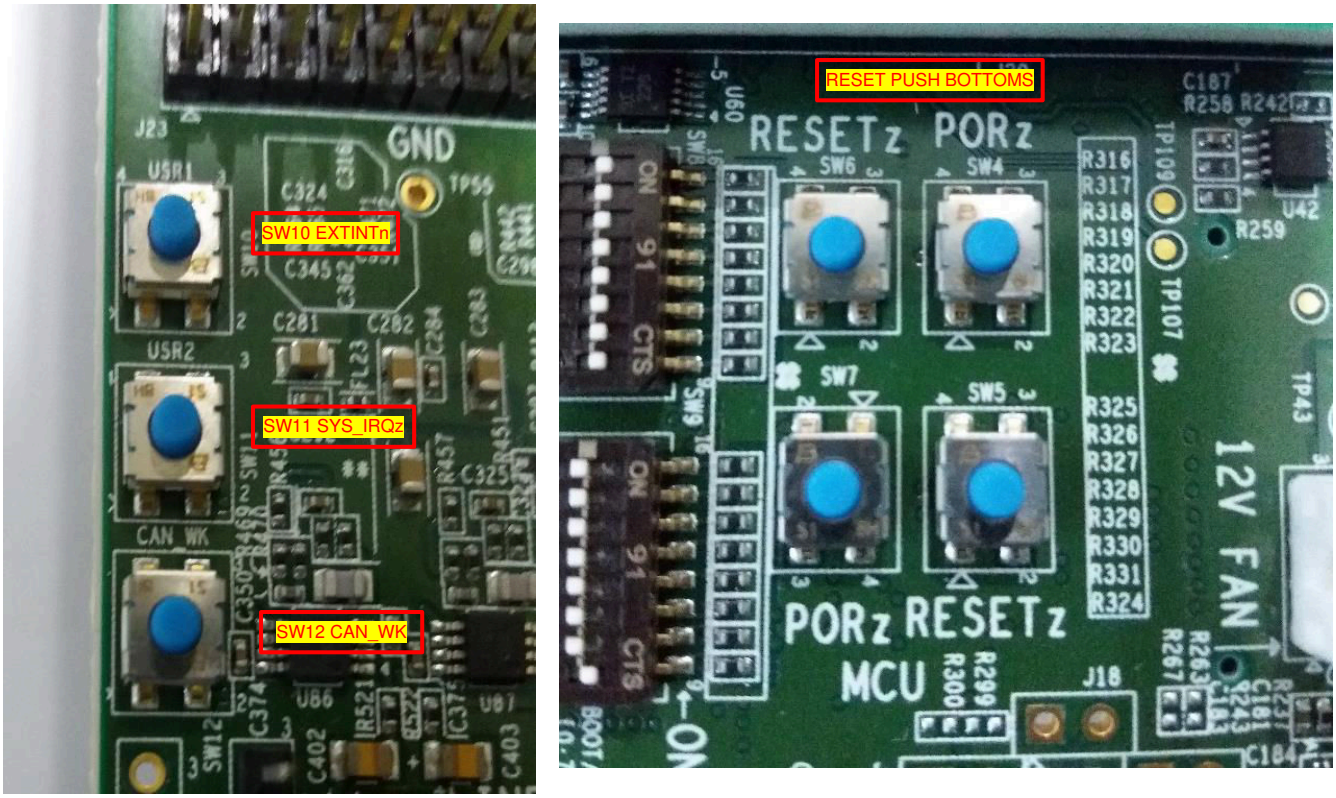


Figure 3-5. EVM Push Buttons

3.4 EVM DIP Switches

J721E EVM supports User DIP Switches for EVM Configuration and SoC Boot mode set function.

3.4.1 EVM Configuration DIP Switch

Figure 3-6 shows that the common processor board has a dedicated EVM configuration switch (SW3) to set the various functions of EVM peripherals. Some of the configuration is for peripherals on the CPB, while others switches are used to configure peripherals on Expansion Boards. For those settings, the device-specific Expansion Board User's Guide will define the switch function.

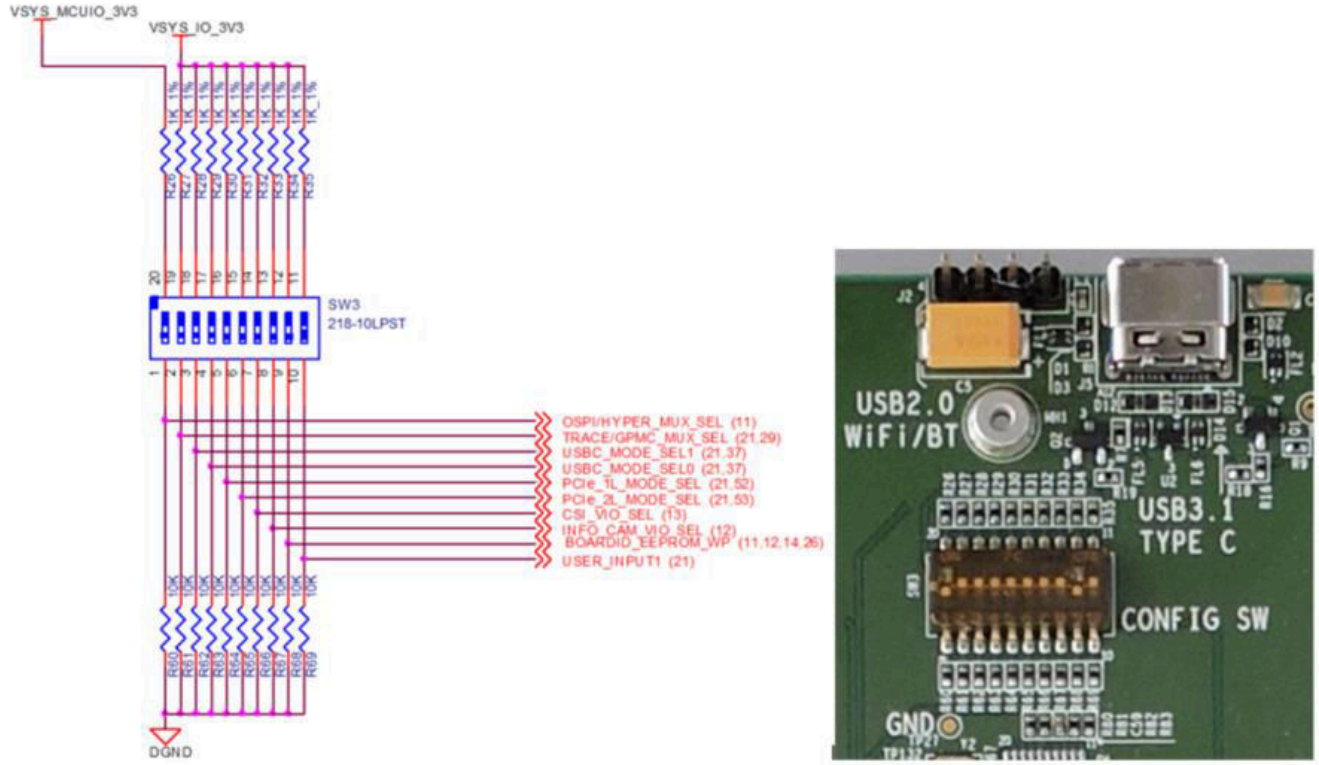


Figure 3-6. EVM Configuration DIP Switch

Table 3-6. EVM Configuration Switch Function

Switch Name	Default Condition	Signal	Operation
SW3.1	OFF	OSPI/HYPER_MUX_SEL	MUX to select between non-volatile memories: ‘0’ (OFF) = OSPI Memory connected to MCU_OSPI0 Interface ‘1’ (ON) = HyperFlash + HyperRAM connected to MCU_OSPI0 Interface
SW3.2	ON	TRACE/GPMC_MUX_SEL	MUX to select Trace interface for debug: ‘0’ (OFF) = Selected signals used for other peripherals (non-debug) ‘1’ (ON) = Debug/Trace connected to MIPI-60 emulation interface
SW3.3	OFF	USBC_MODE_SEL1	Set Mode for USB Type C interface (USB0): '00' (OFF/OFF) = DFP (Downstream Facing Port)
SW3.4	OFF	USBC_MODE_SEL0	‘01’ (OFF/ON) = DRP (Dual Role Port) ‘1X’ (ON, Don’t Care) = UFP (Upstream Facing Port)
SW3.5	OFF	PCIe_1L_MODE_SEL	PCIe 1-Lane Interface Mode Select (supports port PCIe0) ‘0’ (OFF) = Root Complex ‘1’ (ON) = End Point
SW3.6	OFF	PCIe_2L_MODE_SEL	PCIe 2-Lane Mode Select (supports port PCIe1) ‘0’ (OFF) = Root Complex ‘1’ (ON) = End Point
SW3.7	ON	CSI_VIO_SEL	Sets I/O voltage for CSI2 Expansion Interface (LVCMOS signals) ‘0’ (OFF) = 1.8V I/O Voltage ‘1’ (ON) = 3.3V I/O Voltage
SW3.8	ON	INFO_CAM_VIO_SEL	Switch is to be used on Expansion board. See specific expansion board User’s Guide for definition.
SW3.9	ON	BOARDID_EEPROM_WP	Sets EVM’s configuration EEPROM Write Protection ‘0’ (OFF) = Configuration EEPROM can be updated ‘1’ (ON) = Configuration EEPROM cannot be updated/protected
SW3.10	ON	USER_INPUT1	User Define, maps to I/O Expander Input ‘0’ (OFF) = User Defined ‘1’ (ON) = User Defined

3.4.2 SOM Configuration DIP Switch

Table 3-7 shows the J721E SOM configuration switches (SW1-SW3) to set the various functions SOM.

Table 3-7. EVM Configuration Switch Function

Switch Name	Default Condition	Signal	Operation
SW1.1	ON	LPDDR4_IO_SEL	Selects the I/O voltage level for LPDDR4: '0' (OFF) = Selects 0.6 V I/O for LPDDR4X '1' (ON) = Selects 1.1 V I/O for LPDDR4
SW1.2	OFF	SEL_SOC_I2Cn	MUX to select I2C Interface for PMICs: '0' (OFF) = PMIC I2C to SoC WKUP interface '1' (ON) = PMIC I2C to External Header (test mode only)
SW2.1	OFF	SEL_GPIO8_ALT	Selection for PMIC Watchdog Timer/GPIO8: '0' (OFF) = PMIC watchdog timer control is set with SW2.2 '1' (ON) = PMIC I/O used for GPIO8 (test point)
SW2.2	ON	LEOA_WDOG_DIS	Enable/Disable selection for PMIC Watchdog Timer: '0' (OFF) = PMIC watchdog timer is enabled '1' (ON) = PMIC watchdog timer is disabled (note requires SW2.1 to be set to OFF)
SW3.1	ON	SOC_SAFETY_ERRz	Option to combine SOC_SAFETY_ERRz with MCU_SAFETY_ERR and PMIC. '0' (OFF) = SOC_SAFETY_ERRz (Main) is isolated from PMIC. '1' (ON) = SOC_SAFETY_ERRz (Main) is connected to PMIC.
SW3.2	OFF	SOC_PWR_EN	Manual method of enabling PMIC '0' (OFF) = PMIC enabled by EVM system '1' (ON) = PMIC enabled manually (test mode only)

3.4.3 Boot Modes

The boot mode for the processor is determined by a bank of DIP switches (SW8, SW9). All of the boot mode pins have weak pull down resistors and a switch capable of connecting to a strong pull up resister, as shown in Figure 3-7. Note that OFF setting provides a low logic level (‘0’) and an ON setting provides a high logic level (‘1’).

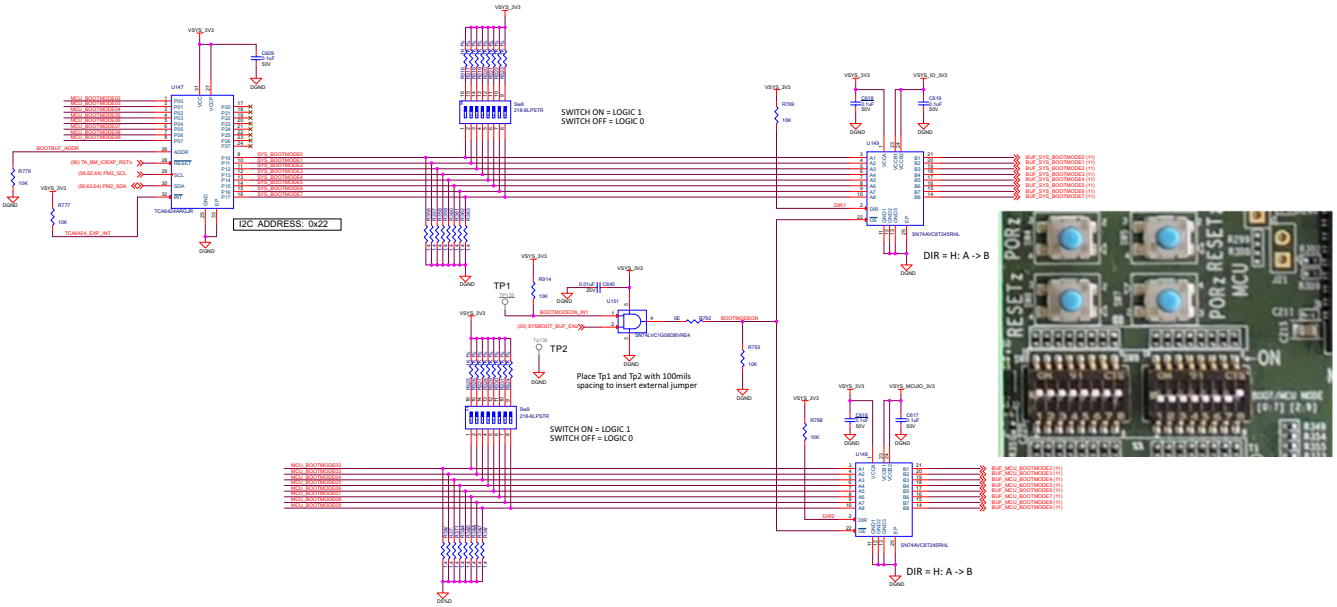


Figure 3-7. BOOT Switches Provided on the Processor Card

Table 3-8 and Table 3-9 provide the switch map to the boot mode functions. For specific settings for each boot interface, see *DRA829/TDA4VM/AM752x Technical Reference Manual*. The selectable boot interfaces supported on the EVM include: Octal-SPI, Quad-SPI, HyperFlash, SD-Card, eMMC, PCIe (as endpoint), CPSW, USB, UFS, UART, and EERPOM.

Table 3-8. Wakup Boot Mode Switch (SW9)

Wakeup Boot Pin Map								
0:1 (Fixed to ‘00’)	2 (SW9.1= OFF)	3 (SW9.2)	4 (SW9.3)	5 (SW9.4)	6 (SW9. 5)	7 (SW9.6)	8 (SW9.7)	9 (SW9.8)
PLL Configuration (Fixed to 19.2 MHz)		Primary Boot Mode A			MCU Only	Rsvd	Rsvd (not for boot use)	

Table 3-9. Main Boot Mode Switch (SW8)

Wakeup Boot Pin Map							
0 (SW8.1)	1 (SW8.2)	2 (SW8.3)	3 (SW8.4)	4 (SW8.5)	5 (SW8.6)	6 (SW8.7)	7 (SW9.8)
Primary Boot Mode B	Backup Boot Mode			Primary Boot Mode Config			Backup Boot Mode Config

3.4.4 Other Selection Switches

The USB2 port of is terminated with USB 3.0 Micro AB connector on the common processor board. The Host and Device function of SoC is set by the ID pin using DIP Switch SW1.

The ID and VBUS supply pin of USB connectors is connected to the DIP switch SW1 to configure the operational modes.

As previously mentioned, the USB2 port, USB3.0 microAB interface is not supported with the J721E SoM.

3.5 EVM UART/COM Port Mapping

Four main domain UART ports of the SoC are interfaced with FT4232H for UART-to-USB functionality and terminated on a micro B connector (J44) provided on the CPB. When the EVM is connected to a Host using the provided USB cable, the computer can establish a Virtual Com Port that can be used with any terminal emulation application. The FT4232H is bus powered. Virtual Com Port drivers for the FT4232H can be obtained from https://www.ftdichip.com/Products/ICs/FT4232H.htm.

Out of four UART ports, one UART port (UART0) supports RS232 with Hardware flow control.

MCU and WKUP UART ports of the SoC are interfaced with FT2232H for UART-to-USB functionality and terminated on a micro B connector (J43) provided on the CPB. When the EVM is connected to a Host using the provided USB cable, the computer can establish a Virtual Com Port that can be used with any terminal emulation application. The FT2232H is bus powered. Virtual Com Port drivers for the FT4232H can be obtained from https://www.ftdichip.com/Products/ICs/FT2232H.html.

RS232 hardware control feature is supported on MCU UART0.

Both FT2232H and FT4232H circuits powered through USB VBUS. Since the circuits are powered through BUS power, the connection to the COM port will not be lost when the EVM power is removed. The maximum length for the IO cables are required to be less than 3 meters.

Table 3-10. UART Port Mapping

UART Port	FTDI Bridge	USB Connector	COM Port	Remarks
MAIN_UART0	FT4232H	J44	COM 1	Supports Hardware Flow control
MAIN_UART1			COM 2	
MAIN_UART2			COM 3	
MAIN_UART4			COM 4	
MCU_UART0	FT2232H	J43	COM 5	Supports Hardware Flow control
WKUP_UART0			COM 6	

The EEPROM of FTDI bridges are programmed with the CPB serial number, users to identify the connected COM port with board serial number when one or more boards connected to the computer.

Example Programming content:

- FT4232H (Main)
  - CPB Serial number: 14197900028
- Programmed Serial number on FT4232H EEPROM: 141979000280A
  - FT2232H (MCU and WKUP)
- CPB Serial number: 14197900028
  - Programmed Serial number on FT4232H EEPROM: 141979000280B

3.6 JTAG Emulation

The Common processor board includes XDS110 class on board emulation through the micro B connector J3. It also has an option to support external emulation through MIPI 60 pin header (J16). When an external emulator is connected, XDS110 emulation circuitry path will be disconnected automatically.

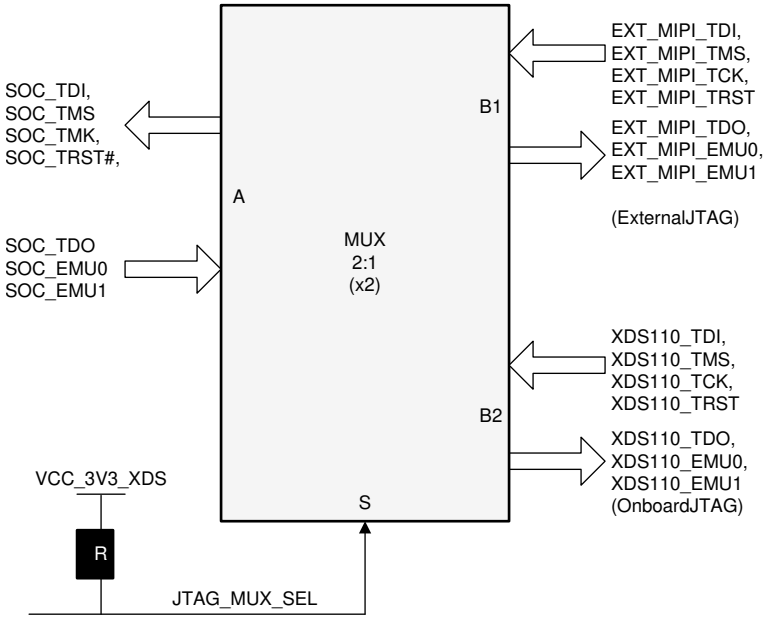


Figure 3-8. JTAG Mux

Table 3-11. JTAG 1:2 Mux selection

Condition	MUX_SEL	Function
XDS110 Powered via USB	HIGH	A<->B2 port [On Board EMU]
External Emulator attached	LOW	A<->B1 port [EXTERNAL EMU]

As mentioned, the design includes a MIPI 60pin (J16) connector with connections for both JTAG and Trace capabilities. The trace pins are multiplexed with other functions (McASP10, McASP11 and GPMC0) and uses an on-board mux to select the different functions. The mux is defaulted to the MIPI 60pin connector. The 1:3 mux is controlled by bits of the I2C GPIO expander2 (I2C add: 0x22; I2C Inst:I2C0) on the common processor board. There is an option to set the state using the DIP switch SW3 Position 2, which allows GPMC to expansion interface to be selected by default (for boot support).

Table 3-12. TI 60 pin Connector (J16) Pinout

Pin No.	Signal	Pin No.	Signal
1	VSYS_IO_3V3	31	TRC_DATA6
2	MIPI_TMS	32	NC
3	MIPI_TCK	33	TRC_DATA7
4	MIPI_TDO	34	NC
5	MIPI_TDI	35	TRC_DATA8
6	MIPI_TGTRST#	36	NC
7	MIPI_RTCK	37	TRC_DATA9
8	MIPI_TRST_PD (EXT_MIPI_TRST#)	38	EXT_MIPI_EMU0
9	MIPI_nTRSTPU	39	TRC_DATA10
10	NC	40	EXT_MIPI_EMU1
11	NC	41	TRC_DATA11
12	VSYS_IO_3V3	42	NC
13	TRC_CLK	43	TRC_DATA12
14	NC	44	NC
15	DGND	45	TRC_DATA13
16	DGND	46	NC
17	TRC_CTL	47	TRC_DATA14
18	TRC_DATA19	48	NC
19	TRC_DATA0	49	TRC_DATA15
20	TRC_DATA20	50	NC
21	TRC_DATA1	51	TRC_DATA16
22	TRC_DATA21	52	NC
23	TRC_DATA2	53	TRC_DATA17
24	NC	54	NC
25	TRC_DATA3	55	TRC_DATA18
26	NC	56	NC
27	TRC_DATA4	57	DGND
28	NC	58	JTAG_MUX_SEL
29	TRC_DATA5	59	NC
30	NC	60	NC

The EVM Common processor board Kit includes two JTAG converters, one is to convert MIPI 60 pin to TI14 pin JTAG emulator and the other one is to convert MIPI 60 pin to CTI20 pin JTAG.

Table 3-13 shows pinouts of the TI14 pin and the CTI 20 pin JTAG converters.

Table 3-13. cTI20 Pin Connector (J1-Refer PROC081E2 SCH) Pinout

Pin No.	Signal	Pin No.	Signal
1	MIPI_20_TMS	11	MIPI_20_TCK
2	MIPI_20_TRST	12	DGND
3	MIPI_20_TDI	13	MIPI_20_EMU0
4	MIPI_20_TDIS	14	MIPI_20_EMU1
5	MIPI_20_VTREF	15	SYSRST#
6	NC (key)	16	DGND
7	MIPI_20_TDO	17	NC
8	20PJTAG_DET	18	NC
9	MIPI_20_RTCK	19	NC
10	DGND	20	DGND

Table 3-14. TI14 Pin Connector (J2-Refer PROC081E2 SCH) Pinout

Pin No.	Signal	Pin No.	Signal
1	MIPI_14_TMS	8	14PJTAG_DET
2	MIPI_14_TRST	9	MIPI_14_RTCK
3	MIPI_14_TDI	10	DGND
4	MIPI_14_TDIS	11	MIPI_14_TCK
5	MIPI_14_VTREF	12	DGND
6	NC (key)	13	MIPI_14_EMU0
7	MIPI_14_TDO	14	MIPI_14_EMU1

4 J721E EVM Hardware Architecture

This section explains the Hardware Architecture of J721E EVM in detail.

4.1 J721E EVM Hardware Top level Diagram

Figure 4-1 shows the functional block diagram of the J721E EVM.

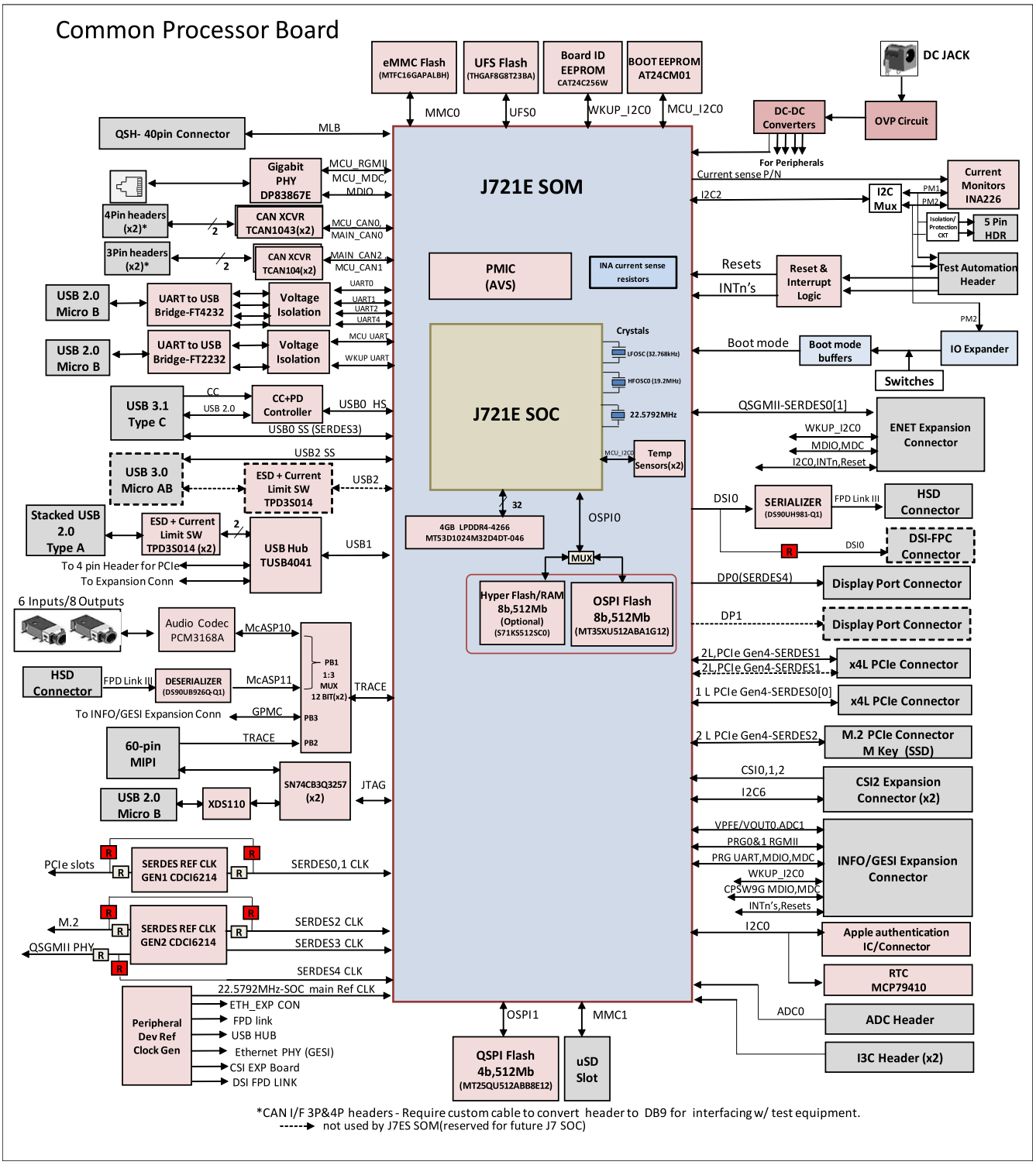


Figure 4-1. J721E EVM Functional Block Diagram

Figure 4-2 shows the Quad Port Ethernet Expansion Board functional block diagram.

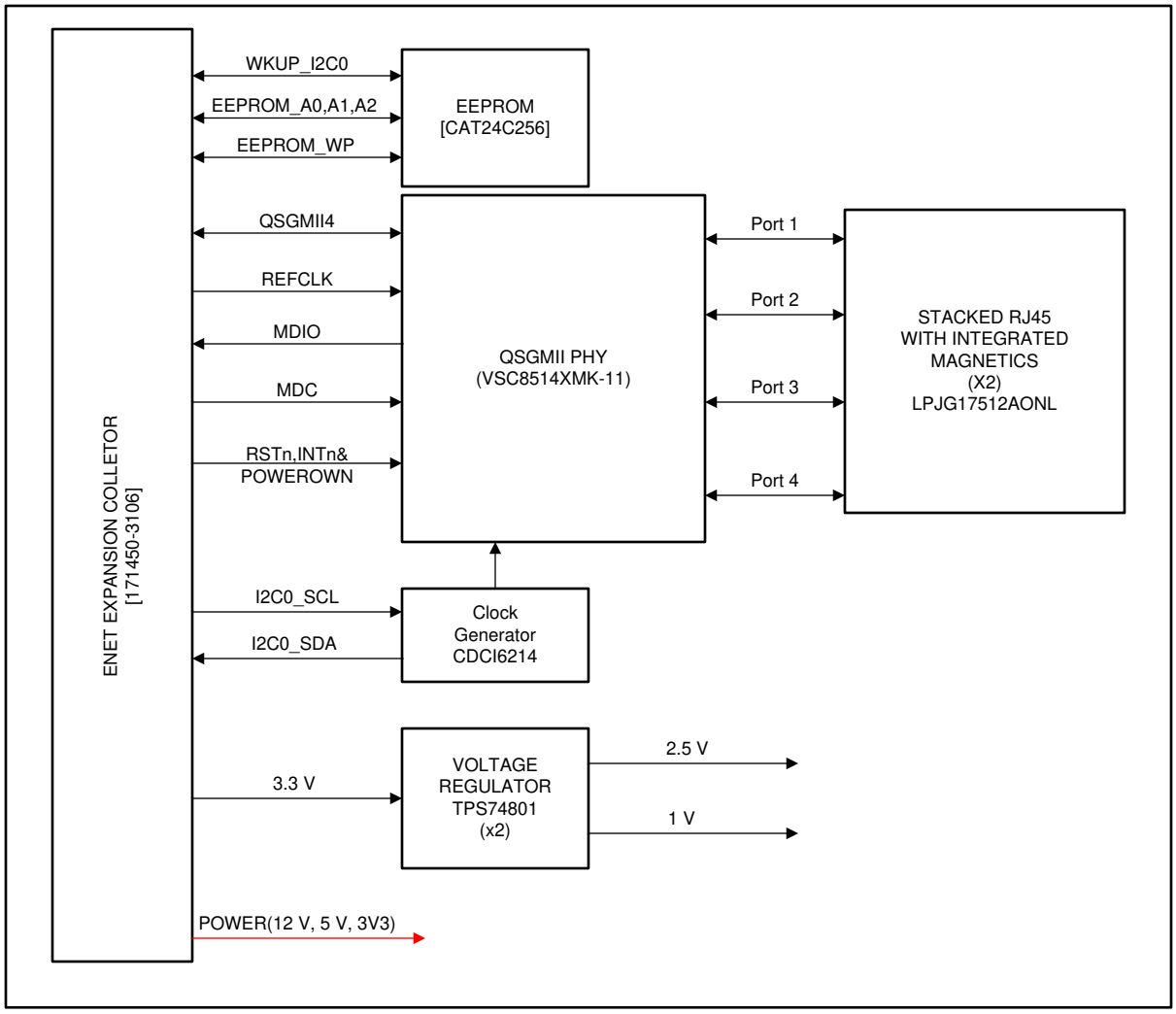


Figure 4-2. Quad Port Ethernet Expansion Functional Block diagram

4.2 J721E EVM Interface Mapping

Table 4-1 shows the J721E EVM Interface Mapping table.

Table 4-1. J721E EVM Interface Mapping

Interface Name	Port on SoC	Device Part Number
Memory – LPDDR4	DDR0	MT53D1024M32D4DT
Memory – OSPI	MCU_OSPI0	MT35XU512ABA1G12-0SIT (Channel B of 1:2 Mux TS3DDR3812RUAR)
Memory – Hyper Flash	MCU_OSPI0	S71KS512SC0BHV000 (Channel C of 1:2 Mux TS3DDR3812RUAR)
Memory – Quad SPI	MCU_OSPI1	MT25QU512ABB8E12-0SIT
Memory – eMMC	MMC0	MTFC16GAPALBH-AAT ES
Memory – Micro SD Socket	MMC1	DM3BT-DSF-PEJS
Memory – UFS	UFS0	THGAF8G8T23BAIL
Memory – Board ID EEPROM	WKUP_I2C0 (I2C6 for CSI Expansion)	CAT24C256WI-GT3 (CAV24C256WE-GT3 for J721E SOM)
Memory – Boot EEPROM	MCU_I2C0	AT24CM01
Ethernet – RGMII	MCU_RGMII1	DP83867ERGZT
Ethernet – Quad SGMII	SERDES0 (SGMII2)	VSC8514XMK
USB – 3.1 Type C + PD + CC Controller	SERDES3 (USB0)	2012670005 + PTPS25830QWRHBTQ1 + TUSB321RWBR
USB – 2.0 (HUB)	USB1	TUSB4041IPAPR
Display Port	SERDES4 (DP0)	472720001
FPD Link Panel Serializer	DSI0	PDS90UB941ASRTDTQ1
FPD Link Radio Tuner	McASP11	DS90UB926QSQE
Audio Codec	McASP10	PCM3168APAP
PCIe – x4 Lane Socket (x1 Lane)	SERDES0 (PCIe0)	10142333-10111MLF
PCI2 – x4 Lane Socket (x2 Lane)	SERDES1 (PCIe1)	10142333-10111MLF
PCIe – M.2 Socket (M-Key 2280)	SERDES2 (PCIe2)	MDT320M01001
MLB/MLBP expansion	MLB0	QSH-020-01-L-D-DP-A-K
UART Terminal (UART-to-USB)	UART [0:2] & 4	FT4232HL
UART Terminal (UART-to-USB)	WKUP_UART0 & MCU_UART0	FT2232HL
CAN (4x)	MCU_MCAN0	TCAN1043-Q1 (W/ Wake function)
	MCU_MCAN1	TCAN1042HGVD
	MCAN0	TCAN1043-Q1 (W/ Wake function)
	MCAN2	TCAN1042HGVD
ADC Header	MCU_ADC0	TSW-110-07-S-D

4.3 I2C Address Mapping

Table 4-2 shows the complete I2C address mapping details on the EVM.

Table 4-2. J721E EVM I2C Table

J721E EVM I2C Table				
Board	**I2C Port**	**Device/Function**	**Part#**	**I2C Address**
EVM/SoM	WKUP_I2C0	PMIC	O917A131TRGZTQ1	0x58-5B
EVM/SoM	WKUP_I2C0	PMIC	LP873200RHDTQ1	0x62
EVM/SoM	WKUP_I2C0	PMIC	LP87524BRNFTQ1	0x60
EVM/SoM	WKUP_I2C0	PMIC	LP87561IRNFTQ1	0x61
EVM/SoM	WKUP_I2C0	Board ID EEPROM	CAT24C256W	0x50
EVM/CPB	WKUP_I2C0	Board ID EEPROM	CAT24C256W	0x53
EXP/QSGMII	WKUP_I2C0	Board ID EEPROM	CAT24C256W	0x54
EVM/CPB	MCU_I2C0	BOOT EEPROM	AT24CM01	0x50,51
EVM/SoM	MCU_I2C0	Temperature Sensors 1	TMP100NA/3K	0x48
EVM/SoM	MCU_I2C0	Temperature Sensors 2	TMP100NA/3K	0x49
EVM/CPB	SoC_I2C0	Peripheral Clock Generator	CDCEL937-Q1	0x6D
EVM/CPB	SoC_I2C0	RTC Module	MCP79410	0x57,6F
EVM/CPB	SoC_I2C0	Apple Authentication Header/Footprint	2214BR-10G	0x10, 0x11
EVM/CPB	SoC_I2C0	SERDES REF CLK GEN - 2	CDCI6214	0x76
EVM/CPB	SoC_I2C0	16 bit I2C GPIO Expander-1	TCA6416ARTWR	0x20
EVM/CPB	SoC_I2C0	24 bit I2C GPIO Expander-2	TCA6424ARGJR	0x21
EVM/CPB	SoC_I2C0	I2C MUX for both x2LANE and x1LANE PCIe Interface	TCA9543APWR	0x70
EVM/CPB	SoC_I2C0	I2C MUX for M.2 PCIe Connector (2 L PCIe Gen4-SERDES2)	TCA9543APWR	0x71
EVM/CPB	SoC_I2C0	MLB Physical Interface Board	<connector interface>	
EXP/QSGMII	SoC_I2C0	Clock Generator on Quad ENET Board	CDCI6214	TBD
EVM/CPB	SoC_I2C1	8 bit I2C GPIO Expander-4	TCA6408ARGTR	0x20
EVM/CPB	SoC_I2C1	FPD Link-IV Serializer (DSI)	DS90UH981-Q1	0x0E
EVM/CPB	SoC_I2C1	DSI FPC	CONNECTOR INTERFACE	TBD
EVM/CPB	SoC_I2C2	Current Monitors 1(PM1_I2C)	INA226	0x40-0x4F
EVM/CPB	SoC_I2C2	Current Monitors 2(PM2_I2C)	INA226	0x40-0x4F
EVM/CPB	SoC_I2C2	Test Automation Header	<connector interface>	
EVM/CPB	SoC_I2C3	8 bit I2C GPIO Expander-3	TCA6408ARGTR	0x20
EVM/CPB	SoC_I2C3	Audio Codec - 1	PCM3168A-Q1	0x44
EVM/CPB	SoC_I2C3	FPD Link-III De-serializer (McASP)	DS90UB926Q-Q1	0x2C
EVM/CPB	SoC_I2C6	8 bit I2C GPIO Expander-5	TCA6408ARGTR	0x20

4.4 GPIO Mapping

The general purpose I/Os (GPIOs) of the SoC have two major groups: WKUP/MCU and MAIN. Table 4-3 describes the detailed GPIO mapping of SoC with EVM peripherals.

Table 4-3. J721E SoC - GPIO Mapping Table

J721E SoC - GPIO Mapping Table						
Package Signal Name	**GPIO**	**Net name**	**In/Out**	**Default**	**State**	**Remarks**
WKUP/MCU Domain						
WKUP_GPIO0_0	WKUP_GPIO0_0	MCU_MCAN0_EN	Output	BOOTMODE	Active High	MCU CAN0 Enable
WKUP_GPIO0_1	WKUP_GPIO0_1	BOOT_EEPROM_WP	Output	BOOTMODE	Active High	Boot EEPROM Write protect
WKUP_GPIO0_2	WKUP_GPIO0_2	MCU_CAN1_STB	Output	BOOTMODE	Active High	MCU CAN1 Standby
WKUP_GPIO0_3	WKUP_GPIO0_3	GPIO_MCU_RGMII1_RST#	Output	PU	Active low	MCU_RGMII1_Reset
WKUP_GPIO0_6	WKUP_GPIO0_6	WKUP_GPIO0_6	I/O	Test Point	NA	Terminated with Test point
WKUP_GPIO0_7	WKUP_GPIO0_7	SYS_IRQz	Input	PU	Active low	Push-button Interrupt, User Defined/Wake S2R ('0>1' - interrupt pending, '1' - normal operation)
WKUP_GPIO0_8	WKUP_GPIO0_8	OSPI/HYPER_MUX_SEL	Output	DIP_SEL	NA	Flash Memory Selection ('0' - OSPI0, '1' - Hyperflash + HyperRam)
WKUP_GPIO0_9	WKUP_GPIO0_9	PMIC_MCU_INT#	Input	PU	Active low	Interrupt from PMIC
WKUP_GPIO0_17	WKUP_GPIO0_17	MCU_OSPI0_ECC_FAIL	Output	NA	Active High	OSPI_ECC_FAIL (Mux option w/ HYPERBUS_CKn), MCU_OSPI0_ECC_FAIL is DNI resistor option.
MCU_SPI0_CLK	WKUP_GPIO0_52	WKUP_GPIO0_52	I/O	BOOTMODE	NA	Terminated with Test point
MCU_SPI0_CS0	WKUP_GPIO0_55	MCU_RGMII1_INT#	Input	PU	Active Low	MCU Ethernet Interrupt ('0' - interrupt pending, '1' - no interrupt)
MCU_SPI0_D0	WKUP_GPIO0_53	SYS_MCU_PWRDN	Output	PD	Active low	System Power Down ('0' - normal operation, '1' -system power down)
MCU_SPI0_D1	WKUP_GPIO0_54	MCU_CAN0_STBz	Output	PD	Active low	MCU CAN0 Standby
Main Domain						
EXTINTN	GPIO0_0	SOC_EXTINTN	Input	PU	Active low	Push-button Interrupt, User Defined
RGMII6_RX_CTL	GPIO0_98	C_MCASP10_AFSR	NA	PU	Active low	I2C0 I/O expander interrupt. ('0' - interrupt pending, '1' - no interrupt)(I2C0_IOEXP_INT#) Note: GPIO only available from Trace/GPMC Mux
RGMII6_RD3	GPIO0_105	IMU_GPIO0	I/O	NA	NA	Used as GPIO0 for IMU Sensor
SPI1_CS1	GPIO0_117	DSI_UB981_INTB	Input	PU	Active low	DSI FPD Link Serializer/Panel Interrupt. Note: resistor option with CON_DSI0_INT#
UART1_CTSN	GPIO0_127	GPIO0_127/EQEP0_S/MLB0_MLBCLK	Output	PU	Active High	CP Board - MCAN2_STB; GESI - Boosterpack_GPIO2
UART1_RTSN	GPIO1_0	GPIO1_0/EQEP0_I/MLB0_MLBDAT	Output	PD	NA	CP Board - PM I2C Mux seletion. ('0' - SOC_I2C2_SCL/SDA → PM1_SCL/SDA, '1' - SOC_I2C2_SCL/SDA → PM2_SCL/SDA) GESI - Boosterpack_GPIO1
MCAN1_RX	GPIO1_3	USBC_DIR	Input	PU	NA	USB Type C Cable Orientation. Type-C plug position 2 (H); Type-C plug position 1 (L)
ECAP0_IN_APWM_OUT	GPIO1_11	GPIO1_11/MAIN_I3C0_SDAPULLEN	Input	PU	Active High	Display I/O expander Interrupt. ('0' - interrupt pending, '1' - no interrupt) (IOEXP4_INT#)
EXT_REFCLK1	GPIO1_12	GPIO1_12/MLB0_REFCLK	Input	PD	NA	CP Board Audio De-serializer UB926_GPIO1 (Tuner Unused GPIO)
MMC1_SDWP	GPIO1_22	ENET_EXP_INTB	Input	PU	Active low	Ethernet Expansion Interrupt. ('0' - interrupt pending, '1' - no interrupt)
I3C0_SCL	GPIO1_5	H_I3C0_SCL	I/O	NA	NA	CP Board Audio De-serializer UB926_GPIO2
I3C0_SDA	GPIO1_6	H_I3C0_SDA	I/O	NA	NA	CP Board Audio De-serializer UB926_GPIO3

4.5 Power Supply

Figure 4-3 shows the SoM's power distribution system. The Power to the SoM is derived from the Dual Buck converter 12 V to 5.0 V / 3.3 V on the Common Processor Board. The J721E processor is powered from a dual TPS6594x PMIC solution, which is optimized for the J721E to support a wide variety of use cases.

Dual load switch TPS22976-Q1 provides the switching option for the LPDDR4 I/O power supply (1.1 V / 0.6 V).

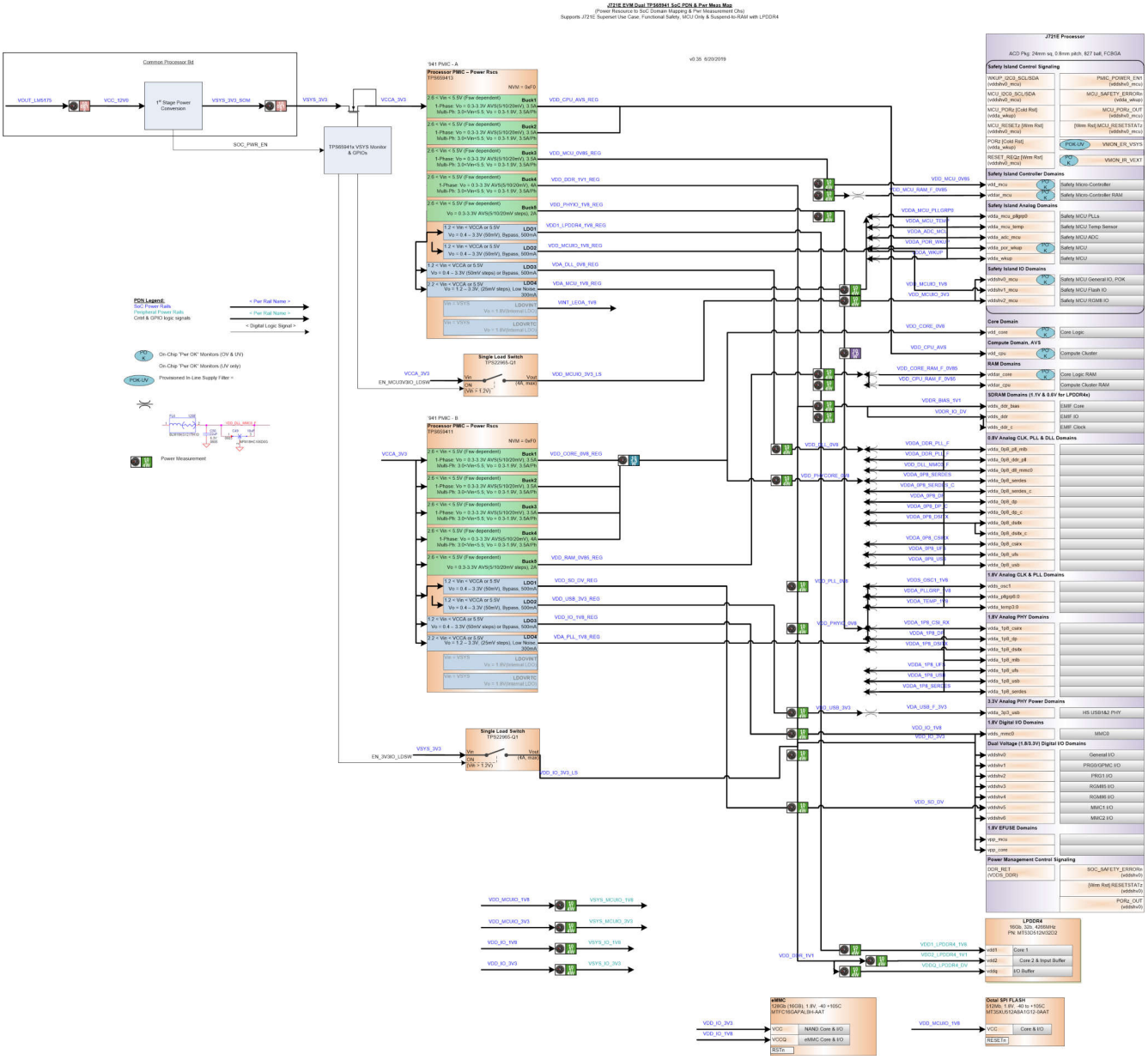


Figure 4-3. J721E SOM Power Distribution Block Diagram

4.5.1 Power Sequencing

Figure 4-4 shows the power up sequence of the all Power supplies present on the processor card. Note processor specific power supplies are provided from the Dual PMICs, and its specific power sequence is to support the processor sequence requirements. This sequence is documented in the device-specific processor's data manual. Figure 4-4 illustrates the support of all the other system supplies.

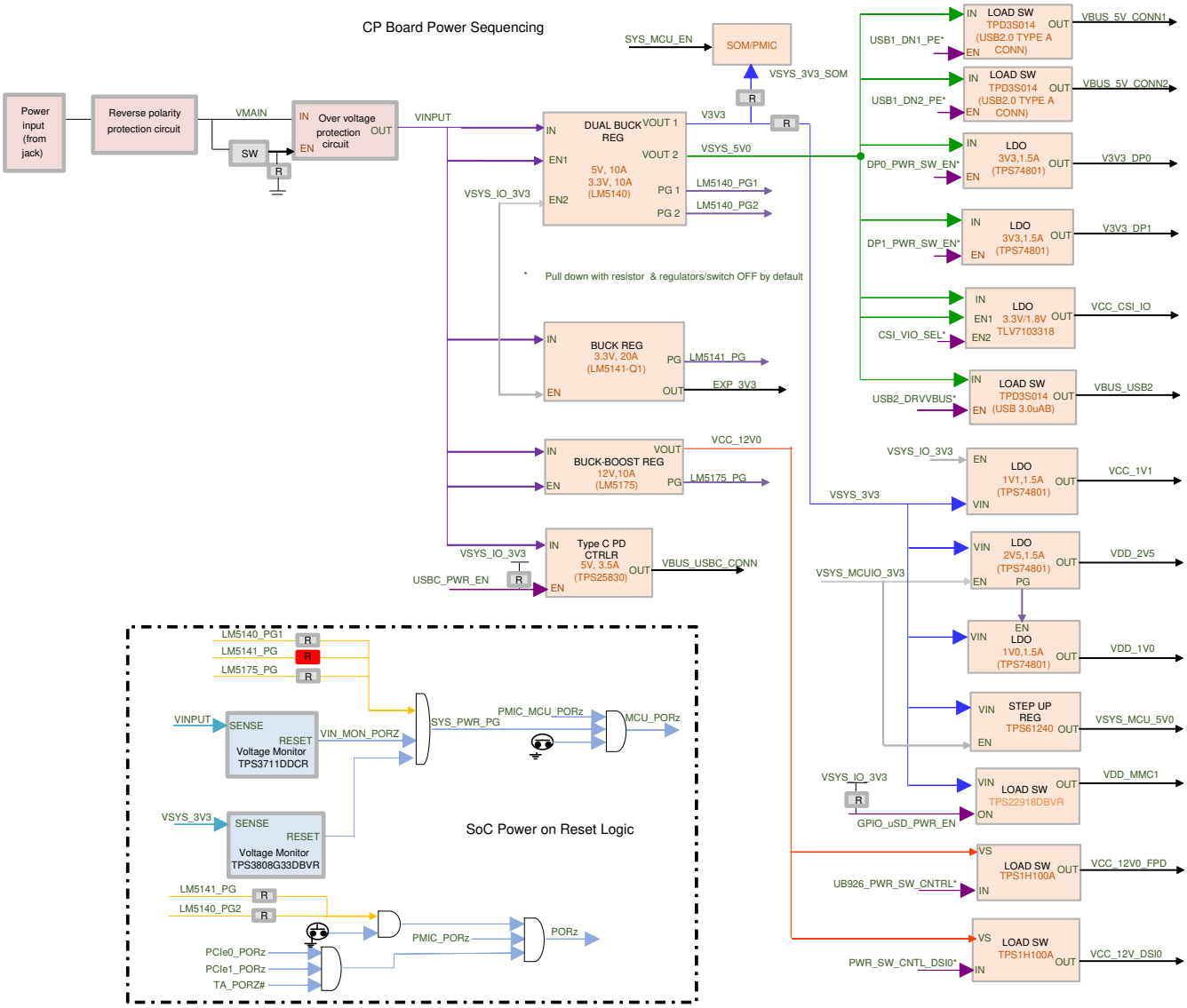


Figure 4-4. Power ON Sequencing

4.5.2 Voltage Supervisor

The power rails are monitored to control the Power ON Reset (MCU_PORz) for SoC. Two supervisor devices are provided to monitor Main power input and VSYS_3V3.

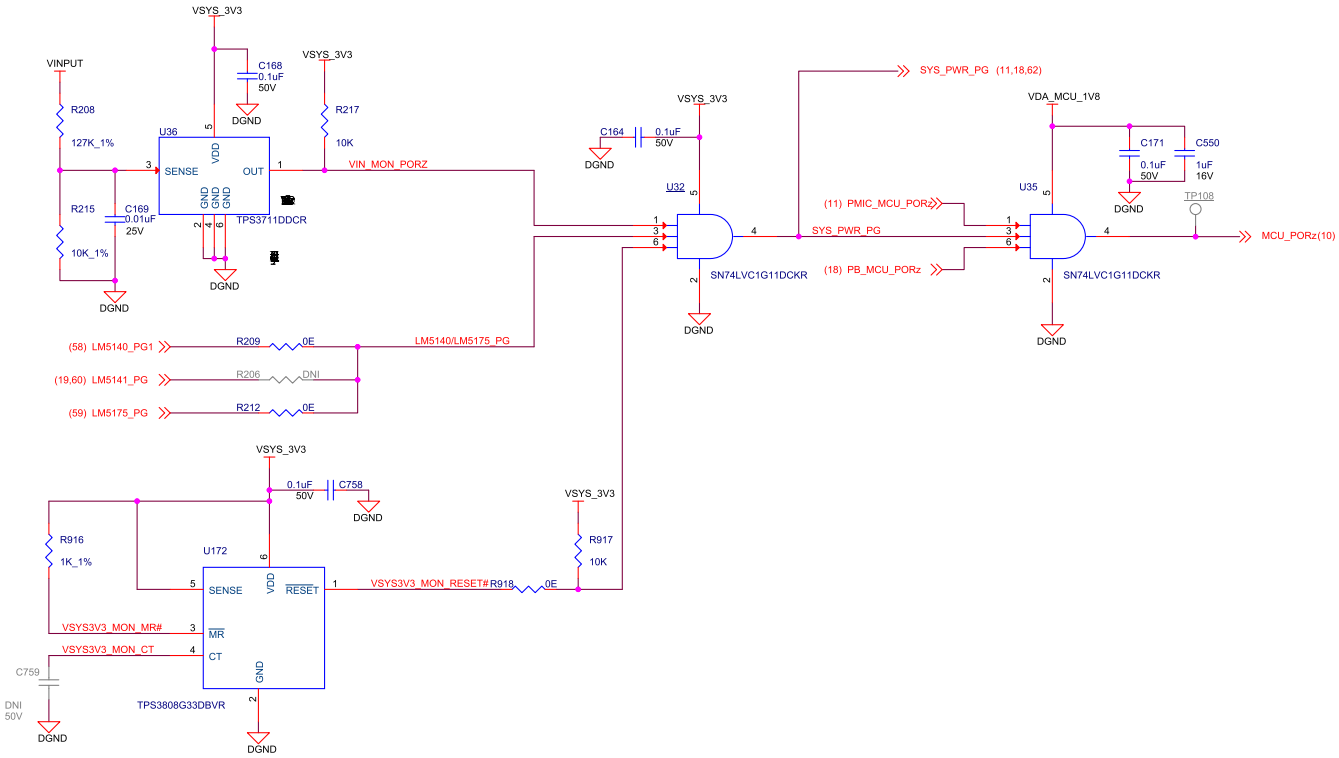


Figure 4-5. Voltage Supervisor Circuit

4.5.3 DDR I/O Voltage Selection

There is a DIP switch provided on the J721E SoM to select the SoC's DDR and LPDDR4 memory I/O supply for the LPDDR4/LPDDR4x.

Currently, the J721E device does not support LPDDR4x. This support may be added at a later date. The EVM does support this feature if/when support is added to the silicon.

The DIP switch SW1 Bit 1 provides an option to change the logic of D Flip-Flop (U7) that controls the Load Switches TPS22965TDSGRQ1 and TPS22976NDPUT to decide the I/O supply voltages.

Table 4-4. DDR I/O Voltage Selection

SW1 Bit 1	SDRAM_TYPE	Selected DDR I/O Voltage
LOW	LPDDR4X	0.6V
HIGH	LPDDR4	1.1V

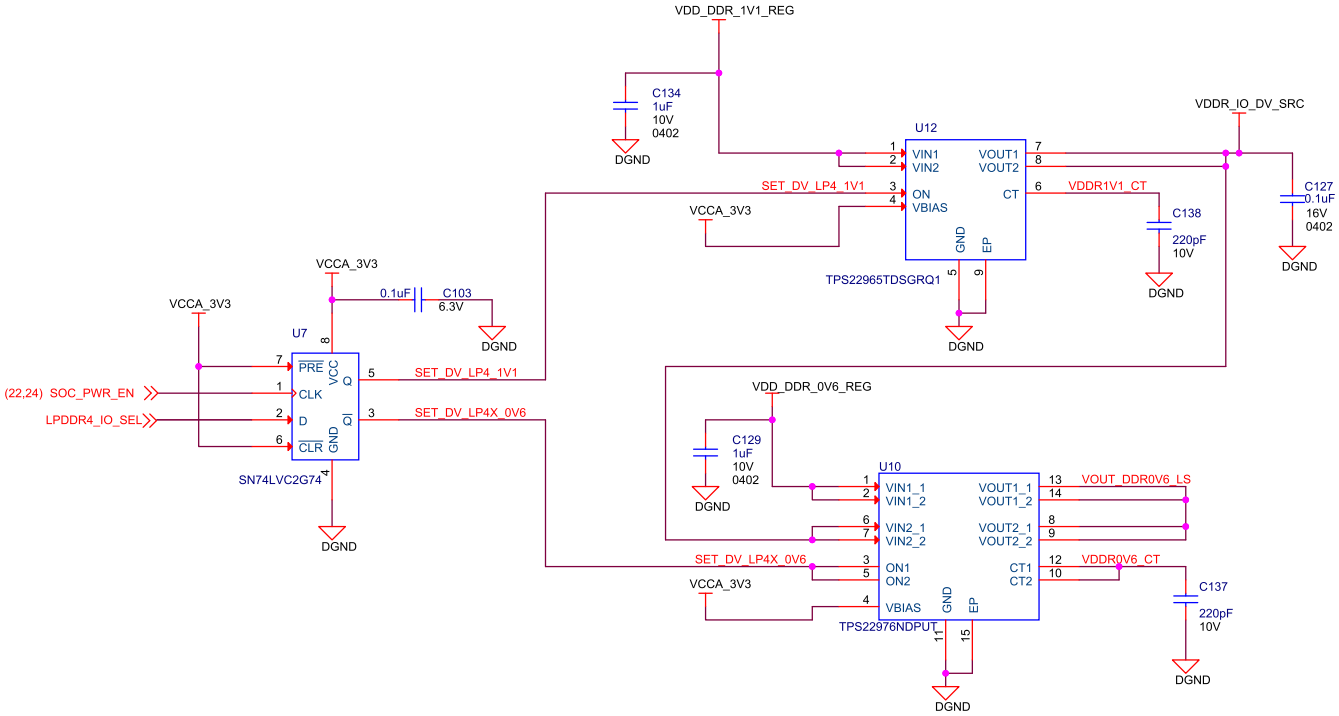


Figure 4-6. LPDDR4 IO Voltage Selection Circuit

4.5.3.1 J721E SoC S2R Logic Flow Diagram

The EVM supports a low power state referred to as Suspend-to-RAM (or S2R). This state allows the processor (or optionally the entire system) to be powered off while the LPDDR4 memory is maintained in self refresh mode. The power state is managed through the PMIC(s). Table 4-5 shows the steps required to enter the S2R state:

Table 4-5. J721E SoC S2R Logic Flow

Leo PMIC Transition From Active Mode to S2R Mode				
Action	**Address**	**Bits**	**Data**	**Register/Bit Names**
Unmask GPIO10_RISE-MASK on LeoA (I2CID: 0x48)	0x51	[4]	0x0	GPIO10_RISE_MASK
Read and write to clear the WKUP1 interrupt	0x63	[1]	0x1	GPIO10_INT
Reconfigure GPIO4 of LeoA to LP_WKUP1	0x34	[7:0]	0xC8	GPIO4_CONFIG
Read and write to clear the LP_WKUP1 interrupt	0x64	[4]	0x1	GPIO_INT
Set nSLEEP2b and nSLEEP1b to '00' to go to S2R state	0x86	[1:0]	0x0	NSLEEP2b, NSLEEP1b
Read and write to clear the ENABLE_INT interrupt	0x65	[1]	0x1	ENABLE_INT

The EVM can be woke from the low power state by pressing the CAN_WAKEn button (SW12).

4.5.3.2 J721E SoC MCU Only Operation

Table 4-6. J721E SoC S2R Logic Flow

Leo PMIC Transition From Active Mode to S2R Mode				
Action	**Address**	**Bits**	**Data**	**Register/Bit Names**
Unmask GPIO10_RISE-MASK on LeoA (I2CID: 0x48)	0x51	[4]	0x0	GPIO10_RISE_MASK
Read and write to clear the WKUP1 interrupt	0x63	[1]	0x1	GPIO10_INT
Reconfigure GPIO4 of LeoA to LP_WKUP1	0x34	[7:0]	0xC8	GPIO4_CONFIG
Read and write to clear the LP_WKUP1 interrupt	0x64	[4]	0x1	GPIO_INT
Set nSLEEP2b and nSLEEP1b to '10' to go to MCU_ONLY state	0x86	[1:0]	0x2	NSLEEP2b, NSLEEP1b
Read and write to clear the ENABLE_INT interrupt	0x65	[1]	0x1	ENABLE_INT

The EVM can be woke from the low power state by the MCU issuing commands to the PMIC through I2C.

4.5.3.3 Power Monitoring

INA226 power monitor devices are used to monitor current and voltage of various power rails of J721E processor. The device reports current, voltage and power to J721E processor through I2C interface. Four Terminal High Precision shunt resistors are provided, and the values are calculated based on load current.

Table 4-7. INA Devices I2C Slave Address

Power Source	Supply Net	I2C Bus	Slave Address (IN HEX)	Value of the Shunt Connected to the Supply Rail
VDD_MCU_0V85_REG	VDD_MCU_0V85	SOC_I2C2/PM1	0x40	0.01E
VDD_MCU_RAM_0V85_REG	VDD_MCU_RAM_0V85	SOC_I2C2/PM1	0x41	0.01E
VDA_MCU_1V8_REG	VDA_MCU_1V8	SOC_I2C2/PM1	0x42	0.01E
VDD_MCUIO_3V3_LS	VDD_MCUIO_3V3	SOC_I2C2/PM1	0x43	0.01E
VDD_MCUIO_1V8_REG	VDD_MCUIO_1V8	SOC_I2C2/PM1	0x44	0.01E
VDD_CORE_0V8_REG	VDD_CORE_0V8	SOC_I2C2/PM1	0x45	0.01E
VDD_CORE_RAM_0V85_REG	VDD_CORE_RAM_0V85	SOC_I2C2/PM1	0x46	0.01E
VDD_CPU_RAM_0V85_REG	VDD_CPU_RAM_0V85	SOC_I2C2/PM1	0x47	0.01E
VDD_CPU_AVS_REG	VDD_CPU_AVS	SOC_I2C2/PM1	0x48	0.01E
V917_SMPS3_1V1	VDDR_BIAS_1V1	SOC_I2C2/PM1	0x49	0.01E
VDDR_IO_DV_SRC	VDDR_IO_DV	SOC_I2C2/PM1	0x4A	0.01E
VDD_CORE_0V8_REG	VDD_PHYCORE_0V8	SOC_I2C2/PM1	0x4B	0.01E
VDA_PLL_1V8_REG	VDA_PLL_1V8	SOC_I2C2/PM1	0x4C	0.01E
VDD_PHYIO_1V8_REG	VDD_PHYIO_1V8	SOC_I2C2/PM1	0x4D	0.01E
VDA_USB_3V3_REG	VDA_USB_3V3	SOC_I2C2/PM1	0x4E	0.01E
SPARE	NA	SOC_I2C2/PM1	0x4F	NA
VDD_MCUIO_1V8_REG	VDD_IO_1V8	SOC_I2C2/PM2	0x40	0.01E
VSYS_3V3	VDD_IO_3V3	SOC_I2C2/PM2	0x41	0.01E
VDD_SD_DV_REG	VDD_SD_DV	SOC_I2C2/PM2	0x42	0.01E
V917_LDO4_1V8	VDD1	SOC_I2C2/PM2	0x43	0.01E
V917_SMPS3_1V1	VDD2	SOC_I2C2/PM2	0x44	0.01E
VDDR_IO_DV_SRC	VDDQ_LPDDR4_DV	SOC_I2C2/PM2	0x45	0.01E
VDD_MCUIO_1V8_REG	VSYS_MCUIO_1V8	SOC_I2C2/PM2	0x46	0.01E
VSYS_3V3	VSYS_MCUIO_3V3	SOC_I2C2/PM2	0x47	0.01E
VDD_MCUIO_1V8_REG	VSYS_IO_1V8	SOC_I2C2/PM2	0x48	0.01E
VSYS_3V3	VSYS_IO_3V3	SOC_I2C2/PM2	0x49	0.01E
VCC_12V0	VCC_12V0	SOC_I2C2/PM2	0x4A	0.01E
VSYS_5V0	VSYS_5V0	SOC_I2C2/PM2	0x4B	0.01E
VSYS_3V3	VSYS_3V3	SOC_I2C2/PM2	0x4C	0.01E
VSYS_3V3	VSYS_3V3_SOM	SOC_I2C2/PM2	0x4D	0.01E
VDD_EXTLDO1_0V8	VDDA_DLL_0V8	SOC_I2C2/PM2	0x4E	0.01E
EXP_3V3	EXP_3V3	SOC_I2C2/PM2	0x4F	0.01E

INA devices can be accessed from processor through Main I2C2 instance. Also, there is an option to Monitor the SoC and peripheral powers using external I2C Master.

Common processor has five-pin header (J12) with isolation circuit to interface the INA devices with external I2C Master. Buffer IC SN74CB3Q3125PWR (U69) is used to isolate the External I2C connections from the INA devices. The control of this buffer is provided from SYS_PWR_PG, which is enabled by default on power up.

External Power Monitor header details:

Mfr. Part# 68002-205HL (CON HDR 1X5 2.54MM PITCH ST TH)

Table 4-8. External Power Monitor Header Pinouts

Header (J12) Pin Number	Signal Name
1	CON_PM1_SCL
2	CON_PM1_SDA
3	DGND
4	CON_PM2_SDA
5	CON_PM2_SCL

Test automation header on the Common processor board also can access these INA devices externally.

4.6 Reset

Figure 4-7 shows the J721E EVM reset architecture.

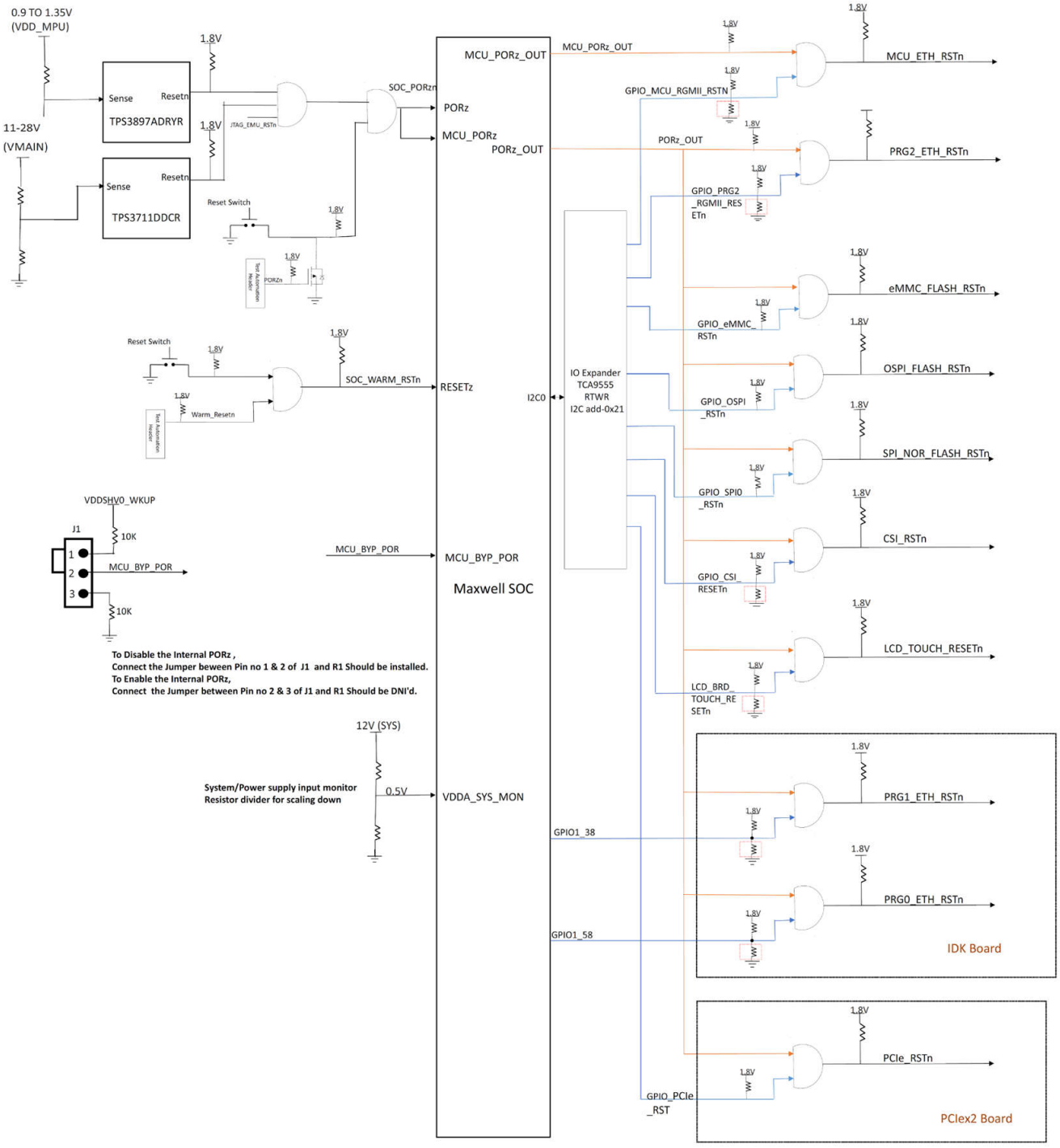


Figure 4-7. EVM Reset Architecture

4.7 Clock

Figure 4-8 shows the J721E EVM clock architecture.

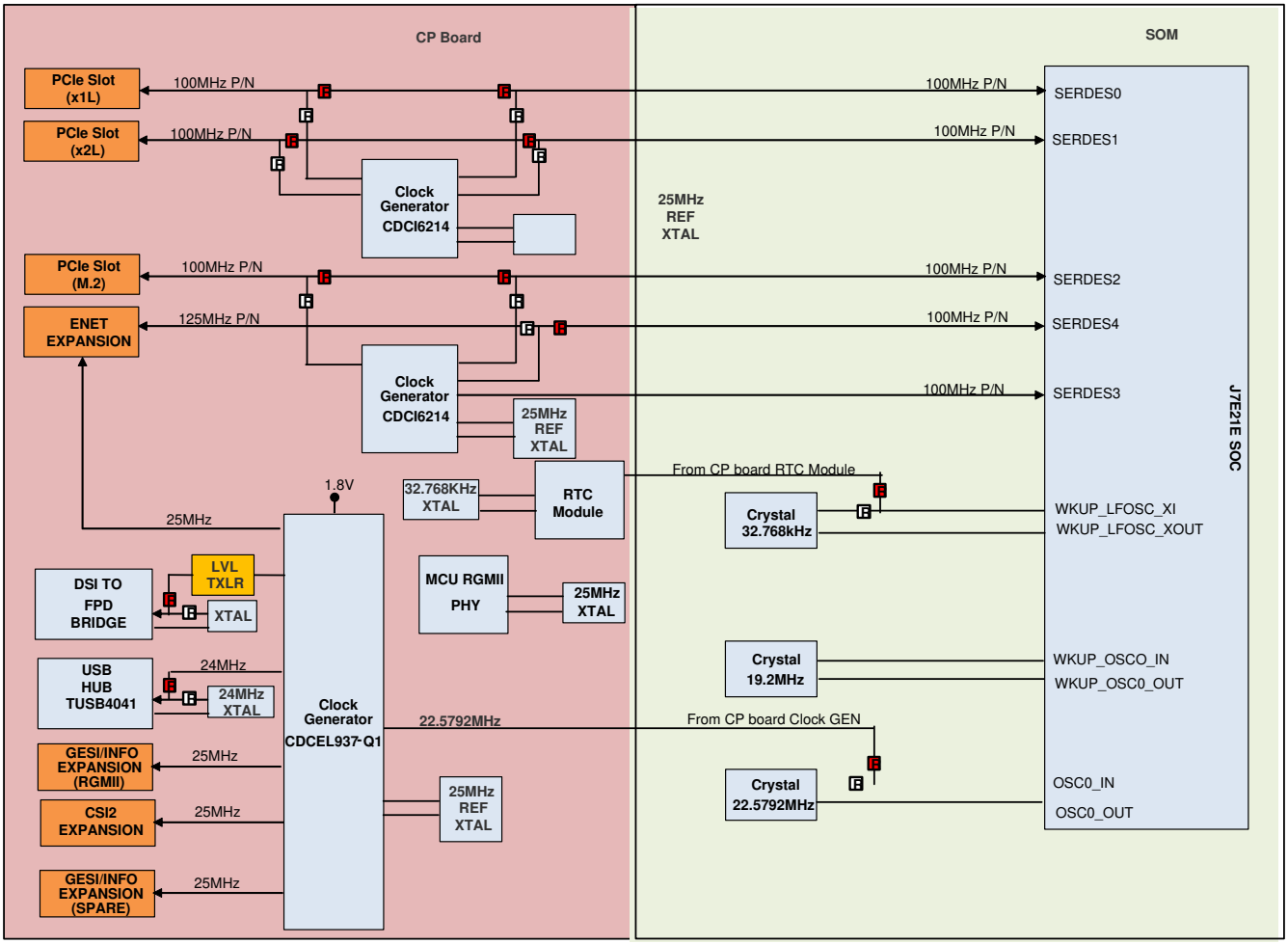


Figure 4-8. EVM Clock Architecture

EVM supports multiple Crystals and Clock generator to provide the reference clock input to the SoC and EVM peripherals.

4.7.1 Processor's Primary Clock

There are three external crystals attached to the J721E processor to provide the SoC's Primary clocks WKUP_LFOSC (32 KHz), WKUP_OSC0 (19.2 MHz) and OSC1 (22.5792 MHz) as shown in Figure 4-9.

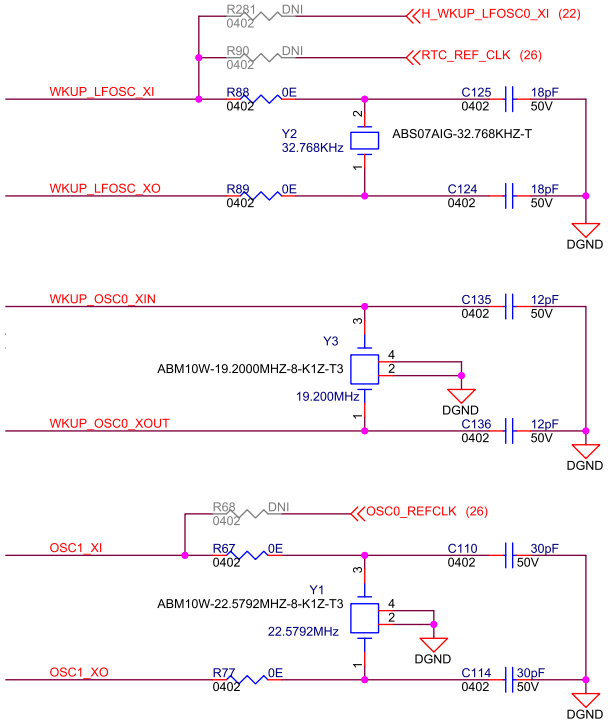


Figure 4-9. J721E SoC Primary Clock

The WKUP_OSC0 is required by the processor. Both WKUP_LFOSC and OSC1 are optional clocks (not required for J721E processing). The WKUP_LFOSC can be sourced either on the on-board crystal or from the PMIC. The OSC1 can be sourced from either the on-board crystal or from clock generator (CDCEL937) on the Common Processor board.

4.7.2 Processor's Secondary/SERDES Ref Clock

In addition to the Primary clock, the SERDES reference clocks to the SoC is sourced from the Clock Generator (CDCI6214) on the Common processor board. All these clocks are 100 MHz with HCSL level for the SoC's SERDES reference clock input. The programming of CDCI6214 chip is done through J721E SoC's I2C0 port.

There are two CDCI6214 clock generators available to source the SERDES reference clocks to SoC. The CDCI1 (U22) is not connected to I2C0 port by default. The clocks from CDCI1 (U22) is derived using factory programmed configuration.

Only the CDCI2 (U17) is required I2C programming for the desired clock outs from each channel. A 25 MHz crystal is attached the each CDCI chip for its reference clock inputs.

Table 4-9. Processor's Secondary/SERDES Ref Clock

Signal/Net Name	Probe Point	Clock Gen/CH	Description	Frequency
CLKGEN_SERDES1_REFCLK_P/N	R176/ R167	CDCI1/Y1	100MHz HCSL Clock to SoC SERDES1	100 MHz
CLKGEN_PCIE0_1L_REFCLK_P/N	R143/ R142	CDCI1/Y2	100 MHz HCSL Clock to PCIe0 x1 L Socket	100 MHz
CLKGEN_SERDES0_REFCLK_P/N	R145/ R153	CDCI1/Y3	100 MHz HCSL Clock to SoC SERDES0	100 MHz
CLKGEN_PCIE0_2L_REFCLK_P/N	R168/ R177	CDCI1/Y4	100 MHz HCSL Clock to PCIe0 x2 L Socket	100 MHz
CLKGEN_SERDES2_REFCLK_P/N	R158/ R157	CDCI2/Y1	100 MHz HCSL Clock to SoC SERDES2	100 MHz
CLKGEN_USB_REFCLK_P/N	R160/ R159	CDCI2/Y2	100 MHz HCSL Clock to SoC USB	100 MHz
QSGMII_PHY_REFCLK_P/N	C108/ C109	CDCI2/Y3	125 MHz LVDS Clock to Ethernet Expansion board	125 MHz
CLKGEN_PCIE2_2L_REFCLK_P/N	R123/ R124	CDCI2/Y4	100 MHz HCSL Clock to PCIe M.2 Socket	100 MHz

The PCIe reference clocks to the PCIe x1, x2 and M.2 sockets are also derived from the CDCI clock generators.

4.7.3 EVM Peripheral Ref Clock

The reference clocks to the EVM peripherals are sourced by the Clock generator (CDCEL937PWR) on the Common processor board, which is programmed through I2C0 port of processor. A 24-MHz crystal is attached to this clock generator to derive the desired clock outputs.

Table 4-10. EVM Peripheral Ref Clock

Signal/Net Name	Probe Point	Clock Gen/Ch	Description	Frequency
USB1_HUB_REFCLK	R80	CDCEL/Y1	24 MHz clock for USB Hub (not used by default)	24 MHz
DSI_REFCLK_1V8	R92	CDCEL/Y2	25 MHz clock for DSI transmitter ('941A)	25 MHz
QSGMII_REFCLK	R81	CDCEL/Y3	25 MHz clock for Ethernet Expansion Board	25 MHz
RGMII_REFCLK	R100	CDCEL/Y4	25 MHz clock for Expansion Board	25 MHz
CSI2_REFCLK	R101	CDCEL/Y5	25 MHz clock for CSI2 Expansion Board	25 MHz
OSC0_REFCLK	R82	CDCEL/Y6	22.5782 MHz clock for SoC (not used by default)	22.5782 MHz
EXP_REFCLK	R83	CDCEL/Y7	<not currently used>	24 MHz

Note

The probe points mentioned above are with reference to Common processor board.

4.8 Memory Interfaces

4.8.1 LPDDR4 Interface

The J721E SOM has 4GB of LPDDR4 using single 32Gb x 8-bit wide memory devices arranged in an 32-bit wide bus. The LPDDR4 interface can operate up to 3733 Mb/s speed. The LPDDR4 device is connected using T-branched routing for the clock and address/command lines and point-to-point connection for the data bus.

The Micron's LPDDR4 memory chip MT53D1024M32D4DT is used on the SoM, it requires 1.8 V for Core (VDD1), 1.1 V for Core2 (VDD2) and 1.1 V or 0.6 V for I/O buffer power (VDDQ). The VDDQ supplies are selected using a dip switch SW1 on the SoM. For more details, see Section 4.5.3.

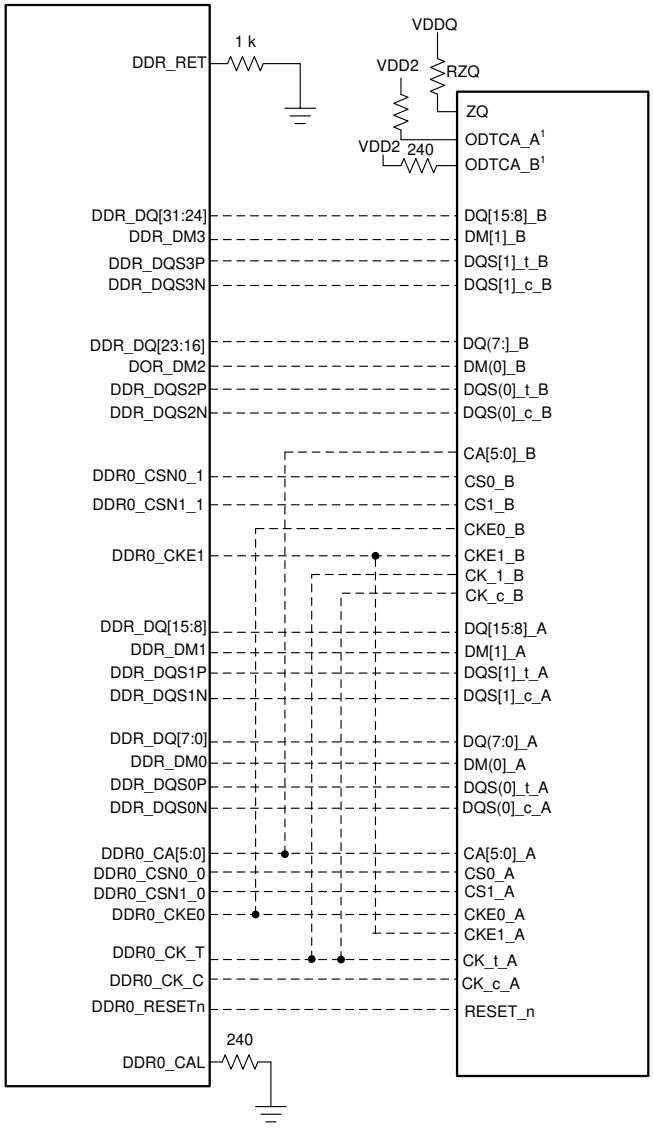


Figure 4-10. J721E SoM LPDDR4

4.8.2 OSPI Interface

The J721E SOM has 512 Mbit OSPI memory device of part number MT35XU512ABA1G12-0SIT connected to OSPI0 interface of J721E processor. The OSPI interface supports single and double data rates with memory speed up to 166 MHz SDR and 200 MHz DDR.

The SOM board also supports an option to include Hyper Flash + Hyper RAM Mfr. Part# S71KS512SC0, which is a 512 Mb flash + 64 Mb DRAM. 12-bit Active mux TS3DDR3812RUAR is provided to select either OSPI or HBMC interface. The selection of OSPI and hyper flash will be done by using a DIP (SW3) switch that is populated on the CP board. For more information, see Section 3.4.1.

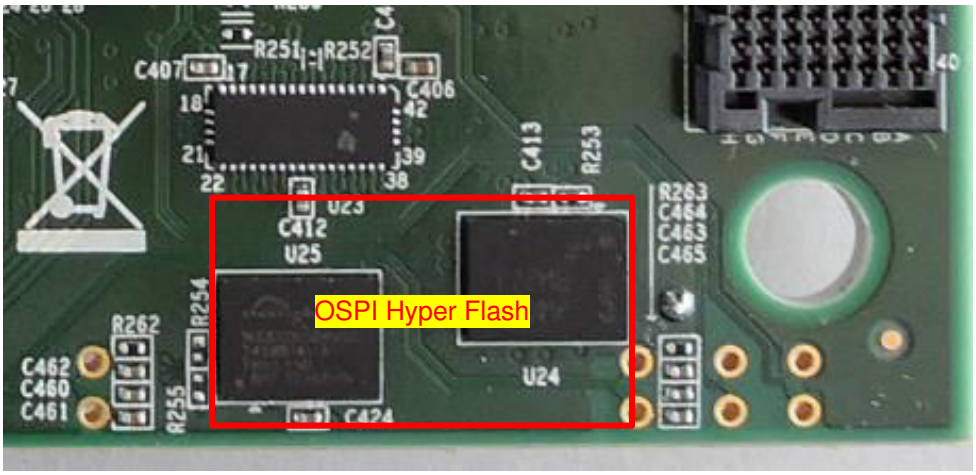


Figure 4-11. J721E SoM OSPI and Hyper Flash

4.8.3 UFS Interface

The Common Processor board has 32GB UFS memory device Mfr. Part# THGAF8G8T23BAIL connected to UFS0 port of SoC. The UFS memory is Gear3/2Lane capable and supports UFS Version 2.1.

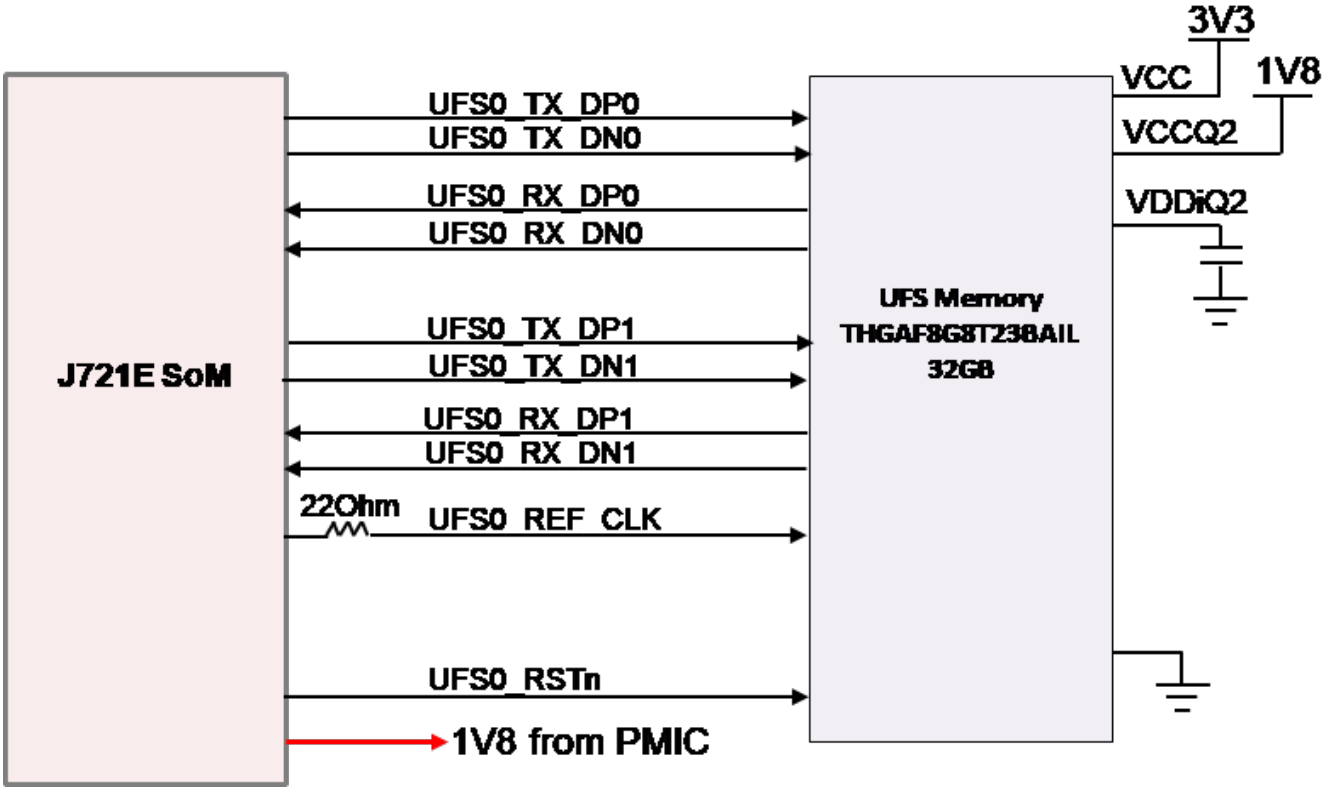


Figure 4-12. UFS Memory Block Diagram

4.8.4 MMC Interface

The processor supports two MMC (MMC0 and 1) ports. MMC0 is connected to eMMC flash and MMC1 is interfaced with Micro SD Socket on the Common processor board.

4.8.4.1 MMC0 - eMMC Interface

A 16GB, V5.1 compliant eMMC flash memory Mfr. Part# MTFC16GAPALBH-AAT ES is interfaced to MMC0 port of the J721E SoC. The flash is connected to 8 bits of the MMC0 interface supporting HS400 double data rates up to 200 MHz. External pull up resistors 49.9K are provided on DATA [7:0], CMD and Reset signals, pull down resistor is provided on the data strobe signal to prevent bus floating.

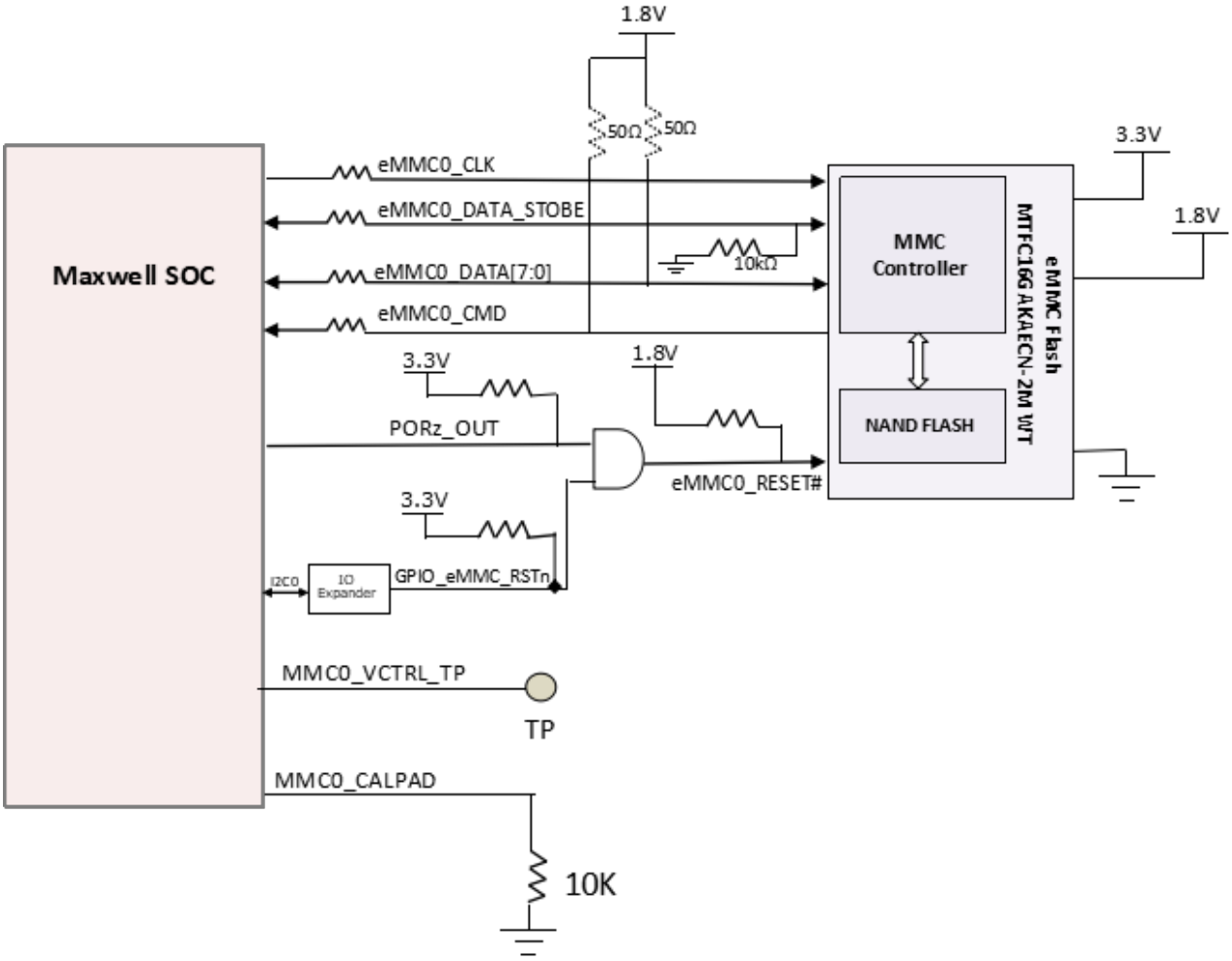


Figure 4-13. eMMC Memory Block Diagram

4.8.4.2 MMC1 – Micro SD Interface

The EVM supports a Micro SD card interface connected to MMC1 port of SoC. The Micro SD card socket Mfr. Part# DM3BT-DSF-PEJS is interfaced with MMC1 port of SoC. This supports UHS1 operation including I/O operations at both 1.8 V and 3.3 V. The Micro SD card interface is set to operate in SD mode by default.

The I/O voltage is controlled using the LDO that provides the I/O voltage for the MMC1 port. The SD Card power is provided using a load switch, which is controlled by a GPIO from I/O expander. Control signal "GPIO_uSD_PWR_EN" is driven by the I2C I/O expander U31 Port02 on the CP board. This I/O expander is controlled by the processor's I2C0 port. I2C address of the I/O expander is 0x22.

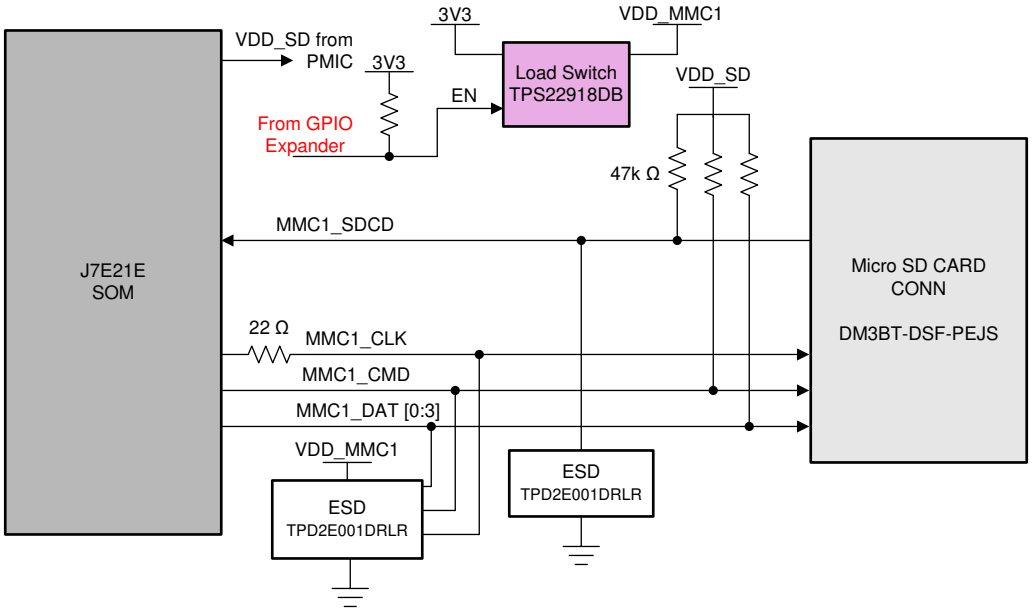


Figure 4-14. micro-SD Card Block Diagram

An ESD protection device Mfr. Part# TPD2E001DRLR is provided for data, clock, command and card detect signals. The CD (card detect) pin of Micro SD card socket is pulled high and connected to CD pin of SoC. An external pull up resistor (47K) is provided on data [3:0] and CMD signals to avoid floating.

4.8.5 Board ID EEPROM Interface

The J721E EVM boards are identified by its version and serial number, which are stored in the onboard EEPROM. The EEPROM is accessible from WKUP I2C0 port of J721E processor.

The board ID EEPROM I2C slave address of various boards are listed in the I2C mapping table.

The J721E SoM board includes a CAV24C256WEI2C EEPROM ID memory. The first 259 bytes of addressable EEPROM memory are preprogrammed with identification information for each board. The remaining 32509 bytes are available to the user for data or code storage.

Table 4-11. Board ID Memory Header Information

Header	Field Name	Size (bytes)	Comments
EE3355AA	MAGIC	4	Magic Number
	TYPE	1	Fixed length and variable position board ID header
		2	Size of payload
BRD_INFO	TYPE	1	Payload type
	Length	2	Offset to next header
	Board_Name	16	Name of the board
	Design_Rev	2	Revision number of the design
	PROC_Nbr	4	PROC number
	Variant	2	Design variant number
	PCB_Rev	2	Revision number of the PCB
	SCHBOM_Rev	2	Revision number of the schematic
	SWR_Rev	2	First software release number
	VendorID	2	
	Build_Week	2	Week of the year of production
	Build_Year	2	Year of production
	BoardID	6	
	Serial_Nbr	4	Incrementing board number
DDR_INFO	TYPE	1	
	Length	2	Offset to next header
	DDR control	2	DDR Control Word
MAC_ADDR	TYPE	1	Payload type
	Length	2	Size of payload
	MAC control	2	MAC header control word
	MAC_adrs	192	
END_LIST	TYPE	1	End Marker

4.8.6 Boot EEPROM Interface

A 1-Mbit EEPROM is interfaced to MCU_I2C0 for booting, I2C address set to 0x50, 0x51.

4.9 MCU Ethernet Interface

The EVM includes RGMII connection between DP83867ERGZT Gigabit Ethernet PHY and the MCU domain network subsystem (NSS) of the Processor. RJ45 connector (J35) with Integrated magnetics LPJG163144NL is used.

A reference clock of 25 Mhz will be generated onboard using a crystal to DP83867ERGZT.

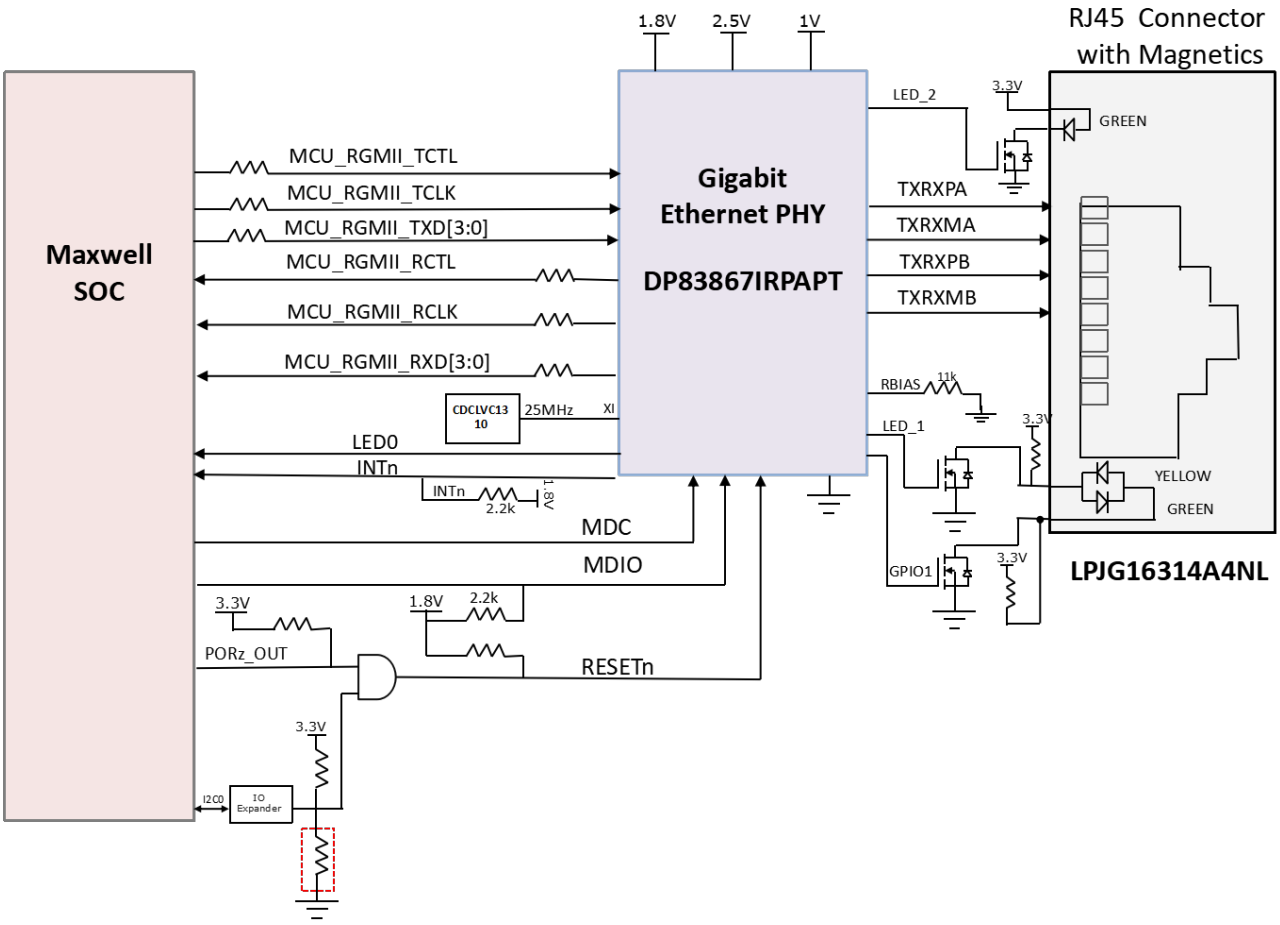


Figure 4-15. MCU Gigabit Ethernet Block

The I/O supply to the Ethernet PHY is set through selection Resistors R445 and R446 to support both 1.8 V and 3.3 V I/O level. The EVM is configured to 3.3 V I/O supply for MCU RGMII PHY I/O signals by default.

4.9.1 Gigabit Ethernet PHY Default Configuration

The default configuration of the DP83867 is determined using a number of resistor pull-up and pull-down values on specific pins of the PHY. Depending on the values installed each of the configuration pins can be set to one of four modes by using the pull up and pull down options provided. The EVM uses the 48-pin QFN package, designated with the RGZ suffix, which supports only RGMII interface.

The DP83867 PHY uses four level configurations based on resistor strapping that generate four distinct voltages ranges. The resistors are connected to the RX data and control pins that are normally driven by the PHY and are inputs to the processor. The voltage range for each mode is shown below:

- Mode 1 - 0V to 0.3V
- Mode 2 – 0.462 V to 0.6303 V
- Mode 3 – 0.7425 V to 0.9372 V
- Mode 4 – 2.2902 V to 2.9304 V

These are the defaults set for the MCU RGMII.

- PHY ADDR: 00000
- Auto_neg: Enabled
- ANGsel 10/100/1000
- RGMII Clk skew Tx: 0 ns
- RGMII Clk skew Rx: 2 ns

The strapping resistors are shown in Figure 4-16.

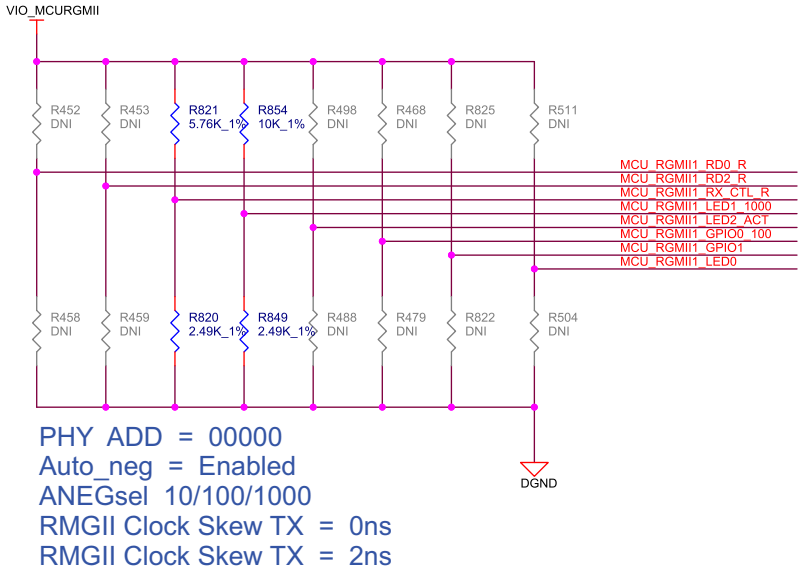


Figure 4-16. MCU Ethernet PHY Settings

4.10 QSGMII Ethernet Interface

The SERDES0 SGMII2 signals of J721E SoC is interfaced to Quad SGMII PHY VSC8514XMK-11 on the Quad Port Ethernet board through CP board, two stacked RJ45 connectors with integrated magnetics PN# LPJG17512AONL used for external communication.

The VC8514 device includes three external PHY address pins, PHYADD [4:2] to allow control of multiple PHY devices on a system board sharing a common management bus. These pins set the most significant bits of the PHY address port map. The lower two bits of the address for each port are derived from the physical address of the port (0 to 3) and the setting of the PHY address reversal bit in register 20E1, bit 9.

Reference clock to the PHY is generated from SERDES clock generator (CDCI2) on the CP board by default. Optionally, clock generator on the Quad Port Ethernet board also can provide the clock to the PHY with resistor option.

Table 4-12. Clock Source Selection

Clock Source	Install	Remove
From CP Board (Default)	R1, R2	R3, R4
From On board clock generator	R3, R4	R1, R2

Programming of the clock generator is done through I2C0 port of the SoC. I2C signals to the on board clock generator is connected through an active switch and paths are disconnected by pulling the CDCI_I2C_SEL signal low. Since, both on-board and CP board clock generators have the same I2C slave address, the programming of these clock generators will need special attention. While programming on board clock generator, the clock generator (CDCI2) on the common processor boards will need to be under reset.

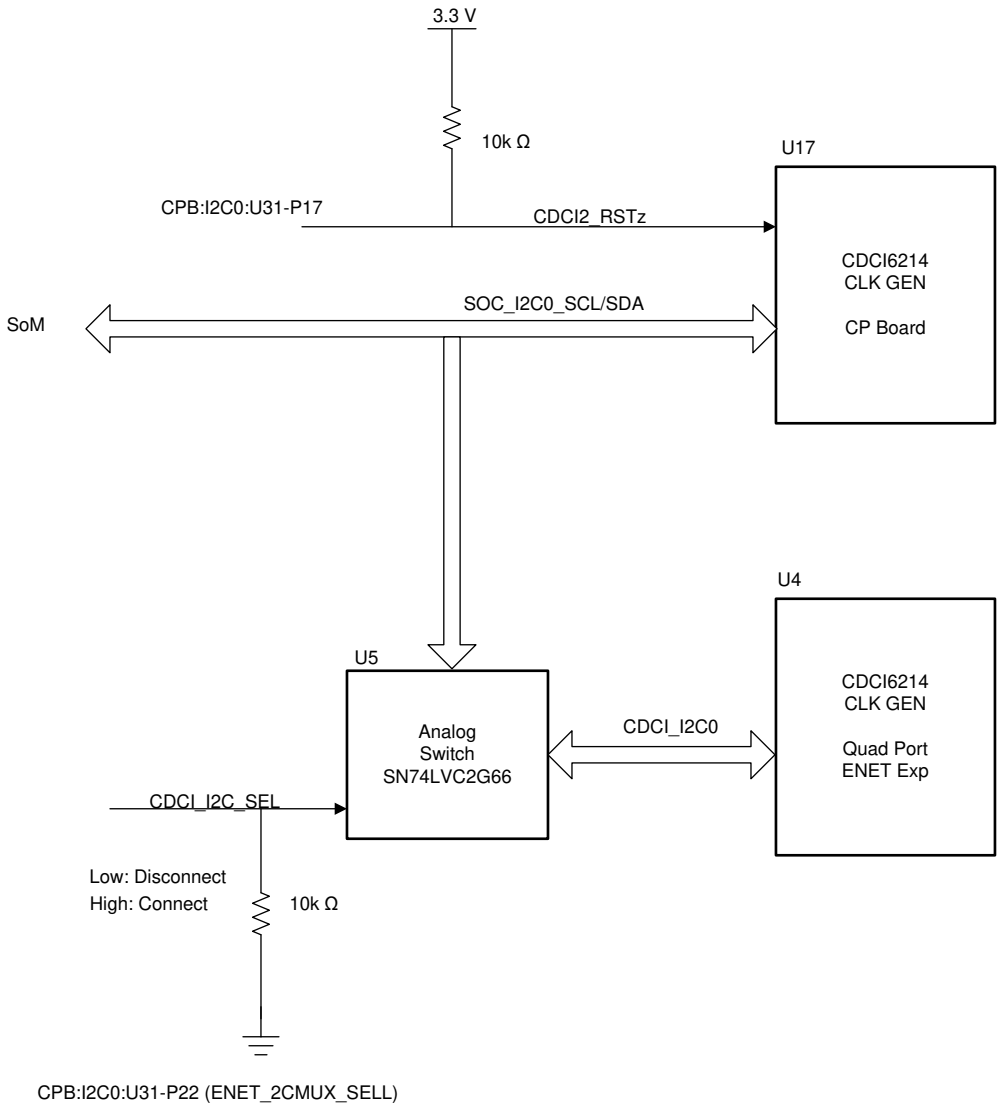


Figure 4-17. Quad-SGMII Board I2C

Coupling capacitors (0.1 µF) added in series at the respective driver ends on the QSGMII data signals.

The address and clock configurations are shown below:

- PHY0: 10000 0X10
- PHY1: 10001 0X11
- PHY2: 10010 0X12
- PHY3: 10011 0X13

The resistor strapping options are shown in Figure 4-18.

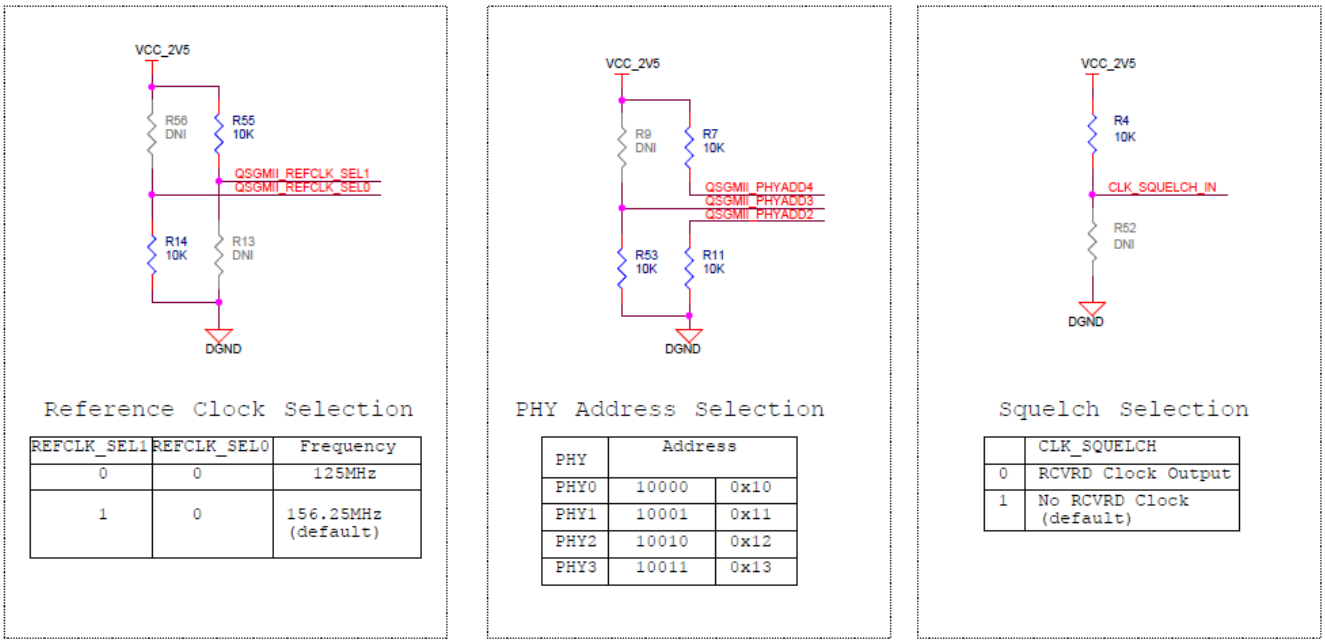


Figure 4-18. QSGMII Ethernet PHY Settings

4.11 PCIe Interface

The Common processor board is supporting two X4 lane (One for x1L and One for x2L interface), PCIe connector to accept PCIe form factor daughter card and support PCIe Gen4 operation. The EVM also supports the PCIe M.2 socket to interface the M keyed PCIe M.2 form factor modules, which are not included in the EVM kit.

4.11.1 X1 Lane PCIe Interface

The x1 lane PCIe interface includes one x4 lane PCIe connector of part number Amphenol 10142333-10111MLF, which supports PCIe Gen4 operation. The pin-out of the connector follows PCIe standard.

The SERDES0 port of J7 SoC is connected to x1 lane PCIe socket for data transfer. PCIe0, USB0_SS and SGMII1, 2 interfaces are pinmuxed with this SERDES0 port.

I2C0 from SoC is used for control purpose and is connected to SMBUS on the connector. I2C0 port is connected to both x1 lane and x2 lane PCIe connectors using a Mux TCA9543APWR.

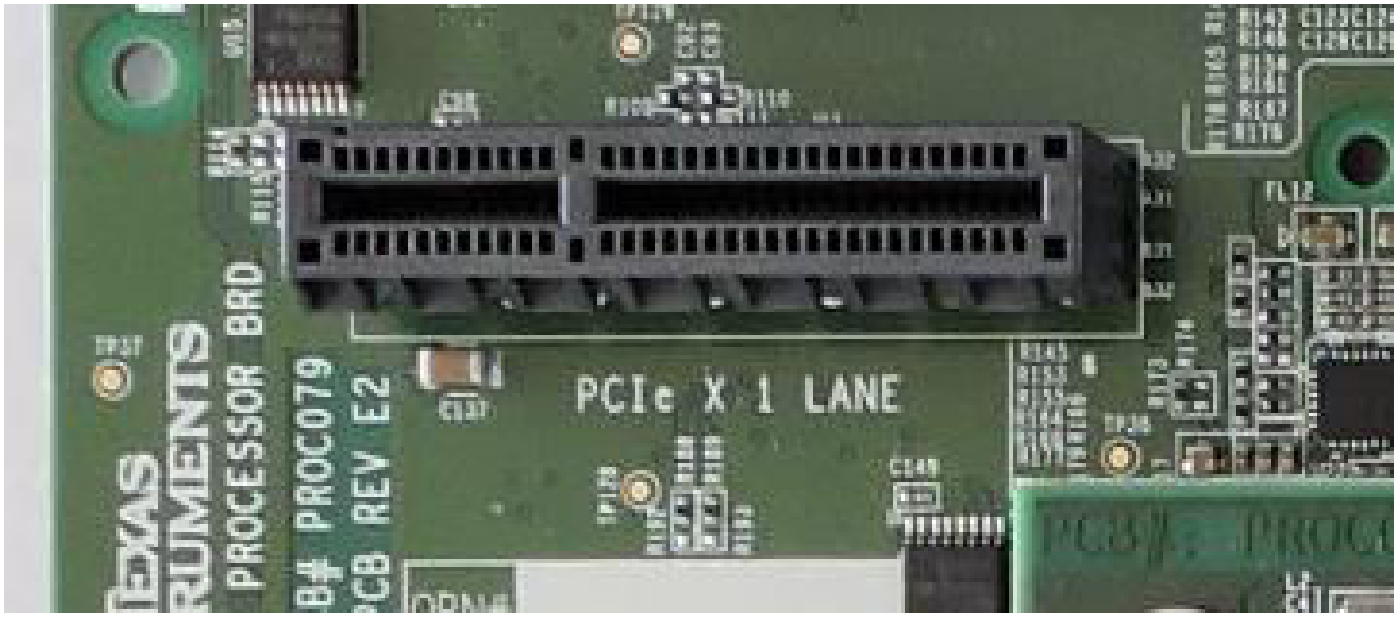


Figure 4-19. PCIe Interface for SERDES0

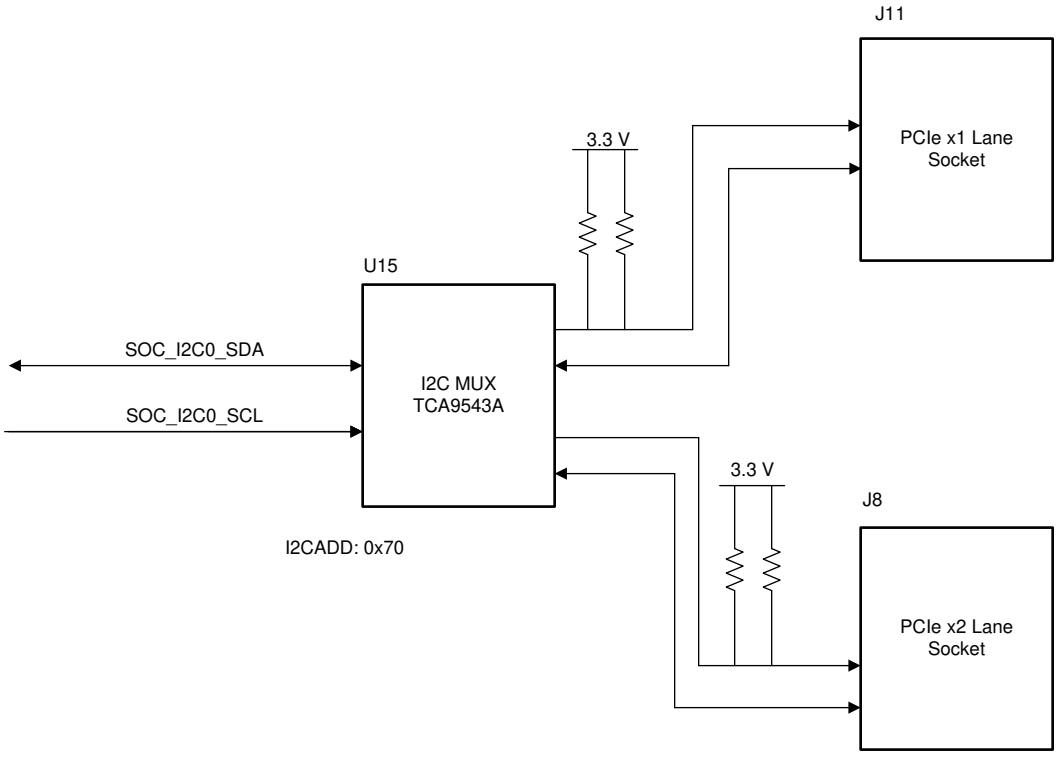


Figure 4-20. PCIe SMBUS Block Diagram

Whereas, in case of PCIe end point operation, the CP board receives reset signal from the PCIe card.

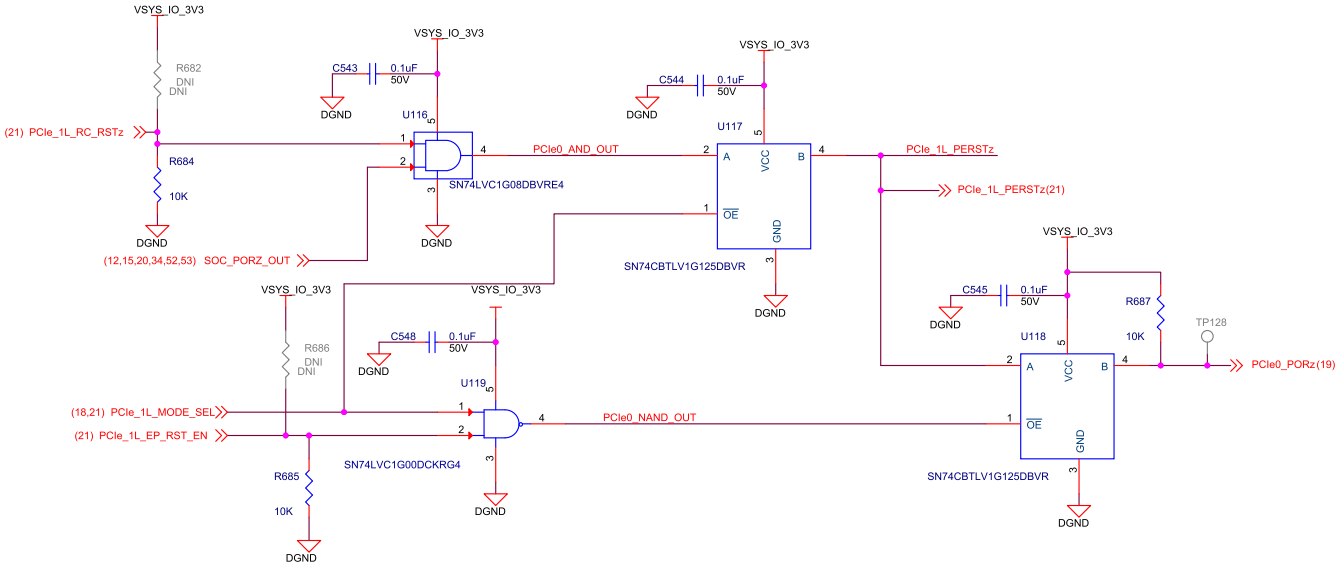


Figure 4-21. 1L-PCIe Root Complex/Endpoint Selection Circuit

Clock: A clock generator (CDCI #1) is provided to drive 100 MHz HCSL clock for PCIe add on cards and SoC. Resistor options are provided to select the clock source for host and end point operation.

For PCIe host operation:

- The add on cards can have clocks driven by SOC or clock generator. Selection can be made through resistors as shown in Table 4-13.

Table 4-13. Reference Clock Selection for PCIe Host Operation

Clock Selected	Mount	Unmount
Reference Clock for SOC from clock generator	R194	R195, C92
	R198	R199, C93
Reference Clock for PCIe connector from SOC	R195, C92	R194, R109
	R199, C93	R198, R110
Reference Clock for PCIe connector from clock generator	R109	R195, C92
	R110	R199, C93

For PCIe Endpoint operation:

- The SOC can have the clock driven by add on cards or clock generator. Selection can be made through resistors as shown in Table 4-14.

Table 4-14. Reference Clock Selection for PCIe Endpoint Operation

Clock Selected	Mount	Unmount
Reference clock for SOC from clock generator	R194	R195, C92
	R198	R199, C93
Reference clock for SOC from PCIe connector	R195, C92	R194, R109
	R199, C93	R198, R110

For choosing Host or device operation of PCIe card, following resistors must be mounted/unmounted as mentioned in Table 4-15.

Table 4-15. Resistors for Selecting PCIe Card Host or Device Operation

Mode	Mount	Demount
Host mode	R674	R675
	R679	
Device mode	R675	R674
		R679

Additional Options:

Optional MDIO bus and USB2.0 interface is supported for external PCIe add on cards.

SoC Main domain (CPSW9G0) MDIO signals are interfaced to the x1L PCIe Socket (J11) through 0-Ω inline resistors (R137 and R136) when network (Ethernet) based add on cards inserted into J11. The path is disconnected by default.

Also, USB2.0 data signals from USB HUB downstream port is interfaced to 4 pin header (J2) and the 5 V supply is provided through the load switch.

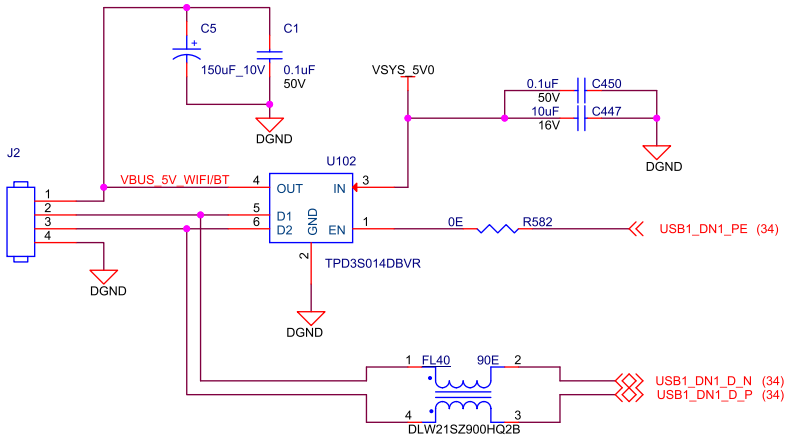


Figure 4-22. USB2.0 Header Connection

4.11.2 X2 Lane PCIe Interface

The x2 lane PCIe interface includes one x4 lane PCIe connector of part number Amphenol 10142333-10111MLF, which supports PCIe Gen4 operation. The pin-out of the connector follows PCIe standard.

The SERDES1 port of J7 SoC is connected to x1 lane PCIe socket for data transfer. PCIe1, USB1_SS, PRG1_SGMII0, 1 and SGMII3, 4 interfaces are pinmuxed with this SERDES1 port.

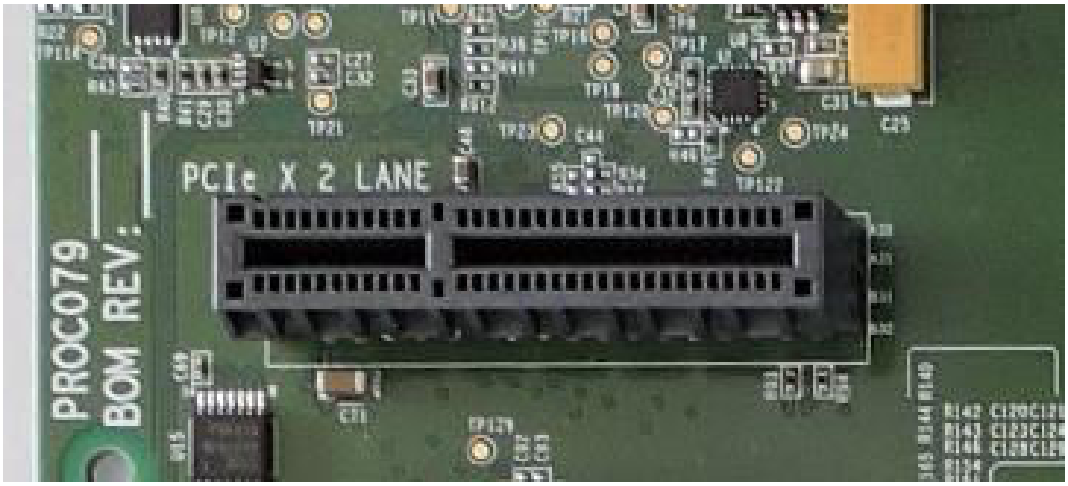


Figure 4-23. PCIe Interface for SERDES1

I2C0 from SoC is used for control purposes and is connected to SMBUS on the connector through I2C switch. The link activation signal (INT#) from both the X1 and X2 lane PCIe connectors is terminated to I2C switch.

Reset: A dip Switch (SW3) is provided to select the reset source for host and end-point PCIe operation.

In case of host mode, signal from GPIO Expander and PORz signals from SoC are ANDed and the output is connected to PCIe connector. The GPIO signal is pulled low to ensure PCIe Reset (#PERST) remains asserted until SoC releases reset.

Whereas, in case of PCIe end point operation, the CP board receives reset signal from the PCIe card.

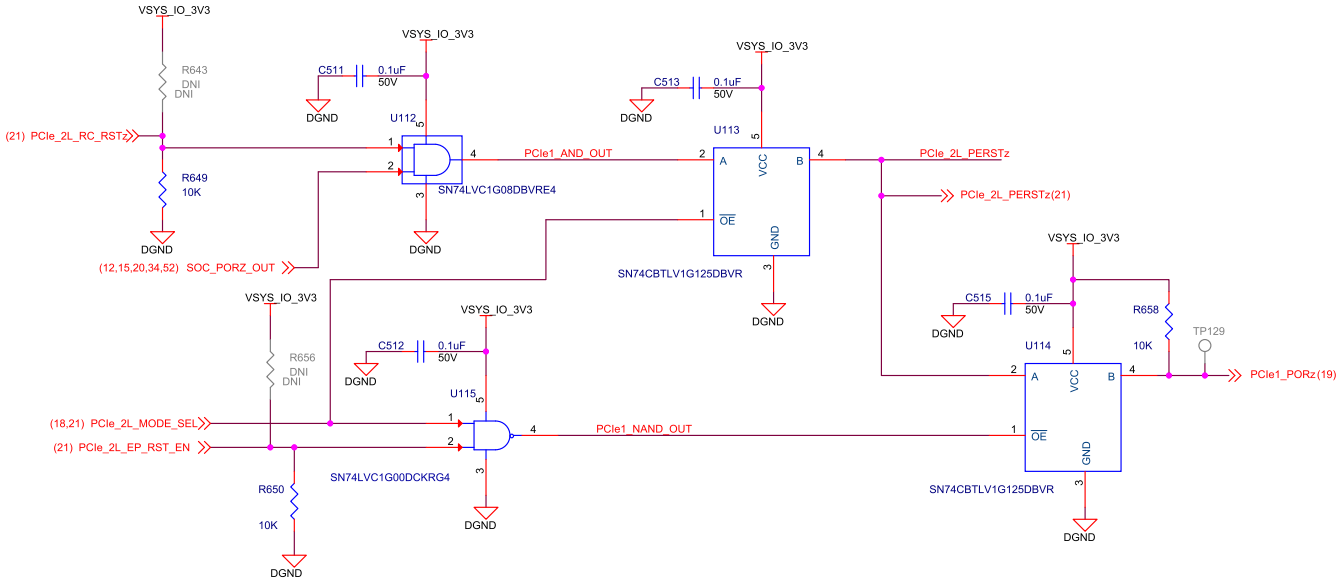


Figure 4-24. 2L-PCIe Root Complex/Endpoint Selection Circuit

Clock: Resistor options are provided to select the clock source for PCIe add on cards and J721e For PCIe host operation:

- The add on cards can have clocks driven by SoC or clock generator. Selection can be made through resistors as shown in Table 4-16.

Table 4-16. Reference Clock Selection for PCIe Host Operation

Clock Selected	Mount	Unmount
Reference Clock for SOC from clock generator	R214	R211, C44
	R213	R210, C51
Reference Clock for PCIe connector from SoC	R211, C44	R214, R54
	R210, C51	R213, R56
Reference Clock for PCIe connector from clock generator	R54	R211, C44
	R56	R210, C51

For PCIe Endpoint operation:

- The SoC can have the clock driven by add on cards or clock generator. Selection can be made through resistors as shown in Table 4-17.

Table 4-17. Reference Clock Selection for PCIe Endpoint Operation

Clock Selected	Mount	Unmount
Reference clock for SOC from clock generator	R214	R211, C44
	R213	R210, C51
Reference clock for SOC from PCIe connector	R211, C44	R214, R54
	R210, C51	R213, R56

Hot plug: The PRSNT1# and PRSNT2# signals are the hot plug presence detect signals. The PRSNT1# is pulled up and PRSNT2# is connected to GPIO expander, so that PRSNT1# will be pulled low when a add on card is plugged in as both the PRSNT signals in add on cards will be shorted. Optional resistor is provided to short the PRSNT1# and PRSNT2# to support host and device mode.

For choosing Host or device operation of PCIe card, the following resistors must be mounted/unmounted as mentioned in Table 4-18.

Table 4-18. Resistors for Selecting PCIe Card Host or Device Operation

Mode	Mount	Demount
Host mode	R631	R630
	R638	
Device mode	R630	R631
		R638

4.11.3 M.2 PCIe Interface

Common Processor board supports 2 Lane PCIe M2.0 standard, to interface external SSD device.

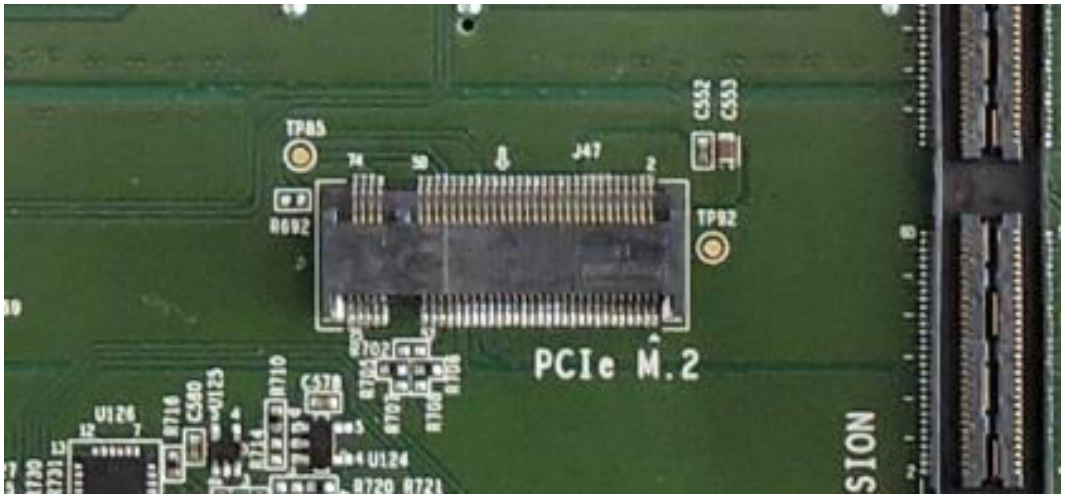


Figure 4-25. PCIe Interface for SERDES2

M.2 series receptacle with M-Keyed Mfr. Part# MDT320M01001 is used to attach the external SSD device on common processor board. The x2 lane PCIe interface signals SERDES2 of J721E SoC will be terminated with receptacle. SoC_I2C0 is used for SMBUS access. Voltage level translator (TCA9543APWR) circuit will be used to change the I/O level of SMBUS signals to 1.8 V. The link activation signal (WKUP) from PCIe connector is terminated to the test point TP85.

Reset: Reset signal to the SSD/add on module is controlled by GPIO expander. The GPIO signal is pulled low with a resistor 10K by default to ensure PCIe Reset (#PERST) remains asserted until SoC releases reset.

Clock: A clock generator (CDCI #2) is provided to drive 100MHz HCSL clock for PCIe add on cards and J721E SoC. Resistor options are provided to select the clock source either from SoC or clock generator.

4.12 USB Interface

The Common Processor Board includes the following USB interfaces:

- One USB 3.1 Type C interface using TUSB321RWBR and PTPS25830QWRHBTQ1 PD controller
- Four USB 2.0 Interfaces using USB Hub (TUSB4041IPAPR)
- (Not supported in J721E SoC) One USB 3.0 Micro AB connector. It is reserved for future J7 family devices.

4.12.1 USB 3.1 Interface

USB Super speed signals from SERDES3 port of J7E21E SoC are connected to USB Type C connector (2012670005). A CC and PD controller Mfr. Part# TUSB321RWBR and PTPS25830QWRHBTQ1 are used for CC detect and power delivery. This CC controller supports Dual Role Port (DRP), Downstream Facing Port (DFP) and Upstream Facing Port (UFP) modes, In CP board DRP, DFP and UFP modes can be selected through an EVM Configuration dip switch (SW3). The Dip switch settings are given in Table 3-5Table 6.

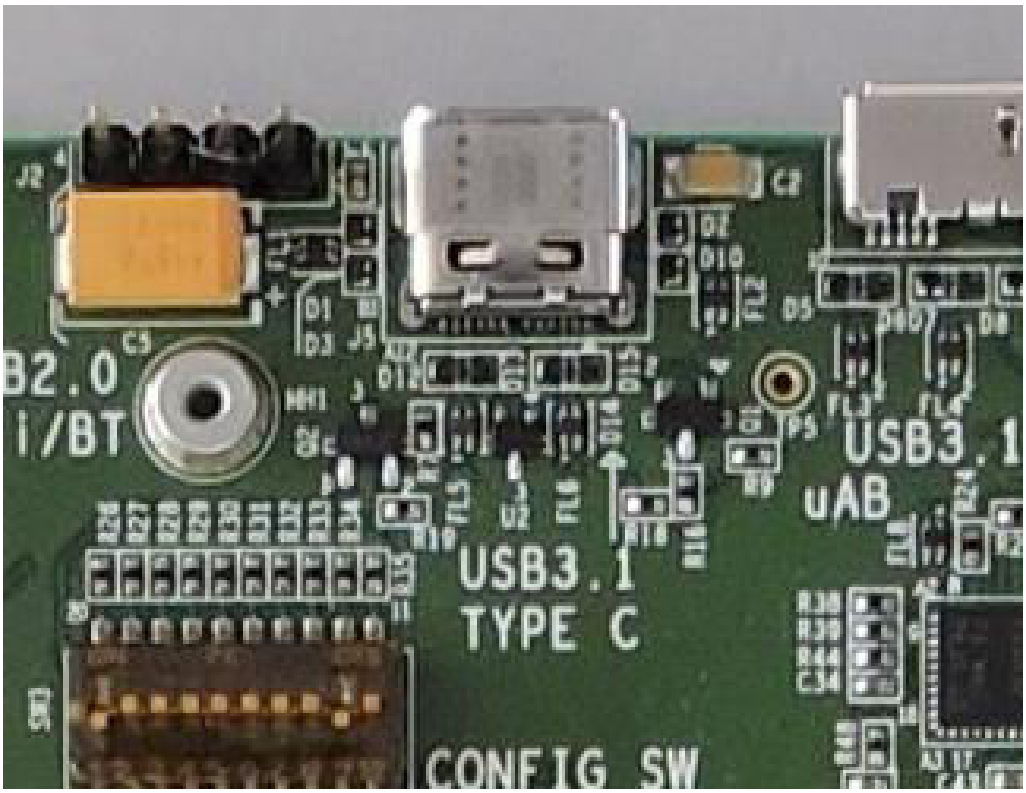


Figure 4-26. USB3.1 Type C Interface

The AC coupling capacitors are provided on TX lines of Super speed signals, and common mode filters (MCZ1210DH900L2TA0G) are used at all the differential pairs. ESD protection diodes are provided on all required USB Signals (TPD1E05U06DPY for super speed signals and TPD2E2U06-Q1 for CC pins). TUSB321‘s Current Mode pin is pulled high through 499K resistor to set the Maximum Current Iout to 1.5A.

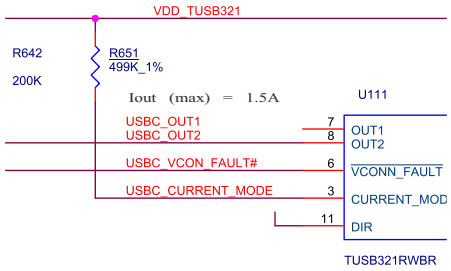


Figure 4-27. Type C Power Delivery Current Settings

The control signals for Powerdown and VBUS enable are given from I2C GPIO Expander2 (I2C add: 0x22 - P03) and the SoC DRVVBUS, respectively.

4.12.2 USB 2.0 Interface

The USB1 port of J721E SoC is used for USB 2.0 interface in J721E EVM. The USB1 signals are connected to upstream port of USB 2.0 Hub (TUSB4041IPAPR). The four downstream ports from USB Hub are connected are shown below:

- 2 USB ports are terminated to Type A Stacked Connector (AU-Y1008-2)
- 1 USB port is connected to 4 Pin Header (PCIe Card - WiFi/BT)
- 1 USB port is connected to EVM Expansion connector

The reference clock to the USB HUB is provided using 24 MHz crystal and also an optional clock input from the Peripheral clock generator using a resistor mux. The default clock source is set to crystal.

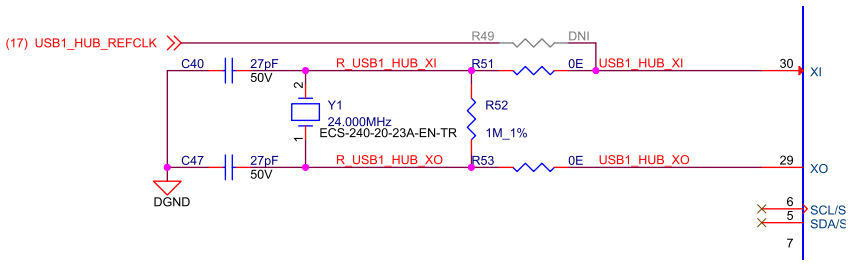
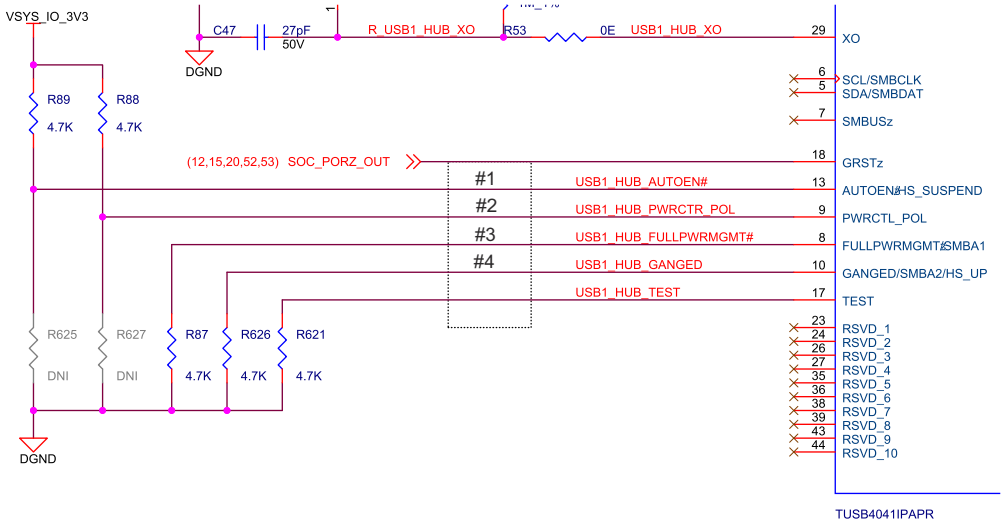


Figure 4-28. USB Hub Reference Clock Circuit

Figure 4-29 shows the USB HUB strapping options.



NOTE:

#1 Automatic Charge Mode Disabled
#2 PWRCTL Polarity is Active High
#3 Power Switching and Overcurrent Inputs Supported
#4 Individual Power Control Enabled

Figure 4-29. USB Hub Settings Circuit

And the USB ID pin is pulled low to operate the SoC in Host mode.

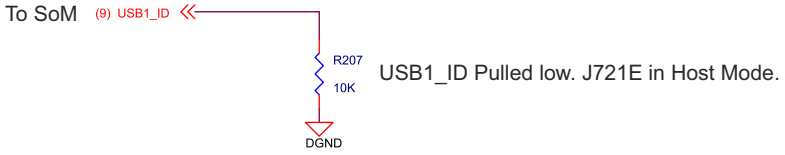


Figure 4-30. USB1 ID Setting for HUB

To PCIe Card Wi-Fi/BT:
The downstream port1 of USB HUB is connected to the Wi-Fi/BT header (J2) on the CP board. The power to the WiFi header is provided through current limit load switch with integrated ESD protection device TPD3S014DBVR. The power is controlled by USB hub power enable signal USB1_DN1_PE.

To Stacked Connector:

The downstreams port2 and 3 of USB HUB is connected to the stacked USB 2.0 Type-A receptacle AU-Y1008-2 on the CP board. The power to the USB Type-A receptacle is provided through current limit load switch with integrated ESD protection device TPD3S014DBVR for each port. The power is controlled by USB hub power enable signals USB1_DN2_PE and USB1_DN3_PE.

To Expansion Connector:

The downstream port4 of USB HUB is connected to EVM Expansion connector. The current version of EVM is not supporting any peripherals on this port. It is reserved for future development.

4.12.3 USB 3.0 Micro AB Interface (Reserved Port)

This is an optional interface provided for a future version of the J7 SoC only; it is not supported in the J721E EVM.

4.13 CAN Interface

The four CAN ports of J721E SoC (MCU_MCAN0, MCU_MCAN1, MCAN0, and MCAN2) is supported on the Common Processor board as explained below.

MCU CAN0

The MCU CAN0 port of J721E SoC is connected to the CAN transceiver with Wake function supported device TCAN1043-Q1. A 2-pin header J29 (68002-202HLF) is provided inline for user probe option.

The output of the CAN transceiver is terminated to a 4-pin header J30 (61300411121).

The signals MCU_MCAN0_H and MCU_MCAN0_L are routed as differential signals with 120E impedance with split termination. This Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

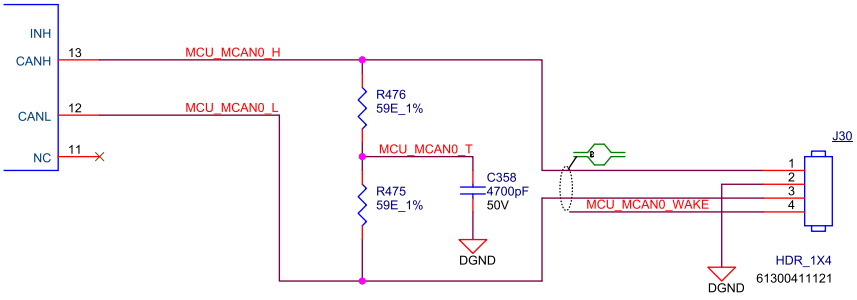


Figure 4-31. MCU CAN0 Interface

VSYS_MCU_5V0 to the CAN transceiver is generated using a Step-Up converter TPS61240DRV by giving VSYS_3V3 as input supply to the converter.

The STB signal is an active low signal held low with integrated pull down by default.

Hardware WAKEn input for the CAN interface is provided using a push-button SW12 available on the Common processor board bottom left corner. However, the MCU_CAN0 wake feature is disabled by default (resistor population). Only CAN wake-up supported is from MAIN domain.

MCU CAN1

The MCU CAN1 port of J721E SoC is connected to the CAN transceiver Mfr. Part# TCAN1042HGVD. A 2-pin header J34 (68002-202HLF) is provided inline for user probe option. This port does not support WAKE function. The signals MCU_MCAN1_H and MCU_MCAN1_L are terminated to a 3-pin header J31 (FCI: 68001-403HLF) with 120E split termination.

The STB signal is an active High signal held high with external pull up by default. The GPIO control from MCU domain provided to pull the line low.

MAIN CAN0 (Supports WAKE function)

The MAIN CAN0 port of J721E SoC is connected to the CAN transceiver with Wake function supported device TCAN1043-Q1. A 2-pin header J24 (68002-202HLF) is provided inline for user probe option.

The output of the CAN transceiver is terminated to a 4-pin header J27 (61300411121).

The signals MCAN0_H and MCAN0_L are routed as differential signals with 120E impedance with split termination. The STB signal is an active low signal held low with integrated pull down by default.

The VCC supply (5V) to the transceiver is derived from a Step-Up converter.

Hardware WAKEn input for the CAN interface is provided using a push-button SW12.

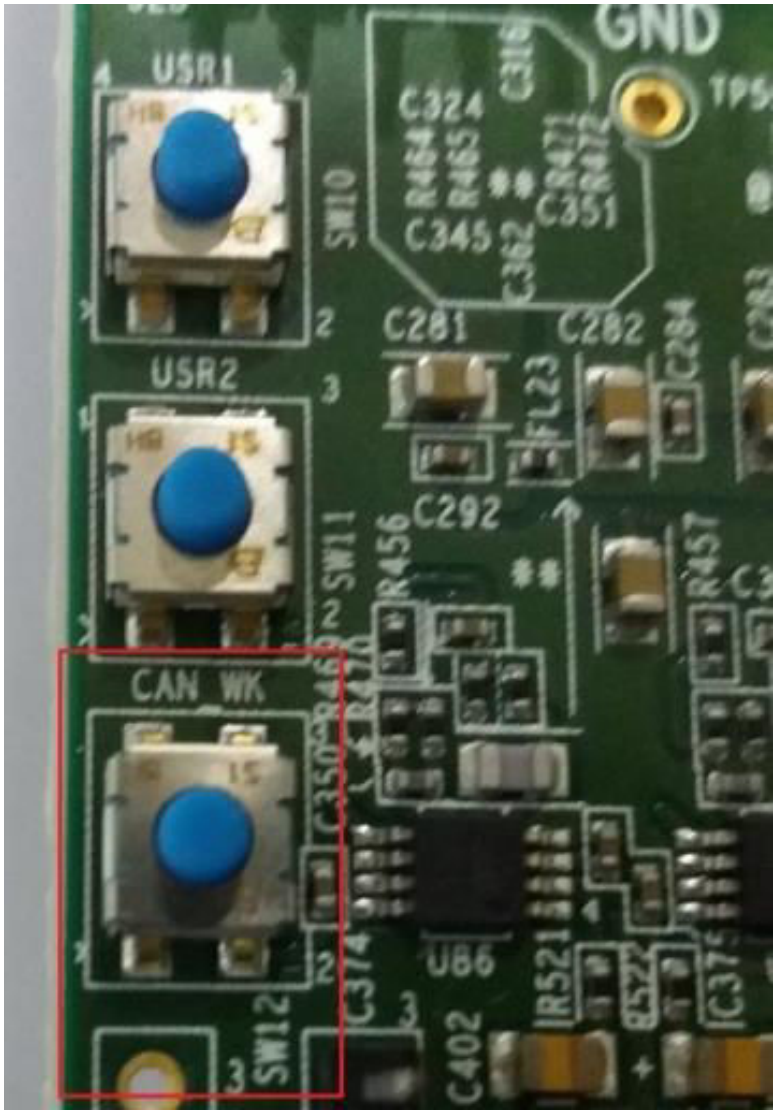


Figure 4-32. CAN Wake Push Button

The CAN Wake signals of both MCU CAN0 and MAIN CAN0 transceivers are tied together and limited the voltage level to 1.8V using a Zener diode and terminated to SOM -CP B2B connector.

MAIN CAN2

The MAIN CAN2 port of J721E SoC is connected to the CAN transceiver Mfr. Part# TCAN1042HGVD. A 2-pin header J25 (68002-202HLF) is provided inline for user probe option. This port does not support WAKE function. The signals MCAN2_H and MCAN2_L are terminated to a 3-pin header J28 (68001-403HLF) with 120E split termination.

The STB signal is an active High signal held high with external pull up by default. The GPIO control from MAIN domain provided to pull the line low.

To interface these CAN signals to Test system, the below given custom converter to be prepared.

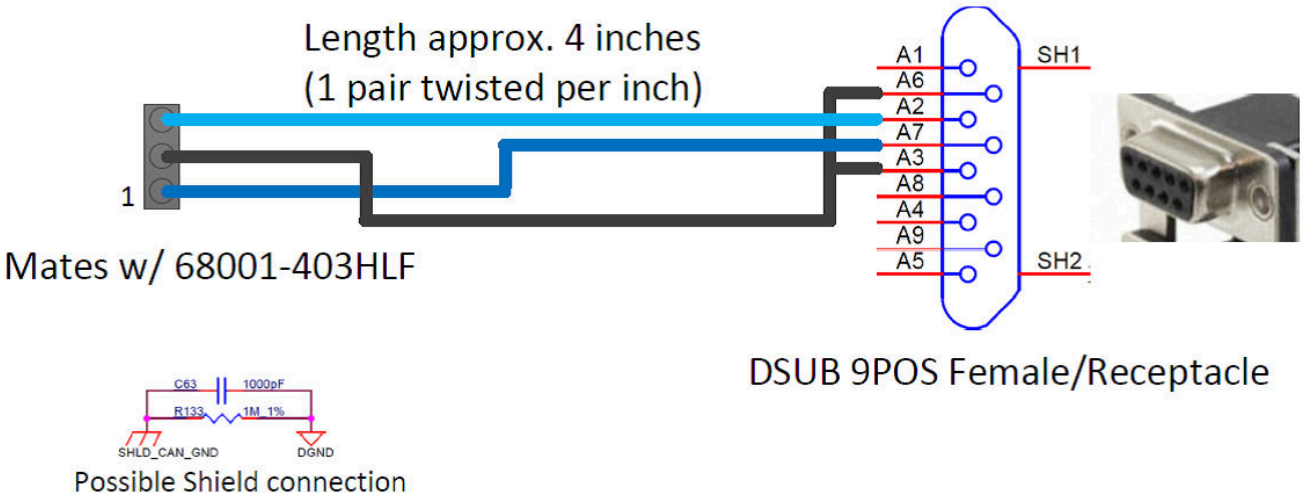


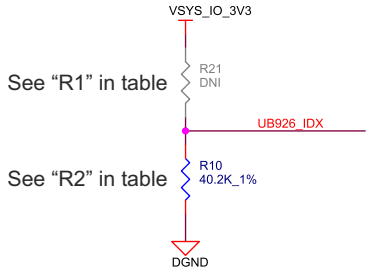
Figure 4-33. CAN Header Connections to DB9/Test Instrument

4.14 FPD Interface (Audio Deserializer)

CP Board supports TI ‘s FPD Link III De-serializer IC Mfr. Part# DS90UB926QSQE for recover the audio signals from Tuner interface using HSD connector Mfr. Part# D4S20G-400A5-C. The de-serializer will recover up to eight digital audio channels plus I2C channel across digital link.

This audio signal shall be connected to McASP11 port of J721E SoC through 1:3 DEMUX (SN74CBT16214CDGGR). The channel selection is supported by both GPIO expander and EVM configuration DIP switch (SW3).

The I2C3 signals of J721E being used for controlling of the De-serializer. A 40.2KΩ pull down is provided on ID[X] pin to set the 7‘b I2C address to 0x2C.



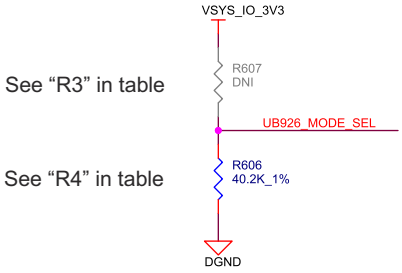
7b’ I2C Address	R1	R2
0x2C	Open	40.2K
(other – see DM)		

Figure 4-34. FPD-Link UB926 ID Setting Circuit

Power +12 V is provided to the HSD connector using a power switch TPS1H100AQPWPRQ1 to power the FPD Link-III Tuner expansion board. The power switch is controlled by a GPIO expander signal (UB926_PWR_SW_CNTRL).

Figure 4-35 shows the mode selection for the de-serializer.

MODE Selection



Selected Mode: 0 (Default)	Software Config Only
LFMODE (15 – <85 MHz) REPEATER (OFF) BACK-COMPATIBLE (OFF) I2S–B OFF. 24B RGB	LFMODE (15 – <85 MHz) REPEATER (OFF) BACK-COMPATIBLE (OFF) I2S–B OFF. 24B RGB
R3 = <open> R4 = 40.2K, 1% (or any)	R3 = <open> R4 = 40.2K, 1% (or any)

Figure 4-35. FPD-Link UB926 Mode Selection Circuit

Table 4-19 lists the pinout for the HSD connector J1.

Table 4-19. FPD Audio Deserializer HSD Connector Pinout

Pin No	Signal
1	GND
2	RIN_N
3	POWER (12V)
4	RIN_P

4.15 FPD Panel Interface (DSI Video Serializer)

CP Board supports TI ‘s DSI to FPD Link III Serializer IC Mfr. Part# PDS90UB941ASRTDTQ1.

DSI0 port of J721E SOC shall be connected to DSI to FPD-Link III serializer bridge and FPD Link-III signals are terminated to HSD connector of Mfr. Part# D4S20G-400A5-C to interface with display panel.

Reference clock to the FPD bridge is provided from Peripheral clock generator (CDCEL) and onboard clock oscillator ASDMB-25.000MHZ-XY-T with the resistor option. The default clock source is selected to onboard clock oscillator.

The I2C1 signals of J721E being used for controlling of the FPD bridge. A 30.1KΩ pull up and 61.9KΩ pull down is provided on ID[X] pin to set the 7‘b I2C address to 0x16.

The device Alias ID and the Mode selection is set by hardware strap resistors, as shown in Figure 4-36.

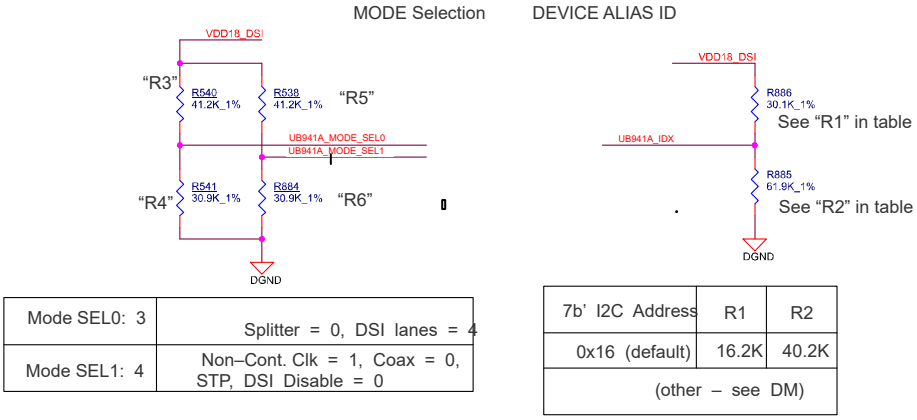


Figure 4-36. FPD-Link UB941A Device Settings Circuit

Power +12 V is provided to the HSD connector using a power switch TPS1H100AQPWPRQ1 to power the display panel. The power switch is controlled by a GPIO expander signal (PWR_SW_CNTL_DSI0).

Table 4-20 lists the pinout for the HSD connector J45.

Table 4-20. DSI to FPD Serializer HSD Connector Pinout

Pin No	Signal
1	DOUT0_P
2	POWER (12V)
3	DOUT0_N
4	GND

4.16 Display Serial Interface (DSI) FPC

The J721E EVM supports DSI interface over FPC connector 52559-3652 by using the resistor mux on the J721E DSI0 port. By default, the resistor mux is set to route the DSI0 signals to FPD Serializer. The power (12 V and 3.3 V), I2C1 interface and GPIO controls (RESET and INTn) are supported in the DSI FPC connector to interface with external display panel.

4.17 Audio Interface

Common Processor Board supports TI ‘s Audio Codec IC Mfr. Part# PCM3168APAP, to interface with J721E SoC McASP Port 10. A 1:3 De-Mux (Mfr. Part# SN74CBT16214CDGGR) Port B1 is used to interface McASP port 10 with codec. Port Selection is controlled by a I2C GPIO Expander and EVM Configuration switch. Table 4-21 shows the MUX table.

Table 4-21. MCASP/TRACE - 1:3 MUX: Truth Table

MUX_SEL2	MUX_SEL1	MUX_SEL0	Function	
High	High	Low	A port = B1 port	(default)
High	High	High	A port = B2 port	
High	Low	High	A port = B3 port	

- Port B1: McASP10
- Port B2: TRACE
- Port B3: GPMC

The Reference clock (SCKI) to the codec device is sourced from processor’s AUDIO_EXT_REFCLK2 using 1 to 2 Fan out clock buffer SN74LVC2G125DCUR, the secondary output clock from the fan out buffer is routed to EVM expansion connector to interface to Infotainment Audio Codec devices.

The MODE pin is held LOW to select I2C as control interface. Codec is configured over I2C3 interface. Default I2C address is set to 0x44. The device reset is controlled by the I2C GPIO expander using a I2C3 master port.

Line IN Port:

Single ended Stereo 1x Line Input signal from the Audio Jack J38 is converted to differential using “single ended to differential converter with Anti-aliasing low pass fiter” and interfaced with CODEC.

MIC Input Port:

Single ended Stereo 2x MIC Input signals from the stacked Audio Jack J39 is converted to differential using “single ended to differential converter with Anti-aliasing low pass fiter” and interfaced with CODEC. Pre-Amplifier circuit is provider inline to LPF circuit to amplify the external microphone inputs.

Microphone Input ports can be configured for Active and Passive microphones and also can be configured for Line Input. The configuration is set by the resistor option, as shown in Table 4-22.

Table 4-22. Config Table (1)

		Install	Remove
PASSIVE-MIC (default)	BIAS + PREAMP	R2, R3, R5, R6	R1, R4
ACTIVE-MIC	BIAS ONLY	R1, R2, R4, R5	R3, R6
LINE-INPUT	NO BIAS/PREAMP	R1, R4	R2, R3, R5, R6

(1) The Reference Rx provided in this table denotes the text provided in the schematics.

Line Out Port:

2x digital Outputs from the CODEC is converted to single ended and terminated to stereo Audio jack J40 bottom port using “differential to single ended” converter Line out circuit.

Head Phone Port:
6x differential digital Outputs from the CODEC is converted to single ended and terminated to stereo Audio Jack J40 top port and stacked audio jack J41 with head phone circuit.

Port Mapping:

Common Processor board audio ports are mapped as below.

- 3x Standard 3.5mm stacked Stereo Audio Jack Mfr. Part# STX-4235-3/3-N is provided for:
  - 2x – MIC IN, 1x – Line OUT and 3x – Head Phone OUT
- 1x Standard 3.5mm Stereo Audio Jack Mfr. Part# SJ-3524-SMT-TR provided for:
  - 1x – Line IN interface

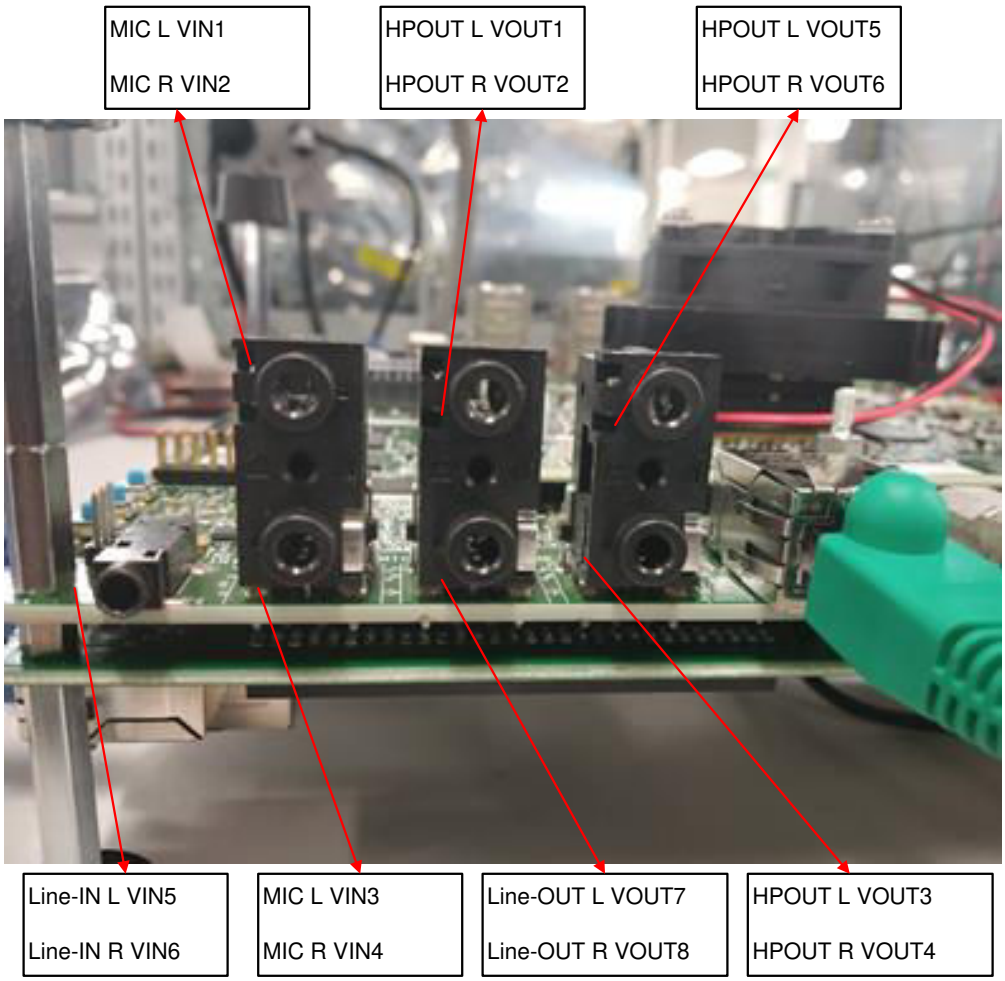


Figure 4-37. Audio Port Interface Assignment

4.18 Display Port Interface

Common Processor Board supports two display port interfaces DP0 and DP1. However, J721E SoC supports only DP0. DP1 shall be available on CP board to support future J7 SoC. Display port is connected to Torrent SERDES (SERDES4) internal to J721E SoC. 4K UHD Display (3840 x 2160) @ 120 Hz (MST- Multi stream support), up to Two 4K UHD Displays (3840 x 2160) @ 60 Hz (MST) can be supported by CP board display port interface. Standard full-size Molex display connector Mfr. Part# 472720001 is used to interface with displays.

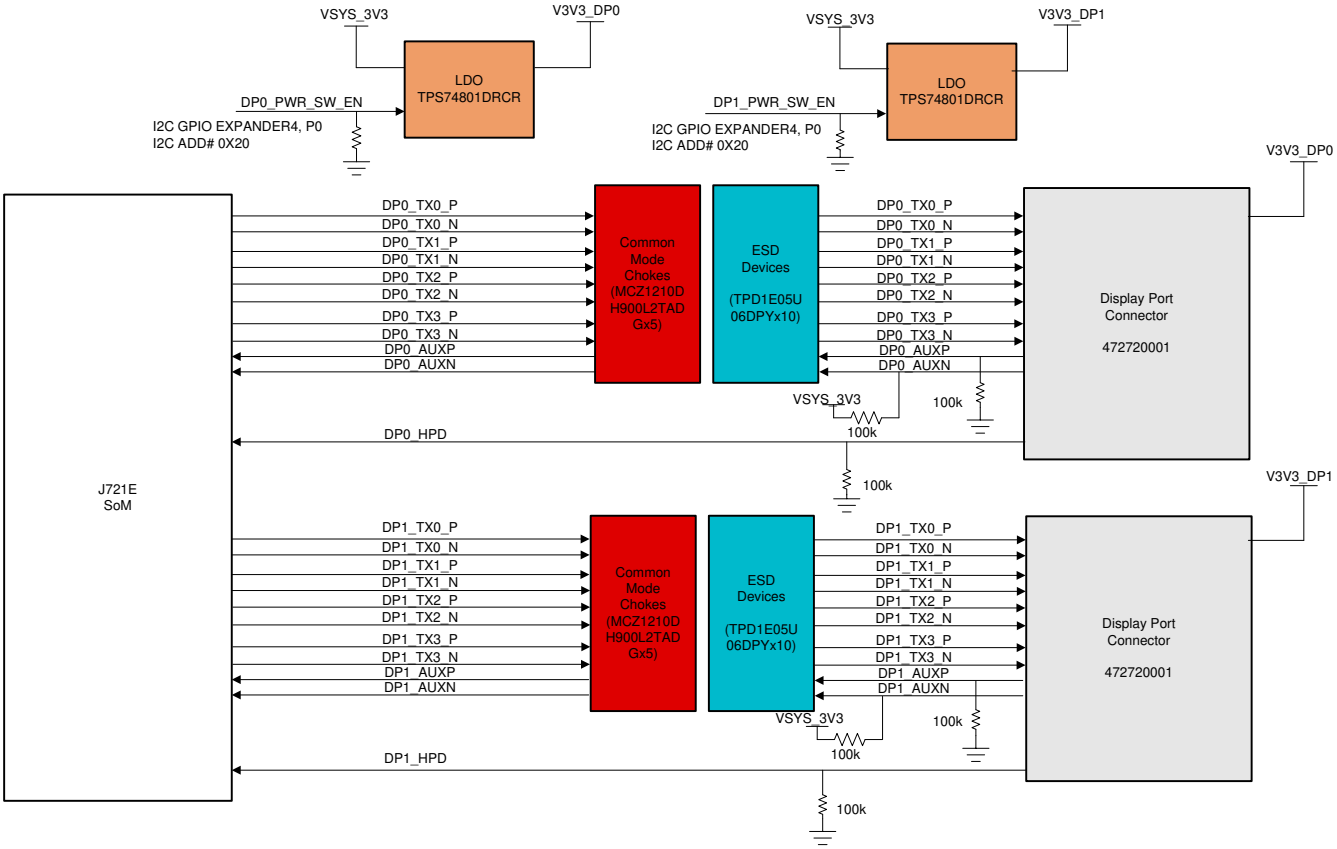


Figure 4-38. Display Port Block Diagram

Separate ESD protection devices of Mfr. Part# TPD1E05U06DPY are used for main and auxiliary data channels and Common mode filters MCZ1210DH900L2TA0G at every differential data and aux pairs. Supply 3.3 V, 500 mA for each connector has been given through individual LDOs Mfr. Part# TPS74801DRCR. The LDO has active high enable input and is disabled by default. Driving high from GPIO from I/O Expander4 (I2C ADD# 0x20) Port0 and Port1 will enable the supplies to Display Port connectors.

4.19 MLB Interface

Common Processor board supports for Media Local Bus (MLB) interface.

Differential pairs of MLB signals from J721E SoC are routed to Samtec header Mfr. Part# QSH-020-01-L-D-DP-A-K. This interfaces is designed to mate with MicroChip's MLB Physical interface board. The differential signals are routed with a characteristic impedance of 100E and also a Pull up and Pull-down option is provided for the N and P signals respectively. The reset signal that comes from the expander (I2C ADD# 0x22, I2C0) is availed with a pull down to avoid floating, and the interrupt signal is equipped with a pull up and routed to J721E SoM.

The 12 V and 3.3 V are drawn from the CP board to the connector; the I2C control is provided to the MLB Header from I2C0 port of J721E SoC.

Figure 4-39. MLB Interface Connector

Table 4-23 lists the pinout for MLB Header J22 (QSH-020-01-L-D-DP-A).

Table 4-23. MLB Header Pinout

Pin No	Signal	Pin No	Signal
1	MLB0_MLBSIG_N	2	H_MLB0_MLBCLK
3	MLB0_MLBSIG_P	4	NC
5	NC	6	H_MLB0_MLBSIG
7	NC	8	NC
9	MLB0_MLBDAT_N	10	H_MLB0_MLBDAT
11	MLB0_MLBDAT_P	12	NC
13	NC	14	NC
15	NC	16	H_MLB0_REFCLK
17	MLB0_MLBCLK_N	18	NC
19	MLB0_MLBCLK_P	20	NC
21	DGND	22	DGND
23	NC	24	MLB0_GPIO0
25	MLB_RSTz	26	NC
27	NC	28	NC
29	NC	30	NC
31	NC	32	NC
33	I2C0_SCL	34	MLB_INT#
35	I2C0_SDA	36	NC
37	VSYS_IO_3V3	38	VSYS_IO_3V3
39	VSYS_IO_3V3	40	VCC_12V0

4.20 I3C Interface

Common Processor board supports two I3C headers to validate the J721E SoC's MCU and MAIN domain I3C interfaces. Out of Two I3C headers, only the MCU I3C header J33 is populated on J721E EVM and the MAIN I3C header J32 is not populated by default. MCU_I3C0_SDA is pulled through 1K Resistor by signal MCU_I3C0_SDAPULLEN from SoC.

MAIN_I3C0_SCL and MAIN_I3C0_SDA are terminated to the I3C header using 2:1 de-muxer IC U46 on Common Processor board. The signal path is disconnected by default using resistors R192 and R193.

The mux selection is controlled by I2C GPIO Expander2 (I2C ADD# 0x22, I2C0) Port16.

Table 4-24 and Table 4-25 lists the I3C Header pinouts.

Table 4-24. MCU I3C Header J33 Pinout

Pin No	Signal
1	DGND
2	MCU_I3C0_SDA
3	MCU_I3C0_SCL

Table 4-25. MAIN I3C Header J32 Pinout

Pin No	Signal
1	DGND
2	MCU_I3C0_SDA
3	MCU_I3C0_SCL

4.21 ADC Interface

MCU ADC0 port of J721E SoC is interfaced to 2x10 header Mfr. Part# TSW-110-07-S-D on Common Processor board. The ADC inputs MCU_ADC0_AIN[7:0] and external Trigger input MCU_ADC_EXT_TRIGGER0 is connected to J721E SoC through SoM board. MCU_ADC0_REF_P and MCU_ADC0_REF_N are not routed to J721E SoC as these signals are tied internally in SoC package.

Note

MCU ADC1 port of J721E SoC is supported on EVM application board (GESI).

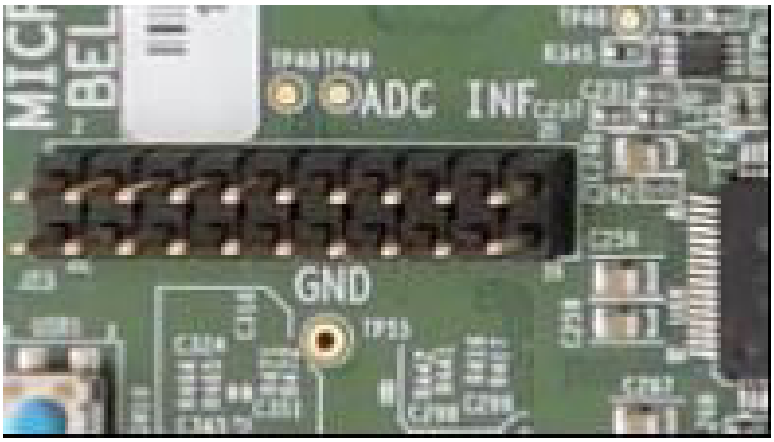


Figure 4-40. ADC Interface Connector

Table 4-26. ADC Header J23 Pinout

Pin No	Signal	Pin No	Signal
1	DGND	2	MCU_ADC0_AIN3
3	MCU_ADC0_AIN7	4	MCU_ADC0_AIN0
5	MCU_ADC0_AIN1	6	MCU_ADC0_AIN6
7	DGND	8	DGND
9	MCU_ADC0_AIN4	10	MCU_ADC0_REF_P
11	MCU_ADC0_AIN2	12	MCU_ADC0_REF_N
13	DGND	14	DGND
15	MCU_ADC0_AIN5	16	MCU_ADC_EXT_TRIGGER0
17	NC	18	NC
19	DGND	20	DGND

4.22 RTC Interface

A real-time clock module Mfr. Part# MCP79410-I/SN is connected I2C0 interface of J721E SoC.

RTC device is being powered by 3.3 V and a battery holder BC501SM is connected to VBAT pin for external battery power option (battery not provided). A 32.768 kHz quartz crystal is used to provide clock for the device.

MFP pin of RTC module is used to generate optional reference clock to the SoC's WKUP_LFOSC.

7-bit I2C addresses are 0x57 and 0x6F.

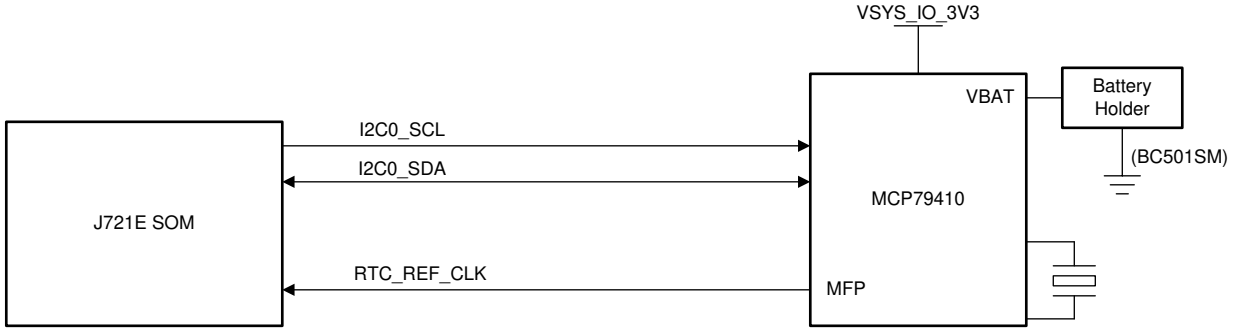


Figure 4-41. RTC Block Diagram

4.23 Apple Authentication Header

The common processor board has a provision to support Apple authentication interface. In the J721E EVM, the Apple authentication board can be interfaced with J721E SoC in two options: one is module interface and the other is device interface.

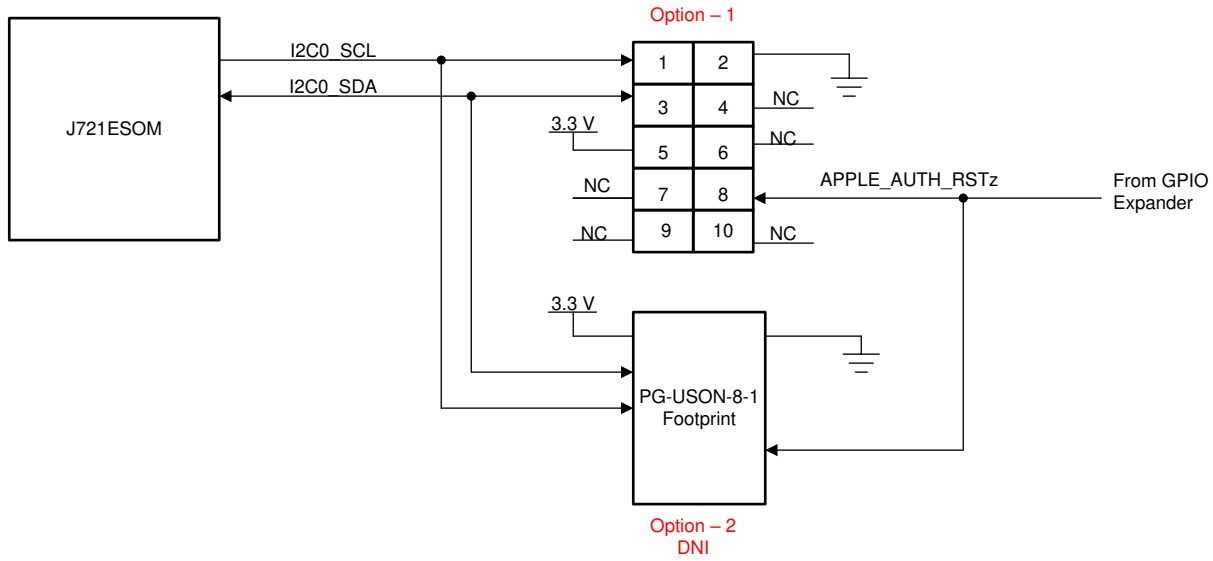


Figure 4-42. Apple Authentication Block Diagram

Module Interface:

Common Processor board have a 2.54 mm Dual row 10 Pin Receptacle Mfr. Part# 2214BR-10G.

I2C0 Port of J721E SoC and Reset from GPIO Expander is terminated to this connector. 3.3 V supply is provided to the connector J9.

Table 4-27 lists detailed signal and pin descriptions.

Table 4-27. APPLE AUTH Header J9 Pinout

Pin No	Signal	Description
1	I2C0_SCL	I2C slave interface, clock connection
3	I2C0_SDA	I2C slave interface, data connection
8	APPLE_AUTH_RSTz	Reset, Active low
5	VSYS_IO_3V3	Power 3.3 V
2	DGND	Ground
4,6,7,9,10	NC	Not Connected

Device Interface:
In this approach Common Processor PCB have a footprint PG-USON-8-1. Apple authentication device will not be assembled to this footprint by default.

Required I2C0, Power, Reset and Ground signals from J721E SoC is routed to this footprint, as shown in Table 4-28.

Table 4-28. APPLE AUTH Footprint U108 Pinout

Pin No	Signal	Description
6	I2C0_SCL	I2C slave interface, clock connection
2	I2C0_SDA	I2C slave interface, data connection
7	APPLE_AUTH_RSTz	Reset, Active low
8	VSYS_IO_3V3	Power 3.3 V
1, 9	DGND	Ground
3,4,5	NC	Not Connected

4.24 EVM Expansion Connectors

The Common processor board includes an Expansion connector of QSH-060-01-L-D-A-K with 5mm mating height allowing multiple expansion boards (Infotainment or GESI Expansion) to be stacked below the processor board.

Either Infotainment or GESI Expansion board can be plugged into EVM expansion connectors (J46 and J51) at once.

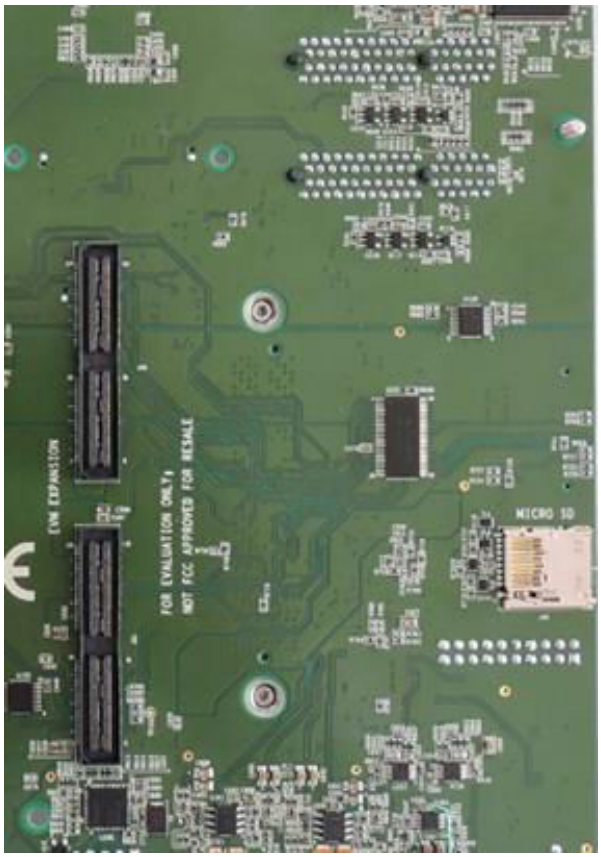


Figure 4-43. Expansion Board Interface Connectors

Table 4-29 and Table 4-30 lists the EVM expansion connectors pinouts.

Table 4-29. EVM Expansion Connector J46 Pinout

INFO/GESI Connector Interface J46			
Pin No	**Signal**	**Pin No**	**Signal**
1	DGND	2	VCC_12V0
3	DGND	4	VCC_12V0
5	DGND	6	VCC_12V0
7	MCASP1_AXR3/PRG0_RGMII2_RXC	8	VOUT0_DATA15/PRG1_RGMII2_TX_CTL
9	PRG0_RGMII2_RD3	10	VOUT0_DATA14/PRG1_RGMII2_TD3
11	MCASP1_AXR2/PRG0_RGMII2_RX_CTL	12	VOUT0_HSYNC/PRG1_RGMII2_TXC
13	MCASP1_AXR0/PRG0_RGMII2_RD0	14	VOUT0_DATA11/PRG1_RGMII2_TD0
15	MCASP1_AXR1/PRG0_RGMII2_RD1	16	VOUT0_DATA13/PRG1_RGMII2_TD2
17	PRG0_RGMII2_RD2	18	VOUT0_DATA12/PRG1_RGMII2_TD1
19	DGND	20	DGND
21	VOUT0_EXTPCLKIN/MCAN6_TX	22	VPFE0_DATA6/MCAN5_TX
23	VOUT0_DATA5/MCAN6_RX	24	VPFE0_DATA7/MCAN5_RX
25	VOUT0_DATA7/MCAN7_TX	26	AUDIO_EXT_REFCLK1/MCAN4_TX
27	VOUT0_DATA8/MCAN7_RX	28	VOUT0_DATA22/MCAN4_RX
29	VOUT0_DATA9/PRG1_UART0_RXD	30	PRG1_UART0_RTS#
31	VOUT0_DATA10/PRG1_UART0_TXD	32	VOUT0_DATA23/SPI6_CS1
33	VOUT0_VSYNC/SPI6_D0	34	VOUT0_DE/SPI6_CLK
35	NC	36	VOUT0_PCLK/SPI6_D1
37	DGND	38	DGND
39	VOUT0_DATA0/PRG1_RGMII2_RD0	40	VOUT0_DATA19/PRG1_RGMII1_TD3
41	VOUT0_DATA2/PRG1_RGMII2_RD2	42	VOUT0_DATA16/PRG1_RGMII1_TD0
43	VOUT0_DATA1/PRG1_RGMII2_RD1	44	VOUT0_DATA20/PRG1_RGMII1_TX_CTL
45	VOUT0_DATA3/PRG1_RGMII2_RD3	46	VOUT0_DATA18/PRG1_RGMII1_TD2
47	VOUT0_DATA4/PRG1_RGMII2_RX_CTL	48	VOUT0_DATA21/PRG1_RGMII1_TXC
49	VOUT0_DATA6/PRG1_RGMII2_RXC	50	VOUT0_DATA17/PRG1_RGMII1_TD1
51	DGND	52	DGND
53	MCASP0_AXR5/MCAN9_TX	54	VPFE0_DATA12/PRG1_MDIO0_MDC
55	MCASP0_AXR6/MCAN9_RX	56	VPFE0_DATA11/PRG1_MDIO0_MDIO
57	MCASP0_ACLKX/SPI3_CS1	58	SPI3_CS0
59	MCASP0_AFSX/SPI3_CS2	60	MCASP1_AFSX/MCAN11_RX
61	McASP0_AXR3	62	NC
63	WKUP_I2C0_SDA	64	SOC_PORZ_OUT
65	WKUP_I2C0_SCL	66	PRG0_PWM0_TZ_OUT
67	DGND	68	DGND
69	MCASP0_AXR0/PRG0_RGMII1_RD0	70	MCASP0_AXR8/PRG0_RGMII1_TD1
71	MCASP0_AXR2/PRG0_RGMII1_RX_CTL	72	MCASP0_AXR7/PRG0_RGMII1_TD0
73	MCASP0_AXR4/PRG0_RGMII1_RXC	74	MCASP0_AXR11/PRG0_RGMII1_TX_CTL
75	PRG0_RGMII1_RD2	76	MCASP0_AXR10/PRG0_RGMII1_TD3
77	MCASP0_AXR1/PRG0_RGMII1_RD1	78	MCASP0_AXR9/PRG0_RGMII1_TD2
79	PRG0_RGMII1_RD3	80	MCASP0_AXR12/PRG0_RGMII1_TXC
81	DGND	82	DGND
83	MCASP1_AXR8/PRG0_RGMII2_TD1	84	MCASP6_ACLKX/PRG1_RGMII1_RD0
85	MCASP1_AXR7/PRG0_RGMII2_TD0	86	MCASP6_AFSR/PRG1_RGMII1_RXC
87	GPIO0_79/PRG0_RGMII2_TXC	88	MCASP6_AFSX/PRG1_RGMII1_RD1

Table 4-29. EVM Expansion Connector J46 Pinout (continued)

INFO/GESI Connector Interface J46			
Pin No	**Signal**	**Pin No**	**Signal**
89	PRG0_RGMII2_TD2	90	PRG1_RGMII1_RD3
91	PRG0_RGMII2_TX_CTL	92	MCASP6_ACLKR/PRG1_RGMII1_RX_CTL
93	MCASP2_AXR0/PRG0_RGMII2_TD3	94	MCASP6_AXR0/PRG1_RGMII1_RD2
95	DGND	96	DGND
97	MDIO0_MDC	98	PRG0_MDIO0_MDC/I2C5_SDA
99	MDIO0_MDIO	100	PRG0_MDIO0_MDIO/I2C5_SCL
101	SPI3_D0	102	MCASP0_AXR13/PRG0_PWM0_B2
103	SPI3_D1	104	NC
105	SPI3_CLK	106	RGMII_REFCLK
107	DGND	108	DGND
109	I2C0_SCL	110	MCASP1_ACLKX
111	I2C0_SDA	112	SOC_I2C2_SCL
113	I2C1_SCL	114	SOC_I2C2_SDA
115	I2C1_SDA	116	NC
117	NC	118	EXP_RSTz
119	DGND	120	DGND

Table 4-30. EVM Expansion Connector J51 Pinout

INFO/GESI Connector Interface J51			
Pin No	**Signal**	**Pin No**	**Signal**
1	DGND	2	EXP_3V3
3	DGND	4	EXP_3V3
5	DGND	6	EXP_3V3
7	MCASP1_AXR5/UART8_RXD	8	I2C3_SCL
9	MCASP1_AXR6/UART8_TXD	10	I2C3_SDA
11	EQEP0_A	12	EQEP0_I
13	EQEP0_B	14	EQEP0_S
15	GPIO1_23/UART9_RXD	16	EXP_CODEC_SCKI
17	GPIO1_24/UART9_TXD	18	NC
19	EXP_EEPROM_A0	20	INFO_CAM_VIO_SEL
21	EXP_EEPROM_A1	22	EXP_REFCLK
23	EXP_EEPROM_A2	24	NC
25	BOARDID_EEPROM_WP	26	PRG1_IEP0_EDIO_OUTVALID
27	GPIO0_6	28	PERIPH_RSTz
29	GPIO0_61	30	RESETSTATz
31	UB926_GPIO2	32	EXP_MUX1
33	UB926_GPIO3	34	EXP_MUX2
35	NC	36	EXP_MUX3
37	NC	38	NC
39	DGND	40	DGND
41	GPMC0_A1	42	GPMC0_A22
43	GPMC0_A2	44	GPMC0_DIR
45	GPMC0_A3	46	GPMC0_A17
47	GPMC0_A4	48	GPMC0_BE1#
49	GPMC0_A5	50	GPMC0_A16
51	GPMC0_A7	52	GPMC0_A21
53	GPMC0_A6	54	GPMC0_A15
55	GPMC0_A9	56	GPMC0_A20
57	GPMC0_A11	58	GPMC0_A14
59	GPMC0_A8	60	GPMC0_A18
61	GPMC0_A10	62	GPMC0_A19
63	GPMC0_A12	64	GPMC0_A13
65	NC	66	NC
67	DGND	68	DGND
69	NC	70	NC
71	NC	72	NC
73	NC	74	NC
75	NC	76	NC
77	DGND	78	VSYS_5V0
79	DGND	80	VSYS_5V0
81	DGND	82	VSYS_5V0
83	MCU_ADC1_AIN0	84	NC
85	MCU_ADC1_AIN1	86	NC
87	MCU_ADC1_AIN2	88	NC
89	MCU_ADC1_AIN3	90	NC
91	MCU_ADC1_AIN4	92	NC

Table 4-30. EVM Expansion Connector J51 Pinout (continued)

INFO/GESI Connector Interface J51			
Pin No	**Signal**	**Pin No**	**Signal**
93	MCU_ADC1_AIN5	94	NC
95	MCU_ADC1_AIN6	96	NC
97	MCU_ADC1_AIN7	98	NC
99	NC	100	VSYS_IO_3V3
101	NC	102	VSYS_IO_3V3
103	MCU_ADC_EXT_TRIGGER1	104	VSYS_IO_3V3
105	DGND	106	NC
107	I2C6_SCL	108	NC
109	I2C6_SDA	110	NC
111	NC	112	NC
113	USB1_DN4_PE	114	VSYS_IO_1V8
115	USB1_DN4_D_N	116	VSYS_IO_1V8
117	USB1_DN4_D_P	118	VSYS_IO_1V8
119	DGND	120	DGND

4.25 ENET Expansion Connector

The Common processor board includes an Expansion connector of 171446-1109 with 5 mm mating height allowing ENET expansion board (Quad-Port Ethernet Expansion) to be stacked on Top side of the processor board.

This section provides an overview of the different interfaces and circuits on the Quad port Ethernet Expansion Board.

4.25.1 Power Requirements

The Expansion Card utilizes power from Common processor board through expansion connector and it has two Low Drop Out circuits to supply Quad Port SGMII PHY with the necessary voltage and the power required.

Test points for each power outputs are provided on the Ethernet Expansion card and are mentioned in Table 4-31.

Table 4-31. ENET Expansion Board Power Test Points

Sl No	Power Supply	Test Point	Voltage	Tolerance
Card Top Side				
1	VCC_12V0	C30.1	12 V	
2	VSYS_5V0	C34.1	5 V	
3	VCC_3V3	C33.1	3.3 V	
4	VCC_2V5	TP2	2.5 V	
5	VCC_1V	TP10	1 V	

4.25.2 Clock

4.25.2.1 Main Clock

The Reference clock to the PHY is generated from TI's Clock Generator Mfr. Part Number# CDCI6214RGET that is placed on the Common Processor (CPU) Board. Clock inputs shall be AC coupled and LVDS compliant. The clock generator can be configured by I2C0 of the J721E SoC. The I2C address of this clock generator is 0x77.

4.25.2.2 Optional Clock

Optionally, the reference clock can be supplied by the SERDES clock generator Mfr. Part Number# CDCI6214RGET, located on Quad port Ethernet Expansion Board, which can be configured by I2C0 of the J721E SOC. The I2C address of this clock generator is 0x77 and this address conflicts with CDCI Chip on Common processor Board. An I2C switch on Quad port Ethernet Expansion Board is used to remove the address conflict by either connecting any one of the clock generators.

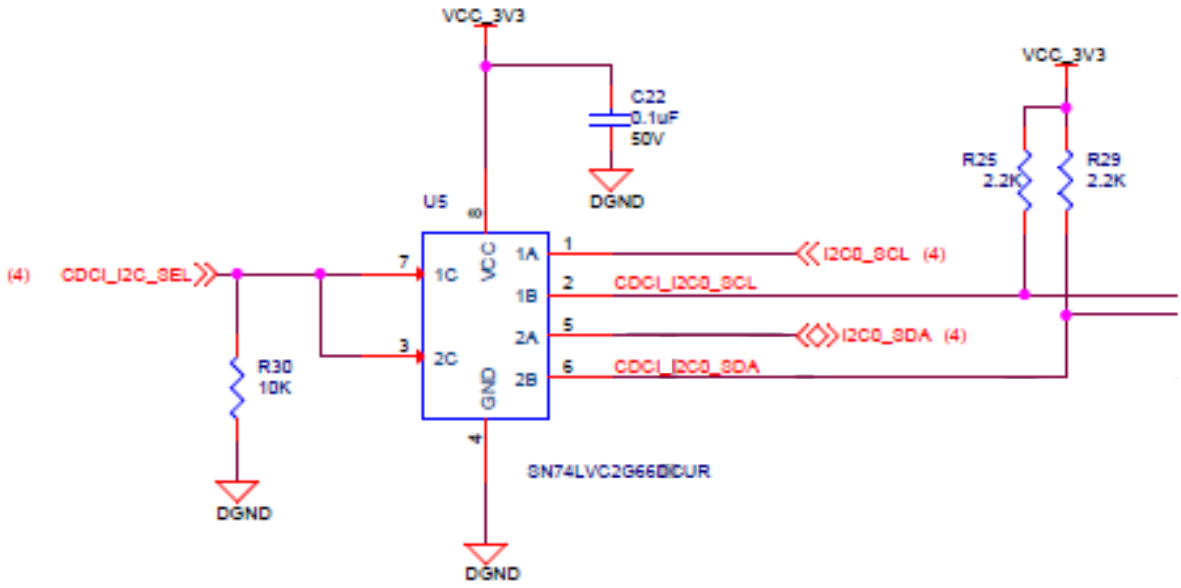


Figure 4-44. CDCI I2C Isolation Circuit

Set the CDCI_I2C_SEL I/O EXP bit high to connect the I2C bus to the CDCI for programming on the Quad Port Ethernet Expansion Board. During this time, the CDCI device U17 on the Common Processor board should be in reset mode.

4.25.3 Reset Signals

QSGMII_RESETz is a reset signal sourced from Common Processor board. This signal is used to reset the QSGMII PHY on the board.

QSGMII_RESETz is an AND output of SOC_PORz_out and ENET_EXP_RSTz . The ENET_EXP_RSTz signal is asserted by an I2C GPIO Expander2 (I2C ADD# 0x22, I2C0) Port21 in the common processor board.

Table 4-32 lists the ENET expansion connector pinouts.

Table 4-32. ENET Expansion Connector J10 Pinout

ENET Expansion connector Interface J10	
Pin No	**Signal**
1	DGND
2	NC
3	NC
4	DGND
5	NC
6	NC
7	DGND
8	NC
9	NC
10	DGND
11	VSYS_IO_3V3
12	VSYS_IO_3V3
13	DGND
14	EEPROM_A0
15	EEPROM_A1
16	EEPROM_A2
17	DGND
18	EEPROM_WP
19	REFCLK_25MHZ
20	DGND
21	WKUP_I2C0_SCL
22	WKUP_I2C0_SDA
23	DGND
24	I2C0_SCL
25	I2C0_SDA
26	DGND
27	VCC_12V0
28	VCC_12V0
29	DGND
30	ENET_EXP_PWRDN
31	QSGMII_INTN
32	DGND
33	QSGMII4_TX_P
34	QSGMII4_TX_N
35	DGND
36	QSGMII4_RX_P
37	QSGMII4_RX_N
38	DGND

Table 4-32. ENET Expansion Connector J10 Pinout (continued)

ENET Expansion connector Interface J10	
Pin No	**Signal**
39	QSGMII_PHY_REFCLK_N
40	QSGMII_PHY_REFCLK_P
41	DGND
42	QSGMII_MDC
43	QSGMII_MDIO
44	DGND
45	QSGMII_RESETN
46	CDCI_I2C_SEL
47	ENET_EXP_SPARE
48	DGND
49	VSYS_5V0
50	VSYS_5V0
51	DGND
52	NC
53	NC
54	DGND
55	VCC_3V3
56	VCC_3V3
57	DGND
58	NC
59	NC
60	DGND
SH1	DGND
SH2	DGND

4.25.4 Ethernet Interface

The J721E EVM includes SGMII connection between VSC8514XMK Quad Port SGMII PHY and the network subsystem (NSS) of the Processor. One channel of SGMII interface (connected to stacked RJ45 connector J1A and J1B, J2A and J2B) from the SERDES domain of J721E processor are used.

4.25.4.1 Quad Port SGMII PHY Default Configuration

The J721E EVM uses the 138-pin QFN package, designated with the XMK suffix that supports only the SGMII interface.

The VC8514 device includes three external PHY address pins, PHYADD [4:2] to allow control of multiple PHY devices on a system board sharing a common management bus. These pins set the most significant bits of the PHY address port map. The lower two bits of the address for each port are derived from the physical address of the port (0 to 3) and the setting of the PHY address reversal bit in register 20E1, bit 9.

4.25.5 Board ID EEPROM Interface

The Quad port Ethernet Expansion Board is identified by its version and serial number, which are stored in the onboard EEPROM. The EEPROM is accessible on the address 0x54.

The first 259 bytes of addressable EEPROM memory are preprogrammed with identification information for each board. The remaining 32509 bytes are available to the user for data or code storage.

4.26 CSI Expansion Connector

The J721E EVM supports different application specific camera expansion boards, which includes:

- Fusion1 Serial Capture Expansion
- Fusion2 Serial Capture Expansion

Common processor board supports to interface with these CSI expansion boards using connector of QSH-020-01-L-D-DP-A-K with 5 mm mating height allowing CSI Expansion to be stacked on bottom side of the processor board.

Camera Serial Interface CSI0 and CSI1 of J721E SoC is interfaced to this CSI expansion connector J52 on the CP board. The Common Processor board supports the Auxiliary CSI expansion connector that is reserved for CSI2 port of future J7 SoC.

Power (12 V and 3.3 V), control GPIOs and reference clock to these CSI expansion boards are provided from Common Processor board through CSI expansion connector. Optionally auxiliary 12 V can be supplied from Common Processor board via terminal block (1757242) using external wire.

The I/O supply to these CSI expansion boards can be configured for both 3.3 V and 1.8 V using the DIP Switch SW3 Position 7.

CSI_VIO_SEL	Sets I/O voltage for CSI2 Expansion Interface (LVCMOS signals) '0' (OFF) = 1.8 V I/O Voltage '1' (ON) = 3.3 V I/O Voltage

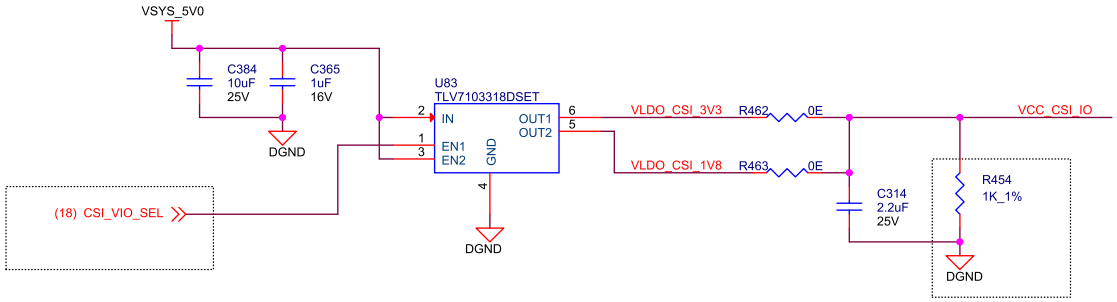


Figure 4-45. Dual I/O Voltage Selection for CSI Expansion Interface

Table 4-33 and Table 4-34 lists the CSI expansion connector pinouts.

Table 4-33. CSI Expansion Connector J52 Pinout

CSI2 Connector Interface J52			
Pin No	**Signal**	**Pin No**	**Signal**
1	VCC_12V0	21	CSI0_RX3_P
2	CSI2_I2C_SCL_DV	22	CSI2_A_GPIO4_DV
3	VCC_12V0	23	CSI0_RX3_N
4	CSI2_I2C_SDA_DV	24	DGND
5	CSI0_RXCLK_P	25	CSI1_RXCLK_P
6	CSI2_A_GPIO0_DV	26	CSI1_RX3_P
7	CSI0_RXCLK_N	27	CSI1_RXCLK_N
8	CSI2_A_GPIO1_DV	28	CSI1_RX3_N
9	CSI0_RX0_P	29	CSI1_RX0_P
10	CSI2_A_REFCLK_DV	30	EXP_3V3
11	CSI0_RX0_N	31	CSI1_RX0_N
12	DGND	32	EXP_3V3
13	CSI0_RX1_P	33	CSI1_RX1_P
14	CSI2_RSTZ_DV	34	EXP_3V3
15	CSI0_RX1_N	35	CSI1_RX1_N
16	DGND	36	EXP_3V3
17	CSI0_RX2_P	37	CSI1_RX2_P
18	CSI2_A_GPIO2_DV	38	VCC_CSI_IO
19	CSI0_RX2_N	39	CSI1_RX2_N
20	CSI2_A_GPIO3_DV	40	VCC_CSI_IO

Table 4-34. CSI Expansion Connector J48 Pinout

CSI2 Connector Interface J48			
Pin No	**Signal**	**Pin No**	**Signal**
1	VCC_12V0	21	CSI2_RX3_P
2	CSI2_I2C_SCL_DV	22	CSI2_B_GPIO4_DV
3	VCC_12V0	23	CSI2_RX3_N
4	CSI2_I2C_SDA_DV	24	DGND
5	CSI2_RXCLK_P	25	NC
6	NC	26	NC
7	CSI2_RXCLK_N	27	NC
8	CSI2_B_GPIO1_DV	28	NC
9	CSI2_RX0_P	29	NC
10	CSI2_B_REFCLK_DV	30	EXP_3V3
11	CSI2_RX0_N	31	NC
12	DGND	32	EXP_3V3
13	CSI2_RX1_P	33	NC
14	CSI2_RSTZ_DV	34	EXP_3V3
15	CSI2_RX1_N	35	NC
16	DGND	36	EXP_3V3
17	CSI2_RX2_P	37	NC
18	CSI2_B_GPIO2_DV	38	VCC_CSI_IO
19	CSI2_RX2_N	39	NC
20	CSI2_B_GPIO3_DV	40	VCC_CSI_IO

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2022) to Revision E (January 2024)	Page
• Updated Section 3.5	22

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