# AM335x ICE EVM Rev2.1 Hardware User's Guide

# User's Guide


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# AM335x ICE EVM Rev2.1 Hardware User's Guide

## 1 Introduction

This document provides the design information on the AM335x processor based ICE EVM (TMDSICE3359) to the users. ICE stands for Industrial Communications Engine. This EVM can be used to evaluate industrial communication protocols based on AM335x.

### 1.1 Description

The low-cost ICE EVM can be used for evaluation and development of industrial communication-type applications. It has been equipped with a TI AM3359 processor and a defined set of features to let the user experience specific industrial communication solutions using serial or Ethernet-based interfaces. It is not intended as a generic development platform, as some of the features and interfaces supplied by the AM335x are not accessible from the ICE board. Using standard interfaces, the ICE board may interface to other processors or systems and act as a communication gateway. In addition, it can directly operate as a standard remote I/O system or simple sensor connected to an industrial communication network. The embedded emulation logic allows emulation and debug using standard development tools, such as TI's Code Composer Studio, by using the supplied USB cable.

It is not intended for use in end products. All of the design information is freely available and can be used as the basis for the development of an AM335x-based product.

### 1.2 EVM System View

The ICE EVM board has dimensions of 3.09" × 4.10 "". The Top Side and the Iso views of the AM335x ICE 2.0 EVM are shown in Figure 1, Figure 2, and Figure 3.

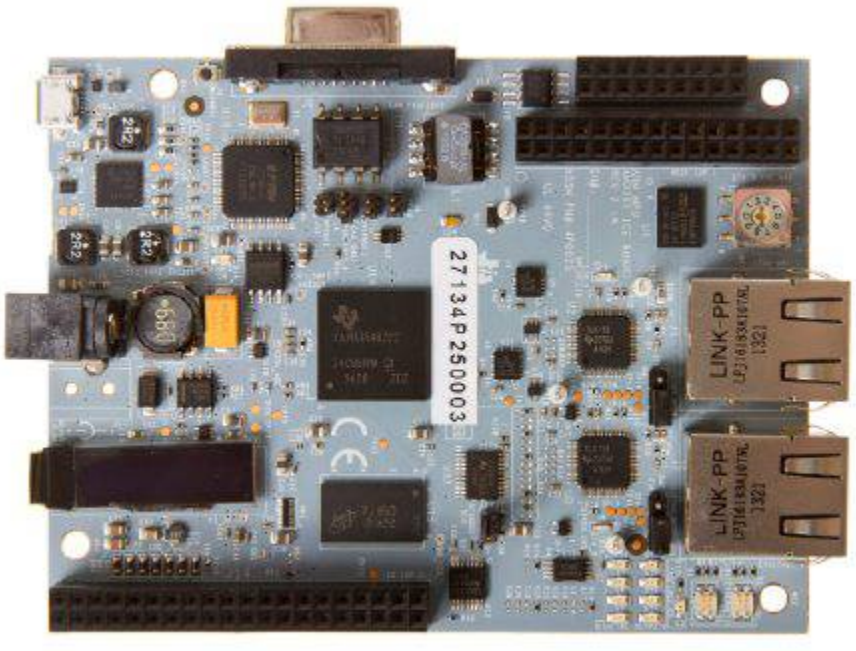


**Figure 1. AM3359 ICE 2.1 EVM Top View**

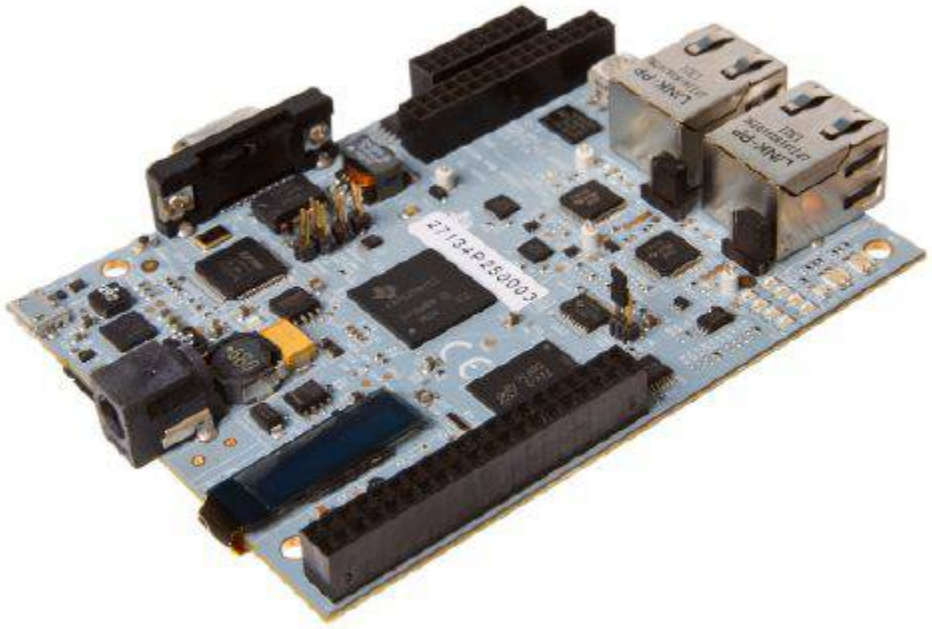

**Figure 2. AM3359 ICE 2.1 EVM Iso View**

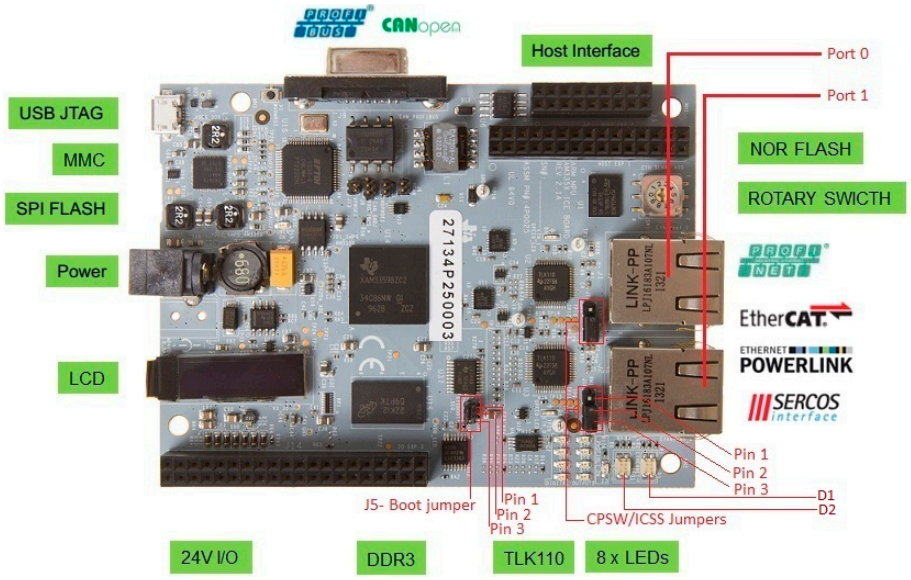


**Figure 3. AM3359 ICE 2.1 EVM Connector and Jumper Loactions**

## 1.3 Schematics and Design Files

Go here for schematics, design files, and other related hardware documentation.

# 2 Functional Blocks Description of the AM335x ICE 2.0 EVM

This section describes the major functional blocks of the AM335x ICE V2.0 EVM system. The functional block diagram of the AM335x ICE 2.0 EVM is shown in Figure 4.

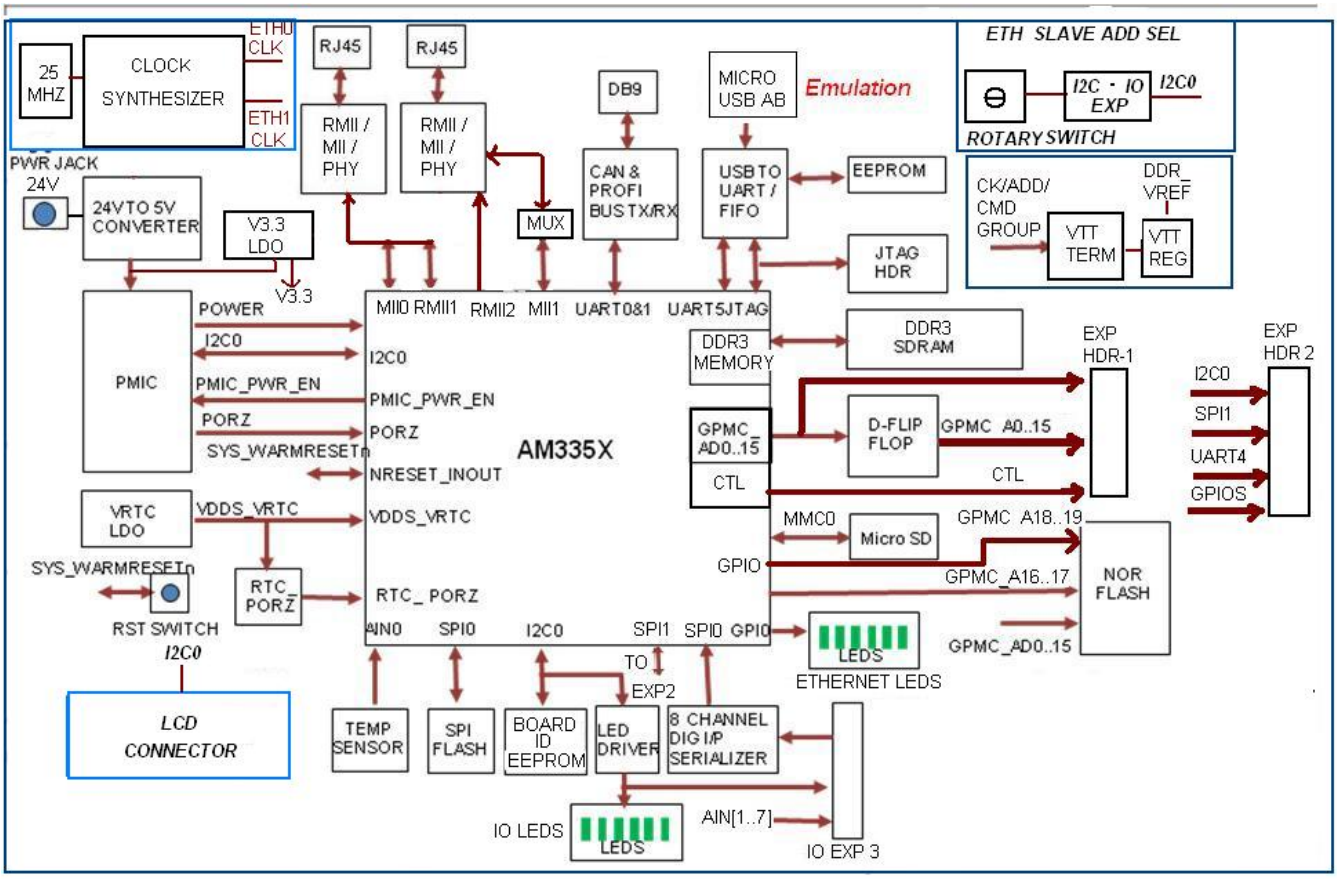


**Figure 4. AM335x ICE Rev. 2.1 EVM Block Diagram**

## 2.1 Processor

The AM3359ZCZ processor is the central processor for this EVM. All the resources on the board surround the AM3359 processor, to provide development capabilities for hardware and software. See the AM3359 data sheet and Technical Reference Manual for the details about the processor.

There are system configuration signals, SYSBOOT, that can be set on the EVM to define some startup parameters on the AM335x processor. See Section 4 for more details.

## 2.2 Clocks

The main clock for the processor is derived from a 24-MHz crystal. An on-board oscillator in the AM3359 generates the base clock and subsequent module clocks as needed within the AM3359 processor. A 32-kHz clock for the RTC section on the AM3359 processor is derived from a 32-kHz crystal on board.

## 2.3 Reset Signals

SYS_RESETn is a signal running to several peripherals and the AM335x which performs a reset on those peripherals. SYS_WARMRESETn is asserted by a pushbutton on the board and used to force a reset of the AM3359. The AM3359 can also pulldown on the RESET_INOUTn signal to cause the SYS_RESETn line to go active. The RTC_PORZ reset signal for the RTC section is derived from an RC delay of the main power supply through the VRTC power rail. An AND gate sharpens the edge to meet the AM3359 requirements.

# 3 Power

The DC power input to the board is from a 24-V DC power supply. The 24-V power input is converted into 5 V to provide power input to the Power Manager TPS65910. The power requirements of the processor are taken care of by the Power Manager IC TPS65910A3. The Power ON LED "D16" is ON if the PMIC is active. The power on sequencing requirements of the AM3359 processor (see the AM3359 data sheet) are handled automatically by the TPS65910A3 PMIC.

**NOTE:** When powering the TMDSICE3359 EVM, always use the recommended power supply (CUI/V-Infinity Part Number EMSA240075) or equivalent model having output voltage of +24 VDC and output current max 0.75 Amps, and that complies with applicable regional safety standards such as (by example) UL, CSA, VDE, CCC, PSE, and so forth. A power supply is not included with the kit.

## *3.1 Power Management IC*

The AM3359 ICE Rev. 2.1 EVM uses the TPS65910A3 power management IC. The I2C0 on the AM335x is used to control the TPS65910A3 PMIC. For the AM335x, the power supplies from the TPS65910A (listed in Table 1) are used.

**Table 1. AM3359 Power Supplies From TPS65910A**

| TPS65910A3 Power Supply | AM335x Power Rail | Voltage |
|---|---|---|
| VAUX2 | VDDSHV1,3,5,6 | 3.3 V (rails that are 3.3 V) |
| VMMC | VDDSHV4 & VDDSHV2 | 3.3 V |
| VDD2 SMPS | VDD_CORE | 1.1 V |
| VDD1 SMPS | VDD_MPU | 1.1 V |
| No supply needed | VDD_RTC | 1.1 V |
| VRTC | VDDS_RTC | 1.8 V |
| VIO_SMPS | VDDS_DDR | 1.8 V (or 1.5 V for DDR3) |
| VIO_SMPS | DDR_VREF | 0.9 V |
| VDAC | VDDS | 1.8 V |
| VDIG2 | VDDS_SRAM_CORE_BG | 1.8 V |
| VDIG2 | VDDS_SRAM_MPU_BB | 1.8 V |
| VDIG2 | VDDS_PLL_DDR | 1.8 V |
| VDIG2 | VDDS_PLL_CORE_LCD | 1.8 V |
| VDIG2 | VDDS_PLL_MPU | 1.8 V |
| VDIG2 | VDDS_OSC | 1.8 V |
| VAUX1 | VDDA1P8V_USB0/1 | 1.8 V |
| VAUX33 | VDDA3P3V_USB0/1 | 3.3 V |
| VAUX33 | USB_VBUS0/1 | 3.3 V |
| VPLL | VDDA_ADC | 1.8 V |
| VDD3 SMPS | Not Used | - |
| VIO_SMPS | DDR3 SDRAM | 1.8 V |

# 4 Configuration and Setup

## 4.1 Boot Configuration

Various boot configurations can be set using the pull up / down resistor combinations provided on the SYS_BOOT pins (LCD_DATA[15..0]). Boot configuration pins are latched upon de-assertion of the PORz pin. The device supports SPI , MMC/SD, and NOR boot mode through the ARM ROM bootloader. Boot mode selection is determined by the state of pins on J5.

### 4.1.1 NOR Boot

Pin 1 and 2 shorted on J5.

The ROM bootloader looks for a valid boot image in NOR sector 0 and if found, executes it from there. If there is no valid image in NOR, the SPI bootloader is executed if present. If the SPI bootloader is also not present, the SD card bootloader is executed.

### 4.1.2 SPI Boot

Pin 2 and 3 shorted on J5.

The ROM bootloader looks for a valid image in SPI flash and if found, loads it to IRAM and executes it. Otherwise, the SD card bootloader is executed if present.

### 4.1.3 MMC/SD Boot

Pin 2 and 3 shorted on J5.

The ROM bootloader looks for a file named 'MLO' in the SD card and if found, loads it to IRAM and executes it. The SPI bootloader should not be present in SPI flash (see Section 8.1).

| SYSBOOT(4..0) | AM3359 Boot Sequence |
|---|---|
| 11010 | XIP (MUX2), UART0, SPI0, MMC0 |
| 11000 | SPI0, MMC0, USB0, UART0 |

## 4.2 I2C Port Address Assignments

Information on I2C address assignments are provided in Table 2.

**Table 2. I2C Bus Addresses**

| AM335x ICE Rev. 2.1A EVM Function | AM335x I2C Port | Address |
|---|---|---|
| ID memory | I2C0 | 0x50 |
| AM65910A PMIC Control | I2C0 | 0x2D |
| CDCE913 Clock Synthesizer | I2C0 | 0x65 |
| PCA9536DGKR – I2C to IO Expander for Rotary Switch | I2C0 | 0x41 |
| TPIC2810 | I2C0 | 0x60 |
| LCD Display | I2C0 | 0x3C |

## 4.3 ID Memory Contents

Information on the contents of the ID memory is listed in Table 3.

**Table 3. ID Memory Contents**

| Name | Size (Bytes) | Contents |
|---|---|---|
| Header | 4 | MSB 0xEE3355AA LSB |
| Version | 8 | Name for board in ASCII “A335_ICE” = AM335x ICE Board |
| Version | 4 | Hardware version code for board in ASCII “2.1A” = rev. 02.1A |
| Serial Number | 12 | Serial number of the board. This is a 12 character string which is: WWYY4P25nnnn where: WW = 2 digit week of the year of production YY = 2 digit year of production nnnn = incrementing board number |
| Configuration Option | 32 | Codes to show the configuration setup on this board. Reserved |
| Reserved | 6 | reserved |
| Reserved | 6 | reserved |
| Available | 32696 | Available space for other non-volatile codes/data |

## 4.4 JTAG

The ICE Rev. 2.1 EVM supports embedded XDS100V2 USB emulation through the MicroUSB AB connector. It also has an optional 20-pin TI CJTAG connector to support the emulation. This CJTAG connector is not installed by default.

## 4.5 Memories Supported

The ICE Rev. 2.1 EVM supports on-board memories such as DDR3 SDRAM, SPI Flash, NOR Flash, and Board ID EEPROM. It also supports a microSD card socket.

### 4.5.1 DDR3 SDRAM

The ICE design contains 2 Gbit (128M × 16) of DDR3 SDRAM memory. The part number for the DDR3 SDRAM memory used is MT41J128M16JT-125. The package used is an 84-ball FBGA package. See the AM335x TRM for the memory locations for this memory.

### 4.5.2 SPI Flash

A 64-Mbit, W25Q64 SPI flash is used in this design. SPI flash boot is enabled through this flash. This flash is connected to the SPI0 port of the processor.

### 4.5.3 NOR Flash

A 16-Mbit, M29W160EB NOR parallel flash memory is used in this design. This NOR flash is connected to the GPMC interface of the processor and is connected as a halfword (16-bit) data width only.

### 4.5.4 Board Identity Memory

The board contains a 256Kb serial EEPROM that contains board-specific data which allows the processor to automatically detect which board is connected and the version of that board. Other hardware-specific data can also be stored on this memory device. The part number of the memory device is CAT24C256WI-GT3. See Section 4 for details on the data in this memory.

### 4.5.5 SDMMC0

The SDMMC0 connector is a card socket SCHA5B0200 (J16). This is a standard SD/MMC card type of connector. It is connected to the MMC0 port of the AM335x processor. Check the AM335x data sheet and AM335x TRM for supported card types and densities. The pin assignment is given in Table 4.

**Table 4. SDMMC0 Connector Pin Details**

| Pin No | Memory Card PIN No. |
|---|---|
| uSD#1 | DAT2 |
| uSD#2 | CD/DAT3 |
| uSD #3 | CMD |
| uSD #4 | VCC |
| uSD #5 | CLK |
| uSD #6 | GND |
| uSD #7 | DAT0 |
| uSD #8 | DAT1 |
| uSD #9 | GND |
| uSD #10 | CD |
| uSD #11 | GND_SD |
| uSD #12 | GND_SD |
| uSD #13 | GND_SD |
| uSD #14 | GND_SD |
| uSD #15 | GND_SD |
| uSD #16 | GND_SD |

## 4.6 Ethernet

The ICE Rev. 2.1 EVM has two 10/100 Ethernet transceivers (TLK110) interfaced to connectors J1 and J2 . These Ethernet ports are connected from the gig switch and the PRU-ICSS units of the AM335x to the transceivers through a muxing /ORing logic. The reset for the transceivers are driven by the board system reset SYS_RESETn and a GPIO control. The various protocols supported in the design are SERCOS III, SERCOS III S, ETHERNET / IP, POWERLINK, ETHERCAT, and PROFINET. The signal MUX_MII_CTL1 is used to switch the muxing logic between the Gb switch and the PRUSS unit control of the Ethernet PHYs.

The XI clock input pins of both the PHYs are driven from the clock synthesizer CDCE913 (synthesizer inputs connected to a 25-Mhz crystal). The PHYAD pins are left unconnected for setting the PHY's address on the PRU1_MII0 Ethernet, so it is by default 0x01. The PHYAD pins on the PRU1_MII1 Ethernet are set to 0x03 using a pull-up resistor on the PHYAD1 pin.

Jumpers J18 and J19 must be set to control the Ethernet ports using CPSW (gig switch) or PRU-ICSS mode. For PRU-ICSS mode, connect Pin2 and Pin3. For CPSW mode, connect Pin1 and Pin2. These jumper settings apply in both RTOS and Linux.

**Table 5. Ethernet Jack Pinout**

| Pin No | Signal Name | Description |
|---|---|---|
| 1 | ETHER0_RDP | Ethernet Data Rx Positive |
| 2 | ETHER0_RDN | Ethernet Data Rx Negative |
| 3 | V3_3D_PRUETH0JCK | Power |
| 4 | V3_3D_PRUETH0JCK | Power |
| 5 | ETHER0_TDP | Ethernet Data Tx Positive |
| 6 | ETHER0_TDN | Ethernet Data Tx Negative |
| 7 | NC | No Connect |
| 8 | GND | Ground |
| D1 | LINK LED Power | Power |
| D2 | LINKLED | Link LED Signal |
| D3 | Active LED Power | Power |
| D4 | ACTLED | Active LED Signal |

## 4.7 USB

A Micro USB-AB connector (J13) is connected to the upstream port of the USB to UART converter IC (FT2232L). This is used for USB to JTAG and USB to UART conversion applications. This USB port can also be used for XDS100V2 JTAG emulation.

**Table 6. USB**

| Pin No | Signal Name | Description |
|---|---|---|
| 1 | USB_DC | USB BUS VOLTAGE |
| 2 | USB_DM | USB DATA MINUS |
| 3 | USB_DP | USB DATA PLUS |
| 4 | USB_ID | USB IDENTIFICATION (NC) |
| 5 | DGND | Ground |

## 4.8 CAN / PROFIBUS

The ICE Rev. 2.1 EVM has a DB9 female connector J9 for the PROFI/CAN bus interfaces. The PR1_UART0 port of the AM335x is used for interfacing with the PROFIBUS transceiver ISO1176T, and the DCAN0 port of the AM335x is used for interfacing with the CAN bus transceiver ISO1050. The Profi signals and CAN signals are on different pins of the connector.

**Table 7. CAN/PROFIBUS Connector Pin Details**

| Pin No | Signal Name | Description |
|---|---|---|
| 1 | Reserved | Upgrade Path |
| 2 | CAN_L | Dominant Low |
| 3 | CAN_GND | Ground |
| 4 | Reserved | Upgrade Path |
| 5 | PROFI_GND | PROFIBUS Ground |
| 6 | VPROFI_DB | PROFIBUS voltage |
| 7 | CAN_H | Dominant High |
| 8 | Profi BusB | PROFIBUS B |
| 9 | CAN_V+ | Power, Optional |

### 4.8.1 CAN / PROFIBUS Selection Jumpers

The jumpers J6, J7, J8, and J10 are used to select between the CAN / PROFI bus. Descriptions of the selection is provided in Table 8.

**Table 8. CAN / PROFIBUS Jumpers**

| Jumper | Selection |
|---|---|
| J6 | Pins 1 and 2 Short for CAN bus Voltage select |
| J10 | Pins 1 and 2 Short for PROFIBUS Voltage select |
| J8 | Pins 1 and 2 Short for PROFIBUSA select,Pins 2 & 3 Short for CAN Ground select |
| J7 | Pins 1 and 2 Short for PROFIBUS Ground select |

### 4.9 Industrial Inputs

For industrial 24-V digital inputs, a SN65HVS882 serializer is used to accept standard signals in and allow the AM335x to read them. The serialized output from the serializer is fed to the SPI0 port of the processor.

### 4.10 Ethernet LEDs

The Ethernet protocol LEDs are used to indicate the status of the various protocols supported in the design, such as SERCOS III, SERCOS III S, ETHERNET / IP, POWERLINK, ETHERCAT, and PROFINET.

**Table 9. Tri-Color LED D1 Mapping**

| Protocol | Status | Colour of LED |
|---|---|---|
| 'SERCOS-III S | | RED, GREEN, YELLOW |
| 'ETHERNET/IP | MODULE STATE | RED, GREEN |
| 'POWERLINK | S/E | RED, GREEN |
| 'ETHERCAT | ERROR | RED |
| 'PROFINET | BF | RED |

**Table 10. Tri-Color LED D2 Mapping**

| Protocol | Status | Colour of LED |
|---|---|---|
| 'SERCOS-III SD1 | | RED, GREEN, YELLOW |
| 'ETHERNET/IP | NETWORK | RED, GREEN |
| 'ETHERCAT | RUN | GREEN |
| 'PROFINET | SF | RED |

### 4.11 Industrial Output LEDs

I2C to 8-bit LED driver TPIC2810 is used to drive the eight Industrial output LEDs D6 to D10 AND D12 , D14 and D15. The I2C interface is connected to the I2C0 port of the AM335x processor. By communicating over the I2C bus, these outputs can be set to arbitrary values. The 8 LED driver outputs are also driven to the I/O expansion header. All the LEDs are green in color.

### 4.12 Temperature Sensor

The ICE design has a temperature sensor LM94022 on board which outputs analog ambient temperature data. The output data from the temperature sensor is fed to the analog input pin AIN0 of the processor.

### 4.13 Rotary Encoded Switch

The EVM has a rotary switch that allows a slave address to be selected. This switch selects a 4-bit (hex) value and an I2C converter allows this encoded value to be read by the AM335x through the I2C0 port.

## 5 Pin Use Description

### 5.1 GPIO Definitions

See Section 8.2, which shows the use case columns for GPIOs.

# 6 Board Expansion Connectors

There are two expansion connectors provided in the ICE board. They are used for HOST and I/O signals expansion. The J4 (15 x2, Female) and J3 (9x2, Female) connectors used for HOST expansion are 25x2 headers. The descriptions of the signals are provided in Table 11, Table 12, and Table 13.

**Table 11. AM335x Host Expansion Connector 1- J4**

| Pin No | Signal | Description |
|---|---|---|
| 1 | GPMC_A0 | Address 0 |
| 1 | GPMC_AD0 | Data 0 |
| 3 | GPMC_A1 | Address 1 |
| 4 | GPMC_AD1 | Data 1 |
| 5 | GPMC_A2 | Address 2 |
| 6 | GPMC_AD2 | Data 2 |
| 7 | GPMC_A3 | Address 3 |
| 8 | GPMC_AD3 | Data 3 |
| 9 | GPMC_A4 | Address 4 |
| 10 | GPMC_AD4 | Data 4 |
| 11 | GPMC_A5 | Address 5 |
| 12 | GPMC_AD5 | Data 5 |
| 13 | GPMC_A6 | Address 6 |
| 14 | GPMC_AD6 | Data 6 |
| 15 | GPMC_A6 | Address 6 |
| 16 | GPMC_AD7 | Data 7 |
| 17 | GPMC_A8 | Address 8 |
| 18 | GPMC_AD8 | Data 8 |
| 19 | GPMC_A9 | Address 9 |
| 20 | GPMC_AD9 | Data 9 |
| 21 | GPMC_CSn2 | Chip Select 2 |
| 22 | GPMC_AD10 | Data 10 |
| 23 | GPMC_WEn | Write Enable |
| 24 | GPMC_AD11 | Data 11 |
| 25 | GPMC_OEn_REn | Output Enable/ Read Enable |
| 26 | GPMC_AD12 | Data 12 |
| 27 | GPMC_ADVn_ALE | Address Latch Enable |
| 28 | GPMC_AD13 | Data 13 |
| 29 | GPMC_AD15 | Data 15 |
| 30 | GPMC_AD14 | Data 14 |

**Table 12. AM335x Host Expansion Connector 2- J3**

| Pin No | Signal | Description |
|---|---|---|
| 1 | V3_3D | 3.3-V Power |
| 2 | DGND | Ground |
| 3 | LATCH0_IN | Latch 0 Input |
| 4 | I2C0_SDA | I2C0 Data |
| 5 | LATCH1_IN | Latch 1 Input |
| 6 | I2C0_SCL | I2C0 Clock |
| 7 | UART4_RXD_SYNC0_OUT | Uart 4 Receive / Sync0 Output |
| 8 | UART4_TXD_SYNC1_OUT | Uart 4 Transmit / Sync1 Output |
| 9 | GPIO3_18 | General Purpose I/O |

**Table 12. AM335x Host Expansion Connector 2- J3 (continued)**

| Pin No | Signal | Description |
|---|---|---|
| 10 | EMU4 | JTAG EMU4 |
| 11 | GPIO3_19 | General Purpose I/O |
| 12 | SPI1_SCLK | SPI1 Port Clock |
| 13 | GPIO3_20 | General Purpose I/O |
| 14 | SPI1_D0 | SPI1 Data0 |
| 15 | DGND | Ground |
| 16 | SPI1_D1 | SPI1 Data1 |
| 17 | V24_IN | 24-V Power |
| 18 | SPI1_CS0 | SPI1 Chip Select 0 |

**Table 13. AM335x I/O Expansion Connector – J14**

| Pin No | Signal | Description |
|---|---|---|
| 1 | INDUS INPUT0 | Digital Input 0 |
| 2 | V24_0HVS | 24-V Power |
| 3 | INDUS INPUT1 | Digital Input 1 |
| 4 | V24_0HVS | 24-V Power |
| 5 | INDUS INPUT2 | Digital Input 2 |
| 6 | V24_0HVS | 24-V Power |
| 7 | INDUS INPUT3 | Digital Input 3 |
| 8 | V24_0HVS | 24-V Power |
| 9 | INDUS INPUT4 | Digital Input 4 |
| 10 | V24_0HVS | 24-V Power |
| 11 | INDUS INPUT5 | Digital Input 5 |
| 12 | V24_0HVS | 24-V Power |
| 13 | INDUS INPUT6 | Digital Input 6 |
| 14 | V24_0HVS | 24-V Power |
| 15 | INDUS INPUT7 | Digital Input 7 |
| 16 | V24_0HVS | 24-V Power |
| 17 | DGND | Ground |
| 18 | DGND | Ground |
| 19 | DRAIN0 | Digital Output 0 |
| 20 | DRAIN1 | Digital Output 1 |
| 21 | DRAIN2 | Digital Output 2 |
| 22 | DRAIN3 | Digital Output 3 |
| 23 | DRAIN4 | Digital Output 4 |
| 24 | DRAIN5 | Digital Output 5 |
| 25 | DRAIN6 | Digital Output 6 |
| 26 | DRAIN7 | Digital Output 7 |
| 27 | V5_0D | 5-V Power |
| 28 | V5_0D | 5-V Power |
| 29 | DGND | Ground |
| 30 | DGND | Ground |
| 31 | AIN1 | Analog Input 1 |
| 32 | AIN5 | Analog Input 1 |
| 33 | AIN2 | Analog Input 2 |
| 34 | AIN6 | Analog Input 6 |

**Table 13. AM335x I/O Expansion Connector – J14 (continued)**

| Pin No | Signal | Description |
|---|---|---|
| 35 | AIN3 | Analog Input 3 |
| 36 | AIN7 | Analog Input7 |
| 37 | AIN4 | Analog Input 4 |
| 38 | GNDA_ADC | Analog Ground |
| 39 | GNDA_ADC | Analog Ground |
| 40 | GNDA_ADC | Analog Ground |

# 7 LCD

The LCD used in this design is a passive matrix, monochrome (light blue) display with 96 × 16 pixels, and has a panel size of 29.10 × 9.20 × 1.60 mm. The J17 connector is provided on board to connect with the LCD assembly. The 13 V required for the LCD is generated on board using the TPS61041 boost converter with power input from the 5-V power available in the board.

**Table 14. LCD Connector**

| Pin No | Signal | Description |
|---|---|---|
| 1 | V13 | Power 13.0-V rail |
| 2 | VCOMH | Voltage output High |
| 3 | IRREF | Current Reference |
| 4 | I2C0_SDA | I2C0 Data |
| 5 | I2C0_SCL | I2C0 Clock |
| 6 | RESn | Power Reset |
| 7 | VDD_3V3 | Power Supply 3.3 V |
| 8 | DGND | Ground |
| 9 | VBREF | Voltage Reference |
| 10 | VBAT_LCD | Power Supply for DC-DC converter |
| 11 | C1N | Charge Pump Capacitor1 negative |
| 12 | C1P | Charge Pump Capacitor1 positive |
| 13 | C2N | Charge Pump Capacitor2 negative |
| 14 | C2P | Charge Pump Capacitor2 positive |

# 8 Appendix

## 8.1 AM335x ICEv2 Flash Erase

The AM3359 ICE development board from Texas Instruments comes pre-loaded with a default application in the on-board SPI flash device. To boot Linux from the SD card, you must clear the SPI flash so that the boot process falls back to SD card boot mode. The following steps clear the SPI flash. These steps were performed with CCS v6.1.3 on a Ubuntu 14.04 host system.

1. Ensure pins 1 and 2 of jumper J5 (sysboot) are connected on the board.
2. Ensure that the USB cable is connected from the AM3359 ICE board to the host development machine.
3. Launch Code Composer Studio (CCS). If you do not have CCS, download it here.
4. Create a target configuration file in CCS to connect to the AM3359 ICE board.
   a. Click File -> New -> Target Configuration File
   b. Filename: AM3359-ice-v2.ccxml. Check "Use shared location" to be available to anyone who uses the workspace.
   c. Click Finish. A window opens up to configure the connection details.
      - Connection: "Texas Instruments XDS100v2 USB Debug Probe"
      - Device: ICE_AM3359
   d. Click Save.
5. Launch the AM3359 ICE target configuration.
   a. Click Window -> Show View -> Target Configurations
   b. Right-click on the AM3359-ice-v2.ccxml file and then click Launch Selected Configuration.
   c. This should switch your current perspective to the CCS Debug perspective. If it doesn't, click View -> Debug to get to the CCS Debug perspective.
6. Connect the debugger to the CortexA8 core.
7. Right-click on Texas Instruments XDS100v2 USB Debug Probe_0/CortxA8 listed in the Debug view, and select Connect Target.
8. Load the SPI flash programmer into the CortexA8 core.
   a. Download the SPI flash programmer and unzip it: File:Isdk spi flasher.zip
   b. Highlight the Texas Instruments XDS100v2 USB Debug Probe_0/CortxA8 by clicking on it.
   c. Click Run -> Load -> Load Program
   d. Browse to the isdk_spi_flasher.out file (that was just downloaded and unzipped) and click OK.
9. Run the SPI flash programmer on the CortexA8.
   a. Highlight the Texas Instruments XDS100v2 USB Debug Probe_0/CortxA8 by clicking on it.
   b. Click Run -> Resume
10. At this point, the SPI flash programmer is running on the CortexA8. Follow the prompts to clear the flash.
    a. If it isn't opened already, open the Console view by clicking Window -> Show View -> Console.
    b. The program gives the following prompts; type the responses and press Enter.
       - Enter Operation [1 - Flash ] [2 - Erase] : 2
       - Enter the offset [in Hex]: 0
       - Enter size to be erased in Kilo bytes: 64

When the program outputs 'Erase complete. Exiting' then you are finished. You can now disconnect the debugger and close CCS. Then, power down the board and reconnect pins 2 and 3 on jumper J5 (sysboot). After that, put the SD card loaded with Linux into the ICE board and reset it to boot Linux.

## 8.2 TMDXICE3359 GPIO Assignments

This section provides the GPIO assignments of the AM335x processor-based Industrial Communication EVM (TMDXICE3359) Version 2.1A board.

The section describes the GPIO pins assignments used for the following functionality:

- FET switch Enable
- Ethernet LEDS, VTT Regulator Enable
- NOR FLASH address (GPMC_A18, A19)
- Host Expansion header GPIOs
- Ethernet Mux Enable
- SYS BOOT buffer Enable

**Table 15. TMDXICE3359 GPIO Assignments**

| Sl No. | Pin No. | GPIO | Net Name | Purpose |
|---|---|---|---|---|
| 1 | C18 | GPIO0_7 | FET_nOE | FET Switch Enable for MII0 Link and Err signals |
| 2 | J18 | GPIO0_16 | LED_2 | Ethernet LED 2 |
| 3 | K15 | GPIO0_17 | LED_1 | Ethernet LED 1 |
| 4 | F16 | GPIO0_18 | DDR_VTT_EN | VTT Regulator Enable |
| 5 | A15 | GPIO0_19 | EMU2_GPIO0_19 | Ethernet LED 6 |
| 6 | D14 | GPIO0_20 | EMU2_GPIO0_19 | Ethernet LED 5 |
| 7 | T3 | GPIO2_12 | GPIO2_12 | GPMC_A18 to NOR Flash |
| 8 | T4 | GPIO2_13 | GPIO2_13 | GPMC_A19 to NOR Flash |
| 9 | B12 | GPIO3_18 | GPIO3_18 | Host Expansion header GPIO 1 |
| 10 | C13 | GPIO3_19 | GPIO3_19 | Host Expansion header GPIO 2 |
| 11 | D13 | GPIO3_20 | GPIO3_20 | Host Expansion header GPIO 3 |
| 12 | T6 | GPIO2_05 | GPIO_KEY4 | User Key4 |
| 13 | J17 | GPIO3_04 | PR1_MII_CTL | Enable signal to the Sysboot buffers (only available in V2.1A) |
| 14 | K18 | GPIO3_09 | LED_3 | Ethernet LED 3 |
| 15 | L18 | GPIO3_10 | MUX_MII_CTL1 | Ethernet Mux Enable |
| 16 | F15 | GPIO3_13 | LCD_BST_CONV_CTL | VCC Enable control for LCD power circuitry |
| 17 | U9 | GPIO1_30 | LED_4 | Ethernet LED 4 |

# 9 EVM Important Notices

The Standard Terms And Conditions for TI Evaluation Modules can be downloaded from here: http://www.ti.com/lit/pdf/sszz027

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