User's Guide

ABSTRACT

This technical User's Guide describes the hardware architecture of the AM65x IDK. The AM65x processor is part of the K3 Multicore SoC architecture platform Arm.

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1 Introduction

The AM65x IDK is a standalone test, development, and evaluation module (EVM) system that lets developers write software and develop hardware for industrial communication-type applications. The IDK is equipped with AM6548 processor from TI and a defined set of features to let the user experience industrial communication solutions using serial, Ethernet-based, PCIe, and many other interfaces. Using standard interfaces, the IDK can communicate with other processors or systems, and act as a communication gateway. In addition, the IDK can directly operate as a standard remote I/O system or simple sensor connected to an industrial communication network. The embedded emulation logic allows for emulation and debugging using standard development tools such as Code Composer Studio™, from TI, by using the supplied USB cable.

1.1 Key Features

The AM65x IDK is a high performance, standalone development platform that enables users to evaluate and develop industrial applications for the Texas Instrument's K3 System-on-Chip (SoC). The AM65x IDK supports the following key features:

- Based on the K3 architecture with Arm
- 4-GB DDR4 supporting data rate up to 1600 MT/s
- 16-GB eMMC Flash
- Full size SD card, up to 64-GB density with UHS-1 support (8-GB UHS-1 card supplied with the kit)
- 128-Mbit SPI EEPROM
- 512-Mbit OSPI EEPROM
- 256-Kbit I2C Boot EEPROM
- 3× PRU-ICSSG, supporting multi-protocol industrial Gigabit Ethernet with up to 6 ports
- 1x MCU Gigabit Ethernet port
- One USB2.0 interface port with Micro AB connector
- CSI-2 connector to interface camera card
- I-PEX EVAFLEX5-VS connector to interface with the LCD adapter card
- GPMC/DSS interface expansion connector
- Application board expansion connector
- SERDES expansion connector to interface two lane PCIe Personality card
- XDS110 on-board emulator
- Quad port UART to USB circuit over microB USB connector
- Expansion headers:
  - Two UART
  - One SPI
  - One I2C
  - Four timer signals
- Boot mode selection using DIP switches
- Two push buttons to generate interrupts
- Industrial Ethernet LEDs
- Rotary switch input
- Two CAN interface terminated to DB-9 connector
- Digital serializer for processing wide range inputs from industrial I/O connector
- Profibus UART transceiver terminated with DB9 connector
- DC Input: 11 V to 28 V
- Status output: LEDs to indicate power status
- INA devices for current monitoring
- Over- and under-voltage protection circuit
- RoHS-compliant design

Featured applications:

- Industrial Drives
- Industrial Sensors

- Factory Automation and Control

2 AM65x IDK Overview

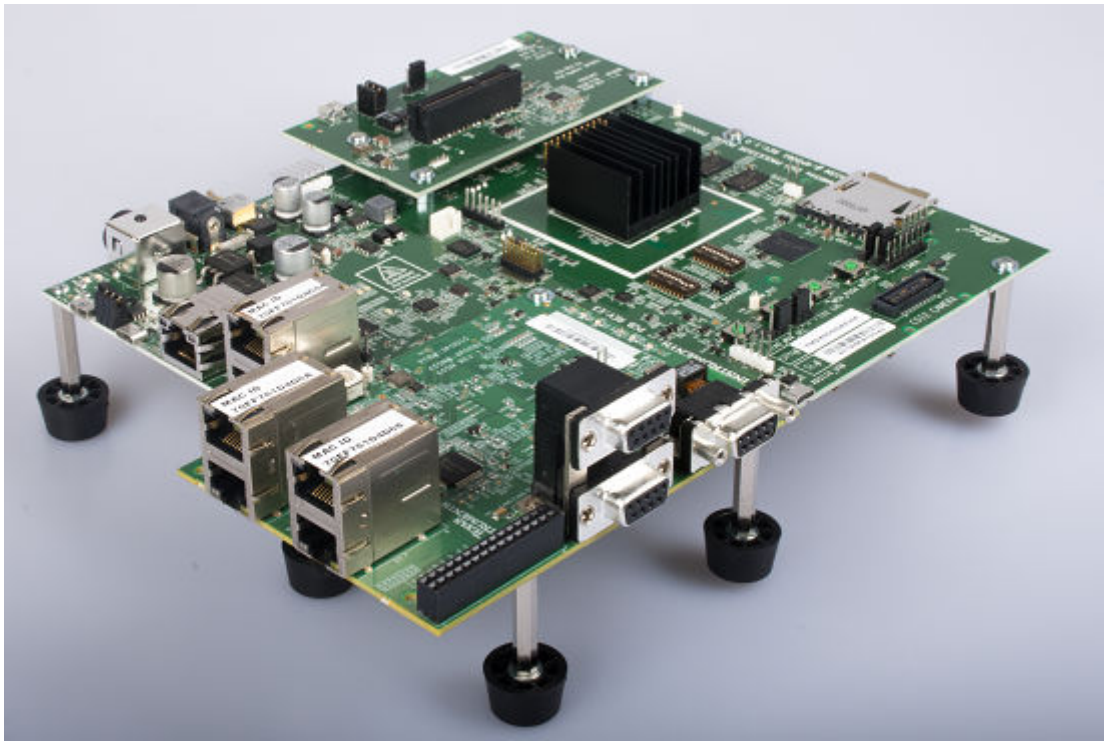

Figure 2-1. System Assembly Image

Figure 2-2 shows the overall architecture of AM65x IDK.

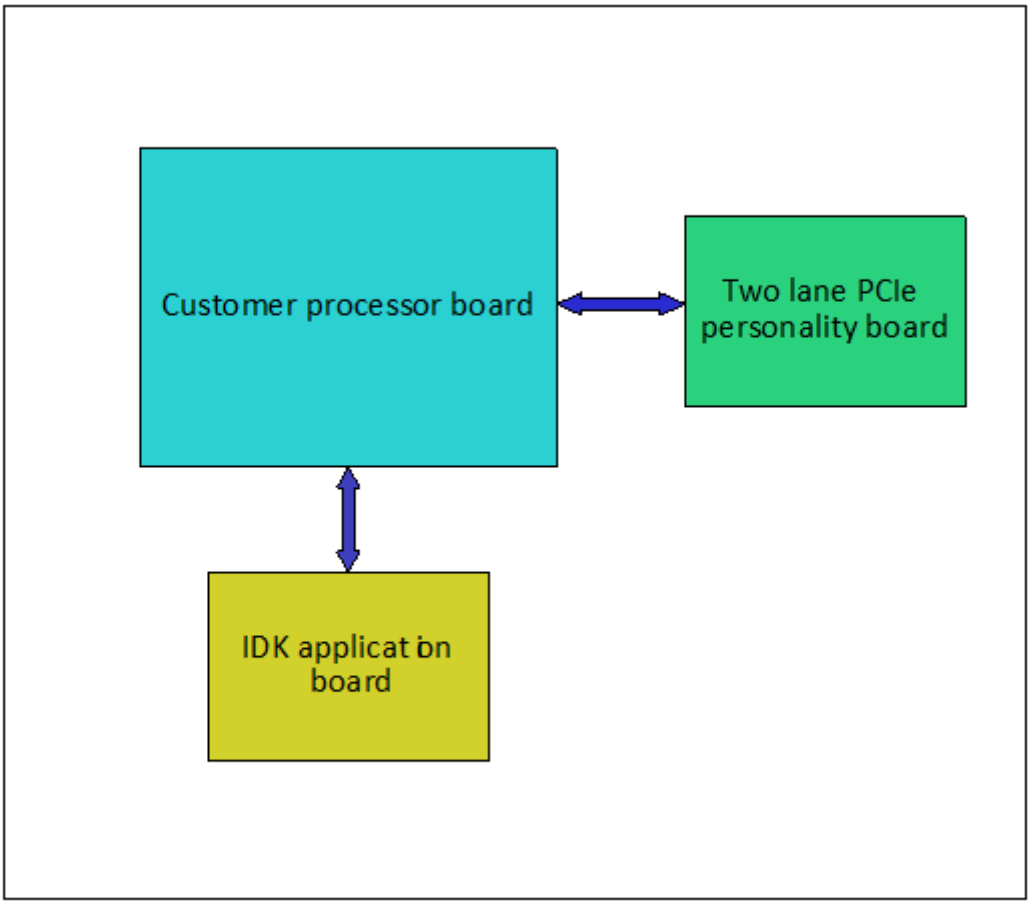

Figure 2-2. System Architecture Interface

The AM65x IDK consists of a common processor board, IDK application board, and a two-lane PCIe personality card. Detailed descriptions of these cards are explained in the following sections.

3 Common Processor Board

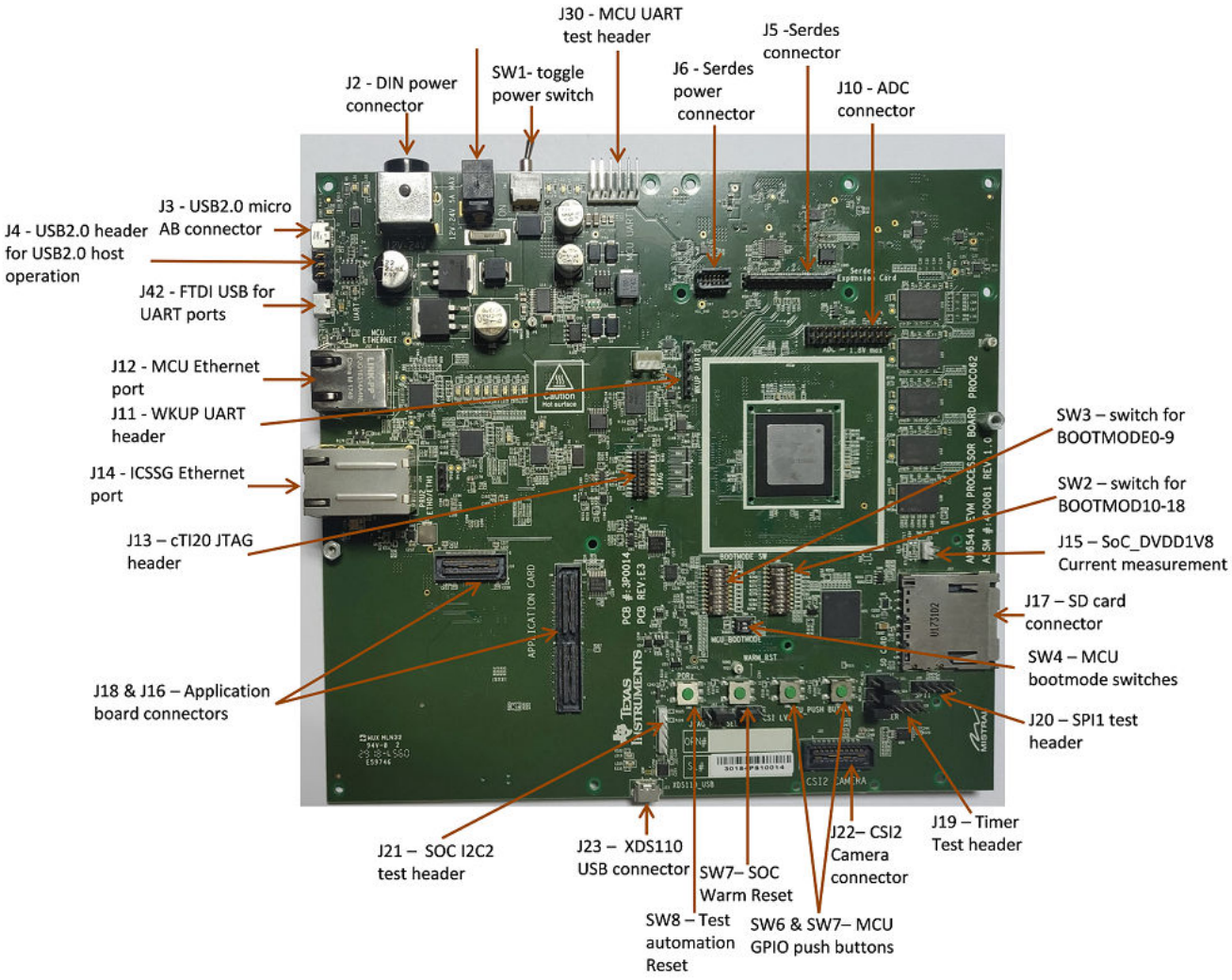

Figure 3-1. Top View of the Common Processor Board

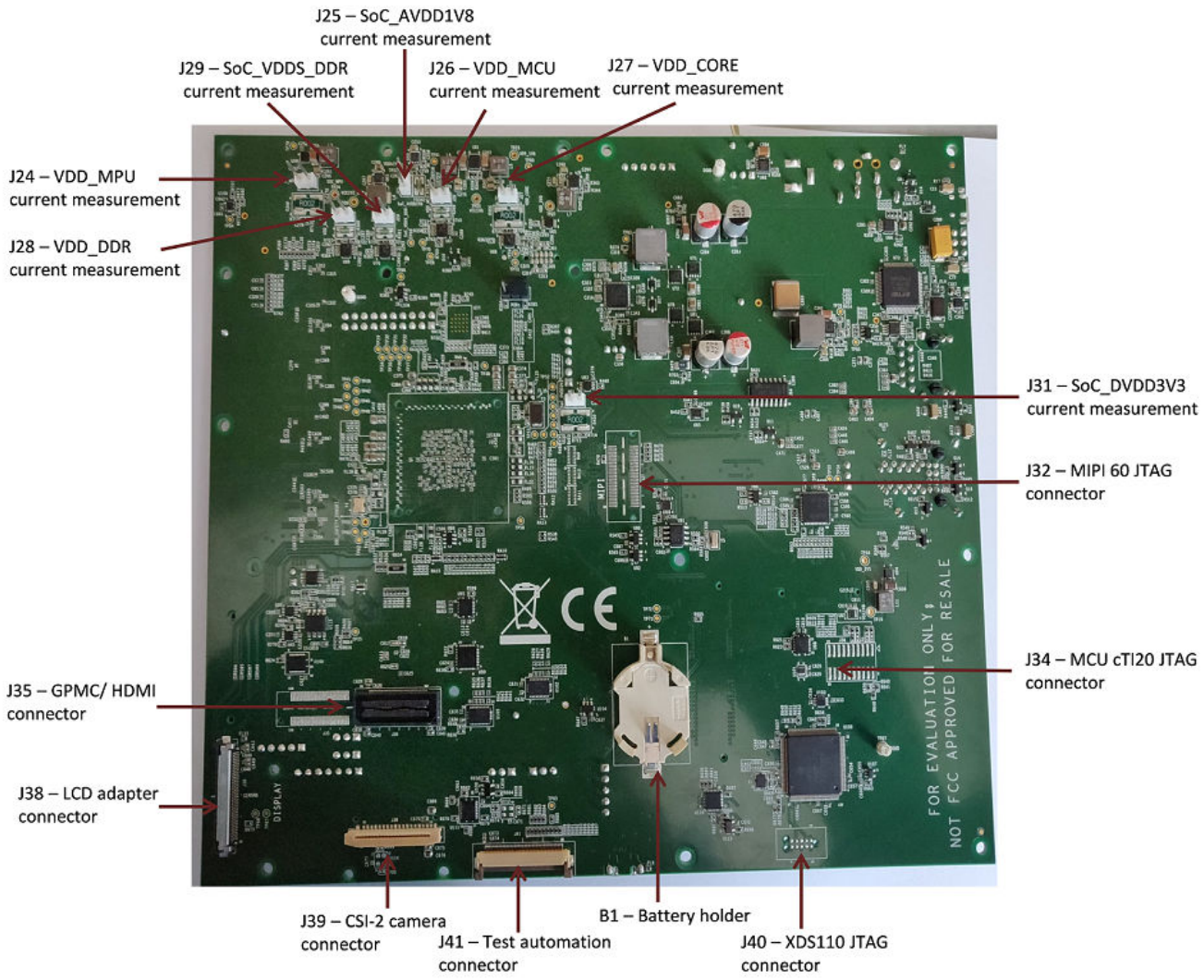

Figure 3-2. Bottom View of the Common Processor Board

3.1 Key Features

SoC:

- Based on the K3 architecture with Quad-Core Arm® Cortex®-A53 Microprocessor and Dual-Core Arm Cortex-R5F Arm
- Heatsink and support for 12-V fan

Memory:

- 4-GB DDR4 supporting data rate up to 1600 MT/s
- 16-GB eMMC Flash which can support HS400 speed of operation
- Full size SD card, up to 64-GB density with UHS-1 support
- 128-Mbit SPI EEPROM
- 512-Mbit OSPI EEPROM
- 256-Kbit I2C EEPROM for Boot

I/O Interface:

- One MCU Gigabit Ethernet port and two Industrial Ethernet ports based on the Gigabit Industrial Communication Subsystem (PRU-ICSS-Gb) paired with Texas Instruments Gigabit Ethernet PHYs
- One USB2.0 interface with Micro AB connector
- CSI-2 connector to interface camera card

Expansion Bus:

- I-PEX EVAFLEX5-VS connector to interface with the LCD adapter card
- GPMC/DSS interface expansion connector for secondary display
- Application connector to expansion application cards
- SERDES expansion connector to support various SERDES modules

Debug:

- XDS110 on-board emulator
- Supports 20-pin JTAG connection from external emulator
- Automatic selection between on-board and external emulator (higher priority)
- Quad port UART to USB circuit over microB USB connector
- Two UART, one SPI, and I2C ports connected to test header for slave testing of the AM65x device
- Four timer signals from Maxwell connected to test header
- Two push buttons to generate Interrupts

Power Supply:

- Wide range DC input: 11 V to 28 V
- Status output: LEDs to indicate power status
- INA devices for current monitoring
- Over- and under-voltage protection circuit

Compliance:

- RoHS-compliant
- REACH-compliant

In compliance with the Article 33 provision of the EU REACH regulation, we are notifying you that this module includes crystals (ABM3-25.000MHZ-D2Y-T, ABM3-12.000MHZ-D2Y-T) from Abracon LLC that contains two Substance of Very High Concern (SVHC) above 0.1%. These uses from Texas Instruments do not exceed 1 ton per year. The SVHC's are Diboron trioxide CAS#1303-86-2 and Lead Oxide CAS# 1317-36-8.

3.2 Functional Block Diagram

The functional block diagram of the common processor board is shown in Figure 3-3.

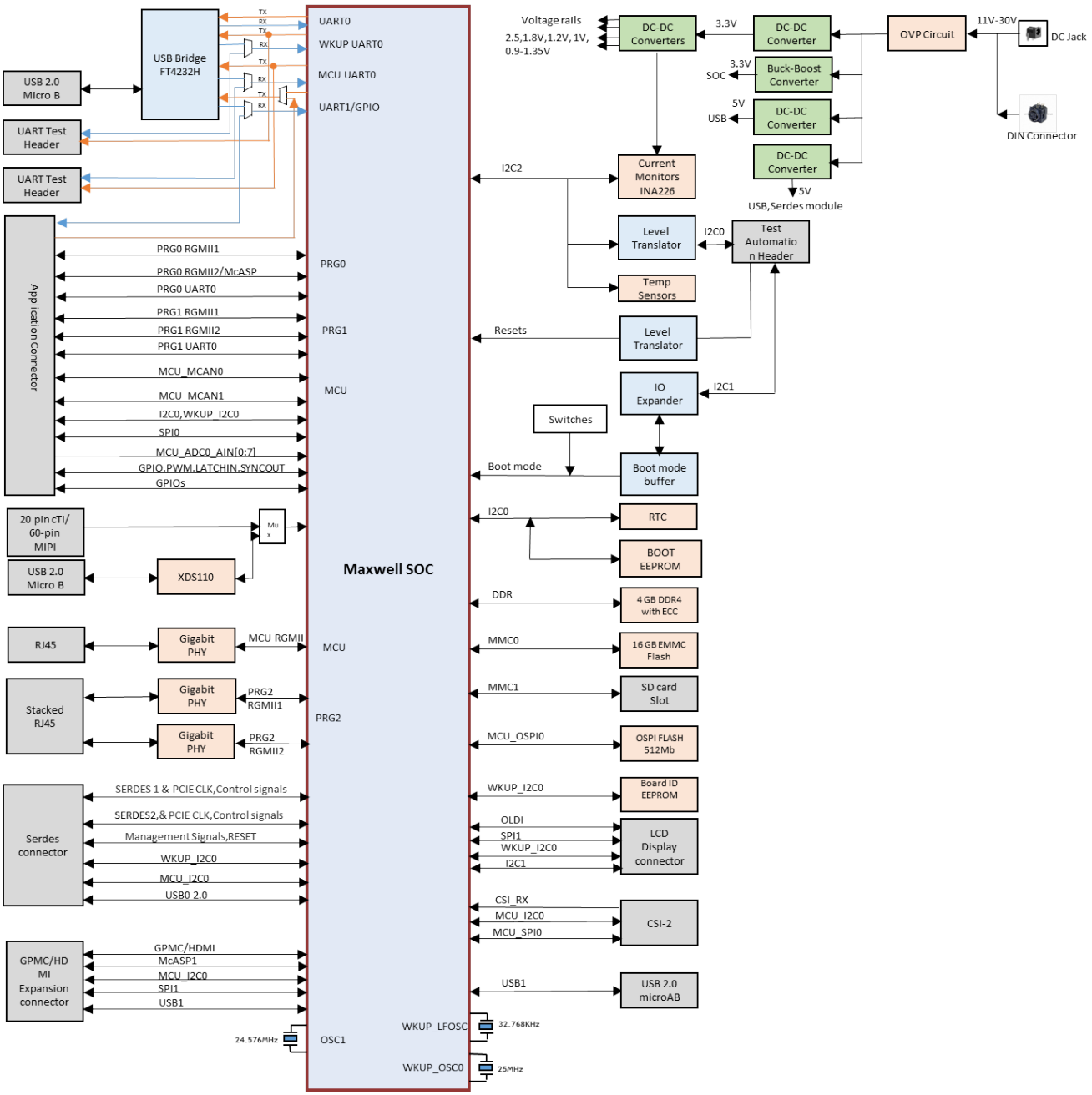

Figure 3-3. Common Processor Board Functional Block Diagram

3.3 Overview of Common Processor Board

This section provides an overview of the different interfaces and circuits on the common processor board.

3.3.1 Clocking

SOC requires a crystal for MCU, System Clock, and a 32.768-kHz square wave input for LFOSC input.

3.3.1.1 RTC Clock

A real time clock IC is connected to the I2C0 interface of the AM65x processor. The RTC device is powered by 3.3 V as a primary supply. This IDK is designed for optional use with a removable CR2032 UL recognized lithium

battery, which can be inserted using a battery holder provided on the CP board. Always use the CR2032VP Energizer 3-V Lithium coin cell battery or similar CR2032 UL-recognized battery with nominal voltage of 3.0 V, Capacity 240 mAh. The battery is not provided with the IDK EVM. A 32.768-kHz quartz crystal is used to provide the clock for the RTC device. The RTC device generates 32.768-kHz square wave output, which is connected to WKUP_LFOSC input of the SoC.

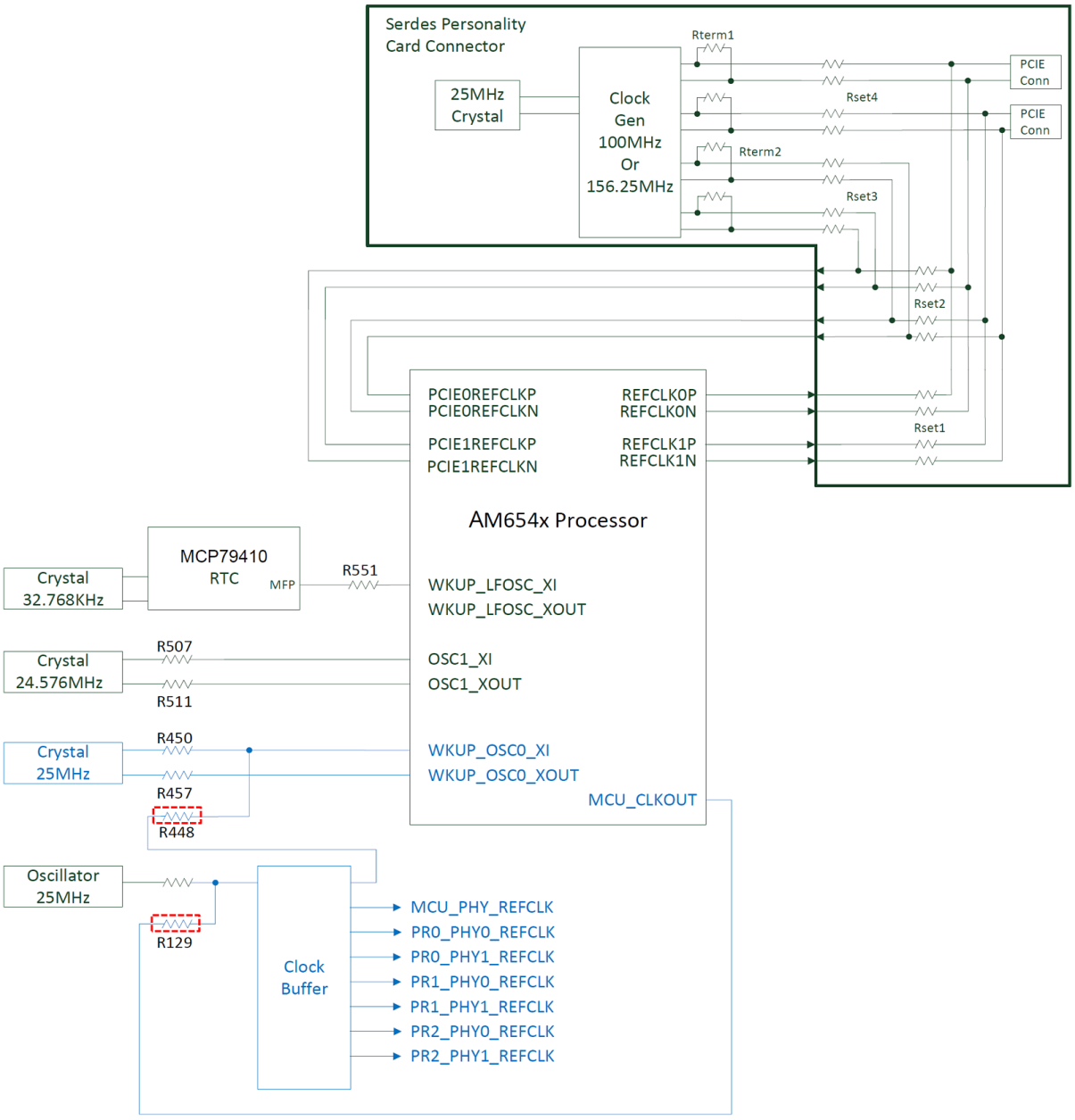

Figure 3-4. AM65x IDK Clock Tree

Note

Resistors marked with a red color box are DNI.

3.3.1.2 Maxwell SoC Clock

HFOSC0, HFOSC1: The HFOSC0 (OSC0) and HFOSC1 (OSC1) clocks are muxed inside the SOC, and the result is connected to main PLL. The output of the main PLL is used as the system clock for SOC. The input of WKUP_OSC 0 can be provided with a 25-Mhz crystal or by using the output of the clock generator. The default

25-Mhz crystal is connected; to use the clock generator output as input for WKUP_OSC 0, resistor R448 must be mounted and resistors R450 and R457 removed.

LFOSC: The 32.768-KHz square wave is provided by the MFP output of the RTC component.

3.3.1.3 Ethernet PHY Clocks

The Ethernet PHYs are clocked with 25 MHz using a 1:10 LVCMOS clock generator. It is a clock buffer, which takes 25-MHz crystal/LVCMOS reference input and provides ten 25-MHz LVCMOS clock outputs.

The source for the clock buffer can be either the MCU_CLKOUT0 signal from the AM65x processor or a 25-MHz oscillator (default). This selection can be made through the select lines of the clock buffer by using the resistor options as shown in Table 3-1. In addition, the pinmux for pin AB3 must be modified to select the MCU_CLKOUT0 function. This function is not present when the part is removed from reset. If MCU_CLKOUT0 is used, the Ethernet boot mode for the AM645x cannot be used.

Note

When MCU_CLKOUT0 is used as the source for the clock buffer, resistor R129 must be mounted.

Table 3-1. Source Clock Selection for the Clock Buffer

IN_SEL1	IN_SEL0	clock chosen	Mount	Unmount
0	0	MCU clock	R187, R197	R189, R193
1	0	Crystal input	R189, R197	R187, R193

3.3.1.4 SERDES Clock

The SERDES reference clock inputs and outputs of the SoC are routed to the Personality module connector. Various options to select the SERDES clock configurations are present on the Personality modules. By default, SERDES reference clocks are generated internally and supplied on the REFCLK0P/N and REFCLK1P/N pins.

3.3.2 Reset

Warm reset input can be applied through manual reset switch SW7.

Power-on reset input can be applied though switch SW8.

The AM65x processor supports an option to bypass the internal POR generation. A 3-pin header J8 is provided to select internal or external POR. Short pin 2 and pin 3 of the header J8 to enable internal POR (default), and short pin 1 and 2 to bypass the internal POR.

Most peripheral resets are “ANDED” with the POR output from the SoC along with a GPIO control, as shown in Figure 3-5.

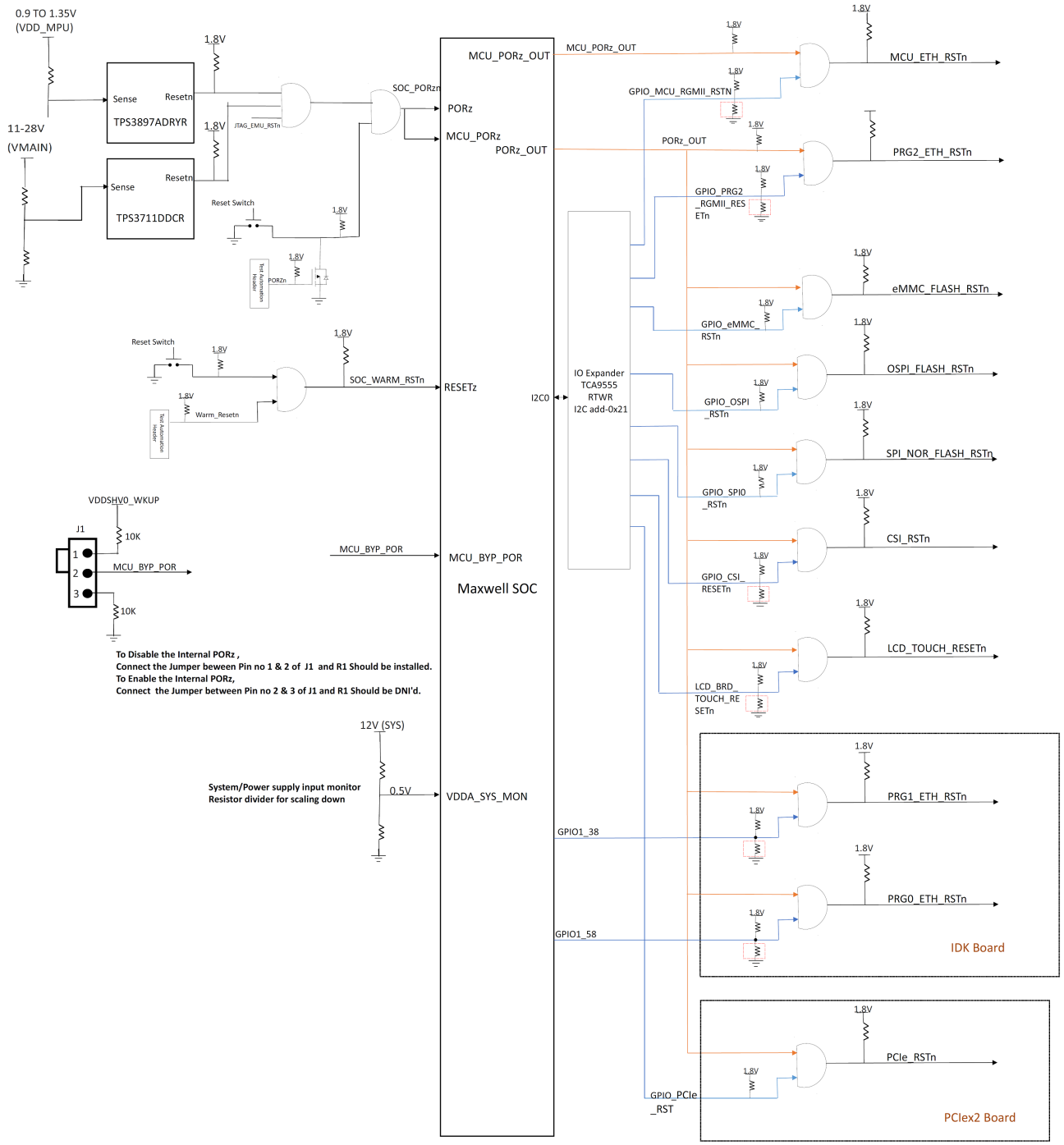

Figure 3-5. Overall Reset Architecture of the AM65x IDK

3.3.3 Power Requirements

3.3.3.1 Power Input

This IDK supports a wide input range of 11 V to 28 V. There are two connectors provided for power input:

- 4-pin DIN connector J2 which supports 10-A current rating
- DC barrel jack connector J1 which supports 5-A current rating

For most applications, the standard DC barrel jack can be used. The 4-pin DIN connector should be used when PCIe card is plugged in to the PCIe daughter card.

CAUTION

Never connect external power supplies to both the barrel jack and the din connectors at the same time.

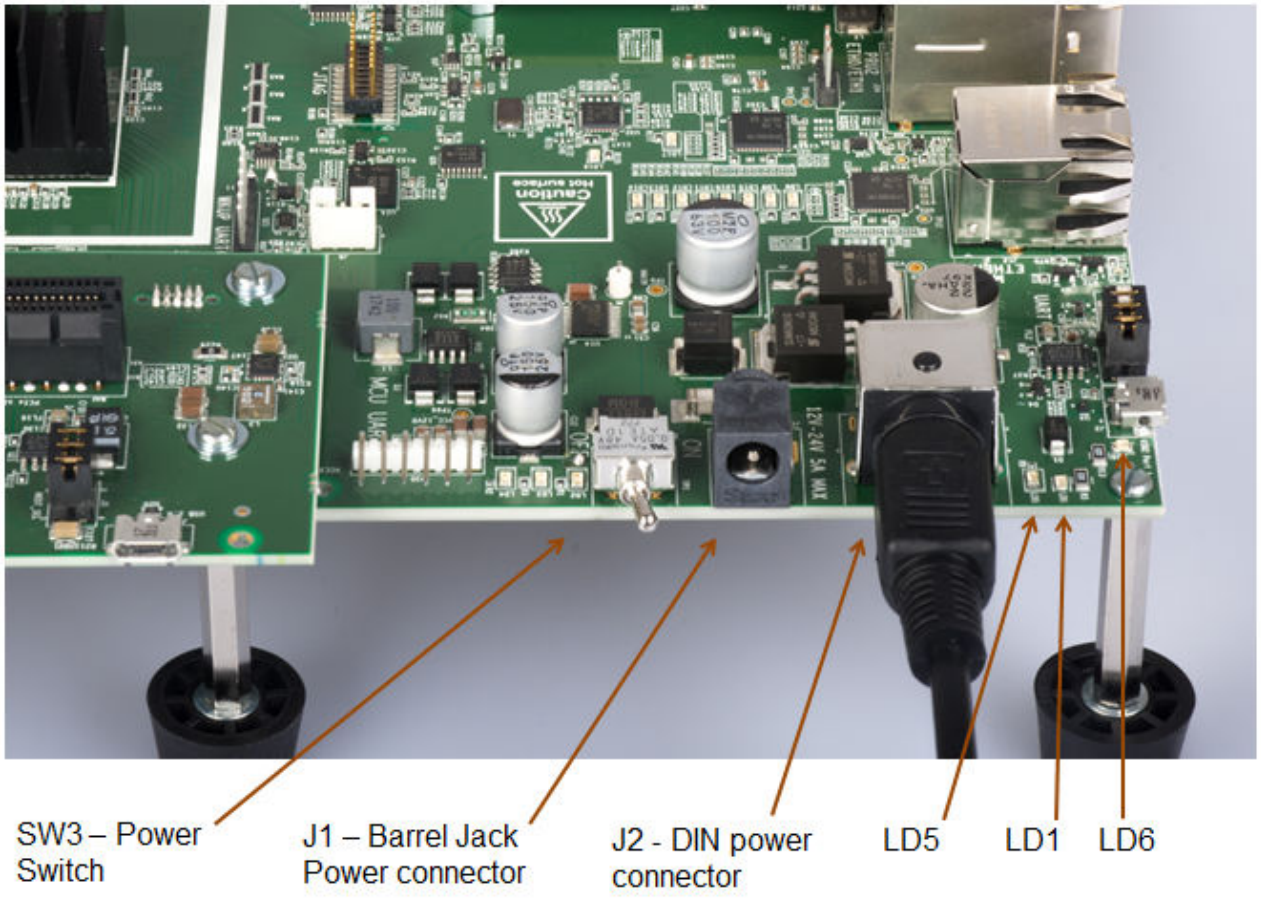

Figure 3-6. Connectors Used for Power Input

3.3.3.2 Overvoltage and Undervoltage Protection Circuit

The voltage protection circuit on the AM65x IDK protects the board from overvoltage, undervoltage, transient voltage, and reverse voltage input cases. The safe operation input voltage range is 11 V to 28 V. A fault indication and power good LEDs are provided to indicate the power status.

Table 3-2. Power LED Status

LED	ON Status	OFF Status
LD1	Power polarity reversed	Power polarity good
LD6	Input voltage is >28 V or <11 V	Input voltage is within the limit
LD5	Board Power on	Board Power off

The power ON/OFF switch functionality is implemented using the over- and undervoltage protection circuit.

3.3.3.3 Voltage Supervisor

The power rails are monitored to control the Power ON Reset (PORz) for SOC. Two supervisor devices are provided to monitor main power input and VDD_MPU rail (last rail in the power on sequence of the SOC).

3.3.3.4 Current Monitoring

INA226 power monitor devices are used to monitor current and voltage of various power rails of the AM65x processor. The device reports current, voltage, and power to the AM65x processor through the I2C interface. Four terminal high precision shunt resistors are provided, and the values are calculated based on load current.

Table 3-3. INA Devices I2C Slave Address

POWER SOURCE	SUPPLY NET	SLAVE ADDRESS(IN HEX)	Value of the Shunt Connected to the Supply Rail
VCC1V0	VDD_CORE	40	0.002E_1%
VCC1V0	VDD_MCU	41	0.01E_0.5%
VCC3V3_IO	VDD_MPU	42	0.002E_1%
SoC_MPU	SoC_DVDD3V3	43	0.002E_1%
VCC1V8	SoC_DVDD1V8	44	0.01E_0.5%
VDDA1V8	SoC_AVDD1V8	45	0.01E_0.5%
VCC1V2_DDR	SoC_VDDS_DDR	46	0.01E_0.5%
VCC1V2_DDR	VDD_DDR	47	0.01E_0.5%

3.3.3.5 Power Supply

The processor card uses an array of DC-DC converters to supply the various memories, clocks, SOC, and other components on the card with the necessary voltage and the power required. Multiple power-good LEDs are provided on the card to give users positive confirmation of the status of output of each supply.

Test points for each power outputs are provided on the processor card and are mentioned in Table 3-4.

Table 3-4. Power Test Points

Sl #	Power Supply	Test Point	Voltage	Tolerance
Card Top Side				
1	VINPUT	TP10	Applied input voltage	11 V to 28 V
2	VMAIN	TP9	Applied input voltage	11 V to 28 V
3	VCC_5V0	TP7	5.0 V	+/- 5%
4	VCC3V3_PREREG	TP1	3.3 V	+/- 5%
5	VCC_12V0	TP66	12.0 V	+/- 5%
6	VCC3V3_IO	TP20	3.3 V	+/- 5%
7	VDDR_VTT	TP5	1.65 V	+/- 5%
8	VCC_2V5	TP82	2.5 V	+/- 5%
Card Bottom Side				
1	SoC_MPU	TP24	1.0-V Typical, Changes based on I2C configuration	+/- 5%
2	VCC1V2_DDR	TP26	1.2 V	+/- 5%
3	VCC1V0	TP25	1.0 V	+/- 5%
4	VPP_1V8	TP23	1.8 V	+/- 2.5%
5	VDDA1V8	TP22	1.8 V	+/- 5%
6	VDD_2V5	TP64	2.5 V	+/- 5%
7	VDD_1V0	TP27	1.0 V	+/- 5%
8	VCC1V8	TP19	1.8 V	+/- 5%

Table 3-5. Power LEDs

Sl #	Power Supply	LED
1	VCC3V3_PREREG	LD3
2	VCC_5V0	LD2
3	VCC_12V0	LD4

3.3.3.6 Power Sequencing

Figure 3-7 shows the power-up sequence of all the power supplies present on the processor card.

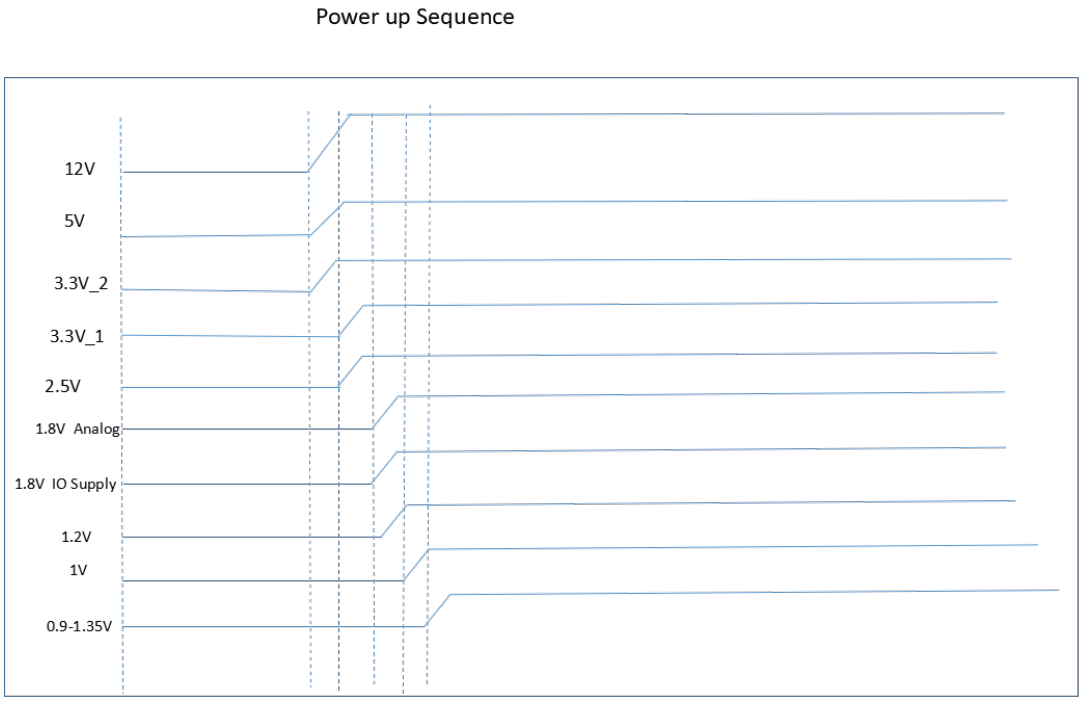

Figure 3-7. Power ON Sequencing

3.3.3.7 SoC Power

SoC has different I/O groups. Each I/O group is powered by specific power supplies, as shown in Table 3-6.

Table 3-6. SOC Power Supply

Sl.No.	Power Supply	SoC Supply Rails	IO Power Group	Power
1	VDDSHV_GENERAL	VDDSHV0, VDDSHV1	GENERAL	3.3 V
2	VDDSHV_GPMC	VDDSHV2	GPMC	3.3 V
3	VDDSHV_PRG0	VDDSHV3	PRG0	1.8 V
4	VDDSHV_PRG1	VDDSHV4	PRG1	1.8 V
5	VDDSHV_PRG2	VDDSHV5	PRG2	1.8 V
6	VDDSHV_MMC0	VDDSHV6	MMC0	1.8 V
7	VDDSHV_MMC1	VDDSHV7	MMC1	1.8 V
8	VDDSHV_WKUP_GENERAL	VDDSHV0_WKUP	MCU_GENERAL	3.3 V

Table 3-6. SOC Power Supply (continued)

Sl.No.	Power Supply	SoC Supply Rails	IO Power Group	Power
9	VDDSHV_WKUP_FLASH	VDDSHV1_WKUP	MCU_FLASH	1.8 V
10	VDDSHV_WKUP_CPSW2G	VDDSHV2_WKUP	MCU_CPSW2G	1.8 V

Table 3-7. SOC Bias Supply

Sl.No.	Bias Supply	I/O Group	Power
1	VDDS_GENERAL	GENERAL	Internal LDO (CAP_VDDA_1P8_IOLDO)
2	VDDS_GPMC	GPMC	Internal LDO (CAP_VDDA_1P8_IOLDO)
3	VDDS_PRG0	PRG0	1.8-V I/O supply
4	VDDS_PRG1	PRG1	1.8-V I/O supply
5	VDDS_PRG2	PRG2	1.8-V I/O supply
6	VDDS_MMC0	MMC0	1.8-V I/O supply
7	VDDS_MMC1	MMC1	1.8-V I/O supply
8	VDDS_WKUP_GENERAL	MCU_GENERAL	Internal LDO (CAP_VDDA_1P8_IOLDO_WKUP)
9	VDDS_WKUP_FLASH	MCU_FLASH	1.8-V I/O supply
10	VDDS_WKUP_CPSW2G	MCU_CPSW2G	1.8-V I/O supply

3.3.4 Configuration

3.3.4.1 Boot Modes

The boot mode for the SoC is defined by a bank of switches SW2, SW3, and SW4. Switch set to “ON” corresponds to logic “HIGH”, while “OFF” corresponds to logic “LOW”. The following boot modes are supported:

1. No boot
2. OSPI
3. MMC1 - SDCard
4. MMC 0- eMMC installed
5. PCIE - PCIE as an endpoint
6. CPSW - Ethernet slave boot
7. USB - boot using host mode with bulk storage. USB2.0 mass storage device using FAT16/32 (such as a thumb drive)
8. USB - device boot DFU
9. UART
10. I2C EEPROM

The BOOTMODE pins provide the means to select the boot mode before the device is powered up. They are divided into the following categories.

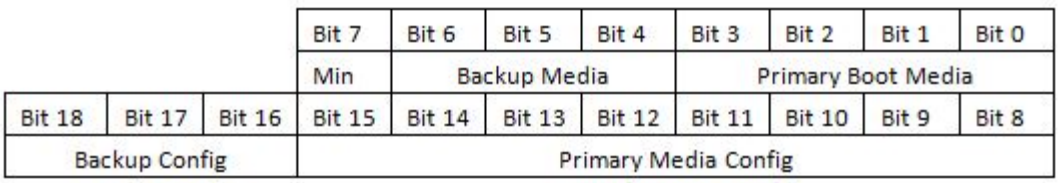

Figure 3-8. BOOTMODE Bits

BOOTMODE[3:0] – This provides the primary boot mode configuration to select the requested boot mode after POR; that is, the peripheral/memory to boot from.

Table 3-8. Boot Device Selection BOOTMODE[3:0]

SW3.4	SW3.3	SW3.2	SW3.1	Primary Boot Device Selected
off	off	off	off	Sleep (No boot – debug mode)
off	off	off	on	OSPI
off	off	on	off	QSPI
off	off	on	on	Hyperflash
off	on	off	off	SPI (on QSPI/OSPI port 0 in legacy SPI mode)
off	on	off	on	I2C
off	on	on	off	MMC/SD card, eMMC boot from UDA or file system
off	on	on	on	Ethernet
on	off	off	off	USB
on	off	off	on	PCIe
on	off	on	off	UART
on	off	on	on	Reserved
on	on	off	off	GPMC XIP
on	on	off	on	eMMC boot from boot partition (with auto-fall back to file system)
on	on	on	off	Reserved (acts as no boot)
on	on	on	on	Reserved (acts as no boot)

BOOTMODE[6:4] – Select the backup boot mode; that is, the peripheral/memory to boot from, if the primary boot device failed.

Table 3-9. Backup Boot Mode Selection BOOTMODE[6:4]

SW3.7	SW3.6	SW3.5	Backup Boot Device Selected
off	off	off	None (No backup mode)
off	off	on	USB
off	on	off	UART
off	on	on	Ethernet
on	off	off	MMC/SD
on	off	on	SPI on OSPI/OSPI port 0 in legacy SPI mode)
on	on	off	Hyper flash
on	on	on	I2C

BOOTMODE07 – This is the minimum (MIN) configuration pin. The min pin is provided as a way to use minimal pin strapping to configure boot. When the min pin value is 1, all configuration fields are based on pre-defined default values. In this case, no boot mode pins beyond the min pin need to be driven because their values are ignored.

BOOTMODE[15:8] – These pins provide optional settings and are used in conjunction with the primary boot device selected. Refer to the *AM65x Multicore ARM Keystone III System-on-Chip (SoC) Technical Reference Manual* for more details.

Table 3-10. Primary Boot Media Configuration BOOTMODE[15:8]

SW2.6	SW2.5	SW2.4	SW2.3	SW2.2	SW2.1	SW3.10	SW3.9	Boot Device
Not Used								Sleep
Pin Cmd			Csel		Speed		Adr Wid	OSPI
Port	Pin Cmd		Csel		Speed		Adr Wid	QSPI
Not Used				Csel		Speed		Hyperflash
Port	Mode		Csel		Cmd	Adr Width		SPI
Not Used		Bus Reset		Mode	Spd	Addr		I2C
Not Used			Port	Interface Config			1bit	MMC/SD card
clkout		iface		spd	dplx	Extern con		Ethernet
Not Used				Usb3	Mode		Port	USB
Port	Dual	sref		BAR Config PCIe				
Not Used								UART
Idx	AD mux		Csel Size		Csel		Wid	GPMC XIP
Not Used	Port	Alt	Bus Width		Speed		ack	eMMC

BOOTMODE[18:16] – These pins provide optional settings and are used in conjunction with the backup boot device devices. Refer to the *AM65x Multicore ARM Keystone III System-on-Chip (SoC) Technical Reference Manual* for more information on bit details. Switches SW2.[7:9] when on sets 1 and sets 0 if off.

Table 3-11. Backup Boot Media Configuration BOOTMODE[18:16]

SW2.9	SW2.8	SW2.7	Boot Device
Not Used			None
Not Used		Port	USB
Not Used			UART
clkout	Interface		Ethernet
Not Used	Port	1 Bit	MMC/SD
Port	Adr Width/Cmd		SPI
	Speed		Hyperflash
reset	Mode	Addr	I2C

MCU_BOOTMODE pins provide ROM code with information for the system clock speed and fail-safe boot device.

Table 3-12. MCU BOOTMODE Bits

Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved						Fail Safe mode		Ref Clock Select		

MCU_BOOTMODE[2:0] – Denotes system clock frequency for PLL configuration. By default, these bits are set for 25 MHz.

Table 3-13. PLL Reference Clock Selection MCU_BOOTMODE[2:0]

Bit 2	Bit 1	Bit 0	PLL REF CLK (MHz)
0	0	0	19.2
0	0	1	20
0	1	0	24
0	1	1	25
1	0	0	26
1	0	1	27
1	1	0	Reserved
1	1	1	No PLL Configuration Done (slow speed backup)

MCU_BOOTMODE[4:3] – Select the fail-safe boot mode, as shown in Table 3-14.

Table 3-14. Fail-Safe Boot Configuration

SW4.2	SW4.1	PLL REF CLK (MHz)
off	off	No fail-safe boot supported
off	on	I2C port 0
on	off	SPI Port 0
on	on	Hyperflash Port 0

MCU_BOOTMODE[10:5]- Reserved

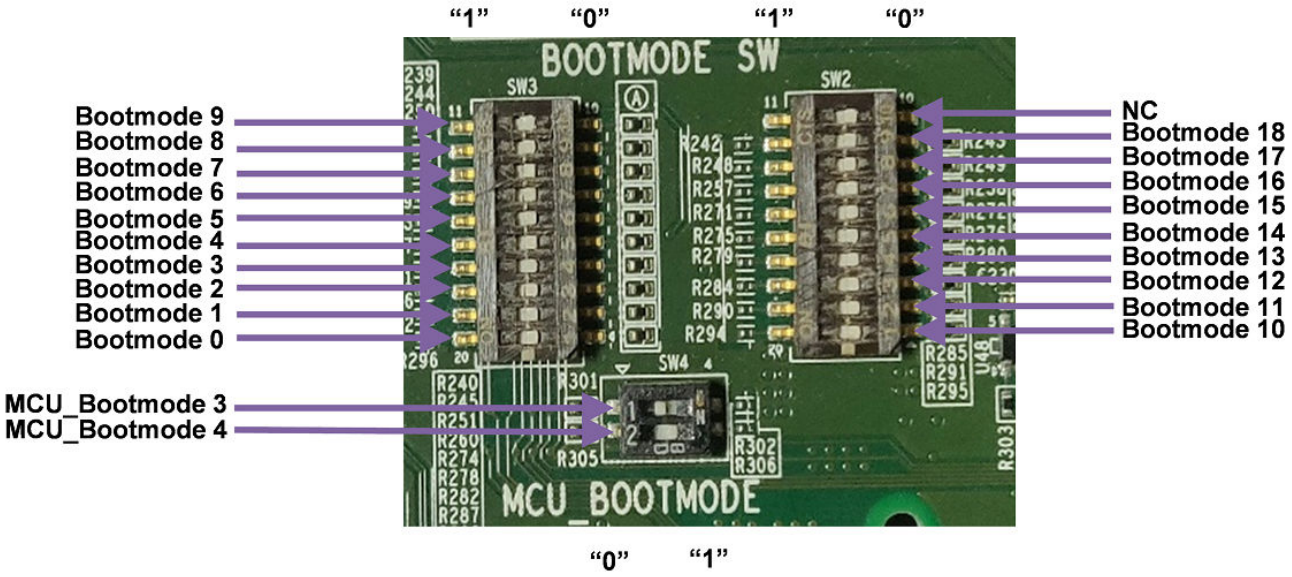

Figure 3-9. BOOT Switches Provided on the Processor Card

3.3.4.2 JTAG

The common processor card includes XDS110 class on-card emulation through the micro B connector J23. It also has an optional TI20 pin (J13) connector to support external emulation. When an external emulator is connected, internal emulation circuitry is disabled. The design includes the footprint for a MIPI60pn (J32) connector with connections for JTAG and trace capabilities. The trace pins are pinmuxed with ICSSG2 RGMII signals which, by default, are connected to Ethernet PHYs on the processor board. Resistor networks are used to steer these signals to either the Ethernet PHYs or to the MIPI60 connector. The MIPI60 is not installed as delivered.

ICSSG2 Ethernet signals from the SoC are multiplexed with JTAG trace signals. Resistor options are provided to connect these signals to the Ethernet PHYs or Trace connector, as shown in Table 3-15.

Table 3-15. Selection of PRG2_Ethernet PHY (CP Board PHY) and JTAG TRACE Functionality

Signals selected	Mount	Un mount
PRG2 signals to Ethernet PHY (default)	RA3	RA10
	RA5	RA11
	RA1	RA9
	R180	R466
	R183	R463

Table 3-15. Selection of PRG2_Ethernet PHY (CP Board PHY) and JTAG TRACE Functionality (continued)

Signals selected	Mount	Un mount
JTAG Trace signals to J32	RA10	RA3
	RA11	RA5
	RA9	RA1
	R466	R180
	R463	R183

Table 3-16. TI20 Pin Connector (J13) Pin-out

Pin No.	Signal	Pin No.	Signal
1	JTAG_CTI_TMS	11	CTI_TCK
2	JTAG_TRSTN	12	DGND
3	JTAG_CTI_TDI	13	JTAG_CTI_EMU0
4	JTAG_TDIS	14	JTAG_CTI_EMU1
5	VCC3V3_CTI	15	JTAG_CTI_EMU_RSTN
6	NC	16	DGND
7	JTAG_CTI_TDO	17	NC
8	SEL_XDS110_INV	18	NC
9	CTI_RTCK	19	NC
10	DGND	20	DGND

Table 3-17. TI 60-pin Connector (J32) Pin-out

Pin No.	Signal	Pin No.	Signal
1	VCC3V3	31	MIPI_TRC_DAT06
2	MIPI_TMS	32	NC
3	MIPI_TCK	33	MIPI_TRC_DAT07
4	MIPI_TDO	34	NC
5	MIPI_TDI	35	MIPI_TRC_DAT08
6	MIPI_EMU_RSTn	36	NC
7	MIPI_RTCK	37	MIPI_TRC_DAT09
8	MIPI_TRSTN	38	JTAG_MIPI_EMU0_1V8
9	NC	39	MIPI_TRC_DAT10
10	NC	40	JTAG_MIPI_EMU1_1V8
11	NC	41	MIPI_TRC_DAT11
12	VCC1V8_MIPI	42	NC
13	MIPI_TRC_CLK	43	MIPI_TRC_DAT12
14	NC	44	NC
15	DGND	45	MIPI_TRC_DAT13
16	DGND	46	NC
17	MIPI_TRC_CTL	47	MIPI_TRC_DAT14
18	MIPI_TRC_DAT19	48	NC
19	MIPI_TRC_DAT00	49	MIPI_TRC_DAT15
20	MIPI_TRC_DAT20	50	NC
21	MIPI_TRC_DAT01	51	MIPI_TRC_DAT16
22	MIPI_TRC_DAT21	52	NC
23	MIPI_TRC_DAT02	53	MIPI_TRC_DAT17
24	MIPI_TRC_DAT22	54	NC
25	MIPI_TRC_DAT03	55	MIPI_TRC_DAT18
26	MIPI_TRC_DAT23	56	NC
27	MIPI_TRC_DAT04	57	DGND

Table 3-17. TI 60-pin Connector (J32) Pin-out (continued)

Pin No.	Signal	Pin No.	Signal
28	NC	58	SEL_XDS110_INV
29	MIPI_TRC_DAT05	59	NC
30	NC	60	NC

3.3.4.2.1 Test Automation

A test automation header J41 is provided to allow an external controller to control the power on/off boot modes, reset functionality, and current measurement to support automated testing. The test automation header includes four GPIOs and two I2C interfaces. The basic controls are listed in Table 3-18.

Table 3-18. List of Signals Routed to Test Automation Header

Signal	Signal Type	Function
POWER_DOWN	GPIO	Instructs the EVM to power down all circuits
POR	GPIO	Creates a PORz into the Maxwell
WARM_RESET	GPIO	Creates a RESETz into the Maxwell
GPIO1	GPIO	GPIO for communications with Maxwell
GPIO2	GPIO	GPIO for communications with Maxwell
GPIO3	GPIO	Used to Enable the BOOTMODE Buffer
GPIO4	GPIO	Used to Reset the Boot mode IO Expander
I2C	I2C	Communicates with boot mode I2C buffer
I2C2	I2C	Communicates with INA226 current measurement devices

One of the I2C interfaces from the test automation header is connected to an I2C I/O expander, which can drive the boot mode pins of the processor. The bootmode selection switches should be in the OFF condition. GPIO3 should be set to logic low to enable this mode.

The other I2C interface is connected to the current measurement and temperature sensing devices present on the I2C2 port of the SoC.

The test automation connector is used by Texas Instruments to control the software regression testing and comparative power measurements. The connector is provided to allow customers to develop their own testing and power measurements of customer applications. Power measurements are not a substitute for the AM65x Power Estimation Tool and should not be used for the design of power supply solutions. Power measurements vary based on silicon process and environment, and measurements should only be used for comparison with other measurements taken on the same EVM.

Table 3-19. Test Automation Header (J41) Pin-out

Pin no.	Signal	I/O Direction (to CP Board)
1	VCC3V3_1	Power (out)
2	VCC3V3_1	Power (out)
3	VCC3V3_1	Power (out)
4	NC	NA
5	NC	NA
6	NC	NA
7	DGND	Ground
8	NC	NA
9	NC	NA
10	NC	NA
11	NC	NA
12	NC	NA
13	NC	NA
14	NC	NA
15	NC	NA
16	DGND	Ground
17	NC	NA
18	NC	NA
19	NC	NA
20	NC	NA
21	NC	NA
22	NC	NA
23	NC	NA
24	NC	NA
25	DGND	Ground
26	TEST_POWERDOWN	Input
27	TEST_PORZn	Input
28	TEST_WARMRESETn	
Input		
29	NC	NA
30	TEST_GPIO1	Bidirectional
31	TEST_GPIO2	Bidirectional
32	TEST_GPIO3	Input
33	TEST_GPIO4	Input
34	DGND	Ground
35	NC	NA
36	SOC_I2C2_SCL	Bidirectional
37	BOOTMODE_I2C_SCL	Bidirectional
38	SOC_I2C2_SDA	Bidirectional
39	BOOTMODE_I2C_SDA	Bidirectional
40	DGND	Ground
41	DGND	Ground
42	DGND	Ground

3.3.4.3 UART Interface

Four UART ports of the SoC are interfaced with FT4232H for UART-to-USB functionality, and terminated on a micro B connector (J42) provided on the processor card. When the AM65x IDK is connected to a host using the provided USB cable, the computer can establish a virtual com port, which can be used with any terminal emulation application. The FT4232H is bus-powered. Virtual com port drivers for the FT4232H can be obtained from https://www.ftdichip.com/Products/ICs/FT4232H.htm.

Of the four UART ports of FT4232H, three are multiplexed; one with the application connector and the other two with test headers (J11 and J30). The control logic is given in Table 3-20.

Table 3-20. UART Selection Logic Table

UART Port	GPO Used From I2C Expander (U82)	S0	Selected Peripheral
MCU_UART0	MCU_UART_SEL	L	Test header
		H	FT4232
WKUP_UART0	WKUP_UART_SEL	L	Test header
		H	FT4232
MAIN_UART1	MAIN_UART1_SEL	L	FT4232
		H	Application connector

The test headers (J11 and J30) pin out is given in Table 3-21.

Table 3-21. UART Connectors (J11 and J30) Pin Out

Pin No.	MCU_UART0 J30	WKUP_UART0 J11
1	GND	GND
2	RTS	RTS
3	NC	NC
4	RX	RX
5	TX	TX
6	CTS	CTS

3.3.5 Memory Interfaces

3.3.5.1 DDR4 Interface

The common processor board has 4 GB of DDR4 using four 8-Gb x8bit wide memory devices arranged in an 32-bit wide bus. An additional 8-Gb x8bit wide memory device is provided to support seven bits of ECC. The DDR4 interface can operate up to 1600 MT/s speed. The DDR4 devices are connected using flyby routing for the address/command lines, and point-to-point connection for the data bus.

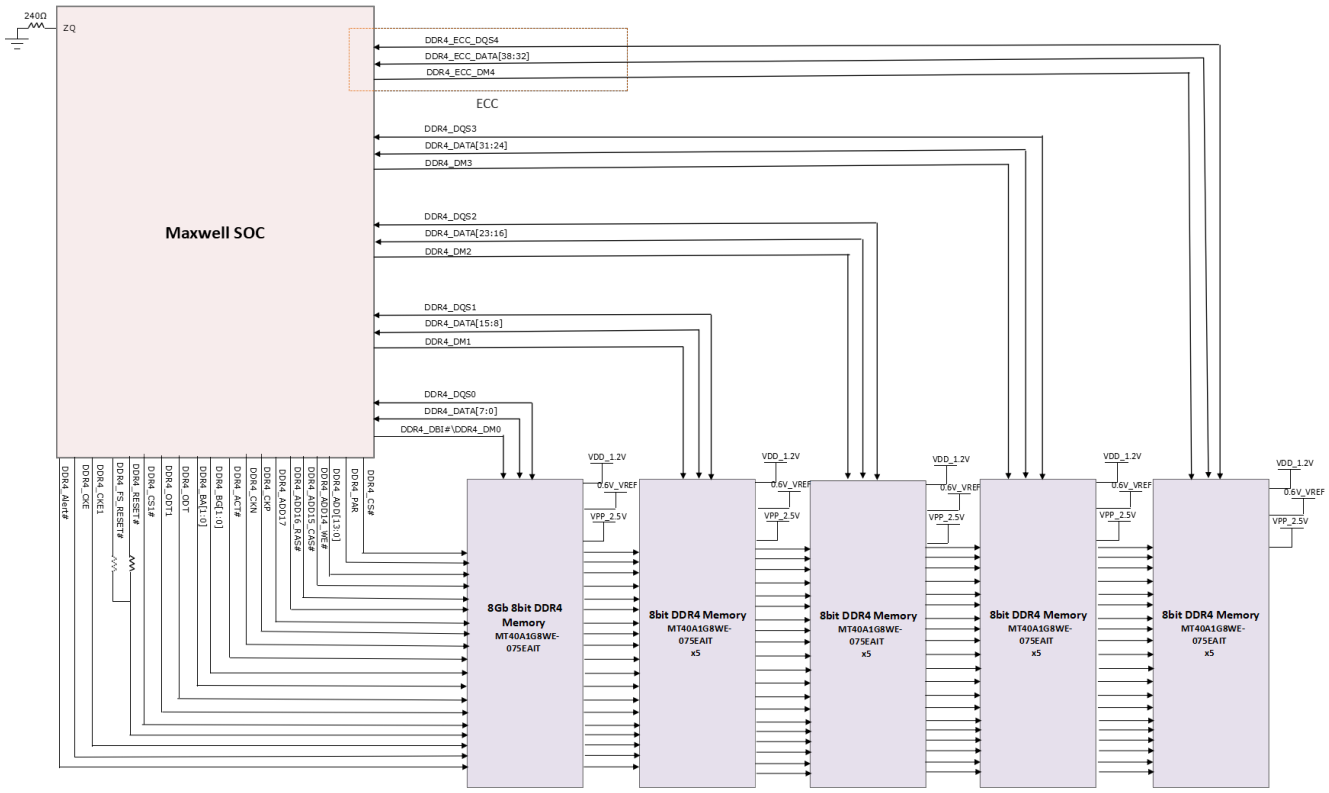

Figure 3-10. DDR4 Interface

3.3.5.2 MMC Interface

The AM65x processor provides two MMC interfaces: one is connected to eMMC flash, and other is used for SD card interface.

3.3.5.2.1 SDHC Interface

The processor card provides an SD card interface through a connector J17, connected to the MMC1 port of the AM65x processor. The SD card interface supports UHS1 operation, including I/O operations at both 1.8 V and 3.3 V. The I/O voltage is controlled using the internal SDIO_LDO, which provides the I/O voltage for the MMC1 port.

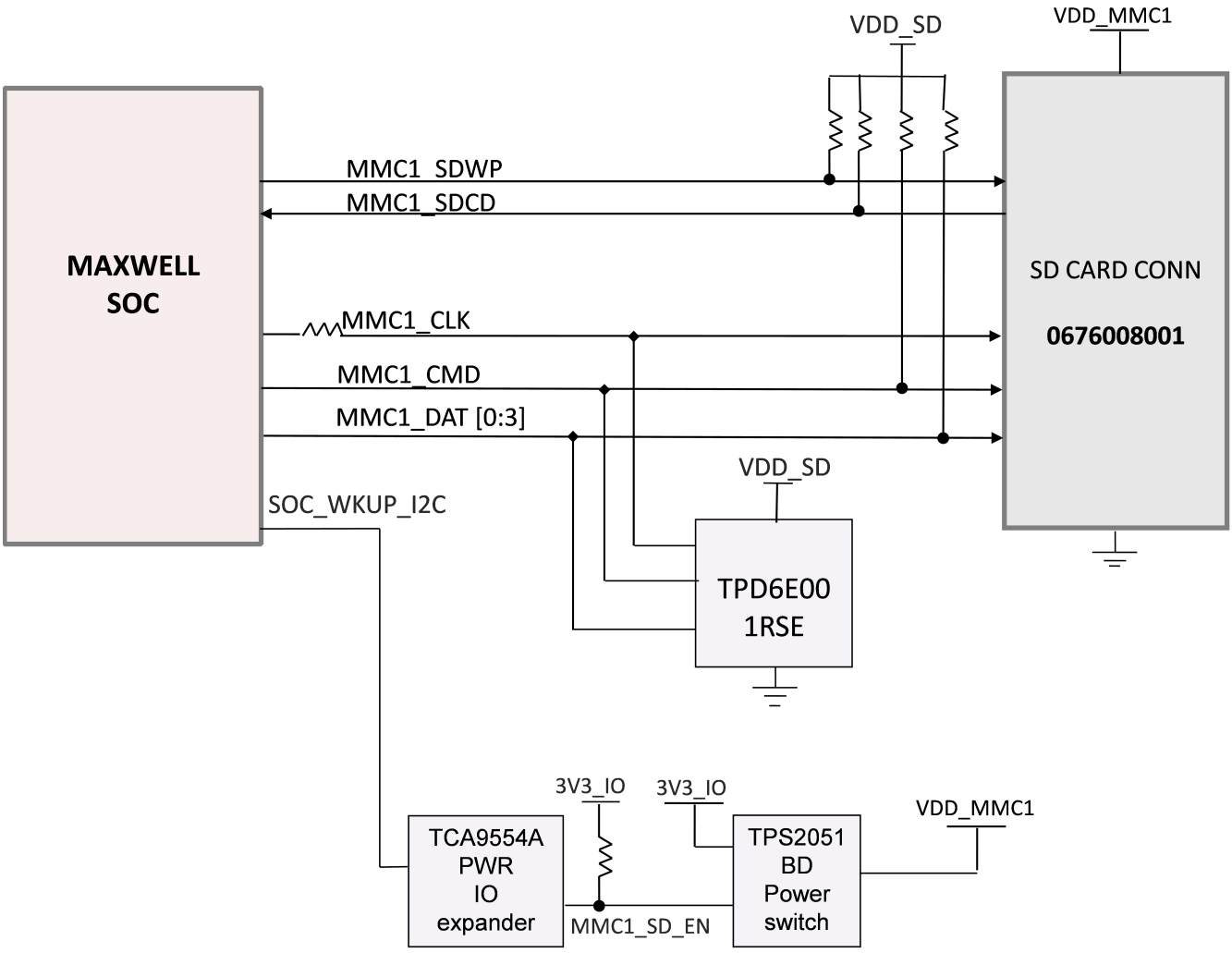

Figure 3-11. SDHC Interface

3.3.5.2.2 eMMC Interface

The processor card supports 16-GB eMMC flash memory (part number Micron MTFC16GAKAEJP-4M IT), connected to the MMC0 port of the AM65x processor. The flash is connected to 8bits of the MMC0 interface supporting HS400 double data rates up to 200 MHz.

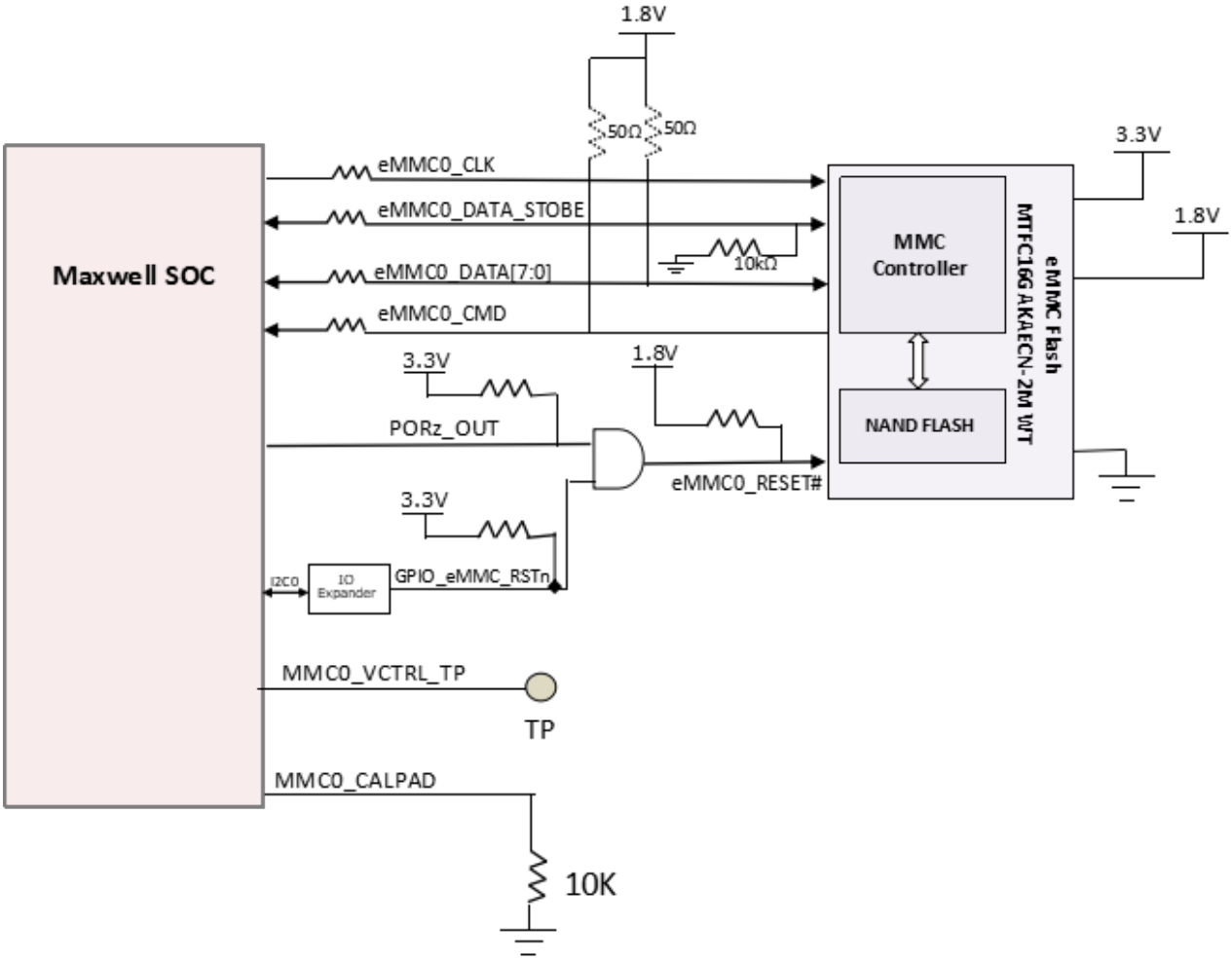

Figure 3-12. eMMC Interface

3.3.5.3 OSPI Interface

The processor card has a 512-Mbit OSPI memory device of part number MT35XU512ABA1G12-0SIT connected to the OSPI0 interface of the AM65x processor. The OSPI interface supports single and double data rates with memory speed up to 166-MHz SDR and 200-MHz DDR.

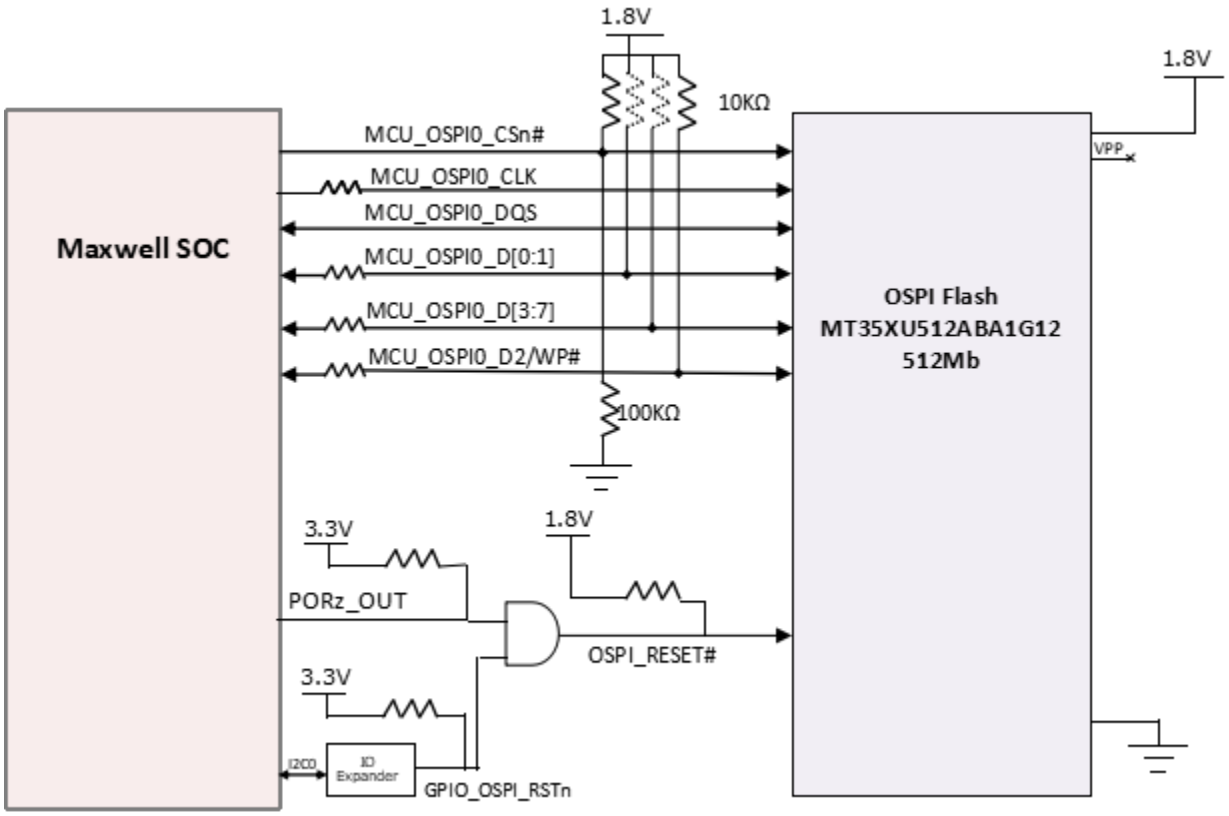

Figure 3-13. OSPI Interface

3.3.5.4 SPI NOR Flash Interface

A 128-Mbit SPI NOR Flash of part number MT25QL128ABA8E12 is interfaced to the SPI0 port of the AM65x processor. In addition, SPI0 is also connected to the application connector and test automation header. SPI_CS0 and SPI_CS1 chip select signals are used for the serial flash and application connector, respectively.

3.3.5.5 Board ID EEPROM Interface

The AM65x processor card is identified by its version and serial number, which are stored in the onboard EEPROM. The EEPROM is accessible on the address 0x50.

The AM65x CP board includes a CAT24C256W I2C EEPROM ID memory. The first 259 bytes of addressable EEPROM memory are preprogrammed with identification information for each board. The remaining 32509 bytes are available to the user for data or code storage.

Table 3-22. Board ID Memory Header Information

Header	Field Name	Size (bytes)	Comments
EE3355AA	MAGIC	4	Magic number
	TYPE	1	Fixed length and variable position board ID header
		2	Size of payload
BRD_INFO	TYPE	1	payload type
	Length	2	offset to next header

Table 3-22. Board ID Memory Header Information (continued)

Header	Field Name	Size (bytes)	Comments
	Board_Name	16	Name of the board
	Design_Rev	2	Revision number of the design
	PROC_Nbr	4	PROC number
	Variant	2	Design variant number
	PCB_Rev	2	Revision number of the PCB
	SCHBOM_Rev	2	Revision number of the schematic
	SWR_Rev	2	first software release number
	VendorID	2	
	Build_Week	2	week of the year of production
	Build_Year	2	year of production
	BoardID	6	
	Serial_Nbr	4	incrementing board number
DDR_INFO	TYPE	1	
	Length	2	offset to next header
	DDR control	2	DDR Control Word
MAC_ADDR	TYPE	1	payload type
	Length	2	Size of payload
	MAC control	2	MAC header control word
	MAC_adrs	192	MAC adress of AM65x PRG2
END_LIST	TYPE	1	End Marker

3.3.5.6 Boot EEPROM Interface

A 256-Kbit EEPROM is interfaced to WKUP_I2C for booting. Earlier versions of the board had this memory address set to 0x54. Later versions have the address set to 0x52.

3.3.6 Ethernet Interface

The AM65x EVM includes an RGMII connection between the DP83867 Gigabit Ethernet PHY and the network subsystem (NSS) of the processor. One RGMII interface (connected to RJ45 connector J12) from the MCU domain and two RGMII ports (connected to stacked RJ45 connector J14A and J14B) from ICSSG (PRG2) domain of the AM65x processor are used.

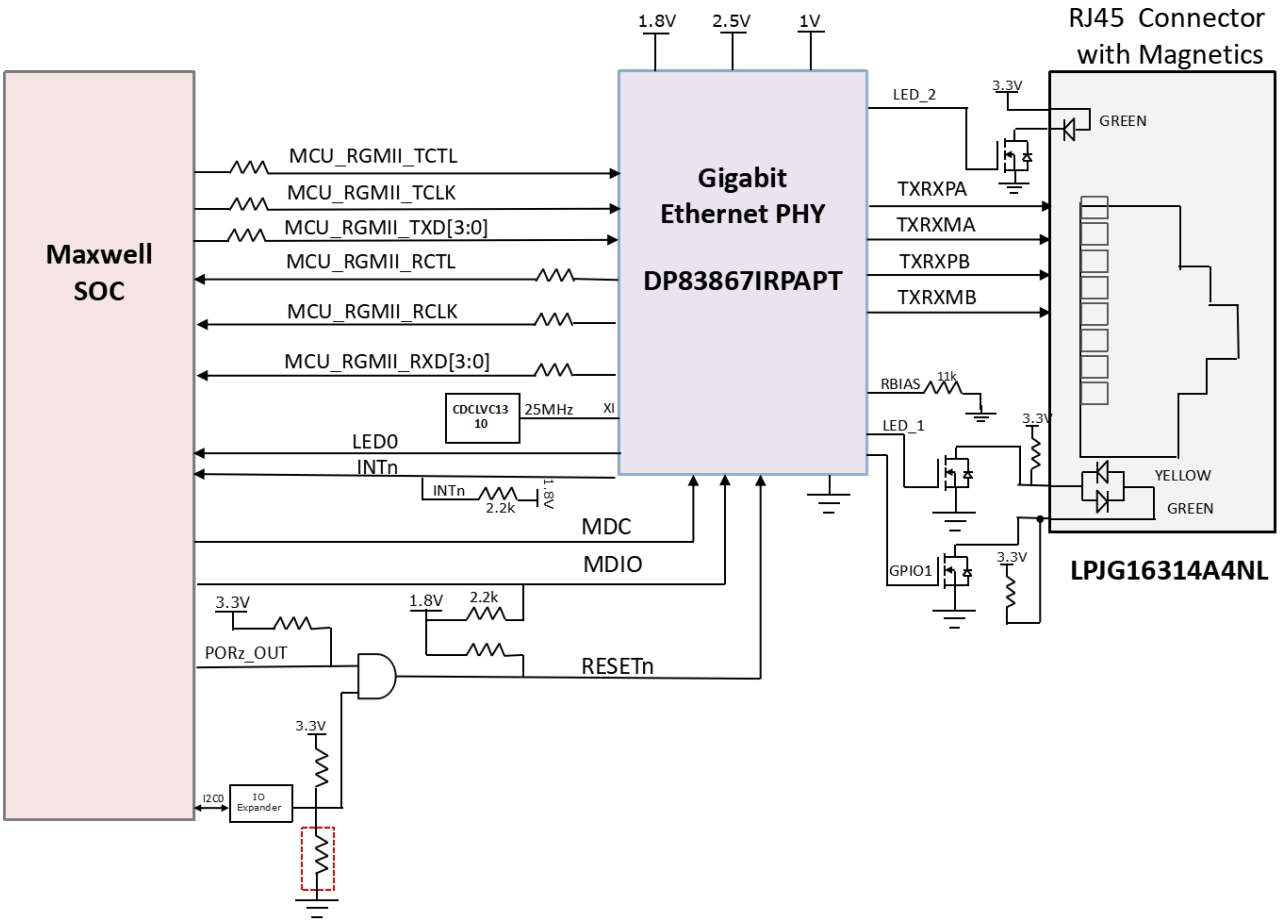

Figure 3-14. Ethernet Interface – MCU Domain

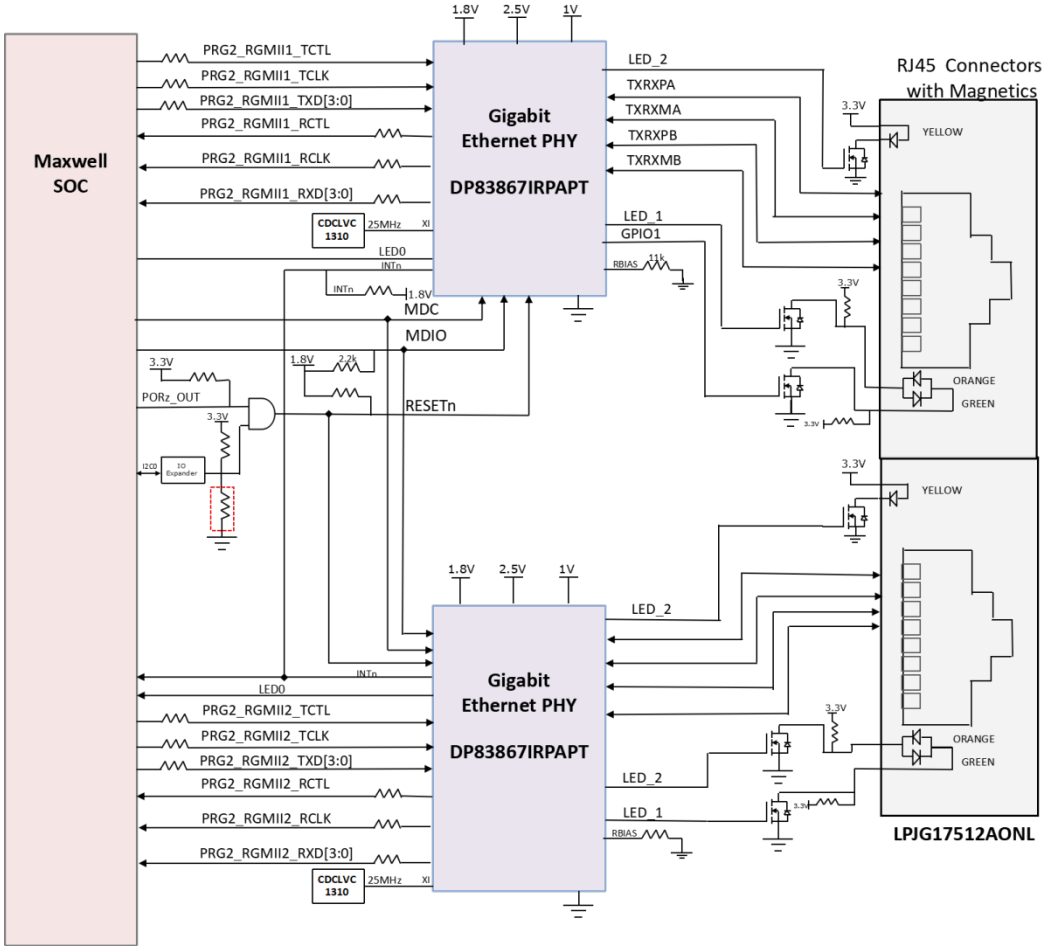

Figure 3-15. Ethernet Interface – ICSSG Domain

3.3.6.1 Gigabit Ethernet PHY Default Configuration

The default configuration of the DP83867 is determined using a number of resistor pull-up and pull-down values on specific pins of the PHY. Depending on the values installed, each of the configuration pins can be set to one of four modes by using the pull-up and pull-down options provided. The AM65x IDK uses the 48-pin QFN package, designated with the RGZ suffix, which only supports the RGMII interface.

The DP83867 PHY uses four level configurations based on resistor strapping, which generate four distinct voltage ranges. The resistors are connected to the RX data and control pins, which are normally driven by the PHY and are inputs to the processor. The voltage range for each mode is shown below:

Mode 1 - 0 V to 0.1764 V

Mode 2 – 0.252 V to 0.3438 V

Mode 3 – 0.405 V to 0.5112 V

Mode 4 – 1.2492 V to 1.5984 V

Default configurations of all phys are mentioned in Table 3-23.

Table 3-23. Default Strap Setting of Ethernet PHYs

	Signal	Mode	Default Configuration		Configuration	Description
			Pull Up	Pull Down		
PRG2 RGMII1 PHY (J14A)	RX_D0	1	Open	Open	PHY_AD1 = 0 and PHY_AD0 = 0	Address of the PHY is set to 00000
	RX_D2	1	Open	Open	PHY_AD3 = 0 and PHY_AD2 = 0	
	RX_DV/ RX_CTRL	1	Open	Open	N/A	N/A
	LED_2	1	Open	Open	RGMII Clock Skew TX[1]=0 and RGMII Clock Skew TX[0]=0	RGMII Clock Skew TX = 2 ns and advertise
	LED_1	1	Open	Open	ANEG_SEL=0 and RGMII Clock Skew TX[1]=0	
	GPIO_0	1	Open	Open	RGMII Clock Skew RX[0]=0	RGMII Clock Skew RX = 2 ns
	GPIO_1	1	Open	Open	RGMII Clock Skew RX[2]=0 and RGMII Clock Skew RX[1]=0	
PRG2 RGMII1 PHY (J14B)	RX_D0	4	2.49K	Open	PHY_AD1 = 1 and PHY_AD0 = 1	Address of the PHY is set to 00011
	RX_D2	1	Open	Open	PHY_AD3 = 0 and PHY_AD2 = 0	
	RX_DV/ RX_CTRL	1	Open	Open	N/A	N/A
	LED_2	1	Open	Open	RGMII Clock Skew TX[1]=0 and RGMII Clock Skew TX[0]=0	RGMII Clock Skew TX = 2 ns and advertise
	LED_1	1	Open	Open	ANEG_SEL=0 and RGMII Clock Skew TX[1]=0	
	GPIO_0	1	Open	Open	RGMII Clock Skew RX[0]=0	RGMII Clock Skew RX = 2 ns
	GPIO_1	1	Open	Open	RGMII Clock Skew RX[2]=0 and RGMII Clock Skew RX[1]=0	
PRG2 RGMII1 PHY (J12)	RX_D0	1	Open	Open	PHY_AD1 = 0 and PHY_AD0 = 0	Address of the PHY is set to 00000
	RX_D2	1	Open	Open	PHY_AD3 = 0 and AN2 = 0	
	RX_DV/ RX_CTRL	1	Open	Open	N/A	N/A
	LED_2	1	Open	Open	RGMII Clock Skew TX[1]=0 and RGMII Clock Skew TX[0]=0	RGMII Clock Skew TX = 2 ns and advertise
	LED_1	1	Open	Open	ANEG_SEL=0 and RGMII Clock Skew TX[1]=0	
	GPIO_0	1	Open	Open	RGMII Clock Skew RX[0]=0	RGMII Clock Skew RX = 2 ns
	GPIO_1	1	Open	Open	RGMII Clock Skew RX[2]=0 and RGMII Clock Skew RX[1]=0	

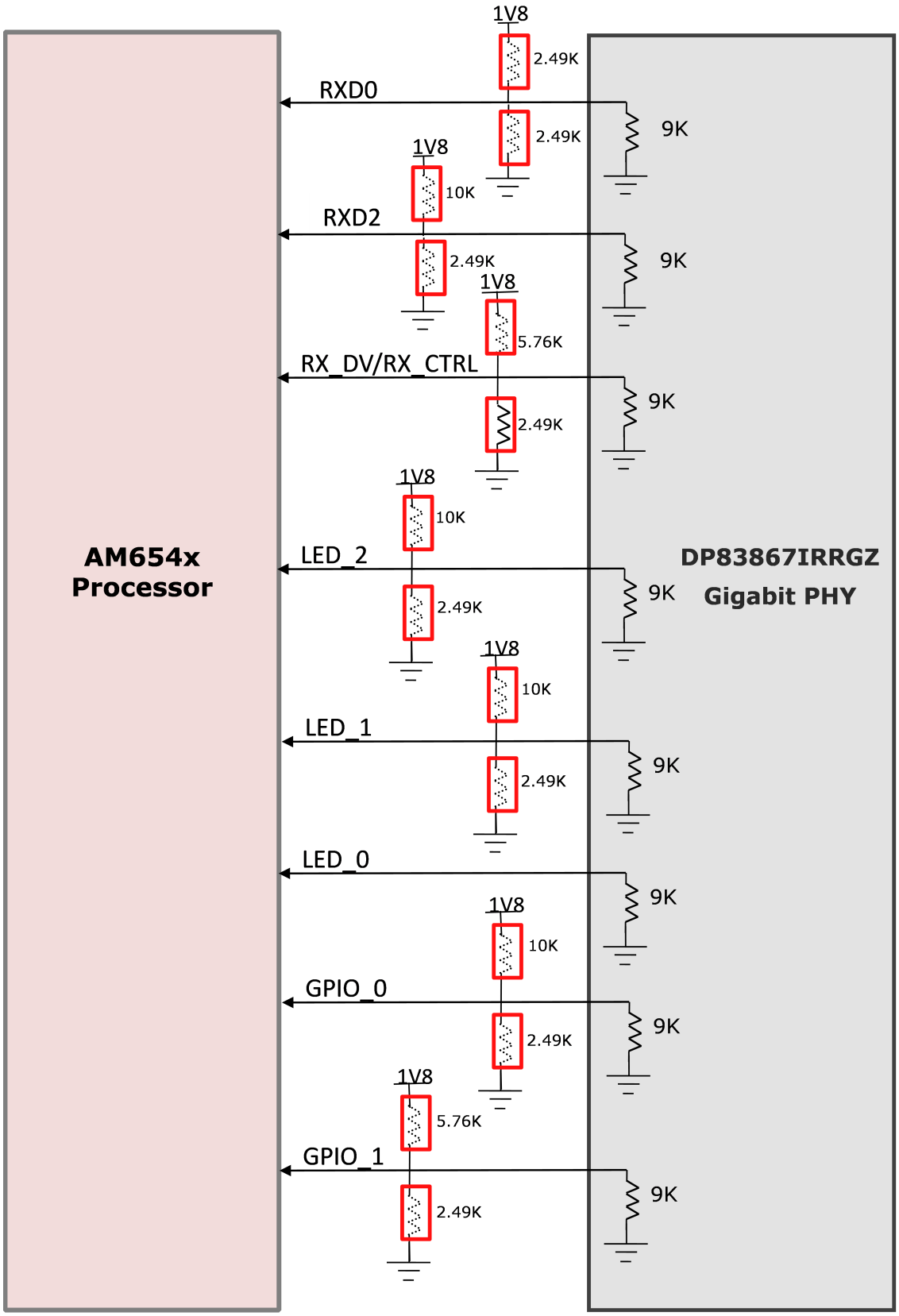

Figure 3-16. Strapping Diagram for MCU and PRG2-RGMII1 Ethernets

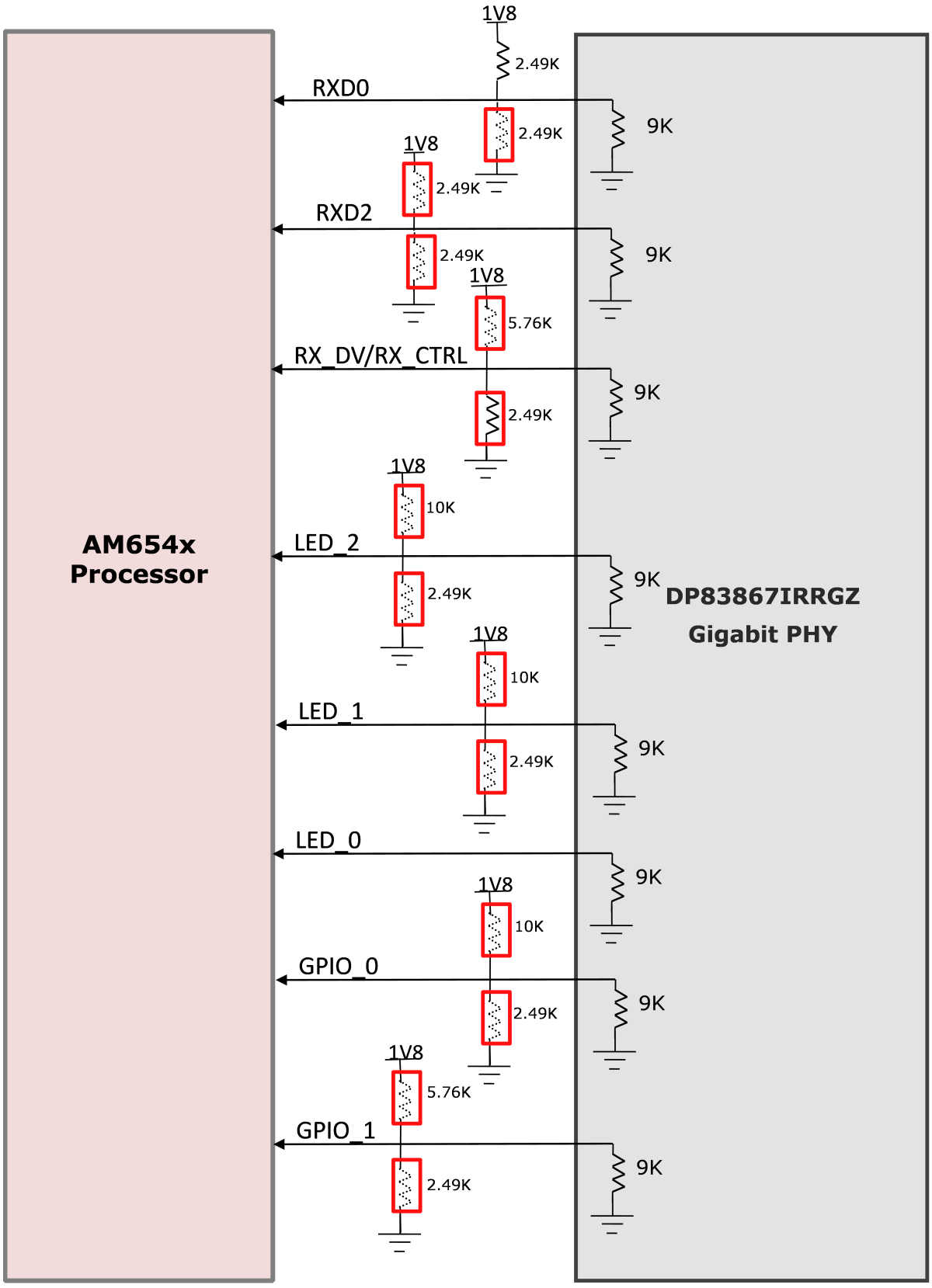

Figure 3-17. Strapping Diagram for PRG2-RGMII2 Ethernet

Note

Resistors which are highlighted in red color boxes are DNI components.

3.3.6.2 Ethernet LEDs

The common processor card has LEDs to indicate the status of the Ethernet link. Some of the LEDs on the CP board are used for industrial applications; those can be controlled with I2C0 of the processor, which is connected to an I/O expander and some processor GPOs.

From the Ethernet PHY, LED1 and GPIO0 are connected to dual LEDs of RJ45 to indicate a 10/100-Mb or 1000-Mb link. The green LED indicates 10/100-Mb speed, and the orange LED indicates 1000-Mb speed.

LED2 is connected to RJ45 LED (Yellow) to indicate transmit/receive activity.

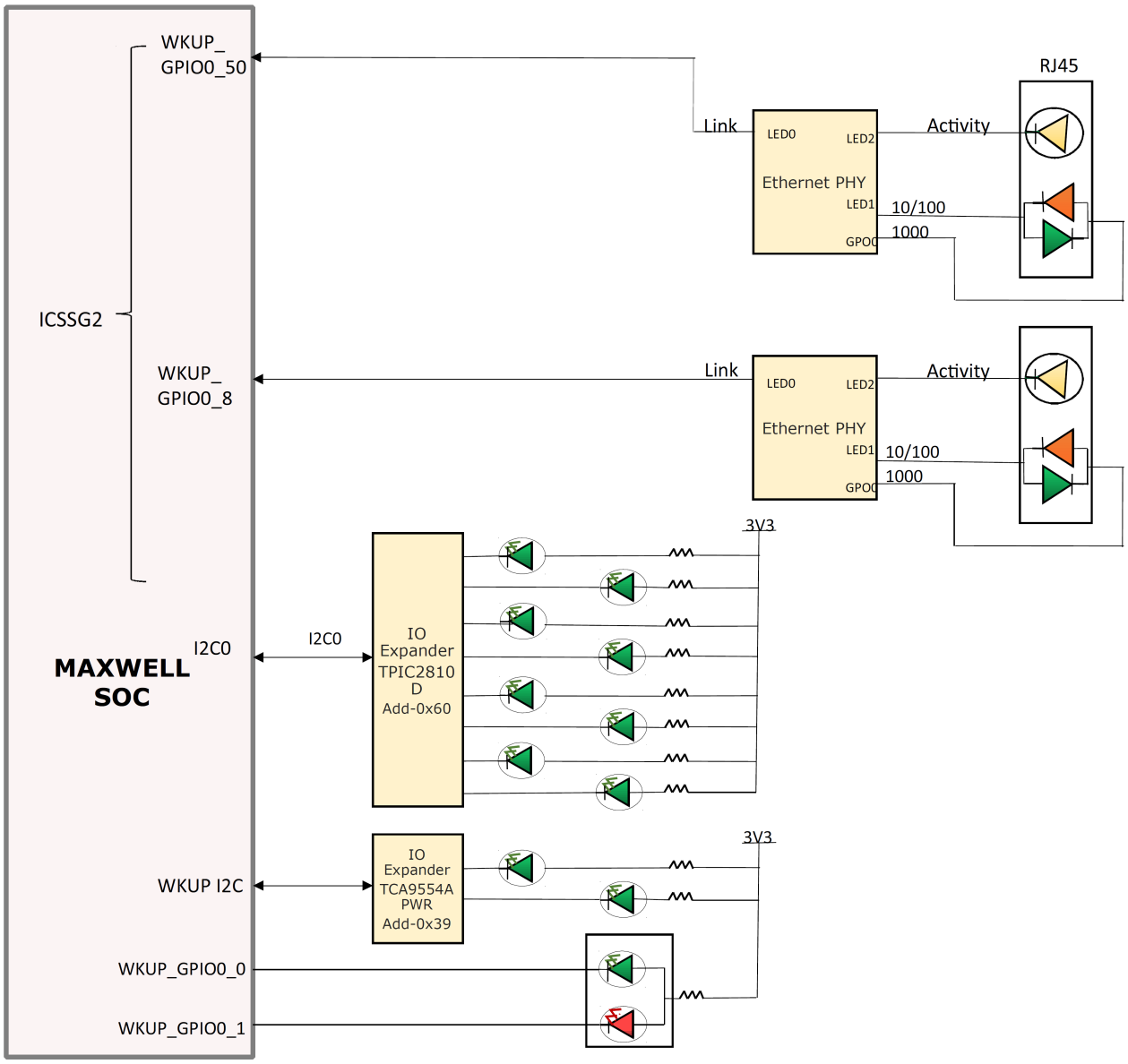

Figure 3-18. CP Board Ethernet Interface – LEDs

3.3.7 LCD Display Interface

The processor board provides a common display interface terminated to the I-PEX connector J38 of part number 20720-040E-02. It is a 0.5-mm pitch Shielded FFC / FPC connector. The PWM output signal from the AM65x processor is terminated to the I-PEX connector, which is used to drive the back-light circuit in the adapter card.

Table 3-24. Display Connector (J38) Pin-out

Pin no.	Signal	Direction
1	VCC_5V0	Power
2	VCC_5V0	Power
3	VCC_5V0	Power
4	VCC3V3_IO	Power
5	VCC3V3_IO	Power
6	DGND	Power
7	DGND	Power
8	OLDI0_A0N	Output
9	OLDI0_A0P	Output
10	DGND	Power
11	OLDI0_A1N	Output
12	OLDI0_A1P	Output
13	DGND	Power
14	OLDI0_A2N	Output
15	OLDI0_A2P	Output
16	DGND	Power
17	OLDI0_A3N	Output
18	OLDI0_A3P	Output
19	DGND	Power
20	OLDI0_CLKN	Output
21	OLDI0_CLKP	Output
22	DGND	Power
23	SOC_WKUP_SCL	Output
24	SOC_WKUP_SDA	Bidirectional
25	DGND	Power
26	SOC_I2C1_SCL	Output
27	SOC_I2C1_SDA	Bidirectional
28	DGND	Power
29	LCD_BRD_TOUCH_INT	Input
30	LCD_DISPLAY_EN/BRD_RSTN	Output
31	CARD ID_LCD_A0	Output
32	SOC_SPI1_CLK	Output
33	SOC_SPI1_CS0	Output
34	CARD ID_LCD_A1	Output
35	SOC_SPI1_MOSI	Output
36	SOC_SPI1_MISO	Input
37	CARD ID_LCD_A2	Output
38	ECAP0_IN_APWM0_OUT	Output
39	LCD_TOUCH_RESETN	Output
40	LCD_BRD_DET	Input

3.3.8 USB 2.0 Interface

The SoC supports two USB 2.0 ports – USB0 and USB1. The USB0 port is routed to the SERDES daughter card connector along with USB0 ID pins and DRVVBUS0 for host / slave detect and power enable. The USB1 port is terminated to a uAB connector (J3) and supports both host and slave mode. In the host mode, up to 500 mA, 5 V is supported for the slave device. A power switch is included which is controlled by DRV_VBUS signal from the AM65x processor. A 2x3 header (J4) is provided to install the 2-position ganged shunt to configure the port for host mode, as shown in Figure 3-19. Place the shunt on pin 1 and 2 to enable bulk capacitance on VBUS, and place the shunt on pin 5 and 6 to connect ID pin to ground.

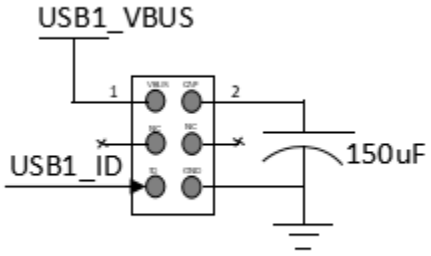

Figure 3-19. J4 Header for USB2.0 Host Interface

3.3.9 CSI-2 Interface

The CSI-2 interface from the AM65x processor is terminated to two camera connectors to interface a CSI-2 standard camera:

- J22 – 40-pin Samtec connector, which is referenced from OV490 / OV10640 Combo Module
- J39 – 36-pin Molex connector, which is referred from Leopard Imaging CPI (VIN) Connector

The two connectors match the existing standards for camera cards. The CSI-2 connector on the board is selected based on the camera module installed. MCU_I2C0 and MCU_SPI0 are also connected to the camera connector through level translators.

The control signals connected to J39 are all 1.8 V, whereas the control signals connected to J22 can be either 1.8 V or 3.3 V. A jumper (J37) is used to select the required I/O voltage, as shown in Figure 3-20. Short Pin 1 and Pin 2 for 1.8-V I/O operation, or Short Pin 2 and Pin 3 for 3.3-V I/O operation. The footprint to mount the oscillator of part number KC2520B24.0000C1GE00 is provided to supply 24-MHz REFCLK to the CSI-2 module. Mount U114 for 1.8-V REFCLK, and mount U112 for 3.3-V REFCLK.

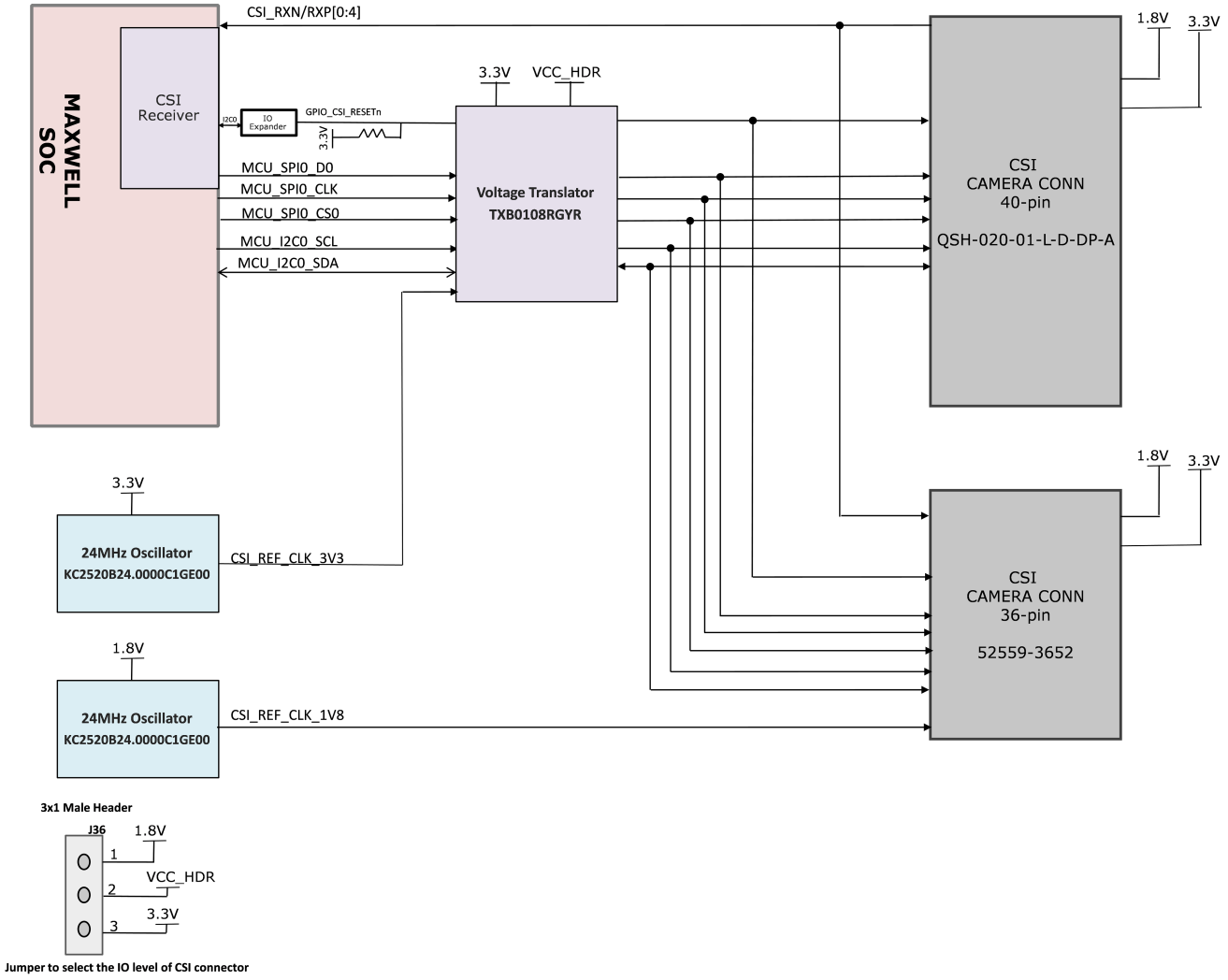

Figure 3-20. CSI Interface

Table 3-25. CSI-2 Samtec Connector (J22) Pin-out

Pin Number	CP Card Signals-CSI	Direction
1	NC	NA
2	CSI_MCU_SCL	Output
3	NC	NA
4	CSI_MCU_SDA	Bidirectional
5	CSI0_RXP0	Input
6	NC	NA
7	CSI0_RXN0	Input
8	NC	NA
9	CSI0_RXP1	Input
10	CSI_REF_CLK	Output
11	CSI0_RXN1	Input
12	DGND	Power
13	CSI0_RXP2	Input
14	CSI_RESETN	Output
15	CSI0_RXN2	Input
16	DGND	Power

Table 3-25. CSI-2 Samtec Connector (J22) Pin-out (continued)

Pin Number	CP Card Signals-CSI	Direction
17	CSI0_RXP3	Input
18	CSI_MCU_SPI0_D0	Output
19	CSI0_RXN3	Input
20	CSI_MCU_SPI0_CLK	Output
21	CSI0_RXP4	Input
22	CSI_MCU_SPI0_CS0	Output
23	CSI0_RXN4	Input
24	DGND	Power
25	NC	NA
26	NC	NA
27	NC	NA
28	NC	NA
29	NC	NA
30	VCC3V3_IO	Power
31	NC	NA
32	VCC3V3_IO	Power
33	NC	NA
34	VCC3V3_IO	Power
35	NC	NA
36	VCC3V3_IO	Power
37	NC	NA
38	VCC1V8	Power
39	NC	NA
40	VCC1V8	DGND

Table 3-26. CSI-2 Molex Connector (J39) Pin-out

Pin Number	CP Card Signals-CSI	Direction
1	VCC3V3_IO	Power
2	VCC3V3_IO	Power
3	VCC3V3_IO	Power
4	VCC1V8	Power
5	VCC1V8	Power
6	DGND	DGND
7	DGND	NC
8	CSI0_RXP0	Input
9	CSI0_RXN0	Input
10	DGND	Power
11	CSI0_RXP1	Input
12	CSI0_RXN1	Input
13	DGND	Power
14	CSI0_RXP2	Input
15	CSI0_RXN2	Input
16	DGND	Power
17	CSI0_RXP3	Input
18	CSI0_RXN3	Input
19	DGND	Power
20	CSI0_RXP4	Input

Table 3-26. CSI-2 Molex Connector (J39) Pin-out (continued)

Pin Number	CP Card Signals-CSI	Direction
21	CSI0_RXN4	Input
22	DGND	Power
23	CSI_RESETN	Output
24	CSI_MCU_SDA	Bidirectional
25	CSI_MCU_SCL	Output
26	CSI_REF_CLK_1V8	Output
27	NC	NA
28	NC	NA
29	DGND	Power
30	CSI_MCU_SPI0_D0	Output
31	CSI_MCU_SPI0_CLK	Output
32	CSI_MCU_SPI0_CS0	Output
33	DGND	Power
34	DGND	Power
35	NC	NA
36	NC	NA

3.3.10 Application Card Interface

The common processor card includes an application connector to interface different pin-multiplexed functions of the PRG0 and PRG1 I/O groups of the AM65x processor. The main purpose of the application card is to highlight the industrial capabilities of the AM65x processor. All the signals associated with the PRG0 and PRG1 interface are routed to the application connector.

The interfaces provided on the application connector are RGMII, UART, MCAN, I2C, SPI, McASP, ADC, and PWM signals. The PRG0 signals are multiplexed with the McASP1 signals of the HDMI/GPMC card. Resistor options are provided to allow for the selection of the required interface, as shown in Figure 3-21. Table 3-27 lists the resistors that are mounted or demounted to select RGMII signals on the application connector.

Table 3-27. Selection of PRG0 Signals on the Application Connector

Refdes	Application Connector	HDMI/GPMC Expansion Connector
R570	Mount	DNI
R589	Mount	DNI
R576	Mount	DNI
R580	Mount	DNI
R578	Mount	DNI
R574	Mount	DNI
R572	Mount	DNI
R587	Mount	DNI
R569	DNI	Mount
R590	DNI	Mount
R575	DNI	Mount
R579	DNI	Mount
R577	DNI	Mount
R573	DNI	Mount
R571	DNI	Mount
R588	DNI	Mount

Figure 3-21. Multiplexed RGMII/McASP1 Signal Selection

The card presence detect signal from the application card is connected to the I/O expander, which in turn is connected to the WKUP I2C0 port of the AM65x processor.

The 120-pin connector pin-out is given in Table 3-28.

Table 3-28. 120-pin Application Connector (J18) Pin-out

Pin Number	CP Card Signals	IDK Card Signals	Direction
1	DGND	DGND	Power
2	DGND	DGND	Power
3	PRG1_RGMII1_ETH1_CLK	ETH0_CLK	Output
4	PRG0_RGMII1_ETH1_CLK	ETH1_CLK	Output
5	DGND	DGND	Power
6	DGND	DGND	Power
7	PRG0_PRU0GPO15	ETH0_RGMII_TD3	Output
8	APP_PRG0_PRU1GPO5	NC	NA
9	PRG0_PRU0GPO13	ETH0_RGMII_TD1	Output
10	APP_PRG0_PRU0GPO17	ETH_LED1	Output
11	PRG0_PRU0GPO14	ETH0_RGMII_TD2	Output
12	PRG0_PRU0GPO19	ETH_LED3	Output
13	PRG0_PRU0GPO11	ETH0_RGMII_TX_CTL	Output
14	PRG0_PRU0GPO18	PRG0_IEP0_LATCH_IN0	Input
15	PRG0_PRU0GPO12	ETH0_RGMII_TD0	Output
16	PRG0_PRU0GPO7	ETH0_LED_LINK	Input
17	DGND	DGND	Power

Table 3-28. 120-pin Application Connector (J18) Pin-out (continued)

Pin Number	CP Card Signals	IDK Card Signals	Direction
18	PRG0_PRU0GPO10	ETH0/1_INTN	Input
19	APP_PRG0_PRU0GPO16	ETH0_RGMII_TXC	Output
20	PRG0_PRU0GPO8	NC	NA
21	DGND	DGND	Power
22	PRG0_PRU1GPO8	NC	NA
23	PRG0_PRU0GPO3	ETH0_RGMII_RD3	Input
24	PRG0_PRU1GPO17	ETH_LED2	Output
25	DGND	DGND	Power
26	APP_PRG0_PRU1GPO4	ETH1_RGMII_RX_CTL	Input
27	PRG0_PRU0GPO6	ETH0_RGMII_RXC	Input
28	APP_PRG0_PRU1GPO3	ETH1_RGMII_RD3	Input
29	DGND	DGND	Power
30	APP_PRG0_PRU1GPO0	ETH1_RGMII_RD0	Input
31	PRG0_PRU0GPO4	ETH0_RGMII_RX_CTL	Input
32	APP_PRG0_PRU1GPO2	ETH1_RGMII_RD2	Input
33	PRG0_PRU0GPO2	ETH0_RGMII_RD2	Input
34	APP_PRG0_PRU1GPO1	ETH1_RGMII_RD1	Input
35	PRG0_PRU0GPO0	ETH0_RGMII_RD0	Input
36	DGND	DGND	Power
37	PRG0_PRU0GPO5	NC	NA
38	PRG0_PRU1GPO16	ETH1_RGMII_TXC	Output
39	PRG0_PRU0GPO1	ETH0_RGMII_RD1	Input
40	DGND	DGND	Power
41	PRG0_PRU1GPO7	ETH1_LED_LINK	Input
42	PRG0_PRU1GPO15	ETH1_RGMII_TD3	Output
43	PRG0_PRU0GPO9	GPIO_ETH2/3_RESETN	Input
44	PRG0_PRU1GPO14	ETH1_RGMII_TD2	Output
45	PRG0_PRU1GPO9	GPIO_ETH0/1_RESETN	Input
46	PRG0_PRU1GPO13	ETH1_RGMII_TD1	Output
47	PRG0_PRU1GPO19	ETH_LED4	Output
48	PRG0_PRU1GPO11	ETH1_RGMII_TX_CTL	Output
49	PRG0_PRU1GPO10	ETH2/3_INTN	Input
50	PRG0_PRU1GPO12	ETH1_RGMII_TD0	Output
51	PRG0_PRU1GPO18	PRG0_IEP1_LATCH_IN0	Input
52	DGND	DGND	Power
53	PRG0_MDIODATA	ETH0/1_MDIO	Bidirectional
54	PRG0_PRU1GPO6	ETH1_RGMII_RXC	input
55	PRG1_PRU1GPO5	NC	NA
56	DGND	DGND	Power
57	PRG1_PRU1GPO8	NC	NA
58	PRG1_PRU0GPO8	NC	NA
59	PRG0_MDIOMDCLK	ETH0/1_MDC	Output
60	PRG1_PRU0GPO5	NC	NA
61	PRG1_PRU1GPO10	RS485_UART_TX	Output
62	PRG1_PRU0GPO9	IDK_IOEXP_LDN_1V8	Output
63	PRG1_PRU1GPO0	ETH3_RGMII_RD0	Input
64	PRG1_PRU1GPO9	RS485_UART_RX	Input

Table 3-28. 120-pin Application Connector (J18) Pin-out (continued)

Pin Number	CP Card Signals	IDK Card Signals	Direction
65	PRG1_PRU1GPO4	ETH3_RGMII_RX_CTL	Input
66	PRG1_PRU0GPO7	ETH2_LED_LINK	Input
67	PRG1_PRU1GPO1	ETH3_RGMII_RD1	Input
68	PRG1_PRU0GPO19	ETH_LED7	Output
69	DGND	DGND	Power
70	PRG1_PRU0GPO17	ETH_LED5	Output
71	PRG1_PRU1GPO6	ETH3_RGMII_RXC	Input
72	PRG1_PRU0GPO18	PRG1_IEP0_LATCH_IN0	Input
73	DGND	DGND	Power
74	PRG1_PRU0GPO10	RS485_UART_RTSN	Output
75	PRG1_PRU1GPO3	ETH3_RGMII_RD3	Input
76	PRG1_PRU0GPO1	ETH2_RGMII_RD1	Input
77	PRG1_PRU1GPO2	ETH3_RGMII_RD2	Input
78	PRG1_PRU0GPO4	ETH2_RGMII_RX_CTL	Input
79	PRG1_PRU1GPO12	ETH3_RGMII_TD0	Output
80	PRG1_PRU0GPO2	ETH2_RGMII_RD2	Input
81	PRG1_PRU1GPO11	ETH3_RGMII_TX_CTL	Output
82	DGND	DGND	Power
83	PRG1_PRU1GPO15	ETH3_RGMII_TD3	Output
84	PRG1_PRU0GPO6	ETH2_RGMII_RXC	Input
85	DGND	DGND	Power
86	DGND	DGND	Power
87	PRG1_PRU1GPO16	ETH3_RGMII_TXC	Output
88	PRG1_PRU0GPO0	ETH2_RGMII_RD0	Input
89	DGND	DGND	Power
90	PRG1_PRU0GPO3	ETH2_RGMII_RD3	Input
91	PRG1_PRU1GPO13	ETH3_RGMII_TD1	Output
92	DGND	DGND	Power
93	PRG1_PRU1GPO14	ETH3_RGMII_TD2	Output
94	PRG1_PRU0GPO16	ETH2_RGMII_TXC	Output
95	PRG1_MDIOMDCLK	ETH2/3_MDC	Output
96	DGND	DGND	Power
97	DGND	DGND	Power
98	PRG1_PRU0GPO11	ETH2_RGMII_TX_CTL	Output
99	PRG1_MDIODATA	ETH2/3_MDIO	Bidirectional
100	PRG1_PRU0GPO14	ETH2_RGMII_TD2	Output
101	DGND	DGND	Power
102	PRG1_PRU0GPO15	ETH2_RGMII_TD3	Output
103	PRG1_RGMII2_ETH2_CLK	ETH3_CLK	Output
104	DGND	DGND	Power
105	DGND	DGND	Power
106	PRG0_RGMII2_ETH2_CLK	ETH2_CLK	Output
107	DGND	DGND	Power
108	DGND	DGND	Power
109	DGND	DGND	Power
110	PRG1_PRU0GPO12	ETH2_RGMII_TD0	Output
111	DGND	DGND	Power

Table 3-28. 120-pin Application Connector (J18) Pin-out (continued)

Pin Number	CP Card Signals	IDK Card Signals	Direction
112	DGND	DGND	Power
113	APP_CARD_PSTN	DGND	Input
114	PRG1_PRU0GPO13	ETH2_RGMII_TD1	Output
115	DGND	DGND	Power
116	DGND	DGND	Power
117	DGND	DGND	Power
118	DGND	DGND	Power
119	DGND	DGND	Power
120	DGND	DGND	Power

Table 3-29. 60-pin Application Connector (J16) Pin-out

Pin No.	CP Card Signals	IDK Card Signals	Direction
1	VCC3V3_IO	VCC_3V3	Power
2	VCC_5V0	VCC_5V0	Power
3	VCC3V3_IO	VCC_3V3	Power
4	VCC_5V0	VCC_5V0	Power
5	VCC3V3_IO	VCC_3V3	Power
6	VCC_5V0	VCC_5V0	Power
7	NC	NC	NA
8	NC	NC	NA
9	NC	NC	NA
10	NC	NC	NA
11	NC	NC	NA
12	NC	NC	NA
13	DGND	DGND	Power
14	NC	NC	NA
15	SOC_WKUP_SCL	EEPROM_I2C_SCL	Output
16	NC	NC	NA
17	SOC_WKUP_SDA	EEPROM_I2C_SDA	Bidirectional
18	DGND	DGND	Power
19	DGND	DGND	Power
20	SOC_SPI0_CLK	IDK_SPI_CLK_3V3	Output
21	SOC_I2C0_SCL	IDK_I2C_SCL_C	Output
22	DGND	DGND	Power
23	SOC_I2C0_SDA	IDK_I2C_SDA_C	Bidirectional
24	SOC_SPI0_CS1	IDK_SPI_CSN_3V3	Output
25	DGND	DGND	Power
26	SOC_SPI0_D0	NC	NA
27	UART1_CTS	PRG1_IEP1_LATCH_IN0	Output
28	SOC_SPI0_D1	IDK_SPI_MISO_3V3	Input
29	UART1_RTS	ETH_LED8	Output
30	MCU_MCAN0_TX	CAN0_TX	Output
31	UART1_RX	ETH_LED6	Output
32	MCU_MCAN0_RX	CAN0_RX	Input
33	UART1_TX	ETH3_LED_LINK	Output
34	MCU_MCAN1_TX	CAN1_TX	Output
35	NC	NC	NA

Table 3-29. 60-pin Application Connector (J16) Pin-out (continued)

Pin No.	CP Card Signals	IDK Card Signals	Direction
36	MCU_MCAN1_RX	CAN1_RX	Input
37	NC	NC	NA
38	PORZ_OUT	PORZ_OUT	Output
39	NC	NC	NA
40	CARD ID_APP_A0	EEPROM_A0	Output
41	NC	NC	NA
42	CARD ID_APP_A1	EEPROM_A1	Output
43	NC	NC	NA
44	CARD ID_APP_A2	EEPROM_A2	Output
45	NC	NC	NA
46	NC	NC	NA
47	NC	NC	NA
48	NC	NC	NA
49	NC	NC	NA
50	NC	NC	NA
51	NC	NC	NA
52	VDD_2V5	VCC_2V5	Power
53	NC	NC	NA
54	VDD_2V5	VCC_2V5	Power
55	VCC1V8	VCC_1V8	Power
56	VDD_1V0	VCC_1V0	Power
57	VCC1V8	VCC_1V8	Power
58	VDD_1V0	VCC_1V0	Power
59	VCC1V8	VCC_1V8	Power
60	VDD_1V0	VCC_1V0	Power

3.3.11 SERDES Interface

The AM65x processor has two SERDES lanes, which support multiplexed USB3.0, PCIe Gen3, or SGMII functionalities. There is a dedicated USB 2.0 (USB0) port terminated to the SERDES connector.

The SERDES0 lane can be configured as a PCIe, USB3.0, or SGMII port. The SERDES1 lane can be configured as PCIe or SGMII. All the signals are terminated to the SERDES connector, allowing various SERDES daughter cards to interface with the processor card. The PCIe lanes can be configured a single 2-lane port or two 1-lane ports independently.

The pin-out of SERDES connector is shown in Table 3-30.

Table 3-30. SERDES High Speed Connector (J5) Pin-out

Pin no.	Signal	Direction
1	DGND	Power
2	SOC_MCU_SCL	Output
3	SOC_MCU_SDA	Bidirectional
4	DGND	Power
5	USB0_DRV_VBUS	Power
6	GPIO_SGMII_PHY_RST	Output
7	DGND	Power
8	BOARDID_SERDES_A0	Power
9	BOARDID_SERDES_A1	Power
10	DGND	Power

Table 3-30. SERDES High Speed Connector (J5) Pin-out (continued)

Pin no.	Signal	Direction
11	BOARDID_SERDES_A2	Output
12	PCIe_GPIO_RESET_IN	Input
13	DGND	Power
14	USB0_ID_SOC	Input
15	PRG2_MDIO	Bidirectional
16	PRG2_MDC	Output
17	DGND	Power
18	VCC3V3_IO	Power
19	VCC3V3_IO	Power
20	DGND	Power
21	PCIE0_PRSNTN	Input
22	PCIE1_PRSNTN	Input
23	DGND	Power
24	SOC_SERDES_REFCLK0_N	Input
25	SOC_SERDES_REFCLK0_P	Input
26	DGND	Power
27	REFCLK1N	Output
28	REFCLK1P	Output
29	DGND	Power
30	PORZ_OUT	Output
31	NC	NA
32	DGND	Power
33	SOC_WKUP_SCL	Output
34	SOC_WKUP_SDA	Bidirectional
35	DGND	Power
36	USB0_DM	Bidirectional
37	USB0_DP	Bidirectional
38	DGND	Power
39	USB0_PCIE0_SGMII0_RXP0	Input
40	USB0_PCIE0_SGMII0_RXN0	Input
41	DGND	Power
42	USB0_PCIE0_SGMII0_TXP0	Output
43	USB0_PCIE0_SGMII0_TXN0	Output
44	DGND	Power
45	SERDES_BRD_DET	Input
46	GPIO_SGMII_PHY_INT	Input
47	USB0_VBUS	Power
48	DGND	Power
49	PCIE1_SGMII1_TXP1	Output
50	PCIE1_SGMII1_TXN1	Output
51	DGND	Power
52	PCIE1_SGMII1_RXN1	Input
53	PCIE1_SGMII1_RXP1	Input
54	DGND	Power
55	SOC_SERDES_REFCLK1_N	Input
56	SOC_SERDES_REFCLK1_P	Input
57	DGND	Power

Table 3-30. SERDES High Speed Connector (J5) Pin-out (continued)

Pin no.	Signal	Direction
58	REFCLK0N	Output
59	REFCLK0P	Output
60	DGND	Power

Table 3-31. SERDES Power and Control Signals Pin-out (J6)

Pin no.	Signal	Direction
1	VCC_2V5	Power
2	VCC_1V0	Power
3	VCC_1V8	Power
4	DGND	Power
5	DGND	Power
6	DGND	Power
7	12V0	Power
8	5V0	Power
9	12V0	Power
10	5V0	Power

3.3.12 GPMC/DSS Interface

The GPMC/DSS interface from the AM65x processor is routed to the GPMC/DSS expansion connector. This connector can be used to install an HDMI or DP adapter daughter card. The connector can also be used to attach to a circuit using the GPMC address/data bus interface. The function of the pins is defined by the pinmux definition.

The following interfaces are available on the GPMC/DSS connector:

- Multiplexed GPMC and DSS signals. The signals are at 3.3-V I/O level.
- McASP1 interface signals to support HDMI audio. The MCASP1 signals are multiplexed with PRG0_RGMII1 signals. Resistor options are provided to select the required interface. The McASP1 signals are at 1.8-V I/O level.
- MCU_I2C0 for configuration and control. The signals are at 3.3-V I/O level.
- WKUP I2C to connect to card ID memory. The signals are at 3.3-V I/O level.
- SPI1 interface for configuration and control. The signals are at 3.3-V I/O level.

The McAPS1 signals are multiplexed with the PRG0_RGMII signals of the application card. Resistor options are provided on the processor card to select the required interface, as shown in Figure 3-21. Refer to Table 3-32 for details.

The board supports an option to mount a 60-pin connector (QSH-030-01-L-D-A-K) or a 120-pin connector (QSH-060-01-L-D-A-K). These connector footprints are overlapped such that only one of them can be mounted. By default, the 60-pin connector is mounted.

GPMC/DSS, I2C, and USB 2.0 signals are connected to 60-pin connector (J36). The McASP1 signals are connected to the second half of the 120-pin connector. Thus, to access the McASP1 signals, the 60-pin should be unmounted and 120-pin connector should be mounted.

Table 3-32. HDMI/GPMC Connector (J35) Pin-out

Pin No.	Signal	Direction
1	VOUT1_DATA23_	Output
2	VCC1V8	Power
3	VOUT1_DATA22	Bidirectional
4	VCC1V8	Power
5	VOUT1_DATA21	Power
6	NC	NA

Table 3-32. HDMI/GPMC Connector (J35) Pin-out (continued)

Pin No.	Signal	Direction
7	VOUT1_DATA20	Bidirectional
8	CARDID_HDMI_A0	Output
9	VOUT1_DATA19	Bidirectional
10	CARDID_HDMI_A1	Output
11	VOUT_D18_BOOTMODE18	Bidirectional
12	CARDID_HDMI_A0	Power
13	VOUT_D17_BOOTMODE17	Bidirectional
14	NC	NA
15	VOUT_D16_BOOTMODE16	Bidirectional
16	PORZ_OUT	Output
17	DGND	Power
18	HDMI_GPMC_BRD_DET	Input
19	VOUT_D15_BOOTMODE15	Bidirectional
20	VOUT1_PCLK	Output
21	VOUT_D14_BOOTMODE14	Bidirectional
22	DGND	Power
23	VOUT_D13_BOOTMODE13	Bidirectional
24	VOUT1_VSYNC	Output
25	VOUT_D12_BOOTMODE12	Bidirectional
26	VOUT1_HSYNC_TEST_HDR	Output
27	VOUT_D11_BOOTMODE11	Bidirectional
28	VOUT1_DE_TEST_HDR	Output
29	VOUT_D10_BOOTMODE10	Bidirectional
30	DGND	Power
31	VOUT_D9_BOOTMODE9	Bidirectional
32	SOC_MCU_SCL	Output
33	VOUT_D8_BOOTMODE8	Bidirectional
34	SOC_MCU_SDA	Bidirectional
35	DGND	Power
36	DGND	Power
37	VOUT_D7_BOOTMODE7	Bidirectional
38	GP1_TOUCH_EVT	Output
39	VOUT_D6_BOOTMODE6	Bidirectional
40	CON_LCD_PWR_DN	Output
41	VOUT_D5_BOOTMODE5	Power
42	SOC_SPI1_CS1	Output
43	VOUT_D4_BOOTMODE4	Bidirectional
44	SOC_SPI1_MOSI	Output
45	VOUT_D3_BOOTMODE3	Bidirectional
46	SOC_SPI1_MISO	Input
47	VOUT_D2_BOOTMODE2	Bidirectional
48	SOC_SPI1_CLK	Output
49	VOUT_D1_BOOTMODE1	Bidirectional
50	USB1_HDMI_GPMC_DRVBUS	Output
51	VOUT_D0_BOOTMODE0	Bidirectional
52	USB1_HDMI_GPMC_DM	Bidirectional
53	NC	NA

Table 3-32. HDMI/GPMC Connector (J35) Pin-out (continued)

Pin No.	Signal	Direction
54	USB1_HDMI_GPMC_DP	Bidirectional
55	VCC_5V0	Power
56	VCC3V3_IO	Power
57	VCC_5V0	Power
58	VCC3V3_IO	Power
59	VCC_5V0	Power
60	VCC3V3_IO	Power
61	NC	NA
62	NC	NA
63	NC	NA
64	NC	NA
65	NC	NA
66	NC	NA
67	NC	NA
68	NC	NA
69	NC	NA
70	NC	NA
71	NC	NA
72	NC	NA
73	NC	NA
74	NC	NA
75	NC	NA
76	NC	NA
77	NC	NA
78	NC	NA
79	NC	NA
80	NC	NA
81	NC	NA
82	NC	NA
83	NC	NA
84	NC	NA
85	NC	NA
86	NC	NA
87	NC	NA
88	NC	NA
89	NC	NA
90	NC	NA
91	NC	NA
92	NC	NA
93	NC	NA
94	NC	NA
95	NC	NA
96	NC	NA
97	NC	NA
98	NC	NA
99	NC	NA
100	NC	NA

Table 3-32. HDMI/GPMC Connector (J35) Pin-out (continued)

Pin No.	Signal	Direction
101	NC	NA
102	NC	NA
103	NC	NA
104	NC	NA
105	MCASP1_AFSX_3V3	IO
106	NC	NA
107	MCASP1_AXR1_3V3	IO
108	NC	NA
109	MCASP1_ACLKX_3V3	IO
110	NC	NA
111	MCASP1_AHCLKX_3V3	IO
112	NC	NA
113	MCASP1_AXR0_3V3	IO
114	NC	NA
115	MCASP1_ACLKR_3V3	IO
116	NC	NA
117	MCASP1_AFSR_3V3	IO
118	NC	NA
119	MCASP1_AHCLKR_3V3	IO
120	NC	NA

3.3.13 I2C Interface

There are five I2C interfaces on the common processor card. All the I2C interface signals use the 3.3-V I/O level.

1. WKUP_I2C0 is interfaced to a presence detect latch to identify the daughter cards which are presently installed. In addition, the processor board and each daughter card has a Board ID memory device connected to WKUP_I2C0. The Board ID memories contain identification and configuration information for the cards. The WKUP_I2C0 is also used to communicate with the power supply IC for the SoC_MPU rail, allowing modification of the voltage.
2. I2C0 is connected to the on-card RTC, LED driver, I/O expander, and application connector to interface the I/O expander. This I2C is also connected to a test header J33 for AM65x processor slave operation. Pin outs of the I2C test header is given in Table 3-33.

Table 3-33. I2C Test Header (J33) Pin-out

Pin no.	Signal
1	DGND
2	I2C0_SDA
3	I2C0_SCL

3. I2C1 is connected to a display adapter connector.
4. MCU_I2C0 is connected to BOOT EEPROM, SERDES connector, GPMC/DSS connector, display port adopter interface, and camera connector.
5. I2C2 is connected to current monitors, temperature sensors, and the test automation header.

I2C0 and I2C1 are powered by VDDSHV_GENERAL, WKUP_I2C0 and MCU_I2C0 are powered by VDDS_WKUP_GENERAL, and I2C2 is powered by VDDSHV_GPMC supply.

One test header for I2C0 is provided for any external validation. Figure 3-22 and Figure 3-23 depicts the I2C tree.

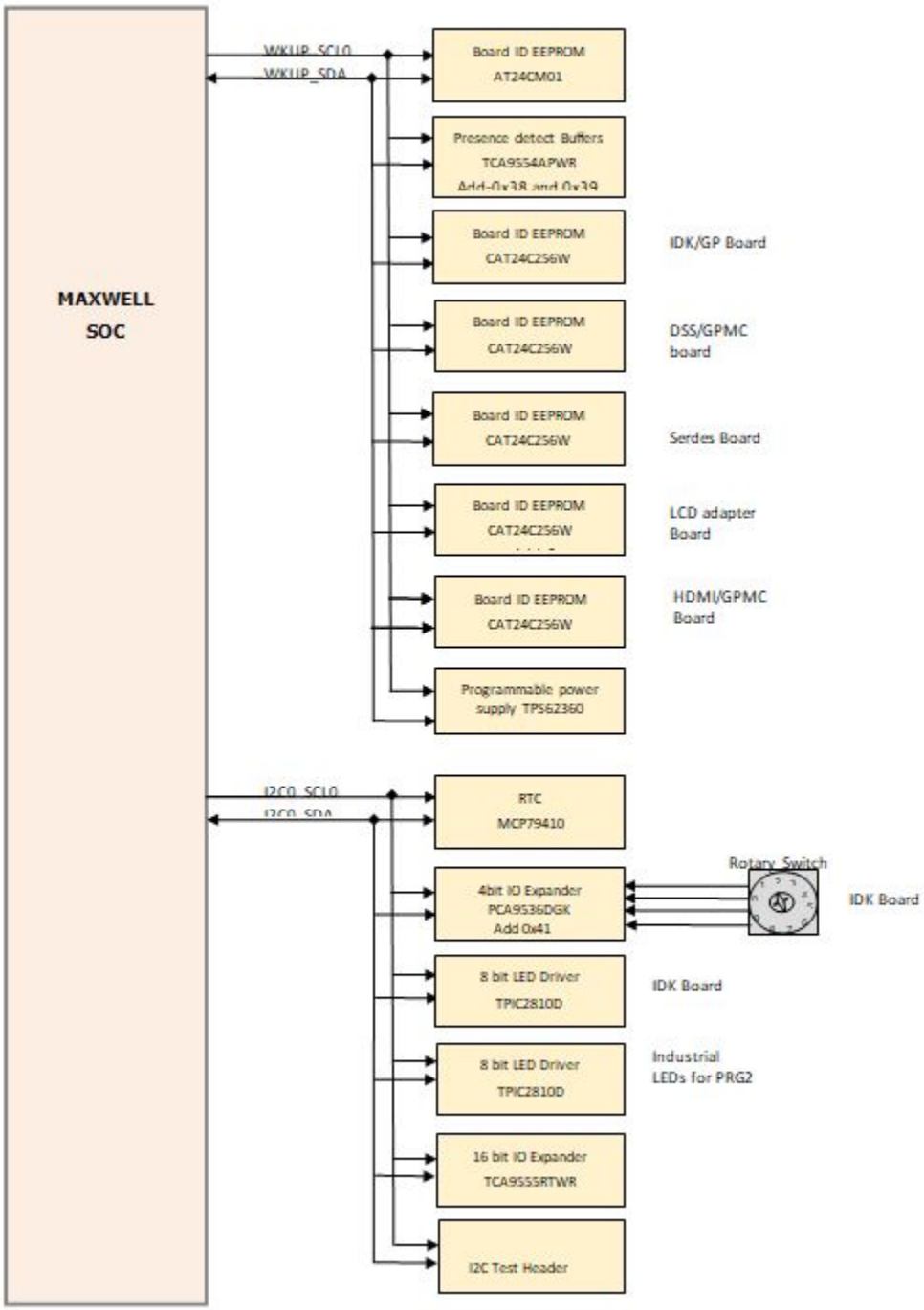

Figure 3-22. I2C Interfaces and Address Assignment to its Peripherals (1 of 2)

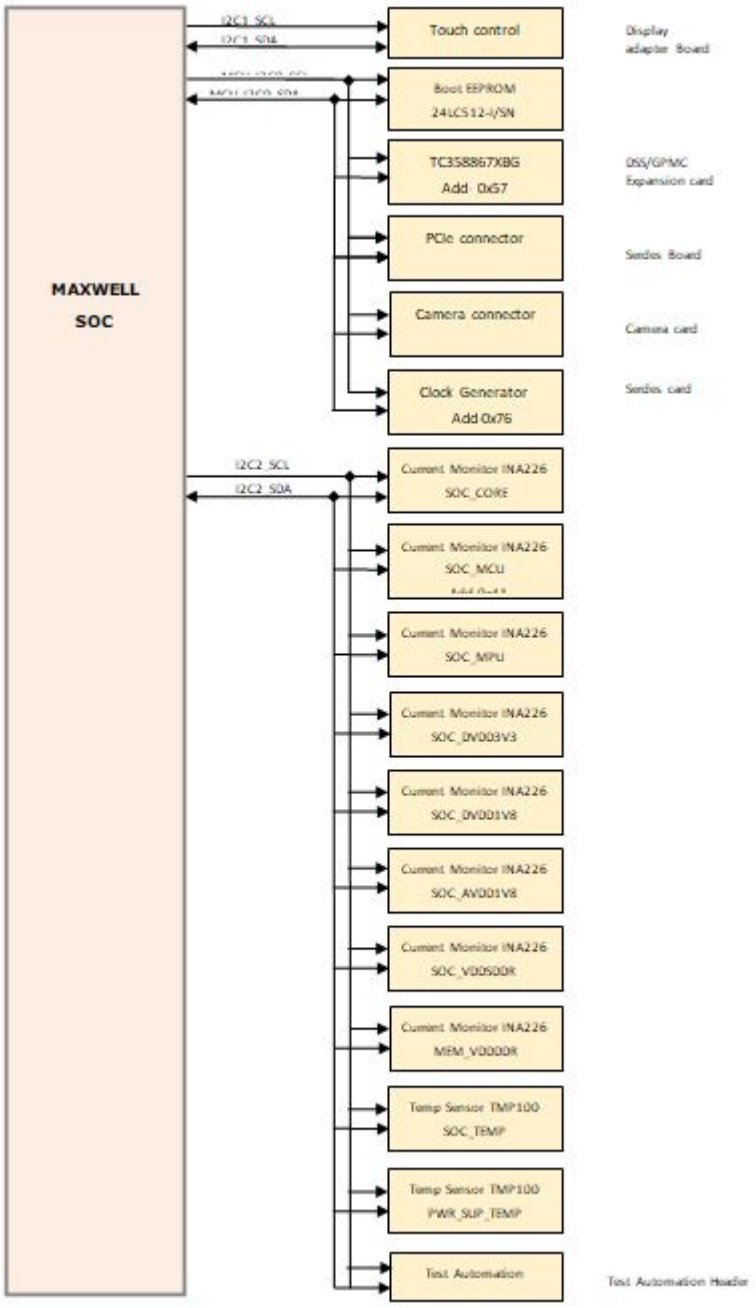

Figure 3-23. I2C Interfaces and Address Assignment to its Peripherals (2 of 2)

3.3.14 SPI Interface

Of the six SPI interfaces supported by the AM65x processor, three are used on the processor card:

- SPI0: A 128-Mbit SPI NOR Flash of part number MT25QL128ABA8E12 is interfaced to the SPI0 port of the AM65x. In addition, SPI0 is also connected to the application connector. SPI_CS0 and SPI_CS1 chip select signals are used for the serial flash and application connector, respectively.
- SPI1 is connected to the display connector, GPMC/DSS connector, and test header. The SPI1 interface signals are at a 3.3-V I/O level. SPI1_CS0 is connected to the display connector and SPI_CS1 is connected to the GPMC/DSS connector. The chip selects SPI1_CS0 and SPI_CS1 are also connected to the test header, through resistors (R316 and R317) as shown in Table 3-35. By default, these resistors are not installed. To use the SPI functionality on the header, either R316 or R317 must be mounted. Pin-outs of the test header (J20) are given in Table 3-34.

Table 3-34. SPI1 Header (J20) Pin-out

Pin no.	Signal
1	SPI1_MOSI
2	SPI1_MISO
3	SPI1_CS
4	SPI1_CLK
5	DGND

Table 3-35. Resistors for Selecting CS Signals for Test Automation Header

Selected SPI1_CS Signal for Test Header	Mount	Unmount
SPI1_CS1	R316	R311
SPI1_CS0	R317	R675

- The MCU_SPI is interfaced to the CSI-2 connector.

The SPI0 and SPI1 interface signals are powered by the VDDSHV_GENERAL power supply of SoC and are at the 3.3-V I/O level.

The MCU_SPI interface signals are powered by the VDDSHV_WKUP_GENERAL power supply of SoC and are at the 3.3-V I/O level.

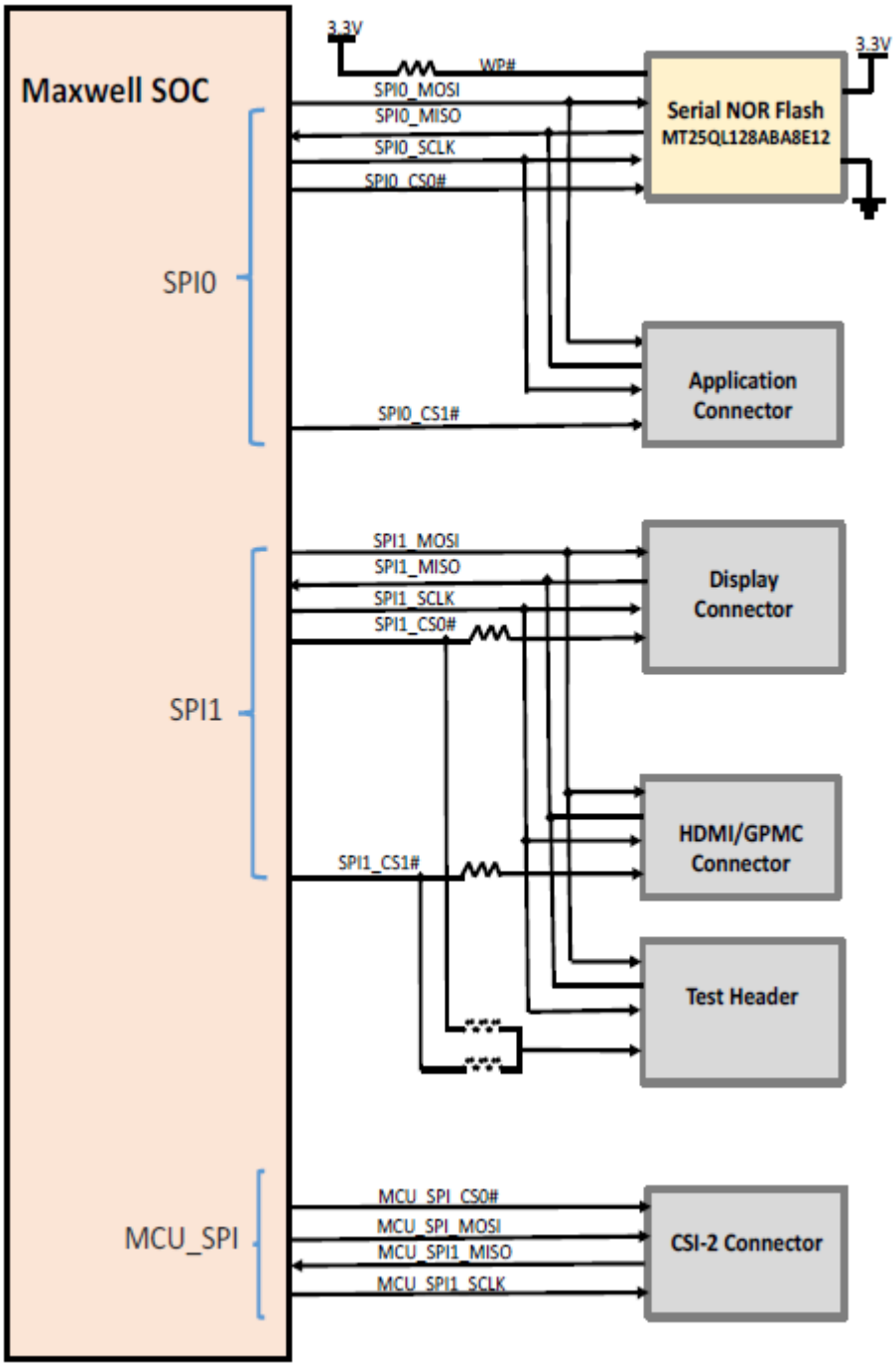

Figure 3-24. SPI Tree

3.3.15 Timer and Interrupt

The card supports the following timer and interrupt options.

3.3.15.1 Timer

There are 6 timer outputs available over the test header (J39) on the common processor card. The timer signals IO2, IO3, IO6, and IO7 are muxed with the VOUT signals of the SoC. Jumpers are provided on the common processor card to select the required interface, as shown in Figure 3-25.

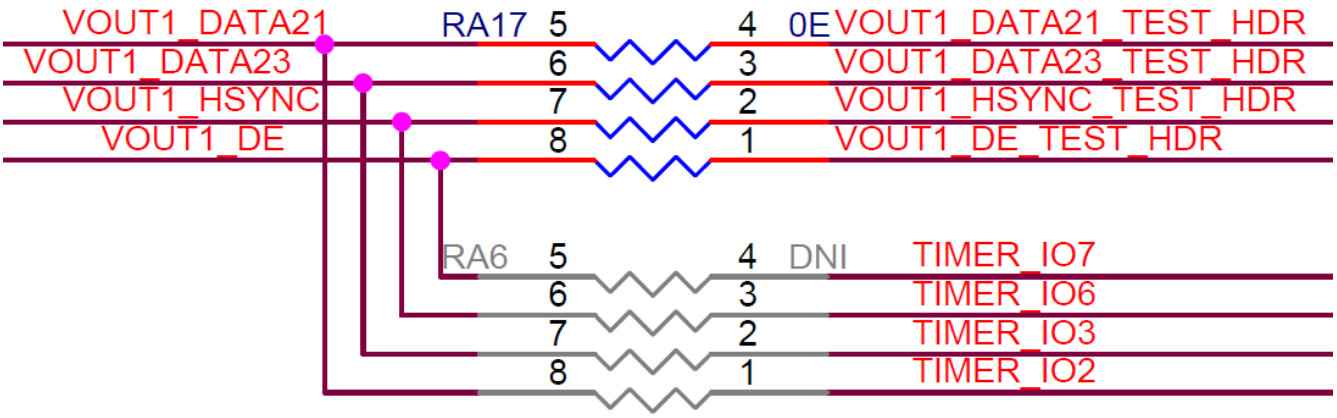

Figure 3-25. Jumpers for Selecting Timer Signals

The following resisters are mounted or unmounted to select the timer signals on the test header.

Table 3-36. Timer Pin Selection

Refdes	Mount/ Unmount
RA17	Unmount
RA6	Mount

Table 3-37. Timer Header(J19) Pin-out

Name	Net Name	Direction
1	TIMER_IO0	Output
2	TIMER_IO1	Output
3	TIMER_IO2	Output
4	TIMER_IO3	Output
5	TIMER_IO6	Output
6	TIMER_IO7	Output
7	DGND	Power

3.3.15.2 Interrupt

There are 2 push-button interrupts (SW5, SW6) supported for the wake-up domain of the processor on the common processor card. These interrupts are implemented with a Schmitt-trigger buffer and RC delays to avoid any de-bounce effects triggering the interrupts.

The push-button SW5 is mapped to WKUP_GPIO0_13, and SW6 is mapped to WKUP_GPIO0_27.

3.3.16 Fan Connector

A 3-pin header (J9) of part number 440054-3 is provided for powering a fan, if needed. The fan is not provided with the EVM.

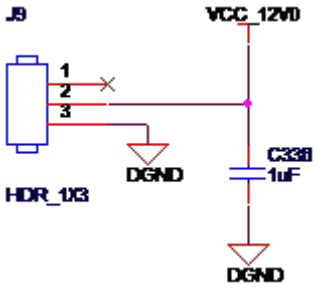

Figure 3-26. Cooling FAN Header

4 IDK Application Card

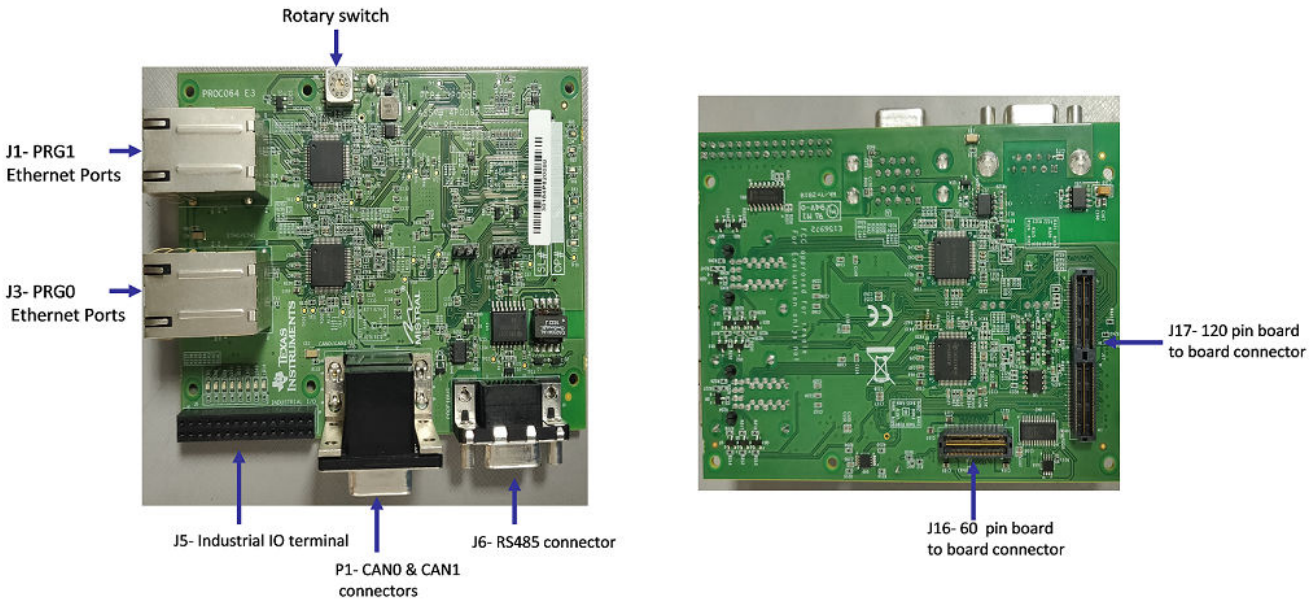

Figure 4-1. IDK Application Card

4.1 Key Features

Interface:

- CAN interface terminated to a DB-9 connector
- Profibus UART transceiver terminated to a DB-9 connector
- Four 1-Gpbs Ethernet ports from PRG0 and PRG1 ports of the AM65x processor using a DP83867IRPAP PHY and RJ45 connector
- I2C interface for EEPROM
- SPI interface for industrial I/O block application

Memory:

- Board ID EEPROM

Power Supply:

- DC input: 3.3 V, 2.5 V, 1 V, 1.8 V, and 5 V
- Powered by the AM65x Common Processor Board

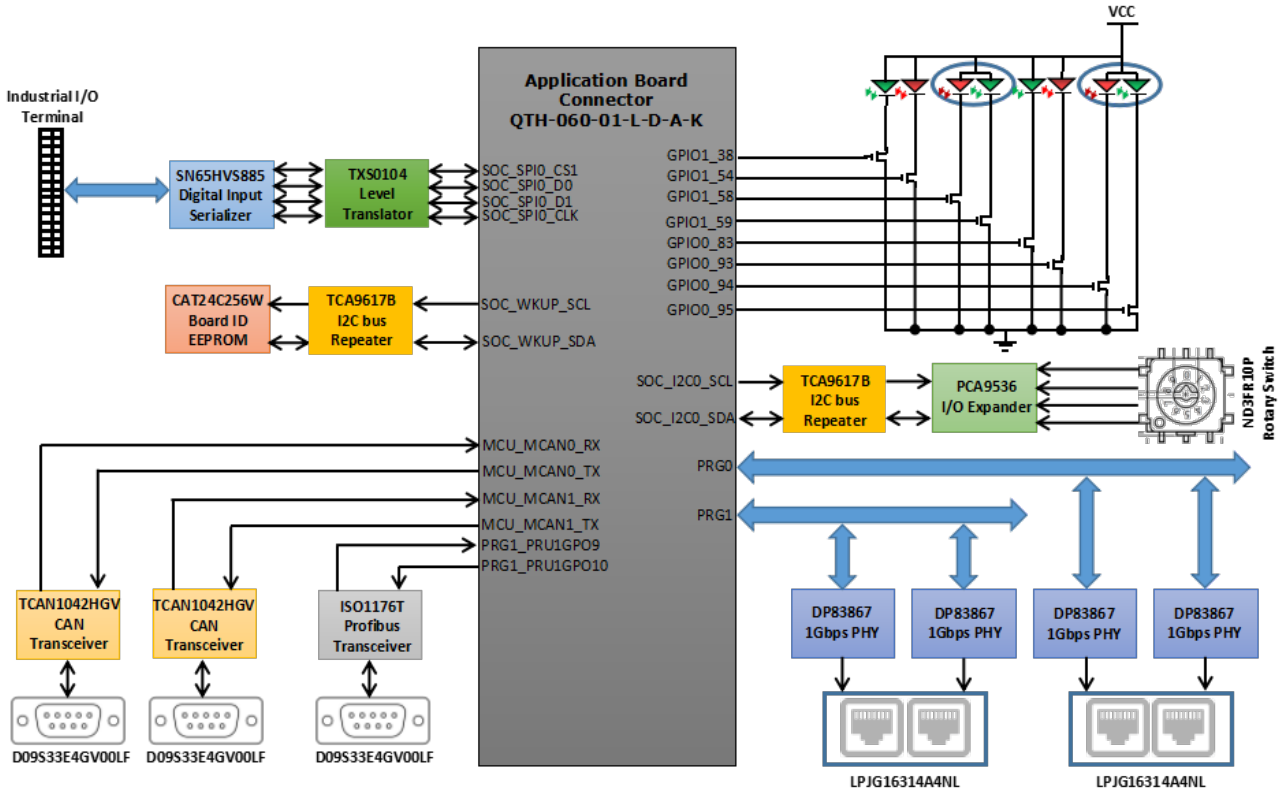

Figure 4-2. IDK Application Card Block Diagram

4.2 Overview of IDK Application Board

This section provides an overview of the different interfaces and circuits on the IDK application board.

4.2.1 Application Card Connector

There are two connectors provided on this card for plugging into the common processor card. A 120-pin connector (J17) and A 60-pin connector (J16) are used. These connectors provide power and data interface for the card.

Table 4-1. 120-pin Application Connector (J17) Pin-out

Pin Number	Signal Name	Pin Number	Signal Name
1	DGND	2	DGND
3	ETH0_CLK	4	ETH1_CLK
5	DGND	6	DGND
7	ETH0_RGMII_TD3	8	ETH1_MII_RXER
9	ETH0_RGMII_TD1	10	ETH_LED1
11	ETH0_RGMII_TD2	12	ETH_LED3
13	ETH0_RGMII_TX_CTL	14	PRG0_IEP0_LATCH_IN0
15	ETH0_RGMII_TD0	16	ETH0_LED_LINK
17	DGND	18	ETH0/1_INTN
19	ETH0_RGMII_TXC	20	ETH0_LED_LINK
21	DGND	22	ETH1_LED_LINK
23	ETH0_RGMII_RD3	24	ETH_LED2
25	DGND	26	ETH1_RGMII_RX_CTL

Table 4-1. 120-pin Application Connector (J17) Pin-out (continued)

Pin Number	Signal Name	Pin Number	Signal Name
27	ETH0_RGMII_RXC	28	ETH1_RGMII_RD3
29	DGND	30	ETH1_RGMII_RD0
31	ETH0_RGMII_RX_CTL	32	ETH1_RGMII_RD2
33	ETH0_RGMII_RD2	34	ETH1_RGMII_RD1
35	ETH0_RGMII_RD0	36	DGND
37	ETH0_MII_RXER	38	ETH1_RGMII_TXC
39	ETH0_RGMII_RD1	40	DGND
41	ETH1_LED_LINK	42	ETH1_RGMII_TD3
43	GPIO_ETH2/3_RESETN	44	ETH1_RGMII_TD2
45	GPIO_ETH0/1_RESETN	46	ETH1_RGMII_TD1
47	ETH_LED4	48	ETH1_RGMII_TX_CTL
49	ETH2/3_INTN	50	ETH1_RGMII_TD0
51	PRG0_IEP1_LATCH_IN0	52	DGND
53	ETH0/1_MDIO	54	ETH1_RGMII_RXC
55	ETH3_MII_RXER	56	DGND
57	ETH3_LED_LINK	58	ETH2_LED_LINK
59	ETH0/1_MDC	60	ETH2_MII_RXER
61	RS485_UART_TX	62	IDK_IOEXP_LDN_1V8
63	ETH3_RGMII_RD0	64	RS485_UART_RX
65	ETH3_RGMII_RX_CTL	66	ETH2_LED_LINK
67	ETH3_RGMII_RD1	68	ETH_LED7
69	DGND	70	ETH_LED5
71	ETH3_RGMII_RXC	72	PRG1_IEP0_LATCH_IN0
73	DGND	74	RS485_UART_RTSN
75	ETH3_RGMII_RD3	76	ETH2_RGMII_RD1
77	ETH3_RGMII_RD2	78	ETH2_RGMII_RX_CTL
79	ETH3_RGMII_TD0	80	ETH2_RGMII_RD2
81	ETH3_RGMII_TX_CTL	82	DGND
83	ETH3_RGMII_TD3	84	ETH2_RGMII_RXC
85	DGND	86	DGND
87	ETH3_RGMII_TXC	88	ETH2_RGMII_RD0
89	DGND	90	ETH2_RGMII_RD3
91	ETH3_RGMII_TD1	92	DGND
93	ETH3_RGMII_TD2	94	ETH2_RGMII_TXC
95	ETH2/3_MDC	96	DGND
97	DGND	98	ETH2_RGMII_TX_CTL
99	ETH2/3_MDIO	100	ETH2_RGMII_TD2
101	DGND	102	ETH2_RGMII_TD3
103	ETH3_CLK	104	DGND
105	DGND	106	ETH2_CLK
107	DGND	108	DGND
109	DGND	110	ETH2_RGMII_TD0
111	DGND	112	DGND
113	PRESENSE_DETECT	114	ETH2_RGMII_TD1
115	DGND	116	DGND
117	DGND	118	DGND

Table 4-1. 120-pin Application Connector (J17) Pin-out (continued)

Pin Number	Signal Name	Pin Number	Signal Name
119	DGND	120	DGND

Table 4-2. 60-pin Application Connector (J17) Pin-out

Pin Number	Signal Name	Pin Number	Signal Name
1	VCC_3V3	2	VCC_5V0
3	VCC_3V3	4	VCC_5V0
5	VCC_3V3	6	VCC_5V0
7	NC	8	NC
9	NC	10	NC
11	NC	12	NC
13	DGND	14	NC
15	EEPROM_I2C_SCL	16	NC
17	EEPROM_I2C_SDA	18	DGND
19	DGND	20	IDK_SPI_CLK_3V3
21	IDK_I2C_SCL_C	22	DGND
23	IDK_I2C_SDA_C	24	IDK_SPI_CSN_3V3
25	DGND	26	NC
27	PRG1_IEP1_LATCH_IN0	28	IDK_SPI_MISO_3V3
29	ETH_LED8	30	CAN0_TX
31	ETH_LED6	32	CAN0_RX
33	ETH3_LED_LINK	34	CAN1_TX
35	NC	36	CAN1_RX
37	NC	38	PORZ_OUT
39	NC	40	EEPROM_A0
41	NC	42	EEPROM_A1
43	NC	44	EEPROM_A2
45	NC	46	NC
47	NC	48	NC
49	NC	50	NC
51	NC	52	VCC_2V5
53	NC	54	VCC_2V5
55	VCC_1V8	56	VCC_1V0
57	VCC_1V8	58	VCC_1V0
59	VCC_1V8	60	VCC_1V0

4.2.2 Profibus Interface

The UART1 signals of the AM65x processor are terminated in the application connector of the common processor card. The IDK application card includes an isolated Profibus RS-485 transceiver with an integrated transformer driver and a DB9 connector.

Table 4-3. RS485 Connector (J6) Pin-out

Pin No.	Signal
3	DATA_P
8	DATA_N
6	VCC_PROFIBUS (5V)
5	GND
1, 2, 4, 7, 9	NC

4.2.3 CAN Interface

The IDK application card includes two CAN interfaces that are terminated with DB-9 connectors. MCAN0 and MCAN1 signals are used from the application connector of CP card to implement the interface. The option for a 120-ohm termination resistor is placed in between CANH and CANL to match the characteristic impedance of the bus. The STB pin of the of IC is held high by default, and a GPIO control line provided to pull the line low.

Table 4-4. CAN Connector Pin-out

CAN0 (P1A)		CAN1 (P1B)	
Pin No.	**Signal**	**Pin No.**	**Signal**
2	CAN0_L	2	CAN1_L
7	CAN0_H	7	CAN1_H
3	GND	3	GND
9	VCC_CAN (5V)	9	VCC_CAN (5V)
1, 4, 5, 6, 8	NC	1, 4, 5, 6, 8	NC

4.2.4 Rotary Switch

The IDK application card includes a rotary switch connected through SOC_I2C0. A 4-bit I/O expander is used to capture the rotary switch position. The I2C slave address for PCA9536 is 0x41.

4.2.5 Industrial I/O Terminal Connector

The IDK application card includes a 2x15 industrial I/O terminal connector (J5) which consists of 8 industrial inputs and 8 industrial outputs. Industrial inputs are connected to a digital input serializer. The serializer is connected to the application connector using the SPI interface. The logic signals at the DB0 and DB1 pins determine the debounce times for the device. The default debounce time is set to 3-ms delay. The input high is defined above 8.2 V, and input low is set below 7.3 V for the industrial inputs.

Table 4-5. Industrial Terminal Block Pin-out (J5)

Pin No.	Signal
1	IP0
3	IP1
5	IP2
7	IP3
9	IP4
11	IP5
13	IP6
15	IP7
17, 29, 30	GND
27, 28	VCC_5V
2, 4, 6, 8, 10, 12, 14, 16, 18	NC
19	OP0
20	OP1
21	OP2
22	OP3
23	OP4
24	OP5
25	OP6
26	OP7

4.2.6 Ethernet Interface

Four RGMII/MII ports from the ICSSG domain of the AM65x processor are terminated to the application card connector. These ports in the IDK application board are connected to Gigabit Ethernet PHYs, and the output of the PHYs are terminated with RJ45 connectors (J1 and J3 stacked RJ45 connectors) with integrated magnetic.

All RJ45 ports support 1000 Mbps / 100 Mbps / 10 Mbps using RGMII, and 100 Mbps / 10 Mbps using MII.

From the Ethernet PHY, LED1 and COL/GPIO are connected to dual LEDs of RJ45 to indicate 10/100 Mb or 1000-Mb link. The green LED indicates 10/100-Mb speed, and the orange LED indicates 1000-Mb speed.

LED2 is connected to RJ45 LED (Yellow) to indicate transmit/receive activity.

The IDK application board is delivered with all PHYs configured to operate in RGMII mode. Some industrial protocols require the use of the MII interface instead of RGMII. To change the interface to MII mode, modifications must be made, as shown in Table 4-6.

Table 4-6. Modifications for MII Mode of Operation

PHY	Mount	Unmount
PHY 0	R271	R269
	R272	R270
	R274	R273
	R276	R275
	R278	R277
	R290	R452
	R444	
	R445	
	R453	

Table 4-6. Modifications for MII Mode of Operation (continued)

PHY	Mount	Unmount
PHY 1	R317	R315
	R318	R316
	R320	R319
	R322	R321
	R324	R323
	R338	R454
	R446	
	R447	
	R455	
PHY 2	R356	R355
	R359	R357
	R361	R358
	R363	R360
	R364	R362
	R378	R456
	R448	
	R449	
	R457	
PHY 3	R399	R397
	R400	R398
	R403	R401
	R405	R402
	R406	R404
	R420	R458
	R450	
	R451	
	R459	

Default strapping details of all the PHYs are listed in Table 4-7.

Table 4-7. Ethernet Strap Settings for RGMII and MII Mode

		MII Mode Strap Setting			RGMII Mode Strap Setting		
	Signal	Mode	Pull Up	Pull Down	Mode	Pull Up	Pull Down
PHY0 (J3A) (PHY Address-00000)	RX_D0	1	Open	Open	1	Open	Open
	RX_D2	1	Open	Open	1	Open	Open
	RX_D4	3	5.76k	2.49k	1	Open	Open
	RX_D5	1	Open	Open	1	Open	Open
	RX_D6	3	5.76k	2.49k	1	Open	Open
	RX_D7	1	Open	Open	1	Open	Open
	RX_DV/RX_CTRL	3	5.76k	2.49k	3	5.76k	2.49k
	CRS	2	10k	2.49k	2	10k	2.49k
	LED_1	3	5.76k	2.49k	1	Open	Open
	LED_0	1	Open	Open	1	Open	Open

Table 4-7. Ethernet Strap Settings for RGMII and MII Mode (continued)

		MII Mode Strap Setting			RGMII Mode Strap Setting		
	Signal	**Mode**	**Pull Up**	**Pull Down**	**Mode**	**Pull Up**	**Pull Down**
PHY1 (J3B) (PHY Address-00011)	RX_D0	4	2.49K	Open	4	2.49K	Open
	RX_D2	1	Open	Open	1	Open	Open
	RX_D4	3	5.76k	2.49k	1	Open	Open
	RX_D5	1	Open	Open	1	Open	Open
	RX_D6	3	5.76k	2.49k	1	Open	Open
	RX_D7	1	Open	Open	1	Open	Open
	RX_DV/RX_CTRL	3	5.76k	2.49k	3	5.76k	2.49k
	CRS	2	10k	2.49k	2	10k	2.49k
	LED_1	3	5.76k	2.49k	1	Open	Open
	LED_0	1	Open	Open	1	Open	Open
PHY2 (J1A) (PHY Address-00000)	RX_D0	1	Open	Open	1	Open	Open
	RX_D2	1	Open	Open	1	Open	Open
	RX_D4	3	5.76k	2.49k	1	Open	Open
	RX_D5	1	Open	Open	1	Open	Open
	RX_D6	3	5.76k	2.49k	1	Open	Open
	RX_D7	1	Open	Open	1	Open	Open
	RX_DV/RX_CTRL	3	5.76k	2.49k	3	5.76k	2.49k
	CRS	2	10k	2.49k	2	10k	2.49k
	LED_1	3	5.76k	2.49k	1	Open	Open
	LED_0	1	Open	Open	1	Open	Open
PHY3 (J1B) (PHY Address-00011)	RX_D0	4	2.49K	Open	4	2.49K	Open
	RX_D2	1	Open	Open	1	Open	Open
	RX_D4	3	5.76k	2.49k	1	Open	Open
	RX_D5	1	Open	Open	1	Open	Open
	RX_D6	3	5.76k	2.49k	1	Open	Open
	RX_D7	1	Open	Open	1	Open	Open
	RX_DV/RX_CTRL	3	5.76k	2.49k	3	5.76k	2.49k
	CRS	2	10k	2.49k	2	10k	2.49k
	LED_1	3	5.76k	2.49k	1	Open	Open
	LED_0	1	Open	Open	1	Open	Open

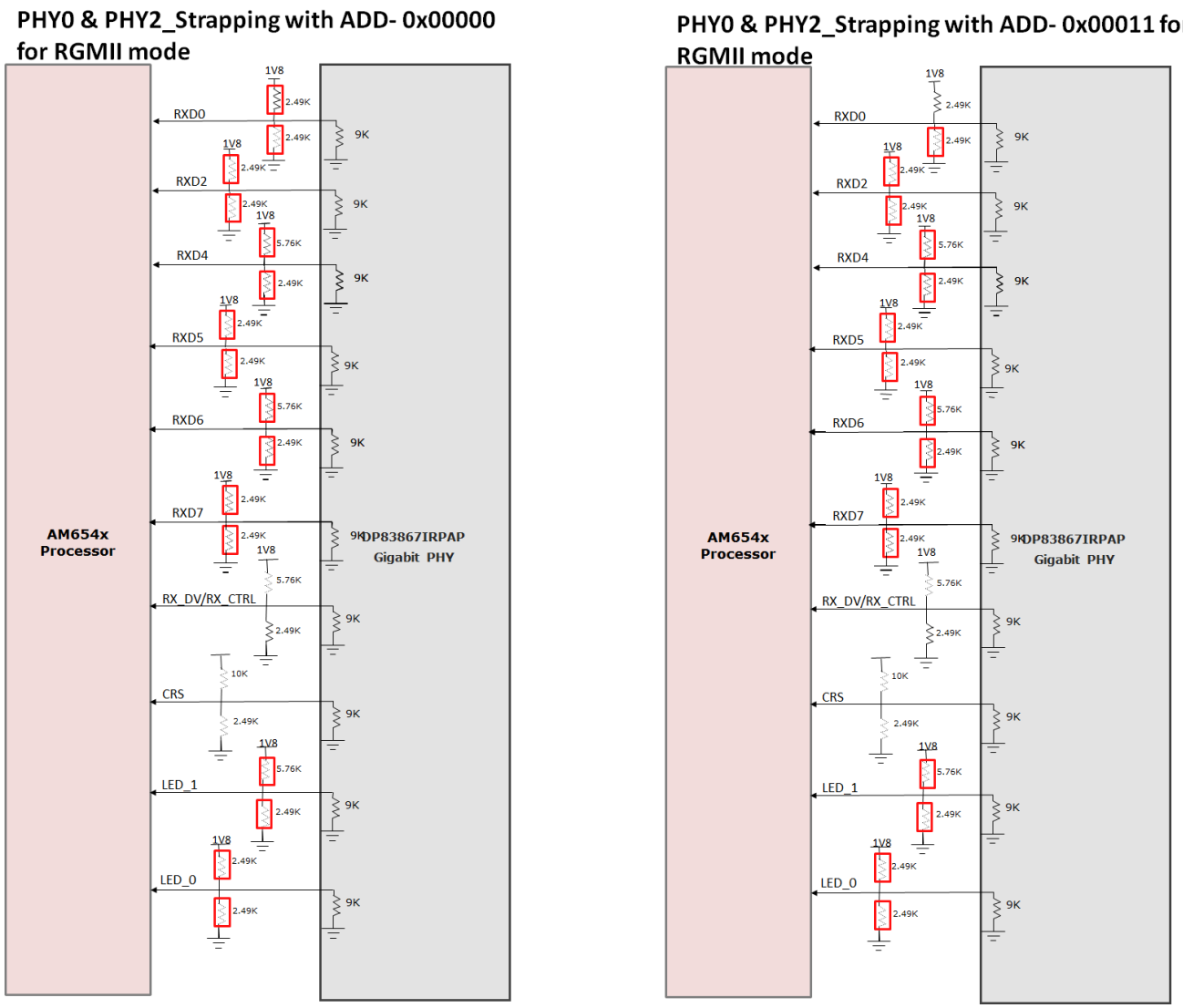

Figure 4-3. PRG0 and PRG1 Ethernet Strapping Diagram in RGMII Mode

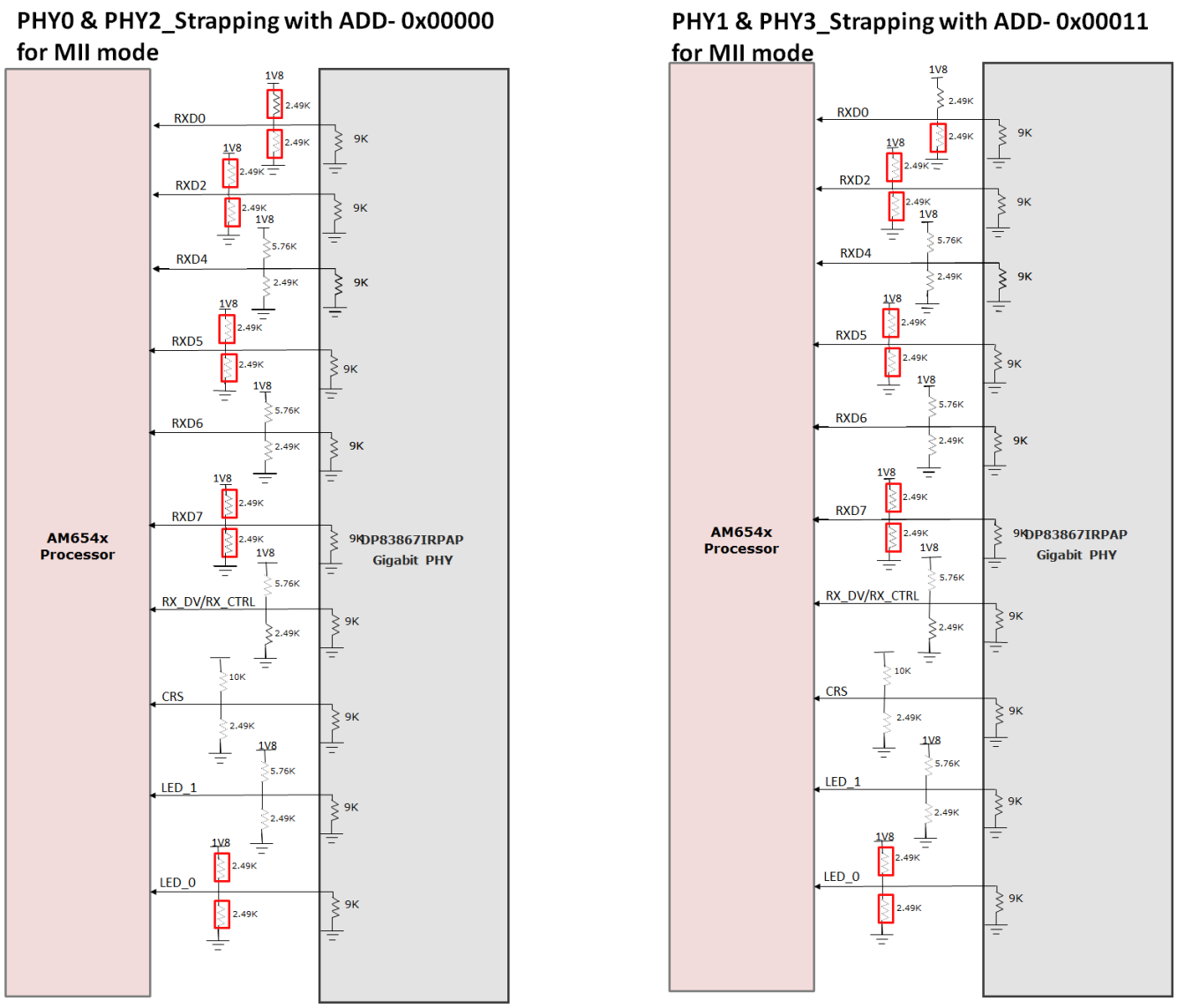

Figure 4-4. PRG0 and PRG1 Ethernet Strapping Diagram in MII Mode

Note

Resistors marked with the red color box are DNI for those particular modes of operation.

Some of the GPIOs are used to indicate Ethernet activities, as shown in Figure 4-5.

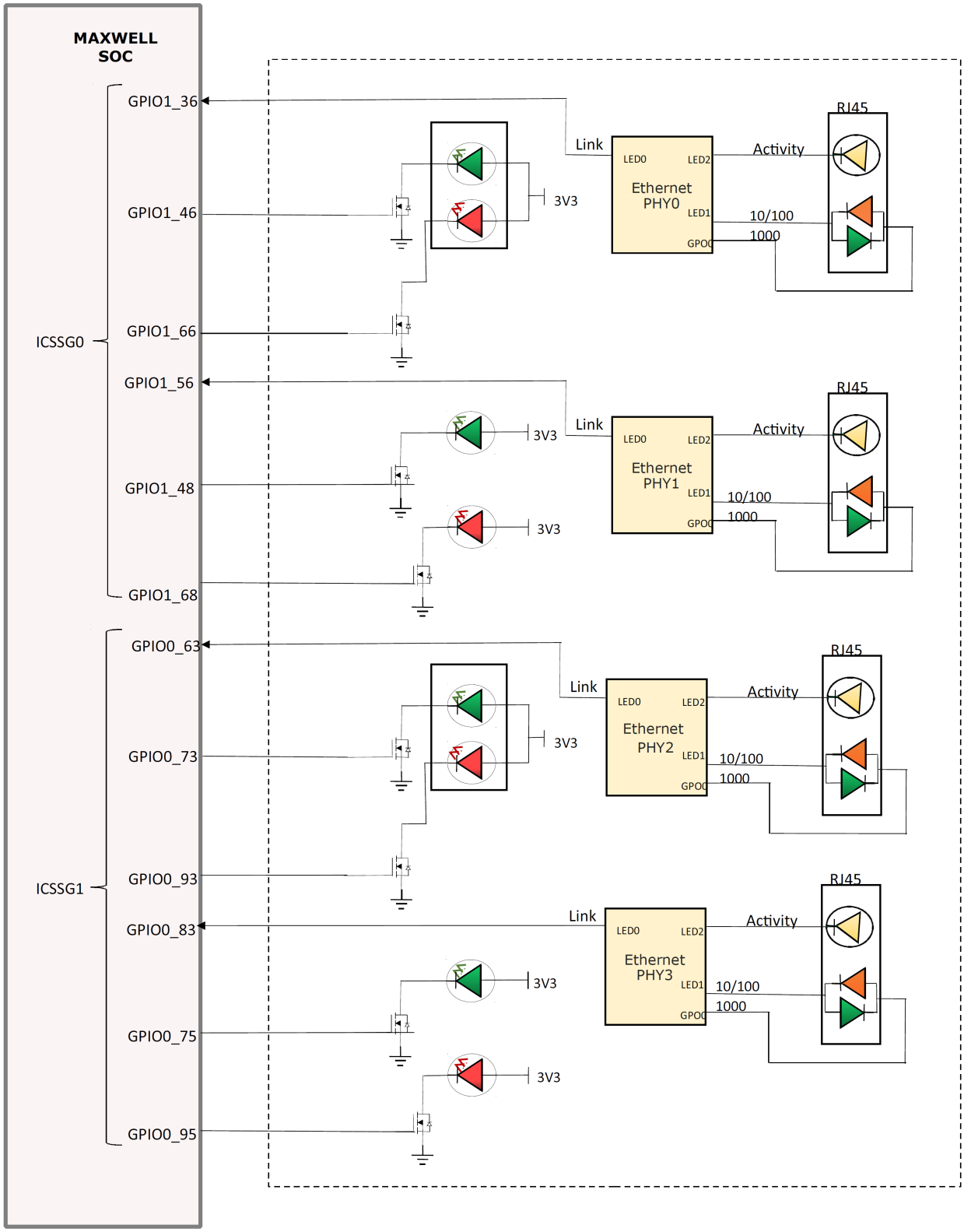

Figure 4-5. IDK Board Ethernet LEDs

4.2.7 Board ID Memory

The IDK application board is identified by its version and serial number, which are stored in the onboard EEPROM. The EEPROM is accessible on the address 0x52.

The IDK application board includes a CAT24C256W I2C EEPROM ID memory. The first 254 bytes of addressable EEPROM memory are preprogrammed with identification information for each board. The remaining 32512 bytes are available to the user for data or code storage.

Table 4-8. Board ID Memory Header Information of IDK Board

Header	Field Name	Nbr bytes	Comments
EE3355AA	MAGIC	4	Magic Number
	TYPE	1	Fixed length and variable position board ID header
		2	Size of payload
BRD_INFO	TYPE	1	payload type
	Length	2	offset to next header
	Board_Name	16	Name of the board
	Design_Rev	2	Revision number of the design
	PROC_Nbr	4	PROC number
	Variant	2	Design variant number
	PCB_Rev	2	Revision number of the PCB
	SCHBOM_Rev	2	Revision number of the schematic
	SWR_Rev	2	software release number
	VendorID	2	
	Build_Week	2	week of the year of production
	Build_Year	2	year of production
	BoardID	6	
	Serial_Nbr	4	incrementing board number
MAC_ADDR	TYPE	1	payload type
	LENGTH	2	Size of payload
	MAC control	2	MAC header control word
	MAC_adrs	192	MAC adress of AM65x PRG0 & PRG1
END_LIST	TYPE	1	End Marker

4.2.8 Power Supply

Power for the IDK application card is obtained from the application connector. All required powers are terminated in the application connector of the AM65x common processor card.

5 x2 Lane PCIe Personality Card

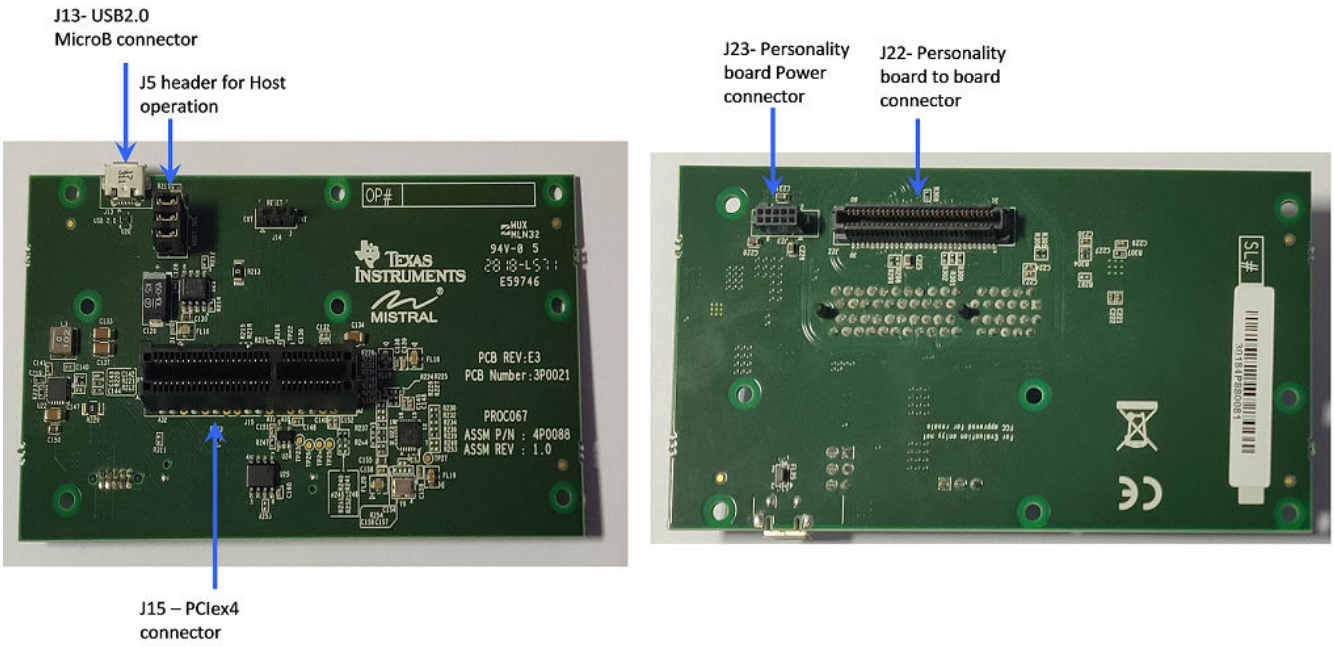

Figure 5-1. x2 Lane PCIe Card

5.1 Key Features

Interface:

- Includes high-speed connector to interface with the AM65x common processor board
- Includes one x4 PCIe connector
- Accepts PCIe form factor daughter card
- Supports PCIe Gen 3 operation
- Includes Board ID EEPROM
- Includes a USB 2.0 interface

Power Supply:

- A 10-pin power connector for DC input: 3.3 V, 2.5 V, 1 V, 1.8 V, and 5 V
- Powered by MAXWELL common processor board

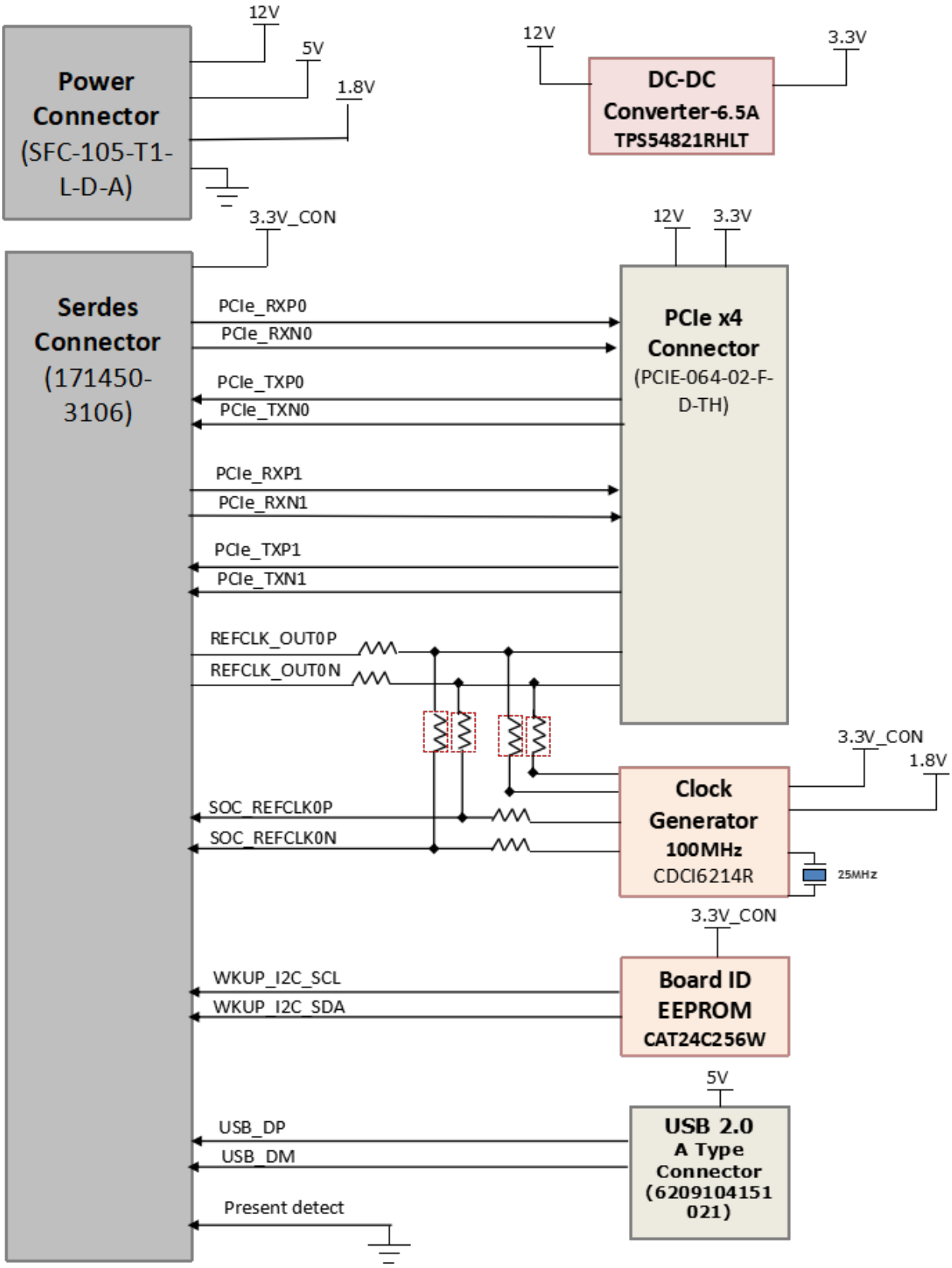

Figure 5-2. x2 Lane PCIe Personality Card Block Diagram

5.2 Overview of PCIex2 Daughter Card

This section provides an overview of the different interfaces on the PCIex2 daughter card.

5.2.1 Personality Card Connectors

There are two board interconnects (J22 and J23) provided on this card mounting on the common processor card. A 10-pin connector J23 for power and a 60-pin connector J22 for high-speed SERDES signals are used.

5.2.2 USB 2.0 Interface

The daughter card includes one USB 2.0 interface connected to the USB0 port of the AM65x processor through the SERDES connector. The USB signals are terminated to a USB micro B connector J13, and a supporting circuitry with a header J5 is included to allow the USB interface to be configured as a host.

A 2x3 header (J5) is provided to install the 2-position ganged shunt to configure the port for host mode, as shown in Figure 5-3. Place the shunt on pins 1 and 2 to enable bulk capacitance on VBUS, and place the shunt on pins 5 and 6 to connect the ID pin to ground.

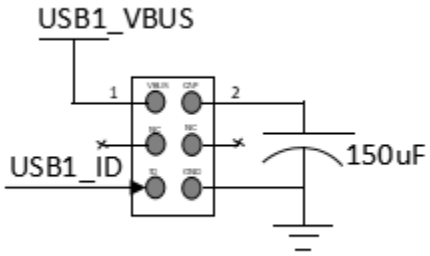

Figure 5-3. J5 Header for USB 2.0 Host Operation

The Personality board can provide maximum of 500 mA, 5 V to the slave device. A power switch is included to power the slave device, which is controlled by the DRV_VBUS signal from the AM65x processor.

5.2.3 PCIe Interface

The x2 lane PCIe daughter card includes one x4 lane PCIe connector J15 to accept PCIe form factor daughter cards and support PCIe Gen3 operation. The pin-out of the x1 lane connector follows PCIe standard. MCU_I2C is used for control. The link activation signals (WKUP) from the PCIe connectors are terminated to the SERDES connector, which is used to interrupt the processor in the processor board.

Reset: a 3-pin header J14 is provided to select the reset source for the host and end-point PCIe operation. Short pin 1 and pin 2 of the header J14 for device operation of the PCIe card, or short pin 2 and pin 3 for host operation of the PCIe card.

5.2.4 x2 Lane PCIe Personality Card Clocking

The PCIe reference clock can be sourced by the SoC, clock generator, or PCIe card depending on whether the SoC is configured for Root complex (RC) or End point (EP). A programmable clock generator is used to generate the 100-MHz HCSL clock to drive the PCIe reference clock input of the SOC.

Resistor options are provided to select the clock source for PCIe RC and EP operation, as explained below.

For PCIe RC operation, the reference clock can be sourced directly from the SOC to the PCIe EP or from the clock generator to the SoC and PCIe EP. Selection can be made through jumpers, as shown in Table 5-1.

Table 5-1. Selection of Reference Clock for PCIe Host Operation

Clock selected	Mount	Unmount
Reference clock for SOC from clock generator	R241	R246
	R240	R245
Reference clock for PCIe connector from SOC	R305	R252
	R306	R251
Reference clock for PCIe connector from clock generator	R252	R305
	R251	R306

For PCIe EP, the SOC clock input can be sourced by the PCIe RC or from the clock generator. Selection can be made through jumpers, as shown in Table 5-2.

Table 5-2. Selection of Reference Clock for PCIe Endpoint Operation

Clock selected	Mount	Unmount
Reference clock for SOC from clock generator	R241	R246
	R240	R245
Reference clock for SOC from PCIe connector	R246	R241
	R245	R240

5.2.5 Board ID EEPROM Interface

The PCIex2 daughter card is identified by its version and serial number, which are stored in the onboard EEPROM. The EEPROM is accessible on the address 0x54.

The AM65x CP board includes a CAT24C256W I2C EEPROM ID memory. The first 57 bytes of addressable EEPROM memory are preprogrammed with identification information for each board. The remaining 32711 bytes are available to the user for data or code storage.

Table 5-3. Board ID Memory Header Information

Header	Field Name	Nbr bytes	Comments
EE3355AA	MAGIC	4	Magic Number
	TYPE	1	Fixed length and variable position board ID header
		2	Size of payload
BRD_INFO	TYPE	1	payload type
	Length	2	offset to next header
	Board_Name	16	Name of the board
	Design_Rev	2	Revision number of the design
	PROC_Nbr	4	PROC number
	Variant	2	Design variant number
	PCB_Rev	2	Revision number of the PCB
	SCHBOM_Rev	2	Revision number of the schematic
	SWR_Rev	2	software release number
	VendorID	2	
	Build_Week	2	week of the year of production
	Build_Year	2	year of production
	BoardID	6	
	Serial_Nbr	4	incrementing board number
END_LIST	TYPE	1	End Marker

5.2.6 x2 Lane PCIe Personality Card Power

The daughter card receives 12-V, 5-V, and 1.8-V power from the processor card through a 10-pin power connector J23, and 3.3-V power from the SERDES connector. The daughter card includes a DC-DC converter to generate 3.3 V from 12 V to power the PCIe daughter cards.

6 Known Issues

The following issues exist on the E3 version of the IDK and the GP EVM.

6.1 Determining the Revision and Date Code for the EVM

The assembly revision of the board can be found on a sticker or in silkscreen on the top of the board.

The serial number that appears on the bar code sticker for the Maxwell EVM is in the following format.

32184P810082

The numbers represent the following using the above as an example:

32 – Build week. Board was built in the 32nd week of the year.

18 - Build year. Board was built in 2018

4P81 – Code for the Maxwell Common Processor Board

0082 – 82nd board built in this lot.

Most issues can be identified using the assembly revision, but some may also need the build date code.

6.2 Known Issues for the A, E4, and E3 Revision

The following issues exist on the A, E4, and E3 revision of the IDK and the GP EVM.

6.2.1 Lack of Reset for I2C IO Expander

ISSUE: The I2C IO Expanders (U110 and U7) provides additional control signals for the EVM. The I2C component does not include a reset input and is only reset to the default values when a power cycle is applied. Thus, if a PORz or warm reset occurs after the power is applied, the output values programmed into the IO expanders will not change. While most values can be reprogrammed by software after a reset is applied as a work-around, the expander does include the GPIO_eMMC_RSTn, GPIO_OSPI_RSTn, MMC1_SD_EN, and the GPIO_SPI0_RSTn signals. These signals hold the associated interfaces in a reset state if set to an active state. If a GPIO reset signal is applied to an interface that is used as a boot device, the boot will not succeed.

SOLUTION: In future versions of the board, an I2C IO expander with a reset input will be substituted for these devices.

WORKAROUND: There is no complete work-around for this issue. The customer should avoid leaving any boot interface in reset for extended periods of time. Even if the reset to this interface is pulsed active, there is a possibility of a reset occurring while the peripheral reset is active, preventing the board from booting. Boot software should reinitialize the I2C IO Expanders.

6.3 Known Issues for the E4 & E3 Revision

The following issues exist on the E4 & E3 revision of the IDK and the GP EVM. Some E4 revisions have been modified to include the 2.0 revision of the AM65 silicon, which required a number of blue wires. If blue wires have been place around U96, the board has the 2.0 silicon revision modifications.

6.3.1 Changes Unique to the E4 Revision Modified for 2.0 Revision

The addition of the 2.0 revision version of the AM65 EVM required a few changes. The initial voltage of the VDD_CORE supply was changed to 1.1 V from 1.0 V for earlier versions of the silicon. The MMC0 SDCD, MMC0_SDWP, MMC1_SDCD, and MMC1_SDWP were moved to a different IO bank in 2.0 revision, so the source voltage for the signals driving these pins was updated. 49.9K pull-up resistors for MMC0_DAT0-7 and MMC0_CLK signals. For more information about these changes, review the Silicon Errata document.

6.4 Known Issues for the E3 Revision

The following issues exist on the E3 revision of the IDK and the GP EVM. All E3 revisions of the EVM have the 1.0 revision of the silicon installed.

6.4.1 Resonance Observed on the SoC Side of Some Filters Associated with VDDA_1V8

ISSUE: A resonance was observed between the filter and the SoC for the following power pins due to a lack of bulk capacitance after the filter.

- FL16 VDDA_3P3_IOLDO_WKUP
- FL22 VDDA_SRAM_CORE
- FL23 VDDA_SRAM_MPU
- FL25 VDDA_WKUP_LDO
- FL27 VDDA_GP1
- FL29 VDDA_GP9
- FL30 VDDA_GP3

This has led to some noise on the internal power supply rails, resulting an increase in jitter on the Ethernet subsystem source clocks.

SOLUTION: A 4.7-uF capacitor was added from the SoC side of the above filters to ground to add sufficient bulk capacitance to dampen the resonance. Customers should include a footprint for a 4.7-uF capacitor in their designs to avoid this issue.

WORKAROUND: 4.7-uF capacitors can be added to the specified rails if problems are observed. Contact Texas Instruments for specific instructions if the change is needed.

6.4.2 Additional LDO Power Supply Needed for VDDA_1P8_SERDES0

ISSUE: The LP5912-1.8DRVT U60 on the common processor board is rated at 500 mA. It is used to drive the analog 1.8-V inputs to the AM6548. Initial testing has shown that this supply is underrated in some use cases.

SOLUTION: Customers should include a second 500-mA LDO specifically for the VDDA_1P8_SERDES0 power input on pins AA14, AB13, and AB15. This resolves the issue with U60.

6.4.3 Length of the RESET Signal to the PCIE Connectors on the SERDES Daughter Card

ISSUE: The RESET signal going to the PCIE daughter card is controlled by the PORz_OUT and a GPIO signal. The reset signal goes high when PORz_OUT is deactivated. This does not allow the software time to prepare for the release of the reset.

SOLUTION: Customers should ensure that the PCIE reset is extended until the software is ready to remove the PCIE from reset. The next revision of the EVM will include a pull-down resistor on the GPIO control for the PCIE reset signal, holding the connector in reset until the GPIO is set high by software.

WORKAROUND: Software can place the GPIO low to put the PCIE in reset, and then release the reset when the software is ready.

6.4.4 The PORz_OUT and MCU_PORz_OUT Signals Go High During Power Sequencing

ISSUE: The logic controlling the PORz_OUT and MCU_PORz_OUT signals requires clock and the VDD_CORE supply before it drives these signal low. During a power sequence, the PORz_OUT and MCU_PORz_OUT will start to rise when the I/O voltage for the VDDS0_WKUP is applied. They remain high until the VDD_CORE is applied. When VDD_CORE is present, the PORz_OUT and MCU_PORz_OUT are driven low and remain low until the part is released from reset.

SOLUTION: Customers should include a pull-down resistor on PORz_OUT and a separate pull-down resistor on MCU_PORz_OUT. This keeps these signals low until the part is released from reset.

6.4.5 Orientation of the Current Monitoring Shunt Resistors

Note

This issue was corrected on revision E3 with date codes of 39-18 or greater.

ISSUE: The footprint for the shunt resistors needed by the INA226 current monitoring circuits for VDD_CORE, VDD_MCU, and SoC_DVDD3V3 is not correct.

SOLUTION: The footprint will be rotated by 90 degrees in the next revision of the EVM.

WORKAROUND: Although this issue does not affect the operation of the board, it will give incorrect values if the current is read for the three rails listed above. The resistors can be installed rotated by 90 degrees if that capability is needed.

6.4.6 SD Card IO Supply Capacitance

Note

This issue was corrected on revision E3 with date codes of 37-18 or greater.

ISSUE: As described in i2026 in the AM65 Errata document, the MMCSD is subject to negative current that exposes the device to damage. Changes were made to the capacitance to minimize the impact to the device.

SOLUTION: This issue will be solved in the next revision of the AM65 device.

WORKAROUND: As stated, this only minimizes the effects described in i2026. The capacitor to ground connected to the CAP_VDDA_1P8_SDIO pin was changed to 3 uF, and a 270 ohm pull-down resistor was added.

6.4.7 PHY Resistor Strapping Changed to Disable EEE Mode

Note

This issue was corrected on revision E3 with date codes of 36-18 or greater.

ISSUE: Initially the Ethernet PHY was strapped to enable the EEE mode. Pin strapping for this mode is not working correctly due to an issue with the PHY. The strapping was changed to disable the EEE mode and enable the auto negotiation.

SOLUTION: The values of the pulling resistors for the RX_CTRL signal are modified to the values for mode 3. See the data manual of the Ethernet PHY for more details.

WORKAROUND: Change R145, R98, and R554 to 5.76K ohm 1% resistors. Change R146, R99, and R553 to 2.94K ohm 1% resistors.

6.4.8 The I2C Address for the I2C Boot Memory changed to 0x52

Note

This issue was corrected on revision E3 with date codes of 36-18 or greater.

ISSUE: The I2C memory available for boot is configured to address 0x54, but the boot rom only supports boot from address 0x50-0x53.

SOLUTION: Change the resistors installed to set the I2C address for U9 to 0x52.

WORKAROUND: Remove R20 and R22. Install a 10K ohm resistor for R21 and R19.

7 Configuring the PRG0 and PRG1 Ethernet Interface to MII

The IDK Application card can be configured to support the use of the MII interface between the AM65 and the Ethernet PHYs. The modification is only supported on the revision E4 or A IDK applications boards. Revisions E3 and earlier of the IDK application board only support the RGMII interface.

7.1 Ethernet PHY Initial Conditions and TX Clock Signal Change

These changes are needed to configure the Ethernet PHYs for MII, regardless of the revision of AM65 silicon installed on the common processor board.

7.1.1 Ethernet PHY0 Clock and Initial Condition for MII

The following modifications are needed for PHY0 (U52) to convert it for use with the MII interface.

Clock modification – The clock resistors for U52 is on the bottom of the board. Remove R452 and install a zero ohm resistor for R453.

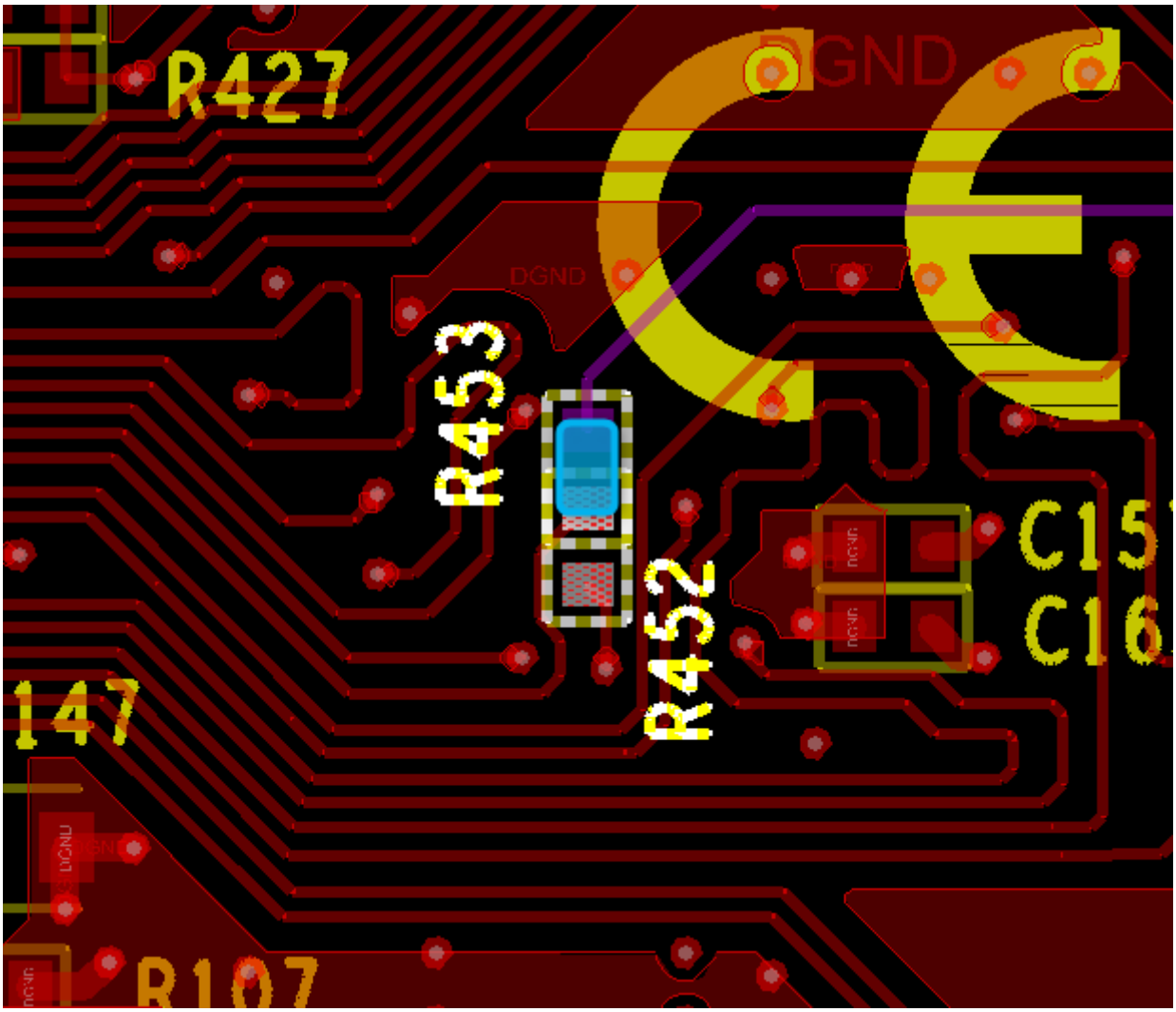

Figure 7-1. PHY0 TX Clock Modification

Configuration modification – The circuit for U52 is on the top of the board. Add three zero ohm 0402 resistors to R445, R290, and R444 to configure the interface for MII.

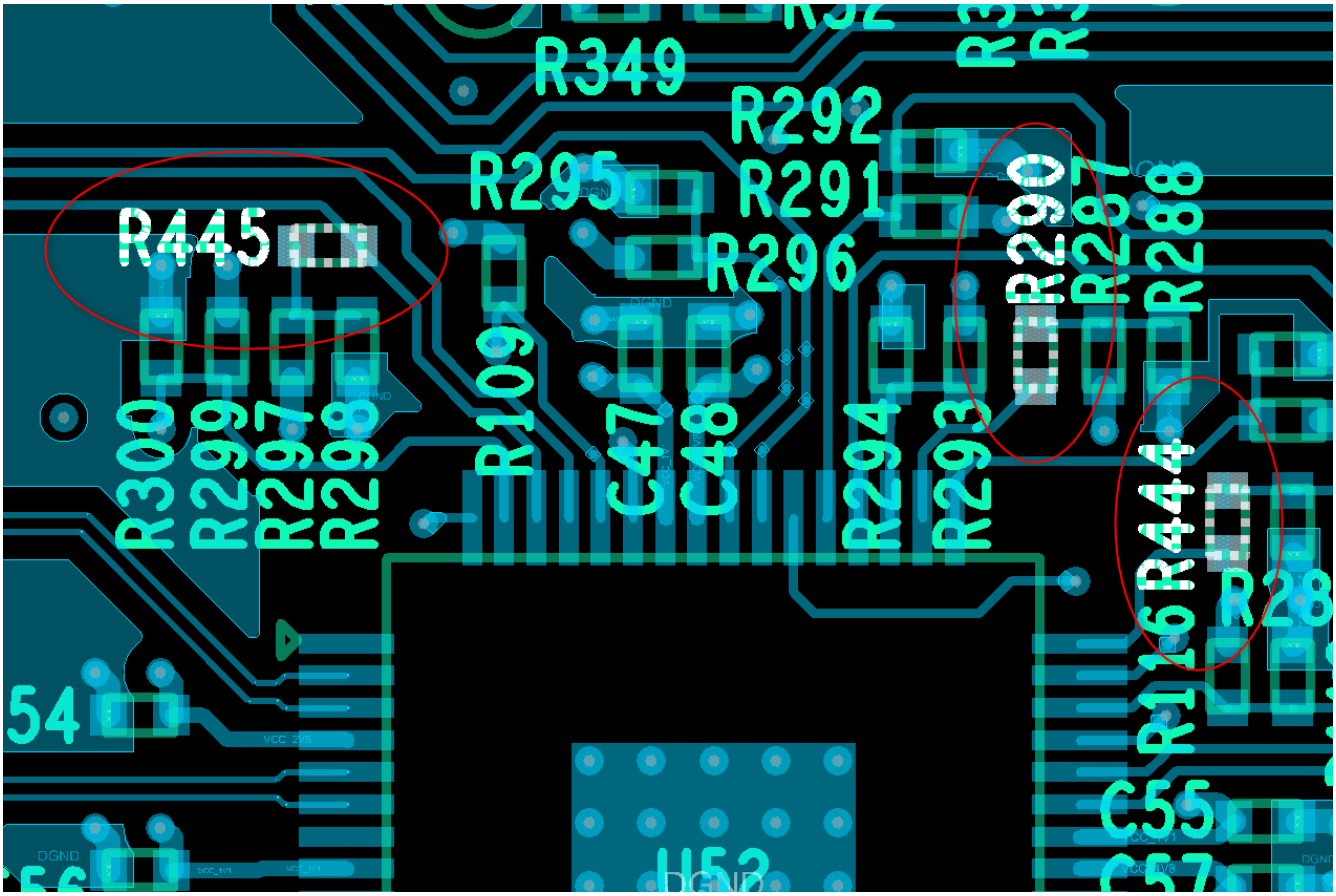

Figure 7-2. PHY0 Initial Condition Modification

7.1.2 Ethernet PHY1 Clock and Initial Condition for MII

The following modifications are needed for PHY1 to convert it for use with the MII interface.

Clock modification – The clock resistors for U9 is on the top of the board. Remove R454 and install a zero ohm resistor for R455 as shown in Figure 7-3.

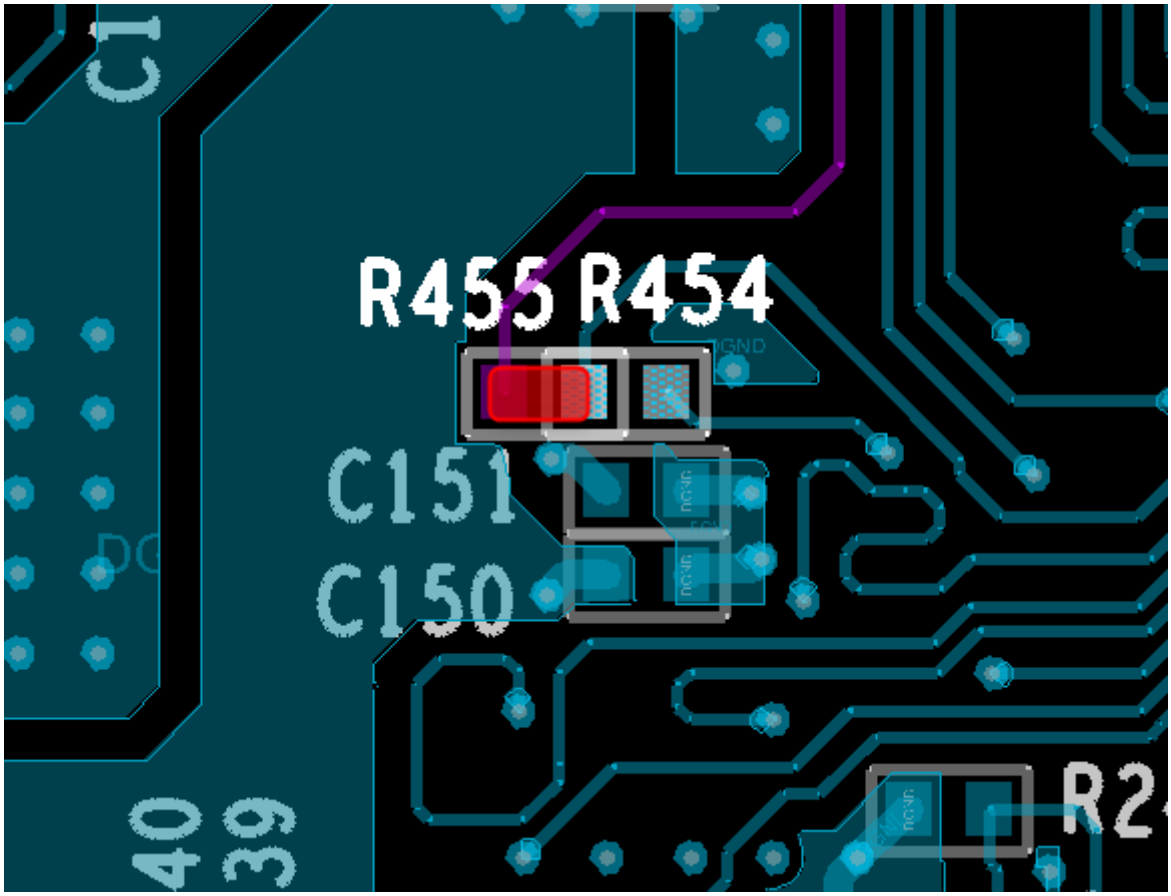

Figure 7-3. PHY1 TX Clock Modification

Configuration modification – The circuit for U9 is on the bottom of the board. Add three zero ohm 0402 resistors to R446, R338, and R447 to configure the interface for MII.

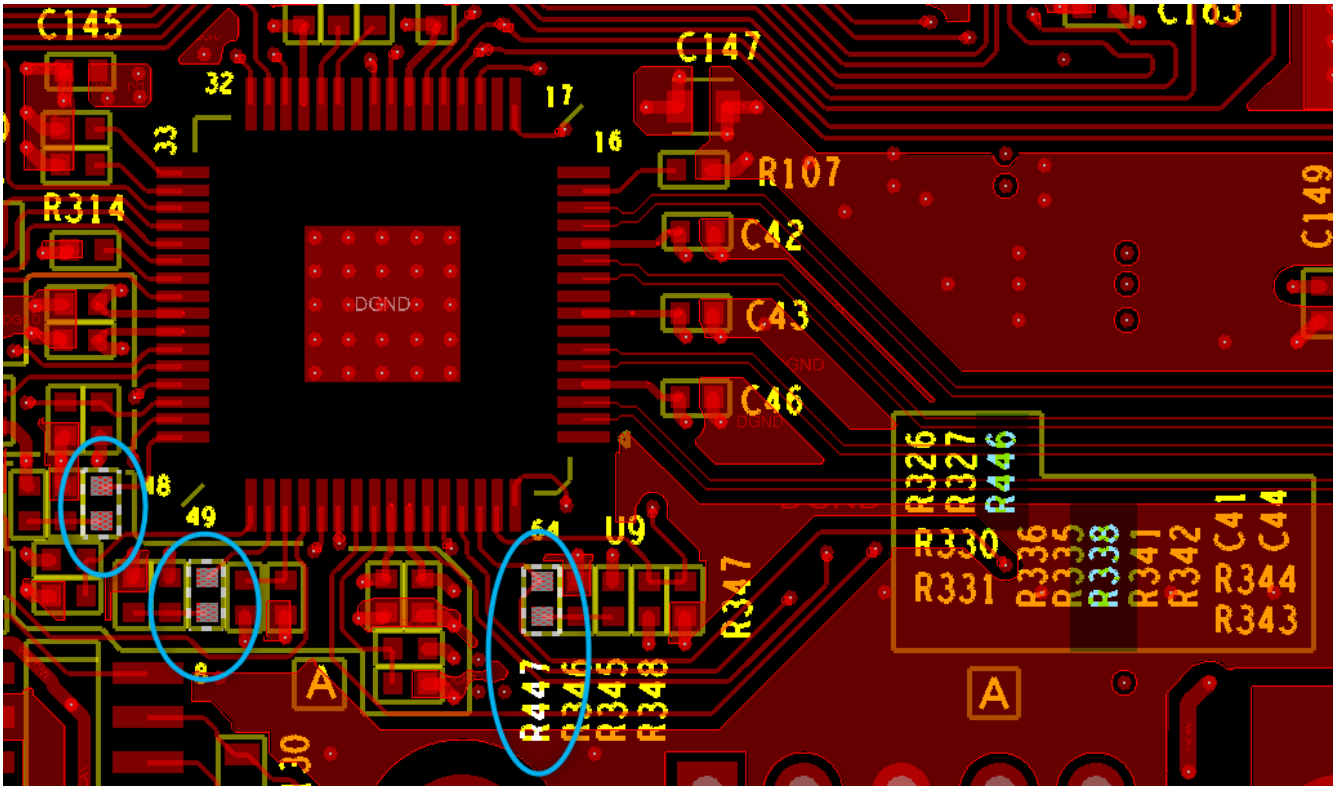

Figure 7-4. PHY1 Initial Condition Modification

7.1.3 Ethernet PHY2 Clock and Initial Condition for MII

The following modifications are needed for PHY2 (U4) to convert it for use with the MII interface.

Clock modification – The clock resistors for U4 is on the bottom of the board. Remove R456 and install a zero ohm resistor in the footprint for R457 as shown in Figure 7-5.

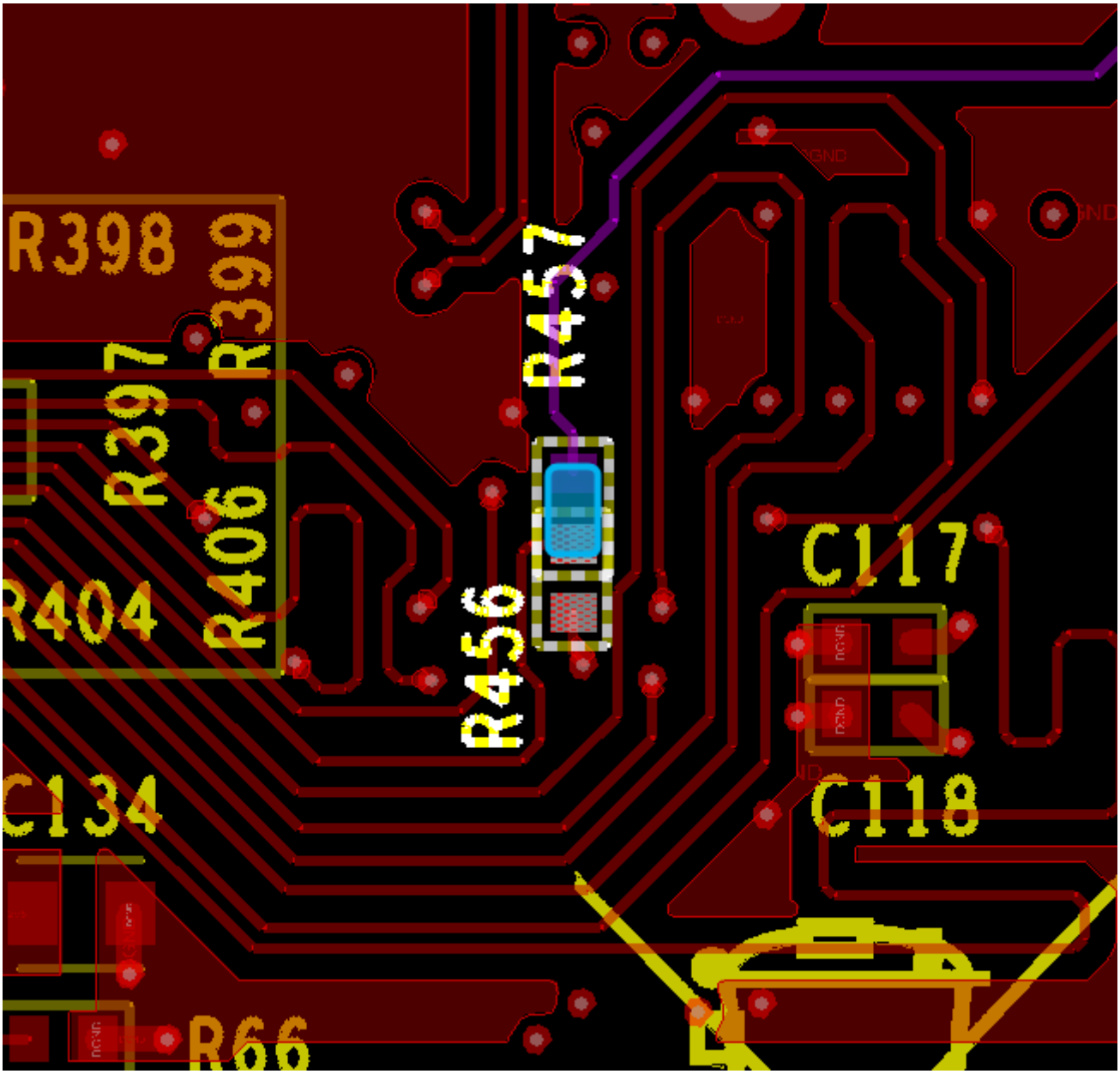

Figure 7-5. PHY2 TX Clock Modification

Configuration modification – The circuit for U4 is on the top of the board. Add three zero ohm 0402 resistors to R449, R378, and R448 to configure the interface for MII.

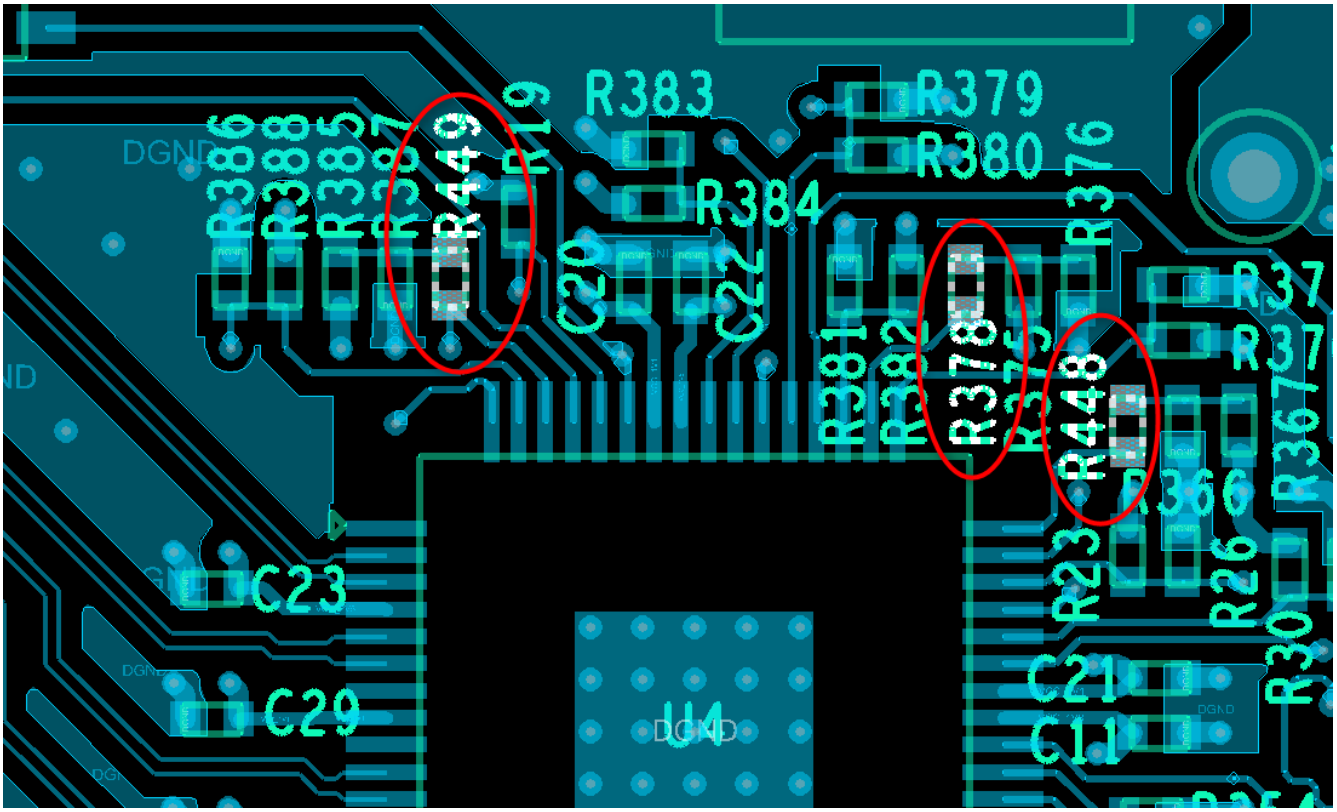

Figure 7-6. PHY2 Initial Condition Modification

7.1.4 Ethernet PHY3 Clock and Initial Condition for MII

The following modifications are needed for PHY3 (U7) to convert it for use with the MII interface.

Clock modification – The clock resistors for U7 is on the top of the board. Remove resistor R458 and install a zero ohm resistor for R459 as shown in Figure 7-7.

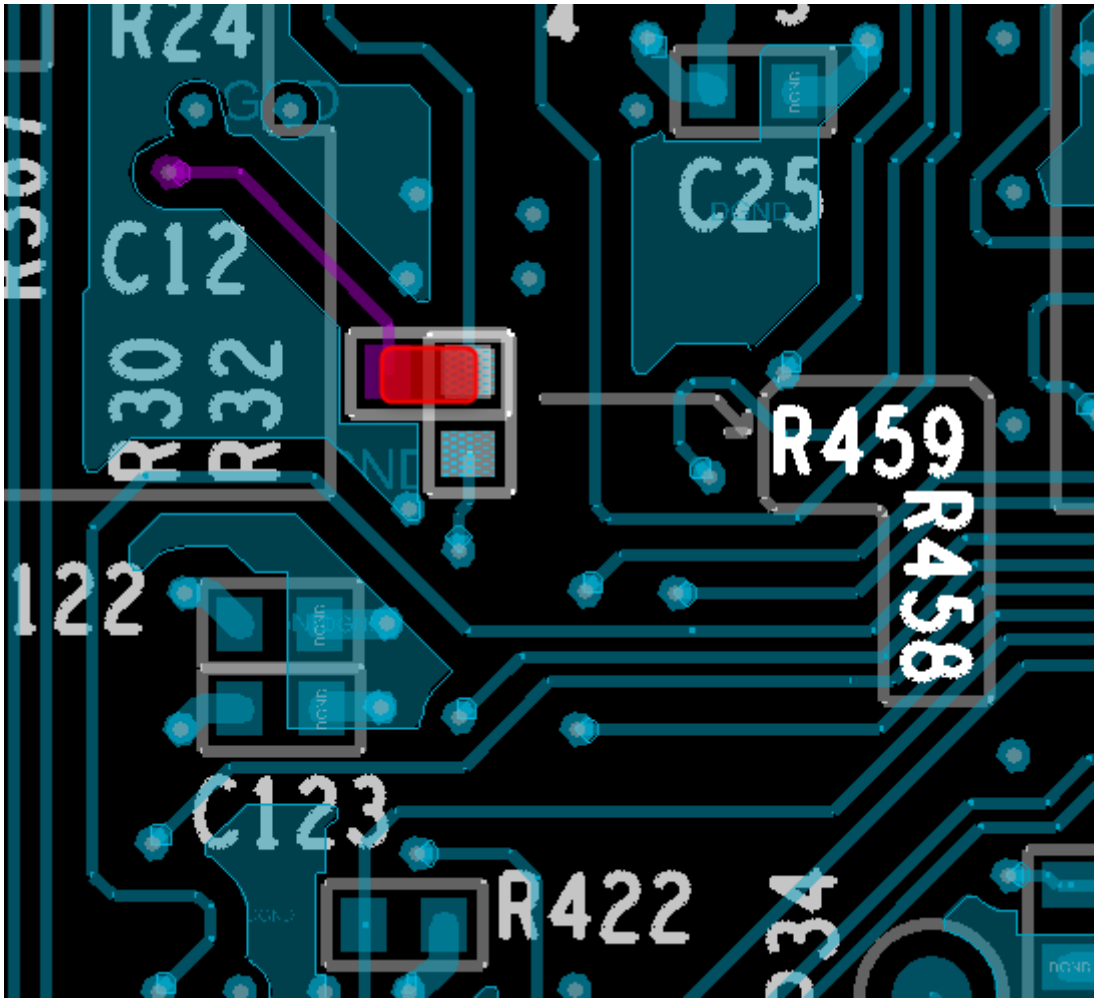

Figure 7-7. PHY3 TX Clock Modification

Configuration modification – The circuit for U7 is on the bottom of the board. Add three zero ohm 0402 resistors to R450, R420, and R451 to configure the interface for MII.

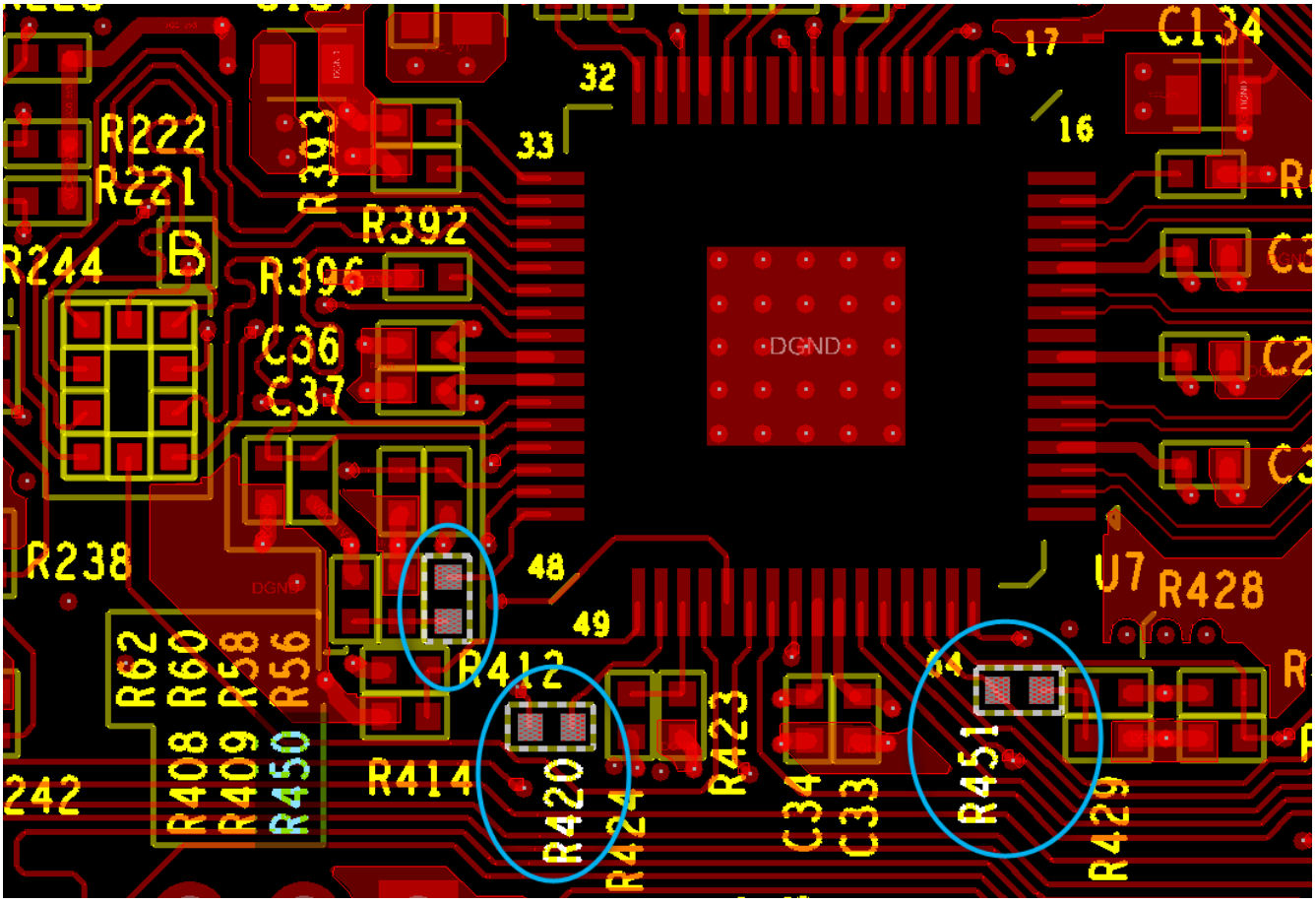

Figure 7-8. PHY3 Initial Condition Modification

7.2 Ethernet PHY and TX Data Signals Change

If the Common Processor board has revision 2.0 of the AM65x silicon, the TX Data and Control signals can be connected to the correct pins on the PHY using the alternate MII TX signal pin muxing. If the alternate pin muxing is selected, no additional changes to the board are needed.

The alternate pin muxing for the TX signals was added in the 2.0 revision of the AM65x silicon. If the Common Processor Board has a revision 1.0 silicon or the default pinmux is desired, an additional modification to the board is needed.

The change involves using an alternate resistor installation pattern for the TX signal steering circuit on the IDK Application board. Figure 7-9 illustrates the difference between the installations of the TX steering resistors for RGMII as delivered on the left vs the installation for MII on the right. Note the clockwise shift in the installation

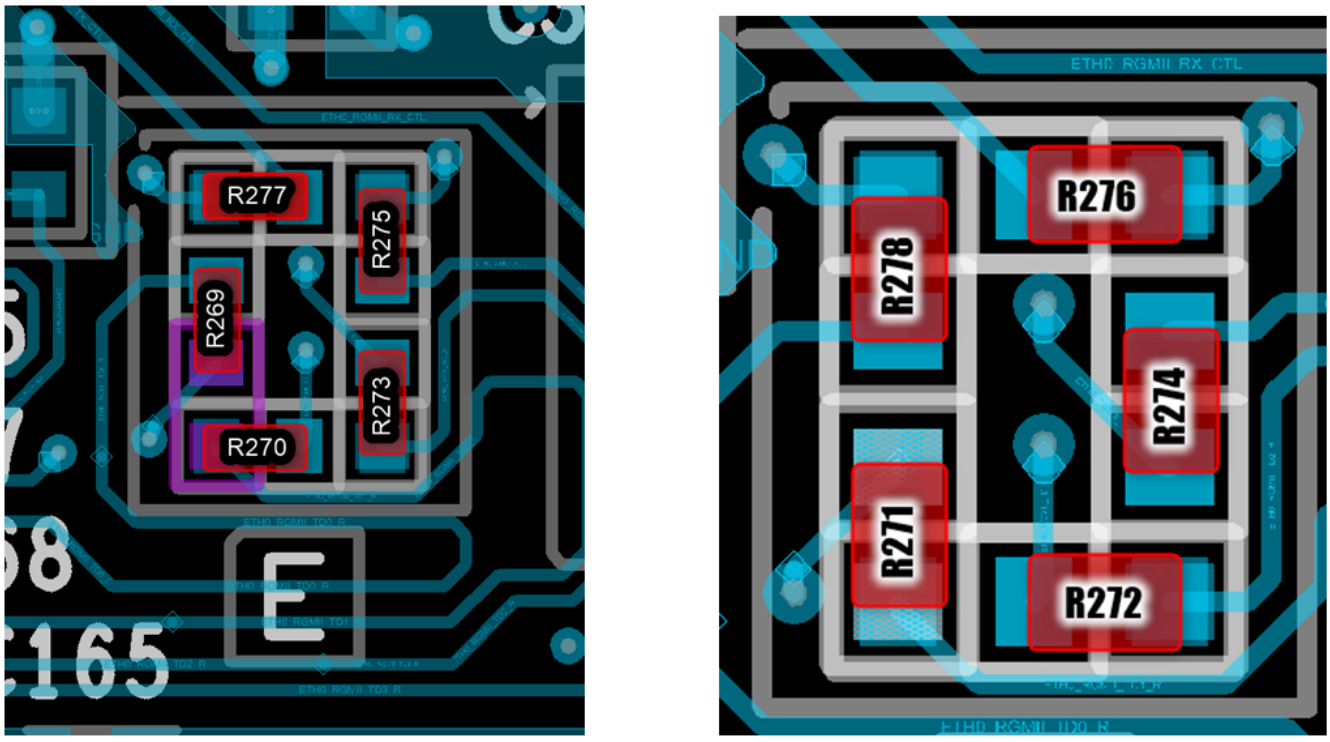

Figure 7-9. PHY0 TX Steering Resistors RGMII Configuration vs MII Configuration

7.2.1 Ethernet PHY0 TX Data Signals for MII

The following modifications are needed for PHY0 (U52) to convert it for use with the MII interface using the default pinmuxing.

TX lane steering modification – The TX lane is steered with a block of shared pad resistors. The resistors are installed in one pattern for RGMII and the opposing pattern for MII. Remove all five resistors from the steering block and replace them in the pattern shown in Figure 7-10.

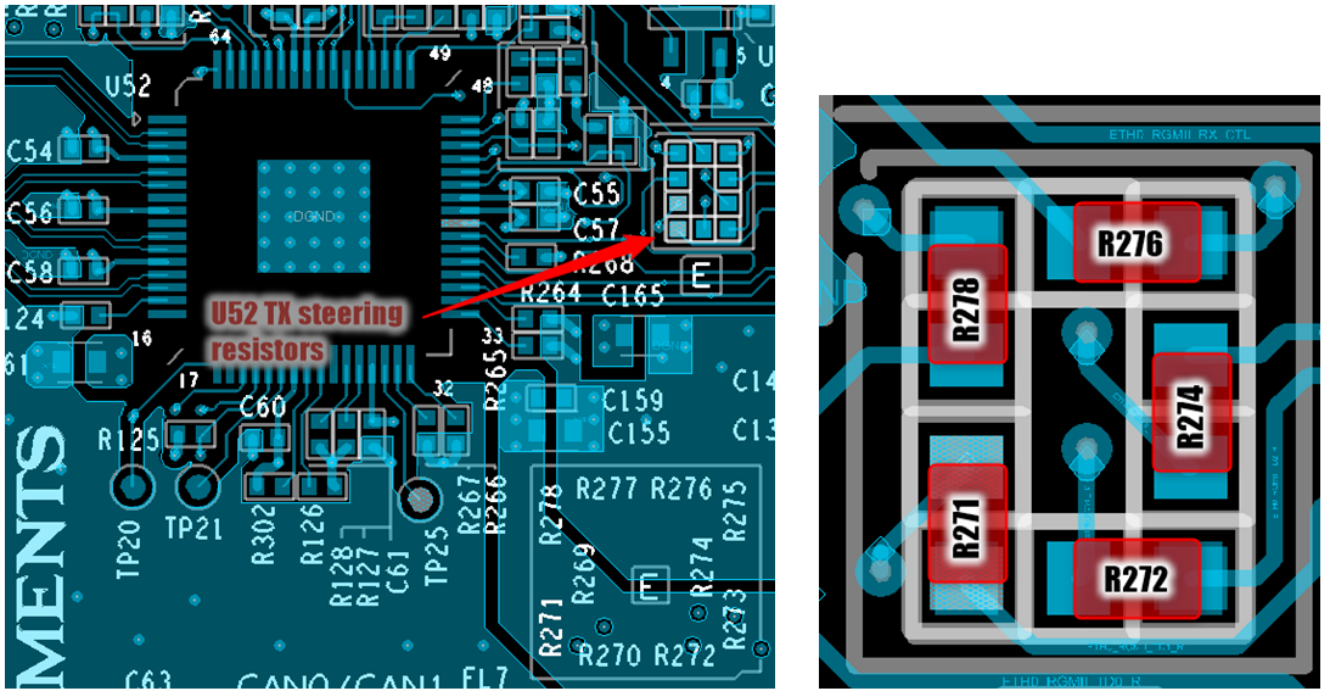

Figure 7-10. PHY0 TX Steering Resistors MII Configuration

7.2.2 Ethernet PHY1 TX Data Signals for MII

The following modifications are needed for PHY1 (U9) to convert it for use with the MII interface using the default pinmuxing.

TX lane steering modification – The TX lane is steered with a block of shared pad resistors. The resistors are installed in one pattern for RGMII and the opposing pattern for MII. Remove all five resistors from the steering block and replace them in the pattern shown in Figure 7-11.

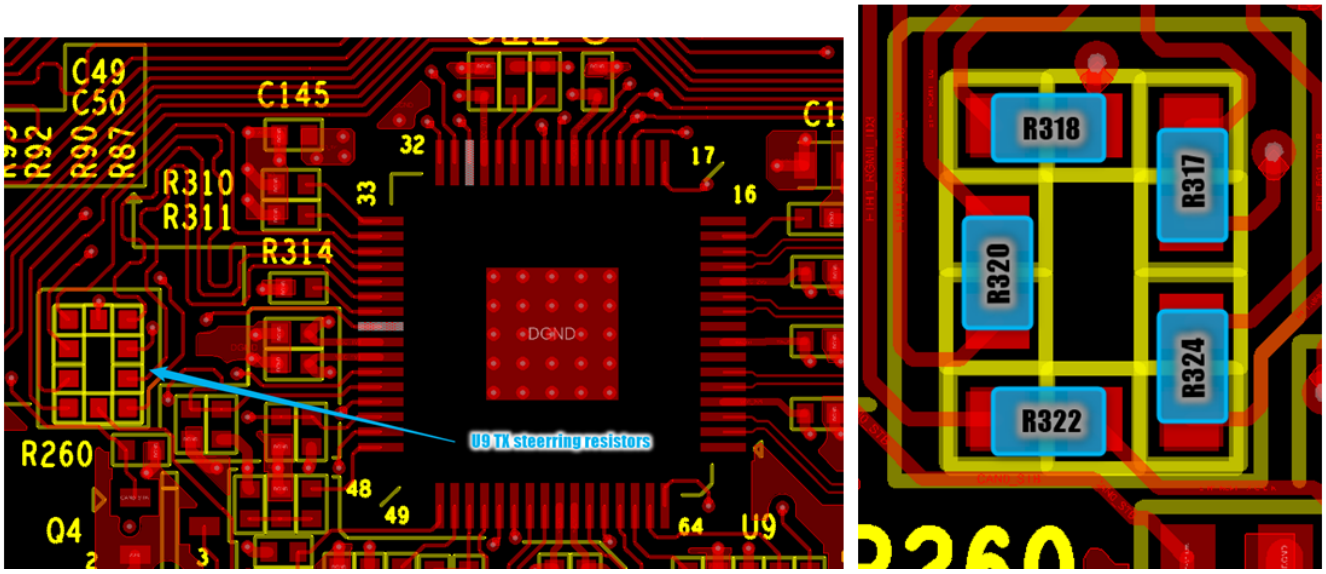

Figure 7-11. PHY1 TX Steering Resistors MII Configuration

7.2.3 Ethernet PHY2 TX Data Signals for MII

The following modifications are needed for PHY2 (U4) to convert it for use with the MII interface using the default pinmuxing.

TX lane steering modification – The TX lane is steered with a block of shared pad resistors. The resistors are installed in one pattern for RGMII and the opposing pattern for MII. Remove all five resistors from the steering block and replace them in the pattern shown in Figure 7-12.

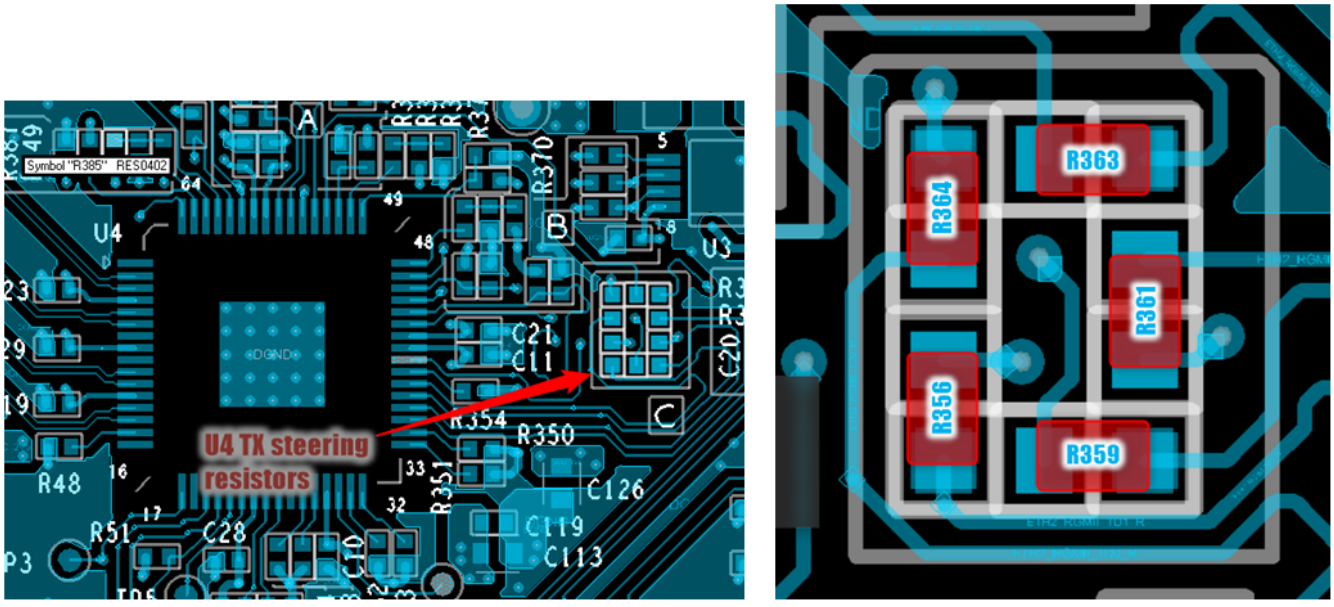

Figure 7-12. PHY2 TX Steering Resistors MII Configuration

7.2.4 Ethernet PHY3 TX Data Signals for MII

The following modifications are needed for PHY3 (U7) to convert it for use with the MII interface using the default pinmuxing.

TX lane steering modification – The TX lane is steered with a block of shared pad resistors. The resistors are installed in one pattern for RGMII and the opposing pattern for MII. Remove all five resistors from the steering block and replace them in the pattern shown in Figure 7-13.

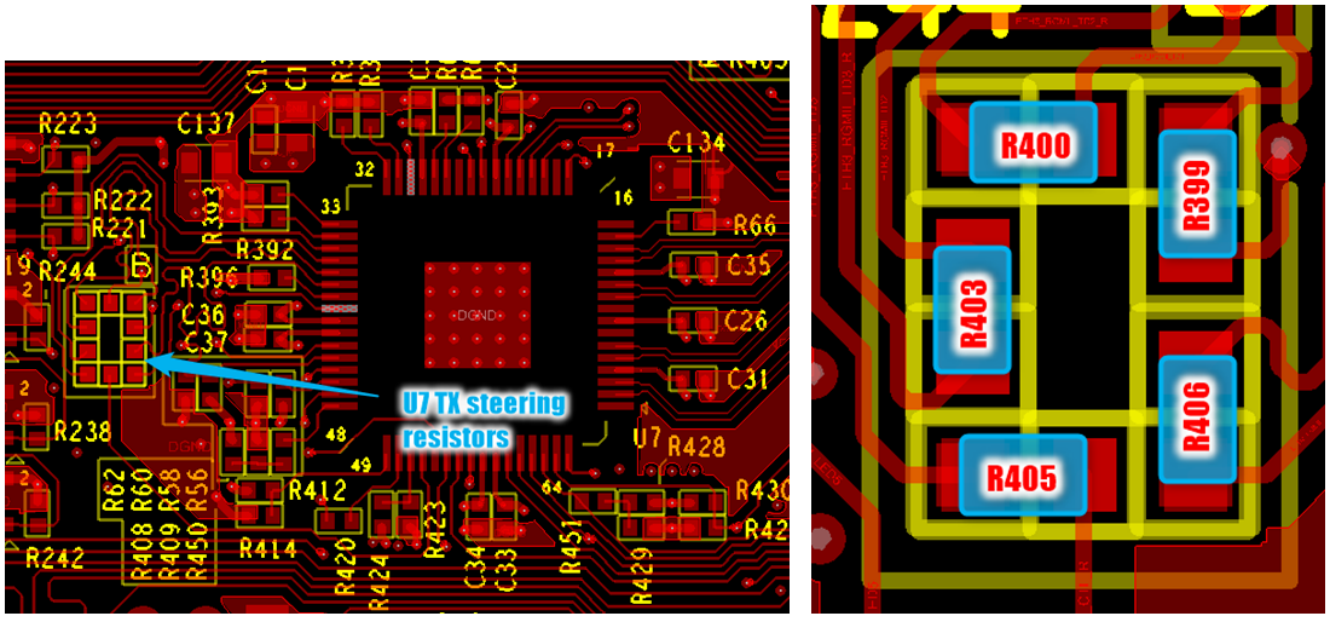

Figure 7-13. PHY3 TX Steering Resistors MII Configuration

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from October 1, 2018 to October 31, 2020 (from Revision () to Revision A ())	Page
• Updated Title to AM65x	2
• Added Determining the Revision and Date Code for the EVM section	72
• Added Known Issues for the A, E4, and E3 Revision section	72
• Added Known Issues for the E4 & E3 Revision section	72
• Added Known Issues for the E3 Revision section	72
• Added Orientation of the Current Monitoring Shunt Resistors section	73
• Added SD Card IO Supply Capacitance section	74
• Added PHY Resistor Strapping Changed to Disable EEE Mode section	74
• Added The I2C Address for the I2C Boot Memory changed to 0x52 section	74
• Added Configuring the PRG0 and PRG1 Ethernet Interface to MII section	75

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