User's Guide
SPRUIL9–October 2018

# AM654x/DRA80xM BGA Escape Routing

This document provides a sample PCB escape routing for the AM654x/DRA80xM SoC. The AM654x/DRA80xM has multiple functions assigned to each pin, making it impossible to provide an escape for all permutations of pinmux definitions. The escape presented here is based on the AM654x/DRA80xM GP EVM and the pinmux defined for that design.

The strategy provided within is designed to help ensure a successful escape. Care must be taken to escape the signals with the most layout constraints early in the routing process. This document does not include those constraints. For additional information on routing these signals refer to the *High-Speed Interface Layout Guidelines*. Care must also be taken to ensure that a robust power delivery network is provided. For additional information, refer to the *Sitara™ Processor Power Distribution Networks: Implementation and Analysis*.

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## Trademarks

# 1 Stackup

The PCB layout designer must balance many different requirements when starting a PCB layout. The first is the board stackup. The AM654x and DRA80xM devices have a 23-mm × 23-mm package which has a 0.80-mm pitch ball array of 28×28. To minimize cost, this ball grid is a solid array. Due to the number of rows of signal balls around the periphery, designs must have four routing layers, not counting the top and bottom layers, which can also contain some signal routes. Also, due to the number of power supply rails, there must be three layers dedicated for power planes. Ground planes must be added adjacent to the power planes and adjacent to the outer layers for shielding and controlled impedance routing. High-speed interfaces such as the SERDES and the DDR require ground planes for impedance matching. Due to the higher speeds, ground layers both above and below the DDR signals are recommended Thus, designs that route out all of the signal balls require a 14-layer stackup similar to the one listed in Table 1.

**Table 1. PCB Layer Stack-up**

| PCB Layer | Layer Routing, Planes or Pours |
|---|---|
| Layer 1 | Component pads and signal routing |
| Layer 2 | Ground |
| Layer 3 | Signal routing(1) |
| Layer 4 | Ground |
| Layer 5 | Signal routing(1) |
| Layer 6 | Power |
| Layer 7 | Power |
| Layer 8 | Power |
| Layer 9 | Ground |
| Layer 10 | Signal routing(1) |
| Layer 11 | Ground |
| Layer 12 | Signal routing(1) |
| Layer 13 | Ground |
| Layer 14 | Component pads (including most decoupling) and signal routing |

(1) Bracketing the signal routing between two ground planes eliminates broadside coupling to prevent crosstalk problems.

A 14-layer stack-up similar to the one above is needed for relatively dense PCBs. Alternately, the layer count can be reduced, assuming one or more of the following exist:

- The PCB is not crowded around the AM654x device. This allows for more routing away from the device on the top and bottom layers, which can reduce layer congestion.
- Many of the signal balls are unused. Many designs do not use all of the interfaces, resulting in unused signal balls. This also reduces routing congestion.
- The PCB layout team has time to carefully place the routes. This can be very time consuming.

It is not acceptable to violate routing rules simply to save money on reduced PCB layers or due to limited routing time. All requirements must still be met. Also, creative routing increases design validation time, both in simulation and bench testing. This can be minimized if the layout is similar to one of the AM654x EVM designs.

The AM654x EVM is implemented in a 14-layer stack-up, similar to the one described in Table 1. This design has nearly every signal ball routed to circuitry or a connector. This drives the requirement for the full number of layers. Additionally, this board is designed for optimum signal integrity on the high-speed interfaces while limiting the board size. The AM654x EVM is implemented without a High Density Interconnect (HDI) and does not use microvias. All vias on the AM654x EVM pass completely through the board. This complicates the escape from the BGA

## 2 Floorplan Component Placement

Optimum trace routing will have routes as short as possible with a minimum of cross-over. This requires careful placement of the components around the AM654x device. Figure 1 shows the default arrangement of the signal balls and the power and ground balls. Some of the interfaces can move to other locations due to pin multiplex choices, and there are other interfaces not listed that are exposed through pin multiplex choices. The PCB layout team must analyze the locations of the interfaces used and the associated components or connectors.

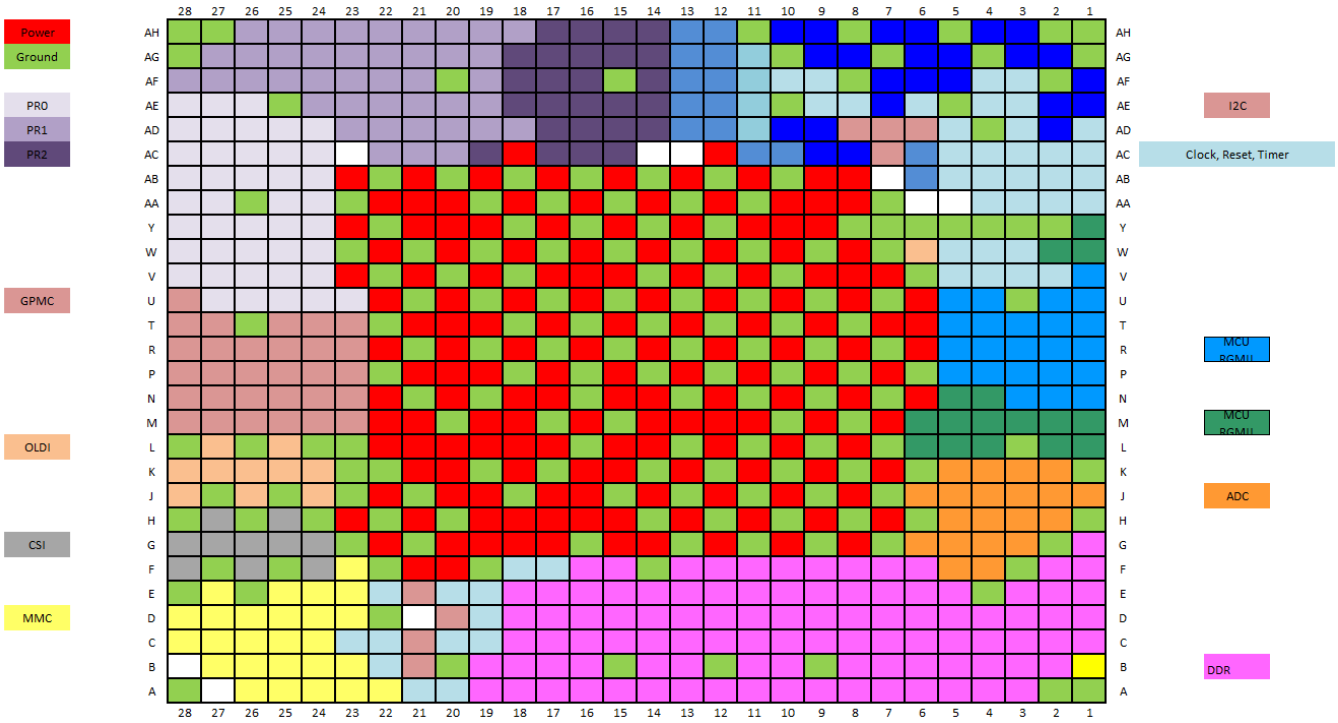



**Figure 1. AMC54x Floorplan**

## 3 Critical Interfaces Impact Placement

Placement of the AM654x device and some of the components or connectors is also dictated by some of the highest performance interfaces. Additionally, due to the PCB losses at multi-gigabit rates, there are routing distance limits that may also limit component placement.

## 4 Route Critical Interfaces

As indicated above, critical interfaces affect component placement options. When routing begins, these critical interfaces must be routed first. The design team must establish a priority for the different interfaces. Those with higher priority must be completed before implementing those of lower priority. PCB layout teams often waste considerable effort ripping up and re-routing traces for lower priority interfaces when deficiencies are found in the routing of more critical interfaces. Always complete routing for the critical interfaces first.

Table 2 lists a recommended priority order for interfaces contained on the AM654x family of devices. Individual design requirements may cause this list to change, but this provides a good baseline.

**Table 2. Routing Priority**

| Interface | Routing Priority |
|---|---|
| PCIe/USB3 | 10 (Highest Priority) |
| DDR3/DDR4/LPDDR4 | 9 |
| USB2, OSPI, CSI2 | 8 |
| Power distribution | 7 |
| RGMII | 6 |
| QSPI, OLDI | 6 |
| eMMC | 5 |
| Parallel Video | 5 |
| Clocks | 5 |
| MII / RMII | 4 |
| SPI | 4 |
| Motor control | 4 |
| Analog audio | 3 |
| GPMC | 2 |
| GPIO | 1 |
| UART | 1 |
| I2C | 1 (Lowest Priority) |

The placement of most of these should appear obvious. The multi-gigabit SERDES interfaces are the most critical due to their data rate and loss concerns. PCIe is at the top because it is very sensitive to PCB losses. The limited length for these routes might affect the PCB placement of the PCIe connector and the AM654x device. PCIe signals are found on the outer rings of the BGA footprint, allowing the traces to escape from the BGA without vias.

The asynchronous and low-speed interfaces are at the bottom. This leaves the synchronous and source-synchronous interfaces on the top, ordered by data rate. Power distribution is often left to last, but this can then result in poor decoupling performance or current starvation and excessive power supply noise, due to insufficient copper to carry the power and ground currents. Space for copper and decoupling must be allocated before routing the middle and low priority interfaces.

## 5 Route SERDES Interfaces

The previous section highlighted priorities for the PCB routing. The BGA ball map is also arranged to support routing the highest priority interfaces first. For additional information on routing these signals, refer to the *High-Speed Interface Layout Guidelines*. Most of the PCIe/USB3 SERDES interfaces are located on the outer two rings, allowing them to route away from the device without requiring vias. See Figure 2 for the routing of the SERDES signals on the AM654x EVM on the top layer. The trace widths must narrow as they approach the device, to allow them to pass between the pads. Wide traces were used on the EVM to limit the signal loss. Series capacitors are needed on the SERDES signals. These capacitors are closer to the daughter card connector on the AM654x GP EVM design, but should be placed closer to the SoC for your layout. The selection of the SERDES interface determines whether series capacitors are needed on the TX pair or the RX pair.

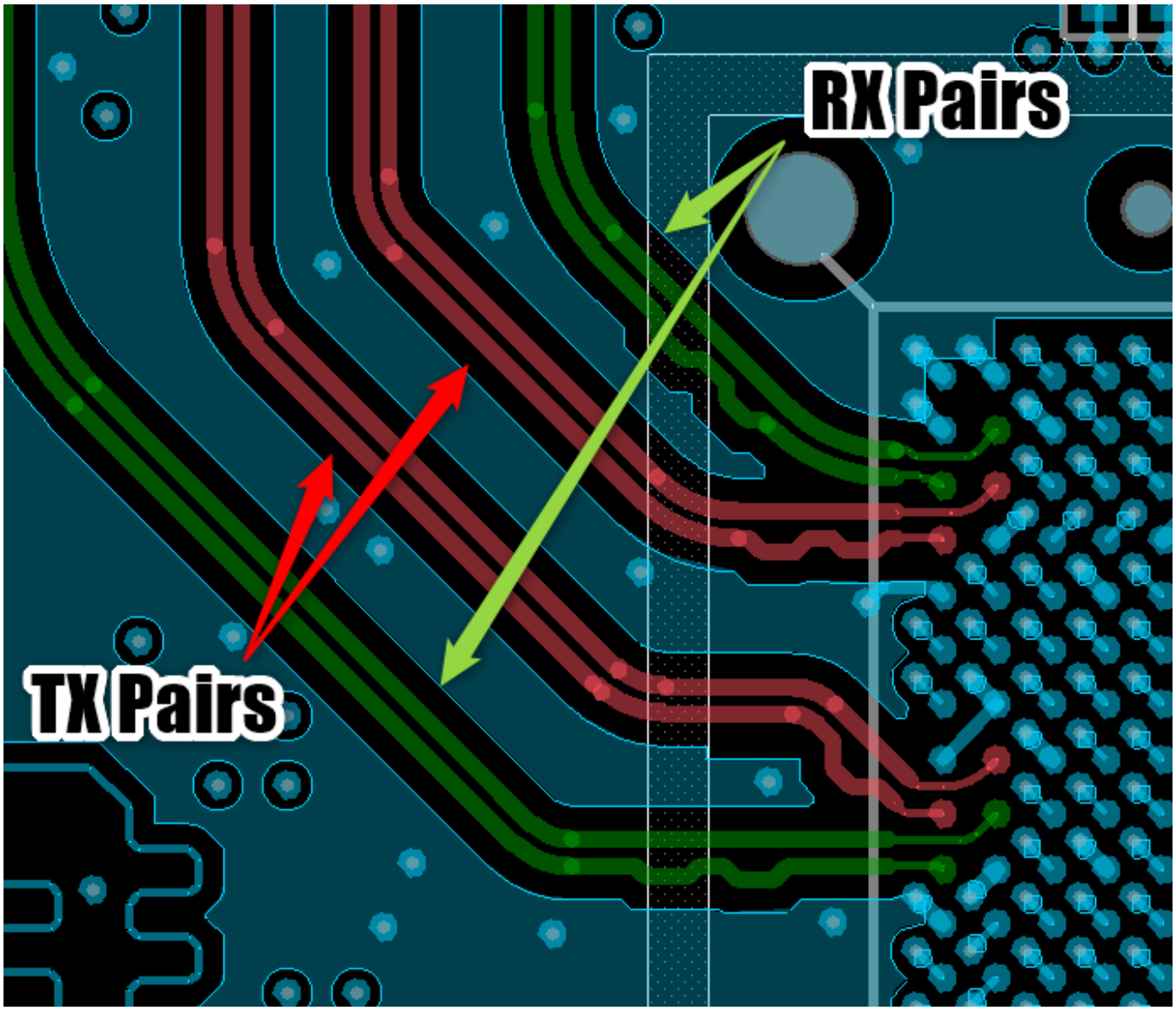



**Figure 2. SERDES Escapes**

## 6 Route DDR Signals

The AM654x supports connection to DDR3, DDR4, and LPDDR4 devices. The DDR signals must be routed next. Refer to the AM654x data sheet (SPRSP08B) for detailed recommendations for DDR routing. The images below show the BGA breakout for the DDR4 on the AM654x GP EVM. Routing for DDR3 and LPDDR4 uses a similar escape.

The DDR4 SDRAM memory devices should be arranged so that the data group balls are closest to the AM654x device. This allows the data group nets to have the shortest possible routing. The Address, Command, and Control signals operate at half the bandwidth of the data, so they are expected to be longer.

## 6.1 Data Group Routes

The following three images show the data group routing for the first DDR4 port. The PCB layout designer grouped all 11 nets for each byte group on a single layer. This is not a requirement, but it is strongly recommended as this simplifies the signal length and delay matching requirements, because the barrel length of the vias is the same for all the signals in the entire byte lane.

The DDR4 design for the AM654x GP EVM includes five 8-bit devices for a 32-bit data bus, plus 7 check byte bits for ECC. The order of the bytes is determined by the order of the bytes on the AM654x. The routing layers shown in Figure 3 include the top, layer 10, and layer 12.

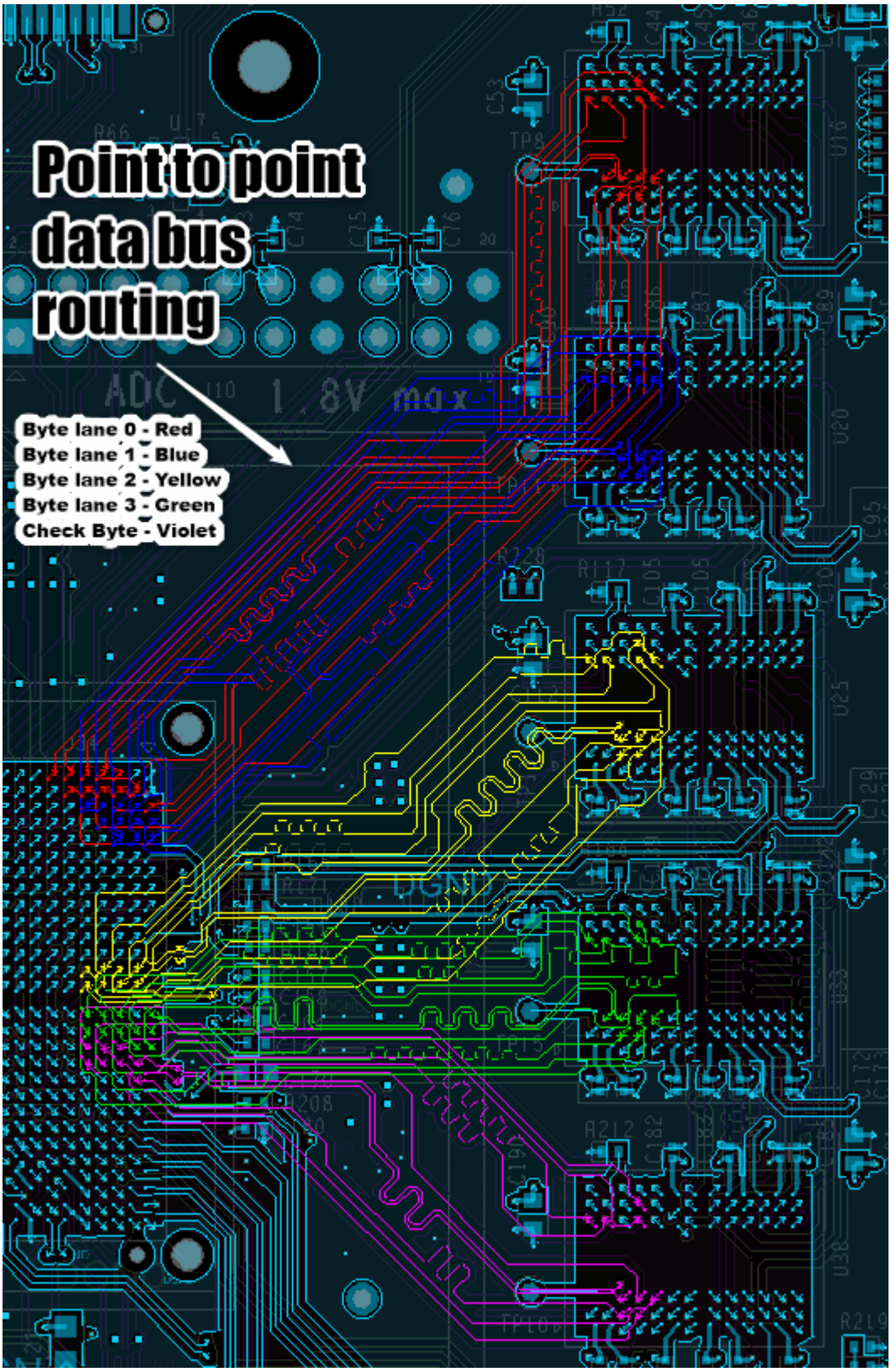



**Figure 3. DDR4 Data Bytes**

Figure 4 shows escape of the signals on the top layer of the board. Most of the routing is not on the top layer. Most of the DDR signals are connected directly to a via within the BGA footprint. Signals travel through traces routed on the top and bottom layers at a different speed than traces routed on internal layers. This difference must be included in the length matching calculations. Ideally, all DDR4 signals should be routed on internal layers. Ground stitching vias are needed close to signal vias whenever the reference plane for a trace changes.

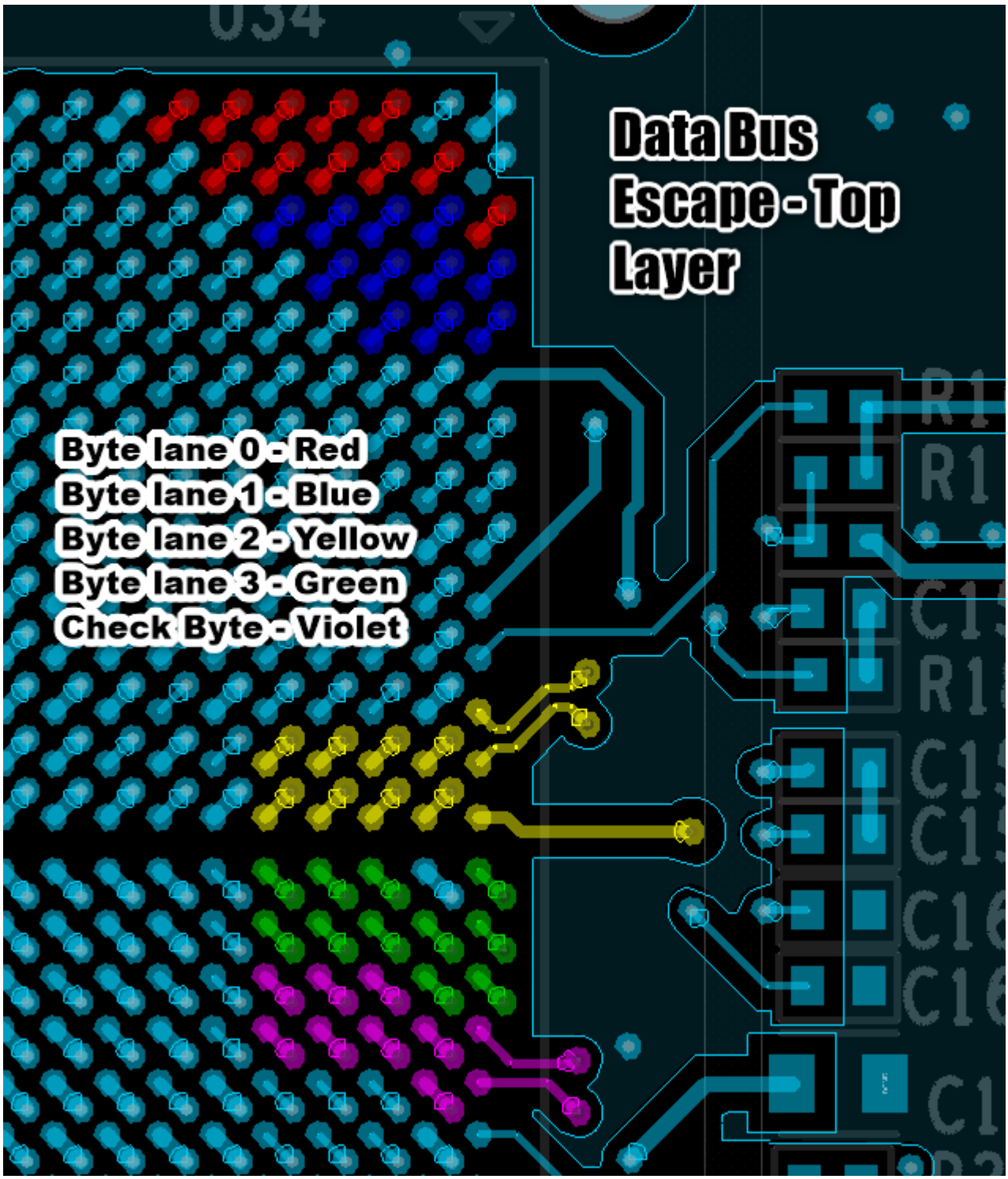



**Figure 4. DDR4 Data Bytes Layer 1**

Figure 5 shows the routing under the BGA on layer 10. Ideally, the odd lanes should be routed on the same layer. The area between the vias for the even lanes can be used to escape signals that are in rows closer to the center. The EVM used layer 10 to escape byte lane 1 and byte lane 3.

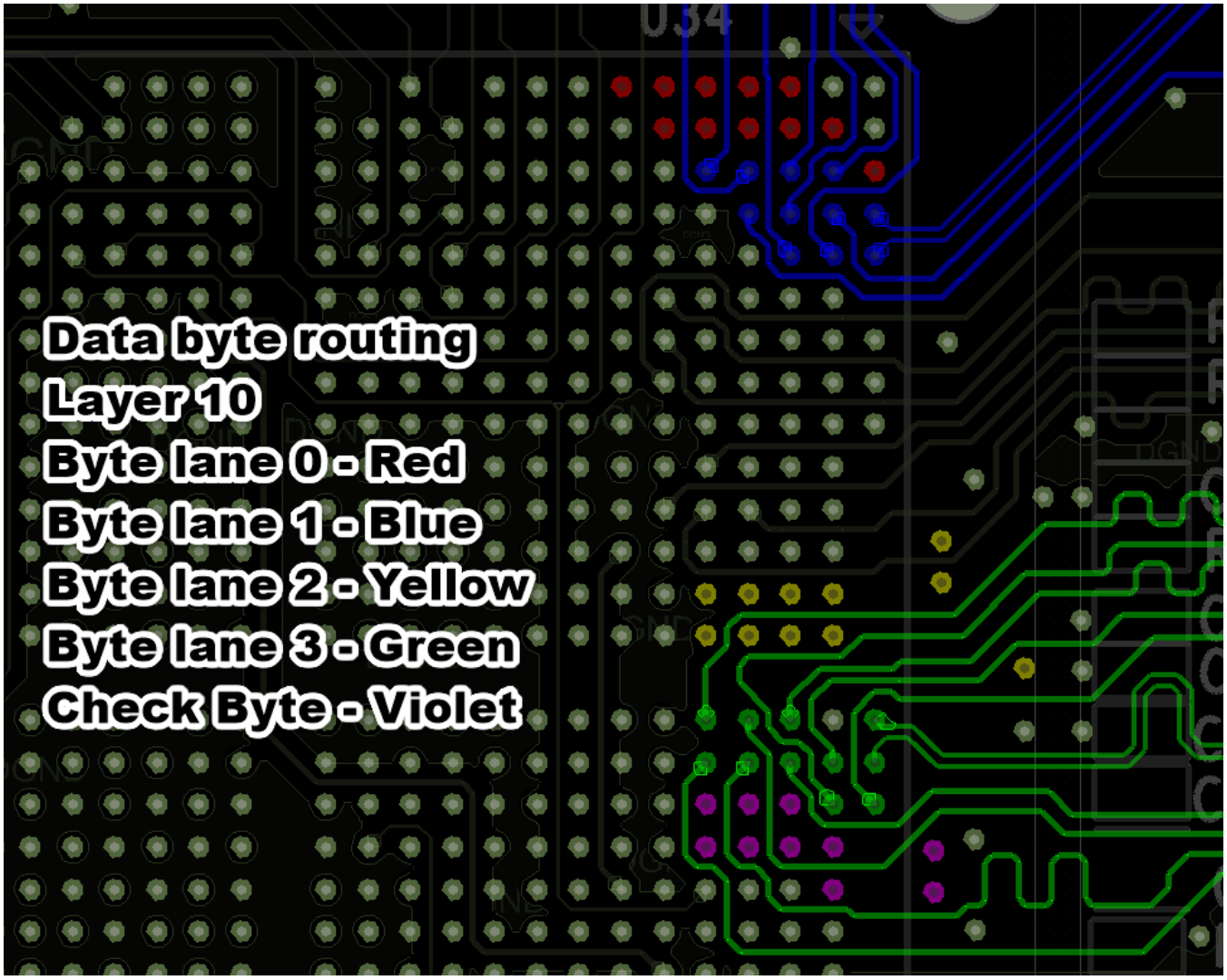



**Figure 5. DDR4 Data Bytes Layer 10**

Figure 6 shows the routing under the BGA on layer 12. Ideally, the even lanes should be routed on the same layer. The area between the vias for the odd lanes can be used to escape signals that are in rows closer to the center. The EVM used layer 12 to escape byte lane 2 and byte lane 0, as well as the check byte signals.

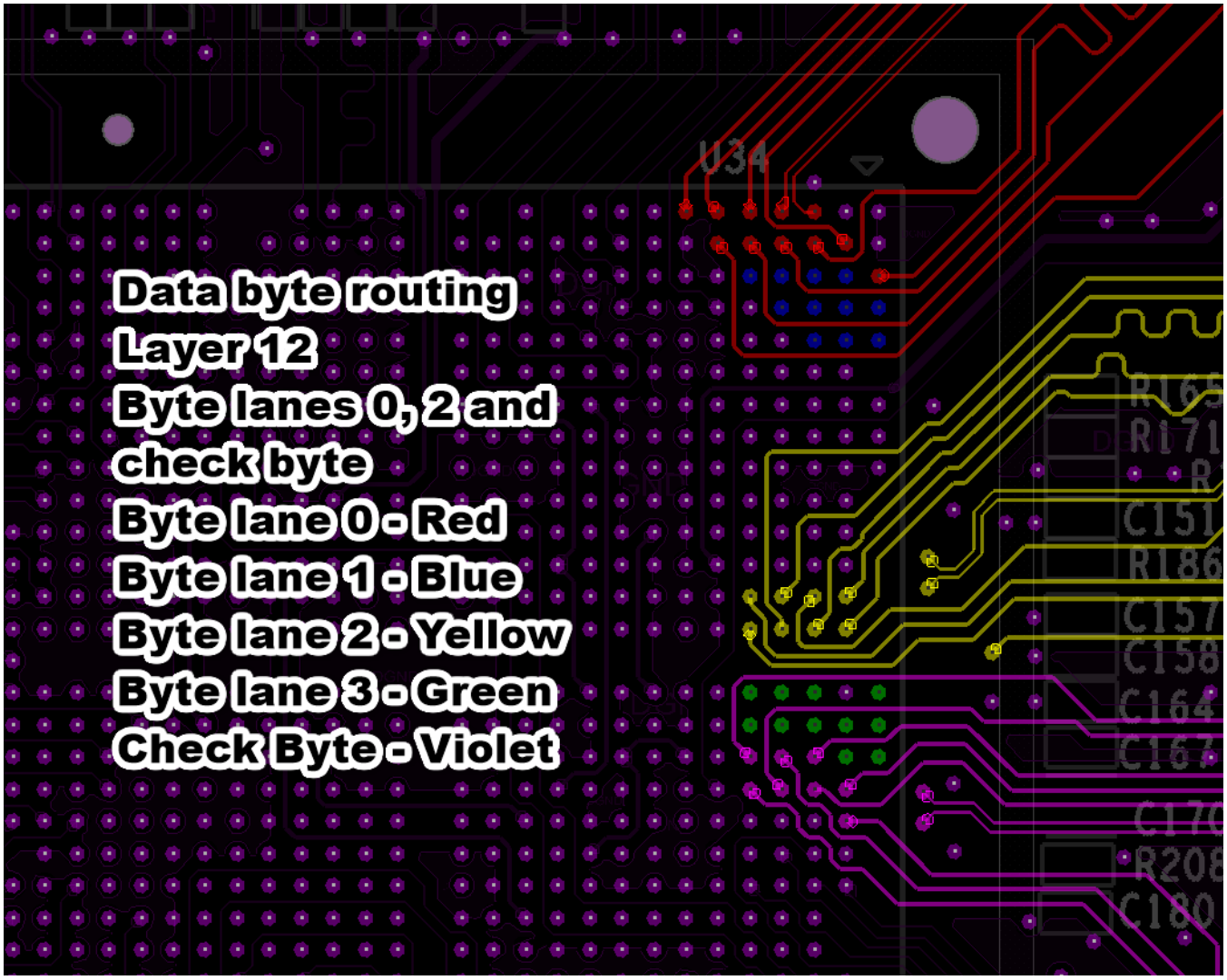



**Figure 6. DDR4 Data Bytes Layer 12**

### 6.2 Address, Command, Control, and Clock Group Routes

The address, command, and clock signals are routed in flyby starting with the check byte memory and moving up to byte lane 0. The VTT termination resistors are placed at the end of the trace past the byte 0 memory device, as shown in Figure 7.

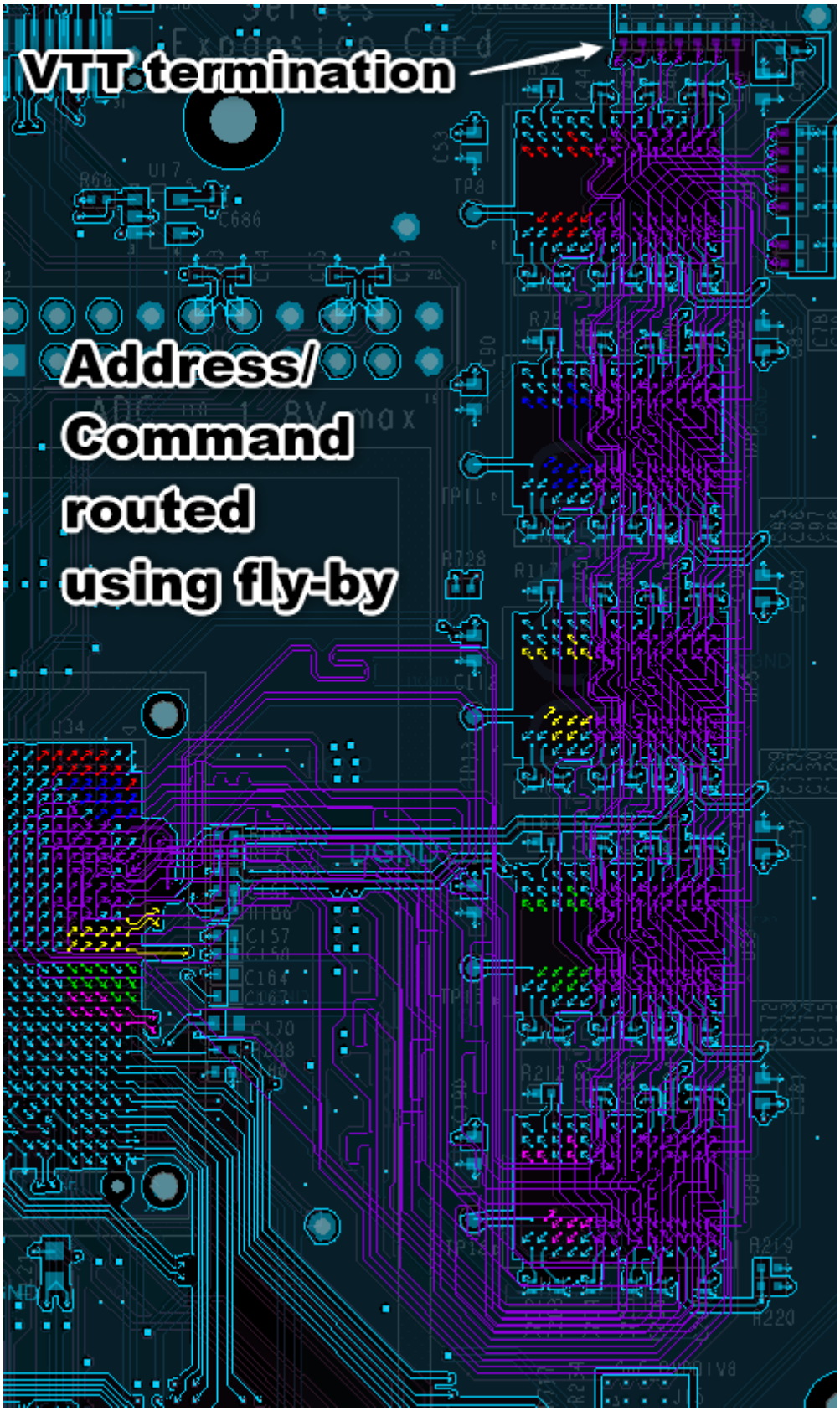
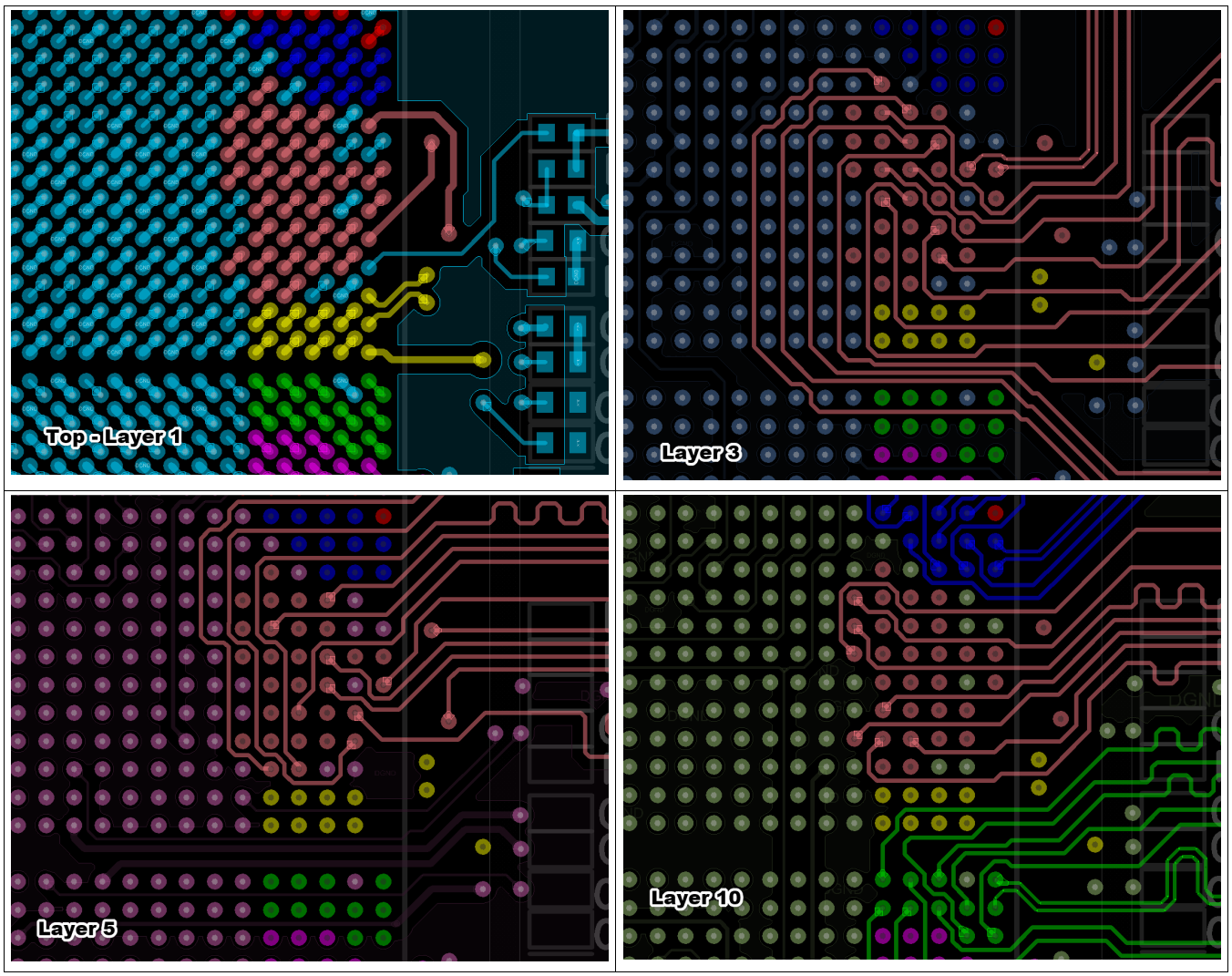



**Figure 7. DDR4 Address and Command Signals**

The layers 3, 5, and 10 are used to escape and route the address and command signals. The signals must be length matched to ensure that the signals arrive at each memory at the same time. Length matching must be from the SoC to each memory individually including the stub to the memory pad. Simply matching the length of each trace from beginning to end is not sufficient. The speed difference between the signals routed on the top layer and the internal layers must also be taken into account.

The escapes of the address and command signals for these three layers are shown in Figure 8. Address signals are routed directly from the SoC to the via next to the associated pad for the first memory device. This requires that the address signals escape in the correct order. Some of the signals were routed from top of the address area to the bottom through the inside to achieve this ordering. Using a steering via at the beginning of the flyby simplifies the escape, but complicates the length matching calculation. Ground stitching vias are needed close to signal vias whenever the reference plane for a trace changes. All DDR signals in the AM654x GP EVM are referenced to ground. If the DDR_VDDS plane is used as a reference, bypass capacitors between DDR_VDDS and ground must be placed near every signal via. This is required even if a trace has a ground plane on one side and DDR_VDDS plane on the other.

**Figure 8. DDR4 Address and Command Escapes**



## 6.3 Complete Power Decoupling

The middle priority interfaces and the power distribution planes and pours are routed after the SERDES and DDR interfaces. TI strongly recommends completing all SERDES and DDR routing before continuing with other interfaces. The power distribution planes and pours and all of the decoupling must be placed before PCB simulations are executed for the SERDES and DDR routes. TI strongly recommends that simulation be performed on the higher speed source-synchronous interfaces, such as RGMII, OSPI, and QSPI. Routing for these interfaces should be completed at this time.

## 6.4 Route Lowest Priority Interfaces

When the length matching and simulations have been completed for the highest priority interfaces, and the Power Distribution Network (PDN) analysis has been completed, then the layout can continue with the medium and lower priority interfaces. For additional information, refer to the *Sitara™ Processor Power Distribution Networks: Implementation and Analysis*.

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