DRA77xP/DRA76xP-ACD CPU EVM Board

This user's guide is intended for software and hardware engineers developing applications for the Jacinto 6 high performance, multimedia application processor based on enhanced OMAP™ architecture implemented with 28-nm technology. It describes the evaluation module (EVM) CPU board's hardware, firmware and software functions supplied by Texas Instruments Inc.

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1 Introduction

The DRA77xP/DRA76xP-ACD is an evaluation platform designed To allow scalability and re-use across DRA77xP and DRA76xP “Jacinto” Infotainment System-on-Chips (SoCs), it is based on “Jacinto 6 Plus” DRA77xP SoC that incorporates a heterogeneous, scalable architecture that includes a mix of two ARM Cortex-A15 Microprocessor Units, two Arm® Cortex®-M4 Processing Subsystems, each with two ARM Cortex-Microprocessors, two Digital Signal Processors (DSPC66x), a Vision AccelerationPac including two Embedded Vision Engines (EVEs), 2D and 3D-GraphicProcessing Units including Imagination Technologies POWERVR™ SGX544 dual-core and High-Definition Image and Video Accelerator. Also it integrates a host of peripherals including multi-camera interfaces(both parallel and serial) for LVDS-based surround view systems, CSI2 interface, displays, Controller Area Network (CAN) and GigB Ethernet AVB.

The main CPU board integrates these key peripherals such as Ethernet or HDMI, while the infotainment application daughter board (JAMR3) and LCD/TS daughter board will complement the CPU board to deliver complete system to jump start your evaluation and application development.

2 Overview

An EVM system is comprised of a CPU board with one or more application boards. The CPU board (shown in Figure 1) can be used standalone for software debug and development. Each EVM system has been designed to enable customers to evaluate the Processor performance and flexibility in the following targeted markets:

- Automotive Infotainment applications
- Automotive Vision applications
- Emerging End Equipment applications

The CPU board contains the (Jacinto 6 Plus/TDA2Px) applications processor, a companion Power Management ICs (TPS65917 + LP87565), Audio Codec (TLV320AIC3106), DDR3 DRAM, four different Flash memories (QSPI, enhanced MultiMedia Card (eMMC), NAND and NOR), a multitude of interface ports and expansion connectors. The board provides additional support components that provide software debugging, signal routing and configuration controls that would not be needed in a final product.

Different version CPU boards will be built to support the development processes that include:

- Socketed processor used for wakeup, early software development, quick and easy chip revision evaluation
- Soldered-down processor used for high performance Use Cases and evaluations

All other components on-board are soldered-down.

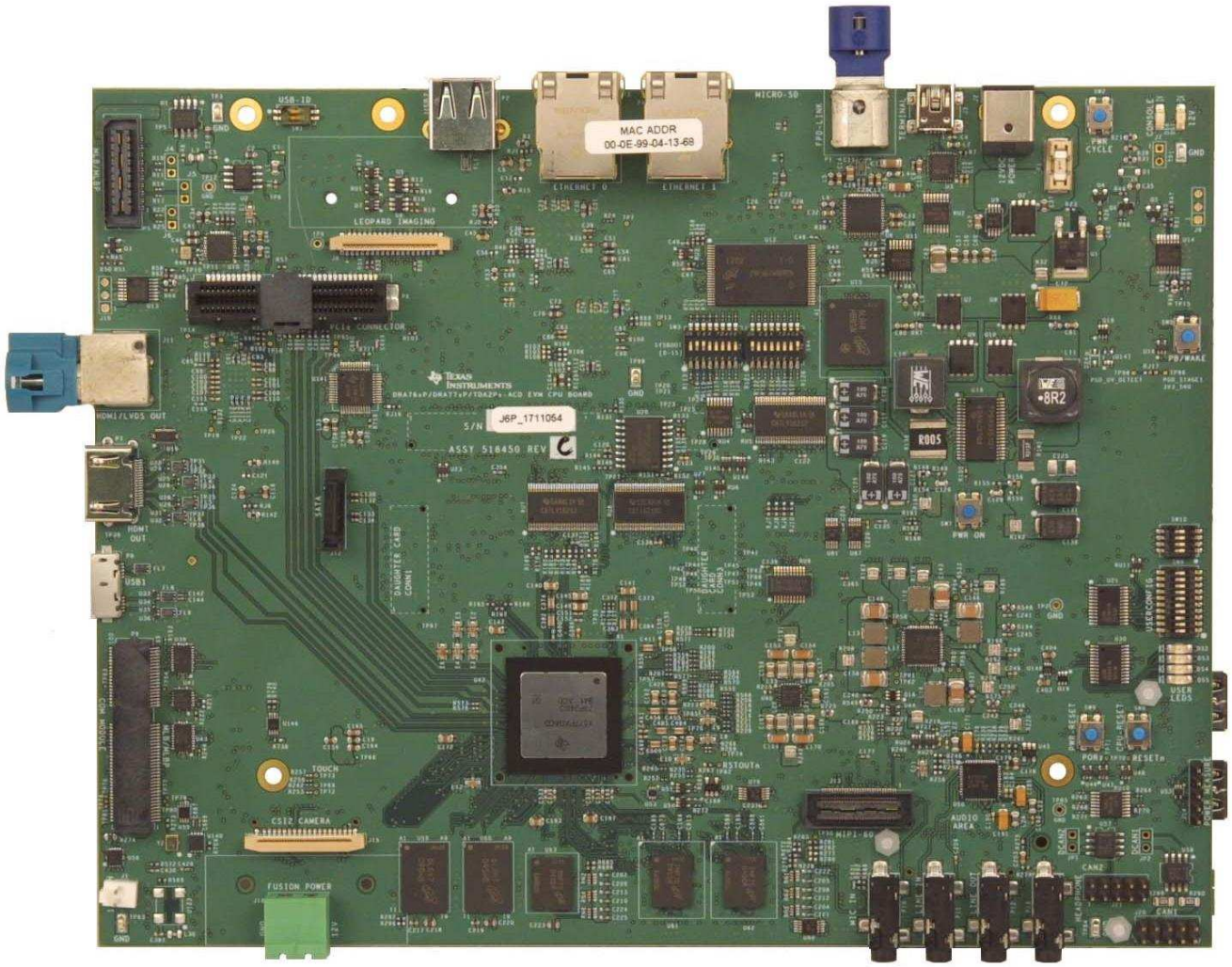


Figure 1. CPU Board

2.1 EVM System Configurations

Table 1. SoC EVMs/Kits

Systems	Description	Model Number
DRA76xP/DRA77xP/TDA2Px-ACD CPU Board ES1.0 GP Rev A (CPU Bd)	GP CPU board, and limited accessory cables	EVM577PBG-01-00-00
DRA76xP/DRA77xP/TDA2Px-ACD CPU Board ES1.0 GP Socketed Rev A (CPU Bd)	Socketed CPU board, and limited accessory cables	EVM577PBG-01-00-S0
DRA76xP/DRA77xP/TDA2Px-ACD CPU Board ES1.0 HS Rev A (CPU Bd)	HS CPU board and limited accessory cables	EVM577PBH-01-00-00
DRA76xP/DRA77xP/TDA2Px-ACD ES1.0 GP EVM Infotainment Kit Rev A	CPU Bd + JAMR3 Apps Bd + 1080P display/multi-touch touchscreen	EVM577PG-01-20-00
DRA76xP/DRA77xP/TDA2Px-ACD ES1.0 GP EVM Kit Rev A	CPU Bd + 1080P display/multi-touch touchscreen	EVM577PG-01-00-00
TDA2Px-ACD ES1.0 GP EVM Vision Kit Rev A	CPU Bd + Vision Apps Board	EVM577PG-01-40-00
TDA2Px-ACD ES1.0 GP EVM Fusion Kit Rev A	CPU Bd +Fusion Apps Board	EVM577PG-01-60-00

Table 2. EVM Accessories

Accessories	Description	Model Number
Fusion Application Bd	Dual ‘960 FPD-link to CSI2 Hus for camera and radar support	EVM577PFUSION-V1-0
Camera Kits for Fusion Board	OV2775 sensor with DS90UB953 serializer module	EVMFUSIONCAM-V1-0
1080P Display/Multi-Touch Touchscreen	13.1” 1080P display with USB interface for touchscreen	EVM577PLCDTS-V1-0
Display with ‘924 FPD-Link interafce	1280X800 display/multi-touch touchscreen w/'924 FPD-link interface	EVM5777LCDTS-V4-0
Vision Application Bd	Support for multiple camera inputs for surround view, stereo vision, and proprietary camera board interfaces	EVM5777VISION-V2-0
JAMR3 Tuner Application Bd	Head-unit DIN form-factor application board with radio tuners, multiple audio I/O’s, and video input extendability	EVM5777JAMR3-V1-0
RGB-to-HDMI Application Bd	RGB to HDMI interface with TFP410(no Audio) and USB for touchscreen	EVM577PHDMI-V1-0

Table 3. EVM Kit Truth Table

EVM/Kit Name	CPU Bd	RGB-to-HDMI	1080P Display	Fusion App Bd	Camera Kit for Fusion	JAMR3 App Bd	Vision App Bd
App Bd	Camera Kit for Fusion	JAMR3 App Board	Vision App Board				
DRA76xP/DRA77xP /TDA2Px-ACD CPU Board ES1.0 GP Rev A (CPU Bd)	X	X					
DRA76xP/DRA77xP /TDA2Px-ACD CPU Board ES1.0 GP Socketed Rev A (CPU Bd)	X	X					
DRA76xP/DRA77xP /TDA2Px-ACD CPU Board ES1.0 HS Rev A (CPU Bd)	X	X					
DRA76xP/DRA77xP /TDA2Px-ACD ES1.0 GP EVM Infotainment Kit Rev A	X	X	X			X	
DRA76xP/DRA77xP /TDA2Px-ACD ES1.0 GP EVM Kit Rev A	X	X	X				X

Table 3. EVM Kit Truth Table (continued)

EVM/Kit Name	CPU Bd	RGB-to-HDMI	1080P Display	Fusion App Bd	Camera Kit for Fusion	JAMR3 App Bd	Vision App Bd
TDA2Px-ACD ES1.0 GP EVM Vision Kit Rev A	X	X					
TDA2Px-ACD ES1.0 GP EVM Fusion Kit Rev A	X	X		X			

2.2 CPU Board Feature List

- Processor:
  - DRA77xP/DRA76xP/TDA2Px (Superset SoC) (23 mm x 23 mm package, 0.8 mm pitch)
  - Support for corresponding socket
- Power supply:
  - 12 V DC input
  - Optimized power management solution
  - Compliant with SoC power sequencing requirements
  - Integrated power measurement
- PCB:
  - Dimension (W x D) 220mm x 170mm
  - 100% PTH technology
- Memory:
  - DRAM (DDR3L-1333): 4 Gbyte (2 GByte for each EMIF) (EMIF1 optionally supports ECC)
  - Quad Serial Peripheral Interface (SPI) Flash: 256 M-bit
  - eMMC Flash: 8G-bit (v4.51 compliant)
  - NAND Flash: 4G-bit
  - NOR Flash: 512 M-bit
  - Serial EEPROM, 32K-bit
  - MicroSD Card Cage
- Boot mode selection DIP switch
- Digital Temperature Sensor (TMP102)
- JTAG/Emulator:
  - 60 pin MIPI Connector/Trace Connector
  - Adapter for 20 pin-CTI adapter: 10 x 2, 1.27mm pitch
- Supported Interfaces and Peripherals:
  - CAN Interface, two 2-wire PHY (either can also support CAN-FD)
  - 2x USB Host receptacles (1x USB3.0 (micro-USB), 1x USB2.0 (Type-A))
  - Audio Codec (AIC3106) with Headphone OUT, Line OUT, Line IN, Microphone IN
  - 3x Video outputs (HDMI, RGB/LCD, FPD-Link III)
  - Camera Sensor(s) supported via Leopard Imaging Module Interfaces (Parallel and MIPI)
  - PCI Express (PCIe), 2x Channel
  - SATA
  - MLB and MLBP on Mictor connector
  - Universal Asynchronous Receiver/Transmitter (UART) terminal via USB FTDI converter (mini-A/B USB)
  - COM8Q module interface for Bluetooth and WLAN support

  - 2x RJ45 Gbit Ethernet (DP83867)
  - I2C General-Purpose Input/Output (GPIO) Expander
- Expansion connectors to support application specific add-on boards

2.3 CPU Board Component Identification

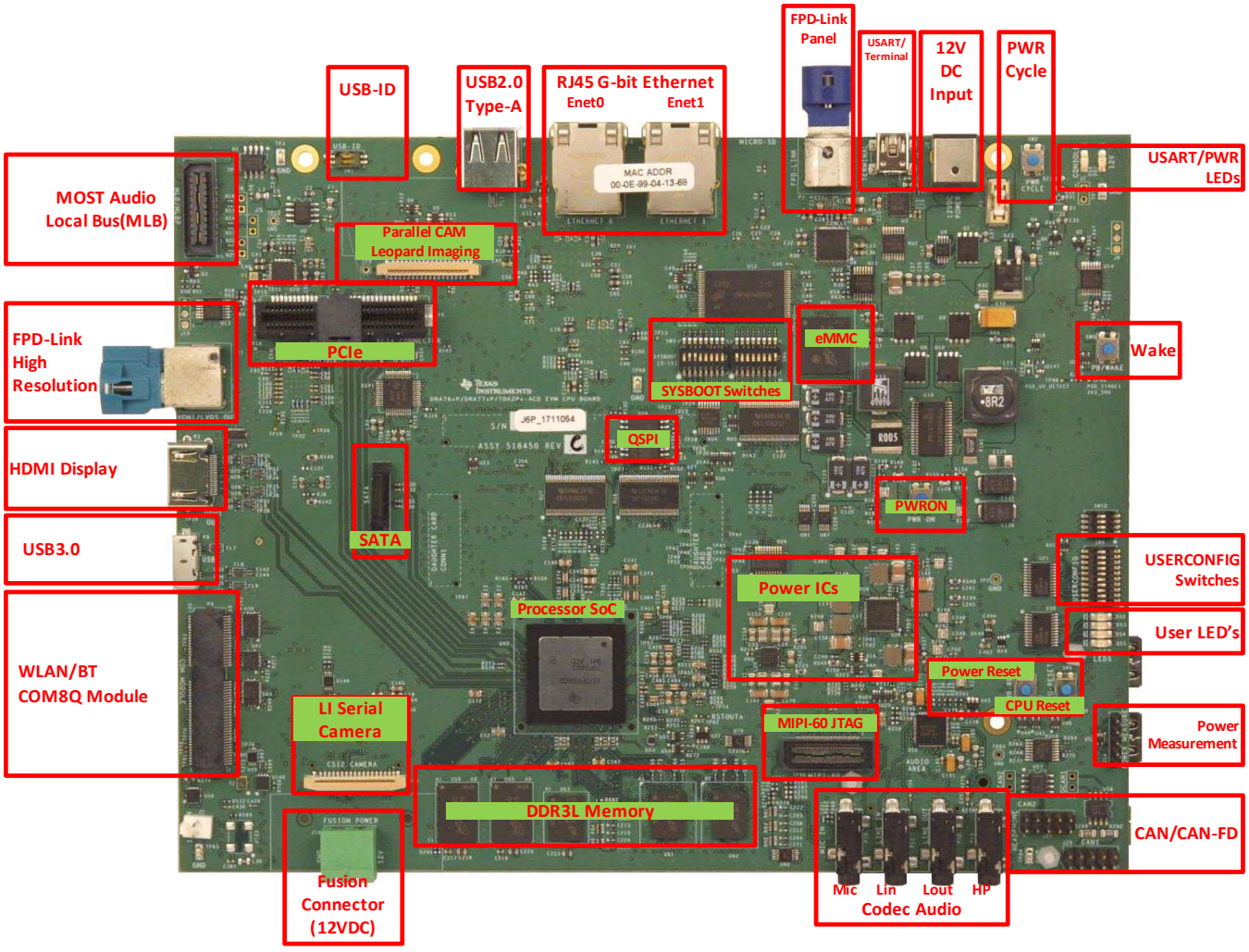


Figure 2. CPU Board - Front

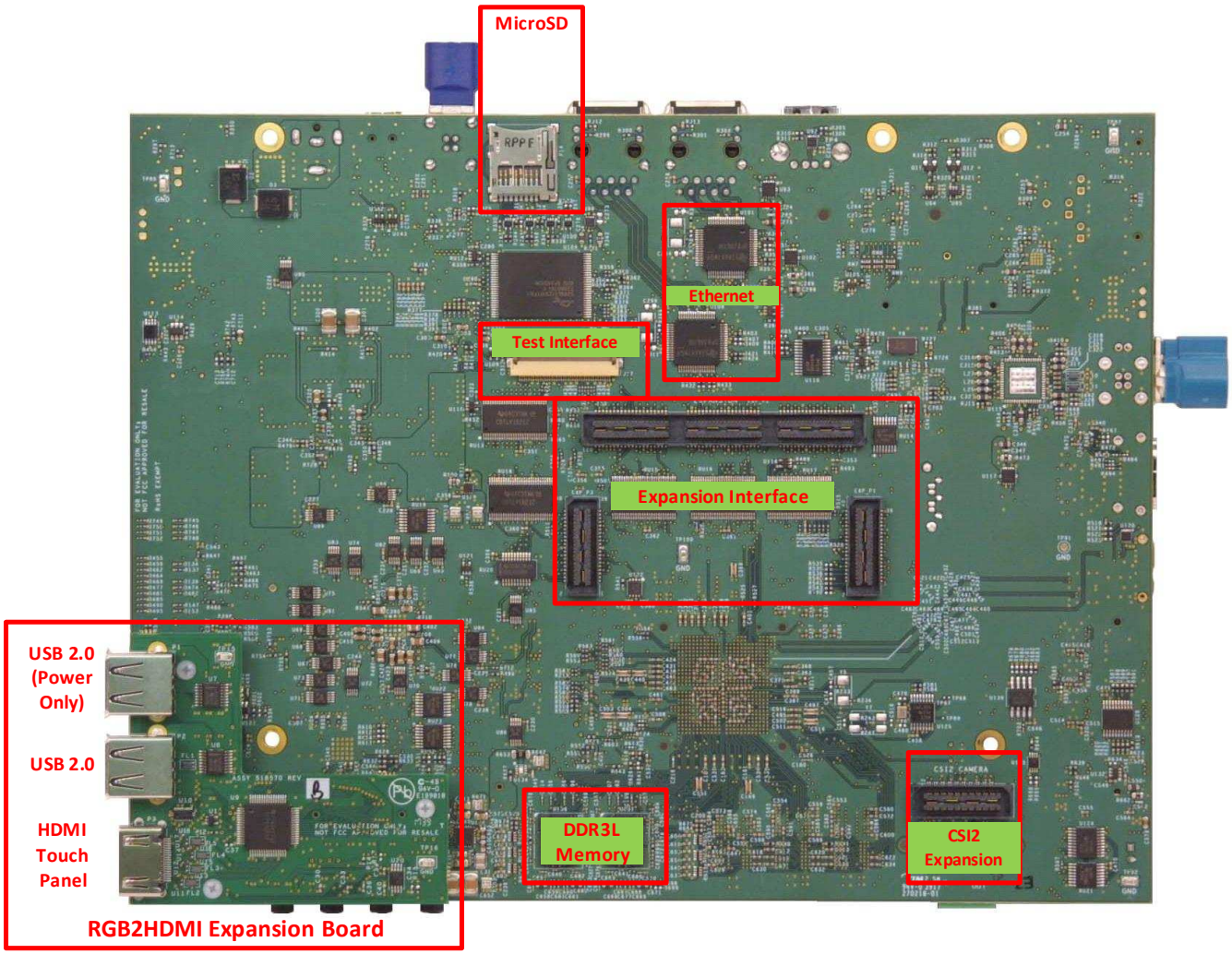


Figure 3. CPU Board - Back

3 Hardware

3.1 Hardware Architecture

Figure 4 shows the CPU board's functional block diagram.

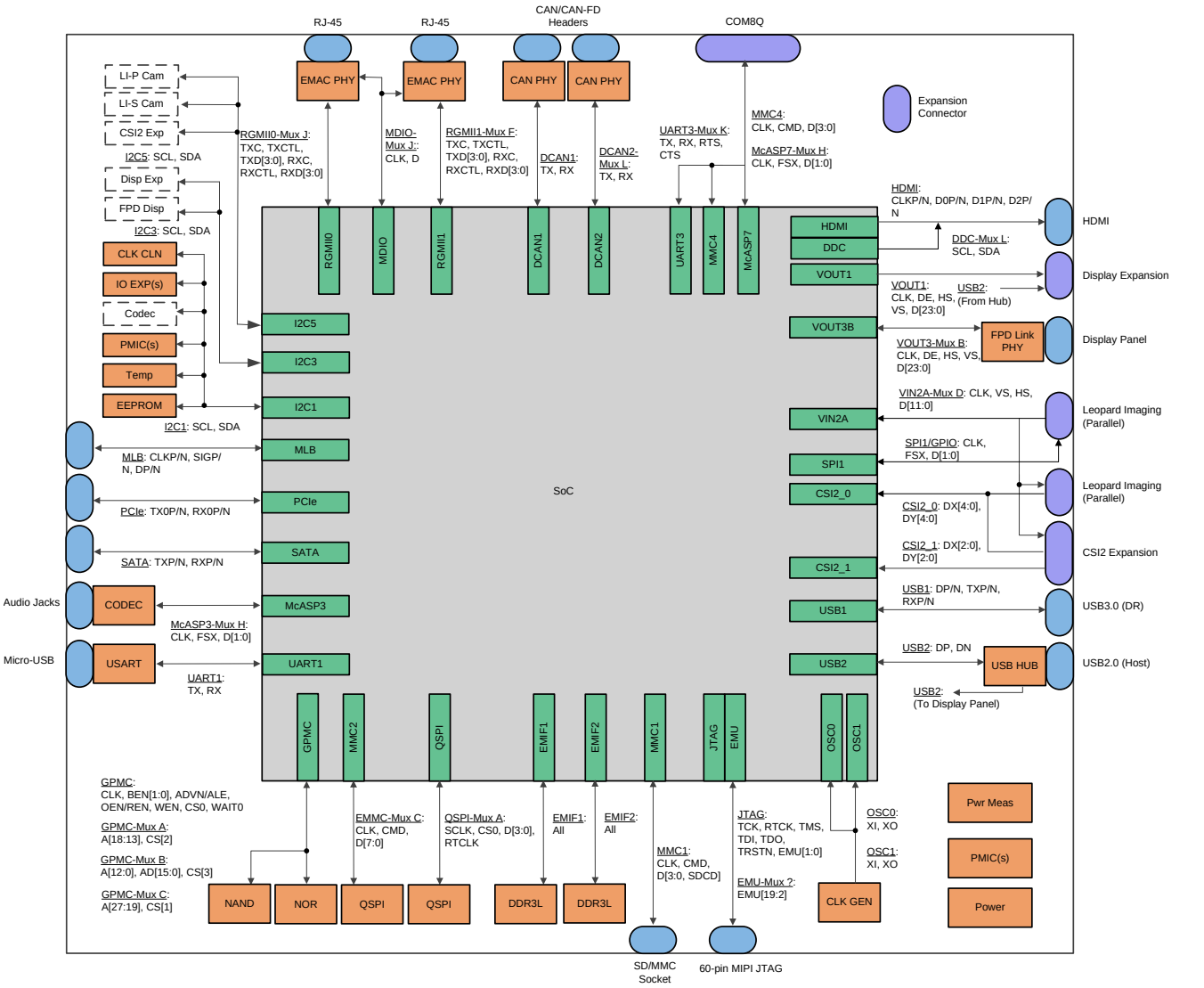


Figure 4. CPU Board Block Diagram

3.2 Power Architecture

Figure 5 shows the EVM's power distribution system. The power management solution is created from four total devices. A step-down 12 V to 5 V / 3.3 V converter provides the primary 5v0/3v3 power rails for the entire system. The TPS65917 and LP87565 devices are optimized for the SoC maximum power and sequence requirements. A sink/source regulator provides the DDR power and termination rails.

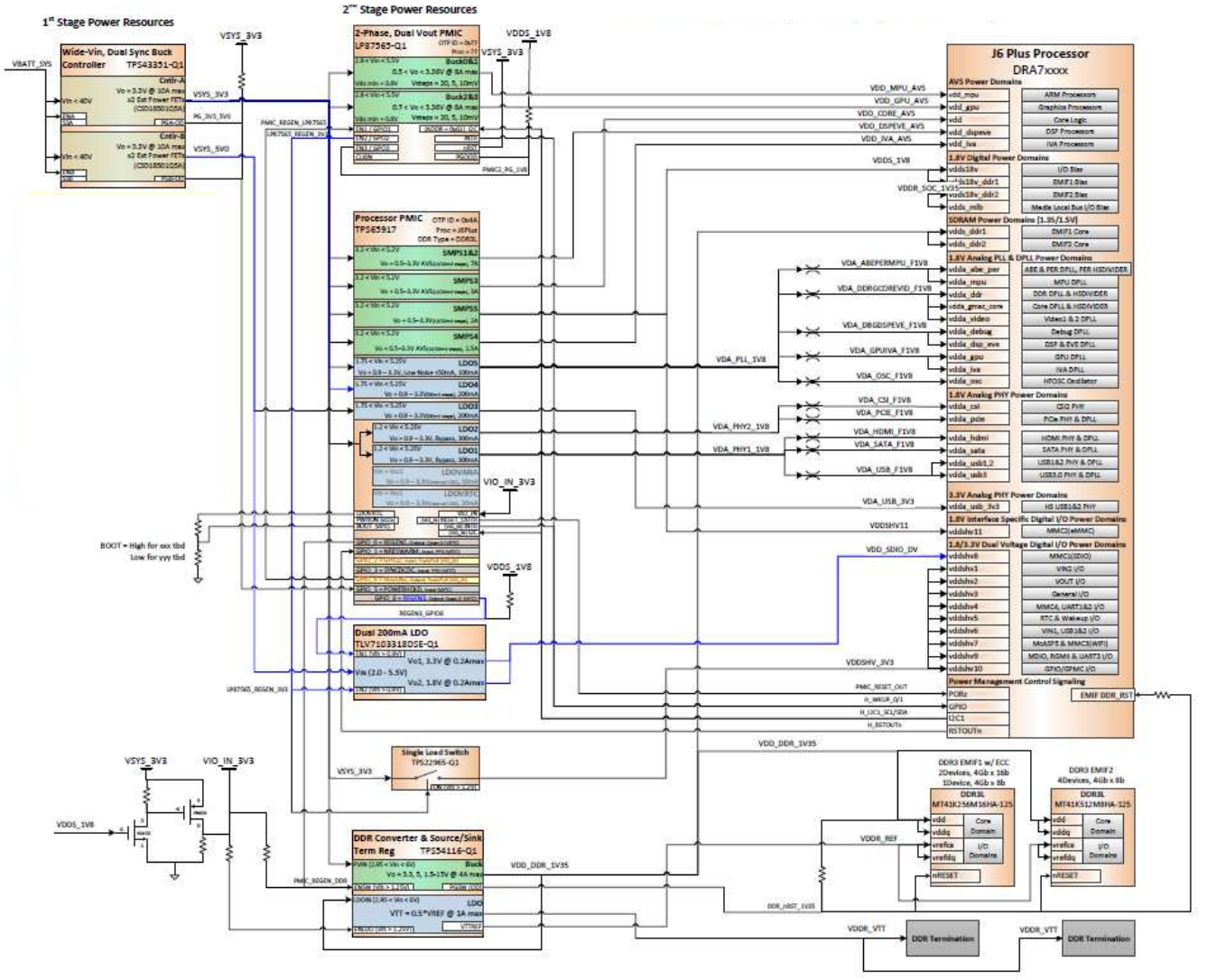


Figure 5. Power Distribution Block Diagram

An external power supply is required to power the EVM, but is not included as part of the EVM kit. The external power supply requirements are:

Power Jack: 2.5 mm ID, 5.5 mm OD
Nom Voltage: 12 VDC
Max Current: 5000 mA
Efficiency Level V

External Power Supply Regulatory Compliance Certifications: Recommended selection and use of an external power supply that meets TI's required minimum electrical ratings in addition to complying with applicable regional product regulatory/safety certification requirements, (for example, UL, CSA, VDE, CCC, PSE, and so forth).

Wall power supply is not included. Table 4 lists the recommended and tested power supplies that can be used with the EVM.

Table 4. Compatible Wall Supplies (12 V, 5A, 65W)

Digi-Key Part Number	Manufacturer Part Number	Manufacturer	Output Connector	Notes
102-3417-ND	SDI65-12-U-P5	CUI Inc.	Barrel Plug, 2.1mm I.D. x 5.5mm O.D. x 9.5mm	Required adapter, provided in the EVM kit
62-1221-ND	KTPS65-1250DT-3P-VI-C-P1	Volgen America/Kaga Electronics USA	Barrel Plug, 2.1mm I.D. x 5.5mm O.D. x 9.5mm	Required adapter, provided in the EVM kit
102-3419-ND	SDI65-12-UD-P5	CUI Inc.	Barrel Plug, 2.1mm I.D. x 5.5mm O.D. x 9.5mm	Required adapter, provided in the EVM kit
SDI65-12-U-P6-ND	SDI65-12-U-P6	CUI Inc.	Barrel Plug, 2.5mm I.D. x 5.5mm O.D. x 9.5mm	
SDI65-12-UD-P6-ND	SDI65-12-UD-P6	CUI Inc.	Barrel Plug, 2.5mm I.D. x 5.5mm O.D. x 9.5mm	

3.3 Reset Structure

The reset structure is shown in Figure 6. The power-on reset timing is controlled primarily from the system power ICs (TPS65917/LP87565). There are two push buttons for user-controlled resets. The power on reset pushbutton (SW9) provides a complete/cold reset to the SoC. The warm reset pushbutton (SW8) provides a warm reset to the SoC. The warm reset can also be sourced from the MIPI-60 JTAG/Trace connector.

The SoC itself provides a reset for all its peripherals (RSTOUT).

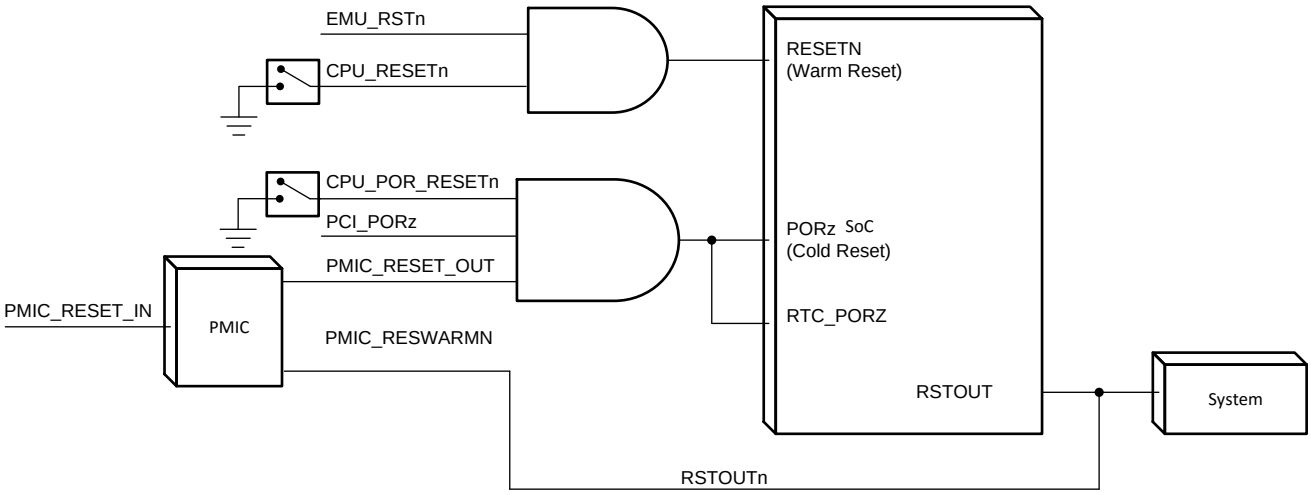


Figure 6. Reset Structure

Table 5 summarizes the reset signals.

Table 5. Reset Signals Structure

Reset Type	Reset Signal Sources	Comments
Power-On Reset (as whole system reset)	CPU_POR_RESETn	PORn push button reset
	PCI_PORz	PCIe inbound reset
	PMIC_RESET_OUT	Power on reset from power ICs
Warm Reset	CPU_RESETn	Warm push button reset
	EMU_RSTn	Reset from Emulator
PMIC Power On Reset	PMIC_RESET_IN	PMIC reset input
Processor Reset Out	RSTOUTn	Reset Output from processor to system, PMIC (warm reset input)

3.4 Clocks

The SoC supports up to two primary clock inputs. The device clock (OSC0) is sourced with 20 MHz clock. The auxiliary clock (OSC1) is sourced with a 22.5792 MHz clock. Both clocks are sourced from a clock synthesizer (CDC925).

In addition to the SoC clock inputs, the EVM includes other clock sources. 25 MHz clocks are provided to Ethernet PHY(s) and 100 MHz clock is sourced for miniPCIe. Both the SoC and Ethernet clocks are sourced from a clock synthesizer (CDC925).

3.5 Memory

3.5.1 SDRAM Memory

The EVM includes 4GBytes of DDR3L memory and can operate at clock speeds up to 667 MHz (DDR3-1333). The SoC supports two separate memory interfaces, EMIF1 and EMIF2, and the memory is distributed evenly between the banks (2 Gbyte each). ECC is supported on EMIF1 only.

While supporting the same amount of memory, the two EMIF interfaces are implemented differently. EMIF1 is configured with two memory devices of 8Gbit each (x16b devices) plus ECC. EMIF2 is configured with four devices of 4 Gbit each (x8b devices). This configuration is done to provide different reference PCB layout/routing for the different examples.

- DDR3L device used: Micron MT41K512M8RH-125-AA:E (4x8 bit @ 4 Gbit/ea) (or equivalent).
- DDR3L device used: Micron MT41K512M16HA-125:A (2x16 bit @ 8 Gbit/each) (or equivalent).
- EEC device used: Micron MT41K512M8RH-125-AA:E (1x8 bit @ 4 Gbit) (or equivalent).

The DDR3L power is generated from the SoC power solution, specifically the TPS54116. Its output voltage is set to 1.35 V. It uses ‘fly-by’ topology with VTT termination. VTT supply is generated by the same TPS54116 device, which includes a sink/source termination regulator.

3.5.2 QSPI Flash Memory

As a primary non-volatile boot device, the EVM includes 256 Mbit of Quad-SPI Flash memory. The device is support on chip select zero of the QSPI interface. The interface can be configured to support either serial mode (1x) or quad mode (4x).

- QSPI device used: Spansion S25FL256S

Booting from the QSPI Flash memory is supported on the EVM. No EVM configuration is required as the QSPI flash is enabled by default. Ensure the correct SoC boot mode is set using the SYS_BOOT switches (SW3, SW4).

3.5.3 EMMC Flash Memory

As a primary non-volatile storage device, the EVM includes 8GBytes of eMMC flash memory. The memory device is EMMC v4.51 compliant, and connects to MMC2 port of the SoC. The design can supports rates up to HS-200.

- EMMC device used: Micron MTFC8GLWDM-3M AIT Z

Booting from the EMMC Flash memory is supported on the EVM. The on-board mux must be to enable EMMC by setting SW8.p3 to ON. Ensure the correct SoC boot mode is set using the SYS_BOOT switches (SW3, SW4).

3.5.4 MicroSD Card Cage

For non-volatile storage expansion, the EVM includes a microSD card cage. The cage is connected to MMC1 port of the SoC. To support higher speed cards that operate at lower voltages, the IO supplies is changed from 3v3 to 1v8 by setting TPS917 REGEN3 register low. As SD card can be a boot peripheral, the power is defaulted to ON. No EVM configuration is required for booting as the SD card is enabled by default. Ensure the correct SoC boot mode is set using the SYS_BOOT switches (SW3, SW4). The SD card power can be disabled using GPIO4_21 and setting it low. For SoC-specific information regarding supported card types, densities, and speeds, see the *DRA75xP, DRA74xP, DRA77xP, DRA76xP SoC for Automotive Infotainment Silicon Revision 1.0* (SPRUI98).

3.5.5 GPMC NOR Flash Memory

A 512M-bit NOR Flash memory (x16) is supported as a non-volatile memory option on the EVM. It is supported on chip select CS0, and therefore can also be uses as a boot device. Booting from the NOR flash memory is supported on the EVM. The on-board mux must be to enable the memory by setting SW6.p2 to ON. Ensure the correct SoC boot mode is set using the SYS_BOOT switches (SW3, SW4).

- NOR device used: Spansion S29GL512S10TFI010

3.5.6 GPMC NAND Flash Memory

A 4G-bit NAND Flash memory (x16) is supported as a non-volatile memory option on the EVM. It is supported on chip select CS0, and therefore can also be uses as a boot device. Booting from the NAND flash memory is supported on the EVM. The on-board mux must be to enable the memory by setting SW6.p1 to ON. Ensure the correct SoC boot mode is set using the SYS_BOOT switches (SW3, SW4).

- NAND device used: Micron MT29F4G16BADWP:D

3.6 Boot Modes

The SoC supports a variety of different boot modes, which is determined by the 16-bit “system boot” setting present on the shared specific I/O balls during power-on sequence. For more details, see *DRA75xP, DRA74xP, DRA77xP, DRA76xP SoC for Automotive Infotainment Silicon Revision 1.0* (SPRUI98). Boot mode selection is accomplished on the EVM by the setting of DIP switches SW3 and SW4 prior to cycling power.

Note that these SoC resources can be “redeployed” to support alternate interfaces after boot-up by way of both SoC pin EVM mux settings.

Table 6. SoC Boot Mode Switch Settings

SoC Interface (Internal System Boot Input)	CPU Board Net	DIP Switch Ref Destination Position Number Connections	Factory Settings
GPMC_AD0 (sysboot0)	GPMC_D00	SW3.P1	ON
GPMC_AD1 (sysboot1)	GPMC_D01	SW3.P2	OFF
GPMC_AD2 (sysboot2)	GPMC_D02	SW3.P3	ON
GPMC_AD3 (sysboot3)	GPMC_D03	SW3.P4	OFF
GPMC_AD4 (sysboot4)	GPMC_D04	SW3.P5	ON
GPMC_AD5 (sysboot5)	GPMC_D05	SW3.P6	OFF
GPMC_AD6 (sysboot6)	GPMC_D06	SW3.P7	OFF
GPMC_AD7 (sysboot7)	GPMC_D07	SW3.P8	OFF
GPMC_AD8 (sysboot8)	GPMC_D08	SW4.P1	ON
GPMC_AD9 (sysboot9)	GPMC_D09	SW4.P2	OFF
GPMC_AD10 (sysboot10)	GPMC_D10	SW4.P3	OFF
GPMC_AD11 (sysboot11)	GPMC_D11	SW4.P4	OFF
GPMC_AD12 (sysboot12)	GPMC_D12	SW4.P5	OFF
GPMC_AD13 (sysboot13)	GPMC_D13	SW4.P6	OFF
GPMC_AD14 (sysboot14)	GPMC_D14	SW4.P7	OFF
GPMC_AD15 (sysboot15)	GPMC_D15	SW4.P8	ON

In addition to SoC boot settings, EVM resources must also be set for the desired boot interface. Table 7 shows the boot interfaces that require selection. DIP switch SW6 is used to configure the various boot memories.

Table 7. Board Controls for Booting Options

Signals	Description	DIP Switch	Factory Settings
NAND_BOOTn	ON = Enable GPMC_nCS0 for NAND flash boot	SW6.1	OFF
NOR_BOOTn	ON = Enable GPMC_nCS0 for NOR flash boot	SW6.2	OFF
MMC2_BOOT	ON = Enable MMC2 Interface for eMMC flash boot	SW6.3	OFF
SEL_VCC_CSI2_IO	OFF = Selects 3.3 V IO for CSI2 imager interfaces (Leopard image and Samtec) ON = Selects 1.8 V IO for CSI2 Interfaces	SW6.4	ON
UART_SEL1_3	OFF = Selects UART3 for terminal USART ON = Selects UART1 for terminal USART	SW6.5	ON
MCASP1_ENn	ON = Enable signal paths to COMx module	SW6.6	OFF
SW_VPP_EN	ON = Enable VPP supply to SOC (also requires IO Exp bit to be set)	SW6.5	OFF
PCI_RESET_SEL	OFF = PCIe device may reset SoC ON = SoC may reset the PCIe device	SW6.8	OFF
GPMC_WPN	ON = Enable write protection of NAND Flash	SW6.9	OFF
I2C_EEPROM_WP	High = Enable write protection of Board identification EEPROM	SW6.10	OFF

1. Routing control for GPMC_nCS0 is “shared” between NOR & NAND Flash memories. Ensure that only one DIP switch, SW8.P1 or SW8.P2, is ever set to “ON” state at any one time so that GMPC_nCS0 is only connected to one memory. Failure to adhere to this requirement will cause NOR & NAND memory data bus contention.
2. UART3 peripheral boot and terminal access requires a on-board resistor modification.

3.7 JTAG/Emulator and Trace

The JTAG emulation interface is supported through the MIPI 60 pin interfaces. The EVM kit includes an adapter(s) for supporting other JTAG interfaces, including TI's 20 pin cJTAG interface. Reset (warm reset) via the emulator is supported.

TRACE/Debug is also support through the MIPI-60 connector. The EVM supports up to 20 trace bits. At the SoC and EVM level, the trace pins are muxed with VOUT1 function. Therefore, these interfaces cannot be used simultaneously. When using TRACE, it is recommended to disconnect any peripheral/expansion board that might be connected to VOUT1 (connected using J19). This is done to minimized the loading/signal integrity impact on TRACE interface.

3.8 UART Terminal

The EVM supports a single UART connection to be used for user terminal. A FT232 device is used to transport the UART information over USB to a host PC. The EVM is designed to use SoC's UART1 as the primary terminal connection, and is connected to port A of the USART transceiver. The USB-side of the FT2232 device is powered from the USB port, and the connection will stay active regardless of power state of the EVM. The green LED (DS6) is used to indicate the USB connection is available.

- USART device to be used: FTD Chip FT232RQ

A USB cable (mini-B to type A) is used to connect the EVM to a PC, and is included as part of the EVM kit.

The EVM can support a second UART connection the FT232 device and is intended to be used for peripheral booting. However, this configuration requires board modifications, and is recommended only for specific users.

3.9 DCAN/CAN Interfaces

The EVM supports access to two DCAN interfaces though pin headers: JP1 and JP2. The SoC supports CAN-FD on either DCAN interface. Both interfaces are connected to 10-pin CAN/CAN-FD headers (J20, J21) through a CAN/CAN-FD transceiver.

- CAN-FD device used: Texas Instruments TCAN1042HGVQ1

3.10 Universal Serial Bus (USB)

The SoC includes two integrated USB transceivers, both supported on the EVM. USB3.0 super-speed bus (USB1) is supported using port USB1 to a mini-AB type connector (P8). This interface supports rates up to 5 Gbps and can operate in host or device mode. The EVM includes capabilities to set and read the connector's ID pin. This supported using the IO expander (EXP2 P1 for USB1). In addition, DIP switch SW2 provides ability to manual set the individual ID value either high (OFF) or low (ON).

USB2.0 interface is connected to high speed USB Hub, and can support rates up to 480 Mbps. The hub provides 2 downstream USB Host ports. One port is connected to Type-A Host connecter, and is available for user to attached external USB devices. The second port is connected to the LCD panel interface, and it is expected to be used for USB-based touch controllers.

All USB interfaces can supply VBUS to peripheral when in host mode by enabling the VBUS switch (controlled via the SoC). However, the EVM cannot be powered from VBUS when operating in device mode.

3.11 Wired Ethernet

Dual Gigabit Ethernet ports are supported on the EVM. RGMII ports 0 and 1 drive the Texas Instruments DP83867 Gigabit PHYs. The PHYs are configured through the Management Data Input/Output (MDIO) bus, with the address set to 0x2 (port 0) and 0x3 (port 1). PHYs are reset at Power-on, but can also be independently reset using the IO expander. Both ports share a common interrupt signal (GPIO6_16).

- IO Expander Control: EXP1, P10 (PHY 0 Reset), P11 (PHY 1 Reset)

NOTE: For the PHY configuration, configure DP83867's RGMII Control Register (RGMIICTL) for RGMII mode and the RGMII Delay Control Register (RGMIIDCTL) for 0 ns TX delay, 2.25 ns RX delay. Set IO Drive Strength Register (IO_IMPEDANCE_CTRL) to maximum drive.

3.12 Video Output

The EVM supports three different options for supporting video output: HDMI (integrated PHY with audio), generic LCD/Display Panel with touch, and FPD-link. Each can be supported independently or all can be used simultaneously.

3.12.1 HDMI Display

The SoC includes a integrated HDMI display interface, which is supported on a type A HDMI connector. The interface supports 1080p with 24b color. A communication channel (DDC/CEC) is supported to the HDMI connector for communication with the HDMI panel. A monitor detect indication is also provided. The DDC/CED interface and monitor detect signals (HPD) are translated through the transceiver, and can be controlled using GPIO from the SoC.

- DDC Transceiver used: Texas Instruments TPD12S016
- Transceiver Control: GPIO7_30 (Lvl Shift Reg Enable, HPD), GPIO7_31 (DDC/CEC Enable)

3.12.2 LCD/Display With Touch Panel

The EVM supports a generic LCD/display panel interface for supporting video output to a display panel. The SoC VOUT1 resource is used drive up to 24b RGB data to interface. The interface supports resource connections for interfacing with a touch panel for advanced user interfaces. These include a control bus (I2C1), USB host interface (USB2), and interrupt for touch indications.

- Connector used: Sametc QSH-030-01

An LCD panel is not included with the CPU EVM, but can be ordered and included as part of an assembly kit.

3.12.3 FPD-Link III Output/Panel

The EVM includes a 720p FPD-link III parallel to serial interface on VOUT3. It supports up to 24 bits of data and can operate at pixel rates up to 85 MHz. An interrupt is supported to enable back-channel communication, typically needed if supporting touch screen. Power control to the panel is also supported via SoC GPIO. The transceiver is configured using I2C (port 3, 0x1B).

Note that the interface clock from the SoC to transceiver is first passed through a de-jitter device to ensure the clock is optimal. This is typically needed if the frequency of the clock is above 70 MHz. The de-jitter IC is configured via I2C (port 1, 0x65).

- Serializer device used: Texas Instruments DS90UH921Q
- Clock de-jitter device used: Texas Instruments CDCE813-Q1
- Connector used: Automotive HSD Connector, right-angle plug for PCB, Rosenberger D4S20D-40ML5-Z

3.13 Video Input

3.13.1 Parallel Imaging

Parallel video input is supported through connections from external sensors and transceivers. The SoC port VIN2A is routed to the connector interface designed to mate with the camera sensors from Leopard Imaging. This approach provides flexibility for customers to select from a variety of available modules, while also supporting connections of custom solutions. The attached module can be configured using either I2C (port 5) or SPI (port 1).

- Connector used: FPC 36 position, 0.5 mm, Molex 052559-3679

3.13.2 Serial Imaging

Serial video input is supported through connections from external sensors and transceivers. The SoC port CSI2-0 is routed to the connector interface designed to mate with camera sensors from Leopard Imaging. This approach provides flexibility for customers to select from a variety of available modules.

Both serial ports (CSI2-0 and CSI2-1) are routed to an expansion connector for supporting a variety of custom solutions. Both interfaces support additional signals for control/configuration of the attached modules (I2C port 5, SPI port 1). These additional signals can be translated to either 1.8 V IO or left at 3.3 V I/O, depending on the configuration setting (Dip Switch SW6 position 4).

- LI Connector used: FPC 36 position, 0.5mm, Molex 052559-3679
- Connector used: Samtec QSH-020-01-L-D-DP-A

3.14 Mini-PCIe

The EVM supports a mini-PCIe (dual lane) interface for connecting with a variety of external modules. An on-board clock generator CDCM9102 provides the 100 MHz reference clock to both the SoC and attached modules. The EVM support two different PCIe reset configurations, select using DIP switch SW6 position 8. The default setting of ON provides ability for SoC to reset the PCIe peripheral. The switch setting of OFF provides ability for the PCIe peripheral to reset the SoC.

3.15 MOST Audio Local Bus (MLB)

The EVM supports a MOST Audio Local Bus interface for connecting to the external hardware (such as the SMSC OS81110/2+0 Physical Interface Board). The interface supports both 3-pin MediaLB and 6-pin MediaLB+ configurations.

- Connector used: Samtec QSH-020-01-L-D-DP-A

3.16 Audio

The EVM supports on-board AIC3106 audio codec for analog audio conversions. Analog inputs are supported on two 3.5 mm audio jacks, including stereo line inputs (P12) and mono microphone (P11). Analog outputs are supported on two 3.5 mm audio jacks, providing stereo line outputs (P13) and stereo headset (P14). The digital audio is connected to SoC using multi-channel serial port (McASP3). The codec requires a master clock (AHCLKX). The audio codec is configured using I2C1, and is accessed at address 0x19.

3.17 COM8 Module Interface

A connector is provided to facilitate the plugging in of TI COM8Q modules, which provide features such as Bluetooth and WiFi. The COM8Q interface requires a 3.6 V power supply, thus a dedicated regulator is provided. All signals on the COM8Q interface are required to 1.8 V, thus voltage translators are placed to convert from the standard IO levels of 3.3 V.

- Connector used: Samtec MEC6-150-02-S-D-RA1

3.18 eFuse Programming Supply

The EVM provides enabling/disabling support for SoC eFUSE programming supply. As a protection, two separate steps are required to enable the programming supply. The DIP switch SW6.p7 must be set ON (default is OFF) and IO expander (EXP2, P17) must be low by software (default is high).

NOTE: The use of this feature is recommended only for specific users.

3.19 User Interface LEDs/Switches

CPU board has four User Interface LEDs for debug, status indication and so on. Details about the User interface LED and its control are shown in Table 8.

Table 8. User LEDs

LED	Controlled By
DS2	IO Expander EXP1, position P7
DS3	IO Expander EXP1, position P6
DS4	IO Expander EXP1, position P5
DS5	IO Expander EXP1, position P4

CPU board has four User Interface switches for debug, mode configuration, and so on. Details about the User interface Switches and its access are shown in Table 9.

Table 9. User Switches

Switch	Accessed By
SW10.1	IO Expander EXP2, position P2
SW10.2	IO Expander EXP2, position P6
SW10.3	IO Expander EXP2, position P7
SW10.4	IO Expander EXP1, position P15

3.20 Power Monitoring

The CPU board has provisions to monitor power for many of the systems primary power rails. The measurement system is implemented using the TI INA226 I2C current shunt/power monitors. The INA226 device monitors both power supply voltage and shunt current measurements. Information is connected from the INA226 devices using dedicated I2C bus(s). The INA226s can be accessed via an off-board modules (FTDI USART, MSP430, or similar device). There is also the option the access the INA devices from the SoC processor. To enable, the EVM must be configured to enable I2C2 bus. (Note this requires loss of HDMI-DDC functionality). Setting IO expander (EXP3, P0) low switches to I2C2 mode (default is HDMI-DDC). IO expander (EXP3, P3) is then used to select between the 2 different power measurement buses.

Table 10 shows a mapping of the current monitoring system. INA226 are located at each shunt location.

Table 10. Power Monitor Mapping

I2C BUS A			
I2C Addr	**Power Net**	**Shunt/Resistor**	**Description**
0x40	VDD_MPU_AVS	10m-Ω	CPU MPU AVS Power Rail
0x41	VDD_GPU_AVS	10m-Ω	CPU GPU AVS Power Rail
0x42	VDD_DSPEVE_AVS	10m-Ω	CPU DSPEVE AVS Power Rail
0x43	VDD_CORE_AVS	10m-Ω	CPU CORE AVS Power Rail
0x44	VDD_IVA_AVS	10m-Ω	CPU IVA AVS Power Rail
0x45	VDDSHV_3V3	10m-Ω	CPU IO power rail (except VDDSHV8)
0x46	VDDR_MEM_1V35	10m-Ω	DDR Memory Power Rail
0x47	VDDR_SOC_1V35	10m-Ω	CPU DDR Power Rail
0x48	VIO_1V8	10m-Ω	EVM 1v8 Peripheral Rail
0x49	VDDS_1V8	10m-Ω	CPU VDDS Power Rail
0x4A	VDDSHV8	10m-Ω	CPU IO power rail for VDDSHV8
0x4B	VDDA_USB3V3	10m-Ω	CPU USB3v3 power rail
0x4C	VDA_PLL_1V8	10m-Ω	CPU PLL Power Rail

Table 10. Power Monitor Mapping (continued)

I2C BUS A			
I2C Addr	**Power Net**	**Shunt/Resistor**	**Description**
0x4D	VDA_PHY2_1V8	10m-Ω	CPU PHY Power Rail (HDMI, SATA, USB2)
0x4E	VDA_PHY1_1V8	10m-Ω	CPU PHY Power Rail (CSI2, PCIe)
I2C BUS B			
0x40	EVM_12V	10m-Ω	Total System 12v power rail
0x41	EVM_5V0	10m-Ω	Total System 5v0 power rail
0x42	VSYS_3V3	10m-Ω	Total System 3v3 power rail
0x43	VIO_3V3	10m-Ω	EVM 3v3 Peripheral Rail
0x44	VPIN_B01_3V3	20m-Ω	LP87565 SMPS Input Power (MPU)
0x45	VPIN_B23_3V3	20m-Ω	LP87565 SMPS Input Power (GPU)
0x46	VPIN_S12_3V3	20m-Ω	TPS917 SMPS Input Power (DSPEVE)
0x47	VPIN_S3_3V3	20m-Ω	TPS917 SMPS Input Power (CORE)
0x48	VPIN_S4_3V3	20m-Ω	TPS917 SMPS Input Power (IVA)
0x49	VPIN_S5_3V3	20m-Ω	TPS917 SMPS Input Power (1V8)
0x4A	VPIN_LDO_3V3	20m-Ω	TPS917 LDO Input Power (PLL, PHY1/2)
0x4B	VPIN_LDO_5V0	20m-Ω	TPS917 LDO Input Power (USBPHY)

3.21 I2C Peripheral Map

Table 11 shows the list of I2C interface available on the EVM with a list of devices connected to each I2C interface and its corresponding device address.

Table 11. I2C Device Address Chart

CPU Board	Part No	I2C1	I2C3	I2C4	I2C5	Device Addr (7b)
FPD-Link Xmit	DS90UB921-Q1		X			0x0C
Audio Codec	AIC3016	X				0x19
FPD-Link Xmit (High Res)	DISABLED					0x1A
GPIO Expander #1	PCF8575	X				0x20
GPIO Expander #2	PCF8575	X				0x21
GPIO Expander #3	PCF8575	X				0x26
Temperature Sensor	TMP102	X				0x48
EEPROM	24WC256	X				0x50
PMIC	TPS917	X				0x58-5B, 0x12
	LP87565	X				0x60
FPD-Link Clock	CDC813-Q1	X				0x65
MLB Connector	Connector	X				NA
COM8 Connector	Connector	X				NA
LCD Interface	Connector		X			NA

Table 11. I2C Device Address Chart (continued)

CPU Board	Part No	I2C1	I2C3	I2C4	I2C5	Device Addr (7b)
LI Camera Interface	Connector				X	NA
CSI2 Camera Interface	Connector				X	NA
Expansion Connector	Connector	X	X	X	X	NA

3.22 GPIO List

Table 12 shows the SoC GPIO list. Signals used for GPIO on expansion boards are not included in this list, as they are dependent on the application board used.

Table 12. SoC GPIO Map

Feature	Peripheral Device	EVM Bd Net	Function	SoC GPIO
Test	Automated Test Connector	GP5[0]	USER_DEFINED	GPIO5_0
HDMI/DDC	HDMI-DDC Level Translator/HPD (TPD12S016)	HDMI_LS_OE	HDMI-DDC Enable	GPIO7_31
HDMI/DDC	HDMI-DDC Level Translator/HPD (TPD12S016)	HDMI_CT_HPD	Monitor Detect/Enable	GPIO7_30
Connectivity on Module	COM8 Connector	H_GP5[4]	Bluetooth Enable	GPIO5_4
Connectivity on Module	COM8 Connector	H_GP5[5]	GPS PPS Output	GPIO5_5
Connectivity on Module	COM8 Connector	H_GP5[6]	GPS Time Stamp	GPIO5_6
Connectivity on Module	COM8 Connector	H_GP5[7]	WLAN Interrupt	GPIO5_7
Connectivity on Module	COM8 Connector	H_GP5[8]	WLAN Enable	GPIO5_8
Media Local Bus(MLB)	MLB Connector	H_GP5[9]	NA	GPIO5_9
Media Local Bus(MLB)	MLB Connector	H_GP6_[28]	NA	GPIO6_28
IO Expander	I2C/IO Expander (3x PCF8575)	H_PCF8575_INT	Interrupt	GPIO1_3
Gig Ethernet	Ethernet PHY(s) (2x DP83867)	ENET_INTSn	Interrupt	GPIO6_16
LCD Touch Panel	LCD Panel Connector	H_GP1[2]_TOUCH	Interrupt	GPIO1_2
LCD Touch Panel	LCD Panel Connector	CON_LCD_PWR_DN	Power Down	GPIO3_1
FPD-Link Panel	FPD-Link-III PHY (DS90UB921-Q1)	VOUT3_INTB	Interrupt	GPIO2_1
FPD-Link Panel	FPD-Link-III PHY (DS90UB921-Q1)	DISP2_VPOC_ONN	Enable	GPIO2_2
Power Mgmt	PMIC (LP87565)	H_WKUP_0	Interrupt	GPIO1_0
Power Mgmt	PMIC (TPS65917)	H_WKUP_1	Interrupt	GPIO1_1
Power Mgmt	PMIC (TPS65917)	POWERHOLD_CLK	System Power Down	GPIO3_30
SD Card	Micro-SD Connector	H_MMC1_SDCD	Card Detect	GPIO6_27
SD Card	Micro-SD Connector	H_MMC_PWR_ON	Card Power Enable	GPIO4_21

NOTE: Functional signals of pin mux are not considered for this table.

3.23 I/O Expander List

Table 13. I/O Expander Map

Device	Slave Address	I2C I/F	Expander IO	Netname	Description
EXP1	0b0010 000 (0x20)	I2C1	INT#	H_PCF8575_INT	Interrupt output to SoC
			P0	TS_LCD_GPIO1	Press Button Switch 1
			P1	TS_LCD_GPIO2	Press Button Switch 2
			P2	TS_LCD_GPIO3	Press Button Switch 3
			P3	TS_LCD_GPIO4	Press Button Switch 4
			P4	USER_LED1	User LED 1
			P5	USER_LED2	User LED 2
			P6	USER_LED3	User LED 3
			P7	USER_LED4	User LED 4
			P10	EXP_ETH0_RSTn	RGMII0 Reset
			P11	EXP_ETH1_RSTn	RGMII1 Reset
			P12	USB1-VBUS_OCN	USB1 Over Current Indication
			P13	USB2-VBUS_OCN	USB2 Over Current Indication
			P14	PCI_SW_RESETn	PCI Interface SW Reset
			P15	USER_SW10_4	User Switch Input
			P16	USB2-VBUS_DET	USB2 VBUS Detection
			P17	USB1-VBUS_DET	USB1 VBUS Detection
EXP2	0b0010 001 (0x21)	I2C1	INT#	PCF8575_INT	Interrupt output to SoC
			P0	SEL_GPMC_AD_VID_S0	MUX out control signal for GPMC vs VOUT3B
			P1	USB1_ID	USB1 ID PIN
			P2	USER_SW10_1	User Switch Input
			P3	SEL_I2C3_CAN2	MUX out control signal for I2C3 Vs DCAN2
			P4	SEL_ENET_MUX_S0	MUX out control signal for RGMII0 Vs VIN
			P5	SEL_EXP_I2C3_DCAN2	Enable I2C3/DCAN2 Signals to Expansion
			P6	USER_SW10_2	User Switch Input
			P7	USER_SW10_3	User Switch Input
			P10	NAND_BOOTn	NAND boot Chip select enable signal
			P11	NOR_BOOTn	NOR boot Chip select enable signal
			P12	MMC2_BOOT	MUX out control signal for GPMC Vs MMC2
			P13	TMP102_ALERT	Temperature sensor alert indicator

Table 13. I/O Expander Map (continued)

Device	Slave Address	I2C I/F	Expander IO	Netname	Description
			P14	UART_SEL1_3	Selection for Terminal UART1 or UART3
			P15	MCASP1_ENn	COM8 interface level shifter enable signal
			P16	SEL_UART3_SPI2	MUX out control signal for UART3 Vs SPI2
			P17	PFC_VPP_ENn	Enable for VPP power supply
EXP3	0b0010 010 (0x26)	I2C1	P0	PM_OEn	Enable to connect PM Bus with I2C3
			P1	VIN6_SEL_S0	MUX out control signal for McASP3/7 to AIC/BT or Expansion
			P2	VIN2_S0	MUX out control signal for EMAC1 and VIN2A Signals
			P3	PM_SEL	Selection to connect I2C3 to either PM bus 1 or 2
			P4	<open>	N/A
			P5	<open>	N/A
			P6	VIN2_S2	MUX out control signal for VIN2A vs expansion signals
			P7	<open>	N/A
			P10	SEL_CSI2n	MUX out control signal for CSI2 configuration
			P11	EXVIN2_S0	MUX out control signal for EMAC1 vs VIN2A vs expansion signals
			P12	EXVIN2_S2	MUX out control signal for EMAC1 vs VIN2A vs expansion signals
			P13	DISP1_VPOC_ONN	Power Enable for Display Panel
			P14	MMC2_BOOT_OVR_OEN	MMC2 DIP Switch Override Enable
			P15	MMC2_BOOT_OVR	MMC2 DIP Switch Override
			P16	NOR_BOOT_OVR_OEN	NOR BOOT DIP Switch Override Enable
			P17	NOR_BOOT_OVR	NOR BOOT DIP Switch Override

3.24 Configuration EEPROM

The CPU board contains a EEPROM memory device for storing and retrieving configuration information. The EEPROM provides 256Kb (or 32KBytes) of storage space, and is accessible via I2C. (Note that the device location information is located in the I2C device table.) The configuration ID information is programmed by the factory at the time of manufacturing and should not be altered. Below is the configuration data format within the EEPROM.

- EEPROM device used: Catalyst Semiconductor CAT24C256WI-G
- I2C Bus/Addr: I2C1,0x50

Data format of the EEPROM is provided in Table 14.

Table 14. Data Format of the EEPROM

EEPROM Field	Byte Location	Value (Rev A CPU Board example)	Description
ID.HEADER	[3:0]	0xAA5533EE	Fixed value at start of header ID.
ID.BOARD_NAME	[19:4]	'DRA76/7xP,TDA2P' (ascii)	For J6P-Family ACD Package - fixed value of 'DRA76/7xP,TDA2P'
ID.VERSION_MAJOR	[21:20]	0xC	A=0x1 B=0x2 C=0x3
ID.VERSION_MINOR	[23:22]	0x0	0x0 for major revision 0x1-0x15 for others
ID.CONFIG_OPTION	[27:24]	0x3E	Bit 6: 1 – EMIF2 ECC Supported, 0 – No Bit 5: 1 – EMIF2 Supported, 0 – No Bit 4: 1 – EMIF1 ECC Supported, 0 – No Bit 3: 1 – EMIF1 Supported, 0 – No Bit 2: 1 – Extended Memory EEPROM Cfg Support, 0 – No (1) Bit 1: 1 – MAC addr in EEPROM (default) Bit 0: 0 - QSPI (default), 1 - NOR
EMIF1_SIZE_BYTES	[31:28]	0x8000 0000	Memory size for EMIF1 in bytes (unsigned long)**
EMIF2_SIZE_BYTES	[35:32]	0x8000 0000	Memory size for EMIF2 in bytes (unsigned long)**
RESERVED	[55:36]	0x0	Reserved**
MAC_ADDR	0x7F00	00.0E.99.zz.yy.xx	Optional MAC address

(1) If Bit 2 is set to 0, all EEPROM data beyond is set to 0 (not defined or used). If it is set to 1, the mapping is per the table.

For reference, a C-style coded structure is provided.

```
Struct EEPROM_ID_T
{
    Unsigned long header;              4
    Char board_name[16];               16
    Unsigned short version_major;      2
    Unsigned short version_minor;      2
    Unsigned long config_option;       4
    Unsigned long emif1_size_bytes;    4
    Unsigned long emif2_size_bytes;    4
    Char reserved[28];                 20
} eeprom_id;
```

4 Signal Multiplex Logic

Due to the high level of multiplexing on the SoC (16+ levels), multiplex control logic is required in order to use the same SoC pins with their various functionality. The information shown in Table 15 provides descriptions of the EVM mux logic.

An I2C-based IO expander is used to control the on-board muxes. Table 15 shows the specific bit(s) assigned to each mux, as well as the specific settings for the various selections.

Table 15. On-Board Mux Setting/Control

MUX	Control Bits	Value	Mux Setting
A	N/A	N/A	NOR Memory (requires mod)
		N/A	QSPI Memory (default)
H (RU18)	EXP3.P1 (VIN6_SEL_S0)	'0'	MCA3/7 to AIC/COMQ8-BT
		'1'	Signals to Expansion (default)
M (RU19)	EXP3.P0 (PM_OEn)	'0'	I2C2 to Power Measurement
		'1'	DDC to HDMI Port (default)
K (RU23)	EXP2.P16 (SEL_UART3_SPI2) '0'	'0'	UART3 to COMQ8/BT
		'1'	SPI2 to Expansion (default)
L (RU22, RU24, RU25)	EXP2.P3 (SEL_I2C3_CAN2)	'0'	DCAN2/MCAN to CAN-FD
		'1'	I2C3 to Displays (default)
	EXP2.P5 (SEL_EXP_I2C3_DCAN2)	'0'	DCAN2/I2C3 to Expansion
		'1'	DCAN2/I2C No Expansion
B (RU13, RU16, RU7)	EXP2.P0 (SEL_GPMC_AD_VID_S0)	'0'	VOUT3B to FPD-Link Display
		'1'	GPMC NOR/NAND (default)
	SW6.P[2:1]	OFF/ ON	GPMC to NAND (Bootable)
		ON/ OFF	GPMC to NOR (Bootable)
D (RU8, RU4)	EXP3.P[6,2] (VIN2_S2, VIN2_S0)	'01'	VIN2A to LI Camera
		'10'	VIN2A to Expansion
		'11'	Open (default)
F (RU15)	EXP3.P[12:11] (EXVIN2_S2, EXVIN2_S0)	'01'	VIN2A-Upper* to LI Camera
		'10'	VIN2A-Upper* to Expansion
		'11'	RGMII1 to Gig PHY (default)
J (RU14, RU17)	EXP2.P4 (SEL_ENET_MUX_S0)	'0'	VIN4B/GPIO to Expansion
		'1'	RGMII0 to Gig PHY (default)
C (RU5)	SW6.[3]	OFF	GPMC to NOR
		ON	MMC2 to eMMC
	EXP3.P[15:14]	'00'	eMMC Memory
		'11'	Memory selected by SW6.3

4.1 GPMC/QSPI Selection (Mux A)

Table 16 is part of the SoC pinmux table for GPMC. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These include:

- Memory Bus (GPMC): A[18:13], CS[2]
- Quad Serial Bus (QSPI): SCLK, RTCLK, CS[0], D[3:0]

Table 16. SoC Pinmux for GPMC/QSPI

Pad Name	Function 1		Function 2	
gpmc_a[13]	GPMC	gpmc_a[13]	QSPI1	qspi1_rtclk
gpmc_a[14]	GPMC	gpmc_a[14]	QSPI1	qspi1_d[3]
gpmc_a[15]	GPMC	gpmc_a[15]	QSPI1	qspi1_d[2]
gpmc_a[16]	GPMC	gpmc_a[16]	QSPI1	qspi1_d[0]
gpmc_a[17]	GPMC	gpmc_a[17]	QSPI1	qspi1_d[1]
gpmc_a[18]	GPMC	gpmc_a[18]	QSPI1	qspi1_sclk
gpmc_cs[2	GPMC	gpmc_cs[2]	QSPI1	qspi1_cs[0]

Mux A: Selects between GPMC (NOR memory) and QSPI memory support.

NOTE: The mux is implemented using resistors. This is due to the signal rate and routing restrictions of the QSPI interface. To enable the GPMC signals to NOR (shown in RED), the board must be modified to move resistors.

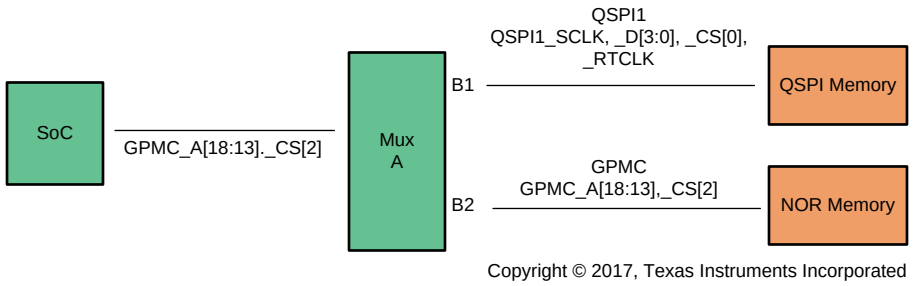


Figure 7. Mux Diagram for GPMC/QSPI

4.2 GPMC/VOUT3 Selection (Mux B)

Table 17 is part of the SoC pinmux table for GPMC. The SoC device supports additional functions not shown in Table 17. The functions shown are intended to reflect those supported on the EVM. These include:

- Memory Bus (GPMC): AD[15:0], A[12:0], CS[3]
- General Purpose I/O (GPIO2): GPIO2_2
- Video Output Port (VOUT3): CLK, HSYNC, VSYNC, DE, D[23:0]
- Boot Mode Selection (SYSBOOT): SYSBOOT[15:0]

Table 17. SoC Pinmux for GPMC/VOUT3

Pad Name	Function 1		Function 4		Function 15		Function 16	
gpmc_ad[15]	GPMC	gpmc_ad[15]	DSS	vout3_d[15]			CHIPGLUE	sysboot15
gpmc_ad[14]	GPMC	gpmc_ad[14]	DSS	vout3_d[14]			CHIPGLUE	sysboot14
gpmc_ad[13]	GPMC	gpmc_ad[13]	DSS	vout3_d[13]			CHIPGLUE	sysboot13
gpmc_ad[12]	GPMC	gpmc_ad[12]	DSS	vout3_d[12]			CHIPGLUE	sysboot12
gpmc_ad[11]	GPMC	gpmc_ad[11]	DSS	vout3_d[11]			CHIPGLUE	sysboot11
gpmc_ad[10]	GPMC	gpmc_ad[10]	DSS	vout3_d[10]			CHIPGLUE	sysboot10
gpmc_ad[9]	GPMC	gpmc_ad[9]	DSS	vout3_d[9]			CHIPGLUE	sysboot9
gpmc_ad[8]	GPMC	gpmc_ad[8]	DSS	vout3_d[8]			CHIPGLUE	sysboot8
gpmc_ad[7]	GPMC	gpmc_ad[7]	DSS	vout3_d[7]			CHIPGLUE	sysboot7
gpmc_ad[6]	GPMC	gpmc_ad[6]	DSS	vout3_d[6]			CHIPGLUE	sysboot6
gpmc_ad[5]	GPMC	gpmc_ad[5]	DSS	vout3_d[5]			CHIPGLUE	sysboot5
gpmc_ad[4]	GPMC	gpmc_ad[4]	DSS	vout3_d[4]			CHIPGLUE	sysboot4
gpmc_ad[3]	GPMC	gpmc_ad[3]	DSS	vout3_d[3]			CHIPGLUE	sysboot3
gpmc_ad[2]	GPMC	gpmc_ad[2]	DSS	vout3_d[2]			CHIPGLUE	sysboot2
gpmc_ad[1]	GPMC	gpmc_ad[1]	DSS	vout3_d[1]			CHIPGLUE	sysboot1
gpmc_ad[0]	GPMC	gpmc_ad[0]	DSS	vout3_d[0]			CHIPGLUE	sysboot0
gpmc_a[0]			DSS	vout3_d[16]				
gpmc_a[1]	GPMC	gpmc_a[1]	DSS	vout3_d[17]				
gpmc_a[2]	GPMC	gpmc_a[2]	DSS	vout3_d[18]				
gpmc_a[3]	GPMC	gpmc_a[3]	DSS	vout3_d[19]				
gpmc_a[4]	GPMC	gpmc_a[4]	DSS	vout3_d[20]				
gpmc_a[5]	GPMC	gpmc_a[5]	DSS	vout3_d[21]				
gpmc_a[6]	GPMC	gpmc_a[6]	DSS	vout3_d[22]				
gpmc_a[7]	GPMC	gpmc_a[7]	DSS	vout3_d[23]				
gpmc_a[8]	GPMC	gpmc_a[8]	DSS	vout3_hsync				
gpmc_a[9]	GPMC	gpmc_a[9]	DSS	vout3_vsync				
gpmc_a[10]	GPMC	gpmc_a[10]	DSS	vout3_de				
gpmc_a[11]	GPMC	gpmc_a[11]	DSS	vout3_fld				
gpmc_a[12]	GPMC	gpmc_a[12]			GPIO2	gpio2_2		
gpmc_cs[3]			DSS	vout3_clk				

Mux B: The selector bit and selects between on-board memories and FPD-Link LCD panel. The selection is made using the IO expander #2, bit P0. The defaults are set to enable GPMC to NOR/NAND memories – which is required for SYSBOOT mode latching.

If booting from NOR/NAND memories, the selection for chip select 0 is made using switch SW6 position 1 (NOR) and position 2 (NAND).

NOTE: Only one of these boot devices can be enabled at any time

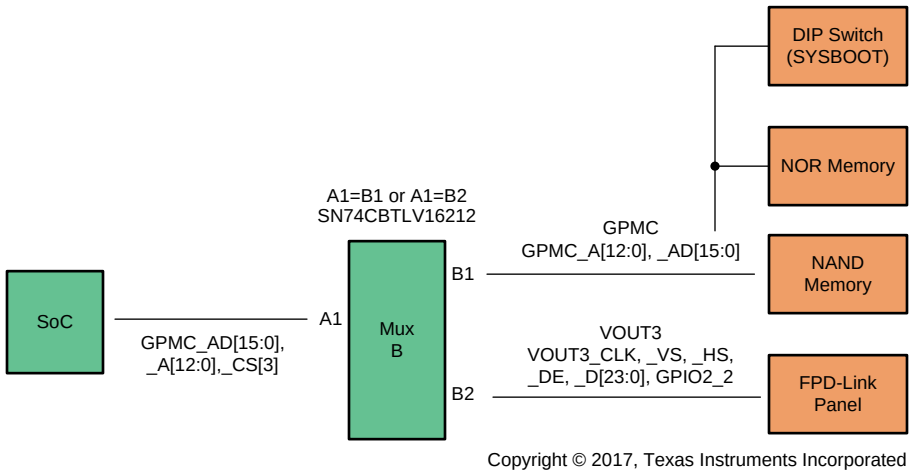


Figure 8. Mux Diagram for GPMC/VOUT3

4.3 GPMC/EMMC Selection (Mux C)

Table 18 shows part of the SoC pinmux table for GPMC. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These include:

- Memory Bus (GPMC): A[27:19], CS[1]
- EMMC Memory (MMC2): CLK, CMD, D[7:0]

Table 18. SoC Pinmux for GPMC/EMMC

Pad Name	Function 1		Function 2	
gpmc_a[19]	GPMC	gpmc_a[19]	MMC2	mmc2_dat[4]
gpmc_a[20]	GPMC	gpmc_a[20]	MMC2	mmc2_dat[5]
gpmc_a[21]	GPMC	gpmc_a[21]	MMC2	mmc2_dat[6]
gpmc_a[22]	GPMC	gpmc_a[22]	MMC2	mmc2_dat[7]
gpmc_a[23]	GPMC	gpmc_a[23]	MMC2	mmc2_clk
gpmc_a[24]	GPMC	gpmc_a[24]	MMC2	mmc2_dat[0]
gpmc_a[25]	GPMC	gpmc_a[25]	MMC2	mmc2_dat[1]
gpmc_a[26]	GPMC	gpmc_a[26]	MMC2	mmc2_dat[2]
gpmc_a[27]			MMC2	mmc2_dat[3]
gpmc_cs[1]			MMC2	mmc2_cmd

Mux C: Selects between on board NOR memory and EMMC memory. The selection is made using dip switch setting (SW6 pin 3), or can be set using the IO expander #3, bits P15:14. If booting from EMMC, the DIP Switch SW6 position 3 is used to select interface.

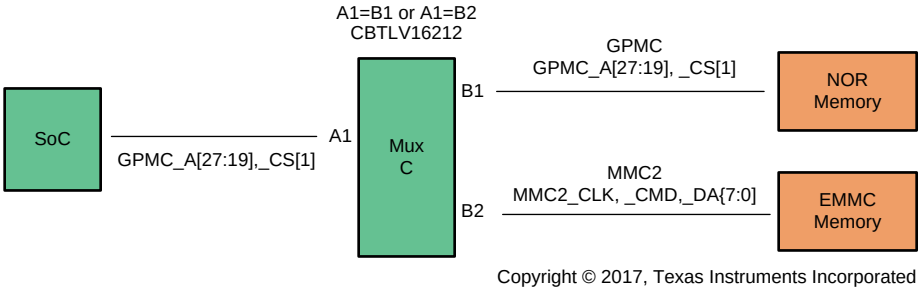


Figure 9. Mux Diagram for GPMC/EMMC

4.4 VIN2A Selection (Mux D)

Table 19 is part of the SoC pinmux table for VIN2A. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These include:

- Video Input Port (VIN2A): D[11:0], CLK, DE, HSYNC, VSYNC

Table 19. SoC Pinmux for VIN2A

Pad Name	Function 1	
vin2a_d[0]	VIP1	vin2a_d[0]
vin2a_d[1]	VIP1	vin2a_d[1]
vin2a_d[2]	VIP1	vin2a_d[2]
vin2a_d[3]	VIP1	vin2a_d[3]
vin2a_d[4]	VIP1	vin2a_d[4]
vin2a_d[5]	VIP1	vin2a_d[5]
vin2a_d[6]	VIP1	vin2a_d[6]
vin2a_d[7]	VIP1	vin2a_d[7]
vin2a_d[8]	VIP1	vin2a_d[8]
vin2a_d[9]	VIP1	vin2a_d[9]
vin2a_d[10]	VIP1	vin2a_d[10]
vin2a_d[11]	VIP1	vin2a_d[11]
vin2a_clk0	VIP1	vin2a_clk0
vin2a_de0	VIP1	vin2a_de0
vin2a_hsync0	VIP1	vin2a_hsync0
vin2a_vsync0	VIP1	vin2a_vsync0

Mux D: Selects between VIN2A to LI Camera or Expansion. Mux H and I are combined to support both selections. The selection is made using the IO expander #3, bits P6 and P2, with the default set to Expansion.

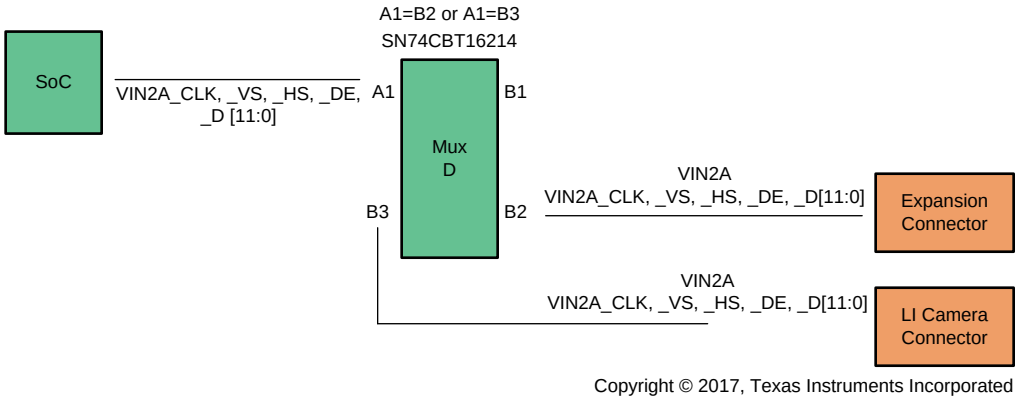


Figure 10. Mux Diagram for VIN2A

4.5 RGMII1/VIN2A Selection (Mux F)

Table 20 is part of the SoC pinmux table for VIN2A (upper data bits). The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These include:

- Gig Ethernet (RGMII1): TXC, TXCTL, TXD[3:0], RXC, RXCTL, RXD[3:0]
- Video Input Port (VIN2A): D[23:12]

Table 20. SoC Pinmux for VIN2A/RGMII1

Pad Name	Function 1		Function 4	
vin2a_d[12]	VIP1	vin2a_d[12]	EMAC	rgmii1_txc
vin2a_d[13]	VIP1	vin2a_d[13]	EMAC	rgmii1_txctl
vin2a_d[14]	VIP1	vin2a_d[14]	EMAC	rgmii1_txd[3]
vin2a_d[15]	VIP1	vin2a_d[15]	EMAC	rgmii1_txd[2]
vin2a_d[16]	VIP1	vin2a_d[16]	EMAC	rgmii1_txd[1]
vin2a_d[17]	VIP1	vin2a_d[17]	EMAC	rgmii1_txd[0]
vin2a_d[18]	VIP1	vin2a_d[18]	EMAC	rgmii1_rxc
vin2a_d[19]	VIP1	vin2a_d[19]	EMAC	rgmii1_rxctl
vin2a_d[20]	VIP1	vin2a_d[20]	EMAC	rgmii1_rxd[3]
vin2a_d[21]	VIP1	vin2a_d[21]	EMAC	rgmii1_rxd[2]
vin2a_d[22]	VIP1	vin2a_d[22]	EMAC	rgmii1_rxd[1]
vin2a_d[23]	VIP1	vin2a_d[23]	EMAC	rgmii1_rxd[0]

Mux F: Selects between Gig Ethernet, LI Camera and Expansion. The selection is made using the IO expander #2, bits P12 and P11, defaulting to Expansion.

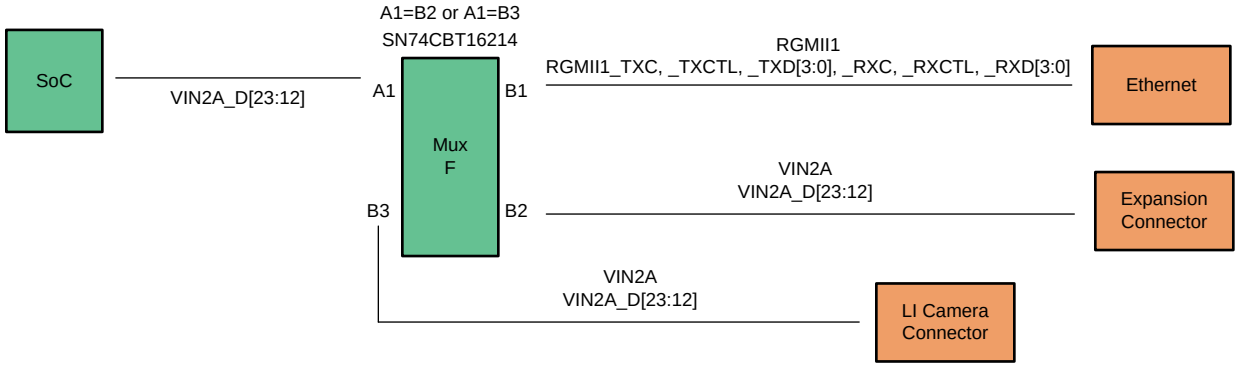


Figure 11. Mux Diagram for VIN2A/RGMII1

4.6 McASP Selection (Mux H)

Table 21 is part of the SoC pinmux table for McASP to AIC3106/COMQ8 or Expansion. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These include:

- Audio Serial Port (McASP3): McASP3 ACLKX, FSX, AXR[1:0]
- Audio Serial Port (McASP7): McASP7 FSX, ACLKX, AXR[1:0]

Table 21. SoC Pinmux for McASP

Pad Name	Function 1		Function 2	
mcasp3_aclkx	MCASP3	mcasp3_aclkx		
mcasp3_fsx	MCASP3	mcasp3_fsx		
mcasp3_axr[0]	MCASP3	mcasp3_axr[0]		
mcasp3_axr[1]	MCASP3	mcasp3_axr[1]		
mcasp2_aclkx				
mcasp1_axr[15]			MCASP7	mcasp7_fsx
mcasp1_axr[14]			MCASP7	mcasp7_aclkx
mcasp1_axr[13]			MCASP7	mcasp7_axr[1]
mcasp1_axr[12]			MCASP7	mcasp7_axr[0]

Mux H: Selects between AIC/COMQ8-BT and Expansion support. The selection is made using the IO expander #3, bits P1, defaulting to Expansion.

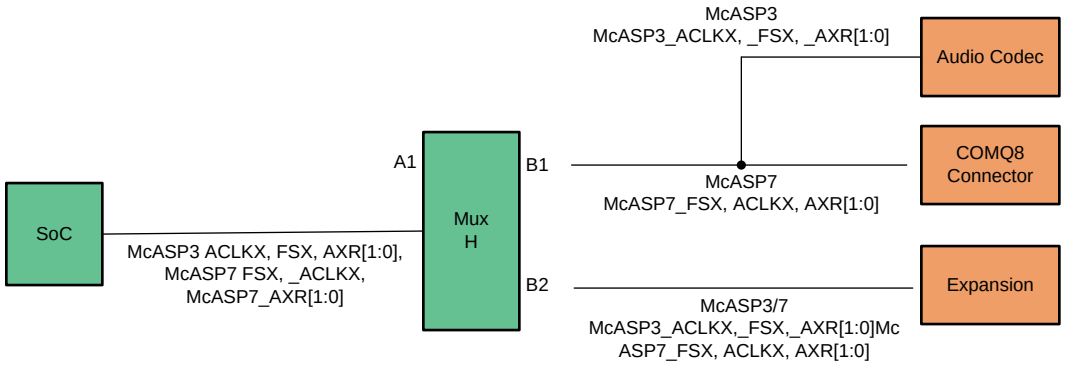


Figure 12. Mux Diagram for McASP3/7

4.7 RGMII0/VIN4B Selection (Mux J)

Table 22 is part of the SoC pinmux table for RGMII0. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These include:

- Gig Ethernet (RGMII0): TXC, TXCTL, TXD[3:0], RXC, RXCTL, RXD[3:0]
- Management Data I/O (MDIO): MCLK, D
- Video Input Port (VIN4B): CLK, HSYNC, VSYNC, [7:0]
- General Purpose I/O (GPIO5): [31:29], 25, 22

Table 22. SoC Pinmux for RGMII0/VIN4B

Pad Name	Function 1		Function 6		Function 15	
rgmii0_rxc	EMAC	rgmii0_rxc	VIP2	vin4b_d[5]		
rgmii0_rxctl	EMAC	rgmii0_rxctl	VIP2	vin4b_d[6]		
rgmii0_rxd[0]	EMAC	rgmii0_rxd[0]			GPIO5	gpio5_31
rgmii0_rxd[1]	EMAC	rgmii0_rxd[1]			GPIO5	gpio5_30
rgmii0_rxd[2]	EMAC	rgmii0_rxd[2]			GPIO5	gpio5_29
rgmii0_rxd[3]	EMAC	rgmii0_rxd[3]	VIP2	vin4b_d[7]		
rgmii0_txd[0]	EMAC	rgmii0_txd[0]			GPIO5	gpio5_25
rgmii0_txd[1]	EMAC	rgmii0_txd[1]	VIP2	vin4b_vsync1		
rgmii0_txd[2]	EMAC	rgmii0_txd[2]	VIP2	vin4b_hsync1		
rgmii0_txd[3]	EMAC	rgmii0_txd[3]			GPIO5	gpio5_22
rgmii0_txctl	EMAC	rgmii0_txctl	VIP2	vin4b_d[4]		
rgmii0_txc	EMAC	rgmii0_txc	VIP2	vin4b_d[3]		
mdio_mclk	EMAC	mdio_mclk	VIP2	vin4b_clk1		
mdio_d	EMAC	mdio_d	VIP2	vin4b_d[0]		
uart3_txd			VIP2	vin4b_d[2]		
uart3_rxd			VIP2	vin4b_d[1]		

Mux J: Selects between Gig Ethernet and Expansion. The selection is made using the IO expander #2, bit P4, defaulting to Gig Ethernet.

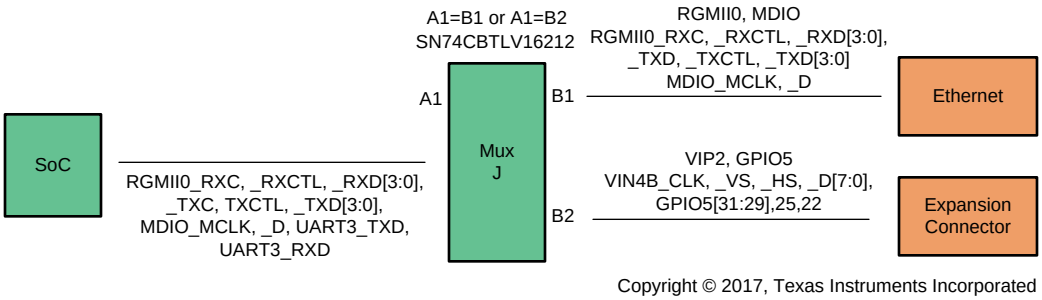


Figure 13. Mux Diagram for RGMII0/VIN1B

4.8 SPI2/UART3 Selection (Mux K)

Table 23 is part of the SoC pinmux table for SPI2. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These include:

- SPI Serial Bus (SPI2): SCLK, D[1:0], CS[0]
- UART Serial Bus (UART3): TXD, RXD, CTSN, RTSN

Table 23. SoC Pinmux for SPI2/UART3

Pad Name	Function 1		Function2	
spi2_sclk	SPI2	spi2_sclk	UART3	uart3_rxd
spi2_d[1]	SPI2	spi2_d[1]	UART3	uart3_txd
spi2_d[0]	SPI2	spi2_d[0]	UART3	uart3_ctsn
spi2_cs[0]	SPI2	spi2_cs[0]	UART3	uart3_rtsn

Mux K: Selects between Bluetooth (COM8Q module) and Expansion interface. The selection is made using the IO expander #2, bits P16, defaulting to Expansion.

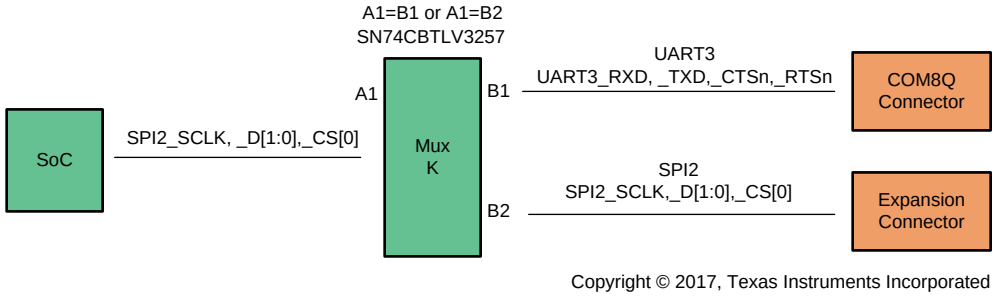


Figure 14. Mux Diagram for SPI2/UART3

4.9 DCAN2/I2C3 Selection (Mux L)

Table 24 is part of the SoC pinmux table for DCAN2. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These include:

- Digital CAN Bus (DCAN2): TX, RX
- I2C Serial Bus (I2C3): SCL, SDA

Table 24. SoC Pinmux for DCAN2

Pad Name	Function 3		Function 10	
gpio6_14	DCAN2	dcan2_tx	I2C3	i2c3_sda
gpio6_15	DCAN2	dcan2_rx	I2C3	i2c3_scl

Mux L: Selects between DCAN2 to CAN/CAN-FD phy and I2C3 for display panel control. The selection is made using the IO expander #2, bits P3, defaulting to I2C3. Additional control is provided by IO expander #2 bit P5, when enables the DCAN2/I2C3 signals access to the expansion interface (default is no access).

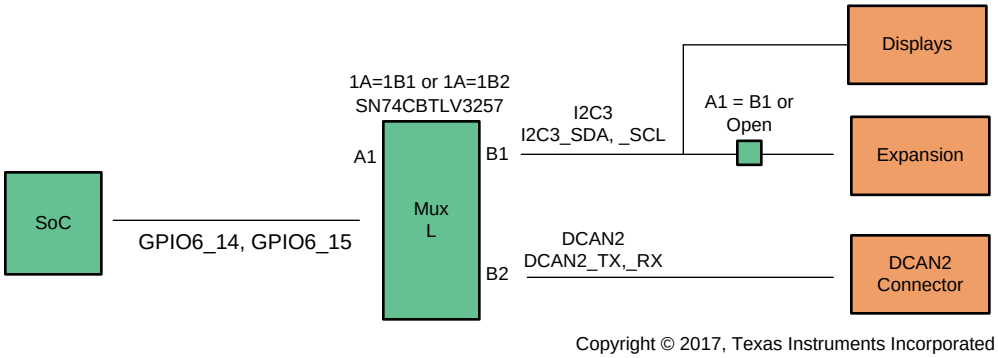


Figure 15. Mux Diagram for DCAN2/I2C

4.10 I2C/DDC Selection (Mux M)

Table 25 is part of the SoC pinmux table for I2C2. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These include:

- I2C Serial Bus (I2C2): I2C2_SCL, I2C2_SDA
- Display Data Channel(DDC): HDMI_DDC_SDA, HDMI_DDC_SCL

Table 25. SoC Pinmux for I2C/HDMI

Pad Name	Function 1		Function 2	
i2c2_scl	I2C2	i2c2_scl	HDMI	hdmi1_ddc_sda
i2c2_sda	I2C2	i2c2_sda	HDMI	hdmi1_ddc_scl

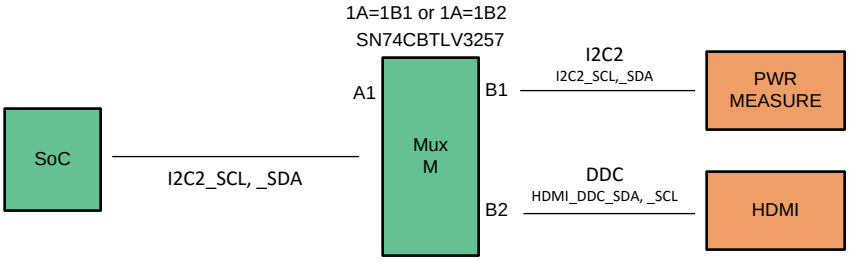


Figure 16. Mux Diagram for I2C/DDC

5 Application Boards

The CPU EVM supports several different interfaces for connecting additional boards/EVMs to enhance the feature set of base EVM. The ability to add either existing applications boards to the systems is provided, or you can design your own. The EVM interfaces that are design for expansion/application boards include:

- Application board expansion – Intended to support a wide range of peripherals/functions. Supports a wide variety of LVCMOS interfaces, including parallel video in/out ports, multi-channel serial ports, I2Cs, UARTs, and GPIO. For a complete list of available IO functions, see the *DRA75xP, DRA74xP Infotainment Applications Processor Silicon Revision 1.0 Data Manual* (SPRS989).
- LCD expansion – Intended to support a display panel with touch. Supports parallel video outputTDA2Px ADAS Applications Processor 23mm Package (ACD Package) Silicon Revision 1.0 Data Manual (, USB2.0, I2C, and GPIO
- Camera expansion – Intended to support video input streams, such as camera sensors. Supports dual MIPI video input channels, I2C, and GPIO

5.1 RGB-to-HDMI Application Board

Assembled with the CPU EVM is an HDMI Panel expansion board, with allows off-the-shelf HDMI panels to be mated with the EVMs LCD panel interface. The expansion board uses the TFP410 for the RGB-to-HDMI translation.

NOTE: The HDMI does not include audio support. The application board uses a USB2.0 port for panels that support touchscreen. An extra power-only USB port is provided if powering the panel via USB

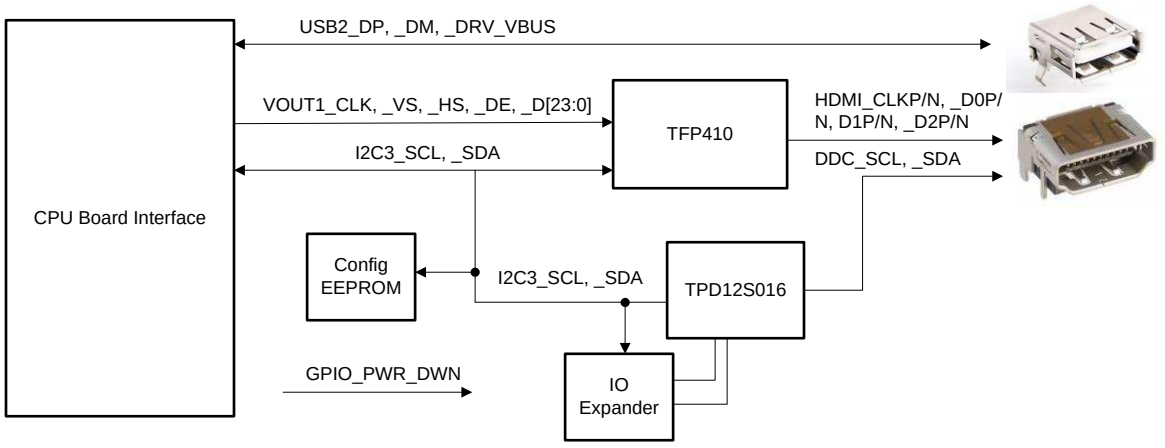


Figure 17. RGB-to-HDMI Application Bd

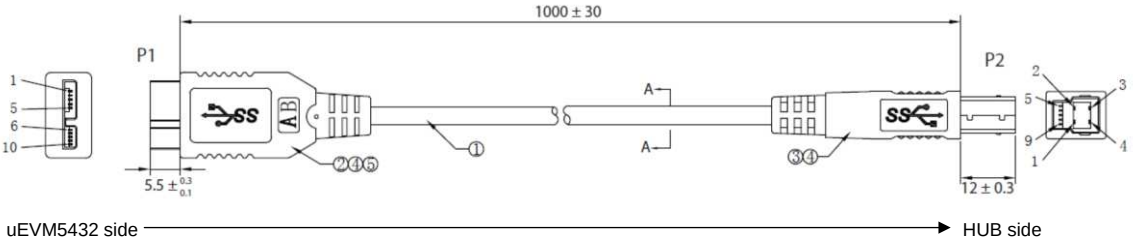
6 USB3 Supported Configurations

The following USB3.x combinations are supportable:

- Micro-A plug to Standard-B plug
  - Connect to hub or external drive/device that has a std B receptacle
- Micro-A plug to Micro-B plug
  - EVM connects to hub or external drive/device that has a micro B receptacle
  - Host connects to the EVM acting as a device
- Standard-A plug to Micro-B plug
  - Host connects to the EVM acting as a device

Option 1

Use a USB3.0 micro-A to standard-B and USB3.0 Hub as the SIIG one as shown below.

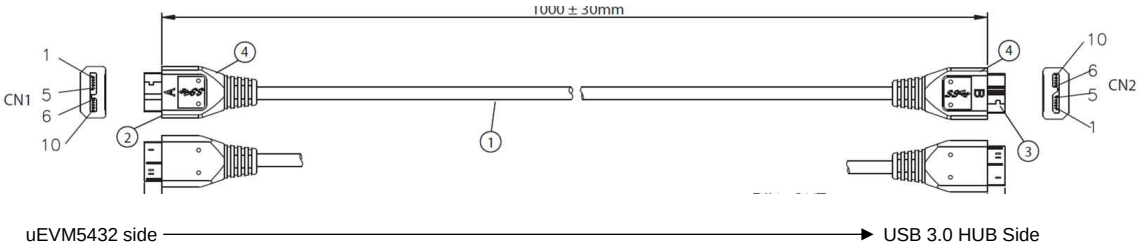


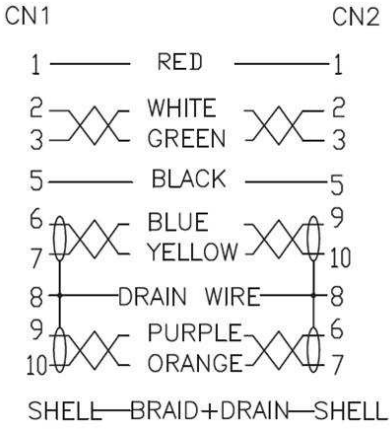
WIRING:

P1	COLOR	P2
1	RED	1
2	WHITE	2
3	GREEN	3
5	BLACK	4
6	BLUE	8
7	YELLOW	9
8	DRAIN WIRE	7
9	PURPLE	5
10	ORANGE	6
SHIELD	BRAID	SHIELD

Option 2

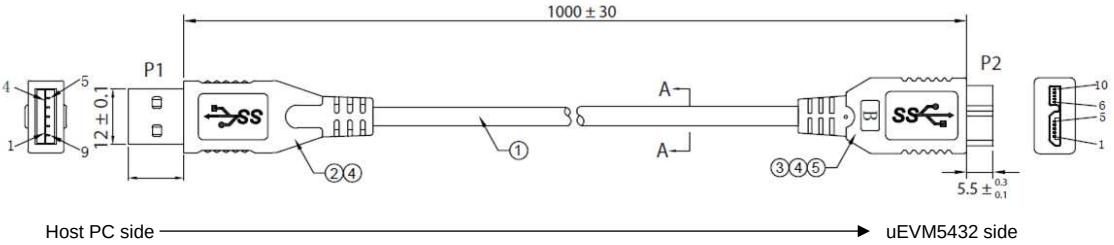
Use a USB3.0 micro-A to micro-B and USB3.0 Hub as the IOGEAR one as shown below.

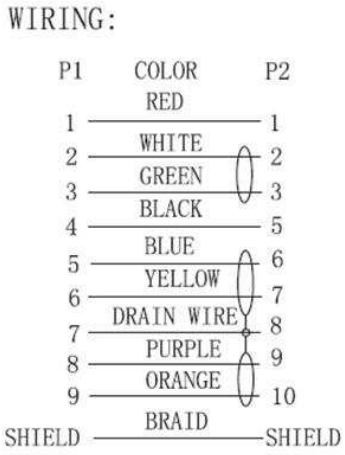




Option 3

Use a USB3.0 micro-B to standard-A. Host PC connects to the EVM acting as a device.





7 References

- *DRA76xP_DRA77xP_TDA2Px_ACD CPU Board PCB Rev C*
- *DRA76xP_DRA77xP_TDA2Px_ACD CPU Board Schematic Rev C*
- *DRA76xP_DRA77xP_TDA2Px_ACD CPU Board BOM Rev C*
- *DRA76xP_DRA77xP_TDA2Px_ACD CPU Board Assembly Drawing Rev C*
- *DRA76xP_DRA77xP_TDA2Px_ACD CPU Board PCB Drawing Rev C*
- *DRA76xP_DRA77xP_TDA2Px_ACD HDMI DISPLAY ADAPTER Board PCB Rev B*
- *DRA76xP_DRA77xP_TDA2Px_ACD HDMI DISPLAY ADAPTER Board Schematic Rev B*
- *DRA76xP_DRA77xP_TDA2Px_ACD HDMI DISPLAY ADAPTER Board BOM Rev B*
- *DRA76xP_DRA77xP_TDA2Px_ACD HDMI DISPLAY ADAPTER Board Assembly Drawing Rev B*
- *DRA76xP_DRA77xP_TDA2Px_ACD HDMI DISPLAY ADAPTER Board PCB Drawing Rev B*

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