DRA71x EVM CPU board

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Trademarks

1 Introduction

The DRA71x evaluation module (EVM) is an evaluation platform designed to speed up development efforts and reduce time-to-market for applications such as infotainment, reconfigurable digital cluster, or integrated digital cockpit. To allow scalability and reuse across DRA71x Jacinto Infotainment SoCs, the EVM is based on the Jacinto 6 Entry DRA718 SoC, which incorporates a heterogeneous, scalable architecture that includes a mixture of the following:

- ARM® Cortex®-A15 core
- Two ARM Cortex®-M4 processing subsystems
- C66x digital signal processor (DSP)
- 2D- and 3D-graphics processing units including the POWERVR™ SGX544 from Imagination Technologies
- High-definition image and video accelerator

The EVM also integrates a host of peripherals including multicamera interfaces (both parallel and serial) for LVDS-based surround view systems, displays, CAN, and Gigabit Ethernet audio video bridging (AVB).

The main CPU board integrates these key peripherals such as Ethernet or high-definition multimedia interface (HDMI®), while the infotainment application daughter board (JAMR3) and LCD/TS daughter board will complement the CPU board to deliver complete system to jump start your evaluation and application development.

2 Overview

An EVM system is comprised of a CPU board with one or more application boards. The CPU board (see Figure 1) can be used as a stand-alone for software debug and development. Each EVM system is designed to let customers evaluate the processor performance and flexibility in the following targeted markets:

- Automotive, radio sound processor (RSP), display audio, gateway, and infotainment applications
- Automotive, ADAS applications

The CPU board contains the DRA71x, DRA79x, TDA2Ex-17, and AM570x (superset part) applications processor, a companion power solution (LP8733 and LP8732), DDR3 DRAM, several types of flash memories (QSPI, eMMC, NAND, and NOR), and interface ports and expansion connectors. The board provides additional support components that provide software debugging, signal routing, and configuration controls that are not needed in a final product. Different versions of the CPU boards will be built to support the development process that includes the following:

- Socketed processor for wakeup, early software development, and quick and easy chip revision evaluation
- Soldered-down processor for high-performance use cases and evaluations

All other onboard components are soldered-down.

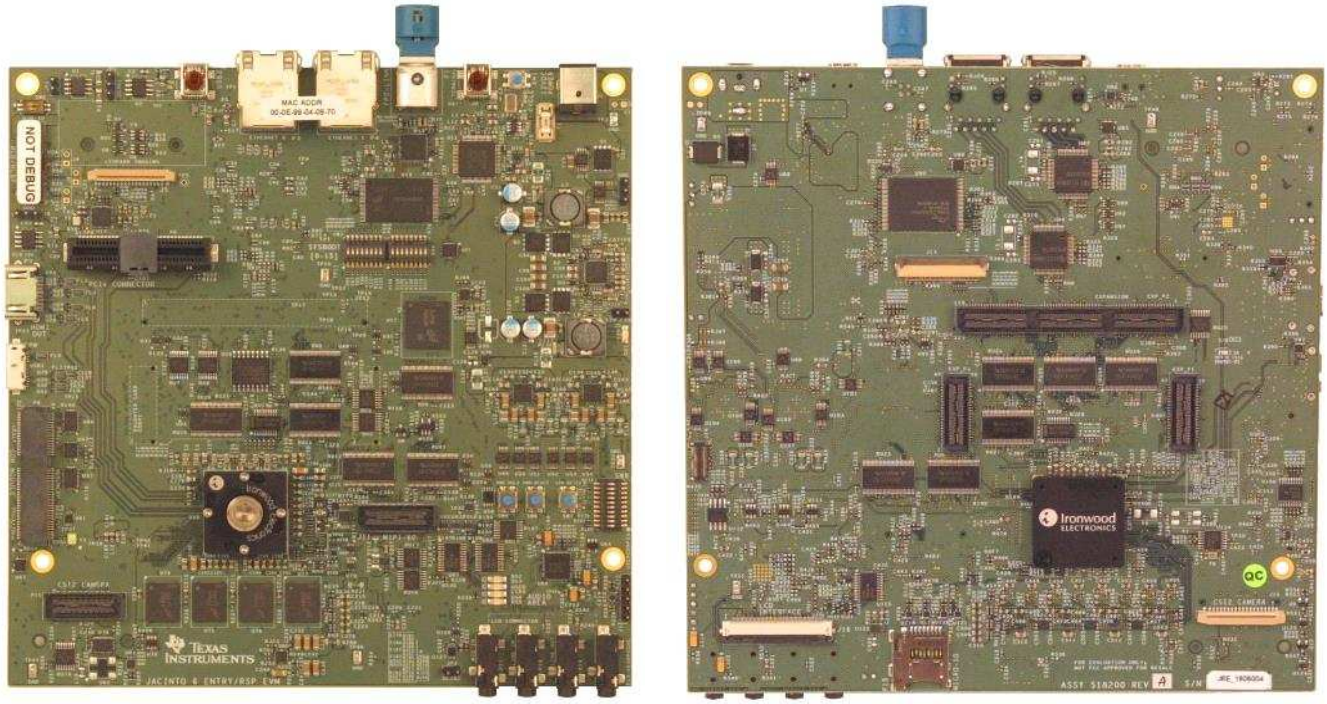


Figure 1. DRA71x, DRA79x, TDA2Ex-17, and AM570x CPU Board (Front and Back Views)

2.1 EVM System Configurations

Table 1 lists the SoC EVMs and kits.

Table 1. SoC EVMs and Kits

Systems	Description	Model Number
DRA71x, DRA79x, TDA2E-17, and AM570x socketed CPU board (GP)	Socketed - CPU board ES2.0 GP (CPU board)	EVMX777BG-01-00-S0
DRA71x, DRA79x, TDA2Ex-17, and AM570x CPU board (GP)	Soldered - CPU board ES2.0 GP (CPU board)	EVMX777BG-01-00-00
DRA71x, DRA79x, TDA2Ex-17, and AM570x CPU board (HS)	Soldered - CPU board ES2.0 HS (CPU board)	EVMX777BH-01-00-00
DRA71x and DRA79x Infotainment EVM kit	Soldered - CPU board ES2.0 GP (CPU board) with: • JAMR3 Tuner Apps board • 10.1-inch, 1280 × 800 LCD/TS board	EVMX777G-01-20-00
TDA2Ex-17 Vision EVM kit	Soldered - CPU board ES2.0 GP (CPU board): with Vision Apps board	EVMX777G-01-40-00
DRA71x, DRA79x, TDA2Ex-17, and AM570x CPU EVM kit	Soldered - CPU board ES2.0 GP (CPU board): with 10.1-inch, 1280 × 800 LCD/TS board	EVMX777G-01-00-00

Table 2 lists the EVM accessories

Table 2. EVM Accessories

Accessories	Description	Model Number
JAMR3 Tuner Application Board	Head-unit DIN form-factor Application Board with radio tuners, multiple audio I/Os, and video input extendibility	EVM5777JAMR3-V1-0
Vision Application Board	Support for multiple camera inputs for surround view, stereo vision, and proprietary camera board interfaces	EVMX777VISION-V2-0
10.1-inch, 1280 × 800, Display/Multitouch Touchscreen	10.1-inch, 1280 × 800, LCD (24-bit color), with Multitouch Touchscreen	EVMX777LCDTS-V1-0

Table 3 lists the EVM kit truth table.

Table 3. EVM Kit Truth Table

EVM or Kit Name	CPU Board	JAMR3 App Board	Vision App Board	LCD/TS Daughter Board	Power Supply Adapter (2.1 to 2.5 mm)
DRA71x, DRA79x, TDA2E-17, AM570x Socketed CPU board (GP)	X				X
DRA71x, DRA79x, TDA2E-17, AM570x CPU board (GP)	X				X
DRA71x, DRA79x, TDA2E-17, AM570x CPU board (HS)	X				X
DRA71x and DRA79x Infotainment EVM kit	X	X		X	X
TDA2E-17 Vision EVM kit	X		X		X
DRA71x, DRA79x, TDA2E-17, and AM570x EVM kit	X			X	

2.2 CPU Board Feature List

- Processor
  - DRA71x, DRA79x, TDA2E-17, and AM570x (superset SoC) (17-mm × 17-mm package, 0.65-mm pitch, with 25 × 25 via-channel array)
  - Support for corresponding socket
- Power supply
  - 12-V DC input
  - Optimized power management solution
  - Compliant with SoC power sequencing requirements
  - Integrated power measurement
- PCB
  - Dimension (W × D) 170 mm × 170 mm
  - 100% PTH technology
- Memory
  - DRAM (DDR3L-1333 with ECC):
    - 2GB (four 4Gb × 8 + one 4Gb × 8 ECC)
  - Quad SPI flash: 256Mb
  - EMMC flash: 8Gb (v.4.51 compliant)
  - NAND flash: 2Gb
  - NOR flash: 512Mb
  - I^2C EEPROM, 32Kb
  - MicroSD card cage
- Boot mode selection DIP switch
- Digital temperature sensor (TMP102)
- JTAG/Emulator:
  - 60-pin MIPI™-60 JTAG/Trace connector
  - Adapter for 20-pin CTI header: 10 × 2, 1.27-mm pitch
- Supported interfaces and peripherals:
  - CAN Interface – 2-wire PHY on DCAN1
  - Two USB host receptacles – one USB 3.0 (micro-USB) and one USB 2.0 (mini-USB)
  - Audio codec (AIC3106) with headphone out, line out, line in, and microphone in
  - Three Video outputs (HDMI, FPD-Link III, LCD)
  - Camera sensors support using the Leopard Imaging Module interface
  - PCIe
  - MLB and MLBP on the MICTOR connector
  - RS-232 using the USB FTDI converter (mini-A/B USB)
  - COM8 module interface for *Bluetooth*® and WLAN support
  - Two RJ45 Gigabit Ethernet (DP83867)
  - I^2C GPIO expander
- Expansion connectors to support application-specific boards.

2.3 CPU Board Component Identification

Figure 2 shows the front of the board and Figure 3 shows the back.

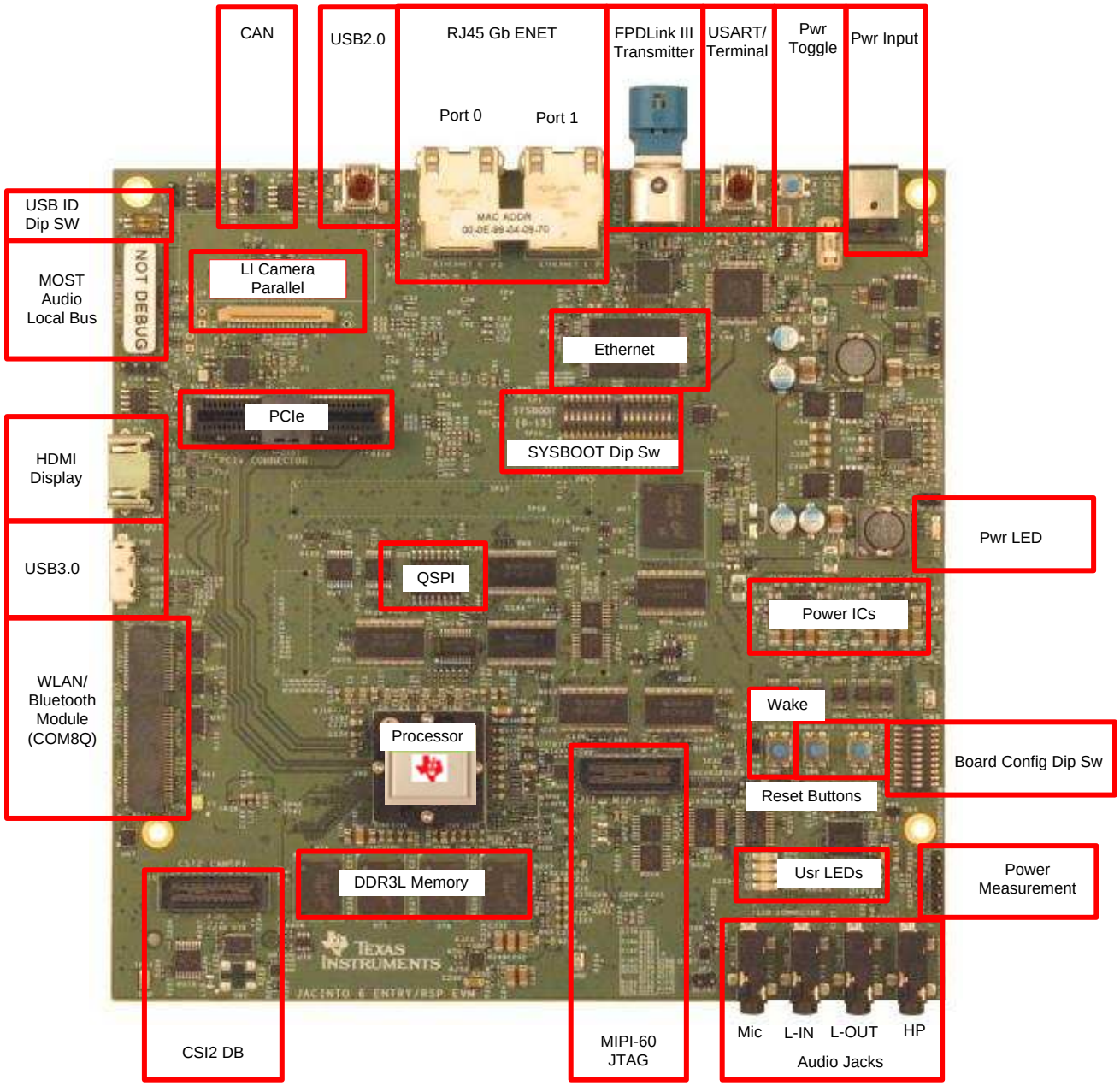


Figure 2. CPU Board – Front

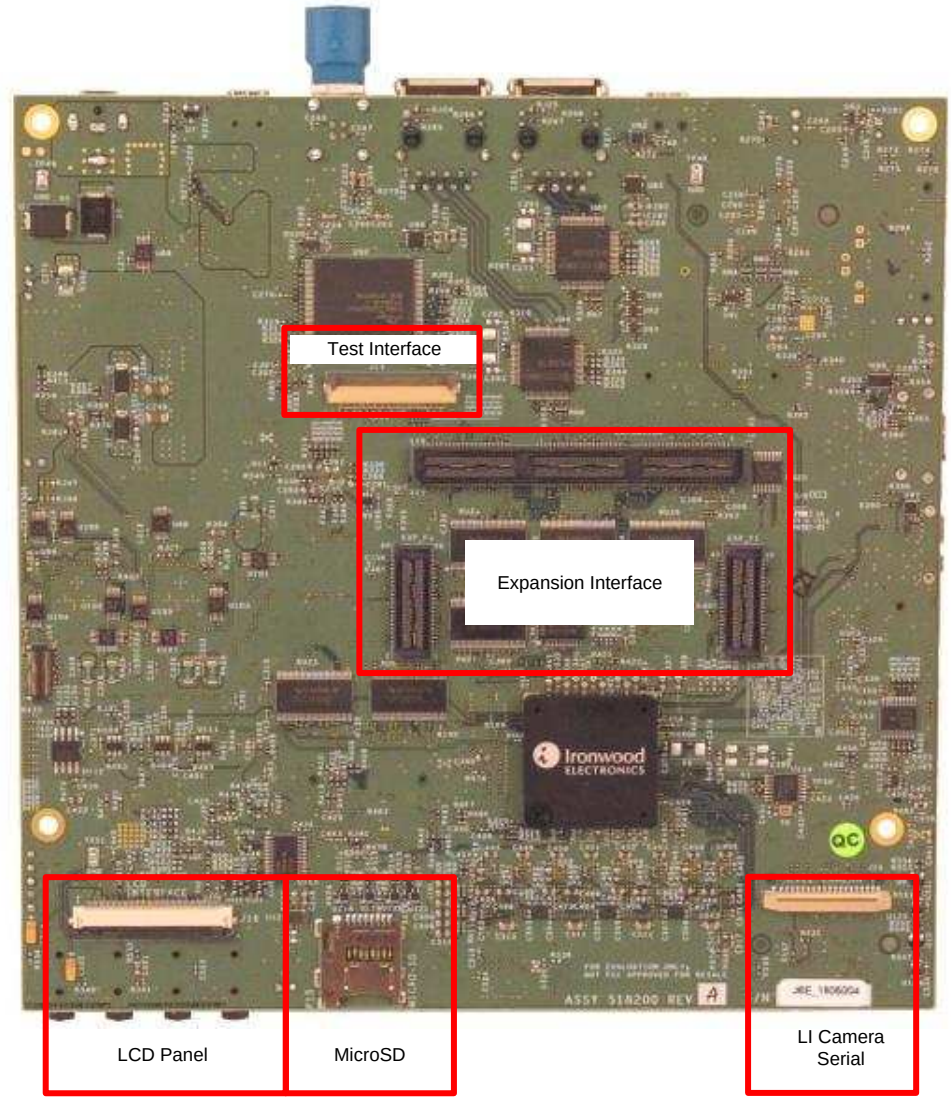


Figure 3. CPU Board – Back

3 Hardware

3.1 Hardware Architecture

Figure 4 shows the functional block diagram of the CPU board.

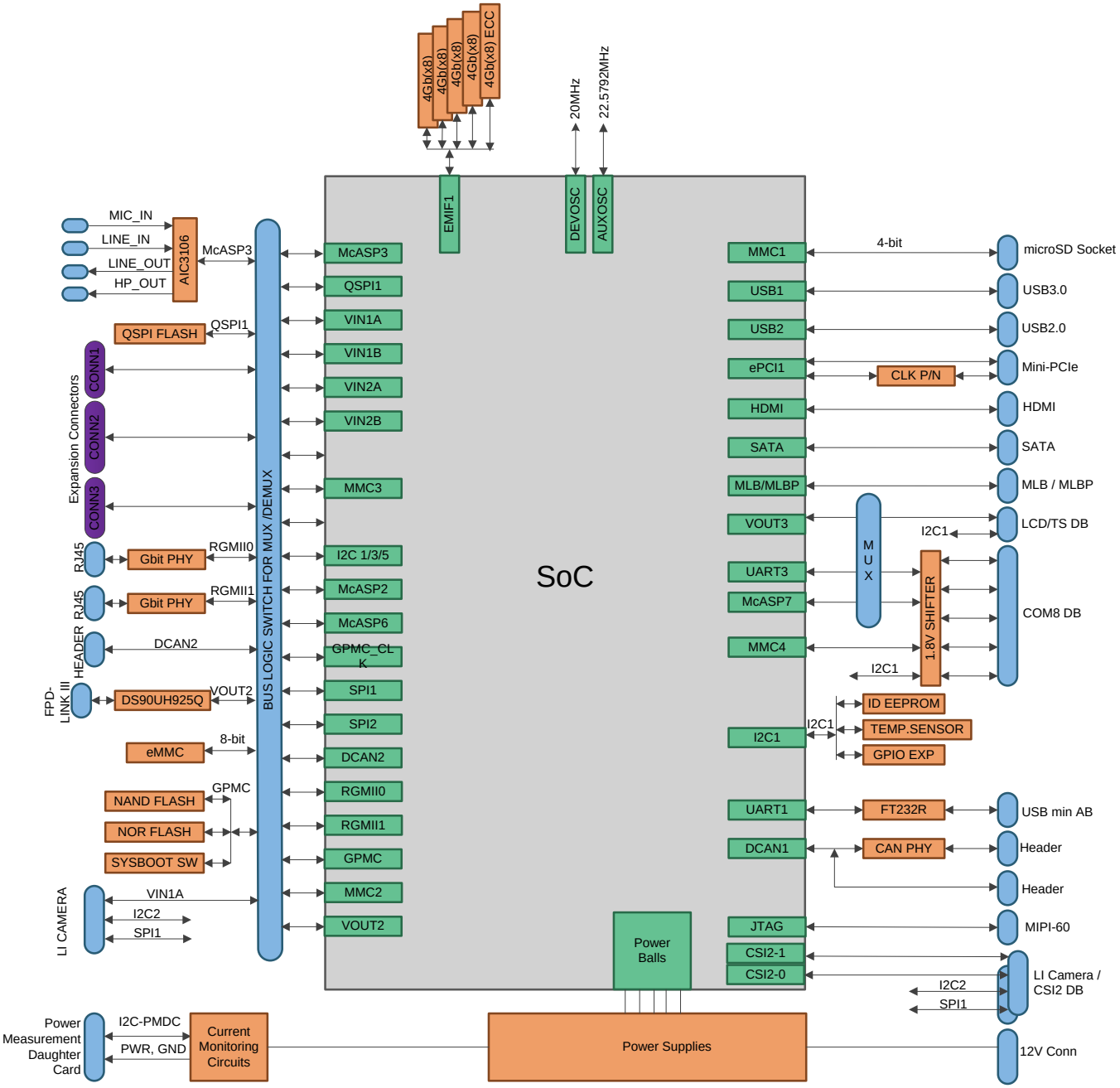


Figure 4. CPU Board Block Diagram

3.2 DRA71x, DRA79x, TDA2E-17, and AM570x Processor

The processor is a highly integrated, programmable, SoC, silicon solution. Figure 5 shows the SoC block diagram.

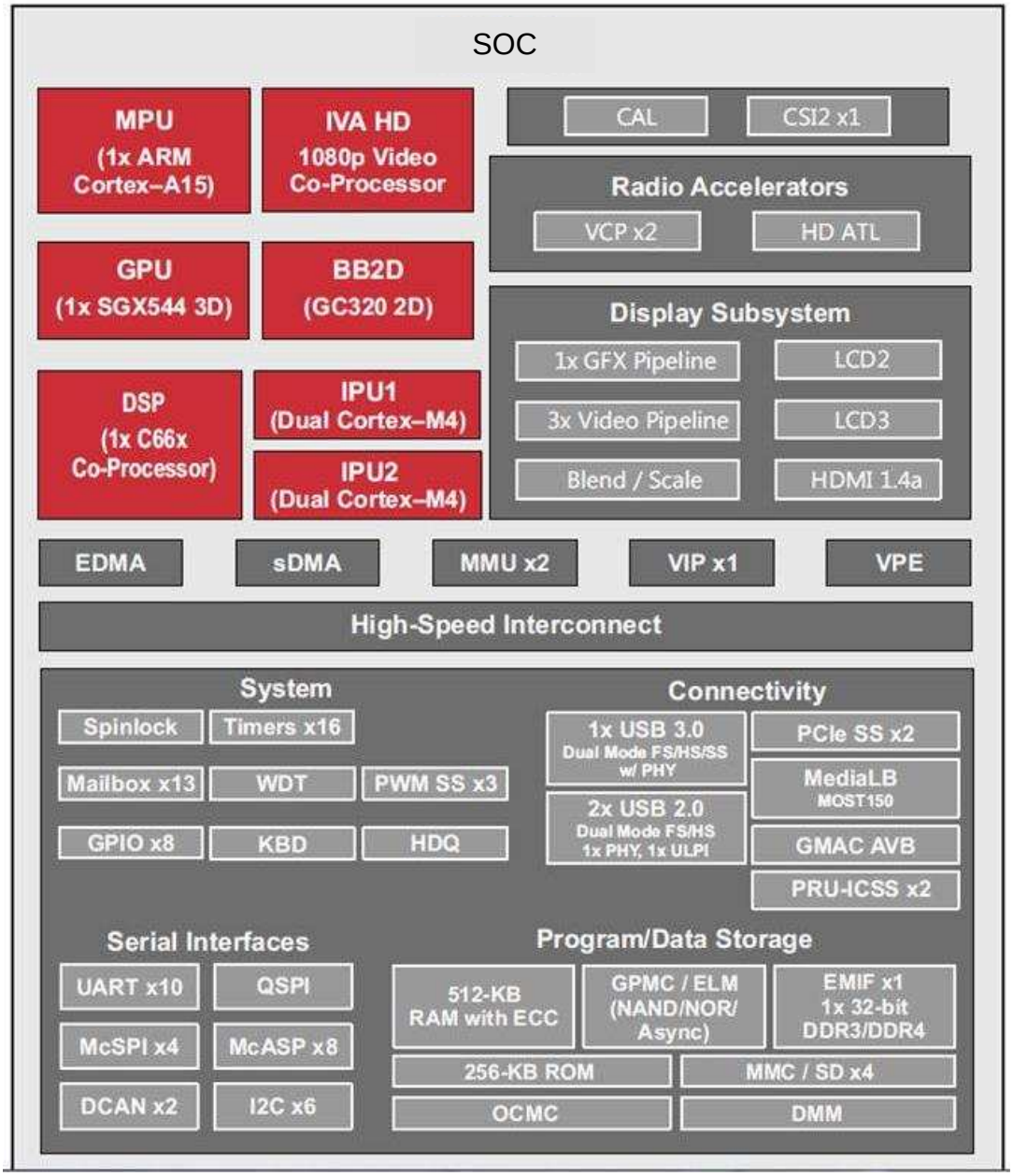


Figure 5. SoC Block Diagram

3.3 Power Architecture

Figure 6 shows the power distribution system of the EVM. The power-management solution is created from four total devices (see Figure 6). A step-down 12 V to 3.3 V, 5-V converter provides the primary 3v3 and 5v0 power rails for the rest of the system. The LP8733 and LP8732 devices are optimized for the SoC power needs and sequence requirements. A sink/source regulator provides the DDR termination.

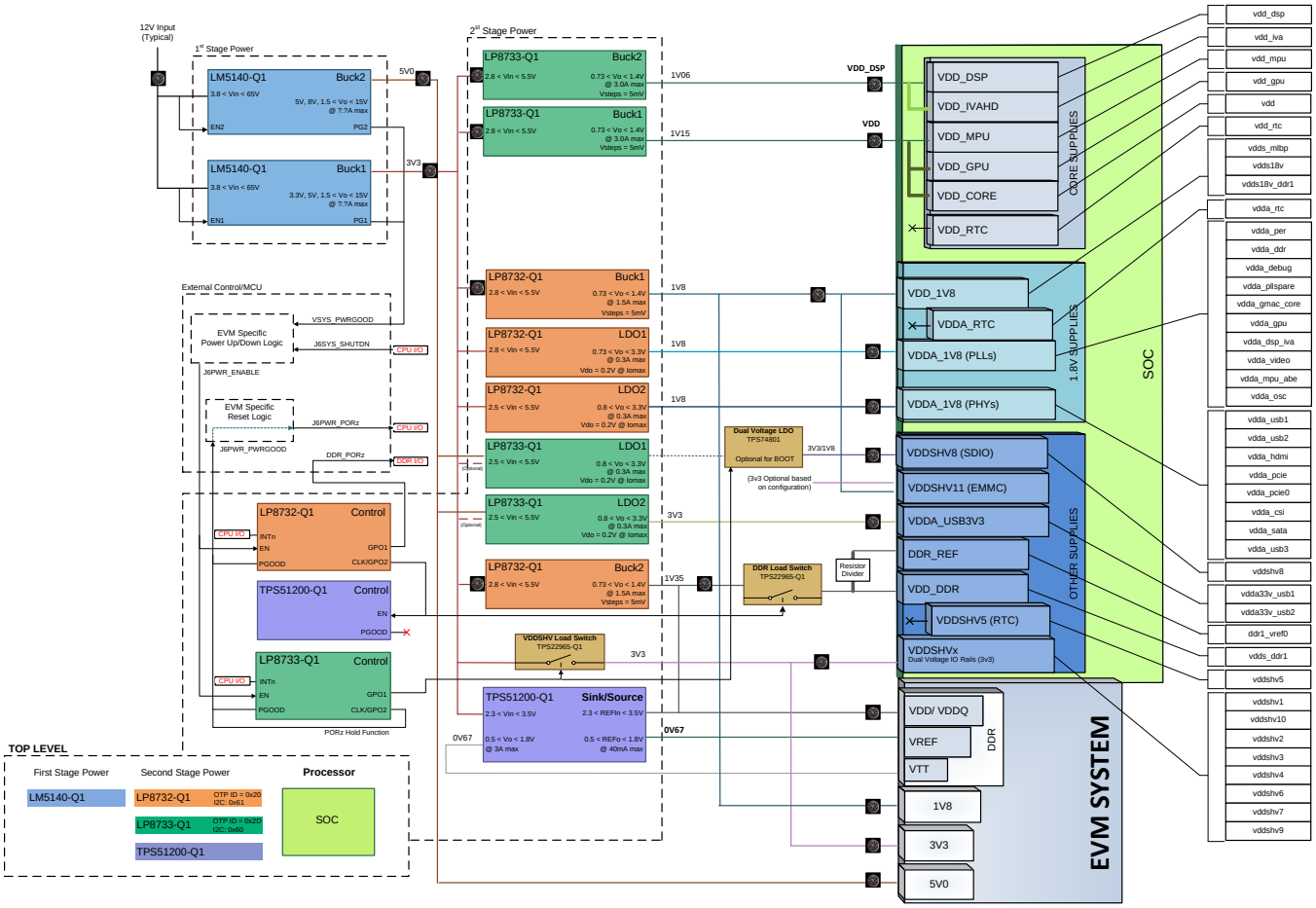


Figure 6. Power Distribution Block Diagram

An external power supply is required to power the EVM, but is not included as part of the EVM kit. The external power supply requirements follow:

- Power jack: 2.5-mm ID, 5.5-mm OD
- Nom voltage: 12 VDC
- Maximum current: 5000 mA
- Efficiency level V

External power supply regulatory compliance certifications: recommended selection and use of an external power supply which meets TI's minimum electrical ratings requirement and complies with applicable regional product regulatory and safety certification requirements, such as UL, CSA, VDE, CCC, and PSE.

Table 4 lists the recommended and tested power supplies that can be used with the EVM.

Table 4. 12 V, 5A, 65W Compatible Wall Supplies

Digi-Key Part Number	Manufacturer Part Number	Manufacturer	Output Connector	Notes
102-3417-ND	SDI65--12-U-P5	CUI Inc.	Barrel plug, 2.1 mm x 5.5 mm O.D. x 9.5 mm	Required adapter, provided in the EVM kits
62-1221-ND	KTPS65-1250DT-3P-VI-C-P1	Volgen America/Kaga Electronics USA	Barrel plug, 2.1 mm x 5.5 mm O.D. x 9.5 mm	Required adapter, provided in the EVM kits
102-3419-ND	SDI65-12-UD-P6	CUI Inc.	Barrel plug, 2.1 mm x 5.5 mm O.D. x 9.5 mm	Required adapter, provided in the EVM kits
SDI65-12-U-P6-ND	SDI65-12-U-P6	CUI Inc.	Barrel plug, 2.1 mm x 5.5 mm O.D. x 9.5 mm	
SDI65-12-UD-P6-ND	SDI65-12-UD-P6	CUI Inc.	Barrel plug, 2.1 mm x 5.5 mm O.D. x 9.5 mm	

3.4 Reset Structure

Figure 7 shows the reset structure. The power-on reset timing is primarily controlled from the system power ICs (LP8733 and LP8732). Two push-buttons are provided for user-controlled resets. One button is the power on reset (SW4) for a complete SoC reset. The other button is for a warm reset (SW5). The warm reset can also be sourced from the MIPI-60 JTAG/Trace connector.

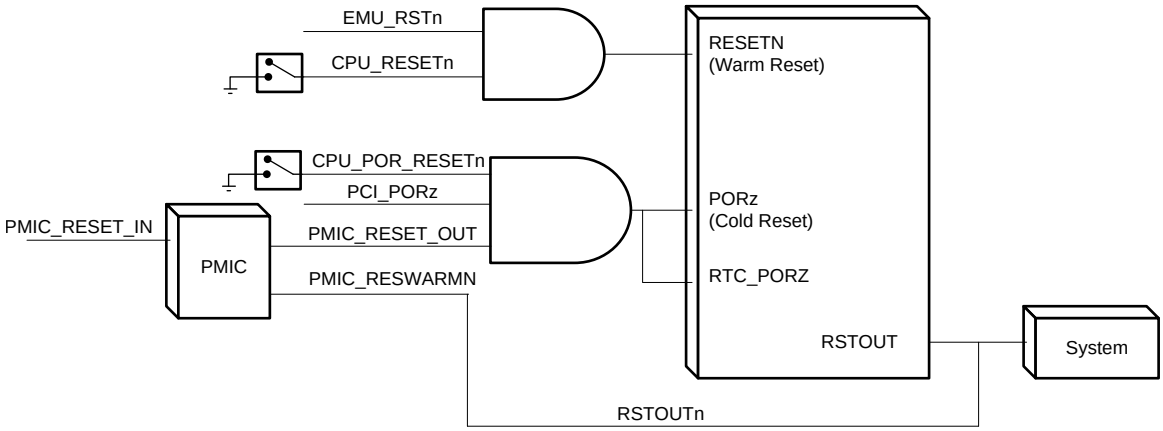


Figure 7. Reset Structure

Table 5 summarizes the reset signals.

Table 5. Reset Signals Structure

Reset Type	Reset Signal Sources	Comments
Power-On Reset (PORn) (as whole system reset)	CPU_POR_RESETn	PORn reset push-button
	PCI_PORz	PCIe inbound reset
	PMIC_RESET_OUT	Power on reset from power ICs
Warm Reset	CPU_RESETn	Warm reset push-button
	EMU_RSTn	Reset from Emulator
PMIC Power-On Reset	PMIC_RESET_IN	PMIC reset input
Processor Reset Out	RSTOUTn	Reset output from processor to system, PMIC (warm reset input)

3.5 Clocks

The SoC supports up to two primary clock inputs. The device clock (OSC0) is sourced with a 20-MHz clock. The auxiliary clock (OSC1) is sourced with a 22.5792-MHz clock. Both clocks are sourced from a clock synthesizer (CDC925).

In addition to the SoC clock inputs, the EVM includes other clock sources. A 25-MHz clock is provided to Ethernet PHY(s) and a 100-MHz clock is sourced for miniPCIe. Both the SoC and Ethernet clocks are sourced from a clock synthesizer (CDC925).

3.6 Memory

3.6.1 SDRAM Memory

The EVM includes 2GB of DDR3L memory, and can operate at clock speeds up to 667 MHz (DDR3-1333). The memory is configured with four 4-Gb devices (x8b devices). ECC is supported.

- DDR3L device used: Micron® MT41K512M8RH-125-AA:E (4× 8b at 4Gb/each) (or equivalent)
- EEC device used: Micron MT41K512M8RH-125-AA:E (1× 8b at 4Gb) (or equivalent)

The DDR3L power is generated from the SoC power solution, and set to 1.35 V. It uses *fly-by* topology with VTT termination. VTT supply is generated using a sink/source termination regulator (TPS51200).

3.6.2 QSPI Flash Memory

As a primary nonvolatile boot device, the EVM includes 256Mb of Quad-SPI flash memory. The device is supported on CS0 of the QSPI interface. The interface can be configured to support either serial mode (1×) or quad mode (4×).

- QSPI device used: Spansion™ S25FL256S

Booting from the QSPI flash memory is supported on the EVM. No EVM configuration is required because the QSPI flash is enabled by default. Ensure the correct SoC boot mode is set using the SYS_BOOT switches (SW3 and SW4).

3.6.3 EMMC Flash Memory

As a primary nonvolatile storage device, the EVM includes 8GB of EMMC flash memory. The memory device is EMMC v4.51 compliant, and connects to the MMC2 port of the SoC. The design can supports rates up to HS-200.

- EMMC device used: Micron MTFC8GLWDM-3M AIT Z

Booting from the EMMC flash memory is supported on the EVM. The onboard MUX must be able to enable EMMC by setting SW8.p3 to on. Ensure the correct SoC boot mode is set using the SYS_BOOT switches (SW3 and SW4).

3.6.4 MicroSD Card Cage

For nonvolatile storage expansion, the EVM includes a microSD card cage. The cage is connected to the MMC1 port of the SoC. To support higher-speed cards that operate at lower voltages, the I/O supplies are changed from 3v3 to 1v8 by setting GPIO7_11 to low. The SD card power can be cycled using I/O expander (EXP2 and PP5). See the data manual for the SoC for specific information regarding supported card types, densities, and speeds.

Booting from the microSD card cage is supported on the EVM. No EVM configuration is required as the QSPI flash is enabled by default. Ensure the correct SoC boot mode is set using the SYS_BOOT switches (SW3 and SW4).

3.6.5 GPMC NOR Flash Memory

A 512Mb NOR flash memory (x16) is supported as a nonvolatile memory option on the EVM. The device is supported on CS0, and therefore can also be used as a boot device. Booting from the NOR flash memory is supported on the EVM. The onboard MUX must be able to enable the memory by setting SW8.p2 to on. Ensure the correct SoC boot mode is set using the SYS_BOOT switches (SW3 and SW4).

- NOR device used: Spansion S29GL512S10TFI010

3.6.6 GPMC NAND Flash Memory

A 2Gb NAND flash memory (x16) is supported as a nonvolatile memory option on the EVM. The device is supported on CS0, and therefore can also be used as a boot device. Booting from the NAND flash memory is supported on the EVM. The onboard MUX must be able to enable the memory by setting SW8.p1 to on. Ensure the correct SoC boot mode is set using the SYS_BOOT switches (SW3 and SW4).

- NAND device used: Micron MT29F2G16AADWP:D

3.6.7 Boot Modes

The SoC supports a variety of different boot modes, which is determined by the 16-bit system boot setting present on the shared specific I/O balls during power-on sequence (see the TRM for details). Boot mode selection is accomplished by the setting of DIP switches SW3 and SW4, as shown in Table 6, before cycling power.

These SoC resources can be redeployed through both SoC pin EVM MUX settings to support alternate interfaces after boot-up.

Table 6. SoC Boot Mode Switch Settings

SoC Interface (Internal System Boot Input)	CPU Board Net	DIP Switch Reference Designator Position Number Connections	Factory Setting
GPMC_AD0 (sysboot0)	GPMC_D00	SW3.P1	On
GPMC_AD1 (sysboot1)	GPMC_D01	SW3.P2	Off
GPMC_AD2 (sysboot2)	GPMC_D02	SW3.P3	On
GPMC_AD3 (sysboot3)	GPMC_D03	SW3.P4	Off
GPMC_AD4 (sysboot4)	GPMC_D04	SW3.P5	On
GPMC_AD5 (sysboot5)	GPMC_D05	SW3.P6	Off
GPMC_AD6 (sysboot6)	GPMC_D06	SW3.P7	Off
GPMC_AD7 (sysboot7)	GPMC_D07	SW3.P8	Off
GPMC_AD8 (sysboot8)	GPMC_D08	SW4.P1	On
GPMC_AD9 (sysboot9)	GPMC_D09	SW4.P2	Off
GPMC_AD10 (sysboot10)	GPMC_D10	SW4.P3	Off
GPMC_AD11 (sysboot11)	GPMC_D11	SW4.P4	Off
GPMC_AD12 (sysboot12)	GPMC_D12	SW4.P5	Off
GPMC_AD13 (sysboot13)	GPMC_D13	SW4.P6	Off
GPMC_AD14 (sysboot14)	GPMC_D14	SW4.P7	Off

Table 6. SoC Boot Mode Switch Settings (continued)

SoC Interface (Internal System Boot Input)	CPU Board Net	DIP Switch Reference Designator Position Number Connections	Factory Setting
GPMC_AD15 (sysboot15)	GPMC_D15	SW4.P8	On

In addition to SoC boot settings, EVM resources must also be set for the desired boot interface. Table 7 lists the boot interfaces that require selection. DIP switch SW8 is used to configure the various boot memories.

Table 7. Board Controls for Memory Booting Options

Signals	Description	DIP Switch	Factory Setting
NAND_BOOTn(1)	On: Enable GPMC_nCS0 for NAND flash boot	SW8.1	Off
NOR_BOOTn(1)	On: Enable GPMC_nCS0 for NOR flash boot	SW8.2	Off
MMC2_BOOT	On: Enable MMC2 Interface for eMMC flash boot	SW8.3	Off
Not Used	Not Used	SW8.4	Off
SW_VPP_EN	On: Enable V_{PP} supply to SOC (also requires I/O expander bit to be set)	SW8.5	Off
MCASP1_ENn	Low: Enable COMx signal paths	SW8.6	Off
NOR_ALT_ADDRn	Off: Selects default pin location for GPMC ADDR On: Selects alternate/new pin locations for GPMC	SW8.7	Off
PCI_RESET_SEL	High: PCIe device may reset SoC. Low: SoC may reset the PCIe device.	SW8.8	Off
GPMC_WPN	Low: Enable write protection of NAND flash	SW5.9	Off
I2C_EEPROM_WP	High: Enable write protection of board identification EEPROM	SW5.10	Off

(1) Routing control for GPMC_nCS0 is shared between the NOR and NAND flash memories. Ensure that only one DIP switch, SW8.P1 or SW8.P2, is ever set to the on state at any time so that GMPC_nCS0 is connected to only one memory. Failure to adhere to this requirement causes NOR and NAND memory data bus contention

3.6.8 JTAG/Emulator and Trace

The JTAG emulation interface is supported through the MIPI 60-pin interfaces. The EVM kit includes an adapters for supporting other JTAG interfaces, including the 20-pin cJTAG interface from TI. Reset (warm reset) using the emulator is supported.

Debug/Trace is also supported through the MIPI 60-pin connector. The EVM supports up to 20 trace bits. At the SoC and EVM level, the trace pins are muxed with VIN2A and VOUT2 functions. Therefore, these interfaces cannot be used simultaneously.

3.6.9 UART Terminal

The EVM supports a dual UART connection to be used for the user terminal. A FT2232 device transports the UART information over USB to a host PC. The EVM is designed to use UART1 of the SoC as the primary terminal connection, and is connected to port A of the USART transceiver. The USB-side of the FT2232 device is powered from the USB port, and the connection stays active regardless of the power state of the EVM. The green LED (D1) indicates that the USB connection is available.

- USART device to be used: FTD Chip FT232RQ

A USB cable (mini-B to type A) connects the EVM to a PC, and is included as part of the EVM kit.

The EVM can support a second UART connection to the FT2232 device, intended for booting. However, this configuration requires board modifications, and is recommended only for specific users.

3.6.10 DCAN and CAN Interfaces

The EVM supports access to two DCAN interfaces though pin headers. The device supports a single, 3-pin, CAN interface, connecting DCAN1 through a CAN transceiver.

- CAN device used: Texas Instruments SN65HVDA541

3.6.11 Universal Serial Bus (USB)

Two independent USB ports are supported on the EVM. USB 3.0 Super-Speed bus (USB1) is supported using port USB1 to a mini-AB type connector. This interface supports rates up to 5 GB/s. USB2.0 interface is supported using port USB2 to a micro-AB type connector. It can supports rates up to 480 MB/s. Both ports can operate in either host or device mode. VBUS can be supplied to the peripheral when in host mode by enabling the VBUS switch (controlled through the SoC). However, the EVM cannot be powered from VBUS when operating in device mode.

The EVM includes capabilities to set and read each ID pin of the connectors. This feature is supported using the I/O expander (EXP2 P1 for USB1 and P2 for USB2). In addition, the DIP switch SW2 provides the ability to manually set the individual ID value either high (off) or low (on).

3.6.12 Wired Ethernet

Dual Gigabit Ethernet ports are supported on the EVM. RGMII ports 0 and 1 drive the TI DP83867 Gigabit PHYs. The PHYs are configured through the management data input/output bus (MDIO), with address set to 0x2 (port 0) and 0x3 (port 1). PHYs are reset at power on, but can also be independently reset using the I/O expander. Both ports share a common interrupt signal (GPIO6_16).

- I/O Expander Control: EXP1, P10 (PHY 0 Reset), P11 (PHY 1 Reset)

NOTE: For PHY configuration, users must configure the RGMII Control register (RGMIICTL) of the DP83867 for RGMII mode, and configure the RGMII Delay Control register (RGMIIDCTL) for a 0-ns TX delay and 2.25-ns RX delay. Set the I/O Drive Strength register (IO_IMPEDANCE_CTRL) to maximum drive.

3.6.13 Video Output

The EVM supports three different options for supporting video output – HDMI display, LCD touch panel, and FPD-Link III. Each option can be supported independently or all can be used simultaneously.

3.6.13.1 HDMI Display

The SoC includes a dedicated HDMI display, which is supported with a type A-HDMI connector. The interface supports 1080p with 24b color. A communication channel (DDC/CEC) is provided to the HDMI connector for communication with the HDMI panel. A monitor detect indication is also provided. The DDC/CED interface and monitor detect signals (HPD) are translated through the transceiver, and can be controlled using I/O from the expander.

- DDC Transceiver used: Texas Instruments TPD12S016
- I/O Expander Control: EXP3, P4 (level shift reg enable, HPD), and P5 (DDC/CEC enable)

3.6.13.2 LCD Touch Panel

The EVM supports an LCD panel interface for providing video output to an LCD panel. The SoC VOUT3 resource is used drive up to 24 bits of RGB data to the interface. The interface supports resource connections for interfacing with a touch panel for advanced user interfaces. These resources include a control bus (I2C1) and interrupt for touch indications (GPIOx). An LCD panel is not included with the CPU EVM, but can be ordered and included as part of an assembly kit.

- Connector used: Molex®

3.6.13.3 FPD-Link III Output/Panel

The EVM includes an FPD-Link III parallel to the serial interface on VOUT2. The device supports up to 24 bits of data and can operate at pixel rates up to 85 MHz. The interrupt is supported to enable back-channel communication, typically needed if supporting a touch screen. The transceiver is configured using I^2C (port 5, 0x1B).

- Serializer device used: Texas Instruments DS90UH925Q
- Connector used: Automotive HSD, right-angle plug for PCB, Rosenberger D4S20D-40ML5-Z

3.6.14 Video Input

3.6.14.1 Parallel Imaging

Parallel video input is supported through connections from external sensors and transceivers. The SoC port VIN2A is routed to the connector interface and designed to mate with camera sensors from Leopard Imaging. This approach provides flexibility for customers to select from a variety of available modules, while also supporting connections of custom solutions. The attached module can be configured using either I^2C (port 5) or SPI (port 1).

- Connector used: FPC 36 position, 0.5 mm, Molex 052559-3679.

3.6.14.2 Serial Imaging

Serial video input is supported through connections from external sensors and transceivers. The SoC port CSI2-0 is routed to the connector interface and designed to mate with camera sensors from Leopard Imaging. This approach provides flexibility for customers to select from a variety of available modules. Both serial ports (CSI2-0 and CSI2-1) are routed to an expansion connector for supporting a variety of custom solutions. Both interfaces support additional signals for control and configuration of the attached modules. These interfaces (I^2C port 5 and SPI port 1) are translated to 1.8-V I/O (with resistor option to leave at 3.3-V I/O).

- LI Connector used: FPC 36 position, 0.5 mm, Molex 052559-3679
- Connector used: Samtec™ QSH-020-01-L-D-DP-A

3.6.15 Mini-PCIe

The EVM supports a mini-PCIe (single lane) interface for connecting with a variety of external modules. An onboard clock generator, CDCM9102, provides the 100-MHz reference clock to both the SoC and attached modules. The EVM supports two different PCIe reset configurations; select one using the DIP switch SW8 position 8. The default setting of on provides the SoC the ability to reset the PCIe peripheral. The switch setting of off provides the PCIe peripheral the ability to reset the SoC.

3.6.16 Media Local Bus (MLB)

The EVM supports an MLB interface for connecting to external hardware (such as the SMSC OS81110/2+0 Physical Interface Board). The interface supports both 3-pin MediaLB and 6-pin MediaLB+ configurations.

- Connector used: Samtec QSH-020-01-L-D-DP-A

3.6.17 Audio

The EVM supports onboard AIC3106 audio codec for analog audio conversions. Analog inputs are supported on two 3.5-mm audio jacks, including stereo line inputs (P12) and mono microphone (P11). Analog outputs are supported on two 3.5-mm audio jacks, providing stereo line outputs (P13) and stereo headset (P14). The digital audio is connected to the SoC using the multichannel serial port (McASP3). The codec requires a master clock (AHCLKX). The audio codec is configured using I2C1, and is accessed at address 0x19.

3.6.18 COM8 Module Interface

A connector is provided to facilitate plugging in of the TI COM8Q modules, which provide features such as Bluetooth and Wi-Fi®. The COM8Q interface requires a 3.6-V power supply, thus a dedicated regulator is provided. All signals on the COM8Q interface are required to 1.8 volts, therefore voltage translators are placed to convert from the standard I/O levels of 3.3 V.

- Connector used: Samtec MEC6-150-02-S-D-RA1

3.6.19 eFuse Programming Supply

The EVM provides enabling and disabling support for the eFUSE programming supply. As a protection, two separate steps are required to enable the programming supply. The DIP switch SW8.p5 must be set to on (default is off) and the I/O expander (EXP2 and P13) must be low by software (default is high).

3.6.20 User Interface LEDs

The CPU board has four user interface LEDs for debug, status indication, and so on. Table 8 lists details about the user interface LEDs and their controls.

Table 8. User LEDs

LED	Controlled By
DS2	I/O Expander EXP1, position P7
DS3	I/O Expander EXP1, position P6
DS4	I/O Expander EXP1, position P5
DS5	I/O Expander EXP1, position P4

3.6.21 Power Monitoring

The CPU board has provisions to monitor power for many of the systems core power rails. The measurement system is implemented using the INA226 I^2C current shunt and power monitors from TI. The INA226 device monitors both power supply voltage and shunt current measurements. Information is connected from the INA226 devices using dedicated I^2C buses. The INA226 devices can be controlled using off-board modules (FTDI USART, MSP430, or a similar device).

Table 9 lists a mapping of the current monitoring system. INA226 devices are at each shunt location.

Table 9. Power Monitor Mapping

I^2C Address	Power Net	Shunt/Resistor	Description
I^2C BUS A			
0x40	VPIN_S1_3V3	20 mΩ	LP8733 Buck0 power input (core)
0x41	VPIN_S2_3V3	20 mΩ	LP8733 Buck1 power input (DSP)
0x42	VPIN_S3_3V3	20 mΩ	LP8732 Buck0 power input (1V8)
0x43	VPIN_S4_3V3	20 mΩ	LP8732 Buck1 power input (DDR)
0x44	VDD_CORE_AVS	10 mΩ	CPU Core power rail
0x45	VDD_DSP_AVS	10 mΩ	CPU DSP power rail
0x46	VDDS_1V8	10 mΩ	CPU 1V8 power rails
0x47	VDD_DDR_1V35	10 mΩ	CPU DDR power rail
0x48	VDA_1V8_PLL	10 mΩ	CPU PLL power rails
0x49	VDA_1V8_PHY	10 mΩ	CPU PHY power rails
0x4A	VDDSHV8	10 mΩ	CPU I/O power rail for VDDSHV8
0x4B	VDDA_USB3V3	10 mΩ	CPU USB3V3 power rail
0x4C	VDDSHV_3V3	10 mΩ	CPU I/O power rail (except VDDSHV8)
I^2C BUS B			
0x40	EVM_12V	10 mΩ	Total system 12-V power rail

Table 9. Power Monitor Mapping (continued)

I²C Address	Power Net	Shunt/Resistor	Description
0x41	EVM_5V0	10 mΩ	Total system 5V0 power rail
0x42	VSYS_3V3	10 mΩ	Total system 3V3 power rail
0x43	VDD_DDR	10 mΩ	DDR memory power rail
0x44	EVM_1V8	10 mΩ	EVM 1V8 peripheral rail
0x45	EVM_3V3	10 mΩ	EVM 3V3 peripheral rail

3.6.22 I²C Peripheral Map

Table 10 lists the I²C interfaces available on the EVM, with a list of devices connected to each I²C interface and its corresponding device address.

Table 10. I²C Device Address Chart

CPU Board	Part No.	I2C1	I2C3	I2C4	I2C5	Device Address (7b)
EEPROM	24WC256	X				0x50
Digital Temperature Sensor	TMP102AIDRLT	X				0x48
GPIO Expander 1	PCF8575	X				0x20
GPIO Expander 2	PCF8575	X				0x21
GPIO Expander 3	PCF8575				X	0x26
MLB Connector	Connector	X				NA
LCD Interface	Connector	X				NA
COM8 Connector	Connector	X				NA
Audio Codec	TLV320AIC3106	X				0X19
Expansion Connector	Connector	X	X	X		NA
PMIC	LP8733	X				0x60
	LP8732	X				0x61
FPD Link	DS90UH925Q				X	0x1B
LI Camera	Connector				X	NA
CSI2 Camera	Connector				X	NA

3.6.23 GPIO List

Table 11 lists the SoC GPIOs. Signals used for GPIOs on expansion boards are not included in this list, because they are dependent upon the application board used.

Table 11. SoC GPIO Map

Feature	Peripheral Device	EVM Board Net	Function	SoC GPIO[(1)]
Connectivity on Module	COM8 Connector	GP5[4]	BT_EN	GPIO5_4
Connectivity on Module	COM8 Connector	GP5[5]	GPS_PPS_OUT	GPIO5_5
Connectivity on Module	COM8 Connector	GP5[6]	GPS_TIME_STAMP	GPIO5_6
Connectivity on Module	COM8 Connector	GP5[7]	WLAN_IRQ	GPIO5_7
Connectivity on Module	COM8 Connector	GP5[8]	WL_EN	GPIO5_8
Media Local Bus (MLB)	MLB Connector	GP5[9]	NA	GPIO5_9
Media Local Bus (MLB)	MLB Connector	GP6_[28]	NA	GPIO6_28
I/O Expander	PCF8575	PCF8575_INT	IOEXP_IRQ	GPIO7_31
Gig Ethernet	Ethernet PHY(s)	ENET_INTSn	ENET_IRQ	GPIO6_16

(1) Functional signals of pin MUX are not consider for this table. See the schematics for further details.

Table 11. SoC GPIO Map (continued)

Feature	Peripheral Device	EVM Board Net	Function	SoC GPIO[1]
LCD Touch Panel	Display Connector	GP1[15]	TS_LCD_IRQ	GPIO1_15
FPD-Link Panel	FPD-Link Txmt	VOUT2_INTB	FPDTX_IRQ	GPIO3_38
Power Management	LP8733/32	LP_INTn	PMIC_IRQ	GPIO1_3
Power Management	Suspend2RAM	POWERHOLD_CLK	POWERDOWN	GPIO7_30
SD Card	Micro-SD	MMC1_SDCD	CARD_DETECT	GPIO6_27
SD Card	Micro-SD	SPI[1]_CS[1]	IO_VOLTAGE_LVL	GPIO7_11
Test	Automated Test	GP5[0]	USER_DEFINED	GPIO5_0

3.6.24 I/O Expander List

Table 12 lists the I/O expander map.

Table 12. I/O Expander Map

Device	Slave Address	I^2C I/F	Expander I/O	Netname	Description
EXP1	0b0010 000 (0x20)	I2C1	**INT Number**	PCF8575_INT	Interrupt output to SoC
			P0	TS_LCD_GPIO1	Push-button switch 1
			P1	TS_LCD_GPIO2	Push-button switch 2
			P2	TS_LCD_GPIO3	Push-button switch 3
			P3	TS_LCD_GPIO4	Push-button switch 4
			P4	USER_LED1	User LED 1
			P5	USER_LED2	User LED 2
			P6	USER_LED3	User LED 3
			P7	USER_LED4	User LED 4
			P10	EXP_ETH0_RSTn	RGMII0 reset
			P11	EXP_ETH1_RSTn	RGMII1 reset
			P12	USB1-VBUS_OCN	USB1 overcurrent indication
			P13	USB2-VBUS_OCN	USB2 overcurrent indication
			P14	PCI_SW_RESETn	PCI interface software reset
			P15	CON_LCD_PWR_DN	LCD board master power enable
			P16	USB1-VBUS_DET	USB1 VBUS detection
			P17	USB2-VBUS_DET	USB2 VBUS detection

Table 12. I/O Expander Map (continued)

Device	Slave Address	I²C I/F	Expander I/O	Netname	Description
EXP2	0b0010 001 (0x21)	I2C1	**INT Number**	PCF8575_INT	Interrupt output to SoC
			P0	SEL_GPMC_AD_VID_S0	MUX out control signal for GPMC versus VOUT3B versus VIN1A
			P1	USB1_ID	USB1 ID PIN
			P2	USB2_ID	USB2 ID PIN
			P3	SEL_I2C3_CAN2	MUX out control signal for I2C3 versus DCAN2
			P4	SEL_ENET_MUX_S0	MUX out control signal for RGMII0 versus VIN
			P5	MMC_PWR_ON	Power on regulator to MMC card
			P6	NOR_ALT_ADDRn	MUX out control signals for alternate location of GPMC control signals
			P7	SEL_GPMC_AD_VID_S2	MUX out control signal for GPMC versus VOUT3B versus VIN1A
			P10	NAND_BOOTn	NAND boot chip select enable signal
			P11	NOR_BOOTn	NOR boot chip select enable signal
			P12	MMC2_BOOT	MUX out control signal for GPMC versus MMC2
			P13	PFC_VPP_ENn	Enable for VPP power supply
			P14	VOUT2_S0	MUX out control signal for EMU versus VIN2A versus VOUT2
			P15	MCASP1_ENn	COM8 interface level shifter enable signal
			P16	SEL_UART3_SPI2	MUX out control signal for UART3 versus SPI2
			P17	VOUT2_S1	MUX out control signal for EMU versus VIN2A versus VOUT2
EXP3	0b0010 010 (0x26)	I2C5	P0	PM_OEn	Enable to connect PM Bus with I2C3
			P1	VIN6_SEL_S0	MUX out control signal for VIN6A and McASPx
			P2	VIN2_S0	MUX out control signal for EMAC1 and VIN2A signals
			P3	PM_SEL	Selection to connect I2C3 to either PM bus 1 or 2
			P4	HDMI_CT_HPD	HDMI hot plug detect
			P5	HDMI_LS_OE	HDMI level shifter enable
			P6	VIN2_S2	MUX out control signal for VIN2A versus expansion signals
			P7	CAN_STB	CAN transceiver standby
			P10	SEL_CSI2n	MUX out control signal for CSI2 configuration
			P11	EXVIN2_S0	MUX out control signal for EMAC1 versus VIN2A versus expansion signals
			P12	EXVIN2_S2	MUX out control signal for EMAC1 versus VIN2A versus expansion signals
			P13	MMC3_SEL	MUX out control signal for MMC3 versus VIN2B
			P14	MMC2_BOOT_OVR_OEN	MMC2 DIP switch override enable
			P15	MMC2_BOOT_OVR	MMC2 DIP switch override
			P16	NOR_BOOT_OVR_OEN	NOR BOOT DIP switch override enable
			P17	NOR_BOOT_OVR	NOR BOOT DIP switch override

3.6.25 Configuration EEPROM

The CPU board contains an EEPROM memory device for storing and retrieving configuration information. The EEPROM provides 256Kb (or 32KB) of storage space, and is accessible using I^2C (the device location information is in Table 10). The configuration ID information is programmed by the factory at the time of manufacturing, and should not be altered. Table 13 lists the configuration data format within the EEPROM.

- EEPROM device used: Catalyst Semiconductor CAT24C256WI-G
- I^2C Bus/Address: I2C1, 0x50

Table 13. Configuration EEPROM

EEPROM Field	Byte Location	Value (Rev A CPU Board Example)	Description
ID.HEADER	[3:0]	0xAA5533EE	Fixed value at start of header ID.
ID.BOARD_NAME	[19:4]	DRA79x, DRA71x (ASCII)	For J6Entry – fixed value of DRA79x,DRA71x
ID.VERSION_MAJOR	[21:20]	0x1	A = 0x1 B = 0x2 C = 0x3
ID.VERSION_MINOR	[23:22]	0x0	0x0 for major revision 0x1-0x15 for others
ID.CONFIG_OPTION	[27:24]	0x0E	Bit 6: 1 – EMIF2 ECC Supported, 0 – No Bit 5: 1 – EMIF2 Supported, 0 – No Bit 4: 1 – EMIF1 ECC Supported, 0 – No Bit 3: 1 – EMIF1 Supported, 0 – No Bit 2: 1 – Extended Memory EEPROM Cfg Support, 0 – No(1) Bit 1: 1 – MAC addr in EEPROM (default) Bit 0: 0 - QSPI (default), 1 - NOR
EMIF1_SIZE_BYTES	[31:28]	0x8000 0000	Memory size for EMIF1 in bytes (unsigned long)
EMIF2_SIZE_BYTES	[35:32]	0x0000 0000	Memory size for EMIF2 in bytes (unsigned long)
RESERVED	[55:36]	0x0	Reserved
MAC_ADDR	0x7F00	00.0E.99.zz.yy.xx	Optional MAC address

(1) If Bit 2 is set to 0, all EEPROM data beyond is set to 0 (Not defined or Used). If Bit 2 is set to 1, mapping is according to the table.

For reference, a C-style coded structure is provided, as follows.

```
Struct EEPROM_ID_T
{
    Unsigned long header;        4
    Char board_name[16];        16
    Unsigned short version_major;    2
    Unsigned short version_minor;    2
    Unsigned long config_option;        4
    Unsigned long emif1_size_bytes;     4
    Unsigned long emif2_size_bytes;    4
    Char reserved[28];            20
} eeprom_id;
```

4 Signal Multiplex Logic

Due to the high level of multiplexing on the SoC (over 16 levels), multiplex control logic is required to use different signals on the same SoC pins with their various functionality. The following information provides description of the logic.

An I^2C-based I/O expander controls the onboard MUXs. Table 14 lists the specific bits assigned to each MUX, as well as the specific settings for the various selections.

Table 14. Onboard MUX Setting and Control

MUX	Control Bits	Value	MUX Setting
A	NA	NA	QSPI Memory (default)
		NA	NOR Memory (requires resistor change)
C (RU4)	SW8.3	Off	NOR Memory
		On	EMMC Memory
	EXP3.P[15:14]	00	EMMC Memory
		01	Memory selected by SW8.3
		10	NOR Memory
		11	Memory selected by SW8.3 (default)
B (RU9, RU11, RU24)	EXP2.P[7,0]	00	Reserved
		01	VIN1A to Expansion
		10	VOUT3 to LCD Panel
		11	GPMC NOR/NAND (default)
D (RU6)	EXP3.P[6,2]	00	Reserved
		01	Peripheral selected by MUX E (desired default)
		10	VIN2A to Expansion
		11	Open (default)
E (RU12, RU23)	EXP2.P[17,14]	00	Reserved
		01	VOUT2 to FPD-Link III Transmitter
		10	VIN2A to LI Camera
		11	EMU (default)
F (RU27)	EXP3.P[12,11]	00	Reserved
		01	Peripheral selected by MUX E
		10	VIN2A to Expansion
		11	RGMII1 to Ethernet Port 1 (default)
K (RJ12)	EXP2.P16	0	UART3 to COM8Q
		1	Route to Expansion (SPI2) (default)
L (RU18)	EXP2.P3	0	Route to Expansion (I2C3)
		1	Route to DCAN2 Connector (default)
J (RU25)	EXP2.P4	0	Route to Expansion (VIN1B)
		1	RGMII0 to Ethernet Port 0 (default)
M (RU8)	EXP3.P13	0	Route to Expansion (VIN2B)
		1	Route to Expansion (MMC3/legacy) (default)
G (RU26)	SW8.7	Off	Use Default NOR Address (default)
		On	Use Alternate NOR Address (with EMMC)
H (RU10)	EXP3.P1	0	Route to COM8Q (MASP3/7)
		1	Route to Expansion (McASP3/7) (default)

4.1 GPMC and QSPI Selection (MUX A)

Figure 8 is part of the SoC pinmux table for the GPMC. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These functions include:

- Memory Bus (GPMC): A[18:13]
- Quad Serial Bus (QSPI): SCLK, D[3:0], CS[0], and RTCLK

Pad Name	Function 1		Function 2	
gpmc_a[13]	GPMC	gpmc_a[13]	QSPI1	qspi1_rtclk
gpmc_a[14]	GPMC	gpmc_a[14]	QSPI1	qspi1_d[3]
gpmc_a[15]	GPMC	gpmc_a[15]	QSPI1	qspi1_d[2]
gpmc_a[16]	GPMC	gpmc_a[16]	QSPI1	qspi1_d[0]
gpmc_a[17]	GPMC	gpmc_a[17]	QSPI1	qspi1_d[1]
gpmc_a[18]	GPMC	gpmc_a[18]	QSPI1	qspi1_sclk
gpmc_cs[2]	GPMC	gpmc_cs[2]	QSPI1	qspi1_cs[0]

Figure 8. SoC Pinmux for GPMC and QSPI

Mux A: Selects between NOR and QSPI memory support. The MUX is implemented using resistors. This was due to the signal rate and routing restrictions of the QSPI device. To enable the GPMC signals to NOR (shown in red), the board must be modified to move resistors. Figure 9 shows the MUX diagram for GPMC and QSPI.

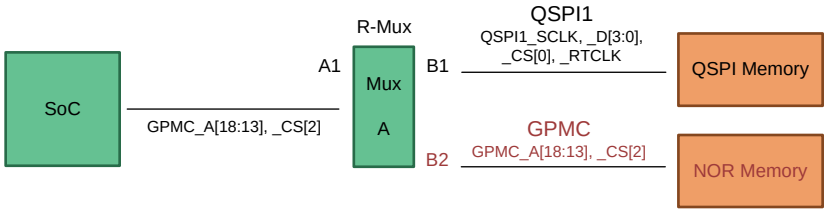


Figure 9. MUX Diagram for GPMC and QSPI

4.2 GPMC, VIN1, and VOUT3 Selection (MUX B)

Figure 10 is part of the SoC pinmux table for GPMC. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These functions include:

- Memory Bus (GPMC): AD[15:0], A[12:0]
- Video Input Port (VIN1A): CLK, HSYNC, VSYNC, DE, and D[23:0]
- Video Output Port (VOUT3): CLK, HSYNC, VSYNC, DE, and D[23:0]
- Boot Mode Selection (SYSBOOT): SYSBOOT[15:0]

Pad Name	Function 1		Function 3		Function 4		Function 16	
gpmc_ad[0]	GPMC	gpmc_ad[0]	VIP1	vin1a_d[0]	DSS	vout3_d[0]	CHIPGLUE	sysboot0
gpmc_ad[1]	GPMC	gpmc_ad[1]	VIP1	vin1a_d[1]	DSS	vout3_d[1]	CHIPGLUE	sysboot1
gpmc_ad[2]	GPMC	gpmc_ad[2]	VIP1	vin1a_d[2]	DSS	vout3_d[2]	CHIPGLUE	sysboot2
gpmc_ad[3]	GPMC	gpmc_ad[3]	VIP1	vin1a_d[3]	DSS	vout3_d[3]	CHIPGLUE	sysboot3
gpmc_ad[4]	GPMC	gpmc_ad[4]	VIP1	vin1a_d[4]	DSS	vout3_d[4]	CHIPGLUE	sysboot4
gpmc_ad[5]	GPMC	gpmc_ad[5]	VIP1	vin1a_d[5]	DSS	vout3_d[5]	CHIPGLUE	sysboot5
gpmc_ad[6]	GPMC	gpmc_ad[6]	VIP1	vin1a_d[6]	DSS	vout3_d[6]	CHIPGLUE	sysboot6
gpmc_ad[7]	GPMC	gpmc_ad[7]	VIP1	vin1a_d[7]	DSS	vout3_d[7]	CHIPGLUE	sysboot7
gpmc_ad[8]	GPMC	gpmc_ad[8]	VIP1	vin1a_d[8]	DSS	vout3_d[8]	CHIPGLUE	sysboot8
gpmc_ad[9]	GPMC	gpmc_ad[9]	VIP1	vin1a_d[9]	DSS	vout3_d[9]	CHIPGLUE	sysboot9
gpmc_ad[10]	GPMC	gpmc_ad[10]	VIP1	vin1a_d[10	DSS	vout3_d[10]	CHIPGLUE	sysboot10
gpmc_ad[11]	GPMC	gpmc_ad[11]	VIP1	vin1a_d[11	DSS	vout3_d[11]	CHIPGLUE	sysboot11
gpmc_ad[12]	GPMC	gpmc_ad[12]	VIP1	vin1a_d[12	DSS	vout3_d[12]	CHIPGLUE	sysboot12
gpmc_ad[13]	GPMC	gpmc_ad[13]	VIP1	vin1a_d[13	DSS	vout3_d[13]	CHIPGLUE	sysboot13
gpmc_ad[14]	GPMC	gpmc_ad[14]	VIP1	vin1a_d[14	DSS	vout3_d[14]	CHIPGLUE	sysboot14
gpmc_ad[15]	GPMC	gpmc_ad[15]	VIP1	vin1a_d[15	DSS	vout3_d[15]	CHIPGLUE	sysboot15
gpmc_a[0]	GPMC	gpmc_a[0]	VIP1	vin1a_d[16	DSS	vout3_d[16]		
gpmc_a[1]	GPMC	gpmc_a[1]	VIP1	vin1a_d[17	DSS	vout3_d[17]		
gpmc_a[2]	GPMC	gpmc_a[2]	VIP1	vin1a_d[18	DSS	vout3_d[18]		
gpmc_a[3]	GPMC	gpmc_a[3]	VIP1	vin1a_d[19	DSS	vout3_d[19]		
gpmc_a[4]	GPMC	gpmc_a[4]	VIP1	vin1a_d[20	DSS	vout3_d[20]		
gpmc_a[5]	GPMC	gpmc_a[5]	VIP1	vin1a_d[21	DSS	vout3_d[21]		
gpmc_a[6]	GPMC	gpmc_a[6]	VIP1	vin1a_d[22	DSS	vout3_d[22]		
gpmc_a[7]	GPMC	gpmc_a[7]	VIP1	vin1a_d[23	DSS	vout3_d[23]		
gpmc_a[8]	GPMC	gpmc_a[8]	VIP1	vin1a_hsyr	DSS	vout3_hsync		
gpmc_a[9]	GPMC	gpmc_a[9]	VIP1	vin1a_vsyn	DSS	vout3_vsync		
gpmc_a[10]	GPMC	gpmc_a[10]	VIP1	vin1a_de0	DSS	vout3_de		
gpmc_a[11]	GPMC	gpmc_a[11]	VIP1	vin1a_fld0	DSS	vout3_fld		
gpmc_a[12]	GPMC	gpmc_a[12]						
gpmc_cs[3]	GPMC	gpmc_cs[3]	VIP1	vin1a_clk0	DSS	vout3_clk		

Figure 10. SoC Pinmux for GPMC, VIN1, and VOUT3

MUX B: Selects between NOR and NAND memories, LCD panel for video, and expansion. The selection is made using the I/O expander 2, bits P7 and P0. The defaults is set to enable GPMC to NOR and NAND memories – which is required for SYSBOOT mode latching. Figure 11 shows the MUX diagram for GPMC, VIN1, and VOUT3

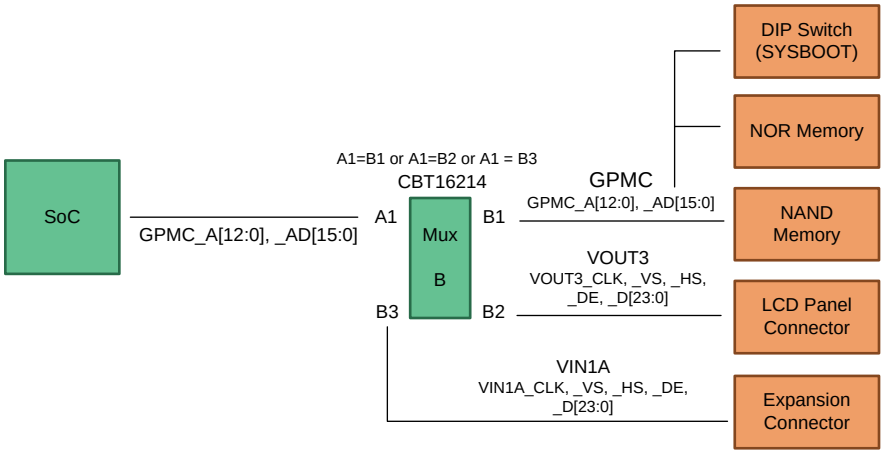


Figure 11. MUX Diagram for GPMC, VIN1, and VOUT3

4.3 GPMC and EMMC Selection (MUX C)

Figure 12 is part of the SoC pinmux table for GPMC. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These functions include:

- Memory Bus (GPMC): A[27:19]
- EMMC Memory (MMC2): CLK, CMD, D[7:0]

Pad Name	Function 1		Function 2	
gpmc_a[19]	GPMC	gpmc_a[19]	MMC2	mmc2_dat[4]
gpmc_a[20]	GPMC	gpmc_a[20]	MMC2	mmc2_dat[5]
gpmc_a[21]	GPMC	gpmc_a[21]	MMC2	mmc2_dat[6]
gpmc_a[22]	GPMC	gpmc_a[22]	MMC2	mmc2_dat[7]
gpmc_a[23]	GPMC	*gpmc_a[23]*	MMC2	mmc2_clk
gpmc_a[24]	GPMC	*gpmc_a[24]*	MMC2	mmc2_dat[0]
gpmc_a[25]	GPMC	*gpmc_a[25]*	MMC2	mmc2_dat[1]
gpmc_a[26]	GPMC	*gpmc_a[26]*	MMC2	mmc2_dat[2]
gpmc_a[27]	GPMC	*gpmc_a[27]*	MMC2	mmc2_dat[3]
gpmc_cs[1]	GPMC	gpmc_cs[1]	MMC2	mmc2_cmd

Figure 12. SoC Pinmux for GPMC and EMMC

MUX C: Selects between NOR memory and EMMC memory. The selection is made using the I/O expander 3, bits P15 and P14. If booting from EMMC, the DIP Switch SW8 position 3 is used to select interface (by default). Figure 13 shows the MUX diagram for GPMC and EMMC.

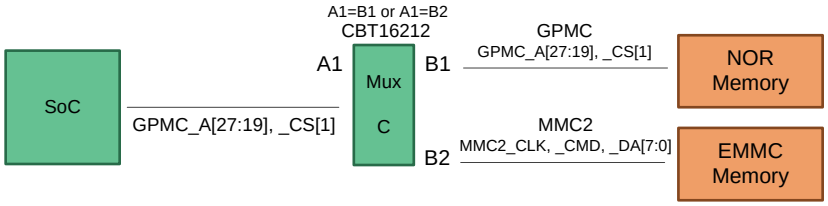


Figure 13. MUX Diagram for GPMC and EMMC

4.4 VIN2A and EMU Selection (MUX D, MUX E)

Figure 14 is part of the SoC pinmux table for VIN2A. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These functions include:

- Video Input Port (VIN2A): CLK, HSYNC, VSYNC, DE, D[9:0]
- Video Output Port (VOUT2): CLK, HSYNC, VSYNC, DE, D[23:14]
- Debug/Trace (EMU): EMU[19:5]

Pad Name	Function 1		Function 4		Function 5		Function 6	
vin2a_clk0	VIP1	vin2a_clk0			DSS	vout2_fld	DEBUGSS	emu5
vin2a_de0	VIP1	vin2a_de0	VIP1	vin2b_de1	DSS	vout2_de	DEBUGSS	emu6
vin2a_fld0	VIP1	vin2a_fld0			DSS	vout2_clk	DEBUGSS	emu7
vin2a_hsync0	VIP1	vin2a_hsync0	VIP1	vin2b_hsync1	DSS	vout2_hsync	DEBUGSS	emu8
vin2a_vsync0	VIP1	vin2a_vsync0	VIP1	vin2b_vsync1	DSS	vout2_vsync	DEBUGSS	emu9
vin2a_d[0]	VIP1	vin2a_d[0]			DSS	vout2_d[23]	DEBUGSS	emu10
vin2a_d[1]	VIP1	vin2a_d[1]			DSS	vout2_d[22]	DEBUGSS	emu11
vin2a_d[2]	VIP1	vin2a_d[2]			DSS	vout2_d[21]	DEBUGSS	emu12
vin2a_d[3]	VIP1	vin2a_d[3]			DSS	vout2_d[20]	DEBUGSS	emu13
vin2a_d[4]	VIP1	vin2a_d[4]			DSS	vout2_d[19]	DEBUGSS	emu14
vin2a_d[5]	VIP1	vin2a_d[5]			DSS	vout2_d[18]	DEBUGSS	emu15
vin2a_d[6]	VIP1	vin2a_d[6]			DSS	vout2_d[17]	DEBUGSS	emu16
vin2a_d[7]	VIP1	vin2a_d[7]			DSS	vout2_d[16]	DEBUGSS	emu17
vin2a_d[8]	VIP1	vin2a_d[8]			DSS	vout2_d[15]	DEBUGSS	emu18
vin2a_d[9]	VIP1	vin2a_d[9]			DSS	vout2_d[14]	DEBUGSS	emu19

Figure 14. SoC Pinmux for VIN2A and EMU

MUX D: Selects between onboard support and expansion support for the VIN2A, EMU signals. The selection is made using the I/O expander 3, bits P6 and P2. The default mode is set to onboard peripheral selection, such JTAG/Trace can be supported without I^2C accesses.

MUX E: Selects between LI Camera, FPD-Link transmitter, and JTAG/Trace. The selection is made using the I/O expander 2, bits P17 and P14. The default mode is set to EM, such JTAG/Trace can be supported without I^2C accesses. Figure 15 shows the MUX diagram for VIN2A and EMU

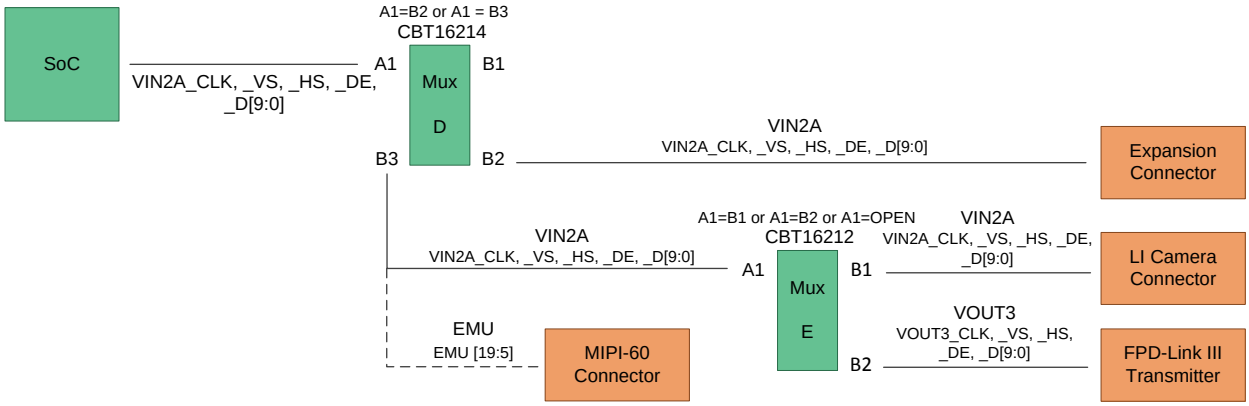


Figure 15. MUX Diagram for VIN2A and EMU

4.5 VIN2A and RGMII1 Selection (MUX F)

Figure 16 is part of the SoC pinmux table for VIN2A. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These functions include:

- Video Input Port (VIN2A): D[23:10]
- Gig Ethernet (RGMII1): TXC, TXCTL, TXD[3:0], RXC, RXCTL, RXD[3:0]
- Management Data I/O (MDIO): MCLK, D

Pad Name	Function 1		Function 4		Function 5	
vin2a_d[10]	VIP1	vin2a_d[10]	EMAC	*mdio_mclk*	DSS	vout2_d[13]
vin2a_d[11]	VIP1	vin2a_d[11]	EMAC	*mdio_d*	DSS	vout2_d[12]
vin2a_d[12]	VIP1	vin2a_d[12]	EMAC	rgmii1_txc	DSS	vout2_d[11]
vin2a_d[13]	VIP1	vin2a_d[13]	EMAC	rgmii1_txctl	DSS	vout2_d[10]
vin2a_d[14]	VIP1	vin2a_d[14]	EMAC	rgmii1_txd[3]	DSS	vout2_d[9]
vin2a_d[15]	VIP1	vin2a_d[15]	EMAC	rgmii1_txd[2]	DSS	vout2_d[8]
vin2a_d[16]	VIP1	vin2a_d[16]	EMAC	rgmii1_txd[1]	DSS	vout2_d[7]
vin2a_d[17]	VIP1	vin2a_d[17]	EMAC	rgmii1_txd[0]	DSS	vout2_d[6]
vin2a_d[18]	VIP1	vin2a_d[18]	EMAC	rgmii1_rxc	DSS	vout2_d[5]
vin2a_d[19]	VIP1	vin2a_d[19]	EMAC	rgmii1_rxctl	DSS	vout2_d[4]
vin2a_d[20]	VIP1	vin2a_d[20]	EMAC	rgmii1_rxd[3]	DSS	vout2_d[3]
vin2a_d[21]	VIP1	vin2a_d[21]	EMAC	rgmii1_rxd[2]	DSS	vout2_d[2]
vin2a_d[22]	VIP1	vin2a_d[22]	EMAC	rgmii1_rxd[1]	DSS	vout2_d[1]
vin2a_d[23]	VIP1	vin2a_d[23]	EMAC	rgmii1_rxd[0]	DSS	vout2_d[0]

Figure 16. SoC Pinmux for VIN2A and RGMII1

MUX F: Selects between Gig Ethernet and Expansion, and combines with MUX E to support the LI Camera and FPD-Link transmitter. The selection is made using the I/O expander 3, bits P12 and P11, with the default set to Gig Ethernet.

The MDIO MUX setting shown (in red) is used only if the RGMII0 port is not selected. Otherwise, the MDIO function is provided by other pins. The MUX selection for MDIO is automatic based on the RGMII0 MUX setting. Figure 17 shows the MUX diagram for VIN2A and RGMII1.

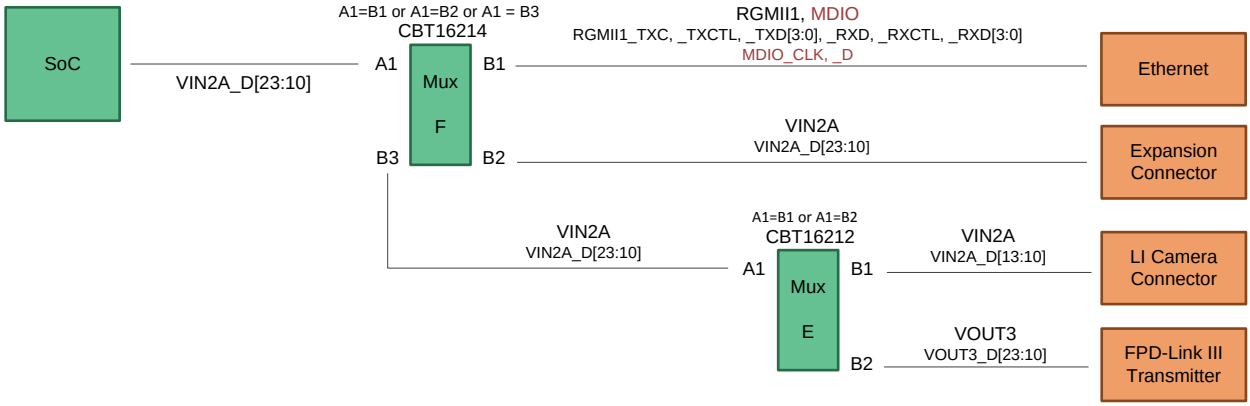


Figure 17. MUX Diagram for VIN2A and RGMII1

4.6 RGMII0 and VIN1B Selection (MUX J)

Figure 18 is part of the SoC pinmux table for RGMII0. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These functions include:

- Gig Ethernet (RGMII0): TXC, TXCTL, TXD[3:0], RXC, RXCTL, RXD[3:0]
- Management Data I/O (MDIO): MCLK, D
- Video Input Port (VIN1B): CLK, HSYNC, VSYNC, DE, [7:0]

Pad Name	Function 1		Function 6	
mdio_mclk	EMAC	mdio_mclk	VIP1	vin1b_clk1
mdio_d	EMAC	mdio_d	VIP1	vin1b_d[0]
uart3_rxd	UART3	uart3_rxd	VIP1	vin1b_d[1]
uart3_txd	UART3	uart3_txd	VIP1	vin1b_d[2]
rgmii0_txc	EMAC	rgmii0_txc	VIP1	vin1b_d[3]
rgmii0_txctl	EMAC	rgmii0_txctl	VIP1	vin1b_d[4]
rgmii0_txd[3]	EMAC	rgmii0_txd[3]	VIP1	vin1b_de1
rgmii0_txd[2]	EMAC	rgmii0_txd[2]	VIP1	vin1b_hsync1
rgmii0_txd[1]	EMAC	rgmii0_txd[1]	VIP1	vin1b_vsync1
rgmii0_txd[0]	EMAC	rgmii0_txd[0]		
rgmii0_rxc	EMAC	rgmii0_rxc	VIP1	vin1b_d[5]
rgmii0_rxctl	EMAC	rgmii0_rxctl	VIP1	vin1b_d[6]
rgmii0_rxd[3]	EMAC	rgmii0_rxd[3]	VIP1	vin1b_d[7]
rgmii0_rxd[2]	EMAC	rgmii0_rxd[2]		
rgmii0_rxd[1]	EMAC	rgmii0_rxd[1]		
rgmii0_rxd[0]	EMAC	rgmii0_rxd[0]	VIP1	vin1b_fld1

Figure 18. SoC Pinmux for RGMII0 and VIN1B

Mux J: Selects between Gig Ethernet and Expansion. The selection is made using the I/O expander 2, bit P4, defaulting to Gig Ethernet. Figure 19 shows the MUX diagram for RGMII0 and VIN1B.

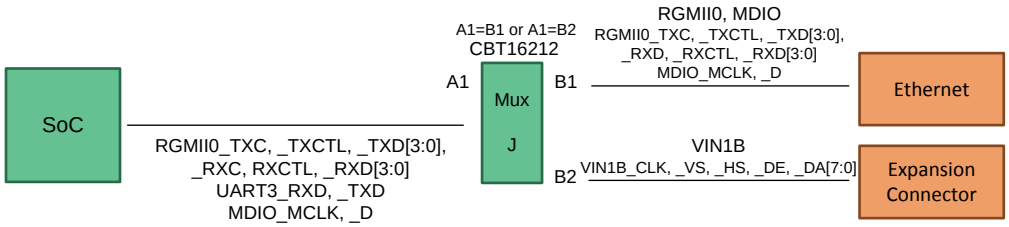


Figure 19. MUX Diagram for RGMII0 and VIN1B

4.7 SPI2 and UART3 Selection (MUX K)

Figure 20 is part of the SoC pinmux table for SPI2. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These functions include:

- SPI Serial Bus (SPI2): SCLK, D[1:0], CS[0]
- UART Serial Bus (UART3): TXD, RXD, CTSN, RTSN

Pad Name	Function 1		Function 2	
spi2_sclk	SPI2	spi2_sclk	UART3	uart3_rxd
spi2_d[1]	SPI2	spi2_d[1]	UART3	uart3_txd
spi2_d[0]	SPI2	spi2_d[0]	UART3	uart3_ctsn
spi2_cs[0]	SPI2	spi2_cs[0]	UART3	uart3_rtsn

Figure 20. SoC Pinmux for SPI2 and UART3

MUX K: Selects between Bluetooth (COM8Q module) and expansion interface. The selection is made using the I/O expander 2, bits P16, defaulting to expansion. Figure 21 shows the MUX diagram for SPI2 and UART3.

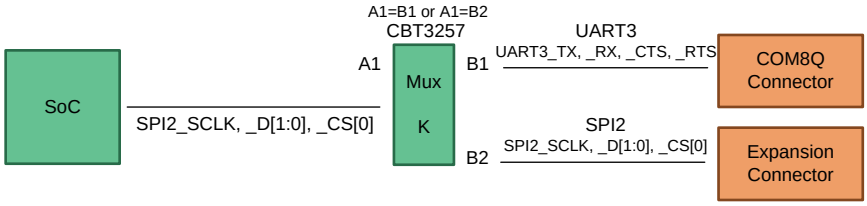


Figure 21. MUX Diagram for SPI2 and UART3

4.8 DCAN2 and I2C3 Selection (MUX L)

Figure 22 is part of the SoC pinmux table for DCAN2. The SoC device supports additional functions not shown in the table. The functions shown are intended to reflect those supported on the EVM. These functions include:

- Digital CAN Bus (DCAN2): TX, RX
- I^2C Serial Bus (I2C3): SCL, SDA

Pad Name	Function 3		Function 10	
gpio6_14	DCAN2	dcan2_tx	I2C3	i2c3_sda
gpio6_15	DCAN2	dcan2_rx	I2C3	i2c3_scl

Figure 22. SoC Pinmux for DCAN2

MUX L: Selects between DCAN2 header and expansion interface. The selection is made using the I/O expander 2, bit P3, defaulting to onboard DCAN header. Figure 23 shows the MUX diagram for DCAN2 and I2C.

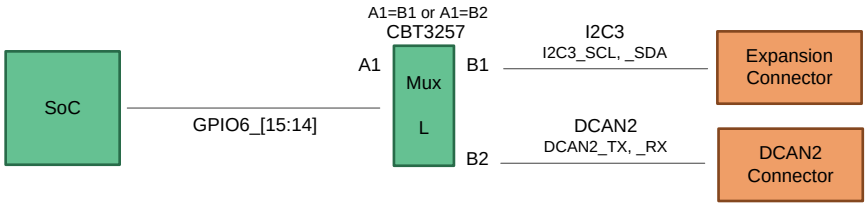


Figure 23. MUX Diagram for DCAN2 and I2C

5 USB3 Supported Configurations

The following USB3.x combinations are supported:

- Micro-A plug to standard-B plug:
  - Connect to hub or external drive/device that has a standard B receptacle.
- Micro-A plug to Micro-B plug:
  - EVM connects to hub or external drive/device that has a Micro B receptacle.
  - Host connects to the EVM acting as a device.
- Standard-A plug to Micro-B plug:
  - Host connects to the EVM acting as a device.

5.1 Option 1

Use a USB 3.0 Micro-AB to standard-B and USB 3.0 SIIG® hub as shown in Figure 24 and Figure 25.

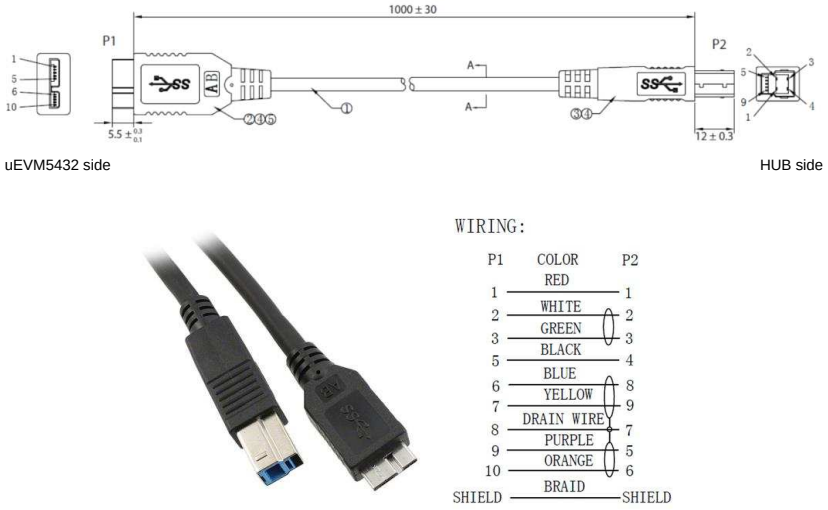


Figure 24. Qualtek 3023009-01M USB 3.0 Micro-AB to Standard-B 1m (3.28')

Figure 25. SIIG JU-H40312-S14-Port USB 3.0 Super Speed USB Hub

5.2 Option 2

Use a USB 3.0 Micro-A to Micro-B and USB 3.0 IOGEAR® hub as shown in Figure 26 and Figure 27.

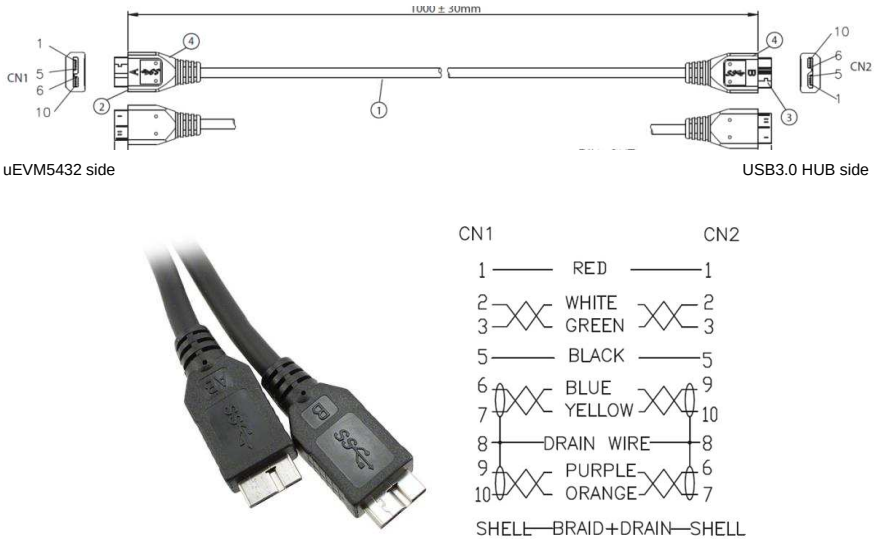
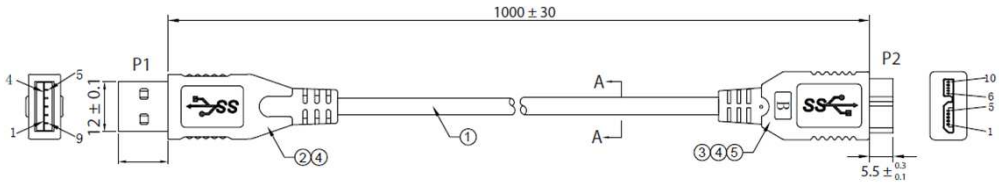


Figure 26. Qualtek 3023007-01M USB 3.0 Micro-A to Micro-B 1m (3.28')

Figure 27. IOGEAR GUH374 4-Port USB 3.0 HUB

5.3 Option 3

Use a USB 3.0 standard-A to Micro-B as shown in Figure 28. The host PC connects to the EVM acting as a device.



WIRING:

P1	COLOR	P2
1	RED	1
2	WHITE	2
3	GREEN	3
4	BLACK	5
5	BLUE	6
6	YELLOW	7
7	DRAIN WIRE	8
8	PURPLE	9
9	ORANGE	10
SHIELD	BRAID	SHIELD

Figure 28. Qualtek 3023005-01M USB 3.0 Standard-A to Micro-B 1m (3.28')

6 References

- Texas Instruments, DRA71x/DRA79x/TDA2Ex-17/AM570x CPU board PCB rev C
- Texas Instruments, DRA71x/DRA79x/TDA2Ex-17/AM570x CPU board Schematic rev C1
- Texas Instruments, DRA71x/DRA79x/TDA2Ex-17/AM570x CPU board BOM rev C
- Texas Instruments, DRA71x/DRA79x/TDA2Ex-17/AM570x CPU board assembly drawing rev C
- Texas Instruments, DRA71x/DRA79x/TDA2Ex-17/AM570x CPU board PCB drawing rev C

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (Auigust 2017) to A Revision	Page
• Update was made in Section 3.3.	10

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