DRA7x EVM CPU Board

User's Guide

Literature Number: SPRUI50
February 2016

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DRA7x EVM CPU Board

This user's guide is intended for software and hardware engineers developing applications for the Jacinto 6 high performance, multimedia application processor based on enhanced OMAP™ architecture implemented with 28-nm technology. It describes the EVM CPU board's hardware, firmware and software functions supplied by Texas Instruments Inc.

The schematics mentioned in this document can be downloaded from the *CPU EVM Schematic Rev H* (SPRR210).

1 Introduction

To allow scalability and re-use across DRA74x and DRA75x "Jacinto" Infotaiment System-on-Chips (SoCs), it is based on "Jacinto 6 Ex" DRA75x SoC that incorporates a heterogeneous, scalable architecture that includes a mix of two ARM® Cortex®-A15 Microprocessor Units, two ARM Cortex-M4 Processing Subsystems, each with two ARM Cortex-Microprocessors, two Digital Signal Processors (DSP C66x), a Vision AccelerationPac including two Embedded Vision Engines (EVEs), 2D and 3D-Graphic Processing Units including Imagination Technologies POWERVR® SGX544 dual-core and High-Definition Image and Video Accelerator. Also it integrates a host of peripherals including multi-camera interfaces (both parallel and serial) for LVDS-based surround view systems, displays, CAN and GigB Ethernet AVB.

The main CPU board integrates these key peripherals such as Ethernet or HDMI, while the infotainment application daughter board (JAMR3) and LCD/TS daughter board will complement the CPU board to deliver complete system to jump start your evaluation and application development.

2 Overview

An EVM system is comprised of a CPU board with one or more application board(s). The CPU board (shown in Figure 1) can be used standalone for software debug and development. Each EVM system has been designed to enable customers to evaluate the Processor performance and flexibility in the following targeted markets:

- Automotive Infotainment applications
- Automotive Vision applications
- Emerging End Equipment applications

The CPU board contains the (Jacinto 6/TDA2x) applications processor, a companion Power Management IC (TPS659039), Audio Codec (TLV320AIC3106), DDR3 DRAM, four different Flash memories (QSPI, eMMC, NAND and NOR), a multitude of interface ports and expansion connectors. The board provides additional support components that provide software debugging, signal routing and configuration controls that would not be needed in a final product. Different version CPU boards will be built to support the development process that include:

- Socketed processor used for wakeup, early software development, quick and easy chip revision evaluation
- Soldered-down processor used for high performance Use Cases and evaluations

All other components on-board are soldered-down.

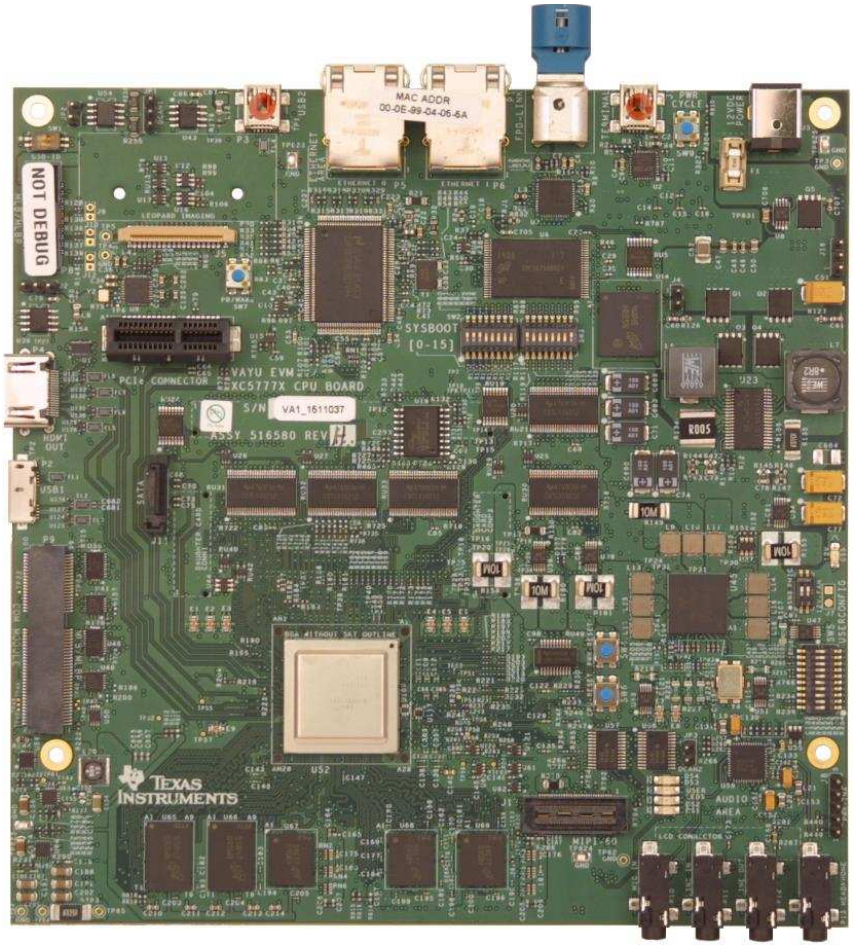


Figure 1. CPU Board

2.1 EVM System Configurations

2.1.1 Revisions

- ES1.0 is on CPU Board through Rev E (obsolete), ES1.1 is on CPU Board Rev G (obsolete), and ES2.0 is on CPU Board Rev H+
- Table 1 through Table 5 indicates the obsolete and valid production versions.

Table 1. EVM Wake-Up Board and Kits (Obsolete)

Wake-Up Platforms	Description	Model Number
ES1.0 CPU Bd	Socketed CPU Board, Power Supply and Limited Accessory Cables.	EVM5777BX-01-00-00
ES1.0 EVM Kit	Socketed CPU Board, LCD/TS Daughter Bd, Power Supply and Limited Accessory Cables.	EVM5777X-01-00-00
ES1.0 EVM Infotainment Kit	Socketed CPU Board, JAMR3 Apps Bd, LCD/TS Daughter Bd, Power Supply and Limited Accessory Cables.	EVM5777X-01-20-00
ES1.0 EVM Vision Kit	Socketed CPU Board, Vision Apps Bd, LCD/TS Daughter Bd, Power Supply and Limited Accessory Cables.	EVM5777X-01-40-00

Table 2. Production Boards (Obsolete)

Production Boards	Description	Model Number
CPU Bd ES1.1 GP	CPU Board, Power Supply and Limited Accessory Cables	EVM5777BG-02-00-00
CPU Bd ES1.1 HS	CPU Board, Power Supply and Limited Accessory Cables	EVM5777BH-02-00-00
CPU Bd ES1.0 GP	CPU Board, Power Supply and Limited Accessory Cables	EVM5777BG-01-00-00
CPU Bd ES1.0 HS	CPU Board, Power Supply and Limited Accessory Cables	EVM5777BH-01-00-00
LCD/TS Daughter Board	7-inch WVGA LCD (24-bit color) with projective / capacitive touch-screen and bezel / frame	EVM5777LCDTS-V1-0
10.1” LCD/TS Daughter Board	10.1-inch 1280X800 LCD (24-bit color) with projective / capacitive touch-screen and bezel / frame	EVM5777LCDTS-V2-0
Vision Application Board	Support for multiple camera inputs for surround view, stereo vision, and proprietary camera board interfaces	EVM5777VISION-V1-0

Table 3. Production Kits (Obsolete)

Production Kits	Description	Model Number
ES1.1 GP EVM Kit	CPU Board, 10.1” LCD/TS Daughter Bd, Power Supply and Limited Accessory Cables.	EVM5777G-02-01-00
ES1.1 GP EVM Infotainment Kit	CPU Board, JAMR3 Apps Bd, 10.1” LCD/TS Daughter Bd, Power Supply and Limited Accessory Cables.	EVM5777G-02-21-00
ES1.1 GP EVM Vision Kit	CPU Board, Vision Apps Bd, 10.1” LCD/TS Daughter Bd, Power Supply and Limited Accessory Cables.	EVM5777G-02-40-00
ES1.0 GP EVM Kit	CPU Board, LCD/TS Daughter Bd, Power Supply and Limited Accessory Cables.	EVM5777G-01-00-00
ES1.0 GP EVM Infotainment Kit	CPU Board, JAMR3 Apps Bd, LCD/TS Daughter Bd, Power Supply and Limited Accessory Cables.	EVM5777G-01-20-00
ES1.0 GP EVM Vision Kit	CPU Board, Vision Apps Bd, LCD/TS Daughter Bd, Power Supply and Limited Accessory Cables.	EVM5777G-01-40-00

Table 4. Production Boards

Production Boards	Description	Model Number
CPU Bd 2.0 GP	CPU Board and Limited Accessory Cables.	EVM5777BG-03-00-00
PU Bd ES2.0 HS	CPU Board and Limited Accessory Cables.	EVM5777BH-03-00-00
10.1” LCD/TS Daughter Board	10.1-inch 1920X1200 LCD (24-bit color) capacitive touch-screen and bezel / frame	EVM5777LCDTS-V3-0
JAMR3 Application Board	Head-unit DIN form-factor Application Board with radio tuners, multiple audio I/O’s, and video input extendibility	EVM5777JAMR3-V1-0
Vision Application Board	Support for multiple camera inputs for surround view, stereo vision, and proprietary camera board interfaces, AD7611 HDMI receiver	EVM5777VISION-V2-0

Table 5. Production Kits

Production Kits	Description	Model Number
ES2.0 GP EVM Kit	CPU Board, 10.1” LCD/TS Daughter Bd and Limited Accessory Cables.	EVM5777G-03-00-00
ES2.0 GP EVM Infotainment Kit	CPU Board, JAMR3 Apps Bd, 10.1” LCD/TS Daughter Bd and Limited Accessory Cables.	EVM5777G-03-20-00
ES2.0 GP EVM Vision Kit	CPU Board, Vision Apps Bd, 10.1” LCD/TS Daughter Bd and Limited Accessory Cables.	EVM5777G-03-40-00

Table 6. EVM Kit Truth Table

Kit Name	CPU Bd	JAMR3 App Bd	LCD/TS Daughter Bd	Vision App Bd	2.1mm to 2.5mm Power Supply Adapter
GP EVM	X				X
GP EVM Infotainment	X	X	X		X
GP EVM Vision	X			X	X

Wall Power Supply not included. Table 7 that lists the recommended and tested supplies.

Table 7. 12 V, 5A, 65W Compatible Wall Supplies

Digi-Key Part Number	Manufacturer Part Number	Manufacturer	Output Connector	Notes
102-3417-ND	SDI65-12-U-P5	CUI Inc.	Barrel Plug, 2.1mm I.D. x 5.5mm O.D. x 9.5mm	Required adapter, provided in the EVM Kits
62-1221-ND	KTPS65-1250DT-3P-VI-C-P1	Volgen America/ Kaga Electronics USA	Barrel Plug, 2.1mm I.D. x 5.5mm O.D. x 9.5mm	Required adapter, provided in the EVM Kits
102-3419-ND	SDI65-12-UD-P5	CUI Inc.	Barrel Plug, 2.1mm I.D. x 5.5mm O.D. x 9.5mm	Required adapter, provided in the EVM Kits
SDI65-12-U-P6-ND	SDI65-12-U-P6	CUI Inc.	Barrel Plug, 2.5mm I.D. x 5.5mm O.D. x 9.5mm	
SDI65-12-UD-P6-ND	SDI65-12-UD-P6	CUI Inc.	Barrel Plug, 2.5mm I.D. x 5.5mm O.D. x 9.5mm	

2.2 CPU Board Feature List

- Processor:
  - SoC (23mm x 23mm package, 0.8mm pitch with 28x28 via-channel array)
  - Support for corresponding socket
- Memory:
  - EMIF1 - DDR3L-1066 (with ECC): two 8Gbit (16bit data/ea) and one 4Gbit (8bit data, for ECC) memory devices
  - EMIF2 - DDR3L-1066: four 4Gbit (8bit data/ea) memory devices
  - QSPI (Quad SPI)
  - eMMC
  - NAND flash memory 16 bit
  - NOR flash memory
  - I2C EEPROM
- Boot mode selection DIP switch
- On-Board Temperature Sensor
  - TMP102
- JTAG/Emulator:
  - 60-pin MIPI Connector
  - 20-pin-CTI adapter: 10 x 2, 1.27mm pitch
  - 14-pin adapter: 7 x 2, 2.54mm pitch
- Audio input and output:
  - AIC3106 codec: Headphone OUT, Line OUT, Line IN, Microphone IN

- Connectors and Transceivers:
  - CAN Interface - 2-wire PHY on DCAN1
  - Two USB Host receptacles:
    - USB3.0 (micro-USB)
    - USB2.0 (mini-USB)
  - PCIe x 1
  - Video - one HDMI Out, one FPD-Link III, one LCD
  - MLB and MLBP on Mictor connector
  - RS232 via USB FTDI converter (mini-A/B USB)
  - COM8 connector
  - Gigabit Ethernet PHY (RJ45) x 2
  - MicroSD socket
  - SATA
  - I2C Expander
  - LCD Daughter Board connector
- Power supply:
  - 12 V DC input (Wall supply not supplied with Kit)
  - Optimized Power Management IC (PMIC) Solution
  - Support sleep mode with wake-up capability
- PCB:
  - Dimension (W x D): 170mm x 170mm
  - Expansion Connectors to support application boards

3 Hardware

3.1 Hardware Architecture

Figure 2 shows the CPU Board's Functional Block Diagram.

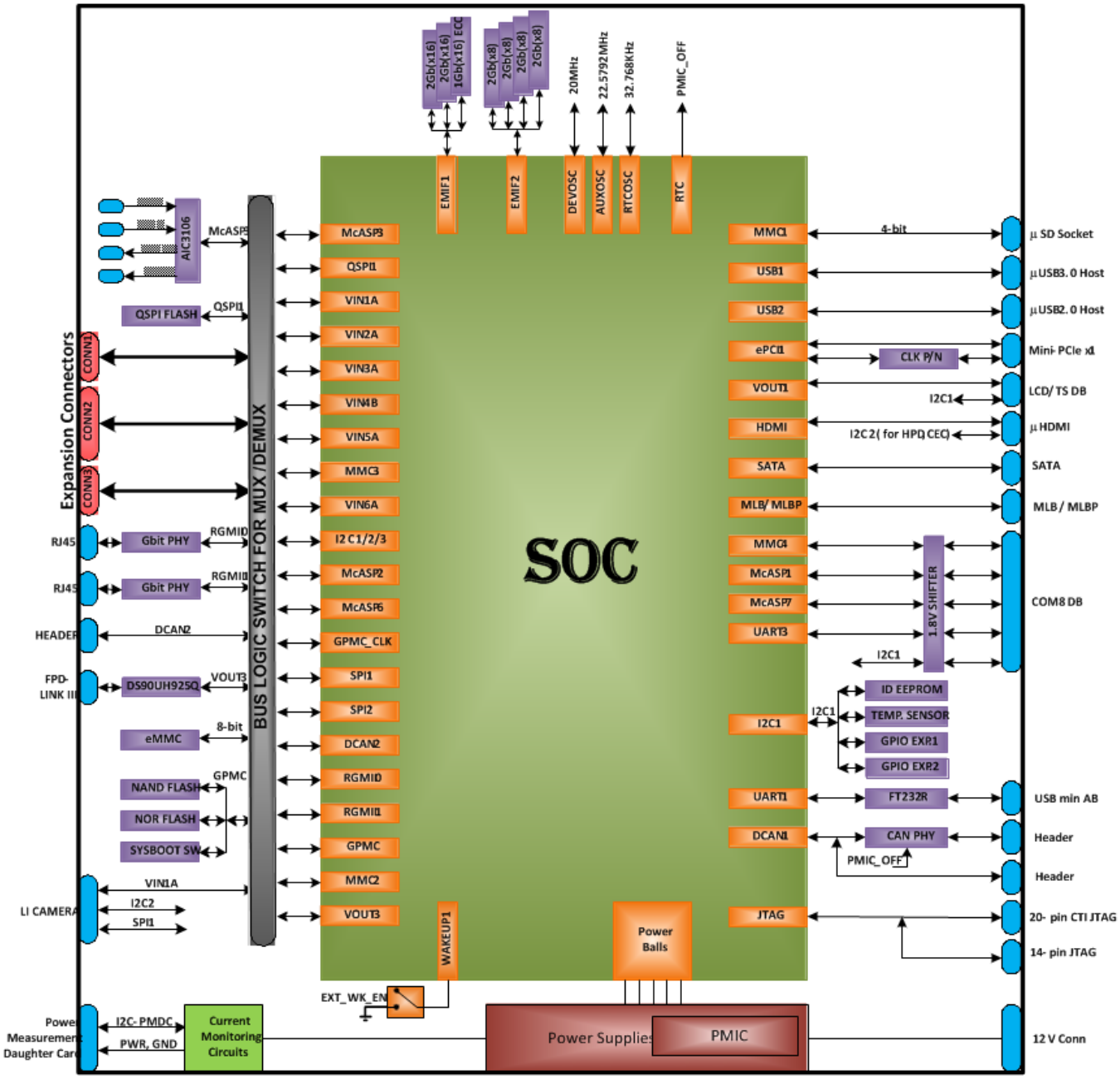


Figure 2. CPU Board Block Diagram

3.2 Reset Structure

The CPU board has two push buttons for reset:

- Power ON reset (PORz) (or cold reset for complete system reset)
- Warm reset (RESETn)

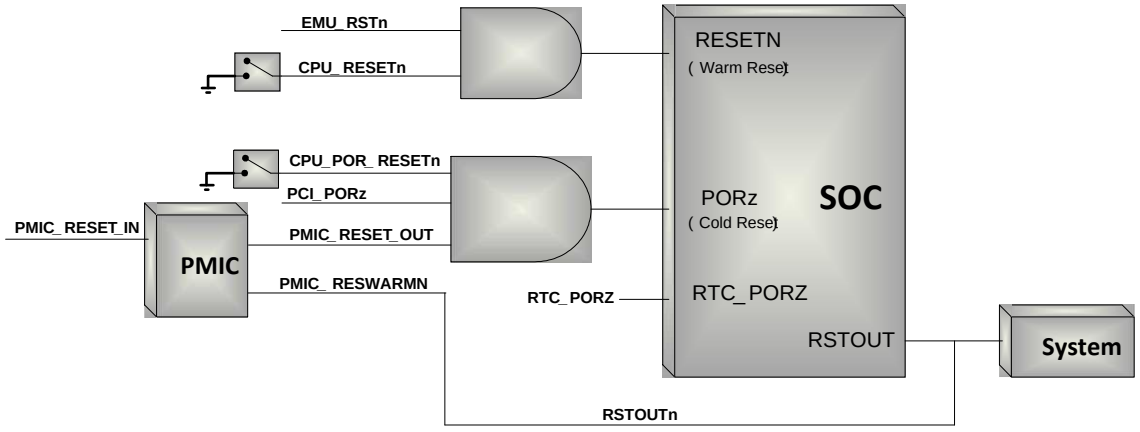


Figure 3. Reset Structure

Table 8 summarizes the reset signals.

Table 8. Reset signals structure

Reset Type	Reset Signal Sources	Comments
Power-On Reset Input (as whole system reset)	CPU_POR_RESETn	PORn push button reset
	PCI_PORz	PCIe inbound reset
	PMIC_RESET_OUT	Power on reset from PMIC
Warm Reset Input	CPU_RESETn	Warm push button reset
	EMU_RSTn	Reset from Emulator
PMIC Power-On Reset Input	PMIC_RESET_IN	PMIC Power on reset input
RTC Power-On Reset Input	RTC_PORZ	RTC block power on reset
Reset Output	RSTOUTn	Reset output from processor to system
	APP_BD_PORz	Reset to expansion connector
	PMIC_NRESWARM	Warm Reset input to PMIC

3.2.1 Wakeup Signals

Wakeup0 is connected to on-board CAN transceiver, and is used for multi-function. Under normal operating modes, the pin can be configured/used as DCAN receive input. When placed in RTC sleep mode, the pin can be configured as to trigger wakeup events from CAN bus.

Wakeup 1 is connected to PMIC, and is used for multi-function. Under normal operating modes, the pin can be configured as input to receive interrupt events from PMIC. When placed in RTC sleep mode, the pin can be configured as to trigger wakeup events from PMIC.

Wakeup 2 is connected to both LCD and expansion connectors. Under normal operation modes, the pin is configured as input to receive interrupts from LCD touch panel controller.

Wakeup 3 is connected to expansion connector, and can be used as either wakeup event or general purpose input.

NOTE: ES1.0 Rev E system and older supported an on-board pushbutton to generate wakeup event. Depending on revision, the button was connected to either Wakeup1 or Wakeup2.

3.3 Boot Modes

Multiple boot modes are supported as determined by the 16-bit “system boot” setting present on the shared specific I/O balls during power-on sequence. For more information, see the device-specific technical reference manual (TRM). These shared I/O resources can be “redeployed” to support alternate interfaces after boot-up by changing of the on-die mux mode settings per I/O and configuring CPU board’s on-board bus logic switches. Boot mode selection is accomplished by the setting of DIP switches SW2 and SW3 as shown in Table 9.

Table 9. SYS_Boot Switch Settings

Interface (Internal System Boot Input)	CPU Bd Net	DIP Switch Ref Des Position No Connections	Factory Settings
GPMC_AD0 (sysboot0)	GPMC_D00	SW2.P1	ON
GPMC_AD1 (sysboot1)	GPMC_D01	SW2.P2	OFF
GPMC_AD2 (sysboot2)	GPMC_D02	SW2.P3	ON
GPMC_AD3 (sysboot3)	GPMC_D03	SW2.P4	OFF
GPMC_AD4 (sysboot4)	GPMC_D04	SW2.P5	ON
GPMC_AD5 (sysboot5)	GPMC_D05	SW2.P6	OFF
GPMC_AD6 (sysboot6)	GPMC_D06	SW2.P7	OFF
GPMC_AD7 (sysboot7)	GPMC_D07	SW2.P8	OFF
GPMC_AD8 (sysboot8)	GPMC_D08	SW3.P1	OFF
GPMC_AD9 (sysboot9)	GPMC_D09	SW3.P2	OFF
GPMC_AD10 (sysboot10)	GPMC_D10	SW3.P3	OFF
GPMC_AD11 (sysboot11)	GPMC_D11	SW3.P4	OFF
GPMC_AD12 (sysboot12)	GPMC_D12	SW3.P5	OFF
GPMC_AD13 (sysboot13)	GPMC_D13	SW3.P6	OFF
GPMC_AD14 (sysboot14)	GPMC_D14	SW3.P7	OFF
GPMC_AD15 (sysboot15)	GPMC_D15	SW3.P8	OFF

3.3.1 On-Board Boot Routing Control

CPU board has external, on-board multiplexing bus logic switches to enhance the flexibility of the EVM. Multiplexing options on-board should be selected accordingly to the desired boot mode to enable interface paths required to access desired boot devices or port. DIP Switch SW5 has 10 individual SPST positions. Positions 1-5 have been used to control board signal routing for booting. Positions 6-10 have been used to control other CPU board signaling paths and modes of operation.

SW5 DIP switches connect nets to strong (1k) pull-down resistors to ground when a switch is set to the “ON” position, corresponding to a “Low” logic level signal. Alternatively, when switch is in the “OFF” position, a 10k pull-up connects it to 3.3 V rail, corresponding to a “High” logic level signal.

Table 10. Board Controls for Booting Options

Signals	Description	DIP Switch	Factory Settings	I2C1 GPIO Expander
NAND_BOOTn (1)	Low = Enable GPMC_nCS0 for NAND flash boot	SW5.1	OFF	U57.P10
NOR_BOOTn (2)	Low = Enable GPMC_nCS0 for NOR flash boot	SW5.2	OFF	U57.P11
MMC2_BOOT	Low = Enable MMC2 Interface for eMMC flash boot	SW5.3	OFF	U57.P12
QSPI_BOOT	Low = Enable QSPI1 Interface for QSPI flash boot	SW5.4	OFF	U57.P13
UART_SEL1_3	High = UART3 Interface for UART boot is enabled	SW5.5	ON	U57.P14

(1) Routing control for GPMC_nCS0 is “shared” between NOR & NAND Flash memories. Ensure that only one DIP switch, SW5.P1 or SW5.P2, is ever set to “ON” state at any one time so that GMPC_nCS0 is only connected to one memory. Failure to adhere to this requirement causes NOR & NAND memory data bus contention.

(2) GPIO Expander (U57) connections to “Board Signal” nets are intended to provide a “read-only” feature to determine boot image source (NOR or NAND). Boot image selection must be set before power on sequence by setting DIP Switches SW2 and SW3 along with SW5.P1 and .P2 appropriately, as shown above.

Table 11. Board Controls for Signaling and Operational Modes

Signals	Description	DIP Switch	Factory Settings	I2C1 GPIO Expander
MCASP1_ENn	Low = Enable COMx signal paths	SW5.6	OFF	U57.P15
FORCE_EMU	Always set low	SW5.7	OFF	U57.P17
PCI_RESET_SEL	High = PCIe device may reset Low = May reset the PCIe device	SW5.8	OFF	NA
GPMC_WPN	Low = Enable write protection of NAND Flash	SW5.9	OFF	NA
I2C_EEPROM_WP	High = Enable write protection of Board identification EEPROM	SW5.10	OFF	NA
PMIC_BOOT1	Low = Always, pull-down resistor	NA	NA	NA
PMIC_BOOT0 (Rev E and older only)	ON = High = Double Reset Pulse Mode OFF = Low = Power-up seq and voltages (Single reset pulse)	SW8.1	ON	NA
PMIC_BOOT0 (Rev G+ Board only)	ON = Low = Power-up seq and voltages (Single reset pulse) OFF = High = Double Reset Pulse Mode	SW8.1	ON	NA
GPIO_PWR_MUX (Rev E and older only)	ON = High = Connect PMIC GPIOs as follows: • GPIO_4 = EVM_3V3_SW power load switch enable • GPIO_6 = 1V35_DDR power converter enable OFF = Low = Connect PMIC GPIOs as follows: • GPIO_4 = 1V35_DDR power converter enable • GPIO_6 = EVM_3V3_SW power load switch enable	SW8.2	OFF	NA
AIC _I2C_ ADDR_CTL (SW8.2 reused in Rev G+, boards for AIC I2C address selection)	ON = High = i2C – 0X19 (for AIC operation with 10.1” display support) OFF = Low = I2C=0X18 (for AIC operation with 7” display support)	SW8.2	ON	NA

Figure 4. CPU Board Switch and Button Locations (Rev E and earlier)

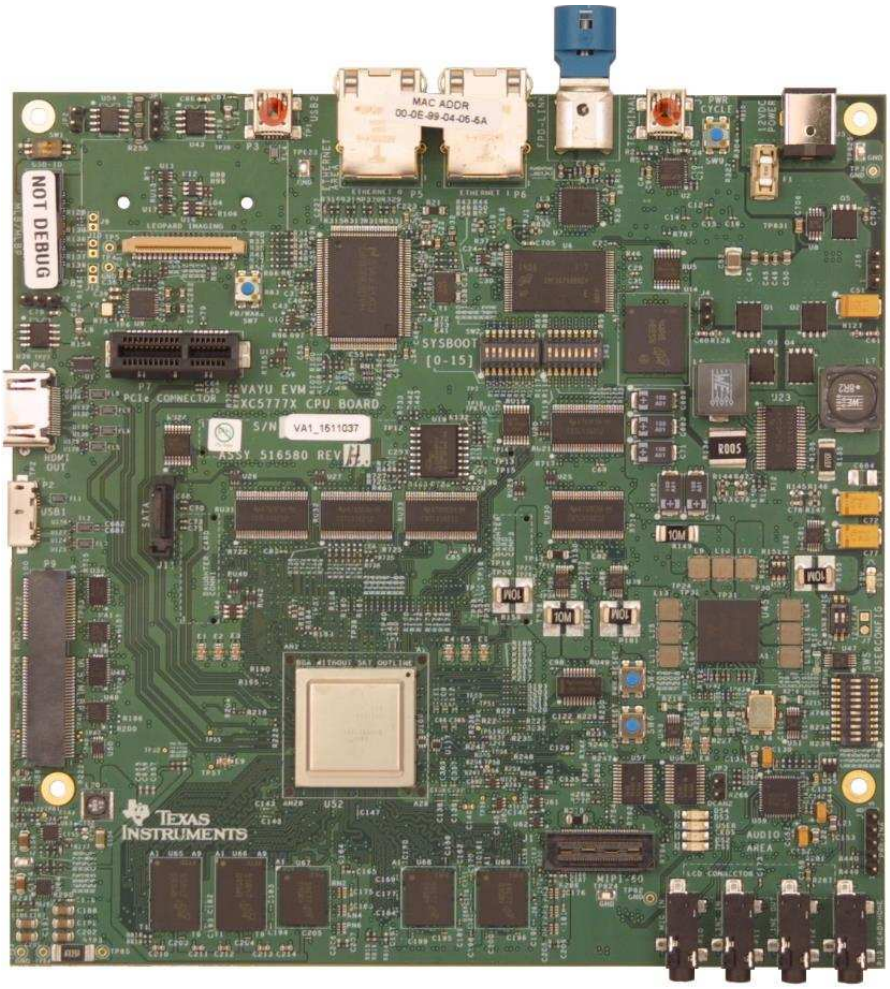


Figure 5. CPU Board Switch and Button Locations (Rev G and later)

3.4 Signal Multiplex Logic

A high level of internal I/O signal multiplexing is supported to maximize silicon functionality available at package balls. Likewise, the CPU board design uses a combination of FET switch and passive resistor multiplexers to route the signals to different functional blocks or peripheral components to maximize development platform system functionality. The following sections and diagrams will illustrate the flexibility of the on-die and CPU's on-board signal multiplexing options.

3.4.1 NOR/NAND Booting vs FPD-Link Video

A high level of internal I/O signal multiplexing is supported to maximize silicon functionality available at the package balls. Likewise, the CPU board design uses a combination of FET switch and passive resistor multiplexers to route the signals to different functional blocks or peripheral components to maximize development platform system functionality. The following sections and diagrams illustrate the flexibility of the on-die and CPU's on-board signal multiplexing options.

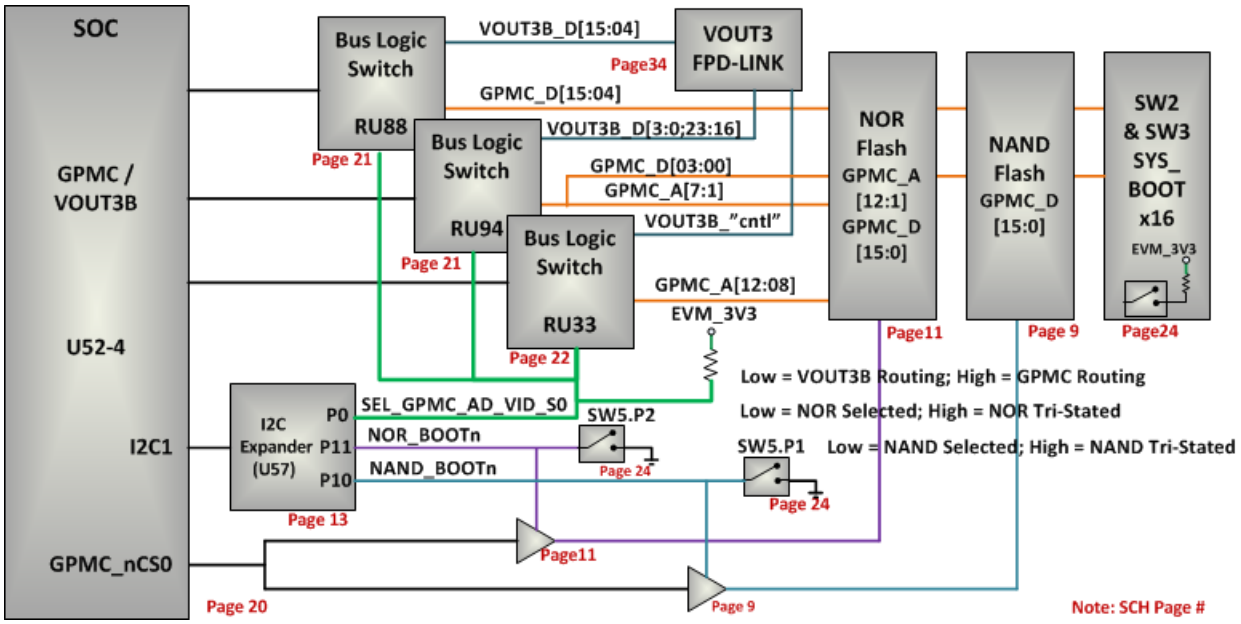


Figure 6. NOR/NAND Booting vs FPD-Link Video Multiplexing

Table 12. NOR/NAND Booting vs FPD-Link Video Mux Control

Interface	NOR_BOOTn (1), (2)	NAND_BOOTn (1), (2)	SEL_GPMC_AD_VID_S0 (3), (4), (5)	Device
GPMC_AD and GPMC_nCS0	Low (SW5.P2 = ON) High (SW5.P2 = OFF)	High (SW5.P1 = OFF) Low (SW5.P1 = ON)	High	NOR Flash NAND Flash
VOUT3B	NA	NA	Low	FPD-Link

(1) Routing control for GPMC_nCS0 is “shared” between NOR and NAND Flash memories. Ensure that only one DIP switch, SW5.P1 or SW5.P2, is ever set to “ON” state at any one time so that GMPC_nCS0 is only connected to one memory. Failure to adhere to this requirement will cause NOR & NAND memory data bus contention.

(2) GPIO Expander (U57) connections to “Board Signal” nets are intended to provide a “read-only” feature to determine boot image source NOR or NAND). Boot image selection must be set before power on sequence by setting DIP Switches SW2 and SW3 along with SW5.P1 and .P2 appropriately, as shown above.

(3) Bus Logic Switch select input S1 is the inversion of select input S0 connected to SEL_GPMC_AD_VID_S0 net controlled via GPIO Expander U57.P0.

(4) Bus Logic Switches (RU33, 88 and 94) power-up with S0 = High via pull-up resistor resulting in GPMC_AD bus routed to memories (S1, S0 = 0, 1).

(5) GPIO Expander (U57) is accessible via I2C1, address 0x21.

3.4.2 QSPI vs NOR Flash Booting

The CPU can be booted from either a QSPI or NOR Flash memory component. The memory interface signals are routed through a “Resistor Bypass Path” for optimal QSPI signal integrity (SI) or “Bus Logic Switch Path” for flexible boot image selection. The source and load “muxing resistors” that enable the “Resistor Bypass Path” have been installed on CPU boards as the default configuration for QSPI booting with optimal SI. As a consequence, six of the upper GMPC address signals (A13 – A18) are not connected to the NOR Flash memory due to source muxing resistors being “No-Mount” on the “Bus Logic Switch Path”. This limits the addressable NOR memory to an 8KByte range (A0-A12) due to default mux resistor mounting. The “resistor muxing” option would need to change to route the GPMC signals via “Bus Logic Switch Path” to the NOR Flash memory in order to access the full addressable range of the NOR memory.

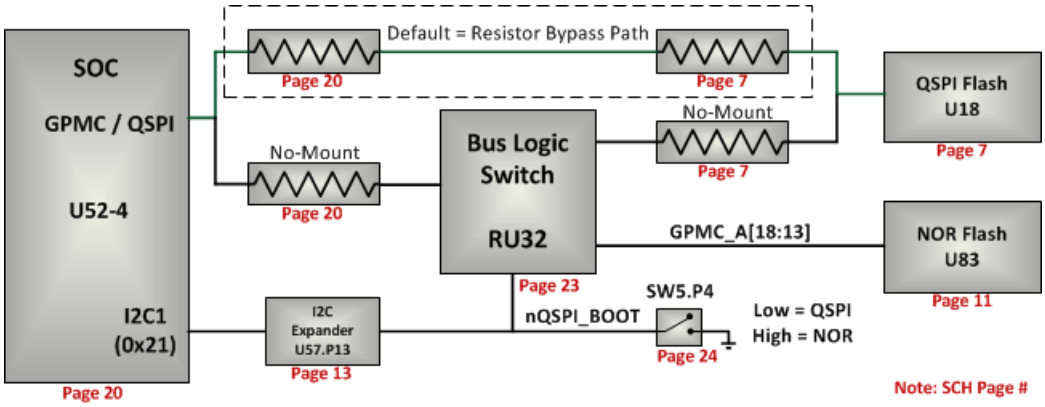


Figure 7. QSPI vs Full Address NOR Flash Multiplexing

Table 13. QSPI vs Full Address NOR Flash Booting Mux Control

Interface	Muxing Resistors Mounted	Muxing Resistors "Not-Mounted"	Signal Path	QSPI_BOOT (3), (4)	Device
QSPI	R735, R737, R739, R741,R743, R745, R747	R736, R738, R740, R742, R744, R746, R748	Resistor Bypass (1)	NA	QSPI Flash
GPMC QSPI	R736, R738, R740, R742, R744, R746, R748	R735, R737, R739, R741, R743, R745, R747	Bus Switch (2)	Low (SW5.P4 = ON) High (SW5.P4 = OFF)	QSPI Flash NOR Flash

(1) Best PCB Signal Integrity (SI) routing is default configuration via Resistor Bypass Path for QSPI signaling.

(2) Most flexible routing is optional configuration via Bus Logic Switch pending SI validation for QSPI signaling.

(3) GPIO Expander (U57) connection to "nQSPI_BOOT" net is intended as a "read-only" feature to determine boot image source (QSPI or NOR). Boot image selection must be set before power on sequence.

(4) GPIO Expander (U57) is accessible via I2C1, address 0x21.

3.4.3 GPMC Vs MMC2

Multiplex control logic for GPMC and MMC2 is shown in Figure 8.

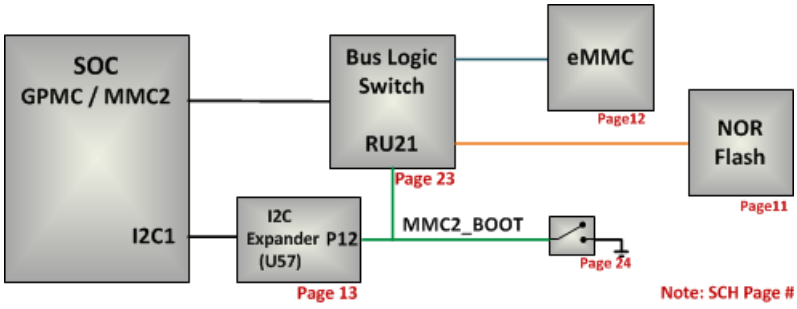


Figure 8. GPMC and MMC2 Multiplexing

The default interface are the GPMC signals; the selection table is shown in Table 14.

Table 14. GPMC and MMC2 Selection Table

GPMC vs MMC2	MMC2_BOOT	Interface	Device
GPMC/MMC2	1	GPMC	NOR Flash
	0	MMC2	eMMC

Use Bit “P12” in the I2C IO Expander (U57) with slave address 0x0100 0010(Write) to control, signal "MMC2_BOOT". A DIP switch is also available to control the MMC2_BOOT signal for boot mode configuration.

3.4.4 VIN1A Vs LI Camera

VIN1A signal group can be switch between on-board LI Imager and expansion connector as shown in Figure 9.

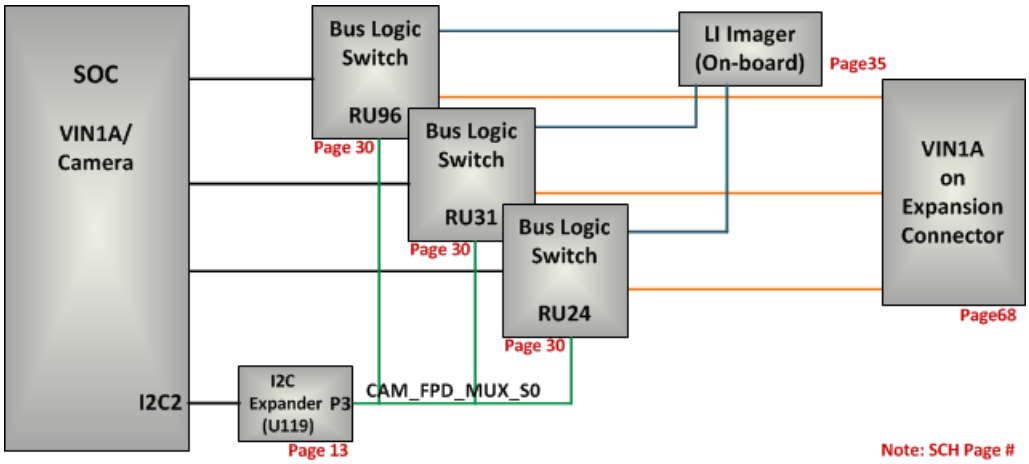


Figure 9. VIN1A and LI Camera Multiplexing

The default interface is VIN1A interface to expansion connectors and the selection table is shown in Table 15.

Table 15. VIN1A Selection Table

VIN1A vs LI Camera	CAM_FPD_MUX_S0	Interface	Device
VIN1A	1	VIN1A	Expansion Connector
	0	VIN1A	LI-CAMERA

Use Bit “P3” in the I2C IO Expander(U119) with slave address 0x0100 0100(Write) to control, signal "CAM_FPD_MUX_S0".

3.4.5 VIN2A Vs RGMII1

Multiplex control logic for VIN2A and RGMII1 is shown in Figure 10.

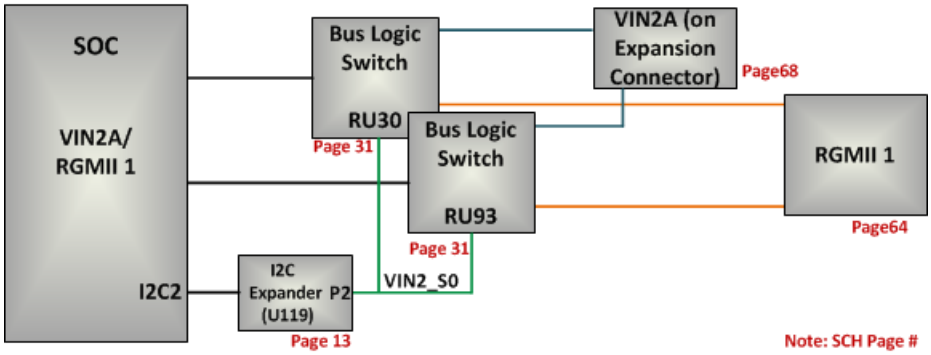


Figure 10. VIN2A and RGMII1 Multiplexing

The default interface is RGMII1 and the selection table is shown in Table 16.

Table 16. VIN2A and RGMII1 Selection Table

VIN2A vs RGMII1	VIN2_S0	Interface	Device
VIN2A/RGMII1	1	RGMII1	Gbit Ethernet PHY
	0	VIN2A	Expansion Connector

Use bit “P2” in I2C IO Expander (U119) with slave address 0x0100 0100(Write) to control, signal "VIN2_S0".

3.4.6 VIN5A Vs MLB

VIN5A or MLB can be selected through the resistor mounting options available on board as shown in Figure 11.

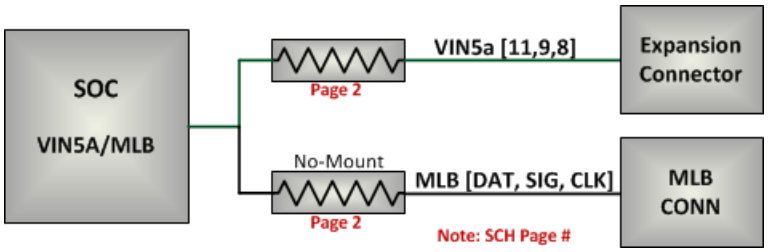


Figure 11. VIN5A and MLB Multiplexing

The default interface is VIN5A to the expansion connector. The selection table is shown in Table 17.

Table 17. VIN5A and MLB Selection Table

VIN5A vs MLB	Mount	No Mount	Interface	Device
VIN5A and MLB	R538, R526, R525	R541, R527, R177	VIN5A	Expansion Connector
	R541, R527, R177	0R538, R526, R525	MLB Interface	MLB Conn

3.4.7 VIN4B vs RGMII0

Multiplex control logic for VIN4B and RGMII0.

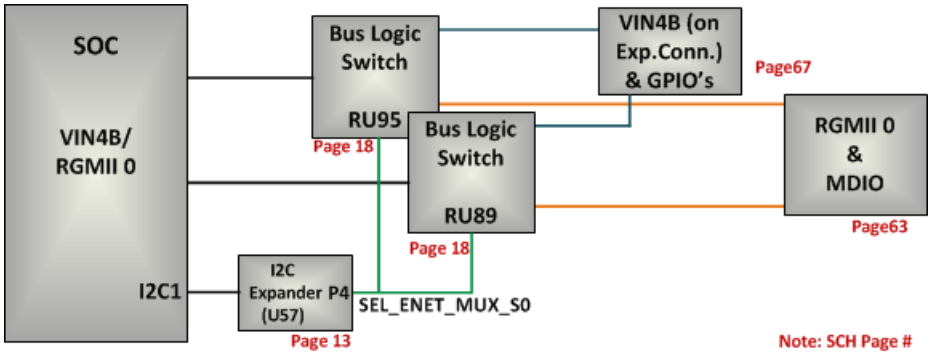


Figure 12. VIN4B and RGMII0 Multiplexing

Table 18. VIN4B and RGMII0 Selection Table

VIN4B vs RGMII0	SEL_ENET_MUX_S0	Interface	Device
VIN4B and RGMII0	1	RGMII0	Gbit Ethernet PHY
	0	VIN4B/GPIO's	Expansion Connector

Use Bit “P4” in I2C IO Expander (U57) with slave address 0x0100 0010(Write) to control, signal "SEL_ENET_MUX_S0".

3.4.8 VIN6A Vs McASP1, 2, 3 and 7

Multiplex control logic for VIN6A and McASP1, 2, 3 and 7.

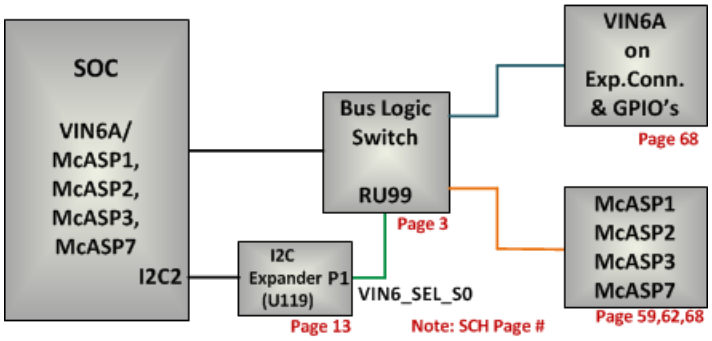


Figure 13. VIN6A and McASP1, 2, 3 and 7 Multiplexing

The default interface is VIN6A to the expansion connector and the selection table is shown in Table 19.

Table 19. VIN6A and McASP1, 2, 3 and 7 Selection Table

VIN6A vs McASP1,2,3 and 7	VIN6_SEL_S0	Interface	Device
VIN6A/McASP1,2,3 and 7	1	VIN6A	Expansion Connector
	0	McASP1,2,3 and 7	TLV320AIC3106, COM8 Conn, Exp.Conn.

Use Bit “P1” in I2C IO Expander (U119) with slave address 0x0100 0100(Write) to control, signal "VIN6_SEL_S0".

3.4.9 UART3 Vs SPI[2]

Multiplex control logic for UART3 and SPI[2].

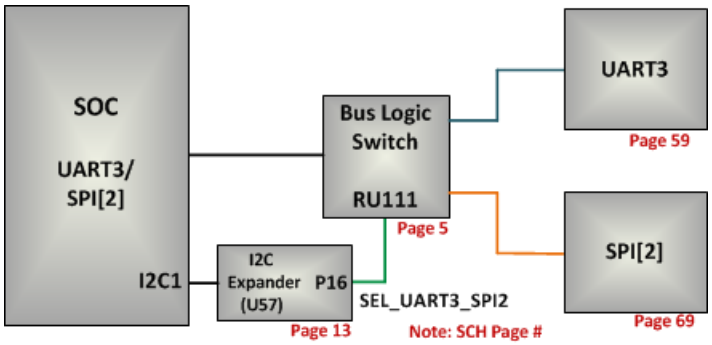


Figure 14. UART3 and SPI[2] Multiplexing

The default interface is UART3 and the selection table is shown in Table 20.

Table 20. UART3 and SPI[2] Selection Table

UART3 vs SPI[2]	CAM_FPD_MUX_S0	Interface	Device
UART3 and SPI[2]	1	SPI[2]	Expansion Connector
	0	UART3	FTDI UART and COM8 Conn

Use Bit “P16” in I2C IO Expander (U57) with slave address 0x0100 0010(Write) to control, signal "SEL_UART3_SPI2".

3.4.10 UART1 vs UART3

Upon selection of UART3, it has been multiplexed with UART1 and then connected to FT232RQ UART to the USB converter for the USB console. GPIO expander selection can be override by available manual switch on board. The corresponding image is shown in Figure 15 and the UART1 vs UART3 selection table is shown in Table 21.

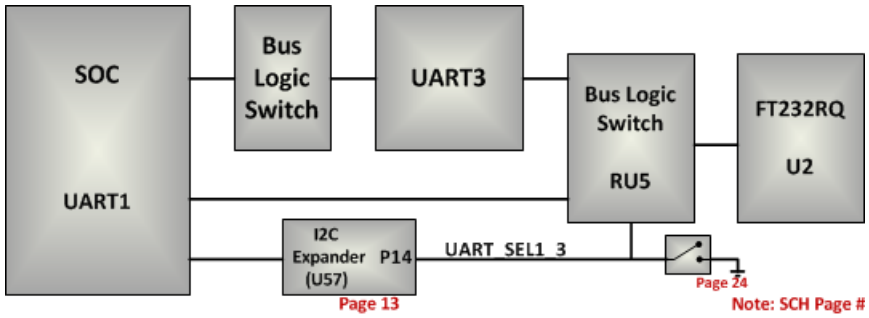


Figure 15. UART1 vs UART3 Multiplexing

Table 21. UART1 vs UART3 Selection Table

UART1 vs UART3	UART_SEL1_3	Interface	Device
UART3 and SPI[2]	1	UART3	FT232RQ
	0	UART1	

Use bit “P14” in I2C IO Expander (U57) with slave address 0x0100 0010(Write) to control, signal "UART_SEL1_3". A DIP switch is also available to control the UART_SEL1_3 signal for boot mode configuration.

3.4.11 I2C2 Vs HDMI

Multiplex control logic for I2C2 and HDMI.

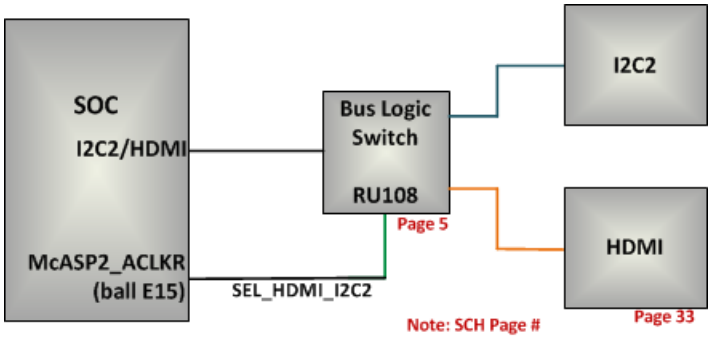


Figure 16. I2C2 Vs HDMI Multiplexing

The default interface is I2C2 interface and the I2C2 Vs HDMI selection table is shown in Table 22.

Table 22. I2C2 vs HDMI Selection Table

I2C2 vs HDMI	SEL_HDMI_I2C2	Interface	Device
I2C2and HDMI	1	HDMI	HDMI DDC and Signals
	0	I2C2	GPIO Expander, FPD-Link, LI Camera, Exp. Conn.

Use McASP2_ACLKR (ball E15) to control signal “SEL_HDMI_I2C2”.

3.4.12 I2C3 vs DCAN2

Multiplex control logic for I2C3 and DCAN.

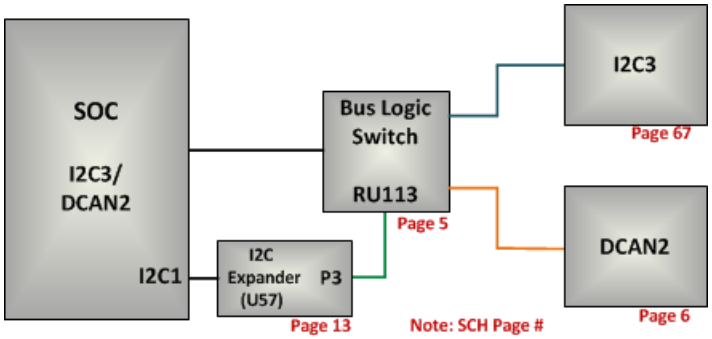


Figure 17. I2C3 vs DCAN2 Multiplexing

The default interface is I2C3 interface and the I2C3 vs DCAN2 selection table is shown in Table 23.

Table 23. I2C3 vs DCAN2 Selection Table

I2C3 vs DCAN2	SEL_I2C3_CAN2	Interface	Device
I2C3 and DCAN2	1	DCAN2	Header
	0	I2C3	Expansion Connector

Use bit “P3” in I2C IO Expander (U57) with slave address 0x0100 0010(Write) to control, signal "SEL_I2C3_CAN2".

3.5 I2C Interface

Table 24 shows the list of I2C interface available with the list of devices connected in each I2C interface and its corresponding device address.

Table 24. I2C Device Address Chart

CPU Board	Part No	Ref. Des	I2C1	I2C2	I2C3	Device Address(7b)
EEPROM	24WC256	U105	X			0x50
Digital Temperature Sensor	TMP102AIDRLT	U117	X			0x48
Digital Temperature Sensor	TMP102AIDRLT	U109	X			Either U117 or U109 will be mounted on board
GPIO Expander	PCF8575	U58	X			0x20
GPIO Expander	PCF8575	U57	X			0x21
MLB Connector	Connector	P8	X			NA
LCD Interface	Connector	J15	X			NA

Table 24. I2C Device Address Chart (continued)

CPU Board	Part No	Ref. Des	I2C1	I2C2	I2C3	Device Address(7b)
COM8 Connector	Connector	P9	X			NA
Audio Codec	TLV320AIC3106	U59	X			0x18 or 0X19 (1)
Expansion Connector	Connector	EXP_P2	X			NA
PMIC	TPS659039 - DVS	U45	X			0x12
	TPS659039 - Power	U45	X			0x58
	TPS659039 - Interfaces	U45	X			0x59
	TPS659039 - Trimming	U45	X			0x5A
	TPS659039 - OTP	U45	X			0x5B
GPIO Expander	PCF8575	U119		X		0x26
FPD Link	DS90UH925Q	U3		X		0x1B
LI Camera	Connector	J5		X		NA
Expansion Connector	Connector	EXP_P3		X		NA
HDMI DDC	Connector	P4		X		NA
Expansion Connector	Connector	EXP_P1			X	NA

1. 0X18 on Rev E boards and older. On Rev G boards and later, I2C address is switchable (SW8.P2). Need 0X18 on AIC when using 7” display and 0X19 when using 10.1” display.

3.5.1 I2C GPIO Expander IO List

Table 25. GPIO Expander IO Chart

Ref. Des	Slave Address	I2C I/F	Expander IO	Netname	Description
U58	0b0010 000 (0x20)	I2C1	INT#	PCF8575_INT	Interrupt output
			P0	TS_LCD_GPIO1	Press Button Switch 1
			P1	TS_LCD_GPIO2	Press Button Switch 2
			P2	TS_LCD_GPIO3	Press Button Switch 3
			P3	TS_LCD_GPIO4	Press Button Switch 4
			P4	USER_LED1	User LED 1
			P5	USER_LED2	User LED 2
			P6	USER_LED3	User LED 3
			P7	USER_LED4	User LED 4
			P10	EXP_ETH0_RSTn	RGMII0 Reset
			P11	EXP_ETH1_RSTn	RGMII1 Reset
			P12	USB1-VBUS_OCN	USB1 Over Current Indication
			P13	USB2-VBUS_OCN	USB2 Over Current Indication
			P14	PCI_SW_RESETn	PCI Interface SW Reset
			P15	CON_LCD_PWR_DN	LCD Board Master power enable
			P16	NC	No Connection
			P17	TMP102_ALERT	Digital Temp. sensor Altert signal

Table 25. GPIO Expander IO Chart (continued)

Ref. Des	Slave Address	I2C I/F	Expander IO	Netname	Description
U57 (0x21)	0b0010 001	I2C1	INT#	NC	No Connection (Rev D and earlier)
			INT#	PCF8575_INT	Interrupt output (Rev E and later only)
			P0	SEL_GPMC_AD_VID_S0	MUX out control signal for GPMC Vs VOUT3B
			P1	USB1_ID	USB1 ID PIN
			P2	USB2_ID	USB2 ID PIN
			P3	SEL_I2C3_CAN2	MUX out control signal for I2C3 Vs DCAN2
			P4	SEL_ENET_MUX_S0	MUX out control signal for RGMII0 Vs VIN4B
			P5	MMC_PWR_ON	Power on MMC
			P6	NC	No Connection
			P7	NC	No Connection
			P10	NAND_BOOTn	NAND boot Chip select enable signal
			P11	NOR_BOOTn	NOR boot Chip select enable signal
			P12	MMC2_BOOT	MUX out control signal for GPMC Vs MMC2
			P13	QSPI_BOOT	MUX out control signal for GPMC Vs QSPI1
			P14	UART_SEL1_3	MUX out control signal for UART1 Vs UART3
			P15	MCASP1_ENn	COM8 interface level shifter enable signal
			P16	SEL_UART3_SPI2	MUX out control signal for UART3 Vs SPI2
			P17	FORCE_EMU	MUX out control signal for EMU signals

Table 25. GPIO Expander IO Chart (continued)

Ref. Des	Slave Address	I2C I/F	Expander IO	Netname	Description
U119 (0x26)	0b0010 010	I2C2	P0	(***DO NOT USE)	Cannot revert back to I2C2 after selecting HDMI ***DO NOT USE. McASP2_ACLKR replaces this signal. Drive McASP2_ACLKR (in McASP GPIO mode) as the SEL_HDMI_I2C2 signal.
			P1	VIN6_SEL_S0	MUX out control signal for VIN6A and McASPx
			P2	VIN2_S0	MUX out control signal for EMAC1 and VIN2A Signals
			P3	CAM_FPD_MUX_S0	MUX out control signal for VIN1A & LI Camera Signals
			P4	HDMI_CT_HPD	HDMI Hot Plug Detect
			P5	HDMI_LS_OE	HDMI Level Shifter Enable
			P6	NC	No Connection
			P7	NC	No Connection
			P10	NC	No Connection
			P11	NC	No Connection
			P12	NC	No Connection
			P13	NC	No Connection
			P14	NC	No Connection(Rev E and earlier)
			P15	NC	No Connection(Rev E and earlier)
			P16	NC	No Connection(Rev E and earlier)
			P17	NC	No Connection(Rev E and earlier)
			P14	MMC2_BOOT_OVR_OEN	MMC2 DIP Switch Override Enable(Rev G)
			P15	MMC2_BOOT_OVR	MMC2 DIP Switch Override (Rev G)
			P16	NOR_BOOT_OVR_OEN	NOR BOOT DIP Switch Override Enable (Rev G)
			P17	NOR_BOOT_OVR	NOR BOOT DIP Switch Override (Rev G)

3.5.2 User Interface LED's

The board has four user interface LEDs for debug, status indication and so on. Details about the user interface LED and its GPIO assignment is shown in Table 25.

3.5.3 Configuration EEPROM

The CPU board contains an EEPROM memory device for storing and retrieving configuration information. The EEPROM provides 256Kb (or 32KBytes) of storage space, and is accessible via I2. Device location information is located in Table 24. The configuration ID information is programmed by the factory at time of manufacturing, and should not be altered. Table 26 shows the configuration data format within the EEPROM.

Table 26. Configuration EEPROM Definition Table

EEPROM Field	Byte Location	Value (Rev H CPU board example)	Description
ID.HEADER	[3:0]	0xAA5533EE	Fixed value at start of header ID.
ID.BOARD_NAME	[19:4]	'5777xCPU-DDR3' (ascii)	Fixed value of '5777xCPU' or '5777xCPU-DDR3'
ID.VERSION_MAJOR	[21:20]	0x7	A=0x1 B=0x2 C=0x3 D=0x4 E=0x5 F Skipped G=0x6 H=0x7
ID.VERSION_MINOR	[23:22]	0x0	0x0 for major revision 0x1-0x15 for others
ID.CONFIG_OPTION	[27:24]	0x3E	Bit 6: 1 – EMIF2 ECC Supported, 0 - No Bit 5: 1 – EMIF2 Supported, 0 – No Bit 4: 1 – EMIF1 ECC Supported, 0 – No Bit 3: 1 – EMIF1 Supported, 0 – No Bit 2: 1 – Extended Memory EEPROM Cfg Support, 0 – No (1) Bit 1: 1 – MAC addr in EEPROM (default) Bit 0: 0 - QSPI (default), 1 - NOR
EMIF1_SIZE_BYTES	[31:28]	0x8000 0000	Memory size for EMIF1 in bytes (unsigned long) (2)
EMIF2_SIZE_BYTES	[35:32]	0x8000 0000	Memory size for EMIF2 in bytes (unsigned long) (2)
RESERVED	[55:36]	0x0	Reserved (2)
MAC_ADDR	0x7F00	00.0E.99.zz.yy.xx	Optional MAC address

(1) If Bit 2 is set to 0, all EEPROM data beyond that is set to 0 (Not defined or Used). If set to 1, the mapping is per the table.

(2) Prior to Rev H, Bytes [55:28] were reserved and set to 0x0.

For reference, a C-style coded structure is provided:

```
Struct EEPROM_ID_T
{
    Unsigned long header;             4
    Char board_name[16];              16
    Unsigned short version_major;     2
    Unsigned short version_minor;     2
    Unsigned long config_option;      4
    Unsigned long emif1_size_bytes;   4
    Unsigned long emif2_size_bytes;   4
    Char reserved[28];                20
} eeprom_id;
                                      56 Bytes
```

3.6 GPIO List

Table 27 shows the GPIO lists.

Table 27. GPIO List (1)

Function	Peripheral Device	CPU Bd Net (I/F Component Des.Pin)	Intermediate Net	GPIO / Sym Ball Name (ball no.)
Application Board	Expansion Connector	GP5[0] (EXP_P2.34)	NA	GPIO5_0 MCASP1_ACLKR (B14)
Application Board	Expansion Connector	GP5[1] (EXP_P2.36)	NA	GPIO5_1 MCASP1_FSR (J14)
Connectivity on Module	COM8 Connector	GP5[4] (P9.89)	BT_EN	GPIO5_4 MCASP1_AXR2 (G13)
Connectivity on Module	COM8 Connector	GP5[5] (P9.50)	GPS_PPS_OUT	GPIO5_5 MCASP1_AXR3 (J11)
Connectivity on Module	COM8 Connector	GP5[6] (P9.48)	GPS_TIME_STAMP	GPIO5_6 MCASP1_AXR4 (E12)
Connectivity on Module	COM8 Connector	GP5[7] (P9.34)	WLAN_IRQ	GPIO5_7 MCASP1_AXR5 (F13)
Connectivity on Module	COM8 Connector	GP5[8] (P9.4)	WL_EN	GPIO5_8 MCASP1_AXR6 (C12)
Media Local Bus(MLB)	MLB Connector	GP5[9] (P8.34)	NA	GPIO5_9 MCASP1_AXR7 (D12)
I2C GPIO Expander	PCF8575	PCF8575_INT (U58.1) Rev D and earlier (U57.1 and U58.1) Rev E and later	NA	GPIO6_11 (AB4)
I2C2/HDMI	I2C2 bus, HDMI HPD/CEC	SEL_HDMI_I2C2	NA	MCASP2_ACLK (use as McASP GPIO)
Interrupt	Ethernet PHY	ENET_INTSn (U15.4)	NA	GPIO6_16 (F21)
Media Local Bus(MLB)	MLB Connector	GP6_[28] (P8.24)	NA	GPIO6_28 MMC1_SDWP (Y9)
Application Board	Expansion Connector	GP5[17] (EXP_P2.32)	NA	RMII_MHZ_50_CLK GPIO5_17 (U3)
Application Board	Expansion Connector	GP5[31] (EXP_P1.38)	C_EMAC[0]_RXD0	RGMII0_RXD0 GPIO5_31 (W2)
Application Board	Expansion Connector	GP5[30] (EXP_P1.36)	C_EMAC[0]_RXD1	RGMII0_RXD1 GPIO5_30 (Y2)
Application Board	Expansion Connector	GP5[29] (EXP_P1.34)	C_EMAC[0]_RXD2	RGMII0_RXD2 GPIO5_29 (V3)
Application Board	Expansion Connector	GP5[25] (EXP_P1.35)	C_EMAC[0]_TXD0	RGMII0_TXD0 GPIO5_25 (U6)
Application Board	Expansion Connector	GP5[22] (EXP_P1.33)	C_EMAC[0]_TXD3	RGMII0_TXD3 GPIO5_22 (V7)
Application Board	Expansion Connector	GP2[27] (EXP_P2.108)	NA	GPMC_BEN1 GPIO2_27 (M4)

Table 27. GPIO List (1) (continued)

Function	Peripheral Device	CPU Bd Net (I/F Component Des.Pin)	Intermediate Net	GPIO / Sym Ball Name (ball no.)
Application Board	Expansion Connector	GP6[17] (EXP_P1.15)	NA	XREF_CLK0 GPIO6_17 (D18)
Application Board	Expansion Connector	GP6[20] (EXP_P3.13)	NA	XREF_CLK3 GPIO6_20 (C23)
Interrupt	PMIC	PMIC_INT (U45.PK1)	NA	WAKEUP1 GPIO1_1 (AC17)
Display Interface	Display Connector	GP1[2] (EXP_P1.13)	GP1[2] - (TS_IRQ)	WAKEUP2 GPIO1_2 (AB16)
Application Board	Expansion Connector	GP1[3] (EXP_P1.14)	NA	WAKEUP3 GPIO1_3 (AC16)

1. Functional signals of pin mux are not considered for this table. For more information, see *CPU EVM Schematic Rev H* (SPRR210).

3.7 TAG and Emulator

The CPU Board has support of the following JTAG emulation headers support:

- 60-Pin MIPI Connector
- Standard 14-pin to 60-pin MIPI adapter
- 20-pin CTI to 60-pin MIPI adapter

4 Power Supply

The companion power management IC (PMIC) for the SOC is TPS659039EP-Q1. A step-down 12 V to 3.3 V and 5 V converters are available in order to provide a 3.3V and 5 V DC input to the PMIC as well as 3.3 V and 5 V power rails at the board level.

Figure 18 shows the complete power supply section of the CPU board. For power on/off sequence, see *TPS65903x-Q1 Automotive Power Management Unit (PMU) for Processor Data Sheet* (SWCS095).

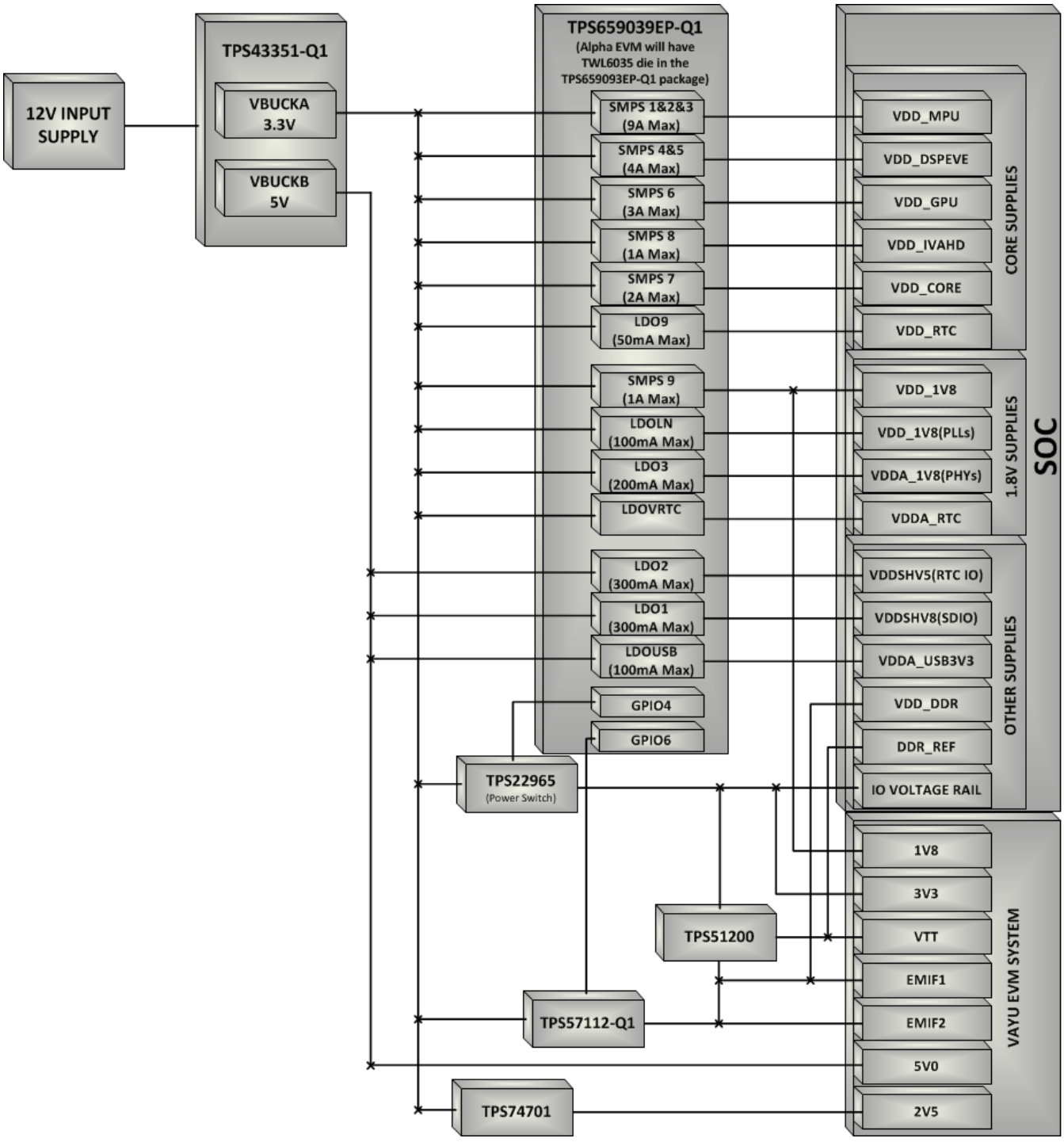


Figure 18. Power Blocks

4.1 Power Monitoring

The CPU Board has provisions for power monitoring using INA226. The measurement system is consisting of the TI INA226 I2C current shunt/power monitors. The INA226 device provides both power supply voltage and shunt current measurements, as well as calculated power via an I2C bus. This allows the device to be placed close to the shunt.

Figure 19 shows a block diagram of the current monitoring system. INA226 are located at the appropriate shunts for various supplies are listed below. These INA226s would be controlled by an off-board MSP430 (or similar device) via a dedicated I2C bus mastered by the off-board device.

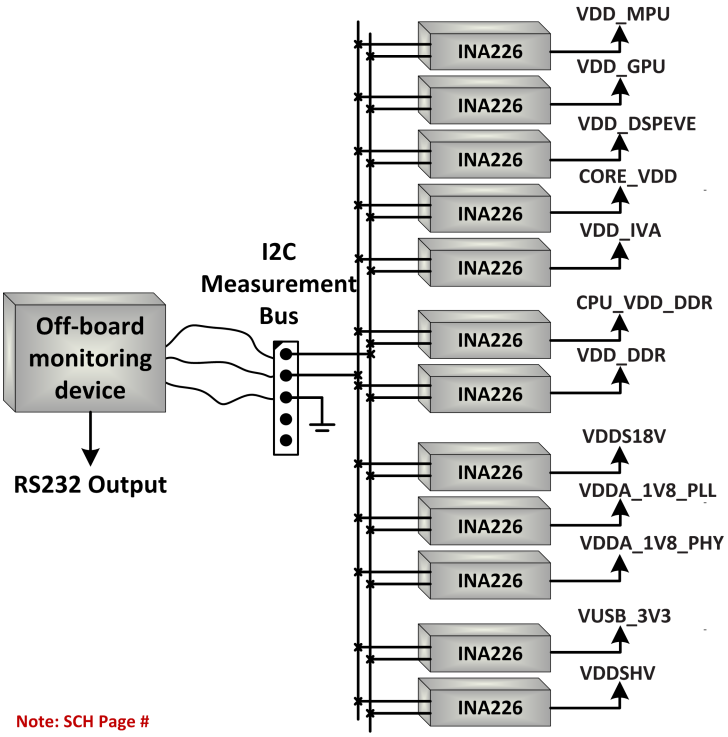


Figure 19. Power Monitoring Block Diagram

Power supply pin groups that are monitored are as follows:

- VDD_MPU
- VDD_GPU
- VDD_DSPEVE
- CORE_VDD
- VDD_IVA
- CPU_VDD_DDR
- VDD_DDR
- VDDS18V
- VDDA_1V8_PLL
- VDDA_1V8_PHY
- VUSB_3V3
- VDDSHV

5 CPU Board With Components Identification

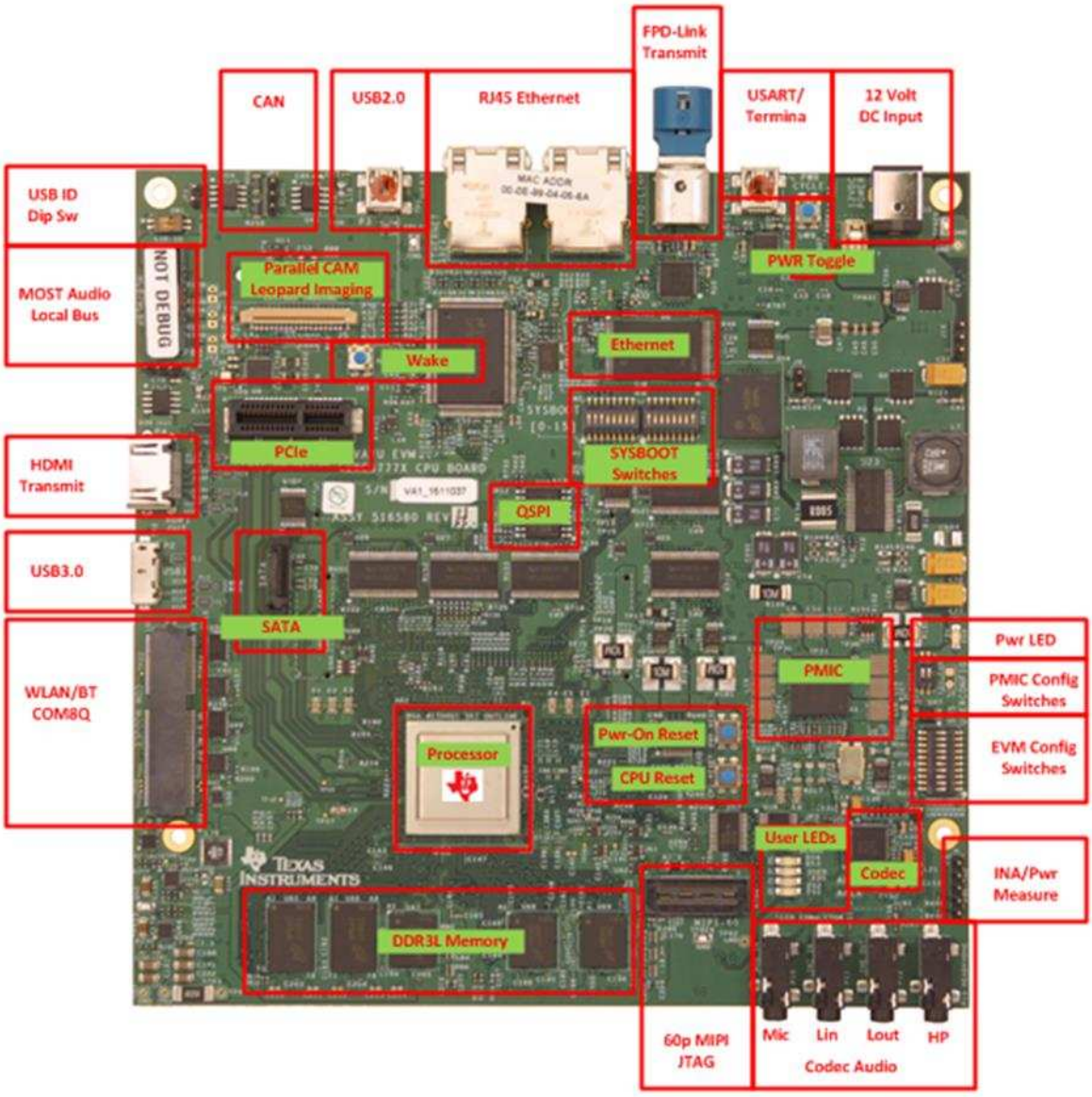


Figure 20. CPU Board

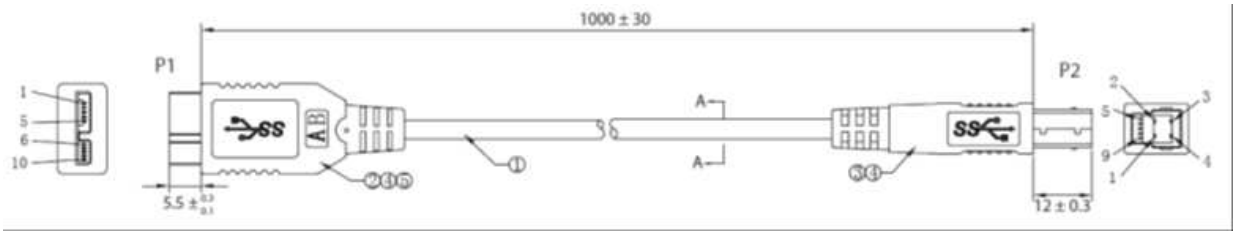
6 USB3 Supported Configurations

The following USB3.x combinations are supportable:

- Micro-A plug to Standard-B plug
  - Connect to hub or external drive/device that has a std B receptacle
- Micro-A plug to Micro-B plug
  - EVM connects to hub or external drive/device that has a micro B receptacle
  - Host connects to the EVM acting as a device
- Standard-A plug to Micro-B plug
  - Host connects to the EVM acting as a device

6.1 Option 1

Use a USB3.0 micro-A to standard-B and USB3.0 Hub like the SIIG shown in Figure 21 and Figure 22.



uEVM5432 Side

HUB Side

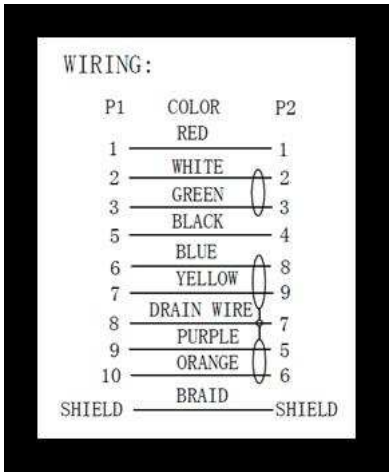
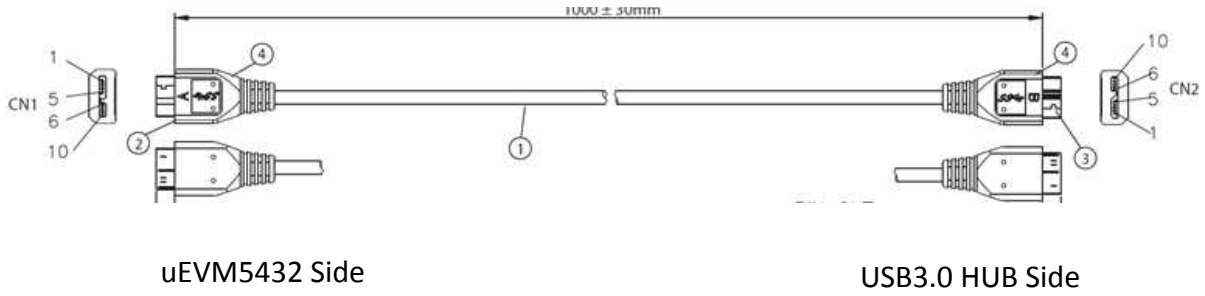


Figure 21. 3023009-01M USB 3.0 Micro-AB TO Standard-B 1m (3.28')

Figure 22. Qualtek SIIG JU-H40312-S14Pport USB3.0 Super Speed USB Hub

6.2 Option 2

Use a USB3.0 micro-A to micro-B and USB3.0 Hub like the IOGEAR as shown in Figure 23 and Figure 24.



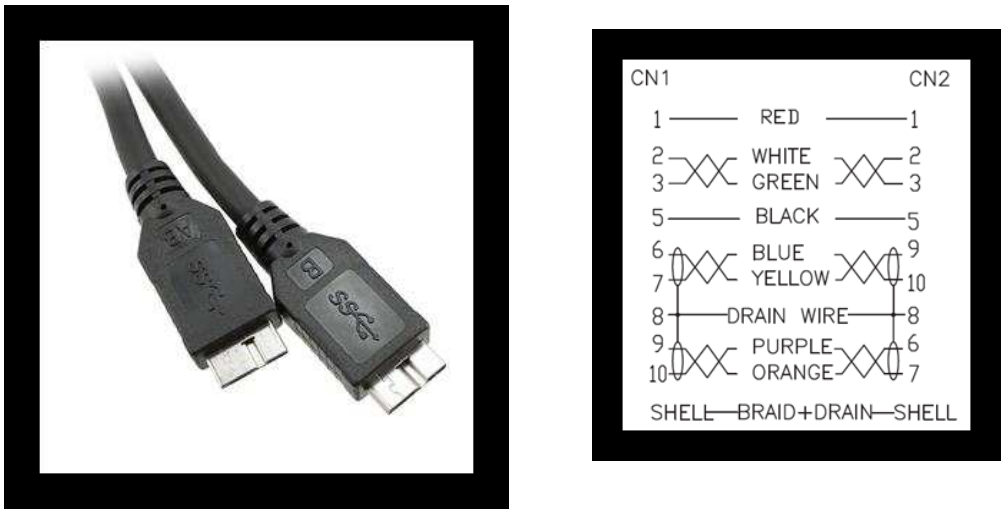


Figure 23. Qualtek 3023007-01M USB3.0 Micro-AB to Micro-B 1m (3.28')

Figure 24. IOGEAR GUH374 4-Port USB3.0 Hub

6.3 Option 3

Use a USB3.0 micro-B to standard-A. Host PC connects to the EVM acting as a device as shown in Figure 25.

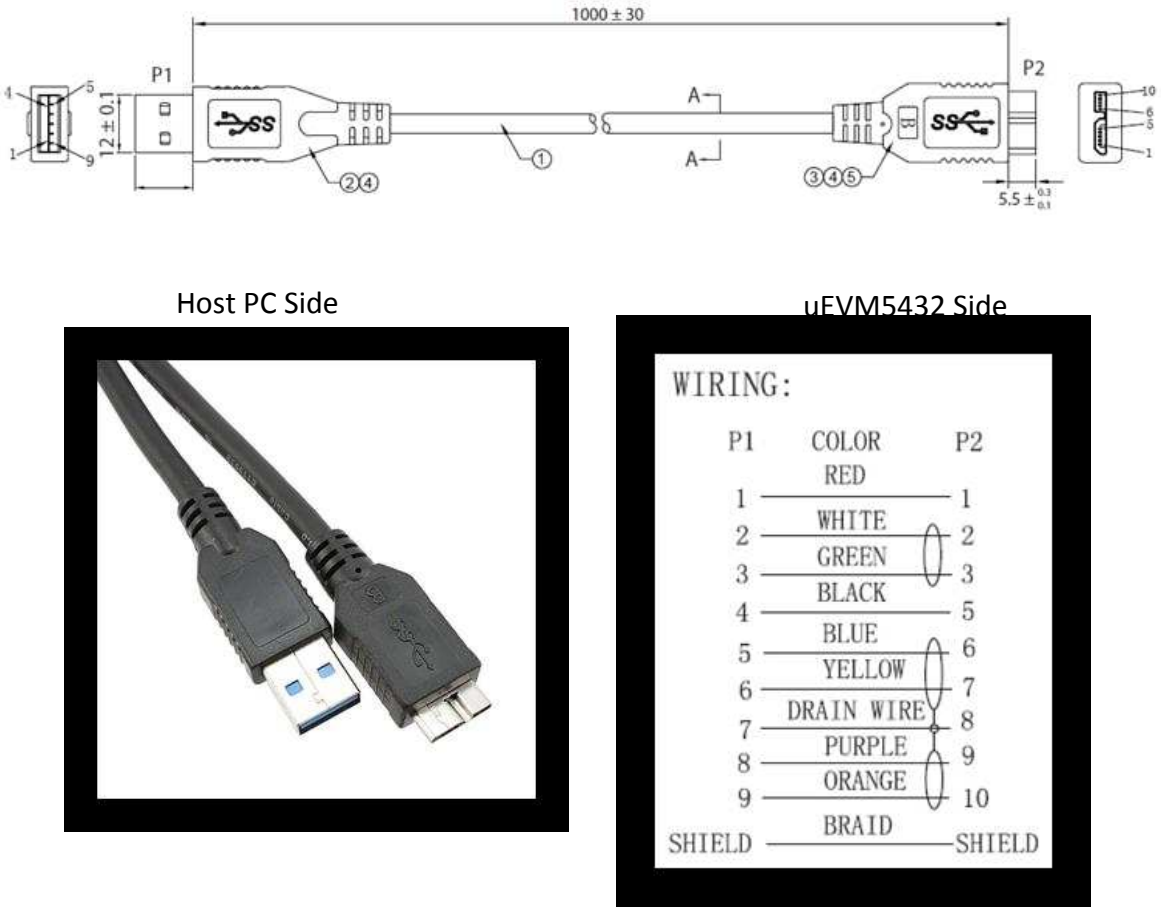


Figure 25. Qualtek 3023005-01M USB3.0 Standard-A to Micro-B 1m (3.28')

7 References

- *CPU EVM PCB Rev H* (SPRR209)
- *CPU EVM Schematic Rev H* (SPRR210)
- *CPU EVM BOM Rev H* (SPRR211)
- *CPU EVM Assembly Drawing Rev H* (SPRR212)
- *CPU EVM PCB Drawing Rev H* (SPRR213)

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      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
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Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

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Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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