DesignDRIVE Development Kit IDDK v2.2.1 Hardware

Reference Guide

Literature Number: SPRUI43
November 2015

Introduction

The DesignDRIVE kit (IDDK) is a single platform that facilitates development and evaluation of design solutions for many industrial drive and servo topologies. The IDDK offers support for a wide variety of motor types, sensing technologies, encoder standards, and communications networks. The IDDK also offers easy expansion to develop with real-time Ethernet communications and functional safety topologies that enable more comprehensive, integrated system solutions. Based on the real-time control architecture of TI's C2000™ microcontrollers (MCUs), the kit is ideal for the development of industrial inverter and servo drives used in robotics, computer numerical control (CNC) machinery, elevators, materials conveyance, and other industrial manufacturing applications.

Trademarks

C2000, Delfino, controlSUITE are trademarks of Texas Instruments.

Overview

The IDDK offers an integrated-drive design with a full-power stage to drive a 3-phase motor, easing evaluation of a diverse range of feedback sensing and control topologies. The kit includes a 180-pin HSEC controlCARD based on the TMS320F28379D C2000 Delfino™ MCU, which integrates dual C28x real-time processing cores and dual CLA real-time coprocessors that provide 800 MIPS of floating-point performance with integrated trigonometric and FFT acceleration.

The sophisticated sensing peripherals on the TMS320F28379D MCU include sigma-delta filter modules with up to eight input channels, four high-performance 16-bit ADCs, and eight windowed comparators. These peripherals enable the IDDK to support shunt, flux gate/HALL, and sigma-delta current sensing simultaneously. For position feedback, the IDDK leverages integrated MCU support for the resolver and incremental encoder interfaces. In addition, customers can also explore configuration options that place the MCU on either side of the high-voltage isolation barrier.

TI designed the kit to plug into 110-V/220-V AC mains, deliver up to 8 amps, and to drive motors to 1 horsepower.

This document covers the kit contents and hardware details and explains the functions and locations of various connector on the board. This document supersedes all the documents for the kit.

WARNING

TI intends this EVM to be operated in a lab environment only and does not consider it to be a finished product for general consumer use.

TI intends this EVM to be used only by qualified engineers and technicians familiar with risks associated with handling high-voltage electrical and mechanical components, systems, and subsystems.

This equipment operates at voltages and currents that can cause shock, fire, and/or injure you if not properly handled or applied. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property.

TI considers it the user's responsibility to confirm that the voltages and isolation requirements are identified and understood before energizing the board and or simulation. When energized, do not touch the EVM or components connected to the EVM.

Getting Familiar With the Kit

1.1 Contents of the Kit

The kit consists of the following items:

- An IDDK EVM
- A TMDXCNCD28379D control processor
- A USB-A to USB Mini-B
- A PMSM motor for evaluation
  - The motor is not included with TMDXIDDK379D.
  - The motor is included with TMDXIDDKM379D bundle.
  - The motor is available stand-alone from the TI eStore. (The part number is HVPMSMMTR.)
- Items not included
  - An external, isolated power supply for developing code at low voltage

1.2 IDDK EVM Features

The EVM has the following features:

- Processor slots for control, real-time connectivity, and functional safety
- The Position Encoder Suite
- The Current Sensor Suite
- A high-voltage rectifier and inverter
- Power supplies

- Two digital-to-analog converters (DACs) to observe system variables on an oscilloscope for debugging
- The Hardware Developer's Package (including schematics and bill of materials) is available through controlSUITE™.

Hardware Overview

2.1 IDDK Evaluation Board

Figure 2-1 shows that the IDDK evaluation board is an open board without enclosures.

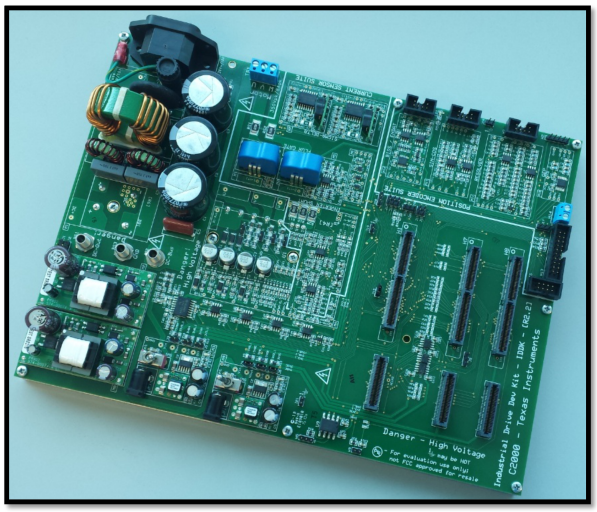

Figure 2-1. IDDK EVM Kit

The board can be divided into the following functional blocks:

- The processor (CPU) block for control, real-time connectivity, and functional safety
- The position encoder suite
- The current sensor suite
- The power inverter and rectifier
- Onboard power supplies

For experimentation, three GND planes are on the board: one plane is for safety and connectivity circuits, another plane is for control and interface, and a third plane is for high power circuits. Provisions are on the board to connect GND planes. If the control GND is tied to the power GND, ensure that position sensors and encoders connected to the board are properly grounded to earth.

NOTE: IDDK offers reconfigurable GND planes, an interprocessor interface, and power stage control. The GND plane configurations can change depending on the style of current sensing and position sensing in the drive solution. The default configuration of the GND planes is only intended for users to develop MCU software drivers to evaluate their topologies. TI does not recommend this configuration for any final drive design or solution. You can select and develop control strategies based on the GND plane reconfigurations and interprocessor interface.

The default isolation/GND configuration of revision R2.2.1 of this evaluation board is set up to have all controlCARDs (H1, H7, and H8) and their interface circuits be separate from the high voltage inverter GND. controlCARDS H1, H7, and H8 have COLD GND, while the inverter has HOT GND.

In the previous release of the board, IDDK R2.2, the control GND was tied to HOT GND in R2.2. In R2.2.1, control GND is tied to COLD GND. Take care while switching between these two boards considering the changes in control GND configuration..

2.2 Functional Blocks

Figure 2-2 shows the functional block diagram of the IDDK. Dedicated processors provide the system with control, real-time connectivity, and safety functions. The control processor has a suite of position encoder interfaces and current sense interfaces. You can configure the controller to select the interfaces you want. Table 2-1 shows that each block is subdivided into macros representing a subfunction.

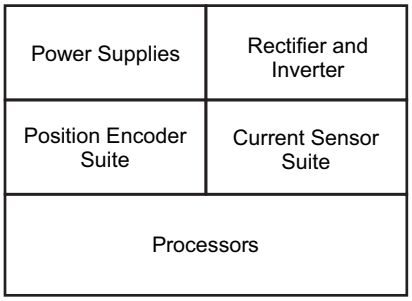

Figure 2-2. Functional Block Diagram of IDDK

Table 2-1. Hardware Macros in IDDK and Their Functions

Functional Block	Macro Reference	Macro Function
Power Supplies	M2	Isolated DC-DC converter – 400 V to 15 V
	M3	DC-Power Supply – Linear Reg 15 V – 5 V to 3.3 V
	M8	Isolated DC/DC Converter – 400 V to 15 V
	M9	DC-Power Supply – Linear Reg 15 V – 5 V to 3.3 V
Rectifier and Inverter	M1	AC Main Power Entry
	M4	3-Phase Inverter
Current Sensor Suite	M5	Flux Gate – Motor Current Sense Interface
	M6	Overcurrent Protection
	M7	Sigma-Delta – Motor Current Sense Interface
Position Encoder Suite	M10	QEP Interface
	M11	Resolver Interface
	M12	EnDat Encoder Interface
	M13	Sin-Cos Encoder Interface
Processors	Main board	All other functions

The following sections present each functional block and their macros. Figure 2-3 shows the layout of various macros in the board. Schematic details of the individual macros are available at *controlSUITE\development_kits\TMDSIDDK_v2.0\IDDK_HwDevPkg_v2.2.1*.

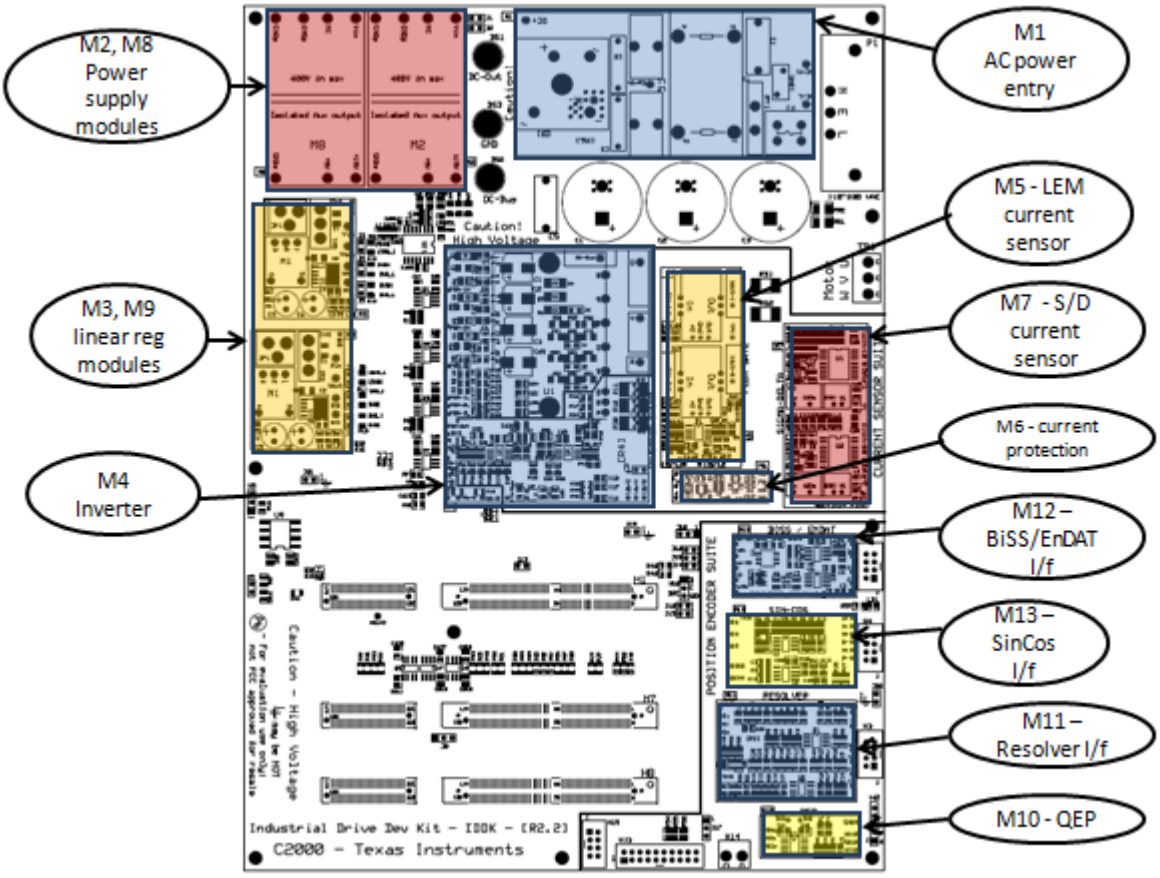

Figure 2-3. Layout of IDDK EVM With Functional Macros

2.3 Processor Section

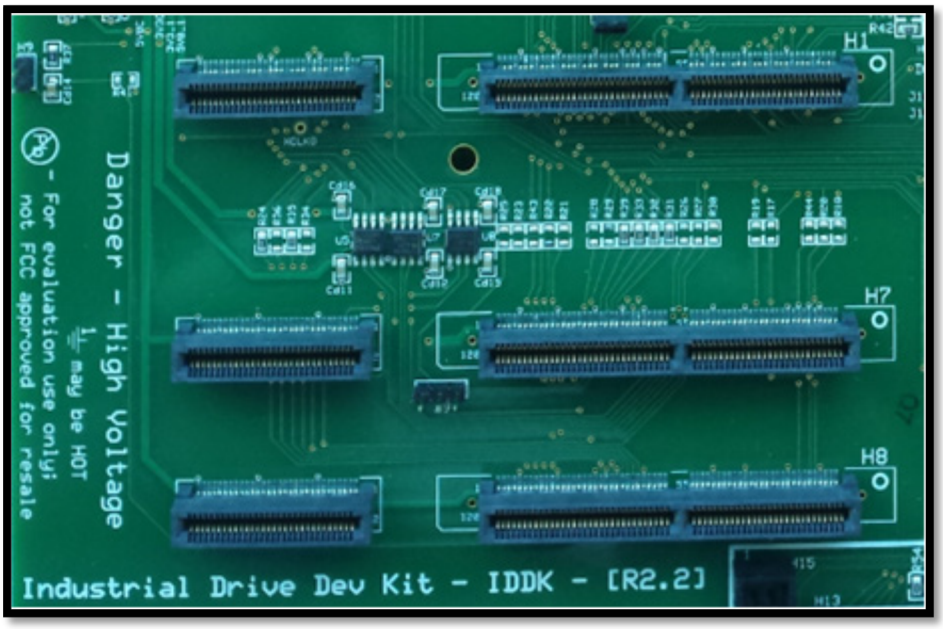

Figure 2-4. Processor Block

2.4 Control Processor Slot – H1

TI design the IDDK around the main control processor card in slot H1. TI design this slot for a C2000 Delfino (TMS320F28379D) MCU control card TMDXCNCD28379D with an HSEC 180-pin edge connector. Digital and analog feedback sensors and the inverter driver connect to this card to evaluate various motor control topologies.

2.5 Expansion Processor Slots

The IDDK supports two expansion control cards slots (H7 and H8) and the control processor slot (H1) for experimenting with the additional capabilities using the main drive control processor. In this release of IDDK, the interface connections among these H1, H7, and H8 connectors are base-level functions achieve a minimum set of interactions. TI will improve or customize this capability in the later revisions of the IDDK. TI will include application solutions for these functions in a future release of the IDDK.

2.5.1 Real-time Connectivity – H7

Real-time connectivity is a necessity in many industrial drives. The control processor (H1) extends the SPI and McBSP signals and the isolated and nonisolated interface to the H7 connector. This processor slot allows real-time connectivity solutions (for example, EtherCAT, Ethernet, Profinet, and so forth) to communicate through SPI or McBSP to the control processor. TI will include application solutions for these functions in a future release of the IDDK.

2.5.2 Functional Safety – H8

Functional safety is mandatory for drives to ensure safety to both the machine and its operator. To implement IEC61800-5-2 drive safety functions, the H8 processor slot allows interface to critical control and sensing signals to the safety processor and to disable the power stage. Many topologies help achieve functional safety to comply with various safety levels. The processor slot lets the external safety module design meet functional safety functions. The control processor (H1) extends SPI interface signals to H8 to communicate with the functional safety processor available on the H8 slot. TI will explore application solutions with functional safety capabilities further in a future release of the IDDK.

2.6 Position Encoder Suite

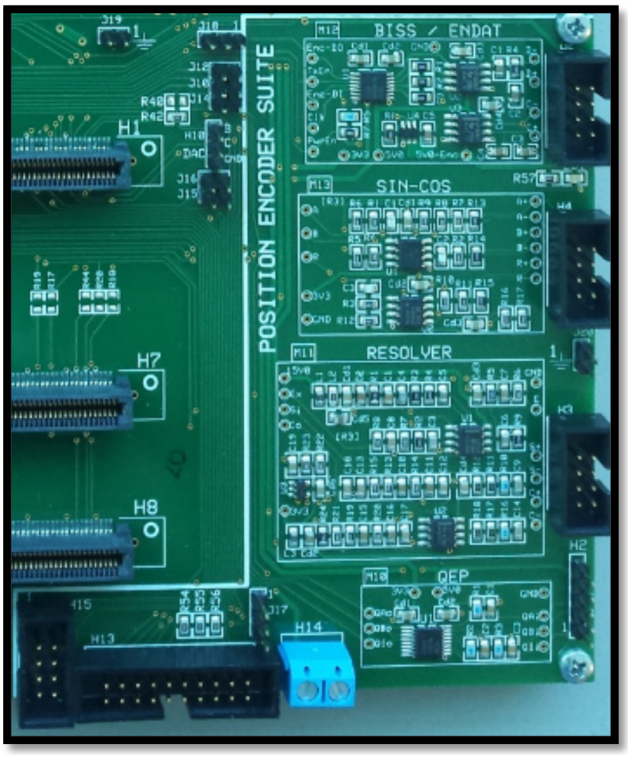

Figure 2-5. Position Sensor Suite

The Position Encoder Suite provides a range of position encoder and sensing interfaces such as the following:

- QEP
- Resolver
- Sin-Cos
- EnDat / BiSS

Ti designed each interface separately. All interfaces can be used simultaneously, except EnDat / BiSS. EnDat / BiSS cannot be used simultaneously without other interfaces because they share resources.

NOTE: Software support for Sin-Cos encoders will be provided in a future release of controlSUITE. See controlSUITE/libs/app_libs/position_manager for more details on the EnDat22 and BiSS-C libraries.

2.6.1 QEP

QEP is a macro (M10). The external interface to QEP is provided by header H2. Figure 2-6 shows the pinouts of the QEP interface.

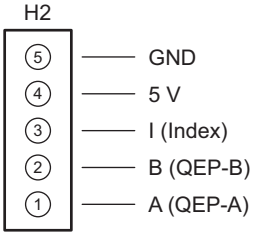

Figure 2-6. QEP Interface Header

2.6.2 Resolver

Resolver is a macro (M11). Refer to the schematic at *controlSUITE\development_kits\TMDSIDDK_v1.0\IDDK_HwDevPkg\IDDK_HwDevPkg_v2.2* for the interface amplifier configuration and gain settings. You can tweak these by modifying the appropriate resistors. The exciter winding amplifier can source and sink 45 mA. For a resolver needing a greater current, use an external buffer. Figure 2-7 shows the External Interface Header (H3) and its pinouts.

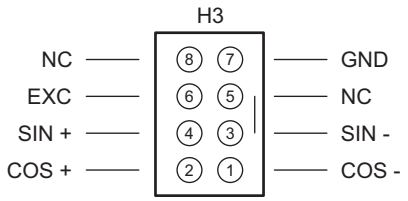

Figure 2-7. Resolver Interface Header

2.6.3 Sin-Cos Encoder

The Sin-Cos Encoder is a macro (M13). This interface is similar to resolver interface because it processes the sine and cosine feedback signals from the encoder. Figure 2-8 shows the External Interface Header (H4) and its pinouts.

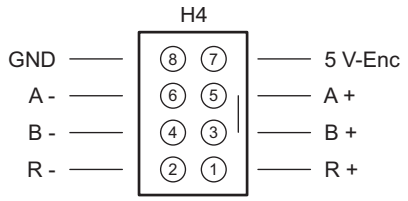

Figure 2-8. Sin-Cos Interface Header

2.6.4 BiSS / EnDat Encoder

The BiSS / EnDat Encoder is a macro (M12). This header is a common interface for both EnDat and BiSS encoders. Figure 2-9 shows the External Interface Header (H6) and how it interfaces with only digital signals. If the BiSS / EnDat encoder have Sin-Cos analog signals, connect them to the Sin-Cos Encoder Interface Header (H4).

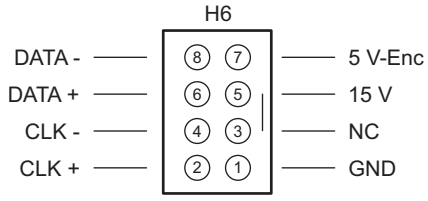

Figure 2-9. EnDat / BiSS Interface Header

2.6.5 TI Design Interface Connector

The encoder signals are brought out on the H13 and H15 connectors and compatible for evaluation with position encoder TI designs such as *Interface to an EnDat 2.2 Position Encoder* (TIDU368).

2.7 Current Sensor Suite

This block provides a range of current sensor interfaces including the following:

- Shunt current sensing within an inverter block
- LEM flux gate or HALL current sensing
- Sigma-delta current sensing

This block also includes circuits to protect against overcurrent. See Figure 2-10 for further information.

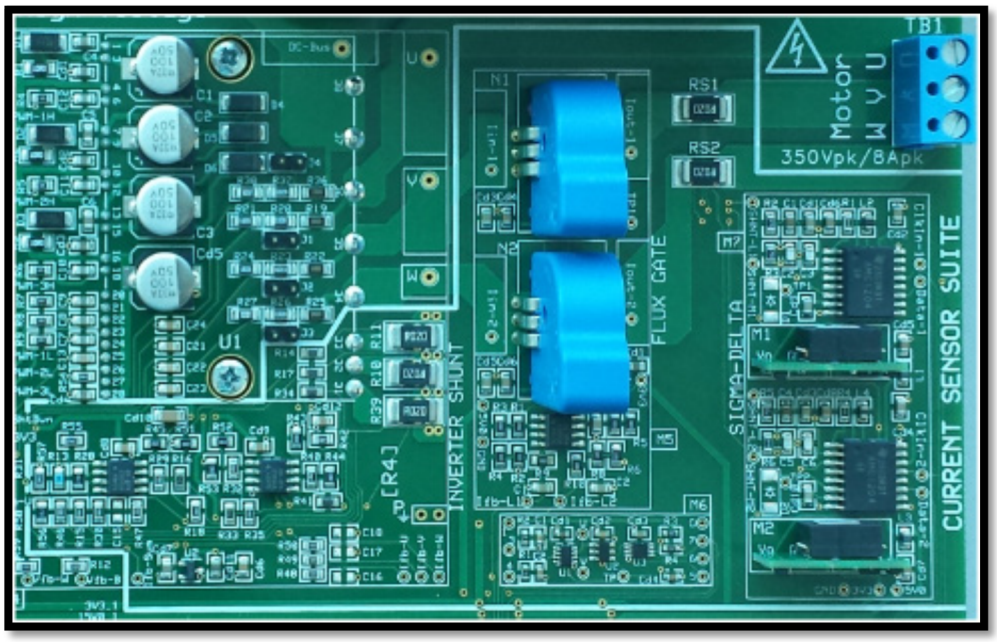

Figure 2-10. Current Sensor Suite

2.7.1 Shunt Current Sensing

Shunt current sensing is a macro (M4). Motor currents are measured by using an on-chip ADC to sense the voltage across shunt resistors connected to the bottom of each half-bridge of the inverter.

NOTE: Shunt current sensing requires the CPU GND and inverter GND be tied together. This sensing method makes the control GND HOT. For applications requiring a COLD control GND, you cannot use this sensing method. See Section 2.8 to enable this sensing method for setting up the HOT control GND.

2.7.2 LEM Current Sensing

LEM current sensing is a macro (M5). LEM sensors are connected to the motor phases in series. Proportional to its input current, use the on-chip ADC to measure the output voltage.

2.7.3 Sigma-Delta Current Sensing

Sigma-delta current sensing is a macro (M7). Connected in series to the motor phases, voltage across a shunt resistor is measured digitally using isolated delta-sigma converters.

All current sensing topologies are designed to give 1.0 per unit value for a current of approximately 10 A. You can sense the currents using all three of them at the same time. You can choose the current feedback to close the current loop using the software.

2.7.4 Overcurrent Protection

Overcurrent protection is a macro (M6). The current sensor suite also includes an overcurrent protection block [M6]. This macro monitors the outputs of both LEM current sensors and generates a TRIP signal to shut down the inverter if the current exceeds 11 A.

2.8 Power Supplies and GND Plane Configurations

The kit has two identical onboard switching power-supply modules (M2 and M8) that take in DC-bus voltage though J1 and J2 jumpers, respectively. Each module delivers an isolated 15-V (400 mA rated) output to identical linear regulator blocks M3 and M9, respectively. The blocks deliver 5 V and 3.3 V to their local GNDs, respectively. M3 (M9) has a power-supply jack (JP1) and a toggle switch (SW1).

An external,15-V power supply can be fed in through JP1 while SW1 selects between the local 15 V from M2 (M8) and the external supply feeds the linear regulators of M3 (M9). TI prefers an external power supply to power the controller during code development so the board operates at low voltage. This low-voltage operation ensures safe operation without a high-voltage node on the board. Figure 2-11 shows the power supply block.

Figure 2-11. Power Supply Block

M3 powers the gate-drive circuits of the inverter (the HOT side) while M9 powers the functional safety and real-time connectivity processors on the H7 and H8 connectors (the COLD side). The control CPU and its interface circuits can either connect to HOT side or COLD side, depending on a set of zero Ω resistor bridges (R8 through R13). You can use only M3 or M9 to power either side by suitably populating a set of jumpers (J3 through J8). Figure 2-12 shows the circuit diagram and Table 2-2 shows the possible configurations.

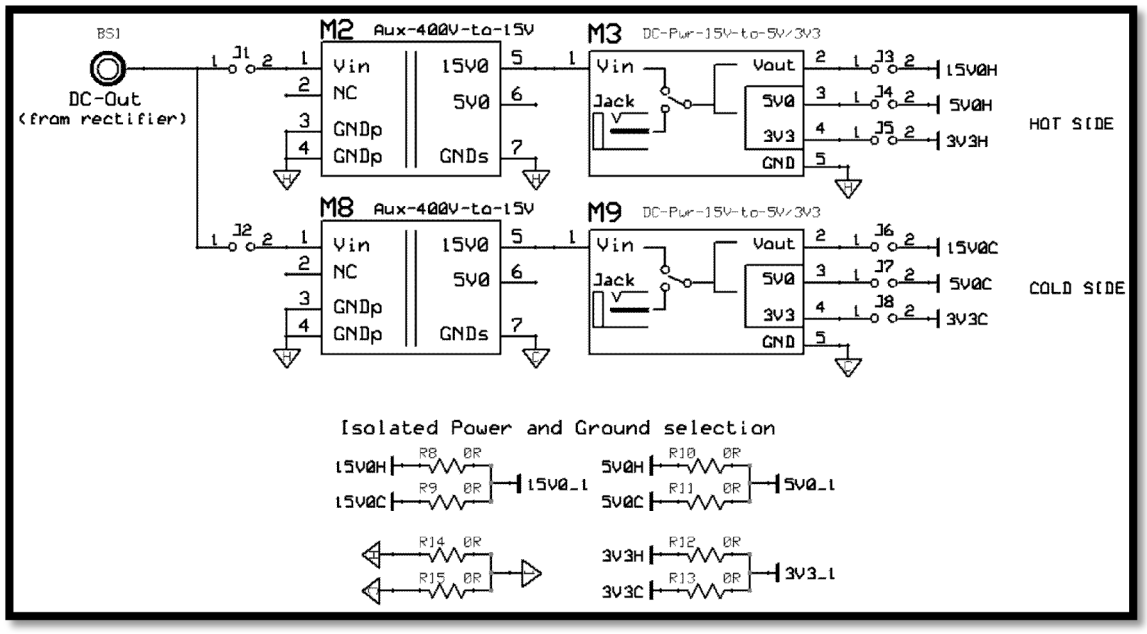

Figure 2-12. Schematic Configuration of Power Supplies

Table 2-2. Power Supply Connection Configuration

Configuration Number	GND Plane Connection	HOT Side Parts			COLD Side Parts		
		J3 to J5	R8, R10, R12	R14	J6 to J8	R9, R11, R13	R15
1	HOT -→ M3 COLD → M9 CONTROL → HOT	√	√	√	√	X	X
2 Default	HOT → M3 COLD → M9 CONTROL → COLD	√	X	X	√	√	√
3	HOT → M3 COLD → M3 CONTROL → HOT	√	√	√	X	√	√
4	HOT → M9 COLD → M9 CONTROL → HOT	X	√	√	√	√	√

The first and second line entries in Table 2-2 are cases that require separate HOT and COLD grounds, the control GND be tied to either HOT GND (as in line 1), or COLD GND (as in line 2). The default GND configuration of the kit out of the box is as in line 2.Line entries 3 and 4 have all GNDs tied together, which makes them all HOT and powered by either M3 or M9.

NOTE: If you choose the HOT control GND configuration, it enables direct measurement of phase voltages and currents through precision resistors. To use this feature, populate resistors R12, R31, R58, R59, and R47–R50 and capacitors C15-C18 (DNPs normally) in M4 (inverter) section of the board.

To power the board out of M9, populate J6 through J8 jumpers and R8 through R13 resistors in the main section of the board. Connecting different GND planes, resistors R14 and R15 are present on the bottom of the board and are unlabeled. Figure 2-13 shows multiple 1206 resistor pads across the various GND planes in multiple locations. TI intends to provide an option to evaluate the impact of the locations tying GND planes together. Carefully identify the GND planes of M9 and M3 before populating these resistors.

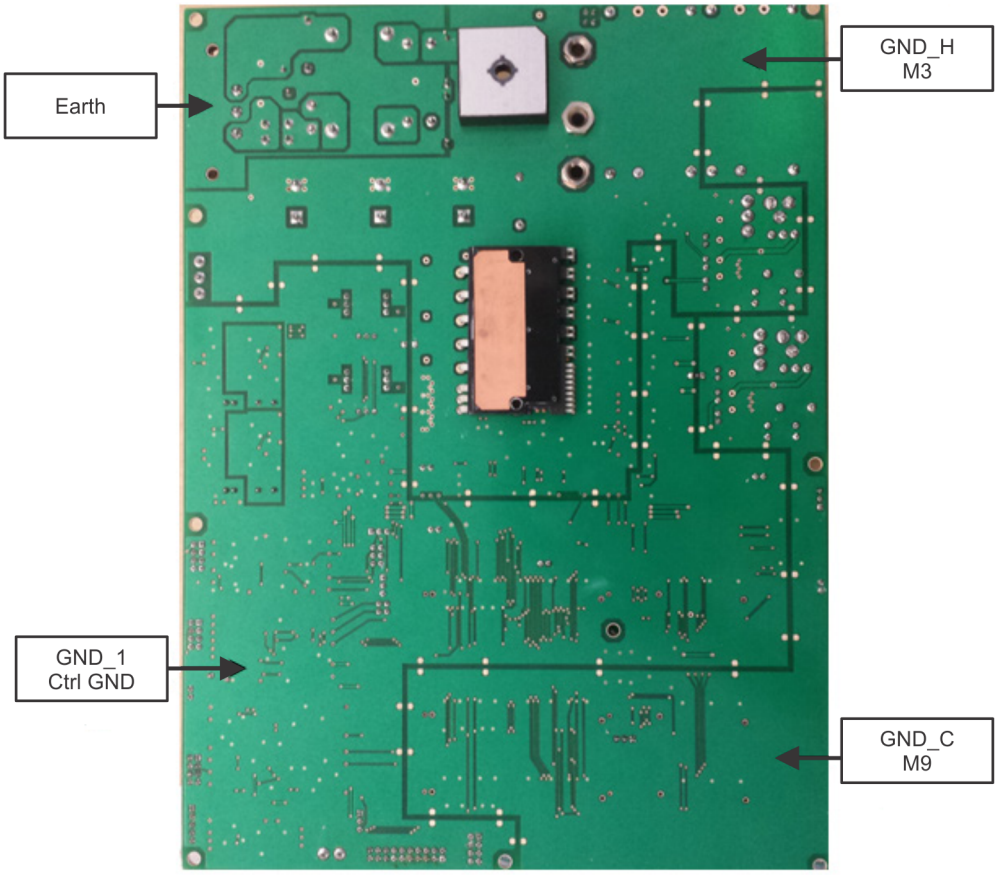

Figure 2-13. Various GND Planes on the Bottom of Board

GND_H and GND_C are tied to M3 and M9, respectively.

The default power supply configuration of the IDDK board is line entry 4 in Table 2-2. This configuration powers the entire board with M9. Figure 2-14 shows the default GND plane connection configuration.

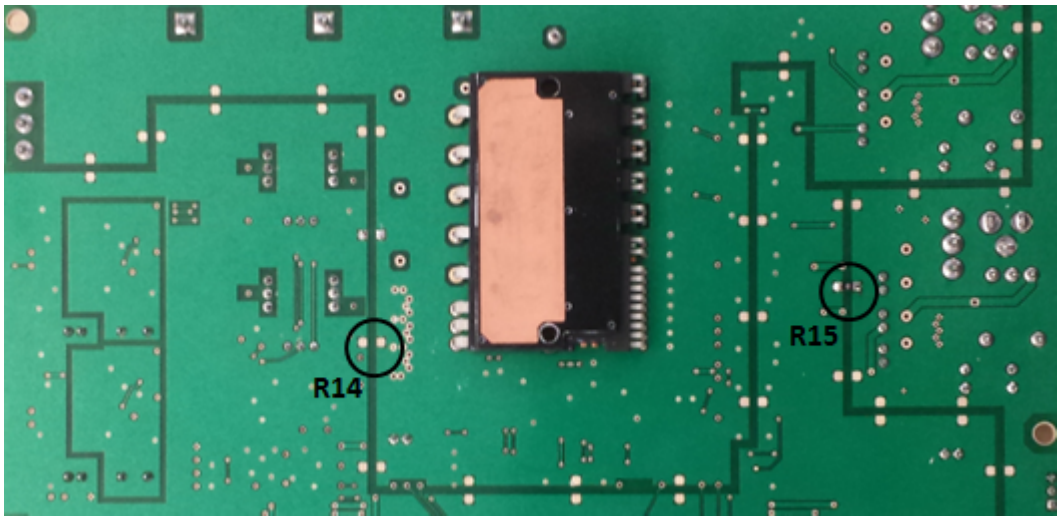

Figure 2-14. Default Connection of Various GND Planes

2.9 Rectifier and Inverter

2.9.1 Rectifier Stage

The rectifier is a block (M1). AC input to the board is fed through a 3-pronged connector (P1). The base of the board (which also acts as heat sink for power components) is connected to the EARTH pin through a pig-tail wire. A diode-bridge rectifier module is mounted on the bottom of the main printed-circuit-board (PCB).

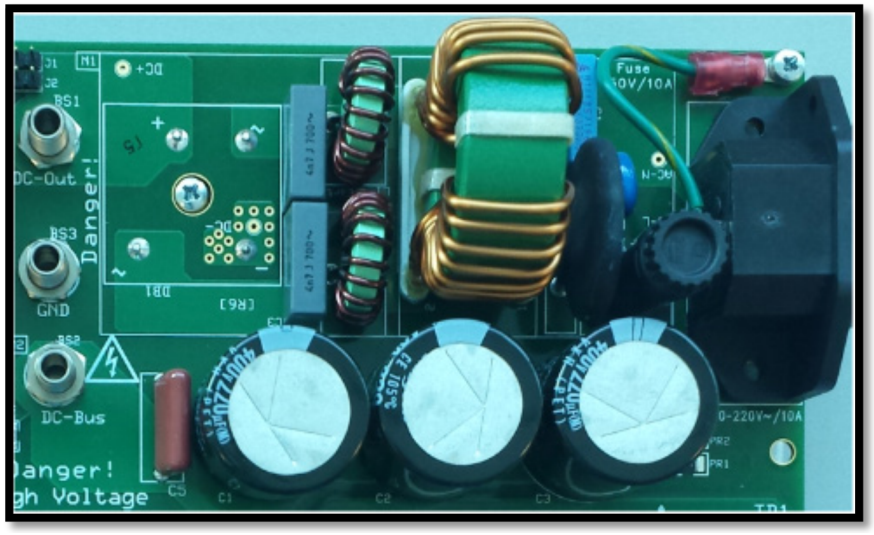

Figure 2-15. AC Line Input Filter and Rectifier

NOTE: The fuse is mounted on fuse holder F1 located close to connector P1

BS1, BS2, and BS3 banana jacks provide flexibility and experimenting with high-voltage power sources. BS1 extends access to unfiltered rectified output of the AC mains. BS2 is tied to the positive terminal of DC-link caps while BS3 is tied to power ground PGND. Figure 2-16 shows how this configuration helps power the board with an external variable DC supply through BS2 and BS3, bypassing the rectifier. Figure 2-17 shows how BS1 and BS2 can connect through a banana cable before turning on the AC when appropriate to restore the AC supply to the board.

2.9.1.1 Connecting the External DC Supply to the DC Link

The external variable power supply can be connected to the board using the BS2 and BS3 banana jacks. If using M2 and M8 bias power supplies, connect BS3 to BS1.

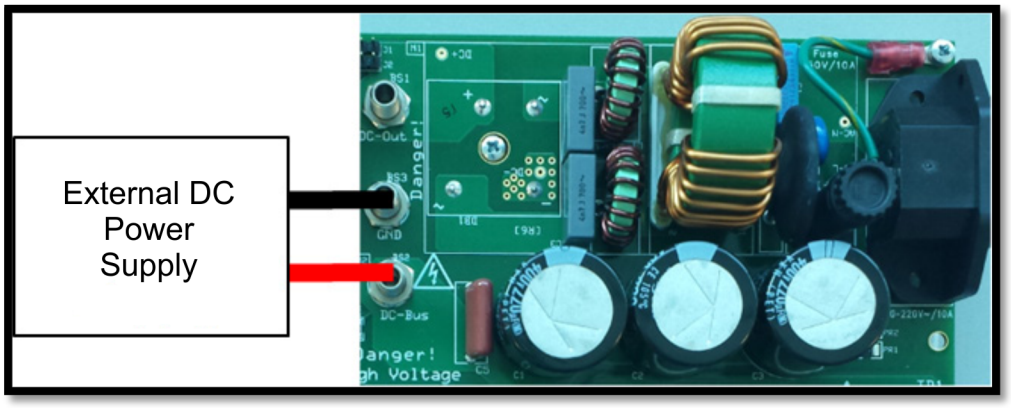

Figure 2-16. Powering Through an External DC Source

2.9.1.2 Connecting Rectifier Output to DC Link

When the drive board is ready to power through AC mains, BS1 and BS2 must be connected through a banana cable before turning on the AC power (110 V–60 Hz/220 V–50 Hz) to P1. BS3 remains open.

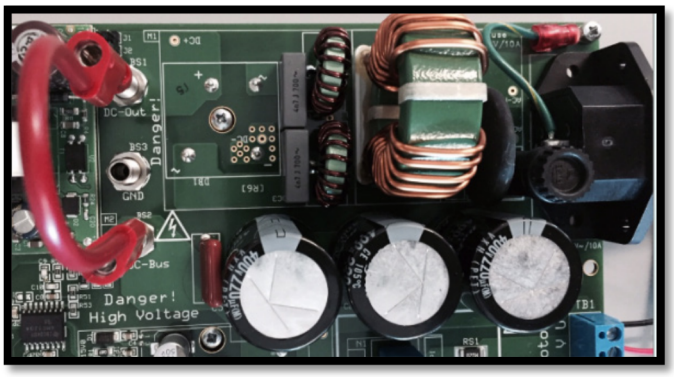

Figure 2-17. Powering Through AC Mains

2.9.2 Inverter Stage

The inverter is a block (M4) with the gate drive circuits on top and IPM on the bottom. A large, thin aluminum base acts as the heat sink and base plate. The jumpers within this block (J1 through J4) are left open for sensing DC-bus voltages up to 400 V but can be populated to sense voltages less than 100 V. Figure 2-18 shows the 3-phase inverter.

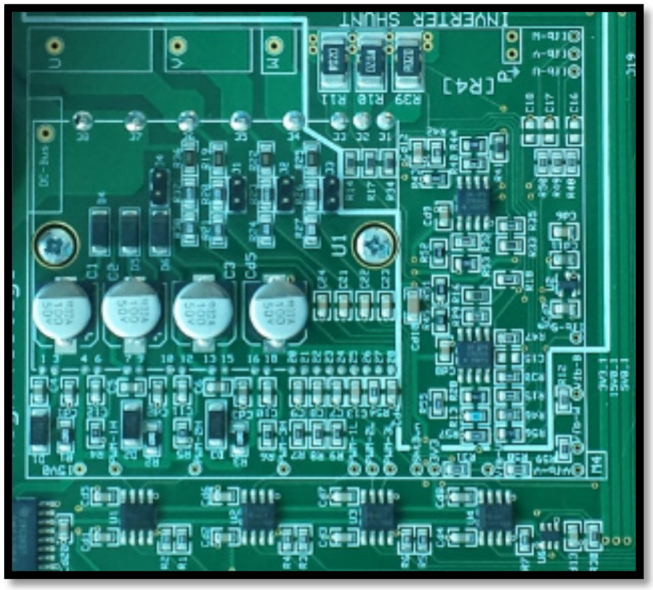

Figure 2-18. 3-Phase Inverter

WARNING

Removing heat sink will break the board connection to earth. Additional safety precautions may be needed to ensure safety of those handling the kit.

2.10 DACs

Figure 2-19 shows the TMS320F28379D with two spare DACs available and how they are brought out on H10 header to visualize control variables in real-time when debugging.

Figure 2-19. DACs

2.11 Power Stage Disable Circuits

The power stage of the IDDK can be shut down using external digital signals. Figure 2-20 shows the external push-button interface employed to generate an emergency shutdown request using the H9 connector. This request can also be generated by overcurrent monitoring hardware, connectivity, and functional safety control processors on H7 and H8 connectors, respectively.

Figure 2-20. External Shutdown Signal Input

Use appropriate protection logics in applications to safely disable the power stage.

WARNING

The board layout may not represent the optimal layout even though the best practices layout guidelines are followed.

Take care to adapt or modify the schematics and layout to meet your application requirements.

Hardware Resource Mapping

3.1 Digital Signal Mapping

Table 3-1 shows the functional mapping of various digital signals connected to control processor on H1.

Table 3-1. Digital Signal Mapping on Control Card H1

IDDK Signal Name	MCU GPIO	MCU Peripheral Associated With GPIO	Function	Reserved
PWM-1A	0	EPWM-1A	PWM for inverter phase U high side	
PWM-1B	1	EPWM-1B	PWM for inverter phase U low side	
PWM-2A	2	EPWM-2A	PWM for inverter phase V high side	
PWM-2B	3	EPWM-2B	PWM for inverter phase V low side	
PWM-3A	4	EPWM-3A	PWM for inverter phase W high side	
PWM-3B	5	EPWM-3B	PWM for inverter phase W low side	
En-Clk	6	ABS ENC-CLK	Absolute Encoder Clock out	
C1-SPIB-CLK	7	PEM CLK	Encoder SPI Clock out	
SD-CLK-PWM5A	8	EPWM-5A	Sigma-delta clk for motor phase current	
SD-CLK-PWM5B	9	EPWM-5B	Sigma-delta clk for Vdc bus	
RES-PWM6A	10	EPWM-6A	PWM for resolver excitation (option)	
AdcSOCXbarOut	11	OUTPUTXBAR7	ADC SoC pulse	√
En-PwrPG	12	GPIO input	Power Good Input from Ext Enc Interface	
-----	13			
CompOutSC-B	14	OUTPUTXBAR3	SinCos Enc Interface – B	√
CompOutSC-A	15	OUTPUTXBAR4	SinCos Enc Interface – A	√
C1-SPIA-SIMO	16	SPIA	SPI signal to CC2 (Connectivity card)	
C1-SPIA-SOMI	17	SPIA	SPI signal to CC2 (Connectivity card)	
C1-SPIA-CLK	18	SPIA	SPI signal to CC2 (Connectivity card)	
C1-SPIA-STE	19	SPIA	SPI signal to CC2 (Connectivity card)	
C1-QEP1-A	20	QEP1	QEP signal	
C1-QEP1-B	21	QEP1	QEP signal	
AdcSOCXbarOut	22	QEP1	QEP signal	
C1-QEP1-I	23	QEP1	QEP signal	

Table 3-1. Digital Signal Mapping on Control Card H1 (continued)

IDDK Signal Name	MCU GPIO	MCU Peripheral Associated With GPIO	Function	Reserved
En-DO	24	SPIB	SPI Interface for Abs Encoder	
En-DI	25	SPIB	SPI Interface for Abs Encoder	
C1-SPIB-CLK	26	SPIB	SPI Interface for Abs Encoder	
C1-SPIB-STE	27	SPIB	SPI Interface for Abs Encoder	
SCI RX (on CC)	28	SCIA	Isolated SCI on control card	
SCI TX (on CC)	29	SCIA	Isolated SCI on control card	
C1-CAN-TX	30	CANA	Isolated CAN Interface	
C1-CAN-RX	31	CANA	Isolated CAN Interface	
En-PwrEn	32	GPIO output	Power Enable for Abs Encoder	
-------	33			
(LED LD3)	34	(GPIO)	(LED lighting)	
En-TxEn		PEM TX En	Tx Enable for Abs Encoder	
-------	35 to 38			
En-PwrFault	39	GPIO input	Power Fault Input from Ext Enc I/f	√
TZn	40	PWM TRIP ZONE	Overcurrent Protection	
CLR FAULT	41		Overcurrent Protection – Clear	
-------	42			
-------	43			
En-TxClkEn	44	GPIO output	Enable TX clk for Abs Encoder	√
GPIO	45	GPIO	Brought out to H15	
STO-PB	46	GPIO	Safe Torque Off signal from CC2/3	√
-------	47			
SD-Data-V	48	SD1	SD data for phase current V	
SD-Clk-PWM5A	49	SD1	SD clk for phase current V	
SD-Data-W	50	SD2	SD data for phase current W	
SD-Clk-PWM5A	51	SD2	SD clk for phase current W	
SD-Data-Volt	52	SD3	SD data for Vdc	
SD-Clk-PWM5B	53	SD3	SD clk for Vdc	
CompOutSC-A	54	QEP2	QEP signal (SinCos)	
CompOutSC-B	55	QEP2	QEP signal (SinCos)	
AdcSOCXbarOut	56	QEP2	QEP signal (SinCos)	
CompOutSC-R	57	QEP2	QEP signal (SinCos)	
TripCC1	58	GPIO output	Inverter Trip control	
CompOutSC-R	59	OUTPUTXBAR2	SinCos Enc Interface - R	√
-------	60-68			

Table 3-1. Digital Signal Mapping on Control Card H1 (continued)

IDDK Signal Name	MCU GPIO	MCU Peripheral Associated With GPIO	Function	Reserved
C1-SPIC-SIMO	69	SPIC	Comm channel to Safety CC – H8	√
C1-SPIC-SOMI	70	SPIC	Comm channel to Safety CC – H8	√
C1-SPIC-CLK	71	SPIC	Comm channel to Safety CC – H8	√
C1-SPIC-STE	72	SPIC	Comm channel to Safety CC – H8	√
-------	73 to 83			
C1-MDX	84	McBSPB	Isolated McBSP connection from CC – H7	√
C1-MDR	85	McBSPB	Isolated McBSP connection from CC – H7	√
C1-MCLKX	86	McBSPB	Isolated McBSP connection from CC – H7	√
C1-MFSX	87	McBSPB	Isolated McBSP connection from CC – H7	√
-------	88 and above			

3.2 Analog Signal Mapping

Table 3-2 shows the functional mapping of various analog signals connected to control processor on H1.

Table 3-2. Analog Signals and Mapping

IDDK Signal Name	MCU Analog	Signal Description	Reserved
DAC-A	A0	Resolver Carrier excitation (option)	
DAC-B	A1	General-purpose display	
Ifb-V	A2	Phase V LEM current feedback	
Vfb-V	A3	Phase V voltage feedback	
Ifb-Sv	A4	Phase V shunt current feedback	
Ifb-Su	A5	Phase U shunt current feedback	
Vfb-Bus	B0	DC-bus voltage from shunts	
DAC-C	B1	General-purpose display	
Ifb-W	B2	Phase W LEM current feedback	
Vfb-W	B3	Phase W voltage feedback	
Ifb-Sw	B4	Phase W shunt current feedback	
-------	B5		
SC-A-2	ADCIN14	Sin Cos Analog input A	√
R-Cos	ADCIN15	Resolver cosine feedback	
Ifb-Su	C2	Phase U shunt current feedback	
Vfb-U	C3	Phase U voltage feedback	
-------	C4		
-------	C5		
SC-B-2	D0	Sin Cos Analog input B	√
R-Sin	D1	Resolver sine feedback	
SC-R	D2	Sin Cos Analog input R	√
-------	D3		
-------	D4		
-------	D5		

3.3 Jumpers and Switches

Table 3-3 shows the various jumpers and switch connections available onboard.

Table 3-3. Purpose of Jumpers and Switches

Jumpers and Switches	Description
[Main] – J1	Connect Vdc to power supply module M2
[Main] – J2	Connect Vdc to power supply module M8
[Main] – J3 to J5	Jumpers to bring out linear regulator block M3 voltages to HOT and COLD sections
[Main] – J6 to J8	Jumpers to bring out linear regulator block M9 voltages to HOT and COLD sections
[Main] – J9	Jumper to enable connectivity and functional safety processors to shutdown the inverter
[Main] – J10	Connects GPIO to EnDat Clock
[Main] – J12	Do Not Populate
[Main] – J13	Connect SPISTE to ground
[Main] – J14-17	Do Not Populate
[Main] – J18	Populate between (1-2) : Connects Encoder data out (En-Do-1 to the processor)
[Main] – J19 to J21	GND headers for probe access
[M3] – SW1	Select 15-V supply from JP1 or onboard from M2 to generate 5 V and 3.3 V
[M9] – SW1	Select 15-V supply from JP1 or onboard from M8 to generate 5 V and 3.3 V
[M4] – J1 to J4	DC-bus voltage sense scaling jumpers, DNP for voltage greater than 100 V

3.4 Headers and Connectors

Table 3-4 shows the headers and connectors available onboard.

Table 3-4. Headers and Connectors

Headers and Connectors	Description
[M3] – JP1	15-V DC power supply jack adaptor
[M9] – JP1	15-V DC power supply jack adaptor
[Main] – H1	180-pin HSEC connector slot for control processor card
[Main] – H2	5-pin header for QEP
[Main] – H3	4 × 2 header for Resolver
[Main] – H4	4 × 2 header Sin Cos
[Main] – H5	3-pin CAN connector
[Main] – H6	4 × 2 header for EnDat / BiSS
[Main] – H7	180-pin HSEC connector slot for real time connectivity processor card
[Main] – H8	180-pin HSEC connector slot for functional safety processor card
[Main] – H9	2-pin header for Safe Torque Off (STO)
[Main] – H10	3-pin header for DAC
[Main] – H13	20-pin header compatible with position encoder TI designs such as *Interface to an EnDat 2.2 Position Encoder* (TIDU368)
[Main] – H14	2-pin power supply header for position encoder TI designs
[Main] – H15	8-pin header compatible with position encoder TI designs such as *Interface to an EnDat 2.2 Position Encoder* (TIDU368)
[Main] – P1	3-pin AC power cord adaptor
[Main] – TB1	3-pin connector for 3-phase motor terminals

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