Digital Front End (DFE) User Guide for Keystone II Devices

User's Guide

![Texas Instruments logo]

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Abbreviations

3GPP	3rd generation Partnership Project
ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Convertor
AGC	Automatic Gain Control
AID	Bus interface connecting IQN2 with DFE
AIL	Antenna Interface Lanes
AxC	Antenna Container
BB	Baseband sub-block in DFE
BDC	Bulk Down Conversion
Be-AGC	Back end AGC
BPF	Band Pass Filter
CB	Capture Buffer
CCDF	Complimentary Cumulative Distribution Function
CFR	Crest Factor Reduction
CDFR	CFR DPD Fractional Re-sampler
CIC	Cascaded Integrator-Comb (Filter)
CMOS	Complementary Metal-oxide Semiconductor
DAC	Digital to Analog Convertor
DDC	Digital Down Conversion
DUC	Digital Up Conversion
DDUC	Digital Down Convertor and Up Convertor (Block within DFE)
DFE	Digital Front End
DL	Downlink
DPD	Digital Pre-Distortion
EVM	Error Vector Magnitude
Fe-AGC	Front End AGC
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
GPIO	General Purpose Input Output
IF	Intermediate Frequency
IMD	Inter Modulation Distortion
IQN2	IQ Net 2 Block within the 66AK2L SoC
JESD	JEDEC Serial Interface for Data Convertors
LTE	Long Term Evolution
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVDS	Low Voltage Differential Signaling
LNA	Low Noise Amplifier
MSPS	Mega-Samples Per Second
NCO	Numerically Controlled Oscillator
PA	Power Amplifier
PAP	PA protection sub-block within DFE
PAR	Peak to Average Ratio
PFIR	Programmable FIR (Filter)
RF	Radio Frequency
RRC	Root Raised Cosine (Filter)
RX	Receive/Receiver
SC	Sum Chain
SEM	Spectral Emission Mask

Abbreviations (continued)

SoC	System on Chip
SERDES	Serializer DeSerializer
SPI	Serial Peripheral Interface
TX	Transmit/Transmitter
UL	Uplink
WCDMA	Wideband Code Division Multiple Access

Introduction

1.1 Overview

The Digital Front End (DFE) is a programmable peripheral integrated into Texas Instruments Keystone II SOCs to perform transmit and receive signal processing. The DFE provides a JESD204B SerDes interface to connect with analog-to-digital and digital-to-analog convertors. The DFE provides for transmit and receive digital signal processing, JESD204B transport, and includes digital down/up convertors (DDUC), Transmit, Receive, and Capture buffer blocks. The DFE connects to the rest of the SOC through the IQN2 module.

DFE signal processing is performed on the transmit path (TX) and the receive path (RX). The transmit path includes channel-based and stream-based up conversion. Specific versions targeted towards wireless base-station markets also include crest factor reduction (CFR) and digital pre-distortion (DPD). The receive path includes functionality for wideband and narrowband automatic gain control (AGC), complex equalization, decimation, filtering, and down conversion. The DFE also includes a feedback path to capture samples from transmit side. This data is utilized for DPD to linearize the power amplifier output. This path can also act as an additional receive path to add extra receive capacity (or for network listening modes for 3GPP applications).

On the transmit side, DFE aggregates multiple real or complex digital data channels into signal streams. On the receive side, DFE receives JESD204B-formatted signal streams containing time-division multiplexed data for multiple ADC channels, and separates them into individual real or complex data channels.

The DFE performs signal processing operations applicable to both individual channels, such as gain, interpolation, decimation, and those which apply to the signal streams, such as filtering, frequency translations, channel combining, crest factor reduction, and digital pre-distortion.
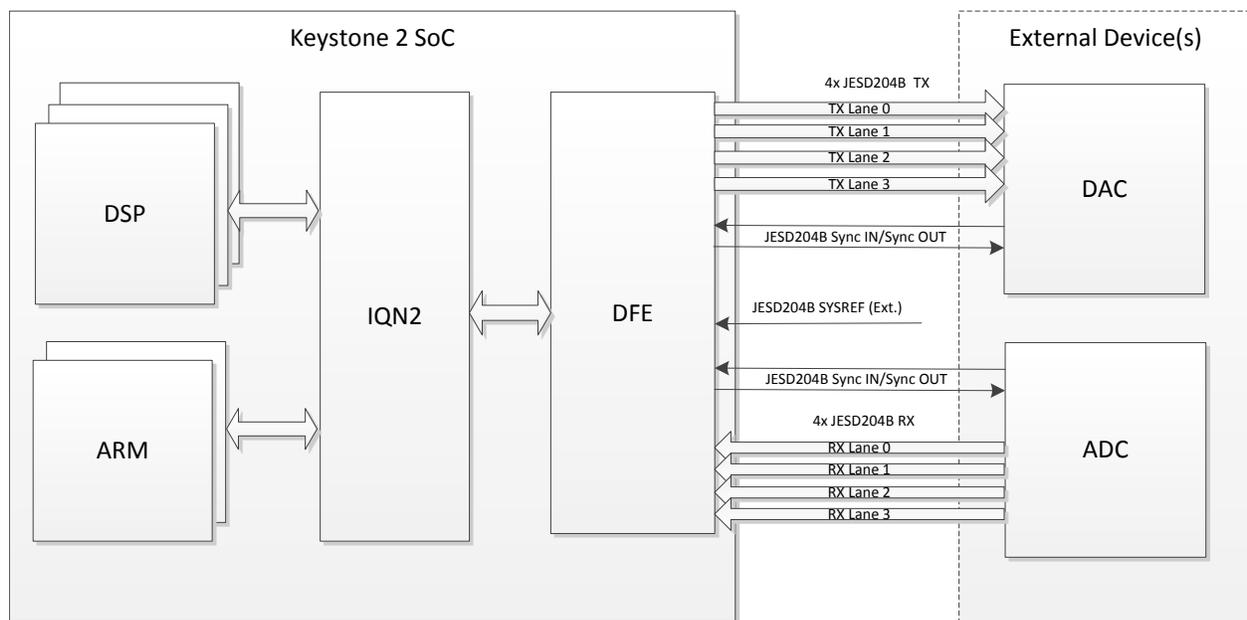
Figure 1-1. DFE Context Diagram

1.2 Features

- 4 JESD SERDES lanes, each supporting up to 7.37 Gbps
- Support for up to 4TX, 4 RX, and 2 feedback RX streams.
- 4 DDUCs, each capable of being used as and up or down convertor.
- Each DDUC supports 1 to 12 channels for a total of up to 48 channels.
- Programmable FIR filters (PFIRs) inside the DDUCs allow for varying tap lengths and storage of multiple filters.
- Transmit Functionality
    - TX includes DUC, CFR, DPD, and Bulk up conversion.
    - TX and RX power meters to support power monitoring
    - PA protection logic built into the TX block to limit RMS or peak power
    - Crest factor reduction to limit the signal peak to average power ratio
    - Digital pre-distortion to improve system linearity by allowing PAs to operate more efficiently
    - Provides post-DPD fractional resampling, mixing and summing options
    - Programmable 55 tap filter to ease TX IF filtering requirements
    - Fractional re-sampler to allow DPD and JESD sample rates to differ
    - 48 bit mixer and NCO
    - Switching, summing options
    - Interfaces to the JESD module
- Receive Functionality
    - Provides receiver functionality prior to digital down-conversion to baseband
    - RX includes DC-offset cancellation, front-end and back-end AGC, decimation, bulk down conversion, RX equalizer and I/Q imbalance correction.
    - Provides 90-dB stops and 80% BW optional real to complex filtering and programmable decimation (supported decimation rates: 1x, 2x, 4x, 8x, and 16x).
    - 16 tap complex equalizer for linear distortion compensation or calibrated frequency-dependent IQ imbalance correction
    - Flexible mixing, switching, and summing options
    - Interfaces to the JESD module
- Tuning and channel aggregation and distribution
- Supports bypass capability to deliver data from JESD straight to the baseband block for JESD attach applications
- GPIOs to control external data convertors and transceivers
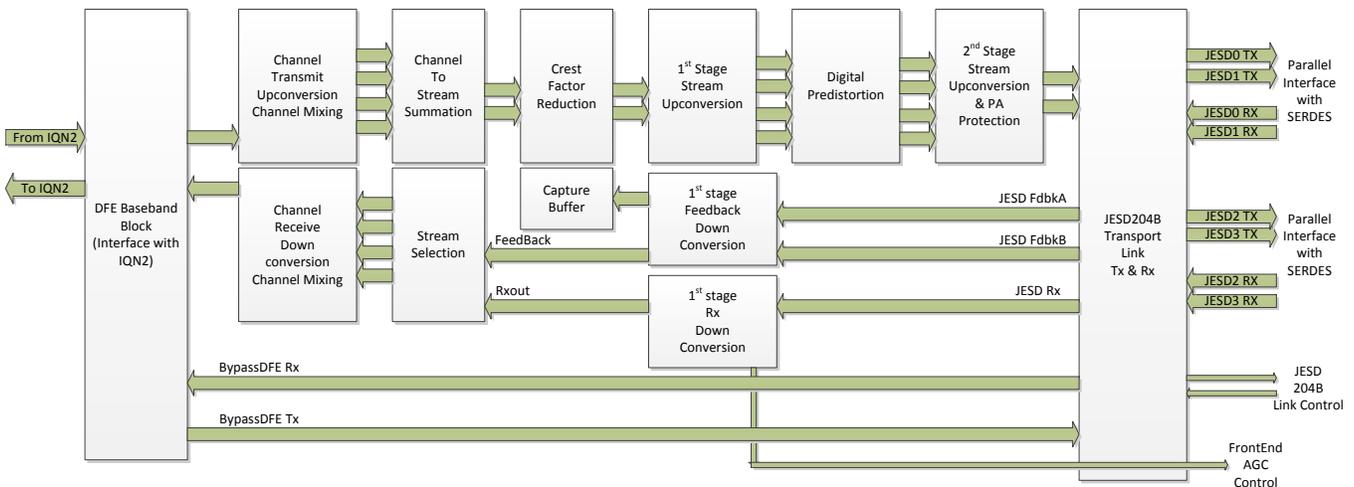
Figure 1-2. DFE Block Diagram

1.3 Connectivity

The DFE block has the following interfaces:

IQNET2 (interface towards the SoC)

- A 128-bit wide AID bus for streaming channel IQ data between DFE and IQN2.
- A 128-bit control port for transferring DPD capture data and coefficients between the DFE and the DSP/ARM cores (PktDMA-based).
- A 32-bit VBUSP slave interface for configuration
- Two interrupt strobes (all of the DFE interrupts get aggregared into 2 interrupts signals - Additional register reads are needed to determine the source of DFE interrupts).

IOs (Data and control interfaces towards data convertors)

- SERDES: 4 lanes
  - (a) 2 lanes directly connected to JESD module in DFE
  - (b) 2 lanes connected through muxes to allow JESD or AIL usage.
- LVDS (3 inputs and 2 outputs)
  - (a) 2 JESD sync inputs and 2 sync outputs (supports connecting up to 2 devices)
  - (b) 1 SYSREF input (from clock generator)
- CMOS (18 GPIOs, most important ones listed below)
  - (a) 1 SYSREF request output per clock generator (from JESD)
  - (b) 2 JESD sync inputs and 2 sync outputs for interfacing to data converters which do not support LVDS sync.
  - (c) Several other GPIOs used for control and interrupt signalling with the external data convertors.

1.4 System Overview and Use Cases

This section provides a system-level functional overview of the DFE and lists the typical use case scenarios.
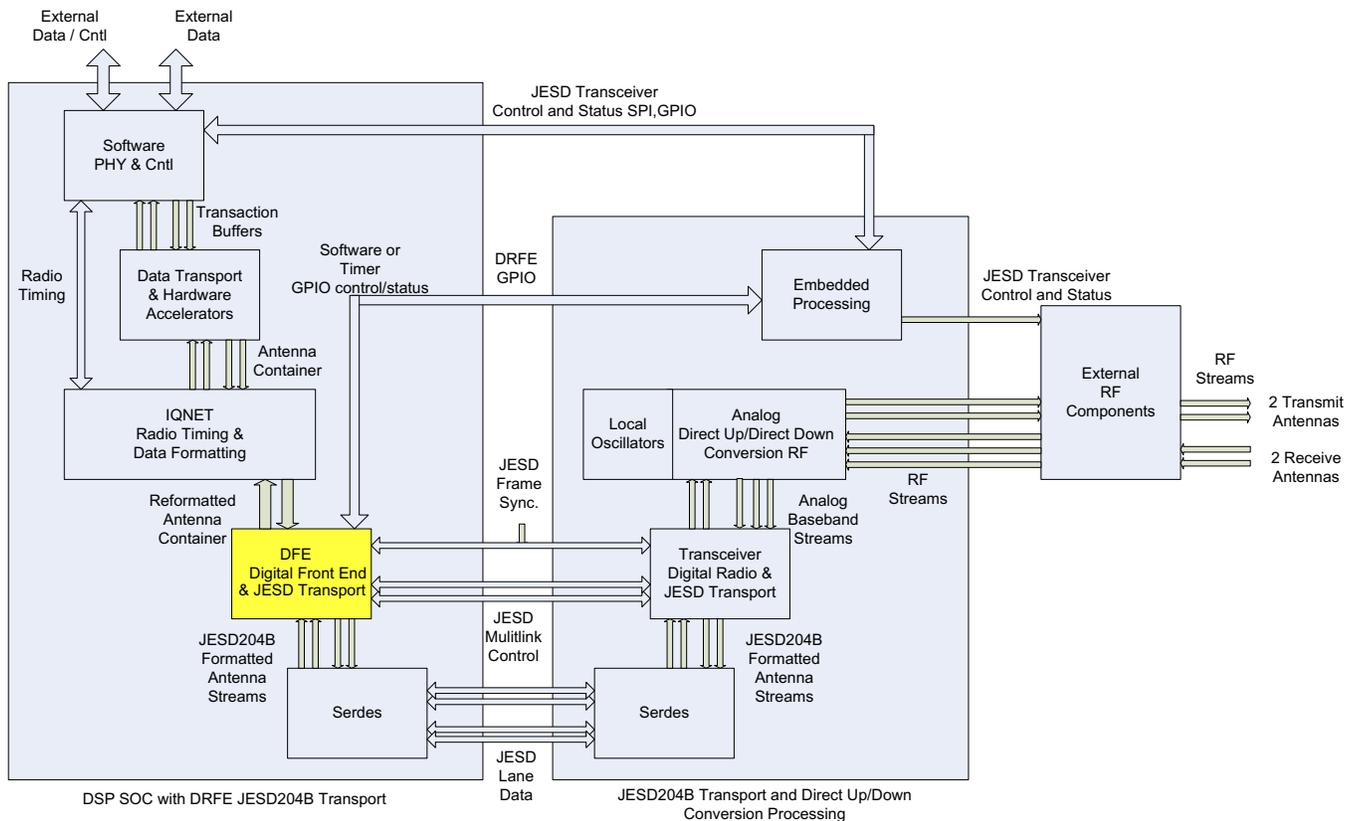
Figure 1-3. DSP SoC to JESD Transceiver SoC Flow and Control Diagram

Figure 1-3 illustrates the connections between the TCI663xK2L SoC blocks and the external transceiver or data convertor. Refer to the TCI663xK2L SoC data manual (SPRS893) for a general overview of the various SoC Blocks shown above.

DFE interfaces with the SoC through the IQN2 module using the AID bus. DFE RX receives JESD-formatted digital channel streams from ADCs over SERDES, and unpacks them into channel containers which are sent to SoC through the IQN2 module. On the TX side, DSP sends digital channel data packed into channel containers to the DFE through the IQN2 block. DFE processes these channel containers into TX streams and after JESD formatting, sends them out to the DAC over SERDES.

DFE TX path provides additional signal processing for TX streams. JESD204B processing is used to synchronize and transport the TX streams across the JESD204B serial data interface to the external transmitter or DAC, which converts it into analog stream for RF up conversion or direct transmission.
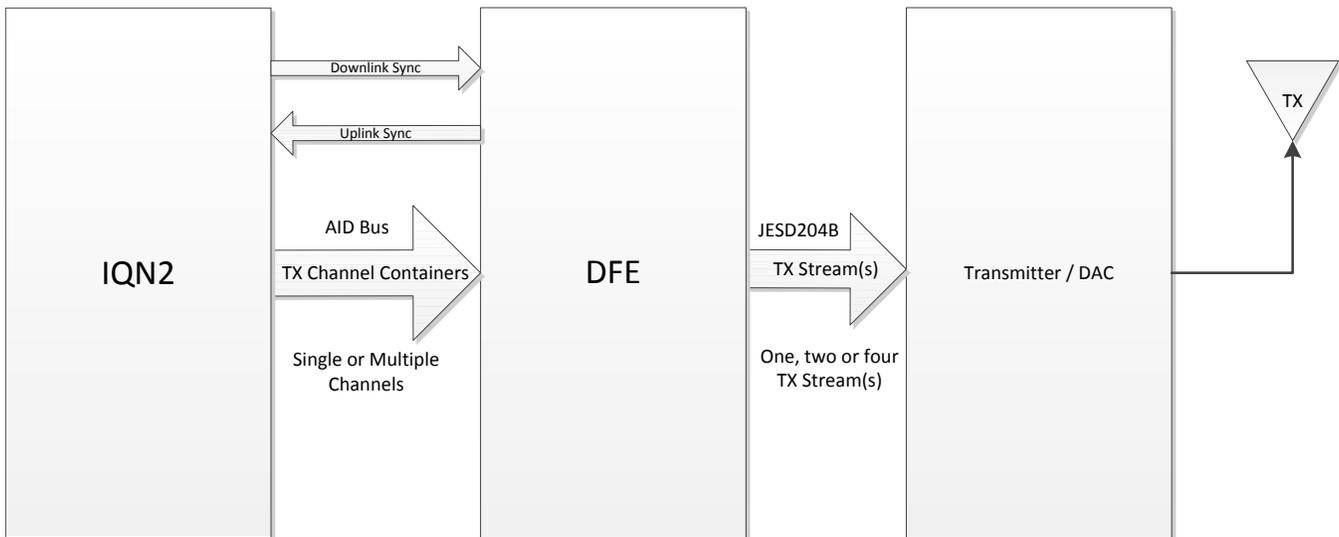
Figure 1-4. DFE TX Signal Processing

DFE RX receives RX streams containing digital (real or complex) RX channel data from ADC sources over JESD204B transport. The received RX streams are processed and converted to the IQNet channel data container format for DSP processing.
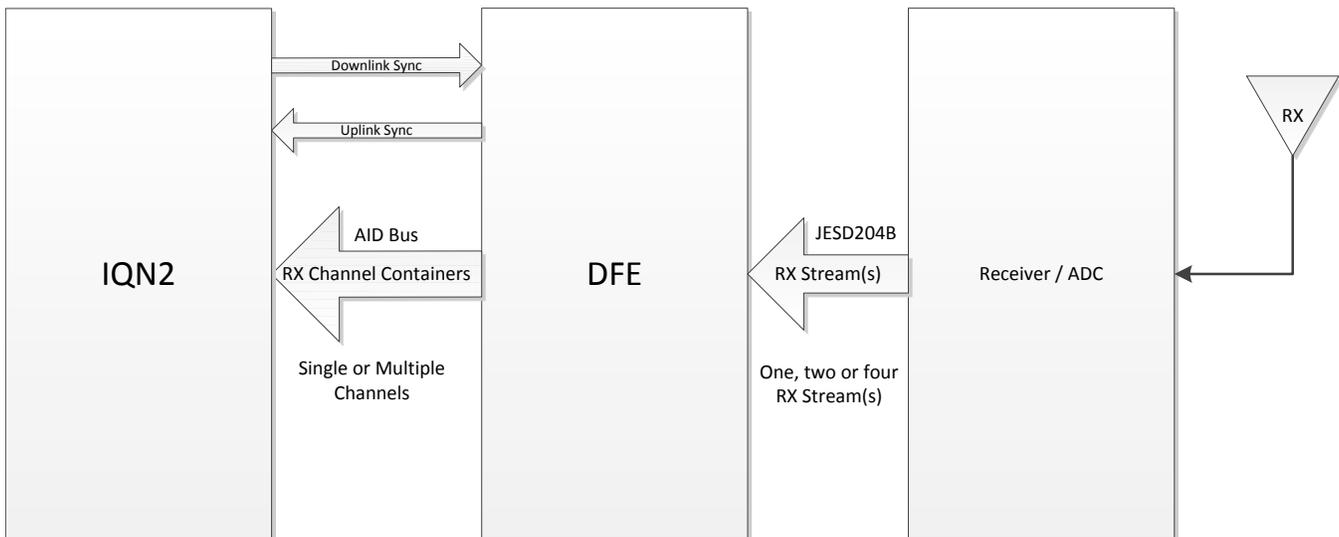
Figure 1-5. DFE RX Signal Processing

The JESD transceiver can provide additional RX signals for wideband monitoring or additional RX capacity. DFE feedback path receives these additional RX streams, which can be used either for TX signal capture for DPD processing, or for added RX capacity. The feedback signal is treated like a JESD204B RX stream, but at the JESD204B TX stream sample rate.

1.5 Use Case Examples

The following sections present typical DFE use case scenarios.

1.5.1 DFE with RF Transceiver (DAC+ADC with Integrated RF Front-End)
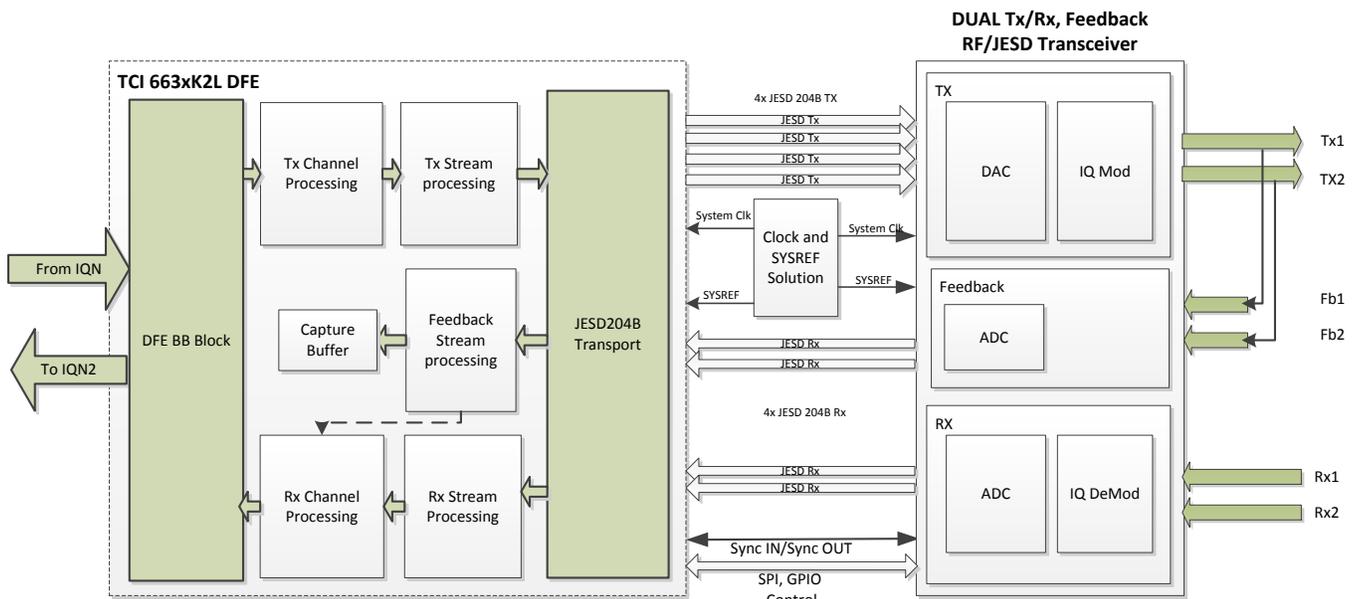
Figure 1-6. DFE with RF Transceiver

DFE can be interfaced directly with Analog Front-End (AFE) devices with integrated RF up/down conversion, for example, in wireless small cell base-stations. In such applications, TX and RX channel data is mapped to antenna streams and antenna carriers:

- **Antenna Stream:** An antenna stream represents a physical antenna and contains TX or RX sample data for a physical antenna. Antenna streams are the equivalent of TX or RX streams referred to in this document.
- **Antenna carrier:** An antenna carrier represents TX or RX sample data for a particular carrier frequency. One or more antenna carriers can be transmitted or received over the same physical antenna; in other words, an antenna stream can contain multiple antenna carriers. Antenna carriers are the equivalent of channel containers referred to in this document.

In DFE TX processing, the antenna carriers are gain corrected, filtered, interpolated, frequency translated, and combined with other antenna carriers into an antenna stream. There are additional DFE processes for each TX antenna stream including CFR, DPD, IF frequency translation, and JESD204B data transport.

In RX side, the JESD transceiver down-converts, digitizes, and processes the RF signal, then formats and outputs the JESD204B complex stream. DFE receives the RX stream (antenna stream) and applies further signal processing, including digital block down conversion and channel down conversion. The down conversion process includes frequency translation, switching, IQ rate reduction, filtering, and RX complex equalization. The RX channel data is then sent to IQNet for conversion to an antenna container. The RX processing rate for UL is the same as the TX rate, or ½ the JESD TX equivalent rate.

The DFE feedback RX path captures samples from the transmit side. This data is utilized for DPD to linearize the power amplifier output. This path can also be used as an additional receive path to add extra receive capacity (shown by a dotted line in Figure 1-6). More details about DFE TX and RX signal processing are given in further sections.

1.5.2 Discrete DAC and ADC

DFE can connect to discrete JESD204B analog-to-digital and digital-to-analog data convertors which are synchronized using the two sets of JESD sync signals provided by the DFE. The clock and SYSREF solution provides phase-aligned system clock and SYSREF to the DFE (SoC), ADC, and DAC. Typically, the feedback RX stream adds additional RX capacity in this case, so the feedback RX stream processing output is sent to DDUC for RX channel processing as shown.
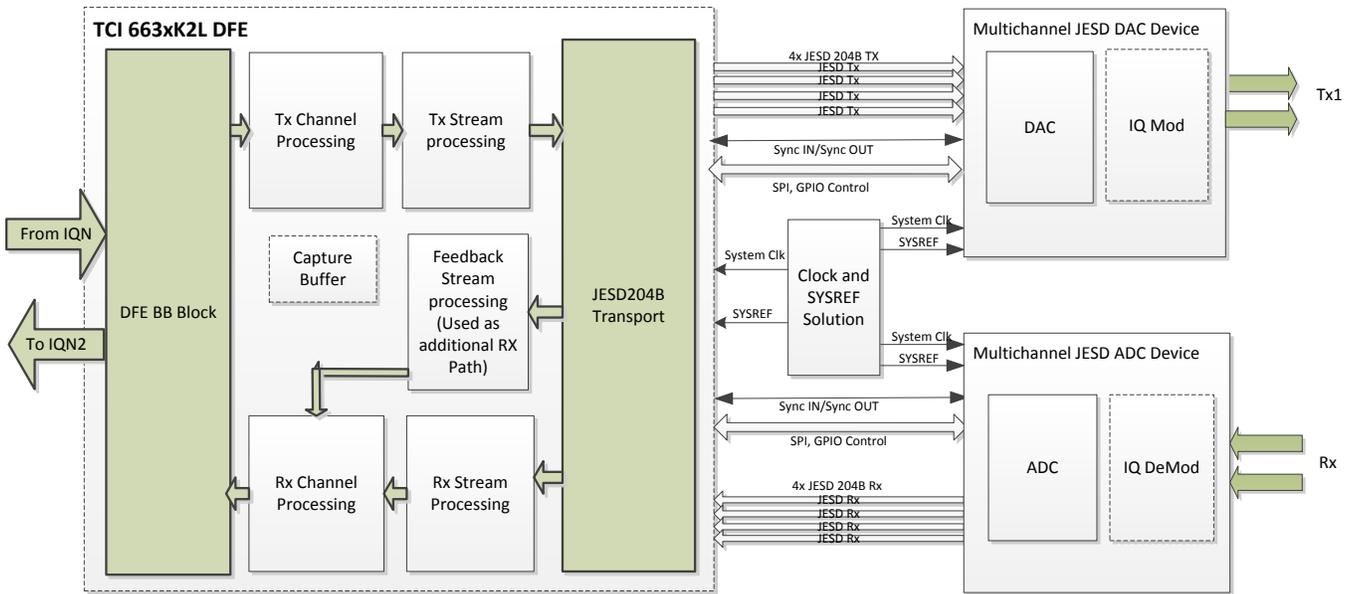
Figure 1-7. DFE with Discrete DAC and ADC

1.5.3 Discrete ADC with DFE Bypass

The various signal processing blocks inside the DFE can be bypassed as shown in Figure 1-8. This allows the DFE to interface with JESD204B-based data convertors in applications involving specialized signal processing, which may be performed on DSP and other accelerators such as FFTC. These applications usually include signal acquisition over a wide bandwidth, such as medical imaging (ultra sound probes) and sonar. Two multichannel ADC devices can be connected using the two sets of JESD sync signals.
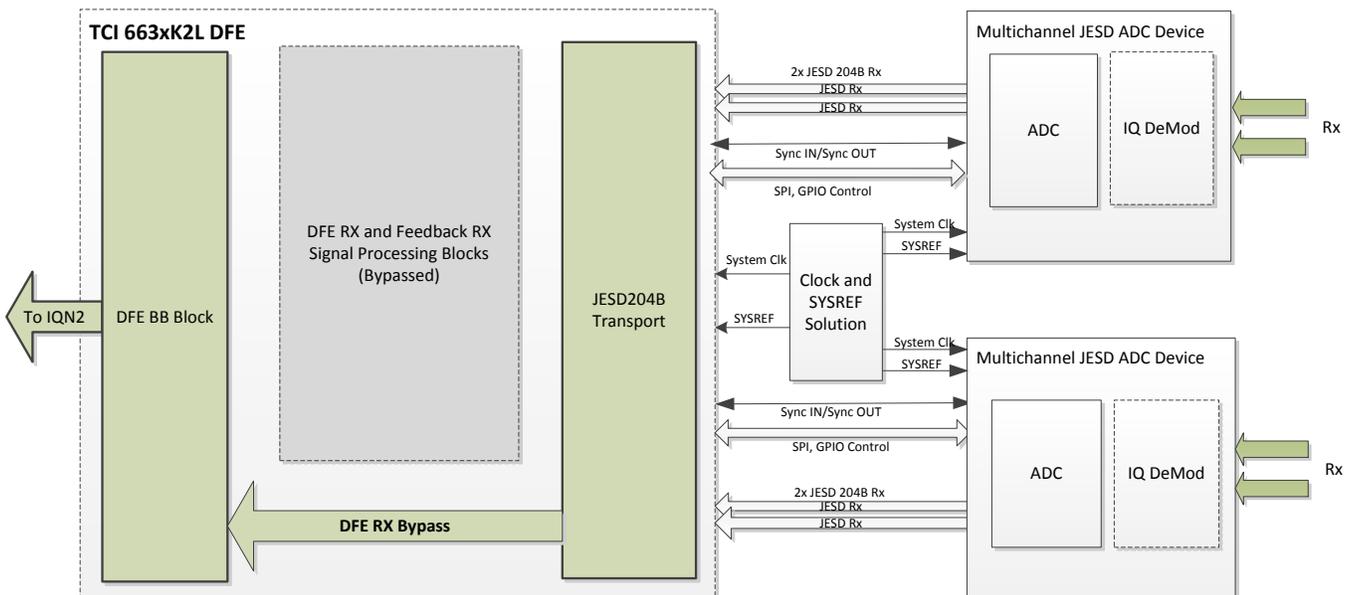
Figure 1-8. DFE RX Bypass

The ADC packs real or complex samples for multiple channels into JESD-formatted RX streams, which are received by the DFE JESD transport block. The JESD transport block unpacks (de-interleaves and decimates if needed) the samples into individual channel containers, which are sent straight to the DFE BB (baseband) block which sends them to IQN2. IQN2 then copies the samples to internal (L2SRAM or MSMCSRAM) or external (DDR3) memory for application processing.

1.6 DFE TX Signal Processing and Frequency Translation

This section shows the DFE frequency translation and processing of antenna containers into antenna streams. The antenna carriers are gain corrected, filtered, interpolated, frequency translated, and combined with other carriers into an antenna stream.

There are additional DFE processes for each TX antenna stream CFR, DPD, IF frequency translation, and JESD204B data transport.

The transmit side frequency translation can be divided into three stages.

1.6.1 TX Frequency Translation Based on a Channel or Carrier

DFE contains 4 DDUC (digital down/up conversion) blocks, each of which can be programmed for transmit (up conversion) or receive (down-conversion) operations and one ratio for interpolation or decimation. In TX operation, the BB block delivers time-interleaved IQ samples to the DUC block, which interpolates the carriers and translates them to individual offset frequencies. The interpolated and frequency-translated carriers are sent to the DFE sum chain, which combines the carriers into a TX stream.

Figure 1-9 shows the frequency translation and combining on a per-channel basis inside the DFE DUC and sum chain blocks.

1. Individual carriers are received for DFE processing. Antenna containers from IQNet are converted to antenna carriers.
2. The individual carriers are interpolated and frequency-translated to an offset frequency. The offset frequency is zero for a single-carrier case.
3. The DFE sum chain combines the individual antenna carriers into an antenna stream.
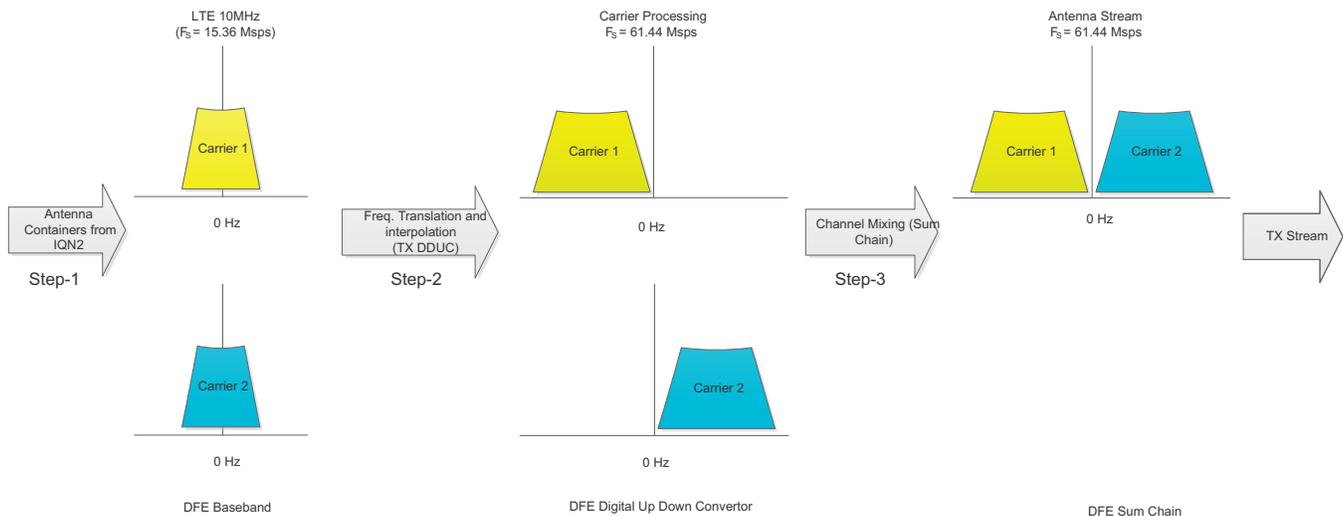
Figure 1-9. DFE TX Channel Processing

The channel processing inside DUC consists of a programmable FIR filter, re-sampler, cascade integrator comb filter (CIC), and a channel complex mixer. The processing has several ratio rules which are based on the number of transmit or receive streams and the number of channels inside the DDUC. These ratio rules are used to define the stream IQ rate.

Number of Transmit or Receive Streams	IQ Rate
1	DFE Clk/2
2	DFE Clk/4
4	DFE Clk/8

1.6.2 *TX Frequency Translation Based on a Stream or Antenna*

On specific versions targeted towards wireless infrastructure applications (such as small cell base-stations), DFE supports additional stream-based functions such as CFR, TX stream bulk up conversion, and DPD. Check the data sheet of your device to find out if these functions are supported.

Figure 1-10 shows the interpolation and frequency translation, as applied after the channel-based frequency translation described in Section 1.5.1, and also shows at what stages CFR and DPD functionality is applied (These modules are described in Chapter 2).

1. The output from DFE sum chain (combined frequency-translated channels) goes through the CFR block, which applies crest factor reduction and then interpolates to the stream rate (post CFR interpolation), as shown in Steps 4 and 5. CFR clips the peaks of the transmit signal to reduce the peak-to-average ratio (PAR), and maintain the desired spectral emission mask (SEM) and adjacent channel power ratio (ACPR).

2. The interpolated TX stream goes through the DPD block and IF frequency translation, then is transported over JESD204B to the JESD transceiver. DPD pre-distorts the TX signal to reduce the intermodulation distortion (IMD) from the power amplifier after the JESD transceiver.

NOTE: On versions that do not support CFR and DPD, the output from the SUM chain is directly interpolated to the stream rate and transported over JESD204B.

Additionally, the DFE TX path also includes PA protection, which limits the peak power or RMS power of each TX stream. The PA protection can also set back the TX gain or inhibit a TX stream output.
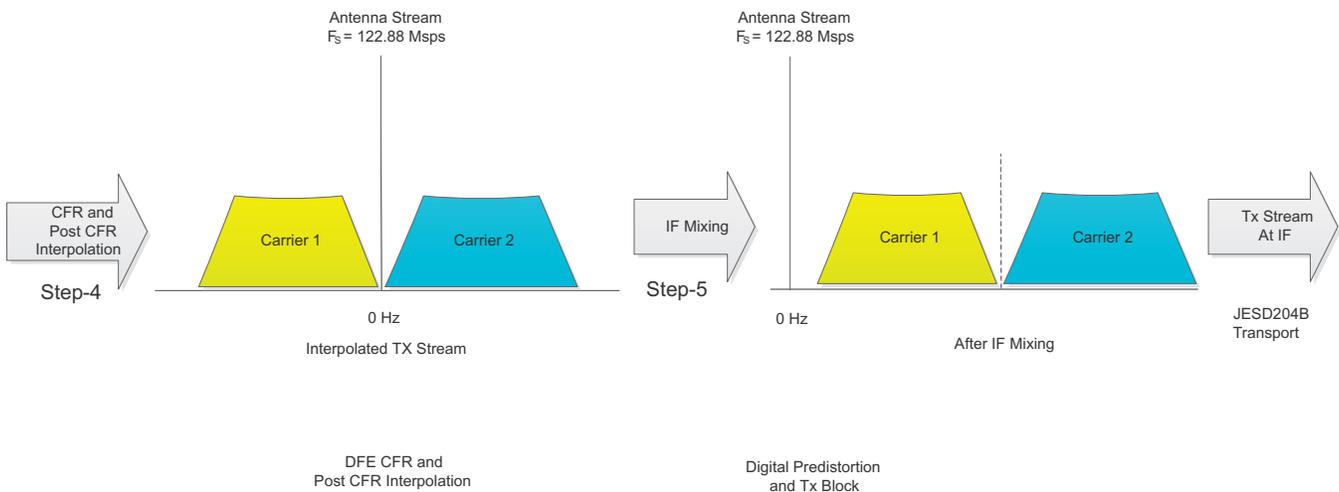
Figure 1-10. DFE TX Stream Processing

1.6.3 *TX Frequency Translation after DFE (Inside the DAC/RF Front-End)*

The last step in the TX chain is the digital-to-analog conversion and direct IQ modulation of the TX stream to the local oscillator frequency. This process is performed in the external DAC or transceiver.

1. The TX stream is transported over JESD204B from DFE to the JESD transceiver.

2. The transceiver performs digital-to-analog conversion of the TX stream and mixes it with the local oscillator frequency (direct IQ modulation).

NOTE: RF Transmit Frequency = Carrier Frequency + IF Frequency + Transmit Local Oscillator

1.7   DFE RX Signal Processing and Frequency Translation

This section shows the DFE frequency translation and processing of antenna streams into antenna carriers. The analog signal is received by the external JESD transceiver, which down-converts, digitizes, and processes the RF signal, then outputs the JESD204B complex stream.

DFE receives the digital RX antenna stream over JESD204B and applies further signal processing, including digital block down conversion and channel down conversion. The down conversion process includes frequency translation, switching, IQ rate reduction, filtering, and RX complex equalization. The RX channel data is then sent to IQNet for conversion to an antenna container.
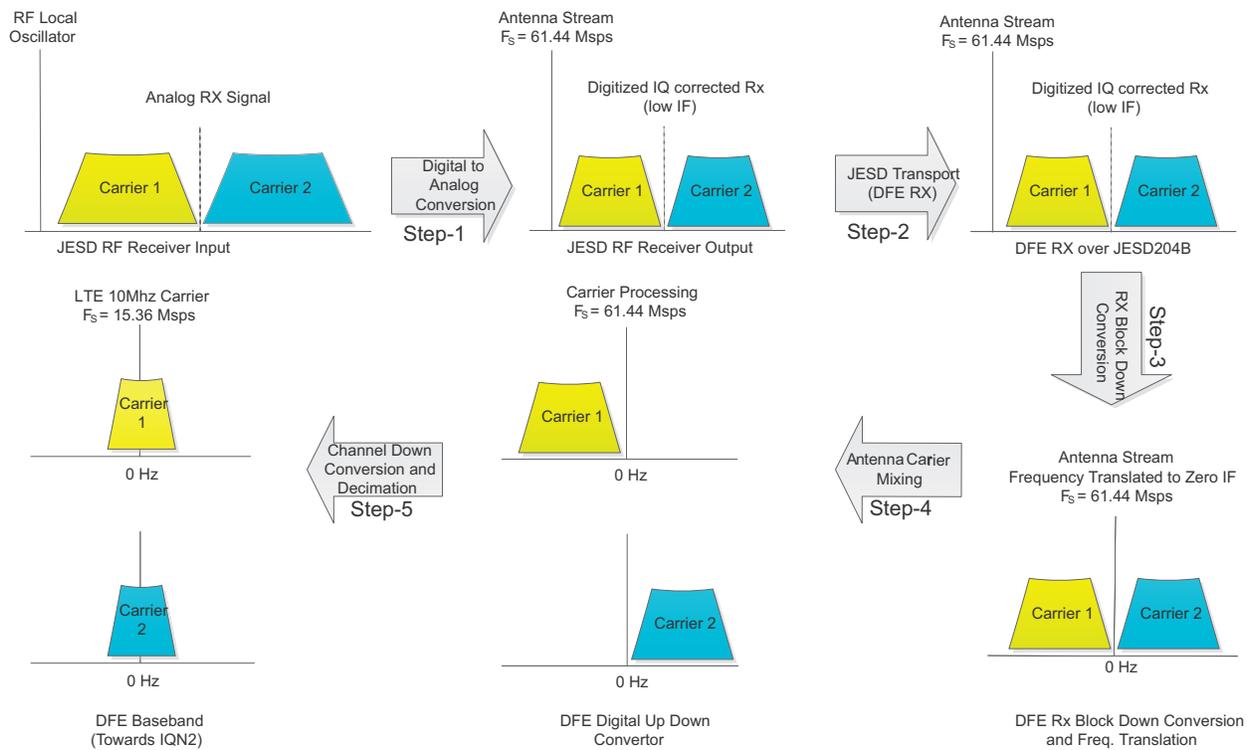
Figure 1-11. DFE RX Processing

Figure 1-11 shows the steps in RX antenna stream processing and frequency translation.

1. RF analog input is received by the external JESD transceiver and frequency translated to low or zero IF (intermediate frequency). The IF is digitized, signal processed, and transported over JESD204B to the DFE.
2. The digital antenna RX stream is received by DFE over JESD204B.
3. DFE translates the intermediate frequency RX stream to zero IF and performs block down conversion.
4. The RX DDUC separates the carriers from the RX stream to individual offset frequencies, and decimates the carriers to the channel baseband sampling rate.
5. The filtered and decimated antenna carriers are gain-normalized and converted to antenna container format to be sent to IQN2, which delivers the RX channel data to the application.

> **NOTE:** RF Receive Frequency = Carrier Frequency + IF Frequency + Receive Local Oscillator

There is an advanced feature in the DFE RX not discussed in the above sections: the JESD-decoded and mapped RX streams are block down converted in the RX sub-block. The block down conversion includes frequency translation, switching, IQ rate reduction and filtering, and RX complex equalization.

1.7.1 *Feedback RX Path*

The DFE feedback RX path captures samples from the transmit side. This data is utilized for DPD calculations to linearize the power amplifier output. This path can also add additional RX capacity.

Similar to the RX path, the feedback RX stream processing starts with the external JESD transceiver, which down-converts, digitizes, and processes the RF signal, then outputs the JESD204B complex stream. The feedback stream is received over JESD204B by the DFE, which performs block down-conversion and frequency translation. The feedback data is then sent to the DFE capture buffer. However, when used as an additional RX path, the output of the feedback RX path is sent to the RX DDUC instead for channel down-conversion and decimation.
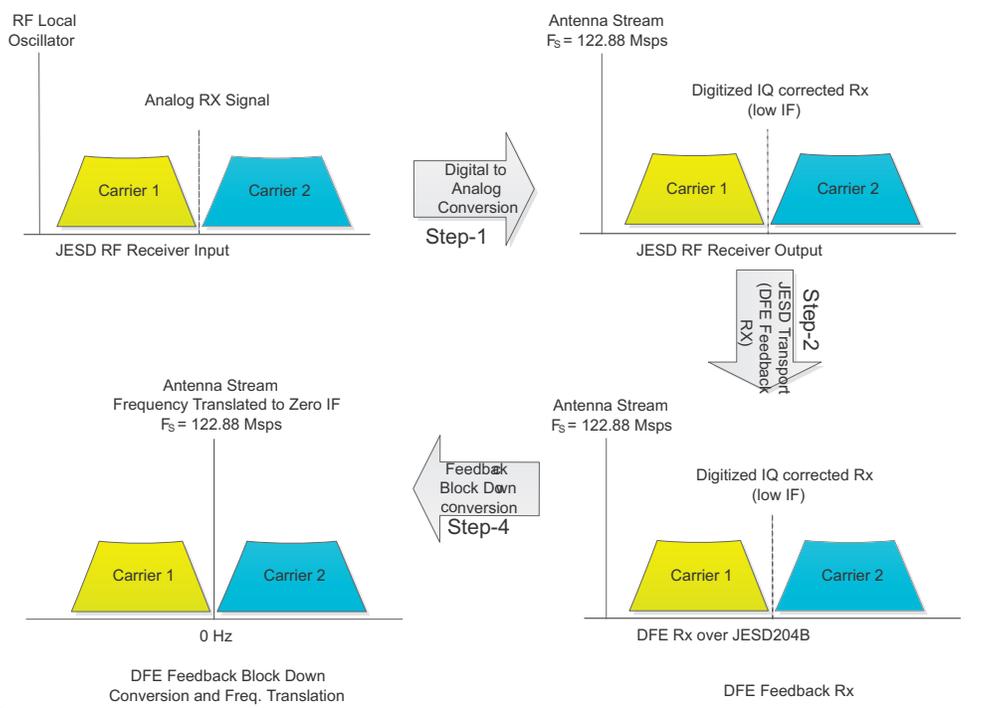
Figure 1-12. DFE Feedback RX Processing

Figure 1-12 shows the steps in feedback RX antenna stream processing and frequency translation.

1. RF analog input is received by the external JESD transceiver and frequency-translated to low or zero IF (intermediate frequency). The IF is digitized, signal processed, and transported over JESD204B to the DFE.

2. The digital antenna RX stream is received by DFE over JESD204B.

3. DFE translates the intermediate frequency RX stream to zero IF, and performs equalization and gain correction. The processed output is captured in the capture buffer.

> **NOTE:** RF Feedback Frequency = IF Frequency + Transmit Local Oscillator

The following additional steps apply when feedback RX is used as an additional RX Path.

1. The feedback RX output from step-3 is sent to RX DDUC, which performs channel down-conversion and decimation.

2. The filtered and decimated antenna carriers are gain-normalized and converted to antenna container format to be sent to IQN2, which delivers the RX channel data to the application.

> **NOTE:** RF Receive Frequency = Carrier Frequency + IF Frequency + Feedback Local Oscillator

1.8   DFE General Input and Output Description

Figure 1-1 shows the interfaces to DFE, and the interconnection to IQNet and SerDes blocks:

1. VBUSP register programming – 32-bit register and memory programming interface (see IQNet Reference 2 - Chapter 3)

2. CTL 32/64-bit DMA data interface from IQNet to DFE, used to stream DFE status, and have a higher BW interface rate to specific DFE registers and memories (see IQNet Reference 2 - Chapter 3)

3. 2 level Interrupt - 2 interrupt signals to IQNet to signal a selected DFE interrupt event (see IQNet Reference 2 - Chapter 3)

4. AID Bus – The main baseband interface for TX and RX BB antenna carriers. The AID bus interfaces between the DFE baseband block, and the IQNet. There are separate single direction flow TX and RX synchronous buses. (see IQNet Reference 2 - Chapter 3)

5. DFE PLL Clock – The DFE and IQNet share a common PLL clock for synchronous operation.

6. SYSREF – A JESD204B frame clock input sourced external to Lamar. SYSREF is distributed from the clock solution to all JESD 204B devices, to align the data frames. (see JESD204B Reference 1 - Chapter 3)

7. SYNCIN – There are one or two JESD204B links in TCI663xK2L DFE. These inputs monitor the JESD204B receiver status from the external JESD204B transceiver (see JESD 204B Reference 1 - Chapter 3).

8. SYNCOUT – There are one or two JESD204B links in TCI663xK2L DFE. These outputs indicate the status of the TCI663xK2L DFE JESD RX devices. (see JESD 204b Reference 1 - Chapter 3)

9. [4] DFE JESD TX Outputs – The DFE has up to 4 TX JESD204B outputs. These TX output buses go to the SerDes for parallel to serial conversion. The 4 JESD204B lanes can be used for 1, 2, or 4 TX antenna streams.

10. [4] DFE JESD RX Inputs – The DFE has up to 4 RX JESD204B inputs. These RX input buses come from the SerDes after serial to parallel conversion. The four JESD204B lanes can be used for 1, 2, or 4 RX antenna streams. The RX antenna streams include the feedback signal.

1.9   TCI663xK2L DFE Boot Mode Considerations

There are two SerDes macros on the TCI663xK2L device, CSISC2_0 and CSISC2_1, and each macro provides two SerDes lanes, making for a total of 4 lanes on the device. DFE shares SerDes resources with IQNet AIL (antenna interface lanes). The SerDes lanes corresponding to CSISC2_0 are multiplexed between IQN2 AIL (used for CPRI interface in wireless base-station applications) and DFE JESD lanes 0 and 1, as shown in Figure 1-13.

The multiplexing of these lanes between IQN2 AIL and DFE is controlled at using a Boot Mode control.

Additionally, TCI663xK2L DFE has two LVDS inputs normally associated with the JESD204B SYNCIN signals. When IQN2 is configured for AIL usage (CPRI), these two LVDS signals can be repurposed to IQN sync signals using pin mux Control.

The BOOT MODE multiplexers for DFE and IQNet are shown in Figure 1-13. The Boot Mode and pin mux controls are discussed in the TCI663xK2L SoC Data Manual (SPRS893).
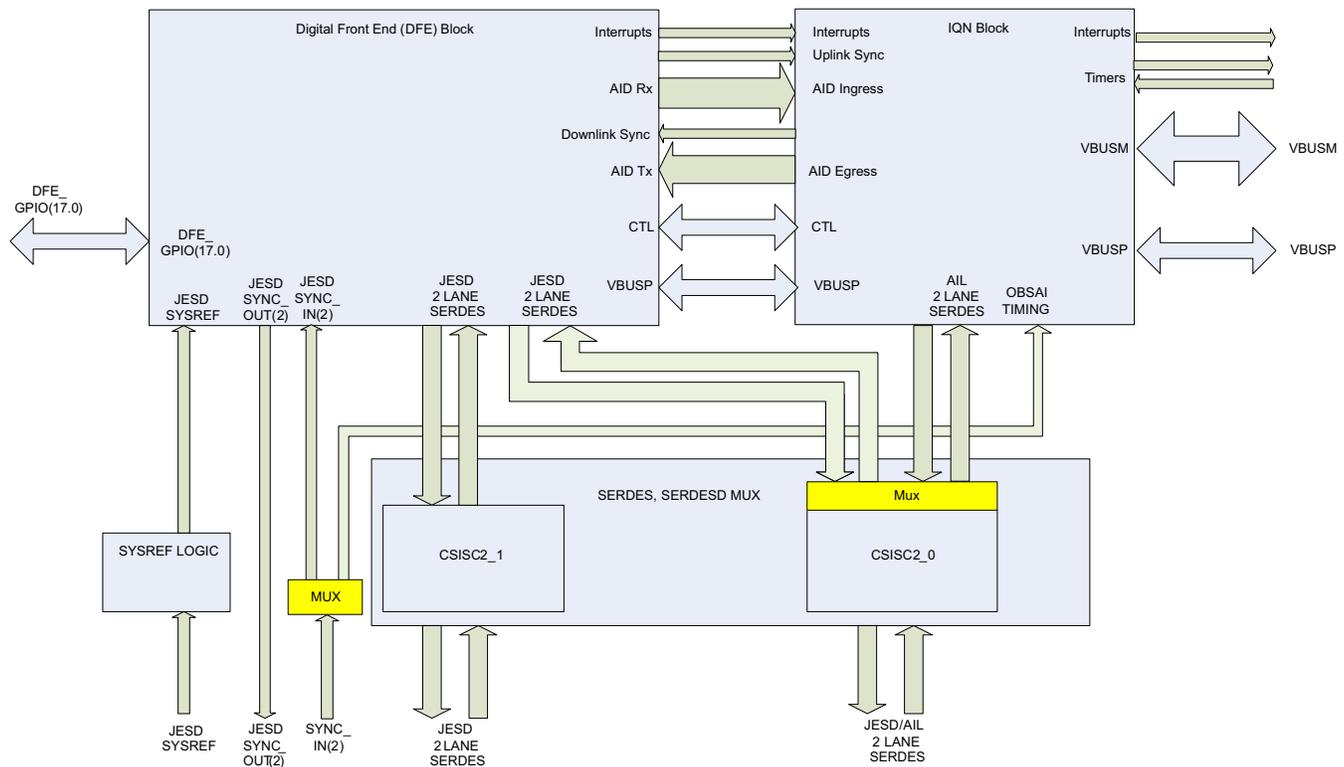
Figure 1-13. Boot Mode Shared Data Multiplexers IQNet and DFE

1.10 SYSREF Logic outside DFE

In Figure 1-13 the SYSREF Logic is used to sample the external LVDS SYSREF signal with SYSCLK, and provide this signal to DFE. The SYSREF logic can also generate a test SYSREF signal used for factory tests.

The SYSREF logic register programming is discussed in the TCI663xK2L SoC Data Manual, Reference 4 (Chapter 20).

1.11 DFE Power Domains

The DFE has three power domains as shown in Table 1-1. The numbers shown in the table are for listing purpose only; the actual power domain numbers are device-dependent. Check the device-specific data manual.

Table 1-1. Power Domains in DFE

Power Domain	DFE Sub-blocks Serviced
PD1	Baseband; (4) DDUC; SumChain; CFR; CDFR
PD2	DPD
PD3	TX; JESD; RX; Feedback

Normally all three power domains are powered up. If DPD is not used, PD2 can be turned off, in which case the TX block is configured accordingly.

The power domain controllers are discussed in the device data manual.

1.12 TCI663xK2L DFE JESD204B SerDes Lanes

The TCI663xK2L and JESD 204B transceivers can be used in two antenna or four antenna configurations. Figure 1-14 shows the two antenna configuration, while Figure 1-15 shows the four antenna configuration with multiple JESD 204B transceivers. Table 1-2 shows the number of SerDes lanes for a specific transfer rate and the number of antennas supported for the rates.

The SYSREF and SYSCLK provide the frame synchronization and clocking. The JESD SyncIn and SyncOut also are used for JESD204B synchronization and error notification. See Reference 1 in Chapter 3 for the JESD204B requirements for SYSCLK, SYSREF, SYNCIN, and SYNCOUT functions.

The TCI663xK2L DFE processes parallel IQ data. The data is passed to the SoC SerDes modules for serialization and other processing. The SoC SerDes has its own PLL and IQ transfer logic. The SerDes configuration must match the intended DFE SerDes rates.

The two antenna configuration can use two or four SerDes lanes. The four antenna configuration uses four SerDes lanes. The SerDes SoC blocks are discussed in the SerDes User Guide, Reference 3 (Chapter 3).

Table 1-2. Example Tx-Fdbk, Rx IQ Rates with JESD 204B Transport

Number Tx/Rx Antennas	Number SerDes Lanes	SerDes Rate	Equiv. Tx/Fdbk IQ Rate	Equiv. Rx IQ Rate
2	2,3(w/Fdbk)	2.4576G	61.44M	61.44M
2	2,3(w/Fdbk)	3.6864G	92.16M	92.16M
2	2	4.9152G	122.88M	61.44M
2	2,3(w/Fdbk)	4.9152G	122.88M	122.88M
2	2	7.3728G	184.32M	92.16M
2	4	3.6864G	184.32M	92.16M
2	4	4.9152G	245.76M	122.88M
2	4	7.3728G	368.64M	184.32M
4	4	4.9152G	122.88M	61.44M
4	4	7.3728G	184.32M	92.16M
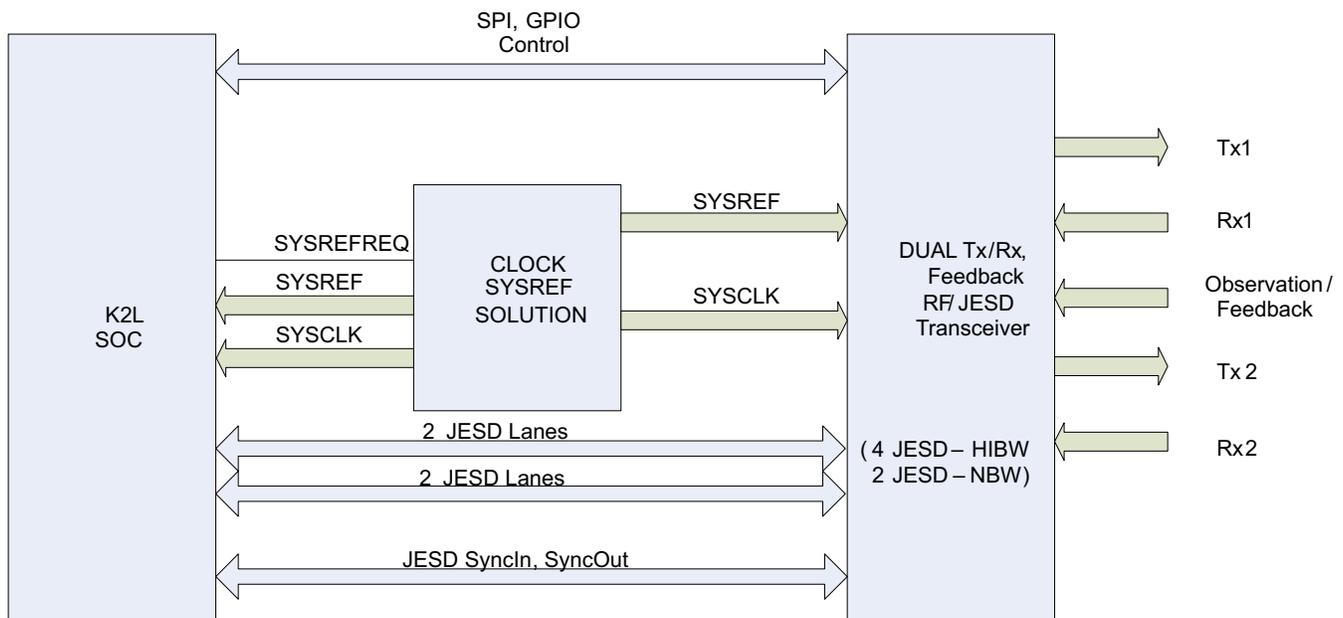
Figure 1-14. TCI663xK2L DFE to Two Antenna JESD Transceiver Block Diagram
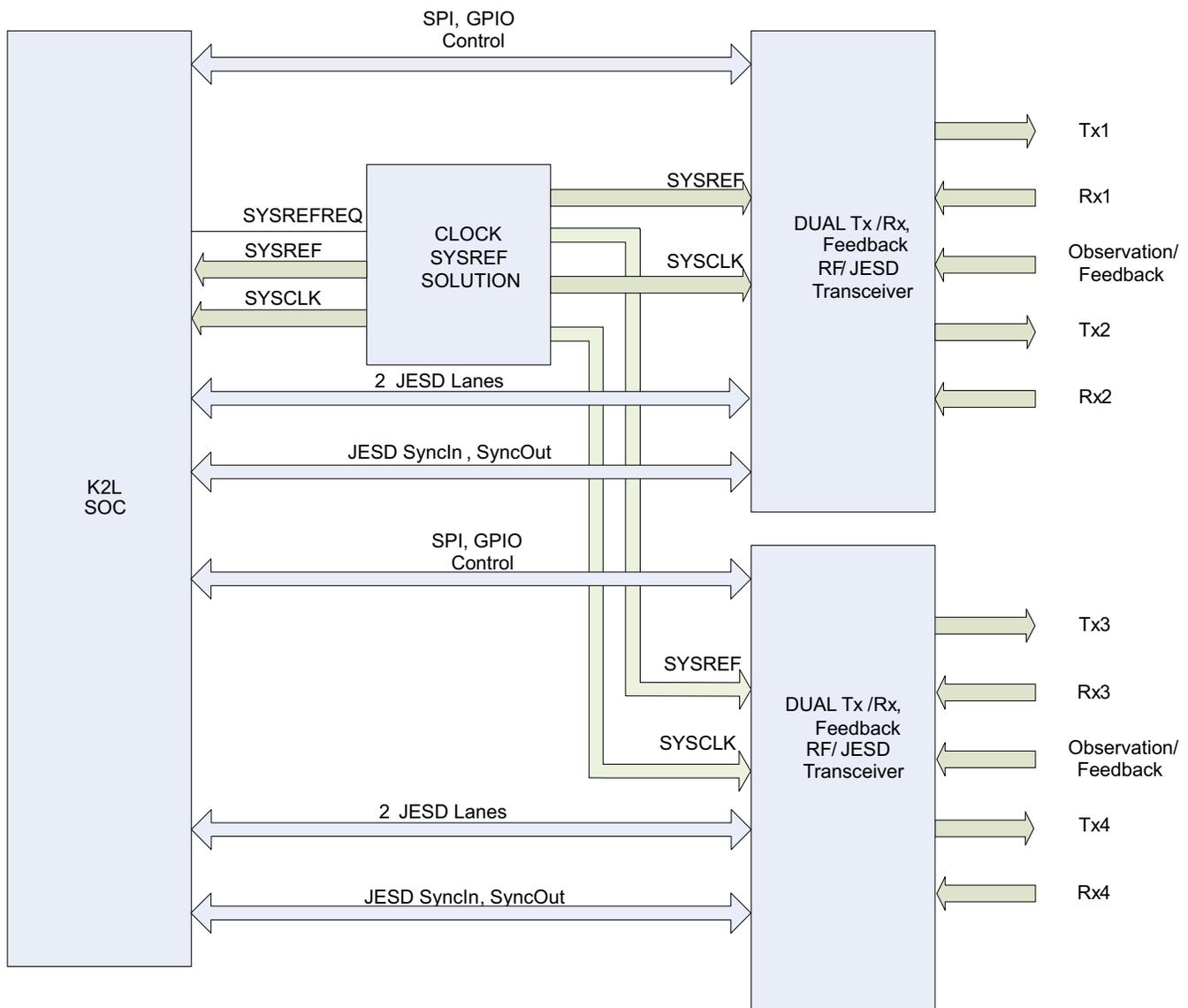
Figure 1-15. TCI663xK2L DFE to Four Antenna JESD Transceiver Block Diagram

1.13 TCI663xK2L DFE and IQNet Clock

The DFE block operates synchronously with the IQNet block, and both blocks share the DFE PLL. The DFE block must be programmed for the appropriate clock output. The PLL is operated at either 245.76 MHz or 368.64 MHz. The DFE and IQNet configurations must be compatible to the selected DFE PLL value.

The DFE PLL for TCI663xK2L is described in the TCI663xK2L Data Manual (SPRS893).

1.14 TCI663xK2L DFE GPIO Shared with Other SoC Functions

The TCI663xK2L DFE GPIO signals are shared with other TCI663xK2L SoC GPIO signals. The selection of GPIO controls is discussed in the TCI663xK2L Data Manual, Reference 4. The programming details of the TCI663xK2L DFE GPIO signals are found in the MMR tables in . The TCI663xK2L GPIO pins are also multifunctional within DFE. They are discussed later in Section 2.12.

There are additional TCI663xK2L SoC counter timer and GPIO pins that can also be used for control. The timer control and GPIO selection are discussed in Reference 4. The two general uses are:

- DFE_GPIO, SoC_GPIO – JESD transceiver hardware trigger signal
- SoC_Counter_Timer – JESD transceiver hardware real time trigger signal

1.15 TCI663xK2L DFE Sub-Blocks and Functions

Chapter 2 has sub block data flow (TX, RX, and feedback), and discussions of each DFE sub block. The DFE block diagram is shown in Figure 1-16. Table 1-3 lists the DFE sub block abbreviation, name, and function.

Table 1-3. DFE Sub-Block Functions

DFE Sub-Block Abbrev. (xxxx – DFE Main Flow Tx,Rx,Fdbk)	DFE Sub-Block Name	DFE Sub-Block Function
BB (Tx,Rx)	BaseBand	Receives and transmits the AID bus, antenna container (Axc) data to/from IQN. Formats the BB antenna carrier data for the DDUCs. Provides antenna carrier fine gain control.
DDUC (Tx,Rx)	Digital Down Up Converter	Provides antenna carrier frequency translation; provides IQ filtering and rate conversion from the baseband rate to the antenna stream rate; there are 4 DDUCs; 2 Tx and 2Rx
SC (Tx)	SumChain	Combines the Tx DDUC antenna carriers into an antenna stream; provides 6db step gain control of the Tx antenna stream
CFR (Tx)	Crest Factor Reduction	Provides peak clipping of each Tx antenna stream, interpolation, and circular clipping (final limiter) from the SC to the CDFR rate. Provides for Tx antenna stream fractional gain before CFR; provides for Tx antenna stream fractional gain after CFR
CDFR (Tx)	CFR DPD Fractional Resampler	Resamples the CFR output to the DPD IQ rate of each Tx antenna stream
DPD (Tx)	Digital PreDistortion	Applies per Tx antenna stream, a nonlinear feed forward correction to the Tx Each Tx can have a unique set of DPD correction coefficients.
Tx (Tx)	Transmit	Provides Tx antenna stream IF frequency translation, provides a PA protection function for each Tx antenna stream
JESD (Tx,Rx,Fdbk)	JESD204B Tx, Rx transport	Provides the multilane, multilink JESD 204B transport from digital IQ for Tx and Rx/Fdbk, provides for local lane loopback for testing, provides separate Rx block and Fdbk block outputs
Rx (Rx)	Receive	Receives Rx streams from JESD performs Rx block down conversion, IF frequency translation, stream switching, decimation filtering, equalization and formatting for Rx DDUC
Fdbk (Fdbk)	Feedback	The feedback block provides different parameters for a selected feedback signal. The feedback block has signal selection, equalization, frequency translation, and gain normalization for the capture buffer wideband output. The Feedback block has an additional decimation filter and signal formatter to send data to the Rx DDUC for Network Listening Mode.
CB (Fdbk,other)	Capture Buffer	Capture buffer collects 1 to 4 sets of signals based on timed delay, and signal statistic information. The capture buffer can also source data to specific DFE sub blocks.
MISC (other)	Miscellaneous – GPIO, CPP, VBUSP2MPU	The CPP provides the DMA interface to and from the DFE. The VBUS2MPU provides the programming interface to the DFE sub blocks. The GPIO logic, and counter timers are used to provide control GPIO outputs depending on user application. The DFE GPIO pins can also be used as generic SoC GPIO pins.
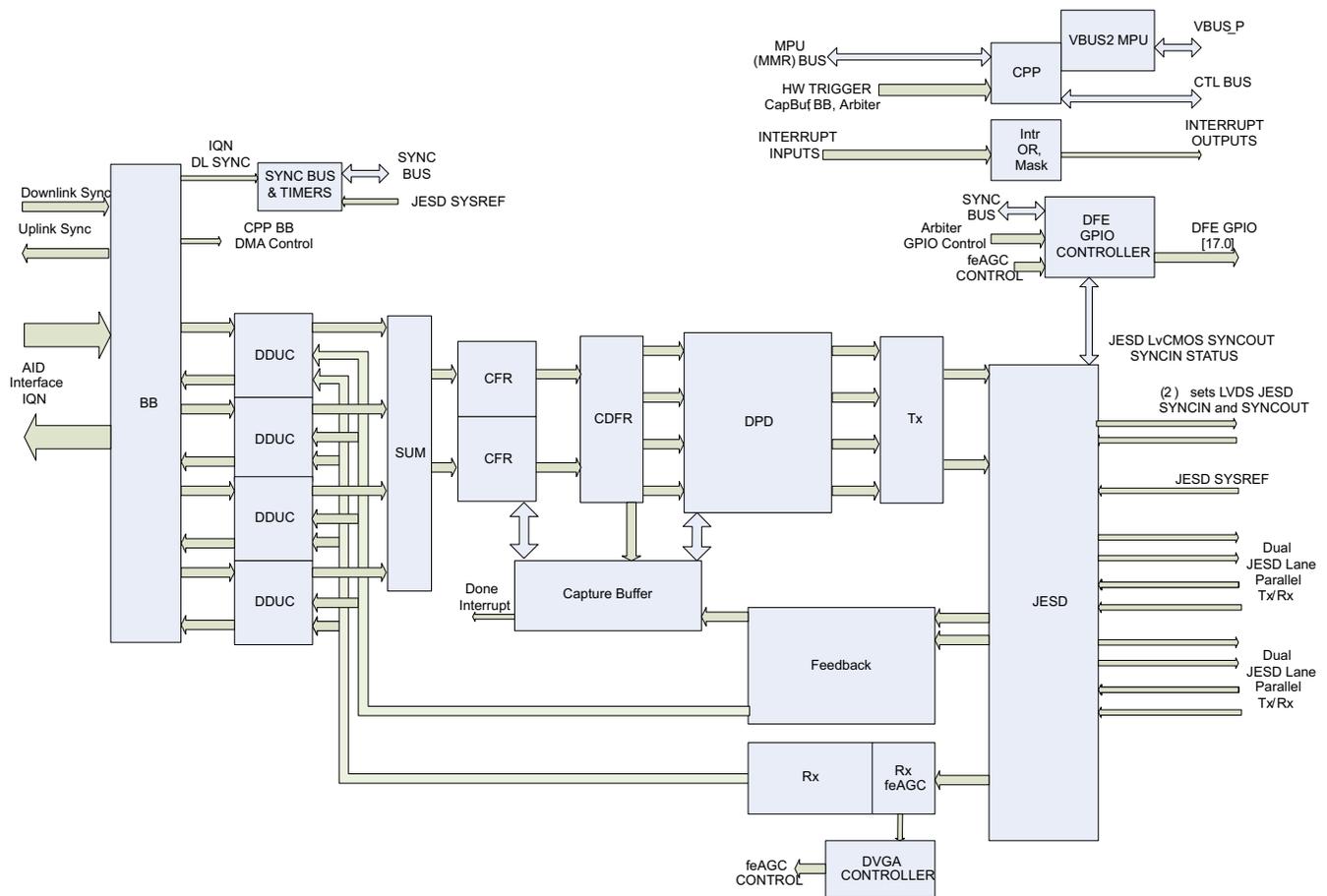
Figure 1-16. TCI663xK2L DFE Block Diagram

1.16 DFE Sub-Block Capacity Considerations

The DFE capacity can be divided into several sections (See Figure 1-9):

- Antenna capacity – The TCI663xK2L DFE supports one, two, or four TX and RX antennas. The feedback can be one or two antenna inputs. The antenna data is transported over JESD204B lanes. The number of SerDes lanes and the SerDes rate for each antenna can change the JESD204B SerDes usage.

- The antenna data is transported over JESD204B TX and RX SerDes links. Table 1-2 lists the most common SerDes data rates. The JESD transceiver and TCI663xK2L must be programmed for the same data interleaving and SerDes rates. The most common IQ rate for TX is 122.88 or 245.76 Mhz. The Fdbk IQ rate matches the TX IQ rate. The RX IQ rate either matches the TX IQ rate, or is ½ the TX IQ rate.

- There are 4 DDUCs within the TCI663xK2L DFE. Typically, two are used for TX and two are used for RX. Each DDUC can have from 1 to 12 carriers, but the TX output must conform to a common IQ rate, and the RX input must have a common IQ rate. Typical DDUC configuration has 1 to 6 channels with a DFE clock/4 IQ interface rate to the sum chain or RX block. Another typical configuration is a DDUC with 8 or 12 channels, with a DFE clock/8 IQ interface rate to the sum chain or RX block. Each DDUC for TX or RX must have a common interpolation (BB -> SumChain) or decimation (RX block out -> BB) ratio. The DDUC output to the sum chain has individual carriers, frequency translated. The DDUC input from the RX block has an RX, or Fdbk (NLM) has an RX stream of one or multiple carriers. The signal bandwidth (BW) is usually limited to 80% of the IQ interface rates listed above.

- The DDUC contains a PFIR (Programmable FIR Filter), re-sampler, CIC filter, and channel mixer. The PFIR has programmable coefficients. Each DDUC has a filter memory that can have one or more

filters, and an index for each channel. There are limitations to the PFIR coefficient size, depending on the number of filters stored, the number of channels in the DDUC, the IQ rate of the channel, and the DFE PLL rate. This can limit the number of DDUC channels, if a specific number of PFIR taps are desired.

- The BB to DDUC interface can support one or two signal IQ rates, where each DDUC has a common IQ rate. The number of channels and the IQ rate per channel must satisfy the following:

$$(2 \times \text{Number of Channels} \times \text{Channel IQ Rate}) \le \text{DFE PLL clock.} \tag{1}$$

- After the TX sumchain, the CFR block provides interpolation, peak clipping in multiple stages, and post-CFR interpolation. After CFR interpolation, the IQ rate DFE Clock/2 for two antennas and DFE Clock/4 for four antennas. A typical post CFR interpolation factor of 2 translates to up to 40% bandwidth after post CFR interpolation.

- CFR clipping is normally based on four successive peak clipping stages. The amount of CFR clipping is based on the introduced EVM in subtracting the in-band signal from the TX antenna stream. Once the EVM target is determined and the EVM budget is assigned to the digital TX stream, the amount of CFR clipping can be adjusted, during run time, by adjusting the sum shift gain, preCFR gain, and monitoring the Tx power meter.

- The CDFR block fractionally interpolates the CFR output to the desired DPD rate. The desired DPD rate is typically equal to DFE clock, DFE clock * 2/3, or DFE clock/2. Since the interpolation after CFR and CDFR is done to provide the DPD IQ rate, the CDFR output rate is typically ≥ 3 × the signal BW. If DPD is not used, the CDFR can operate the DPD block at a lower IQ rate. The DPD expansion ratio (≥ 3) * signal BW must fit to the DFE clock ratios available. Operating the DFE PLL at 368.64 vs. 245.76 provides more DPD IQ rate (which is used for DPD with a higher signal BW).

- There are four discrete sections for DPD, so each TX stream can have a unique nonlinear correction. Within DPD, the number of calculated solutions and memory taps can be optimized for specific system usage. The most common setup is three calculated solutions (different functions at the same time) and up to six memory taps for four antenna, or 12 memory taps for two antenna. Typically the hardware configuration is for the maximum solution and memory size, while the software adaptation can choose to update a smaller portion of the available resources.

- The TX block fractionally decimates or filters the DPD nonlinear processed signal to the desired JESD rate. See Table 1-2 for the equivalent IQ rates for the JESD204B antenna streams.

- The TX block has a PA protection logic that must be set for the desired rms or peak limiting mode. The block can be bypassed.

- The RX block takes the RX antenna streams, provides IF mixing, and provides decimation filtering to match the RX DDUC interface rate (DFE Clk/4 for 2 antenna, DFE Clk/8 for 4 antenna). The signal BW can be at most 80% BW after the decimation filtering. The RX block receives the JESD 204B reformatted RX streams, at the TX IQ rate, or TX/2 IQ rate (when two RX streams are interleaved within one JESD204B stream). The RX decimation matches the desired output format for the RX DDUC to the JESD RX rate.

- The Fdbk block takes the Fdbk antenna stream from the JESD block, provides equalization, IF mixing, and gain for the wideband capture in the capture buffer. The capture buffer length and the TX = Fdbk IQ rate determine the amount of time that the software can sample the TX path for DPD adaption. Typically, the capture buffer collects the DPD input and feedback, or DPD output and feedback, to synchronously capture the DPD signal and the delayed in-time feedback.

1.17 Example 2 and 4 Antenna Configurations

The RFSDK user guide discusses the configuration selection and API modification of DFE variables. Table 1-4 discusses some specific 2 and 4 antenna configurations based on wireless applications for typical LTE channels and bandwidths. The carrier types listed are per antenna values.

Example 2 and 4 Antenna Configurations www.ti.com

Table 1-4. Example TCI663xK2L JESD Transceiver IQ Rates, Num Antennas and Carriers/Antenna

Num Antenna Tx/Rx	BB Mode	LTE20	LTE10	LTE5	WCDMA	TxIQ Rate	RxIQ Rate
2	Single	1				122.88	61.44
2	Single		2			122.88	61.44
2	Single			4-5		122.88	61.44
2	Single				4-5	122.88	61.44
2	Single	2[1]				245.76 184.32[1]	122.88 92.16[1]
2	Single		4-5			245.76 184.32[1]	122.88 92.16[1]
2	Single			7-8		245.76 184.32[1]	122.88 92.16[1]
2	Single				7-8	245.76 184.32[1]	122.88 92.16[1]
2	Dual	1[1]	1-2			122.88	61.44
2	Dual	1		2-3		122.88	61.44
2	Dual	1			2-3	122.88	61.44
2	Dual		1-2	2-3		122.88	61.44
2	Dual	1	2-3			245.76	122.88
2	Dual	1		2-3		245.76	122.88
2	Dual	1			2-3	245.76	122.88
2	Dual		2	2 -3		245.76	122.88
4	Single	1				122.88	61.44
4	Single		2-3			122.88	61.44
4	Single			3-4		122.88	61.44
4	Single				3-4	122.88	61.44
4	Dual	1(sp)[2]	1			122.88	61.44
4	Dual	1(sp)[2]		1-2		122.88	61.44
4	Dual	1(sp)[2]			1-2	122.88	61.44
4	Dual		1	1-2		122.88	61.44
4	Dual		2(sp)[2]	1-2		122.88	61.44
4	Dual		2(sp)[2]		1-2	122.88	61.44
4	Dual			4(sp)[2]	4(sp)[2]	122.88	61.44

(1) the DFE PLL is set to 368.64Mhz

(2) the PFIR number of taps may be limited, and/or Network Listening Mode (NLM) may not have enough DDUC capacity to have an additional RxDDUC channel

DFE Flow and Sub-Block Descriptions

This chapter provides three color-coded versions of DFE block diagram: one for TX, one for feedback, and one for RX. These figures and the first pages of this section include flow discussions between the DFE sub-blocks.

Topic **Page**

2.1   Signal Flow

The signal flow in Figure 2-1 for TX goes from IQNet through the AID interface to the baseband block. The baseband reformats and deinterleaves the IQ data for the TX DDUCs. The DDUC converts antenna containers to filtered, interpolated, and upconverted carriers. The sumchain combines one to several DDUC channels into a digital IQ stream. The CFR block provides for peak clipping and usually post-CFR interpolation. The CDFR interpolates the CFR output to the DPD processing rate. The DPD block provides nonlinear correction for each TX antenna stream. The TX block resamples the TX antenna streams to the JESD IQ rate. The JESD block formats the IQ data to the JESD 204B standard.

In Figure 2-1, the purple color indicates TX elements.
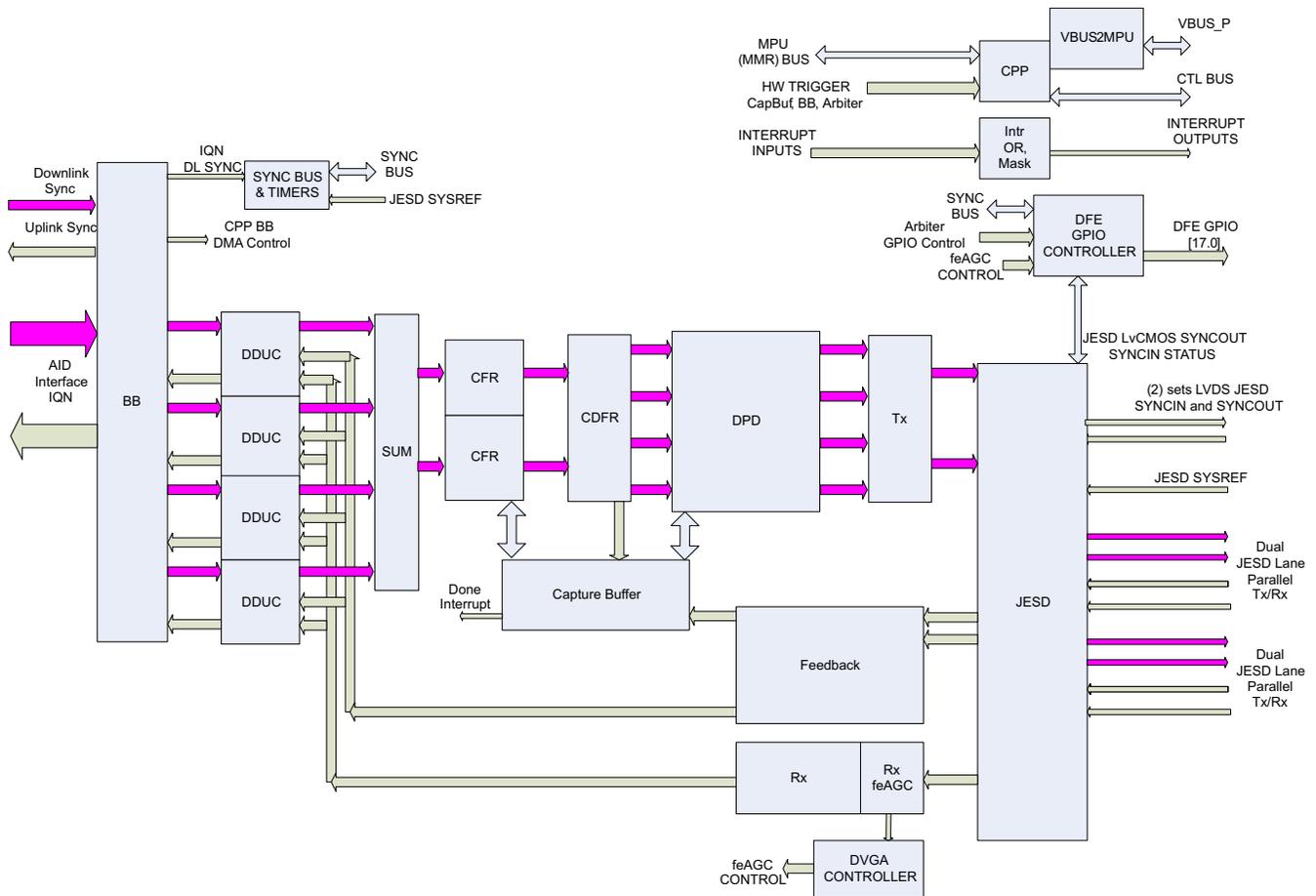
Figure 2-1. DFE Block Diagram – TX Flow

Refer to Figure 2-2 for RX channels. The receive antenna inputs come from the JESD transceiver and are received in the JESD block. The JESD block format and mapping convert the JESD receive data into the RX antenna streams. The RX sub-block provides a block down conversion and RX equalization of each RX antenna stream. The RX stream outputs are sent to each RX DDUC, where the channel-down conversion, filtering, and decimation or resampling are performed. The IQ data is passed from the RX DDUC to the baseband block. In the RX direction, the baseband block converts the buffered IQ data to the baseband block AID interface formats. The IQNet takes the RX AID data and forwards this for antenna-carrier RX processing.

In Figure 2-2, the purple color indicates RX and network listening elements.

Figure 2-2. DFE Block Diagram – RX Flow

The feedback block takes the JESD RX data received, and with the appropriate mapping, up to two feedback IQ data sets are sent to the feedback sub-block (see Figure 2-3). The feedback block selects one of the two feedback inputs for processing. The feedback sub-block has block down conversion function, equalization, tuning, and decimation filtering for network listening mode, where the IQ data is sent to the RX DDUC (see Figure 2-2). The feedback block equalization and tuning and gain then process the wider band feedback signals for collection in the capture buffer.

In Figure 2-3, the purple color indicates feedback elements.

Figure 2-3. DFE Block Diagram – Feedback Flow

2.2   Baseband Block (BB) in DFE
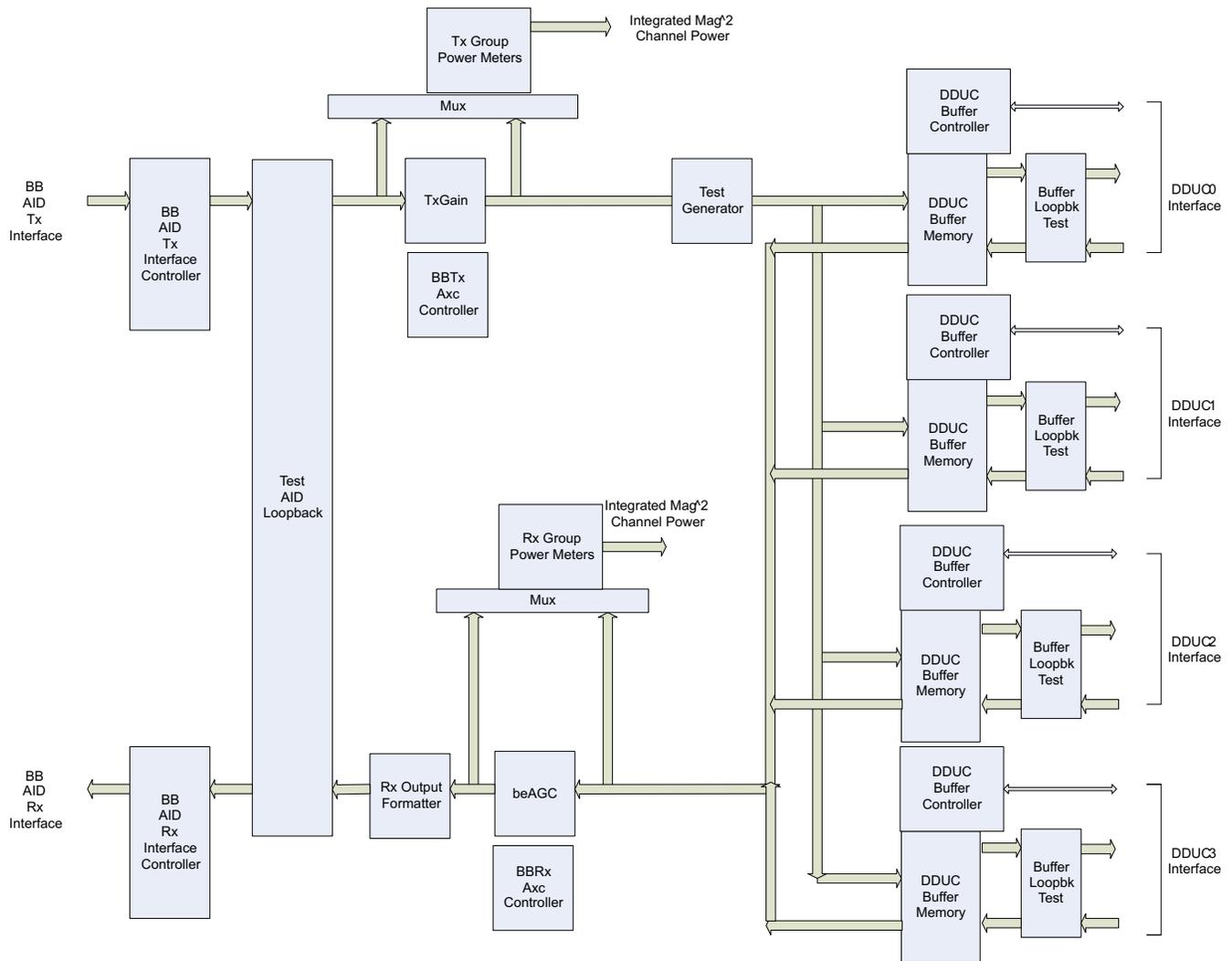
Figure 2-4. BB Block Diagram

2.2.1   *Function*

Baseband (BB) logic block within DFE provides the IQ interface to the IQN2 block over the AID bus. The AID bus TX receiver has a direct loopback-test to the AID bus RX transmitter (see Figure 2-4)

The BB block receives the TX AID Axc carrier data, provides a baseband complex gain for each Axc channel, and utilizing the BBTx program sequence parses the TX Axc carriers to the DDUC TX input buffers. The TX Axc carrier data is 16-bit IQ data. Each TX Axc channel has power meter monitoring.

The TX signal path can have a test signal substituted for the IQ input.

The BB block receives the RX DDUC buffer IQ data, and parses this data into the RX Axc carrier stream. The BBRx section provides for fixed and adaptive gain. The pre- or post-gain RX Axc signals have power meter monitoring. The RX Axc output is scaled to provide 16-bit, IQ-packed WCDMA or 16-bit IQ LTE data.

The BB module has interrupt outputs for signaling events.

The BB module has signals to the CPP module to identify when the BB power meter is ready to be read.

There are different sets of multiple channel power meters so that specific Axc channels can be processed on a specific group.

2.2.2   Inputs and Output Buses

Table 2-1. BB Inputs and Outputs

Name	I/O	Basic description
AID TX input Bus	I	Axc TX carrier data from IQN2.
AID RX Output Bus	O	Axc RX carrier data to IQN2.
MPU Bus	Both	Parallel data/ address/ module address synchronous bus for programming registers / memories.
DDUC TX inbus	I	BB output data for TX to DDUC[3.0] 18-bit interleaved IQ.
DDUC RX outbus	O	BB input data from DDUC[3.0] for BBRx output, 24-bit interleaved IQ.
Sync Bus	Both	A group of signals that indicate the time-event to perform an operation, the BB block can insert the AID-DLSync, AID-ULSync signal as events.
Interrupt Bus	O	Signals to MISC module to indicate a BB event occurred.
Test Bus	Both	Signals to global capture buffer Test Bus data source for capture.
CPP Triggers	O	Event triggers for the CPP block to service the BB events that require CTL service.

2.2.3   Basic Description

2.2.3.1   BBTx

The TX AID interface takes the IQN parallel bus and converts this into the time division interleaved IQ bus for the DDUC. The AID interface has four 16-bit IQ, Axc#, and sync information. The TX configuration table has the specification for a specific Axc# to route the received data to the desired DDUC TX buffer. The BBTx gain is adjusted for each channel of the received IQ data. The BBTx AID interface has DL sync information that is extracted and sent to the sync bus within DFE.

The BBTx AID bus has a test loopback configuration. This test configuration is used with IQN2 for AID loopback, and is a static test configuration (that is, loaded with the register programmation). The AID bus loopback is used for single mode tests.

The BBTx programming has a dependency on the IQ sample rate, and each IQ sample rate is a specific type-group. Table 2-2 shows examples of wireless applications. The BBTx programming table contains the mapping from an Axc#, to the TX functions performed, to the DDUC# and channel buffer within the DDUC. This BBTx programming table is fixed at register programmation time. The BBTx controller converts the sample received in the packet through the selected functions, then sends the data to the proper DDUC buffer and channel.

Table 2-2. BB Signal Groups

Signal Type	TX IQ Rate (Mhz)	TX Inbits	RX IQ Rate (Mhz)	RX Outbits
LTE20	30.72	16	30.72	16
LTE10	15.36	16	15.36	16
LTE5	7.68	16	7.68	16
LTE3	3.84	16	3.84	16
LTE1.4	1.92	16	1.92	16
WCDMA	3.84	16	7.68*(3.84)	Dual(*) packed 8

BBTx_Gain is set as dbvalue_Inphase, quadrature value is –inf, for each Axc#. The BBTx gain is stored for each Axc# in an active and shadow register. The BB gain scales the 16-bit input to an 18-bit IQ output. The gain output is rounded and saturated. A sync signal transfers the new gain value for each Axc at a selected sync bus time. The BBTx gain update is controlled through an API.

> **NOTE:** The BBTx power meter monitors the postgain value, and the Axc# power meter values should be below fullscale. Normally the BBTx_Gain for each Axc# is < 0db.

The BBTx bus has a test generator that can insert an IQ constant, IQ ramp_delta, as a test signal. The BBTx bus to the DDUCs has a test bus single Axc connection for troubleshooting. Each of the BBTx DDUC buffers has a buffer loopback special test mode, DDUC0 TX -> DDUC3 RX, DDUC1 TX -> DDUC2 RX.

The DDUC buffer loopback is used for loopback to AID/IQN2 for dual-mode configurations. The DDUC buffer loopback is a static test configuration (that is, loaded with the register programmation).

The BBTx bus can be monitored by a test bus with software API for a select single Axc#.

2.2.3.2 BBRx

The BBRx section takes 24-bit IQ data from the DDUC RX buffers and provides gain scaling (fixed and beAGC adaptive beAGC), power meter measurement, and RX output formatting for use in AID-IQN2 interface.

The BBRx programming has a dependency on the IQ sample rate, and each IQ sample rate is a specific type-group. The BBRx programming table contains the mapping from a DDUC# and channel within the DDUC buffer, RX functions, the gain operations performed, the power meter usage, and the RX output formatting for the AID interface. This BBRx programming table is fixed at register programmation time. The BBRx controller converts the time offset, pulls the samples from the DDUC buffer and channel, performs the desired signal processing, and routes this to the AID RX bus.

The BBRx Axc IQ values are processed with the BBRx gain block for fixed gain, or fixed gain + adaptive gain. The fixed gain has an active and shadow set of channel values that are updated through an API. The beAGC block applies adaptive gain for WCDMA applications.

The BBRx gain is controlled through the beAGC mode. The available gain modes are controlled through software APIs. Most applications are initialed in fixed-gain mode.

- BBRx gain – Fixed mode – The MPU register is used for integer and fractional gain, gain range is -Inf to 90 db. (This mode is used for LTE channels for TCI663xK2L.)
- BBRx gain – BBRx Power Mtr assisted mode – The MPU registers load a peak channel power value and Axc backoff (PAR) value to develop an RMS target value. The BBRx power meter reading is subtracted from the setpoint, and is converted to an Axc channel gain value. (This mode is not used for TCI663xK2L.)
- Fixed gain + beAGC with adaptive error accumulation – The BBRx gain fixed mode is added to an Axc channel-specific adaptive gain. The adaptive gain is based on the Axc group AGC threshold, gain shift, and upper and lower adaptive gain limit. (This mode is used for WCDMA.)
- BBRx Power Mtr assisted mode + beAGC - In this mode, the fixed gain is based on the power meter setpoint and measured value. Between the power meter updates, the beAGC adaptive gain changes the adaptive gain. This mode requires special gating of the AGC. (This mode is not used for TCI663xK2L.)

2.2.3.3 beAGC (Adaptive BBRx Gain)

The WCDMA carrier IQ data has a wide dynamic range. The goal is to provide the optimal dynamic range of the signal, by adapting the BBRx gain to a target mean signal value. The magnitude of the IQ sample is compared with the threshold, and an error value is generated. The error signal is scaled by a control range multiplier (normal AGC, zero AGC, and saturate AGC) and this signal adds or subtracts from the error accumulator. Each carrier channel has an independent error accumulator to develop channel-independent adaptive gain. Each error accumulator is limit checked for a maximum and minimum gain, to minimize reset-windup affects of the integral controller. See Figure 2-5.

The error signal scaling develops the integral controller dynamics for attack and decay times, and is calibrated with specific basestation fading models. In most cases, a scaling is used that has slow acting, above, below, zero, and saturate scaling typically, less than .5% current sample and 99.5% previous samples.

NOTE: Changing the scaling values to faster-acting decay and attack values also has overshoot and undershoot affects, which change the AGC noise contribution to the RX output.
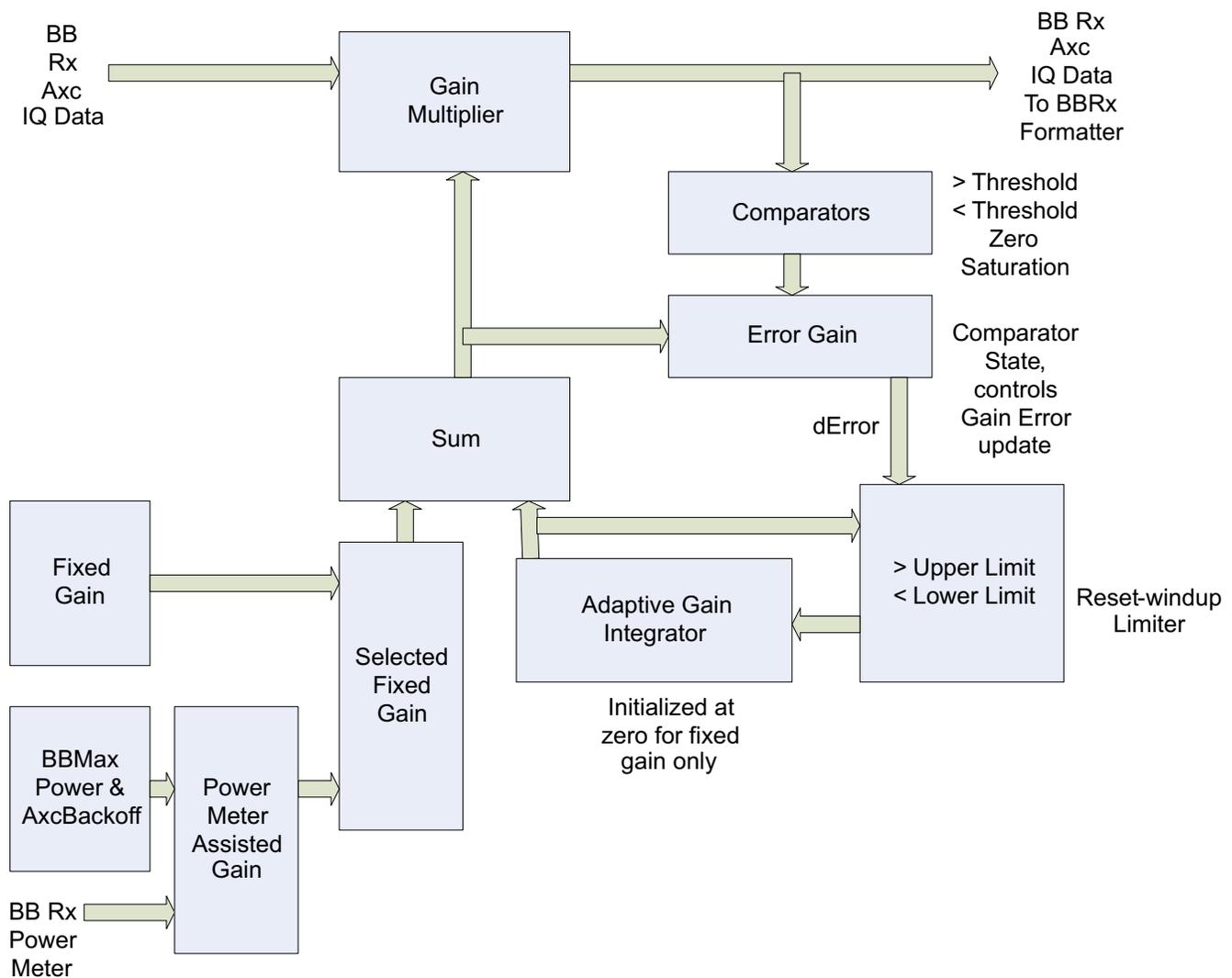
Figure 2-5. beAGC Block Diagram|

2.2.3.4 BBRx Formatter

The BB gain adjusted 48-bit IQ data is scaled to fit in the specific format of data for the AID interface. The format conversion does scaling, rounding, and saturation.

The AID interface supports 16-bit IQ, and dual sample 8-bit IQ data. The 16-bit IQ format is for general applications. The dual sample 8-bit IQ format is for WCDMA applications. Another component of the formatting is the number of IQ samples placed on the AID bus for transfer to IQNet. In most cases, 4 LTE 16-bitI, 16-bitQ samples, or 8 WCDMA 8-bitI, 8-bitQ samples are transferred. In general applications, pack four 16-bit I and Q 1xsample-rate into one RX AID output bus cycle. In WCDMA applications, pack eight 8-bit I and Q 2x sample-rate into one RX AID output bus cycle.

2.2.3.5 Power Meter

Each BBTx Axc# and BBRx Axc# can be assigned to a power meter group. There are eight BBTx and eight BBRx multi-channel power meter groups. The Axc# is assigned in the static configuration programming to a specific power meter group. There is one signal type per power meter group. The power meter can monitor before the gain block or after the gain block on a per group basis.

The power meters have several operational modes:

• Off – Idle state, power meter not used

• Single power measurement – Once triggered, updates registers from a single measurement

• Continuous power measurement – The sync event triggers the power meter, then the delay integrate-interval and period counters are used to integrate and store the power meter measurement.

See Figure 2-6. The power meter has a synchronized start signal, then utilizes the three counter timers. The sync delay is a count after the start signal, before starting to integrate the I^2+Q^2 signals. The intergration period is the number of baseband samples to integrate. The interval is the number of IQ samples from the sync delay that restart the continuous power meter measurement. A software API sets up the BB power meters, and another API reads the power meter values. There is a separate power meter value for each Axc# within a power meter group.
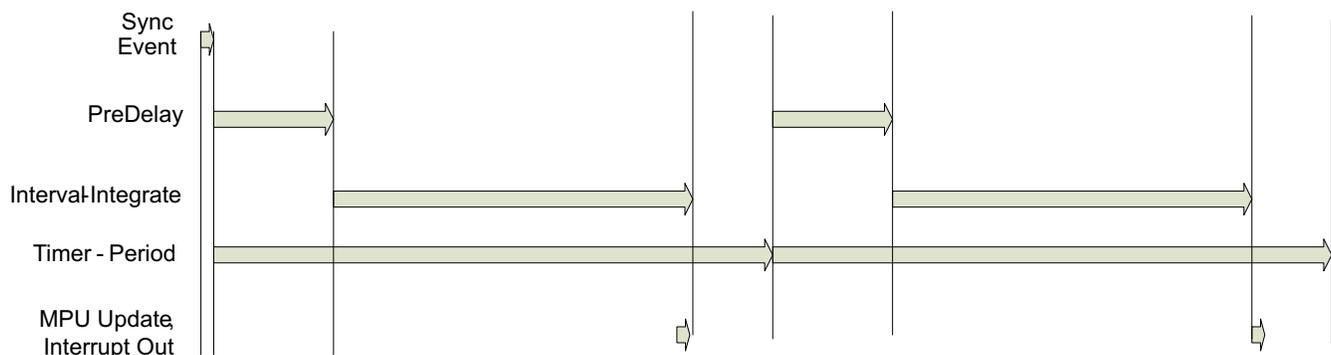
Figure 2-6. BB Power Meter Cycle

2.2.4 Synchronization Events

The DL sync signal from IQN2 is received with the TX AID data, and is sent to the DFE sync bus. The UL sync is a BB register-controlled delayed version of a DFE sync bus signal, and is sent back to IQN2 as the UL sync.

2.2.5 Software Application Interface (API) Functions

NOTE: API topics are covered in more than one section. See Reference 6 (Chapter 3) and for additional information.

API_BB_TxGain – Adjusts the BBTx antenna carrier signal level

API_BB_TxPower_Setup – Configures and initializes the BBTx antenna carrier power meter by group (signal type)

API_BB_TxPower_MeterRd – Reads the BBTx antenna carrier power, multiple antenna carriers in a group

API_BB_Tx_TestGen – (diagnostics) Substitutes a ramp, constant, or LFSR signal type for the antenna carrier input

API_BB_RxGain – Adjusts the BBRx antenna carrier signal level

API_BB_RxGain_beAGC_setup – Adjusts the adaptive gain parameters by group for WCDMA carriers

API_BB_RxPower_MeterSetup - Configures and initializes the BBRx antenna carrier power meter by group (signal type)

API_BB_RxPower_MeterRd - Reads the BBRx antenna carrier power, multiple antenna carriers in a group

API_BB_RxPower_MeterRdCPP – Configures special BBRx power meter readings for CTL data transport (must have compatible setup in CPP sub-block)

API_BB_TestBus – (diagnostics) Sends the BBTx or BBRx selected antenna carrier to the CB testbus

2.2.6 Important Programming Concepts (or Selection from Pre-Built Configurations)

The BBTx number of channels is fixed in the static configuration.

The carrier types are grouped by IQ rate, processing functions, RX gain mode. The group concepts also apply to other BB functions such as baseband power meter.

In most cases, the BB TX and RX power meters are set up for post-gain monitoring.

2.3   Digital Downconverter/Upconverter (DDUC) in DFE
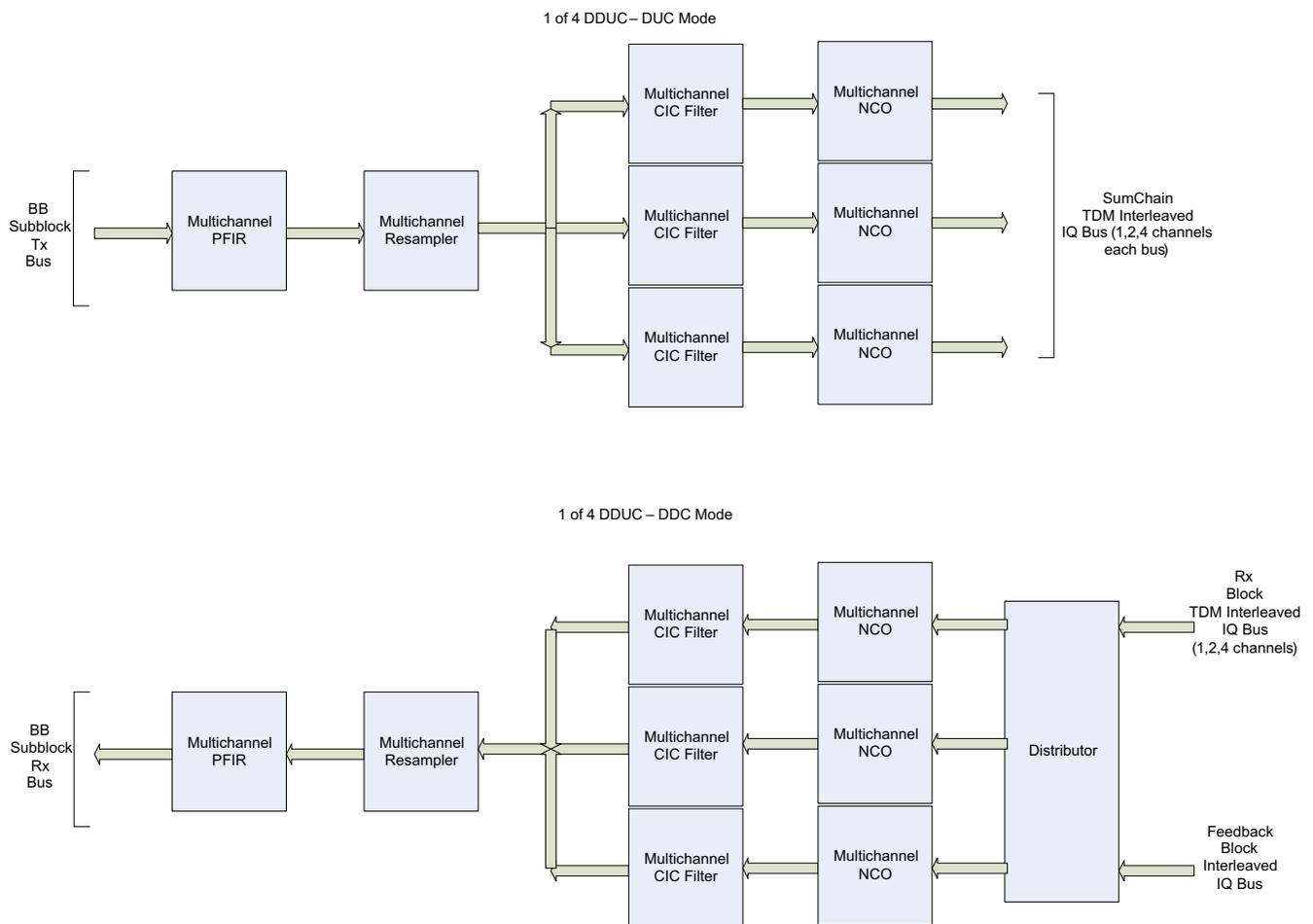
Figure 2-7. DDUC Block Diagram

2.3.1 Function

The digital downconverter/upconverter (DDUC) logic block within DFE provides the Axc channel interpolation and decimation, filtering, and individual channel tune to carrier frequency functions (See Figure 2-7). The digital upconverter shown in Figure 2-7 interpolates, filters, and frequency-translates the channel signals. The digital downconverter (lower diagram) takes the complex receive signal, provides frequency translation for each carrier (translates the stream to the 0 Hz for the desired carrier), then provides filtering and decimation. The IQ structure within the DDUC block is interleaved IQ format.

TCI663xK2L has four DDUCs. Typically, two DDUCs are used for TX, and two DDUCs are used for RX. The TX flow path is shown in Figure 2-1. The RX flow path is shown in Figure 2-2.

The baseband TX bus BB to DDUC has an 18-bit data path. The individual upconverted carriers in the digital upconverter that go to the summer have an 18-bit interleaved IQ data path. In Figure 2-8, each DDUC has three CIC/Mixer outputs. Each CIC/Mixer output can be 1, 2, or 4 time-interleaved carriers.

The RX stream or feedback-sniffing stream from the RX block or feedback block has an 18-bit interleaved IQ data path. The baseband RX bus from DDUC to BB has a 24-bit data path.
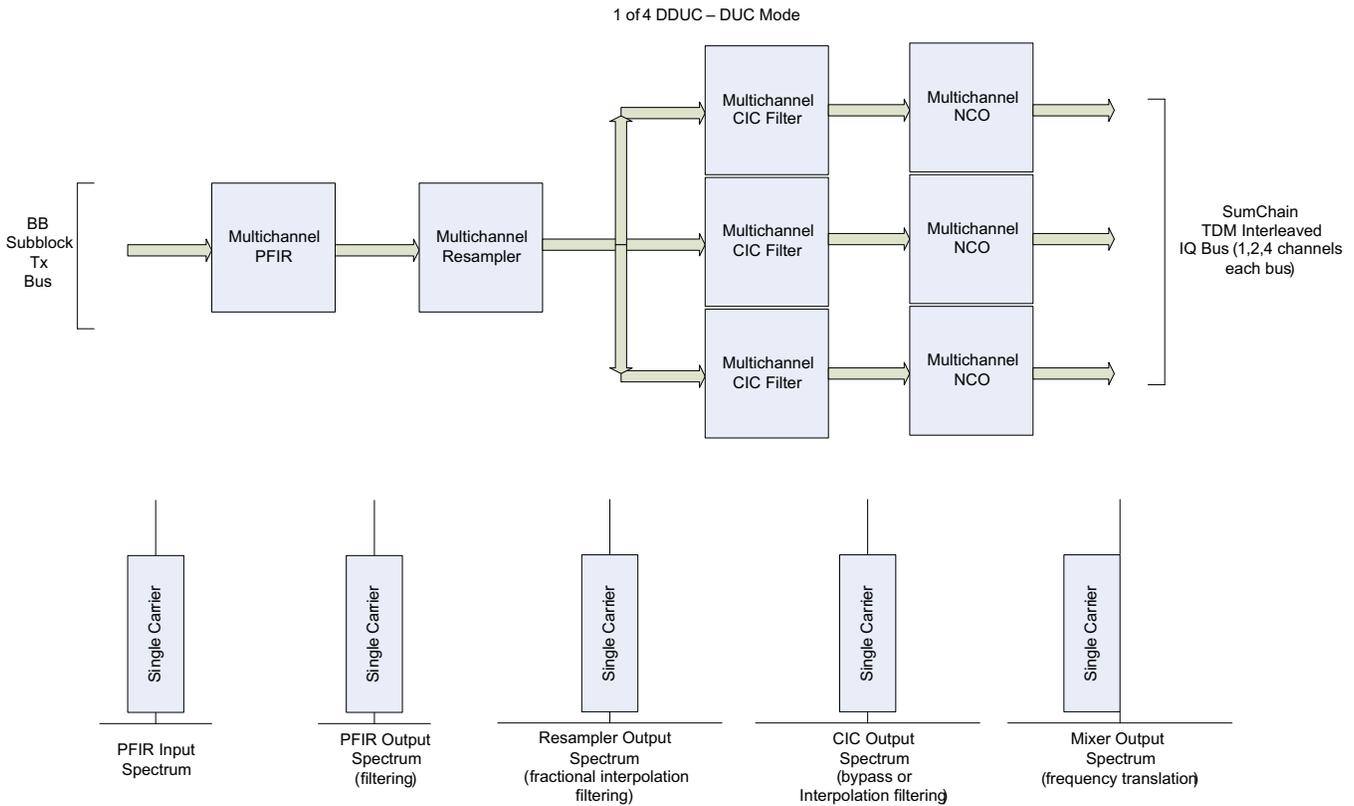
Figure 2-8. DDUC as a Digital Up Converter (1 Carrier Shown) Block Diagram

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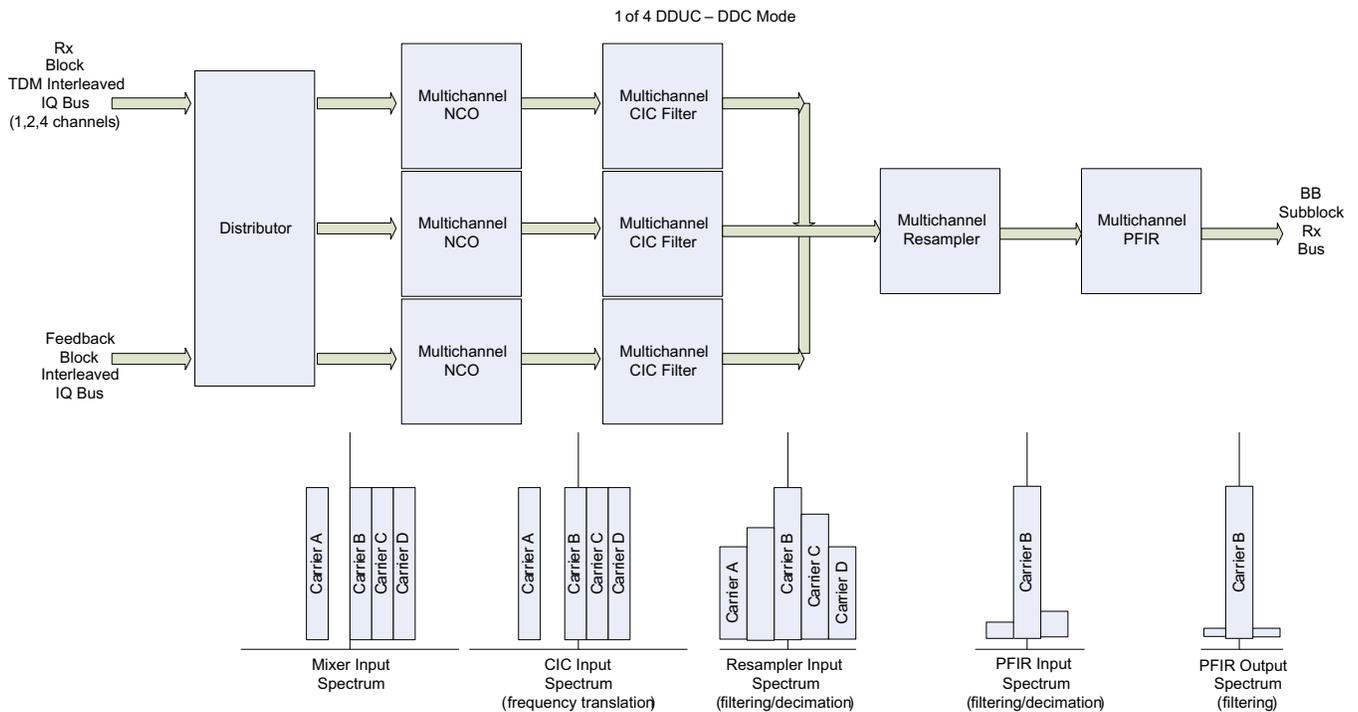
Figure 2-9. DDUC as a Digital Down Converter (Multicarrier Shown) Block Diagram

In the TX mode (see Figure 2-8) antenna carriers create the upsampled and tuned carrier streams. In the RX mode (see Figure 2-9) the RX or feedback sniffing streams are tuned to a specific carrier frequency, and filtered or decimated for the Axc output rate.

The DDUC programmable finite impulse response (PFIR) filter provides the spectral shaping of each channel. You can select different PFIR taps for specific DDUC channel numbers. The PFIR can have a ratio of one or two.

The DDUC resampler provides for a Farrow-implemented interpolation and decimation fractional-rate filter. The resampler has a fixed Farrow set of polynomial coefficients, and a fractional 'D' accumulator to compute the coefficients used for each 'D' value by the filter. The resampler ratio is programmed to the same value for all channels within a DDUC at initial register programming time.

The cascade integrator comb (CIC) filter provides for further interpolation or decimation, ratios 1, 2, or 3. The number of DDUC channels in a specific use determines the ratio:

- 1 or 2 channels, ratio 1
- 4 or 8 channels, ratio 2
- 3, 6, 12 channels, ratio 3

The complex mixer has several blocks, the general function has a phase calculation per DDUC channel, the phase value is converted to a cosine/sine mixer frequency, and the mixer frequency is multiplied by the channel or stream complex value.

Phase offset and phase dither can be added to the calculated channel phase value. The mixer frequency phase can be updated dynamically. This is controlled through an API.

2.3.2　Inputs and Output Buses

Table 2-3. DDUC Inputs and Outputs

Name	I/O	Basic Description
MPU Bus	Both	Parallel data/address/module address synchronous bus for programming registers/memories.
DDUC TX Inbus	I	DDUC input data for TX from BB block, 18-bit interleaved IQ.
(3) CIC/Mixer Output Buses	O	DDUC output data for TX from DDUC to Summer block, 18-bit time interleaved IQ, 1, 2, or 4 interleaved channels in time.
DDUC RX Outbus	O	DDUC output data for RX to BB block, 24-bit interleaved IQ.
RX block RX Out Bus	I	DDUC input stream (multiple channel) data from RX block, 18-bit time interleaved IQ, 1, 2, or 4 interleaved streams in time.
Feedback Out Bus	I	DDUC input stream (multiple channel) data from feedback block for Network Listening Mode, or Feedback sniffing, 18-bit time interleaved IQ, 1, interleaved streams in time, similar format to RxOutbus.
Sync Bus	I	A group of signals that indicate the time-event to perform an operation.
Interrupt Bus	O	Signals to MISC module to indicate a DDUC event occurred.
Test Bus	Both	Signals to global capture buffer Test Bus data source for capture.

2.3.3　Basic Description

2.3.3.1　PFIR

The PFIR provides the spectral shaping for each baseband channel, first processing for TX and then processing for RX. The PFIR can have an interpolation or decimation of one or two. The PFIR can store multiple sets of FIR coefficients in memory. The PFIR can utilize different coefficient sets for different DDUC channels, but usually has the same symmetry and same number of coefficients for all channels within a DDUC.

The number of coefficients within the PFIR is based on the DFE clock rate, PFIR input IQ rate, interpolation or decimation, ratio, number of active PFIR channels within this DDUC, and the number of stored filters. The number of PFIR coefficients also may be limited by the allowed DDUC latency. The selection of each DDUC channel, using a specific PFIR filter set, is selectable using an API. Applications typically have the single natural sampling rate PFIR filter. Some applications can have multiple PFIR filters, in which case the dynamic selection of PFIR filter set can be done at run time with an API.

In WCDMA applications, the user typically interpolates by 2, and has a root raised cosine (RRC) filter. In WCDMA the decimation ratio is usually 1, and has a root raised cosine filter, with a 2x output rate.

In LTE applications, the user typically interpolates and decimates by 1, and has a low pass filter.

> **NOTE:** The PFIR can be >50% of the channel latency for an application, so selecting a longer PFIR set of coefficients can provide more close-in spectral rejection or shaping, but has longer latency.

> **NOTE:** If the CIC ratio for this DDUC channel is >1, the PFIR design is modified to add a high pass filter for CIC droop correction. This flattens the passband of the DDUC channel response. CIC correction is typically a five tap high pass filter, if the CIC ratio > 1. This results in an RRC or low pass filter of number of coefficients – 4.

The PFIR has an internal scaling for all DDUC channels. The log2 (sum_of PFIR taps) is used for scaling. Some applications use a maximum center tap of 131071 and have loss through the DDUC channel, to get better close-in rejection. Most applications scale the PFIR coefficients so that the sum of coefficients is a power of 2. The scaling must be the same for all sets of PFIR coefficients in DDUC use.

The number of PFIR taps in the DDUC can be computed using the following equation:

((DFE_clock/(PFIR_input_rate × #channels)) × 20) - 1   (2)

Typical numbers of PFIR 18-bit signed coefficient taps used in wireless communications are shown in Table 2-4.

Table 2-4. DDUC PFIR Number of Taps Estimate

Channel Signal	Number Channels in DDUC	DFE Clock - Mhz	Number of Taps
LTE20	2	245.76	79
LTE20	2	368.64	119
LTE20	3	368.64	79
LTE10	4	245.76	79
LTE10	4	368.64	119
LTE10	6	368.64	79
LTE5/ WCDMA	8	245.76	79
LTE5/ WCDMA	8	368.64	119
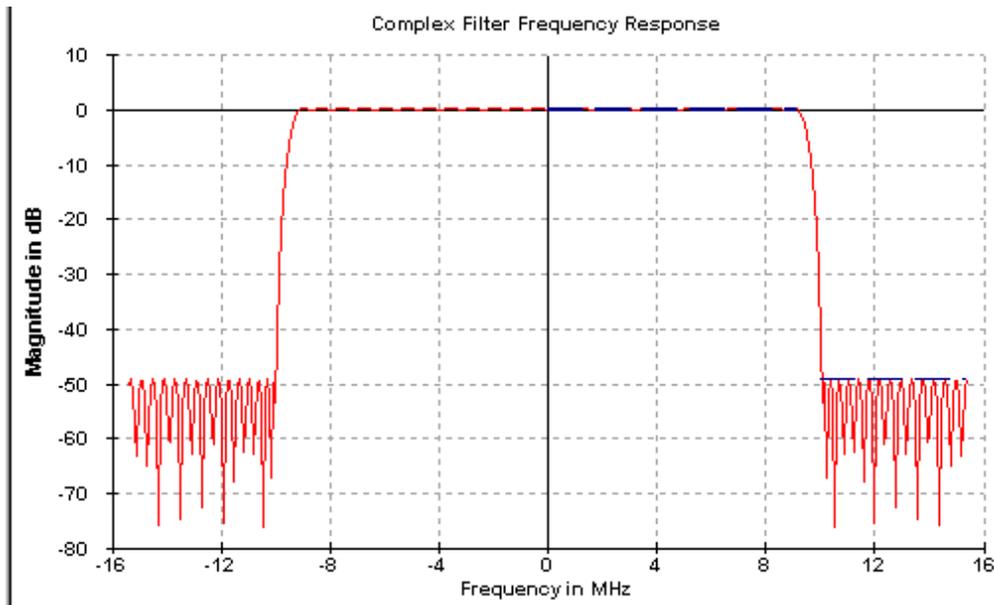
Figure 2-10. Example 79 Tap – Low Pass Filter Used for LTE20 Application
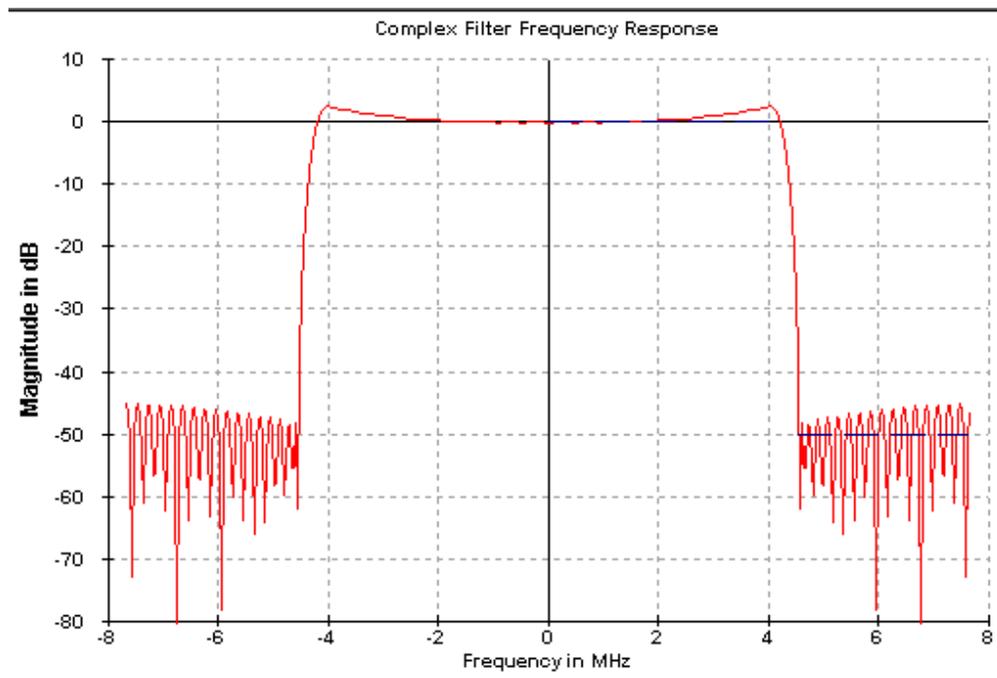
Figure 2-11. Example 79 Tap – Low Pass Filter Used for LTE10, with CIC Droop Compensation

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NOTE: The PFIR filter establishes the close-in rejection for the transmit channel. The PFIR transition band and stopband response, along with the IQ baseband signal response, determines the final transition and stopband response. In Figure 2-10, only the FIR filter tap response is shown. The PFIR affects the passband, transition (passband to stopband), and the stopband up to the resampler input rate. The resampler is mostly an equivalent low pass filter for normal applications. In wideband applications or if the CIC ratio is >1, some PFIR taps are reserved for a high pass filter, convolved with the low pass filter, to correct for droop in the passband. See Figure 2-11 as an example. Droop compensation changes the AC gain of the filter, so the PFIR shift may need to attenuate the PFIR output more.

2.3.3.2 Resampler

The resampler block interpolates (TX) or decimates (RX) by an M/N ratio. If the M/N ratio is 1, the resampler is set to bypass. All channels in the DDUC have the same M/N ratio. The resampler keeps track of the fractional interpolation or decimation count for each clock cycle. The resampler applies the appropriate filter coefficients to the PFIR out (TX) or CIC out (RX) for each channel in the DDUC.

The resampler ratio is based on the PFIR output rate and CIC input rate. The CIC input rate can be calculated from the TX sumchain rate/CIC ratio, or from the RX or Fdbk output rate/CIC_ratio.

- These ratios are in the pre-built configurations. Once the DFE registers are loaded, the ratios are fixed during operation.
- Each DDUC channel has a fractional count offset that can decorrelate peaks on the TX DDUC channels that are combined in a common stream. The value must be known from the initial reg. file programming to update the integer offset with the same value. Normally, TX and RX use of fractional 'D' programming is not used.
- The resampler has a gain adjustment for the RX direction, which is set with the initial register loading. The gain adjustment applies to all channels within the RX DDUC.

2.3.3.3   Cascade Integrator Comb (CIC)

The CIC filter has a ratio of 1, 2, or 3. There are three CIC filters within the DDUC: each one can process 1, 2, or 4 channels. The CIC has seven stages and a differential delay of 1. The CIC filter has a scaling, integrator, and differentiator. In the DDC applications, there is an adjustable gain value, but it is set when the registers are initially loaded.

Table 2-5. DDUC Number of Channels, Relationship to DFE Clock, and CIC Rate

Numch per DDUC	Num CICs Used	CIC Ratio	DFE Clk Ratio	CIC Input Rate (DFE Clk Ratio/CICRatio)
2	1	1	DFEclk/4	DFEclk/4
3	3	3	DFEclk/4	DFEclk/12
4	2	2	DFEclk/4	DFEclk/8
6	3	3	DFEclk/4	DFEclk/12
8	2	2	DFEclk/8	DFEclk/16
12	3	3	DFEclk/8	DFEclk/24

2.3.3.4   Complex Numerically Controlled Oscillator (NCO)

The complex NCO provides the per channel (TX) and signal (RX) frequency translation (see Figure 2-12). The NCO is based on multiplying the signal or channel by an I and Q value. The I and Q value are the current time value of the calculated complex frequency. The I (cosine), Q (sine) values are based on the phase of the complex frequency for each channel. Each channel in the DDUC has a delta-phase value, and an offset phase value. Each channel in the DDUC has a phase integrator, whose value is updated for each channel-time in the DDUC.

DeltaPhase = (2^{47}) * TuningFreq / DDUC IQ SampleRate

Iout = Iin * cos(phaseNCO) – (Qin * sin(phaseNCO))

Qout = Qin * cos(phaseNCO) + (Iin * sin(phaseNCO))

> **NOTE:** The tuning frequencies initially are programmed into the register values. Another API calculates the delta phase, based on the tuning frequency and channel number of DDUC IQ sample rate.

The delta phase and phase offset for each channel can be dynamically updated while the DFE is operating. All channels in a DDUC are updated at a specific synchronization event. This is also API-controlled. The complex NCO output is shifted, rounded, and saturated to an 18-bit output.

> **NOTE:** The phase offset range is 0 to 2^{16} counts, for 0 to 2*pi. This can be used to decorrelate carrier peaks when more than one DDUC channel is summed together for a TX stream.

> **NOTE:** In the DDUC, the multichannel delta phase (tuning frequency) is in a section called the frequency hopper (hopping is not used for TCI663xK2L DFE), and the NCO phase offset registers are MMR-located near the mixer. There is only one frequency hopper for all DDUC NCO channels. There are three multichannel mixer sections for all DDUC NCO channels. (See Figure 2-8, Figure 2-9.)
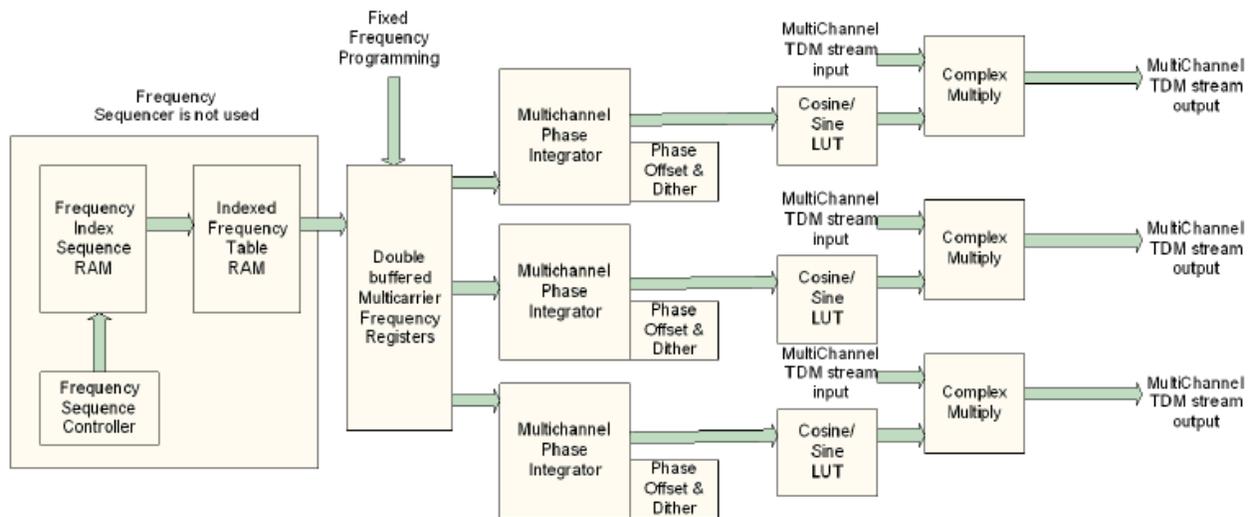
Figure 2-12. Multichannel Complex Mixer (3 Sections Shown)

2.3.3.5   Distributor

The distributor is used in the DDUC for the DDC receive processing. It receives the RX block time interleaved IQ stream data and the feedback block-sniffing RX time interleaved IQ stream data. The distributor reformats this data into the three sets of Mixer/CIC buses of interleaved IQ data. (See Figure 2-9.)

There is no TDM interleave reformatting in the distributor, so the RX output TDM format must match the CIC/Mixer-programmed format.

> **NOTE:** The distributor RX or feedback stream selected by CIC/Mixer number, and the signal within the CIC/Mixer number, can be changed with an API.

2.3.4   Synchronization Events

The sync bus DL sync or MPU sync are selected as the sync select sources for the DDUC block. A sync bus UL sync (delayed DL sync in BB block) is also available.

2.3.5   Software Application Interface (API) Functions

> **NOTE:** API topics are covered in more than one section. See Reference 6 (Chapter 3) and for additional information.

API_DDUC_PFIRFiltSel – If multiple PFIR filters are stored in PFIR memory, the index selects a specific filter.

API_DDUC_NCOUpdate – Provides the frequency translation offset frequency for each channel in this DDUC.

API_DDUC_Distributor – RX channel/ Fdbk NLM channel; provides the stream selection for RX processing.

2.3.6 Important Programming Concepts (or Selection from Prebuilt Configurations)

The number of DDUC channels and DDUC use as DUC/DDC are fixed at register programming time. In the TX usage, the sumchain block can disable extra TX channels.

The PFIR ratio (DUC) interpolation, (DDC) decimation, resampler ratio, and CIC ratio are fixed for all channels in a DDUC at the register programming time.

WCDMA uses a root raised cosine (RRC) PFIR filter; LTE channels use a low pass PFIR filter.

In cases where multiple PFIR filter sets are programmed, the index for the DDUC channels must be consistent with the filter programmed. The dynamic filter select API can change the PFIR filter taps of a specific channel, but does not change the interpolation or decimation ratio.

The PFIR coefficients are programmed at the register programming time. The coefficients must be compiled in the application, as they are in a specific order.

2.4 Sum Chain
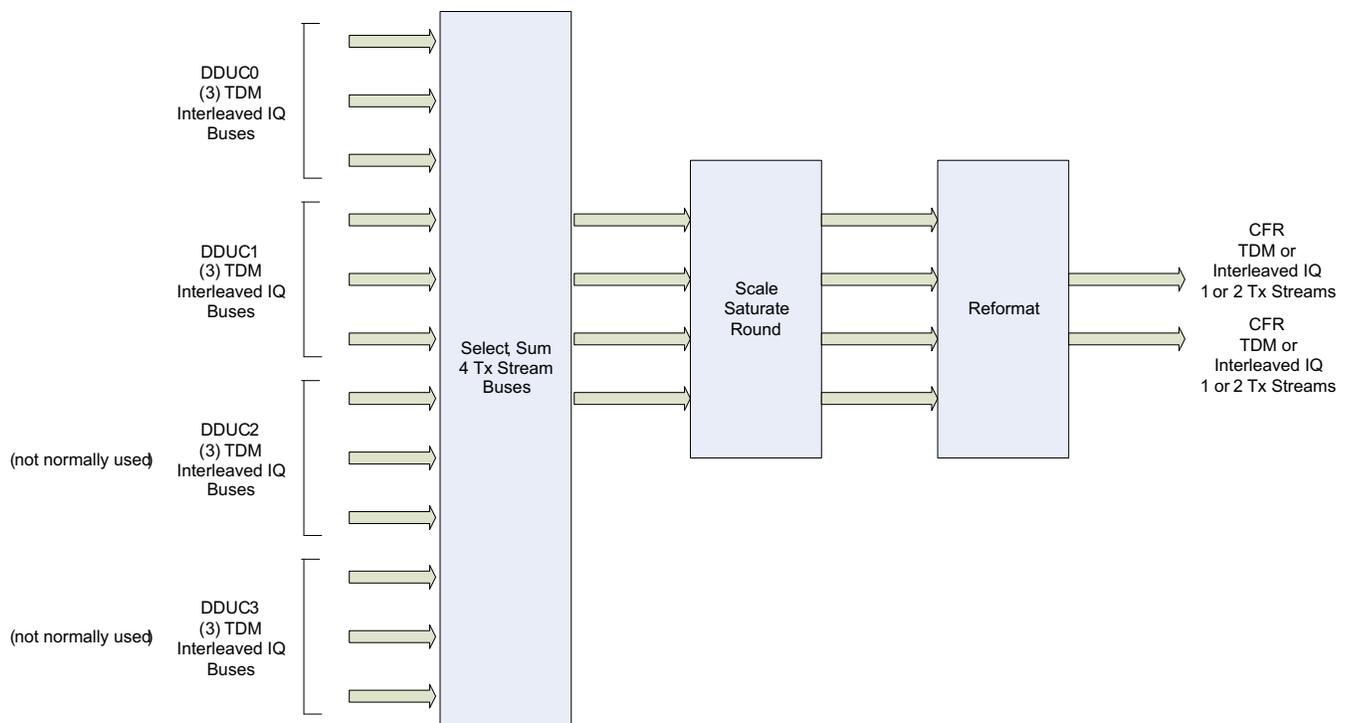
Figure 2-13. Sum Chain

2.4.1 Function

The sumchain provides a method to select which carriers are assigned to the four CFR buses. The sumchain provides gain scaling, rounding, and saturation for the CFR buses. The sumchain reformats the output buses, to the CFR block-interleaved IQ structure (two formats).

2.4.2 Inputs/Outputs

Table 2-6. SumChain Inputs and Outputs

Name	I/O	Basic Description
MPU Bus	Both	Parallel data/ address/ module address synchronous bus for programming registers / memories
DDUC0_CIC_MixBus0 in	I	DDUC0 CIC Mix Bus with time interleaved I; 1,2, or 4 channels in time
DDUC0_CIC_MixBus1 in	I	DDUC0 CIC Mix Bus with time interleaved I; 1,2, or 4 channels in time
DDUC0_CIC_MixBus2 in	I	DDUC0 CIC Mix Bus with time interleaved I; 1,2, or 4 channels in time
DDUC1_CIC_MixBus0 in	I	DDUC1 CIC Mix Bus with time interleaved I; 1,2, or 4 channels in time
DDUC1_CIC_MixBus1 in	I	DDUC1 CIC Mix Bus with time interleaved I; 1,2, or 4 channels in time
DDUC1_CIC_MixBus2 in	I	DDUC1 CIC Mix Bus with time interleaved I; 1,2, or 4 channels in time
DDUC2_CIC_MixBus0 in	I	DDUC2 CIC Mix Bus with time interleaved I; 1,2, or 4 channels in time
DDUC2_CIC_MixBus1 in	I	DDUC2 CIC Mix Bus with time interleaved I; 1,2, or 4 channels in time
DDUC2_CIC_MixBus2 in	I	DDUC2 CIC Mix Bus with time interleaved I; 1,2, or 4 channels in time
DDUC3_CIC_MixBus0 in	I	DDUC3 CIC Mix Bus with time interleaved I; 1,2, or 4 channels in time
DDUC3_CIC_MixBus1 in	I	DDUC3 CIC Mix Bus with time interleaved I; 1,2, or 4 channels in time
DDUC3_CIC_MixBus2 in	I	DDUC3 CIC Mix Bus with time interleaved I; 1,2, or 4 channels in time
CFR OutBus0	O	Time interleaved output bus for 1 or 2 IQ interleaved streams
CFR OutBus1	O	Time interleaved output bus for 1 or 2 IQ interleaved streams
Sync Bus	I	A group of signals that indicate the time-event to perform an operation.
Test Bus	Both	Signals to global capture buffer Test Bus data source for capture

2.4.3 Basic Description

The time-interleaved carriers from the DDUCs are combined onto the CFR-interleaved IQ buses based on register programming. The Axc mapping from the baseband input are summed onto a specific output bus through a specific DDUC channel CIC/Mix and time offset. There are up to four output buses. In most cases, DDUC0 and DDUC1 are used for TX, and the DDUC2 and DDUC3 sum chain selections are 0.

When carriers are summed there is a change in scale (for example, if four carriers are added, it is similar to scaling the data by a factor; the scale factor is not linear, and depends on the complex IQ peak combining of multiple carriers tuned to different frequencies). The sumchain has more bits of resolution to allow for many carriers to be summed from an 18-bit input. The sum is rounded, shifted, and saturated to the 18-bit interleaved IQ output format.

The CIC/Mixer bus has a different number of clock cycles, depending on the number of interleaved IQ carriers that are output:

Table 2-7. Example Number of Carriers per CIC/Mixer and Number DFE Clock Cycles

Number of Carriers on CIC/Mixer Bus	Number of DFE Clock Cycles to Output the CIC/Mixer Carriers
1	2
2	4
4	8

The sumchain can interleave one or two buses for each CFR block; two clock cycles for one bus, four clock cycles for two buses interleaved.

The sumchain combination and sum shift controls have APIs to allow for synchronized and dynamic changes of the number of carriers summed onto a CFR output bus, and the sum scaling (shift).

2.4.4 Synchronization Events

The synchronization events for the sum chain APIs are normally the DLSynchronization signal from the BB block or the MPU sync (updated immediately).

2.4.5 Software Application Interfaces

NOTE: API topics are covered in more than one section. See Reference 6 (Chapter 3) and for additional information.

API_Summer_Stream_CarrierSelect – User selects which TX DDUC channels are combined into a TX antenna stream.

API_Summer_SumShiftGain – User adjusts the TX antenna stream gain in 6db increments.

2.4.6 Important Programming Concepts

The sumchain has no rate conversion capability, so the CIC/Mixer output rate must match the CFR sub-block input rate.

The number of carriers within a TX stream has a scaling factor at the BBTx input, for < 6db steps. The sum shift value is a 6db step. The typical starting value is 0 for two carriers, –6db for four carriers, –12 db for six-eight carriers, and –18db to –24db for more than eight carriers.

The sum shift in some cases is adjusted to higher attenuation for determining the signal PAR, to remove CFR clipping from the CFR output, and to not trigger the circular limiter. This is a temporary setting.

2.5 Crest Factor Reduction (CFR)

1 OF 2 CFR MODULES
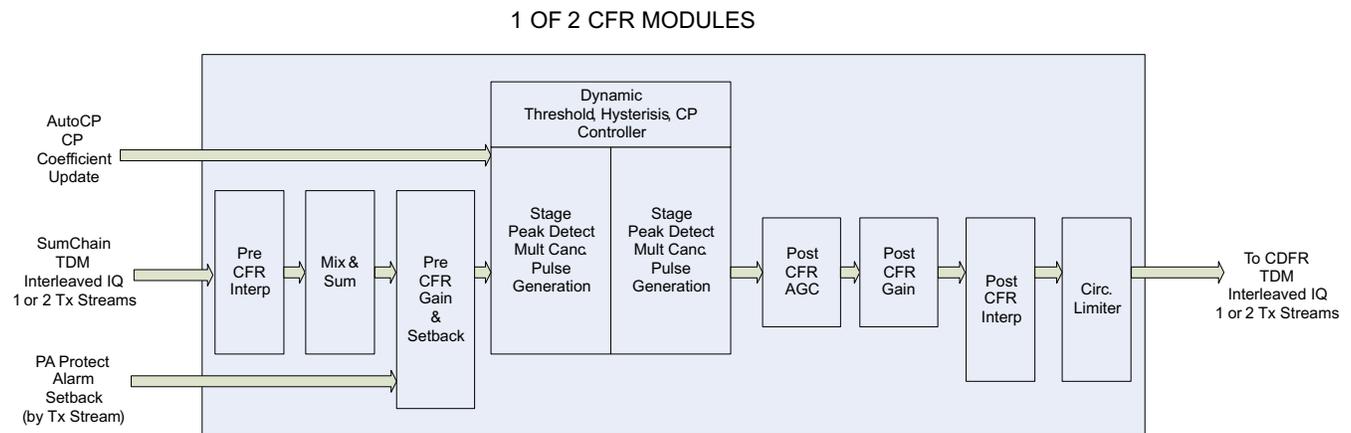
Figure 2-14. CFR Sub-Block Diagram

2.5.1 Function

The CFR block has two or four stages that estimate the peak of a signal and determine the time and amplitude of applying the cancellation pulse to reduce the peak of the signal. The two or four stages are distributed within two physical CFR logic sections that support 1, 2, or 4 antennas.

Each stage can support cancelling multiple peaks at the same time. There is special logic to arbitrate multiple peaks detected within the cancellation pulse time span, and cancel the highest magnitude peak.

CFR is important to operating TX chain and power amplifiers efficiently, as they reduce the power supply and cooling requirements by reducing the peak signal level. Because CFR adds cancellation pulse noise to the signal, there is an increase in the error vector magnitude for reducing the peaks. CFR can also improve the digital predistortion processing by restricting the operating range of the power amplifier.

Figure 2-15 shows the complimentary cumulative distribution function (CCDF), which shows the signal peak statistics. Also shown is a vector demodulation graph for the WCDMA waveform. The upper graphs show the unCFRed signal, higher peak, and lower EVM. The lower graphs show the CFRed signal, lower peak, and higher EVM. The cancellation pulse filter and settings for CFR balance the amount of clipping, the inband error, and affect on the transmit signal ACP and SEM.

Note the peak reduction and the increase in the signal demodulation error. The amount of CFR applied is measured for the signal type, and the gains are applied before CFR to cause a specific amount of clipping, to and measure the TX stream power peak and RMS levels.

CFR is normally adjusted for the largest signal (such as number of users), and at times where the number of users is less, there is less peak reduction.
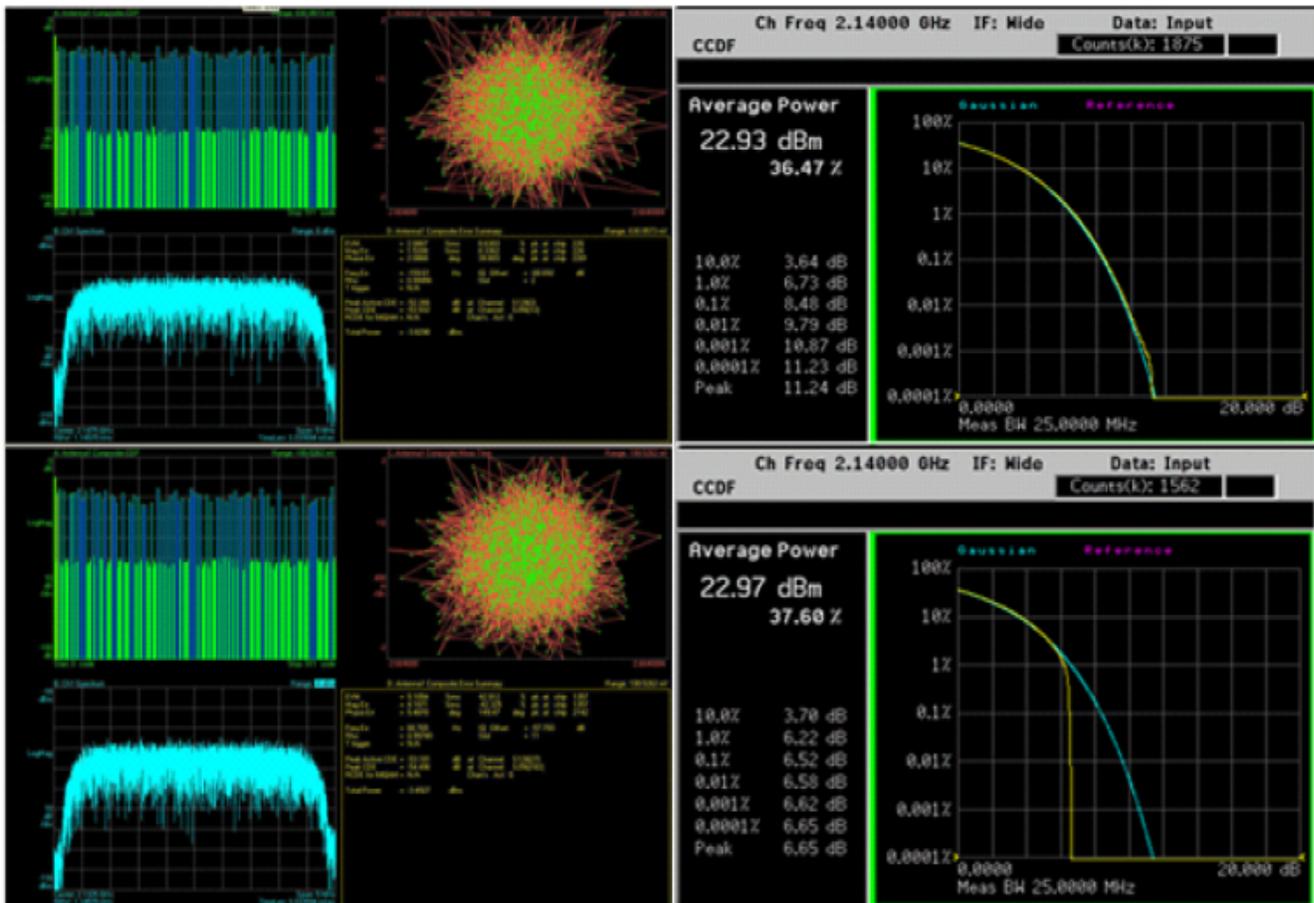
Figure 2-15. Effect of CFR on TX Antenna Carrier Signal (Upper-Before CFR/ Below after CFR)

PreCFR, CFR, and postCFR have specific relationships to the TX antenna stream IQ rate. They are set in the programmation of CFR before it runs. The most common CFR operating modes in Table 2-8 have a (*).

Table 2-8. CFR Operating Modes, Interpolation, and DFE Clock Rates

DDUC IQrates	Number of Antennas	PreCFR Interp	CFR	Number Streams per CFR Block	Post CFRInter	CDFR Input IQ Rate
DFE clock/4	2	1	4 stages of CFR for each stream	1	1	DFE clock/4
DFE clock/4	2	1	4 stages of CFR for each stream	1	2-Int2m	DFE clock/2(*)
DFE clock/8	2	2-Int2m	4 stages of CFR for each stream	1	1	DFE clock/4
DFE clock/8	2	2-Int2m	4 stages of CFR for each stream	1	2-Int2f	DFE clock/2(*)
DFE clock/8	4	1	4 stages of CFR for each stream	2	1	DFE clock/8
DFE clock/8	4	1	4 stages of CFR for each stream	2	2-Int2m	DFE clock/4(*)

The preCFR interpolation is used to interpolate and filter the DDUC output to a higher IQ rate. The interpolation 2 function can be bypassed. The preCFR interpolation filter uses the 107tap fixed coefficient half band filter. The preCFR interpolation filter supports 80% BW and 90-db stopband rejection.

The preCFR gain and setback (reduced gain with PA protection) logic apply a stream-specific gain to the antenna stream IQ data before CFR is applied. The gain value can be set by the user to adjust the amount of CFR clipping. If the TX block detects an over-magnitude condition, a logic signal can select a reduced gain value.

The postCFR gain changes antenna stream gain after CFR clipping. This gain adjustment is important to the target TX peak output level.

The postCFR interpolation interpolates and filters the postCFR antenna stream signals. The postCFR interpolation filter can use a 107tap fixed-coefficient half-band filter if the filter is not used in the preCFR interpolation. In cases where preCFR interpolate by 2 is performed, the postCFR interpolation by 2 is performed by a 19tap 45% BW filter.

The circular limiter provides a IQ sample-based magnitude limiter. The circular limiter limits the IQ sample magnitude for follow on DPD processing (gain expansion) to minimize peak clipping after DPD.
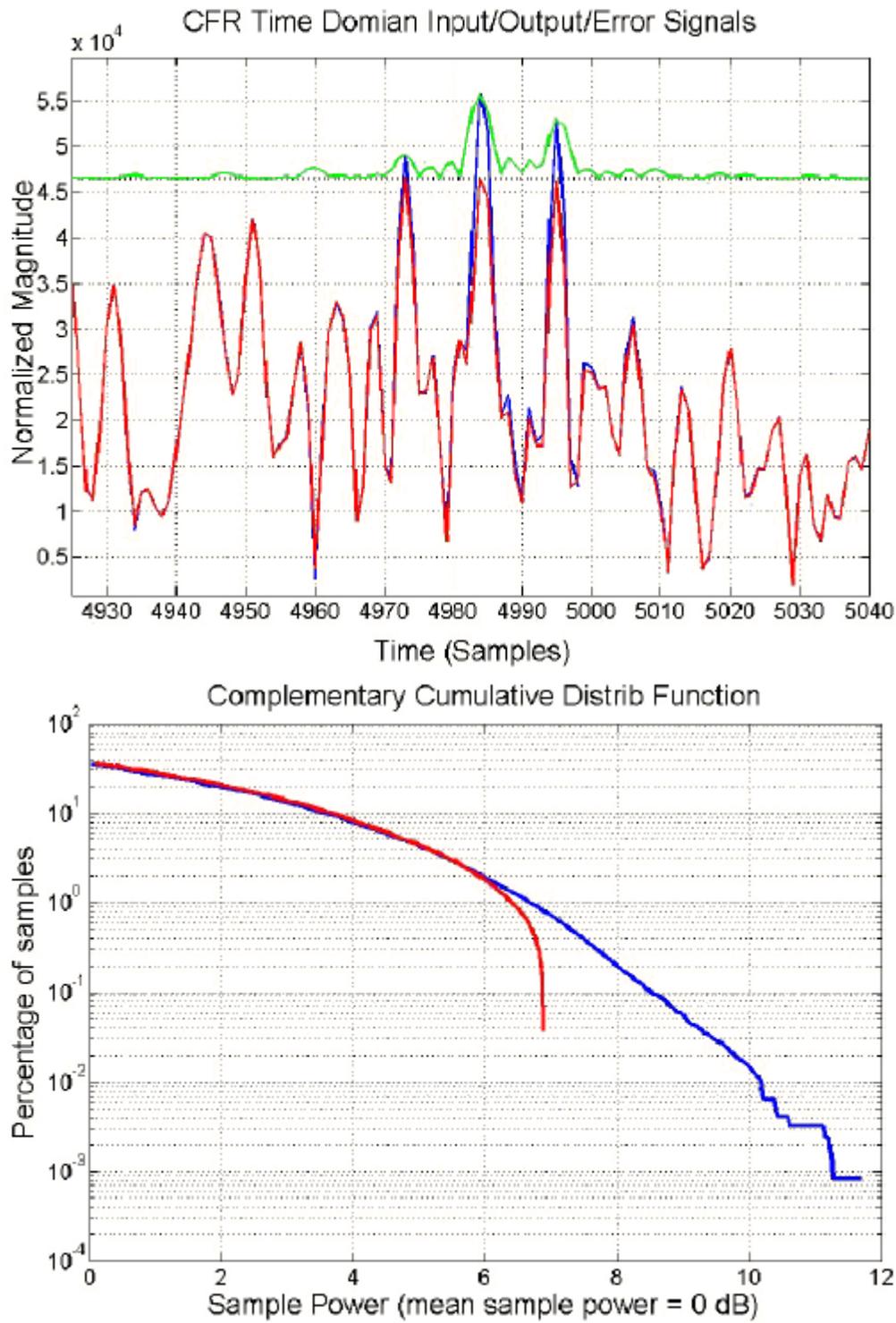
Figure 2-16. CFR Sub-Block Diagram

Figure 2-16 shows CFR processing for a typical dual-carrier 3G test model signal. The complementary cumulative distribution function (CCDF) plot shows the signal sample distribution before and after CFR. The signal peak-to-average power ratio is reduced from over 12dB to under 8dB. CFR can reduce the PAR based on the allowed increase in signal error vector magnitude. CFR peak cancellation is based on having a complex cancellation pulse that has the same spectral shape as the input signal. The logic estimates how much cancellation is applied to reduce the peak at input (blue) in left graph, to the peak at output (red) in left graph.

The cancellation pulse scaled to the appropriate gain and phase is applied to the signal to reduce the peak amplitude to below a set threshold. There are four successive peak estimation and cancellation operations within the CFR stream. Some gain tuning, peak setpoint, target value, hysteresis tuning, and CFR cancellation pulse filter tuning is also used to optimize CFR performance. The gain tuning and CFR cancellation pulse filter tuning can be optimized while CFR is operating. The other items must be set when loading the DFE registers.

2.5.2 Inputs/Outputs

Table 2-9. CFR Inputs and Outputs

Name	I/O	Basic Description
MPU Bus	Both	Parallel data/ address/ module address synchronous bus for programming registers / memories.
CFR signal bus 0 in	I	Time interleaved IQ bus from Summer block, contains 1 or 2 antenna stream data.
CFR signal bus 1 in	I	Time interleaved IQ bus from Summer block, contains 1 or 2 antenna stream data.
TxOverPower signals	I	Each Tx antenna stream has a setback signal, this is used to select the Setback gain for PreCFR , from Tx sub-block.
CFR signal bus 0 out	O	Time interleaved IQ bus from postCFR output to CDFR, contains 1 or 2 antenna stream data.
CFR signal bus 1 out	O	Time interleaved IQ bus from postCFR output to CDFR, contains 1 or 2 antenna stream data.
CaptureBufferCFR0 InBus	I	IQ bus to stream the preCFR IQ for specific antenna streams from CFR0.
CaptureBufferCFR0 OutBus	O	IQ bus to stream the postCFR IQ for specific antenna streams from CFR0.
CaptureBufferCFR1 InBus	I	IQ bus to stream the preCFR IQ for specific antenna streams from CFR1.
CaptureBufferCFR1 OutBus	O	IQ bus to stream the postCFR IQ for specific antenna streams from CFR1.
Sync Bus	I	A group of signals that indicate the time-event to perform an operation.
Interrupt Bus	O	Signals to MISC module to indicate a CFR event occurred.
Test Bus	Both	Signals to global capture buffer Test Bus data source for capture.

2.5.3 CFR Basic Description

The CFR block functions are divided into three sections:
- PreCFR processing
- CFR processing
- PostCFR processing

The DFE programming has general CFR parameters specific to static configuration. The CFR mode connects the CFR block functions with specific signal processing modes. In these modes, the CFR blocks are used as a single stream/block or two streams/block.

2.5.3.1 PreCFR Processing

PreCFR Interpolation is based onTable 2-9. The DDUC interface is clock/8 interpolated to the clock/4 mode for two antenna mode usage.

PreCFR gain is the primary CFR clipping control, in that the user changes the PreCFR gain to drive the antenna stream signal to the desired amount of CFR clipping. The preCFR gain goes from –Inf to 6db.

For example, the peak signal level for an antenna stream is –4dbc (preCFG gain 0db). The clipping peak thresholds are -3.5, -4.5, -5.5, and -6.5dbc. The PreCFR gain of 0dbm would result in the first clipping stage not detecting peaks. The clipping peak thresholds are not normally adjusted in DFE, the preCFR gain is adjusted.

2.5.3.2 CFR Processing

CFR processing is done as two or four cancellation stages for each TX antenna stream. Based on Table 2-9, the CFR blocks process the antenna stream signals from the sumchain. In certain modes, each of the two CFR sub-blocks processes two antenna streams (DFEPLL clk/8). If the CFR sub-block processes one antenna stream, the IQ rate is higher (DFEPLLclk/4).

Each CFR stream has magnitude cancellation thresholds and targets. There can be different values for each of the four peak cancellation stages. These are programmed in the fixed register configuration. When the TX antenna stream signal is greater than the threshold, and the multiple peak detection block indicates this is the highest peak, a cancellation event occurs. The peak value and the stored cancellation target determine the cancellation pulse gain. The stored cancellation coefficients scaled to the desired gain are subtracted from the peak signal.

Each peak cancellation stage can cancel multiple peak events (depending on the CFR mode). Figure 2-17 shows a peak cancellation stage. Figure 2-18 shows a single cancellation event, based on peak detection, multiple peak logic, scaling the cancellation pulse CPGE, and delaying the CPGE to the aligned peak to cancel.
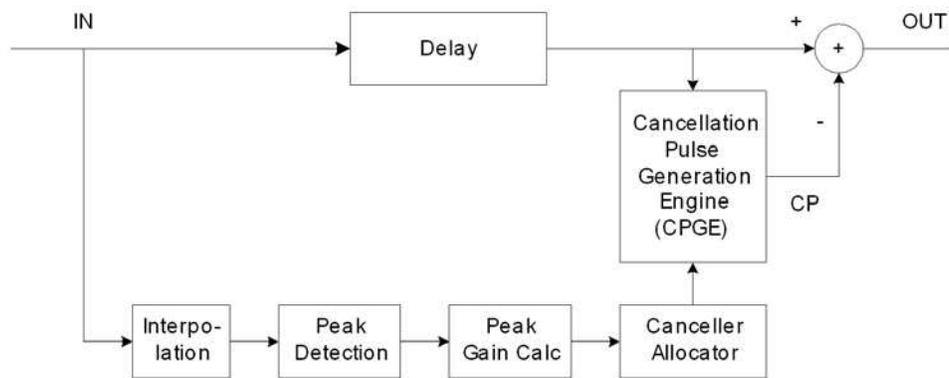
Figure 2-17. Cancellation Logic Diagram for CFR

Referring to Figure 2-14, there are two cancellation stages with reused logic, effectively making four cancellation stages for each TX antenna stream. This is the most common configuration, but there are other modes. Since there are multiple (two or four) cancellation stages, the user can reduce the peaks from stage 1 to stage 4, by reducing the peak in each stage. Figure 2-17 shows one stage with a representative cancellation pulse generator engine (CPGE). The CPGE has a complex cancellation pulse to subtract the center peak-aligned signal. Figure 2-15 shows a system perspective of CFR clipping, and Figure 2-18 illustrates a cancellation event. The complex cancellation filter has a zero delay and ½ delay version, which is selected by the peak detection logic.

As an example in the below peak detection setpoints, for the first of four peak cancellation stages, if the peak detected is greater than -4dbc, then a peak is checked for hysteresis (Figure 2-19), and the difference between the peak detected and the target value is used to scale the complex cancellation coefficients to subtract from the signal see Figure 2-18.

Example Peak detection threshold by stage -4, -5, -6, -6

Example Peak target by stage -6, -6, -6, -6

NOTE: The peak detection thresholds are adjusted with the PreCFR gain to achieve a specific amount of peak clipping, which can be tolerated by the LTE or WCDMA TX carrier within the TX antenna signal. This example has 2db of peak clipping.

CFR Peak Thresh   CFR Peak Thresh

CFR Gain Target   CFR Gain Target

Antenna Stream   Antenna Stream
Magnitude Signal   Magnitude Signal

ADD(AntennaStream , Canc Pulse)

Spectrum of
Cancellation Pulse is
within Tx Stream
spectrum

Spectrum of
Clipped Signal

Complex FIR Filter base   Scaled Complex FIR
Cancellation Pulse   Cancellation Pulse
                               (Peak Det – Gain Target)
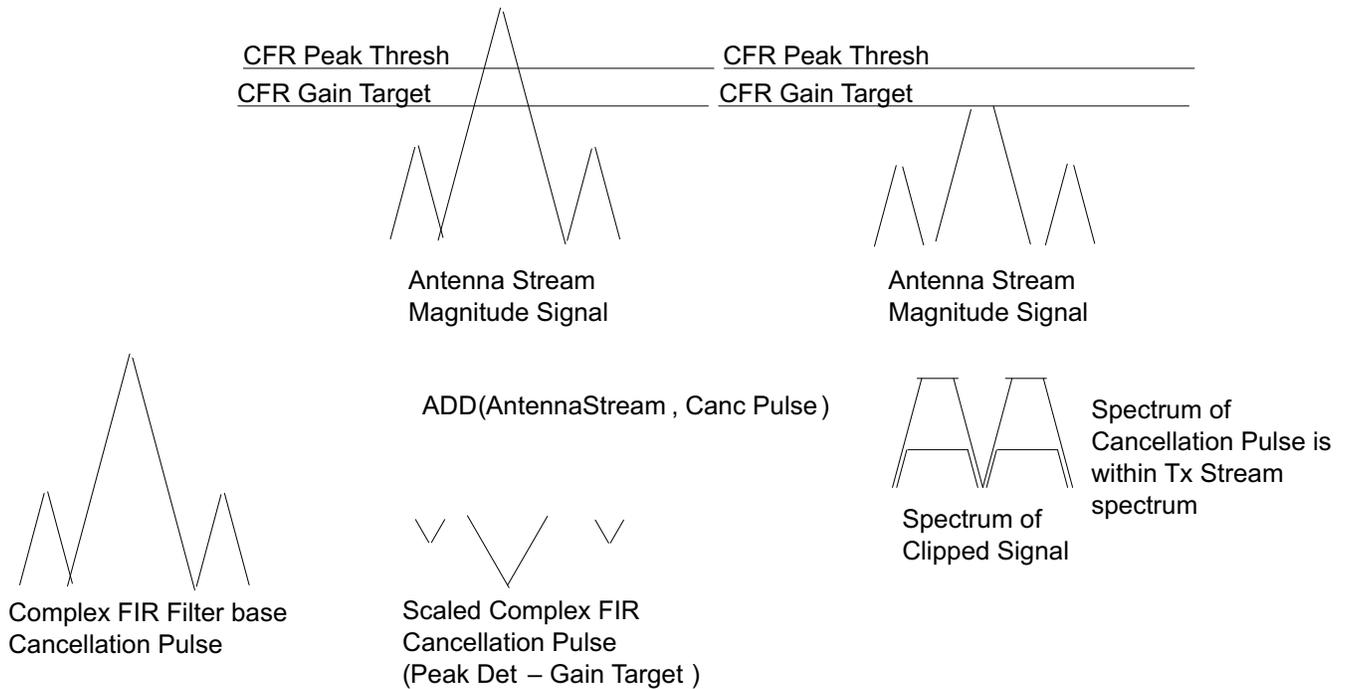
Figure 2-18. Example TimeSeries, Spectrum of Peak Clipping

The complex FIR filter base cancellation pulse can be single carrier or multiple carrier type.

> **NOTE:** In certain multicarrier examples (adjacent carriers), a signal cancellation pulse can be designed to cover the multiple antenna carriers. This has added benefits of CFR distortion between the antenna carriers. The carrier magnitude, frequency, and carrier BW are designed into the cancellation pulse. The base filter is provided for the LTE and WCDMA carriers. This is designed with an API, and sample CFR prototype cancellation base filters.

Another component of the CFR clipping and detecting peaks is the hysteresis control. The hysteresis control limits over-cancellation of peaks that are closely spaced in the time series. This is adjusted in the fixed configurations. The hysteresis control is adjusted to a higher number to limit the number of CPGEs triggered in a stage when the magnitude is above the detection threshold. See Figure 2-19 for an example.
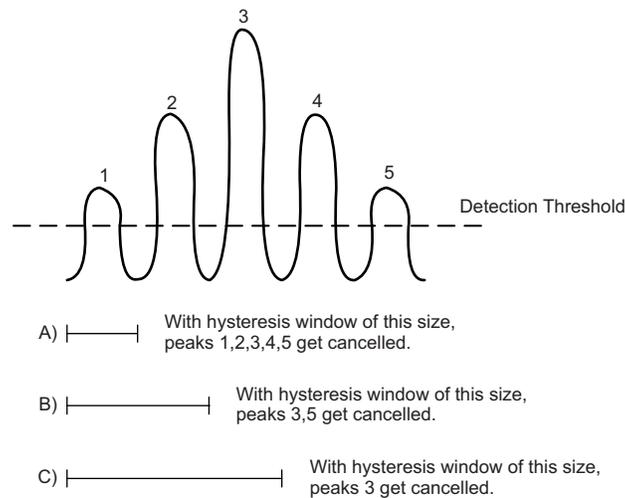
Figure 2-19. Example Hysterisis Control Related to Multiple Peak Cancellation

2.5.3.3 PostCFR Processing

In Figure 2-14, the postCFR processing is the peak signal gain adjustment, with the interpolation by 2 and the circular limiter.

PostCFR gain – After CFR has clipped the signal, the peak antenna stream output is adjusted for both proper DPD range of operation and peak TX signal power (this is the last fractional db gain adjustment in DFE). The postCFR gain has a range of -inf to 6db, and an operating and updating setpoint for each antenna stream. The postCFR gain is updated with an API.

PostCFR interpolate by 2 – The CFR mode of operation (see Table 2-9) uses the postCFR interpolate by 2 function to increate the IQ rate after CFR clipping. This is done in preparation for DPD, which needs expansion bandwidth. If the preCFR interpolate by 2 is not used, the Int2m 109 tap half band filter is used. If postCFR interpolation is done and preCFR interpolation is done, the postCFR interpolation uses the 19tap halfband filter.

Circular limiter – The circular limiter limits the antenna stream signal to a fixed IQ magnitude. This limiter is a single-sample gain correction based on the lookup table (LUT) gain (see Figure 2-20). The LUT table is loaded with the fixed register writes for CFR. Normally, the user operates the CFR block and postCFR gain to have a peak IQ output < -6dbc. The circular limiter is not intended to clip the signal: when it activates, the TX output spectrum will not meet the desired TX spectrum quality. The magnitude and inverse gain programmed in the LUT limit the IQ magnitude to (-6dbc/sqrt2). The LUT has 128 sample elements and interpolation between points for the inverse gain calculations.
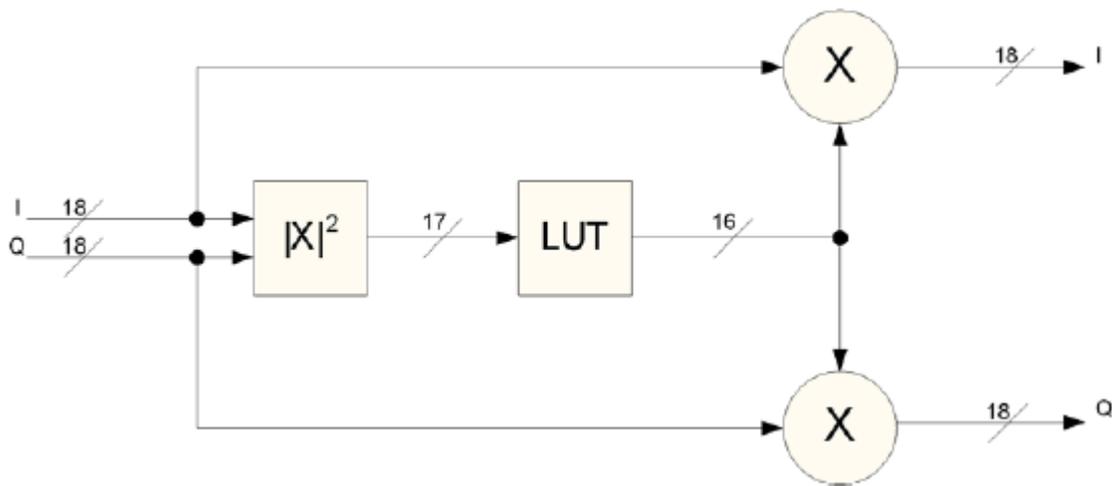
Figure 2-20. Circular Limiter Diagram

2.5.4 Synchronization Events

The synchronization events for the CFR block APIs are normally the DL synchronization signal from the BB block, or the MPU sync (updated immediately).

2.5.5 Software Application Interfaces

> **NOTE:** See Reference 6 (Chapter 3) and for additional details.

API_PreCFR_Gain – The gain before CFR is adjusted per TX antenna, with a PA protection setback gain adjust. This gain is adjusted in consideration of the sumchain shift gain.

API_PostCFR_Gain – The gain after CFR, normally adjusted for peak level to DPD

API_CFR_CoefUpdate – The calculated CFR clipping coefficients are updated into a CFR stream

API_CFR_CalcCoef – The user provides the TX antenna stream carrier frequency, base filter, and carrier gain to calculate the CFR clipping filter.

2.5.6 Important Programming Concepts

CFR Table 2-8 indicates the sumchain-interleaved IQ stream formats, and the desired number of CFR processing streams. Table 2-9 helps select the fixed configuration.

PreCFR interpolation and postCFR interpolations are important for the final DPD block sampling rate. These are set in the fixed configuration and the CFR mode tables. In most applications, use the postCFR interpolation of 2.

The amount of CFR that can be applied to an antenna stream is based on the peak detection, target fix values, and the antenna stream, which typically for LTE clips 2db of peaks. In WCDMA, the standard tolerates more EVM per carrier, so more clipping can be done. The TX block has power meters to monitor antenna stream peak and RMS power during adjustment. The preCFR gain and sumshift in the summer set the TX antenna stream IQ value for CFR.

The cancellation pulse complex filter must be computed and updated for the carrier type, carrier frequency (DDUC NCO), and weighting factor; there is an API for the calculation and update of the CFR filter. The cancellation pulse is generated in a zero delay and half-delayed format. These two filters must be loaded for proper CFR operation.

PostCFR gain sets the transmit stream peak gain for the antenna stream.

2.6 CDFR
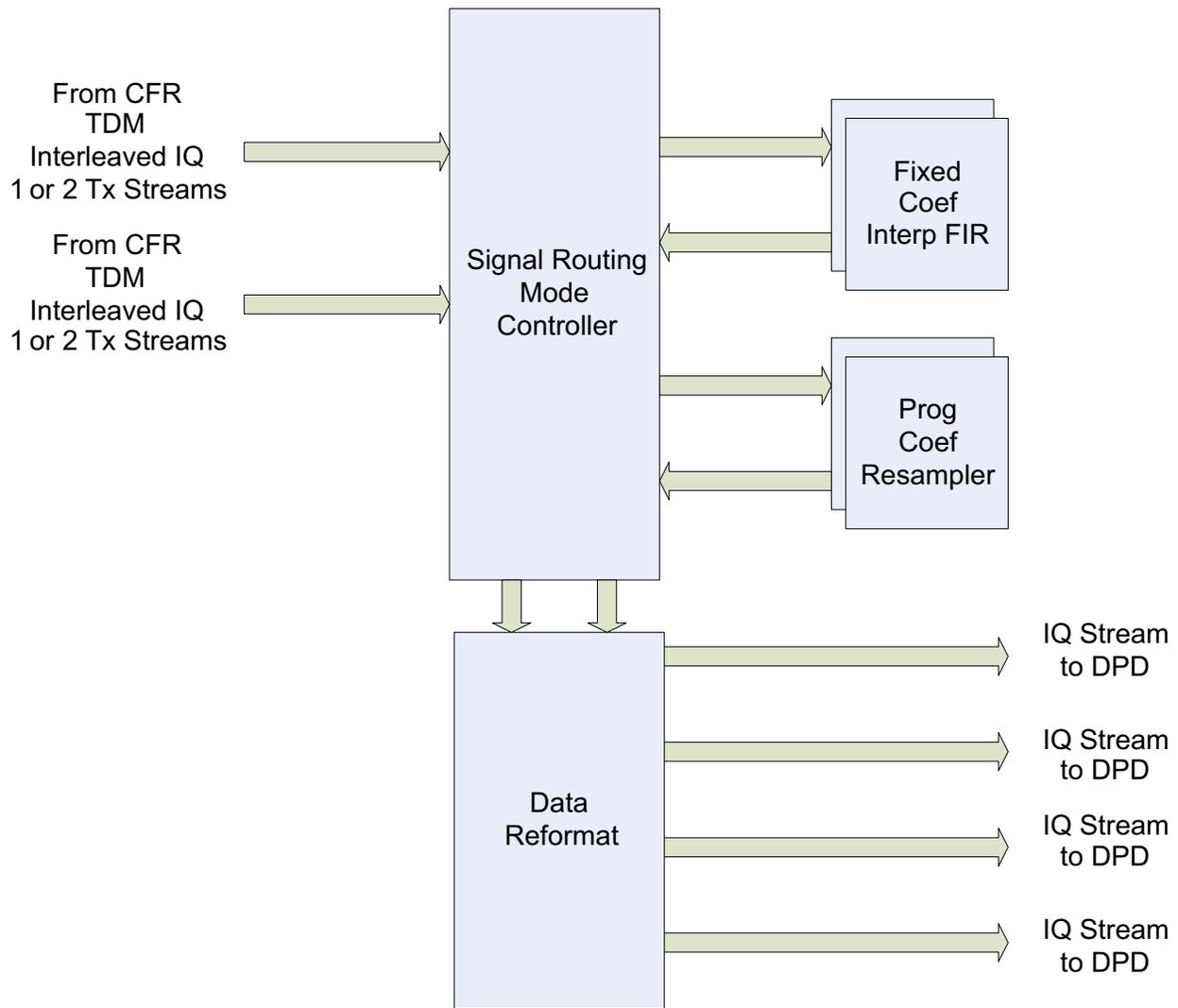
Figure 2-21. CDFR Block Diagram

2.6.1 CDFR Function

The CDFR block interpolates the CFR block output streams to the DPD input rate. The CDFR block has two different interpolation blocks that are utilized based on the operating mode. Each of the two CFR buses has one or two interleaved IQ data buses. Each of the DPD output streams has a unique parallel IQ bus.

2.6.2   CDFR Inputs/Outputs

Table 2-10. CDFR Inputs and Outputs

Name	I/O	Basic Description
MPU Bus	Both	Parallel data/ address/ module address synchronous bus for programming registers / memories
CFR signal bus 0 in	I	Time interleaved IQ bus from Summer block, contains 1 or 2 antenna stream data
CFR signal bus 1 in	I	Time interleaved IQ bus from Summer block, contains 1 or 2 antenna stream data
TxOverPower signals	I	Each TX antenna stream has a setback signal, this is used to select the Setback gain for PreCFR , from TX sub-block
CFR signal bus 0 out	O	Time interleaved IQ bus from postCFR output to CDFR, contains 1 or 2 antenna stream data
CFR signal bus 1 out	O	Time interleaved IQ bus from postCFR output to CDFR, contains 1 or 2 antenna stream data
CaptureBufferCFR0 InBus	I	IQ bus to stream the preCFR IQ for specific antenna streams from CFR0
CaptureBufferCFR0 OutBus	O	IQ bus to stream the postCFR IQ for specific antenna streams from CFR0
CaptureBufferCFR1 InBus	I	IQ bus to stream the preCFR IQ for specific antenna streams from CFR1
CaptureBufferCFR1 OutBus	O	IQ bus to stream the postCFR IQ for specific antenna streams from CFR1
Sync Bus	I	A group of signals that indicate the time-event to perform an operation.
Interrupt Bus	O	Signals to MISC module to indicate a CFR event occurred
Test Bus	Both	Signals to global capture buffer Test Bus data source for capture

2.6.3   CDFR Basic Description

The CDFR provides filtering and interpolation from the CFR output bus rate to the desired DPD or TX (if DPD is not used) sample rate. The CFR output buses are time-division-multiplexed buses that operate at DFEPLL clock/2 (one antenna per bus) or DFEPLL clock/4 (two antennas per bus). The CDFR bus can control clock gating for a effective slower IQ rate to the DPD block. The CDFR interpolation ratio and gating factors are selected during initial register programming, and cannot be changed after the block is initialized.

Table 2-11. CDFR Common Operating Modes

CDFR Operating Mode	Total Interpolation	Interp2 – Fixed Filter	Resampler	CDFR Eng Modes
Bypass	1	Bypass – 1	Bypass - 1	b1
Interp2	2	Interp2	Bypass - 1	d1/d2/d3
Fract Resample	3/2	Bypass - 1	3int/2dec	b1 or b2

The CDFR mode configures the fixed interpolate by two, and the resampler into the signal path. The same CDFR interpolation ratio is applied to all antenna streams. The desired DPD oversample rate and special clocking controls provide the output buses to the DPD block. In some cases, the fixed interpolate by two, and the fractional interpolation are used together.

The DPD processing operates at the CDFR output rate. The CDFR output rate is a combination of the DFE PLL rate and clock gate controls, set in the programming file.

In most cases, interpolating by two means the fixed filter mode is used. If there is a different interpolation ratio, the resampler or fixed interpolation by two and resampler can be used. It is important to set the IQ rate of the DPD block, or the TX input, if the DPD block is not used.

The CDFR fixed interpolation filter is a 95 tap fixed filter. The CDFR filter has 40% BW. The CDFR resampler coefficients are programmed at initial register programming. The number of taps is based on the interpolation/decimation ratio (8 * interpolation ratio).

2.6.4 CDFR Synchronization Events

The CDFR is synchronized to the DL sync event or MPU (software) sync event.

2.6.5 CDFR Software Application Interfaces

There are no software API dynamic adjustments for the CDFR block.

2.6.6 CDFR Important Programming Concepts

The CFR operates with at least 1.1× the signal bandwidth, typically 1.25× the signal bandwidth. CFR normally interpolates by two after CFR, and this is coupled with the CDFR interpolation to develop the DPD bandwidth. If DPD is not used, the CDFR ratio can be one. CDFR is programmed during the DFE fixed configuration.

CDFR Interpolation = DPD IQ rate/CFR Output IQ rate

The CDFR interpolation, CFR output IQ rate, DPD desired IQ rate, and DFEPLL must be considered for the register programming file.

For an example without DPD, the CFR input rate is 61.44 Mhz, the CFR output rate is 122.88 Mhz, and CDFR can have a ratio of one, so that the CFR output rate matches the JESD TX equivalent IQ rate.

For an example with DPD, the CFR input rate is 61.44 Mhz, the CFR output rate is 122.88 Mhz, and the CDFR is programmed to a 3/2 interpolation. The CDFR parallel output occurs at the 245.76-Mhz IQ rate, and every four clock cycles there are three valid outputs. Special clock controls are used, and the DPD rate is 184.32 Mhz. The TX block also resamples the DPD output back to the JESD TX equivalent rate.

2.7 Digital Pre-Distortion (DPD)
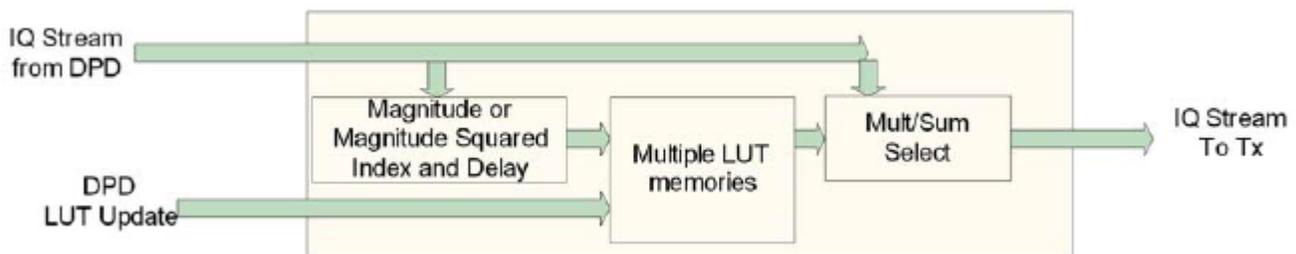
Figure 2-22. DPD (1 of 4 streams) Block Diagram

2.7.1 DPD Function

Each of the four TX streams from the CDFR block is an input to the DPD block. The DPD block provides a non-linear correction function for each TX stream independently. The nonlinear correction has both a number of correction solutions (one to four) available, and a number of memory solution look up tables (LUT) utilized for each TX antenna stream.

The nonlinear correction is indexed based on the magnitude, or magnitude squared, of the incoming TX signal. This signal is determined with a hardware register setup, and software configuration and software update of the LUT entries. The LUT is designed like the circular limiter discussed in Section 2.4. Each magnitude or magnitude squared sample creates an index to the memory. The correction coefficients for DPD are generated from the sampled signal, and the delay, using an example, has a magnitude or magnitude squared index to the LUT. There are several LUTs which provide the nonlinear coefficients for a specific TX antenna stream. The LUT and delays for the LUT index generate a specific solution set for DPD. The numbers of LUTs utilized are equal to the number of memory terms for this DPD solution. In the initial configuration, the LUT contents provide a linear gain of one and no nonlinear solution. As the DPD cycle updates the coefficients, the nonlinear LUT content is updated, and then the FIR-like structure convolved with the TX antenna stream provides the nonlinear correction.

All of the LUT memories have a dual set of coefficients; one that is currently in the signal path, and one that can be updated by the MPU bus to the DPD TX antenna selected.

2.7.2 DPD Inputs and Outputs

Table 2-12. DPD Inputs and Outputs

Name	I/O	Basic Description
MPU Bus	both	Parallel data/ address/ module address synchronous bus for programming registers / memories
DPD Bus0 in	I	Interpolated IQ parallel bus from CDFR
DPD Bus1 in	I	Interpolated IQ parallel bus from CDFR
DPD Bus2 in	I	Interpolated IQ parallel bus from CDFR
DPD Bus3 in	I	Interpolated IQ parallel bus from CDFR
DPD Bus0 out	O	Interpolated IQ parallel bus with nonlinear distortion for TX stream0
DPD Bus1 out	O	Interpolated IQ parallel bus with nonlinear distortion for TX stream1
DPD Bus2 out	O	Interpolated IQ parallel bus with nonlinear distortion for TX stream2
DPD Bus3 out	O	Interpolated IQ parallel bus with nonlinear distortion for TX stream3
Sync Bus	I	A group of signals that indicate the time-event to perform an operation.
Interrupt Bus	O	Signals to MISC module to indicate a DPD event occurred
Test Bus	both	Signals to global capture buffer Test Bus data source for capture

2.7.3 DPD Basic Description

The interpolating LUT first described in the circular limiter (see CFR description) is the basis for the memory nonlinear function solution set (see Figure 2-22). The CDFR antenna stream signal is processed for magnitude squared or magnitude, then quantized to create the LUT index for the memory nonlinear function solution set.

The quantized LUT index can be magnitude squared or magnitude format. This must be selected in the DPD register programming before initialization, and by the DPD software.

The interpolating LUT generates a memory coefficient for the specific memory element of the solution set. The DPD hardware and processor software must be programmed for the proper number of terms for each solution set. There are two general DPD operating modes, two TX antennas, and four TX antennas. The numbers of solution sets and memory taps per solution set are based on the DPD mode and the number of TX antennas. The hardware is typically programmed for maximum utilization. The software can zero the unused LUTs for the unused memory or unused solution sets. A solution set is a LUT programmed with a nonlinear set of coefficients for a specific TX antenna. The DPD hardware must be programmed for the same number of solution sets and memory taps as the software, to ensure that the delay-indexing and LUT contents are applied correctly.

Table 2-13. DPD Memory Taps Based on Number of TX Antennas/Number LUT-Solution Sets

Number 1x Tx Antennas	1 Solution Set Number Memory Taps	2 Solution Set Number Memory Taps	3 Solution Set Number Memory Taps
2	36	18	12
4	18	9	6

As an example, if the user has two TX antennas and three solution sets, they can have up to 12 memory taps. Each solution set has one LUT index, and a set of LUT index delays to index the memory tap LUTs. The nonlinear coefficients for this solution are generated from LUT magnitude indexed coefficients (each LUT has a specific magnitude to coefficient function). The memory tap LUT coefficients are multiplied by the I and Q stream signal with appropriate IQ signal delays, such as a FIR filter. The memory tap sum of products is for each solution set. The multiple solution set sum is then output to the TX block for the current IQ sample of this antenna stream. The nonlinear functions are DPD TX antenna-independent.

For example, if the user had a single LUT, they could correct for the gain expansion term only. Having multiple memory taps allows a magnitude or magnitude squared real correction to be applied to the IQ data.

In Figure 2-23 for AM-AM correction, the LUT is programmed for the software-corrected typical PA response, by measuring the feedback path, computing an error condition to an initial power amplifier desired response (model), and creating the inverse gain, so the system response matches the red line ideal response. The 3db headroom provides a limitation so that the PA system operates below the P1db point.

Figure 2-23. DPD Correction for AM-AM Distortion

The DPD system applied after using CFR to reduce the dynamic range of the signal allows the PA to be operated above the first region in Figure 2-23. The TX spectral emission mask and transmit error vector magnitude are typically improved in 3 DPD cycles for most power amplifiers. Figure 2-24 shows the nonlinear correction used to cascade the DPD nonlinear distortion, with the PA nonlinear distortion, to create a linear system. Figure 2-25 shows the transmit signal, and odd-order intermodulation harmonic distortion (IMD).
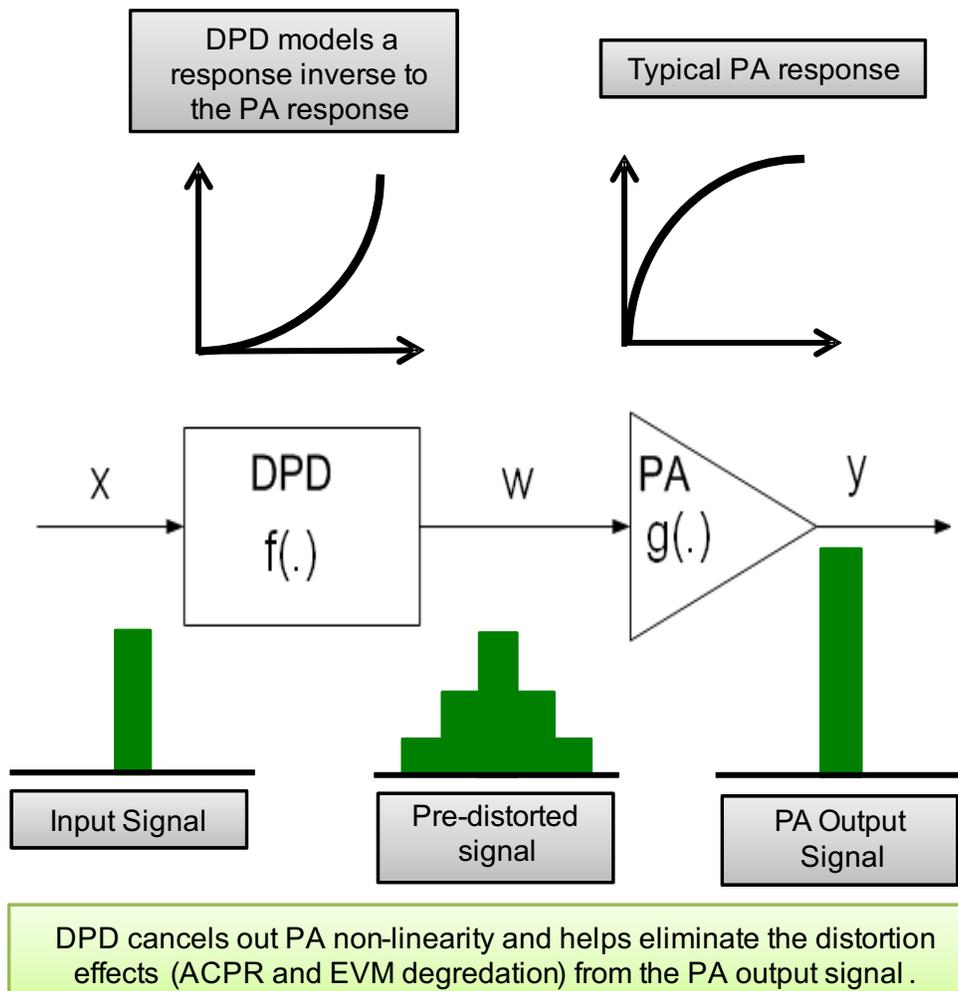
Figure 2-24. DPD Correction Showing TX Before Correction, Predistortion, and Post PA Response
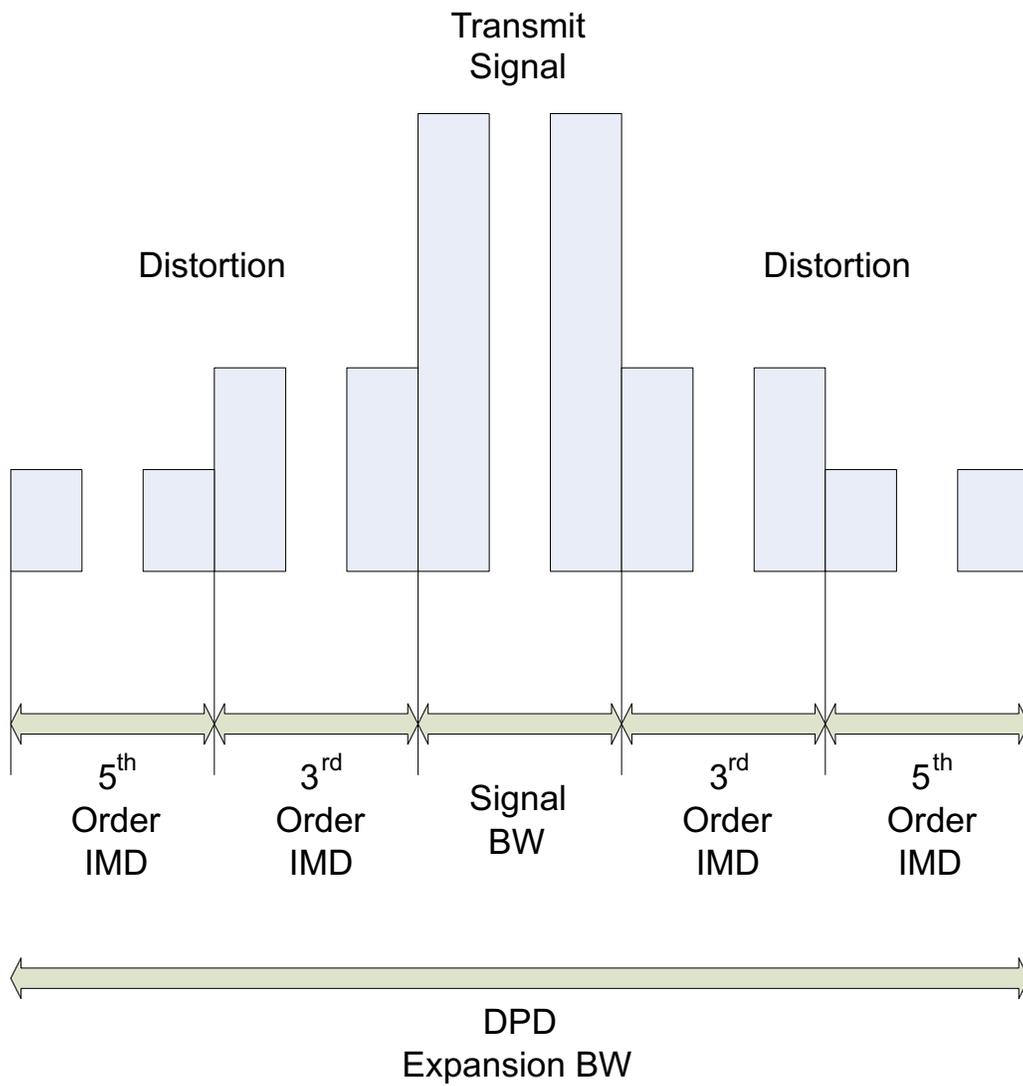
Figure 2-25. Transmit Bandwidth and DPD Expansion Bandwidth Example.
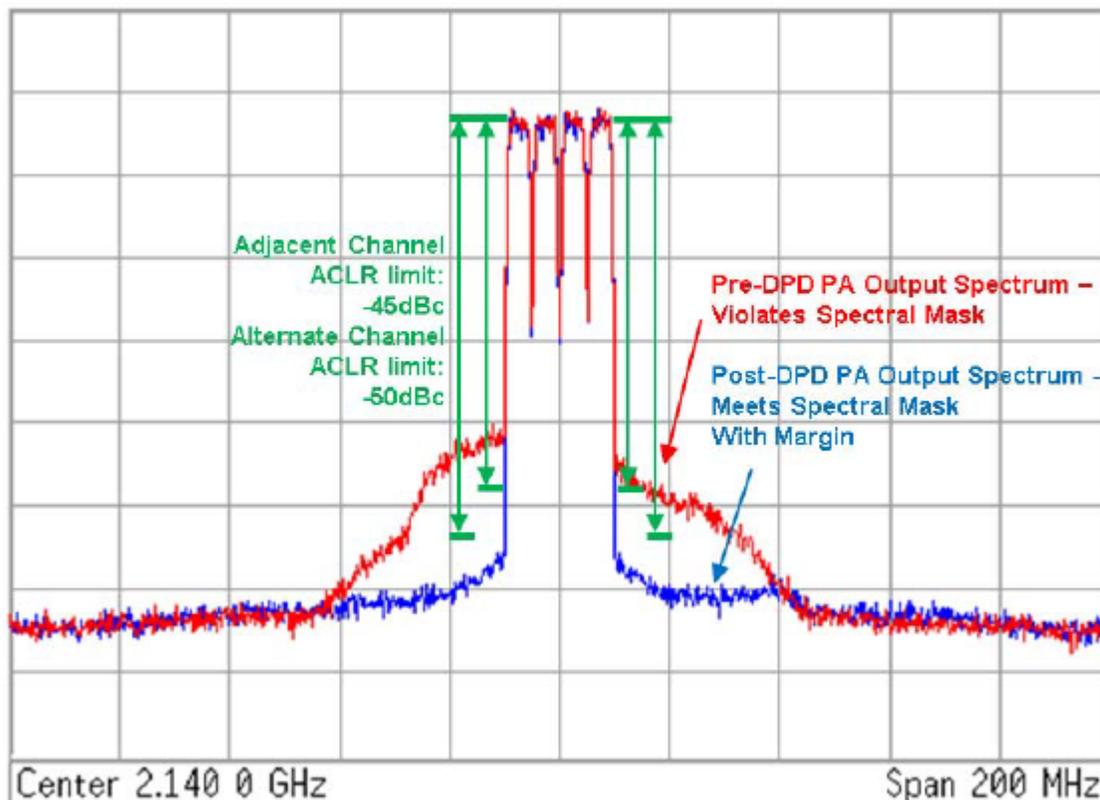
Figure 2-26. DPD Correction Showing Spectral Emission Mask Improvement

2.7.4 DPD Synchronization Events

The DPD is synchronized to the DL sync event or MPU (software) sync event.

2.7.5 DPD Software Application Interface

> **NOTE:** See Reference 6 (Chapter 3) and for additional details.

The DPD sub-blocks require hardware (register programming) and software configuration to manage the number of nonlinear solution sets (1 to 4), and the number of memory terms (depends on mode and the number of solution sets).

The DPD sub-block solution sets and memory terms are programmed by the DPD antenna stream over the MPU bus. After programming one or more DPD antenna streams, the memory data is transferred for signal processing with a synchronization signal.

API_DPDCoefUpdate indicates that the DPD coefficients for a specific TX stream can be updated. This is normally controlled from the DPD adaption process and not loaded separately.

2.7.6 DPD Important Programming Concepts

DPD hardware must be programmed for the desired number of solutions (1-4), and number of memory terms (depends on solution and mode).

DPD hardware must be programmed for signal quantization index for LUTs, based on magnitude or magnitude squared.

Because the signal processing is applying gain expansion for most power amplifiers and nonlinear gain, –6dbfs peak at the DPD input is desired, to allow for dynamic range expansion by at least 3 db. This must be co-ordinated with the setup of the TX PA limiter (range to trigger setback / trip), and the follow on JESD-TX processing gain.

The DPD coefficient has a double buffer that is synchronized when new coefficients are loaded. The initial hardware coefficients used in programmation are a single tap slope 1 as a DPD bypass. The software calculates the new coefficients, updated for a specific DPD stream, then the software applies a hardware-timed (DL sync) or MPU sync (software MPU update).

When DPD is in the initial register programming setup, the DPD input and DPD output capture buffer should have the same spectral component, where the DPD output is delayed by the effective memory tap and hardware delay.

When software is updating the DPD coefficients, the nonlinear gain expansion raises the gain at the DPD output. The amount of gain expansion must be factored into the settings for the TX PA protection, and the peak TX power. The JESD transceiver power monitors and JESD transceiver input gain can help set the final TX peak power level.

2.8 TX Sub-Block
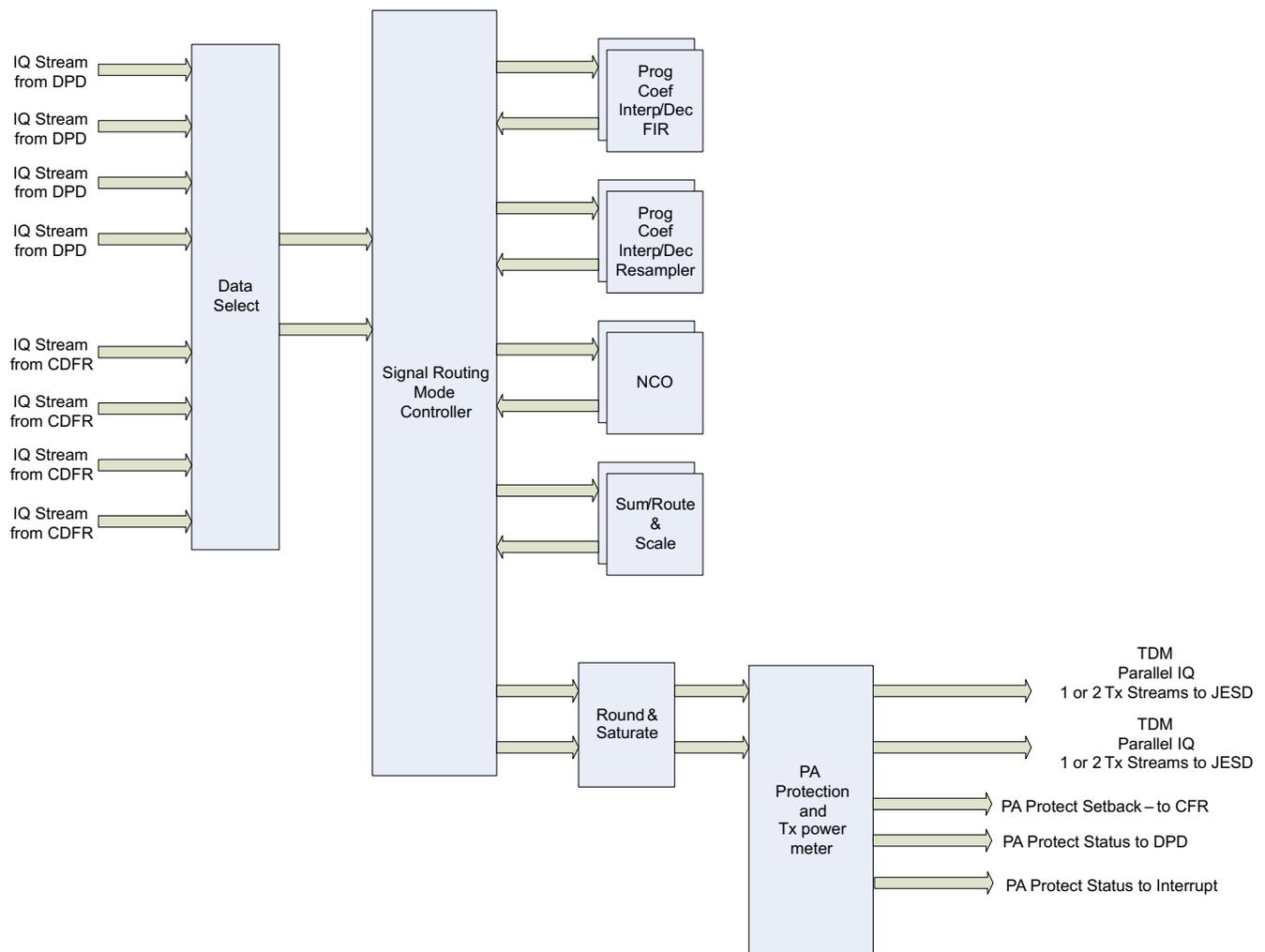
Figure 2-27. TX Sub-Block Block Diagram

2.8.1 TX-Sub-Block Function

The TX block provides 5 important functions for the TX signal processing:

1. The TX block selects the signal path from the DPD block, or from the CDFR block if the DPD block is powered down.

2. The TX block interpolates or decimates the DPD signal rate to the JESD TX output rate. The TX interpolation or decimation mode is programmed during initial TX programmation.

3. The TX block has numerically controlled oscillators (NCO) to provide a frequency translation for low IF systems. If the NCO is not utilized, this is a zero IF complex transmit output.

4. Each TX antenna has a power monitor and protection logic function. The power monitor provides the RMS and peak power of each TX stream. The protection logic provides a setback or transmit-inhibit function if the RMS power exceeds a programmed setpoint. The protection logic has a limiter that can reduce the signal peak magnitude.

5. The TX sub-block reformats the data for the JESD TX input.

2.8.2 TX Sub-Block Inputs and Outputs

Table 2-14. TX Sub-Block Inputs and Outputs

Name	I/O	Basic Description
MPU Bus	both	parallel data/ address/ module address synchronous bus for programming registers / memories
DPD Bus0 out	I	DPD output bus TX stream 0
DPD Bus1 out	I	DPD output bus TX stream 1
DPD Bus2 out	I	DPD output bus TX stream 2
DPD Bus3 out	I	DPD output bus TX stream 3
CDFR Bus0 out	I	CDFR interpolated output bus to DPD input stream 0
CDFR Bus1 out	I	CDFR interpolated output bus to DPD input stream 1
CDFR Bus2 out	I	CDFR interpolated output bus to DPD input stream 2
CDFR Bus3 out	I	CDFR interpolated output bus to DPD input stream 3
TX stream Protection bus output	O	TX PA Protection output has a setback control for each preCFR gain selection, and a inhibit status indication for the DPD block
TX stream output bus0	O	TX antenna stream 0, 1 are output as a TDM parallel IQ bus
TX stream output bus1	O	TX antenna stream 2, 3 are output as a TDM parallel IQ bus
Sync Bus	I	A group of signals that indicate the time-event to perform an operation.
Interrupt Bus	O	signals to MISC module to indicate a DPD event occurred
Test Bus	both	signals to global capture buffer Test Bus data source for capture

2.8.3 TX Sub-Block Basic Description

See Figure 2-27 for the TX sub-block diagram. The selection of the DPD output, or CDFR output for the TX input bus, is controlled through programmation at initialization.

The interpolation or decimation of the selected TX stream output data is common for all TX antennas. The TX sub-block mode and the desired TX input/output ratio are programmed when loading the initial registers. The TX stream output IQ rate must match the JESD TX IQ rate. The TX sub-block mode determines which filter or set of filters to use. The resampling filter has a set of user-configurable coefficients, so the filtering and rate can be designed to interpolate/decimate, resample, bypass, or filter the TX stream signal. The rate ½ filter can have programmable coefficients used for the image attenuation, and for DPD correction filtering.

In the TX Table 2-15, the programmable taps, ratio 1 or 2 filter, can decimate or interpolate by 2, or just be a filter. The ratio 2 filter is programmed with 55 tap odd symmetric half band taps. In the ratio 1, this filter has 27 odd symmetric taps. In the 27-tap case, the FIR filter passband and stopband can be designed for DPD-desired transmit bandwidth. In the ratio 1-bypass cases, the center tap impulse is programmed. The resampler is programmed given the M (interpolate) / N (decimate) ratio, where M*8 is the number of resampler coefficients. Although the resampler coefficients can be reprogrammed, to provide fractional timing offsets the initial programming is based on the fractional bandwidth and image attenuation. TI recommends leaving the resampler coefficients with the default programmation.

Table 2-15. TX Sub-Block Common Operating Modes

TX Sub-Block Operating Mode	TX Interpolation (I) or Decimation (D)	Ratio 1 or 2 Interpolation(I) or Decimation(D) Filter	Resampler	TX Eng Mode
bypass	1	1 – 27 tap odd symmetric filter, with Impulse center tap	Special Int2/Dec2 – special impulse filter	Mode 8 or 10 or 14
Decimate by 2	Dec 2	2 – Decimation – 55 tap half band filter is programmed for 40% BW	Resampler coefficients and ratio set for bypass	Mode 2-9. Prig Resampler coefficients for bypass
Dec 3/2	Dec 1.5	1 – 27 tap odd symmetric filter, with Impulse center tap	Int2/Dec3 – typically programmed for 60% of the resampled BW	Mode 2-9

If the DPD IQ rate is at a higher rate than the JESD TX IQ rate, the DPD signal can be filtered and decimated to the JESD transmit rate. Typically, the DPD output is not interpolated to the JESD TX IQ rate.

The NCO provides frequency translation of the TX antenna stream signal. The NCO is similar in description to the one found in the digital downconverter/upconverter (DDUC) (Section 2.3). The NCO can be dynamically changed while the TX block is processing signals, using a software API. The NCO converts the zero IF transmit to low IF transmit.

The route/sum/scale block scales or rounds the transmit stream that is applied to a specific JESD TX stream. The sum is used when multiple TX streams are combined. The scale applies power of 2 gain or attenuation to the TX output stream signals.

There is one PA protection block for every two TX antenna streams. The PA protection block has peak and RMS power limiting functions, based on each TX antenna stream magnitude squared value, and user-programmable thresholds (see Figure 2-28).
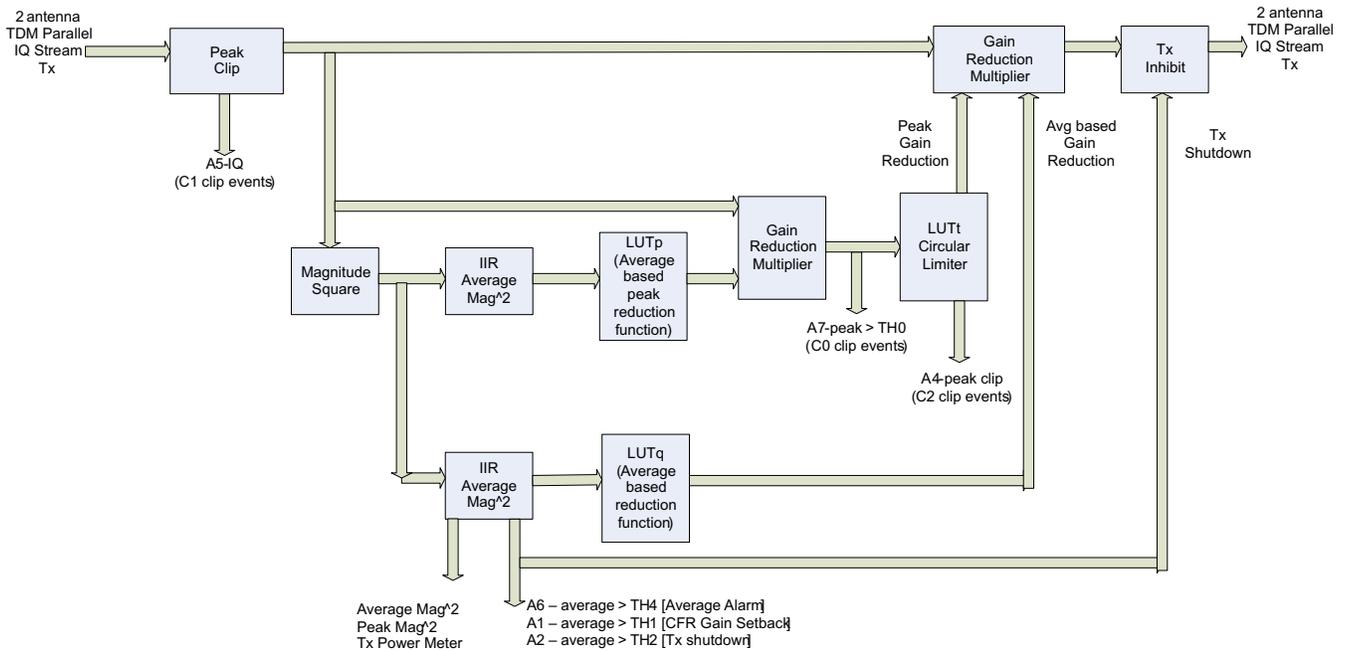
Figure 2-28. TX Sub-Block PA Protection (1 of 2) Diagram

Control functions output the A1 preCFR gain setback, and A2 inhibit TX stream output.

The square clipper appears to limit the I and Q input to a peak value. A counter counts for an interval, and a peak alarm is generated if there are more than C1 clipping events. The logic signal for the peak clip is called A5.

The IQ signal is converted to magnitude squared for peak and rms processing for gain setback, control functions, and for the TX power meter.

There are two IIR (infinite impulse response) filters to generate an average magnitude squared signal.

The IIR filter (upper IIR in Figure 2-28) computes an average of the magnitude squared signal. LUTP applies a transfer function from the filtered magnitude squared to the power setback function for the peak IQ signal. The LUTp table provides a transfer function for the peak power setback, based on the average power.

The A7 status signal is a peak alarm output, if magnitude squared peaks are higher than Th0 (threshold) for more than C0 counts.

LUTt provides a circular limiter function, in that the magnitude squared signal of the IQ sample is used to develop a peak gain setback. The LUT is programmed with inverse gain so the gain is 1 for signals below the limiter threshold and are programmed to < 1, and a peak over the LUT table-threshold occurs.

The A4 status signal indicates that peak clipping has occurred for C2 counts within a sample count. The A4 signal is a peak limiter status signal.

At the output of the LUTt, if the gain is 1, there is no limiting action for peaks. A low comparator at the LUTt output checks to see if there are peak clipping events (cc2). If the number of cc2 events is > C2, then A4 is active. A4 is a status indicator that peak clipping is occurring.

The IIR filter (lower IIR in Figure 2-28) computes an average of the magnitude squared signal. The arithmetic average and peak are used for the TX power meter output for this antenna stream. The arithmetic average is also used for the alarm and control functions:

- If the average magnitude squared value is above a setpoint TH4, the A6 output activates an interrupt indicating filtered magnitude squared (power) is too high.

- If the average magnitude squared value is above a setpoint TH1, the A1 output activates, and the preCFR gain setback function occurs.
- If the average magnitude squared value is above a setpoint TH2, the A2 output activates, and the TX stream output is inhibited.

The IIR average magnitude squared value is also input to another LUT (LUTq), which develops an average power setback function. This function is not normally used in TCI663xK2L applications.

The peak and average magnitude squared setback multiplier is then applied to the IQ stream of the signal. The IQ stream is then sent through the TX inhibit to gate the TX output to the JESD block.

2.8.4 TX Sub-Block Synchronization Events

The TX sub-block is synchronized to the DL sync event or MPU (software) sync event.

2.8.5 TX Sub-Block Software Application Interface

> **NOTE:** See Reference 6 (Chapter 3) and for additional details.

API_Tx_ NCOUpdate – Frequency-translates the TX antenna stream

API_Tx_PAProtectConfig – Configures registers and initializes the PA protect logic

API_Tx_PAProtectStatus – Gets PA protection status by TX antenna stream

API_Tx_PAProtectControlUpdate - Modifies the PA protection state after an event

API_Tx_PAProtectPowerMeterConfig – Configures the IIR power meter (part of PAprotect configuration)

API_Tx_PAProtectReadPowerMtr – Reads the IIR power meter for TX antenna streams

2.8.6 TX Sub-Block Important Programming Concepts

The TX sub-block must be programmed to select the DPD output or CDFR output.

The TX sub-block mode determines the TX FIR filter and TX resample ratio. The TX FIR filter has programmable coefficients. The TX resampler interp/decimation ratio has preprogrammed coefficients. These coefficients are loaded at programmation time only. The TX sub-block interpolation and decimation adapts the DPD IQ rate to the JESD TX IQ rate.

The TX sub-block for zero IF (default) or low IF can be programmed using the TX NCO mixer. The feedback mixer must be programmed in a complimentary fashion for low IF mode. The TX and feedback mixer can be programmed after initial register programming, using APIs.

The Tx_PA protection can have custom thresholds and count values for the protection alarms, CFR setback, and TX antenna inhibit functions. The PA protection LUTs are not dynamically updateable; they must be initially programmed to the desired function.

Special software is needed to control the PA protection logic for alarm, power setback, clipping, and trip conditions.

2.9 JESD Block
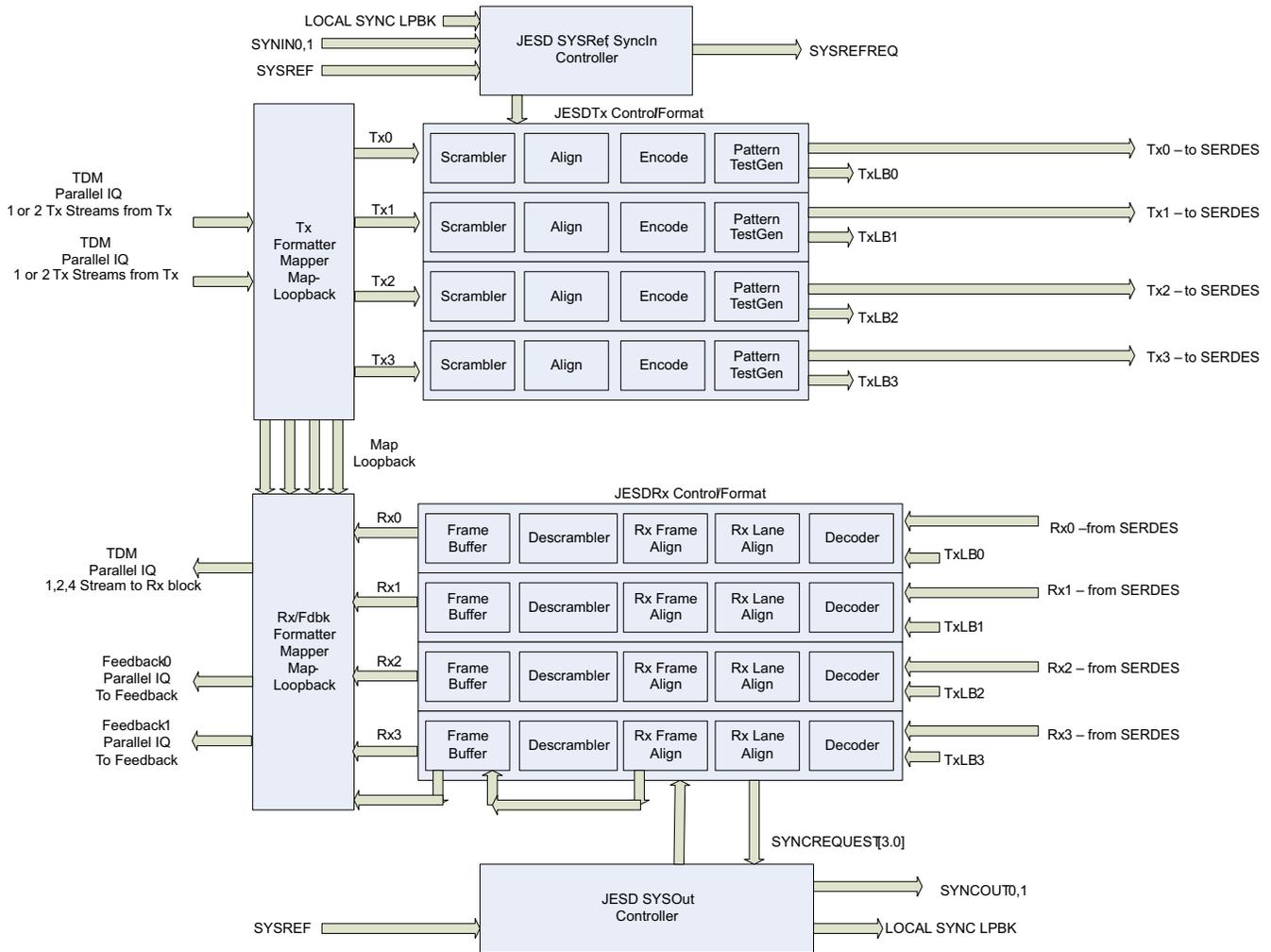
Figure 2-29. JESD Block Diagram

2.9.1 JESD Block Functions

The JESD block implements a JESD 204B subclass 0 or 1 multi-SerDes lane, and multi-link interface. The JESD block has four TX lanes, and four RX lanes that can be combined or separately used to support 1, 2, or 4 antenna streams. The JESD 204 interface can support one or two links in each direction to synchronize the TCI663xK2L DFE with an external JESD 204B transceiver.

The JESD block implements the mapping loopback for internal TX to RX, or TX to feedback digital loopback.

The JESD block formatter can route IQ signals, multiple IQ signals, or split I and Q signals to a JESD204 TX lane.

The JESD block provides JESD 204B scrambling, encoding, alignment, and test pattern generation for the TX lanes.

The JESD block implementation has a lane loopback used for testing.

The JESD block implements the RX sync output, and TX sync input JESD204B subclass 1 signals used for synchronization and error notification. The controllers also implement the JESD 204B SYSREF local multiframe clock (LFMC).

The JESD block implements the JESD 204B receive logic, decoding, synchronization, alignment, descrambler, and buffering.

The JESD formatter/mapper selects the map loopback or received JESD signals, and reformats them for the TDM parallel IQ RX block, and parallel IQ feedback blocks.

2.9.2 JESD Block Inputs and Outputs

Table 2-16. JESD Block Inputs and Outputs

Name	I/O	Basic Description
MPU Bus	Both	Parallel data/ address/ module address synchronous bus for programming registers / memories
TX stream input bus0	I	TX antenna stream 0 (2 antenna stream) 0, 1(4 antenna stream) are output as a TDM parallel IQ bus
TX stream input bus1	I	TX antenna stream 1(2 antenna stream) 2, 3(4 antenna stream) are output as a TDM parallel IQ bus
Rx0 parallel input bus from SerDes	I	20-bit 8b-10b encoded bus from SerDes
Rx1 parallel input bus from SerDes	I	20-bit 8b-10b encoded bus from SerDes
Rx2 parallel input bus from SerDes	I	20-bit 8b-10b encoded bus from SerDes
Rx3 parallel input bus from SerDes	I	20-bit 8b-10b encoded bus from SerDes
SYSREF	I	The SYSREF signal is used for LMFC alignment in JESD204B subclass 1 mode. The SYSREF can be generated external to TCI663xK2L for multi-device synchronization, or internal to TCI663xK2L from the SYSREF logic section.
SYNCIN0,1	I	JESD204B Sync transmitter input, from the external JESD204B receiver through LVDS DFE signals, or DFE GPIO
Tx0 parallel output bus to SerDes	O	20-bit 8b-10b encoded bus to SerDes
Tx1 parallel output bus to SerDes	O	20-bit 8b-10b encoded bus to SerDes
Tx2 parallel output bus to SerDes	O	20-bit 8b-10b encoded bus to SerDes
Tx3 parallel output bus to SerDes	O	20-bit 8b-10b encoded bus to SerDes
SYSREFREQ (output)	O	SYSREF enable signal to external Clock solution through DFE GPIO
SYNCOUT0,1 (output)	O	JESD204B Sync receiver synchronization status, error to external JESD device through LVDS DFE signals, or DFE GPIO
Sync Bus	Both	A group of signals that indicate the time-event to perform an operation.
Interrupt Bus	O	Signals to MISC module to indicate a JESD event occurred
Test Bus	both	Signals to global capture buffer Test Bus data source for capture

2.9.3 JESD Block Basic Description

The JESD block within DFE has TX block to JESD 204 logic, TX JESD 204B single and multilane logic, parallel connections to SerDes, parallel connections from SerDes, RX JESD 204B single and multilane logic, JESD 204 logic to RX block, and feedback block outputs.

2.9.3.1 Link Synchronization and Error Handling of Link Errors

The SYSREF aligns the JESD 204B TX frame and multiframe clocks. The SYSREF also aligns the JESD204B RX frame and multiframe clocks. This alignment is discussed in section 4.8, 4.11 of the JESD204B standard (see reference 1 in Chapter 3). See Figure 2-30.
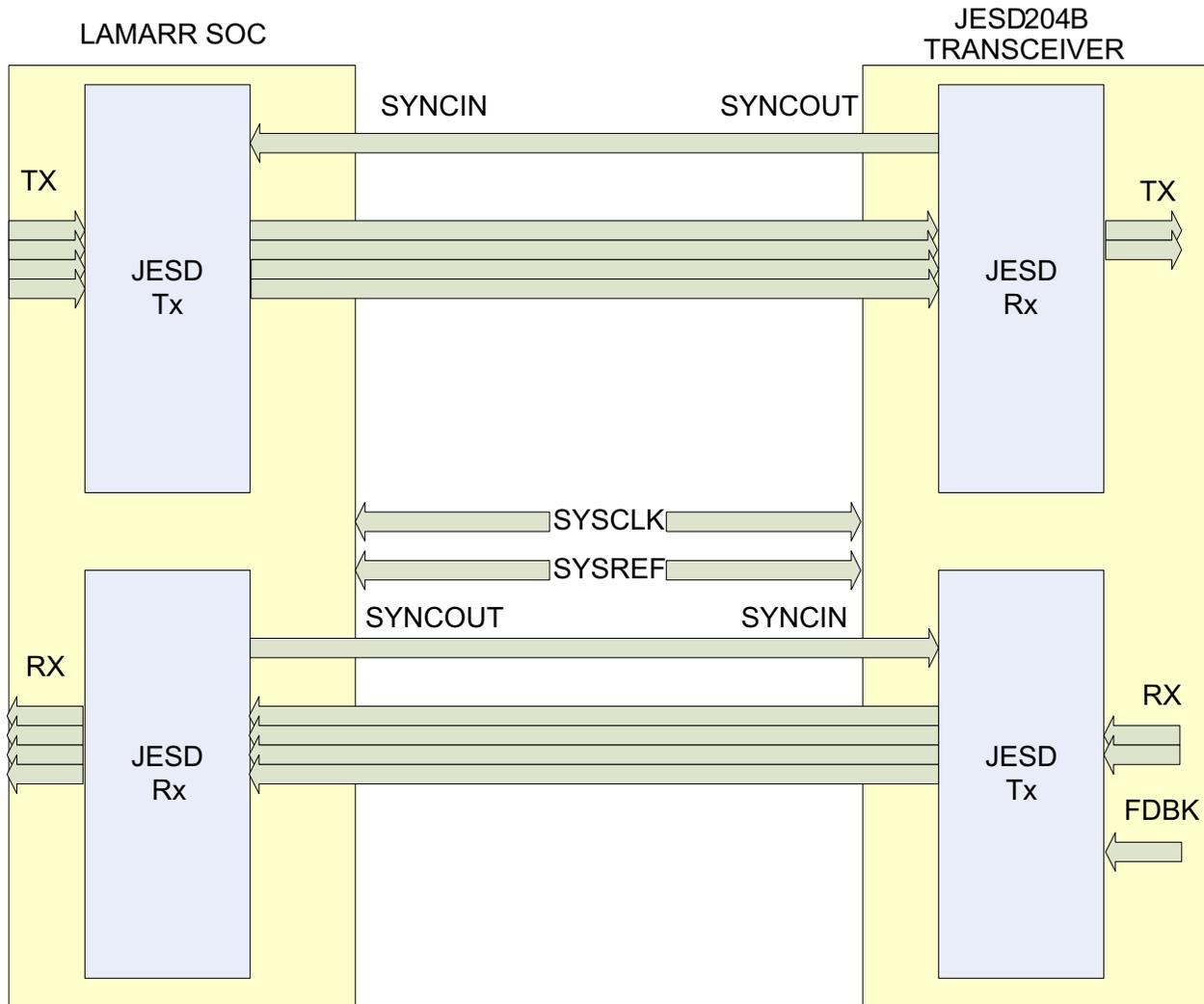
Figure 2-30. JESD Clock, Synchronization, and SerDes Data Diagram

2.9.3.2 Synchronization

Synchronization between the transmitter and receiver is done in several sections (see Figure 2-30). While the figure shows a SYNCOUT and SYNCIN pair, there are two SYNCOUT and two SYNCIN link controls in TCl663xK2L. Normally, link 0 is used for two-stream applications. Link 1 is used when there is a second JESD transceiver. Figure 2-30 is a simplified example, using one JESD Transceiver.

The initial synchronization is sampled by the common clock (SYSCLK) to align both devices to the frame or multiframe using the SYSREF. The transmitter initially sends synchronization characters over the serial links, while the receiver asserts the SYNCOUT (active low). When the receiver has detected the synchronization characters in the received stream, the received de-asserts SYNCOUT (logical high). The transmitter samples the SYNCIN, and determines that this link has been synchronized. The initial link operation alignment is discussed in section 5.3.3, 6.3 of JESD204B specification (ref 1 in Chapter 3) In Figure 2-29, the SYNCIN is used to control the SerDes lane synchronization by sampling the SYNCOUT from the other device JESD RX. In Figure 2-30, there is an individual lane check for the receiver. If a JESD receive lane detects that it is out of alignment, the SYNC_REQUEST controls the SYNCOUT(0,1) in programming to indicate the need to resynchronize a lane.

NOTE: The SYNCOUT link status signals can also indicate JESD lane errors received in the RX sections. The JESD error statistics are available in registers to determine the number of errors.

The JESD logic and software perform the initial powerup and device alignment.

2.9.3.3 Link SYNCOut, SYNCIn

There are two links for synchronization status. The link to JESD lane is done in programmation. Typically, a two antenna configuration uses SYNCIN0, SYNCOUT0. A four antenna configuration uses (ant0/1) SYNCIN0, SYNCOUT0 and (ant2/3) SYNCIN1, SYNCOUT1.

2.9.3.4 Signal Mapping

The TX formatter and mapper converts the TX stream signals from the TX block into four TX streams. The conversion process depends on the JESD TX mode (which is programmed during register writes). The JESD signal mapping block must support a parallel implementation of the desired IQ-interleaved, TDM IQ-interleaved, I-only, or Q-only interface. The mapping mode for loopback is discussed separately below. Table 2-17 shows some examples of JESD transceiver modes (there are other supported modes).

Table 2-17. JESD Signal Mapping Based on JESD Transceiver Mode

JESD Transceiver Mode	Number of Antennas	Map0T	Map1T	Map2T	Map3T	Map0R	Map1R	Map2R	Map3R
1	2	I-T0	Q-T0	I-T1	Q-T1	IQ-R0	IQ-R1	I-Fdbk	Q-Fdbk
3b	2	IQ-T0	IQ-T1			IQ-R01		IQFdbk	
3b3b	4	IQ-T0	IQ-T1	IQ-T2	IQ-T3	IQ-R01	IQ-R23	IQFdbk01	IQFdbk23
6b	2	IQ-T0	IQ-T1			IQ-R0	IQ-R1	IQFdbk	

The JESD signal transfer to and from the SerDes must conform to the desired data format and transfer rates.

Table 2-18. JESD Signal Transfer and Number of Clocks

TX to SerDes Interface Mode	Number of DFEPLL Clocks for IQ Transfer
Split (or individual) I,Q	1
1 antenna stream interleaved IQ	2
2 antenna stream interleaved IQ	4

NOTE: Other JESD transceiver IQ mappings are possible; these are programmed at the initial register load.

2.9.3.5 Internal Signal Loopback

In Figure 2-29, the TX mapped signals can be looped back to the RX (RX and feedback) at the mapping loopback. The signal is still in the initial IQ format, so no JESD processing has been performed. This is useful for internal testing; a configuration file sets up this internal loopback. Some of the mapping loopback is done through register programmation (special reg file configuration). Some of the mapping loopback and lane mapping are done through an API after the register files are loaded.

2.9.3.6 Scrambler (TX), Descrambler (RX or Feedback)

The scrambler and descrambler encode the IQ data in a method to reduce spectral distortions and EMI; this can be disabled. The programming of the DFE JESD and the JESD transceiver must be compatible to the scrambler and descrambler usage. See section 5.2 of the JESD 204B specification.

In Figure 2-29, the JESD TX alignment, encode, and test generator are the link layer, as referred to in section 5.2 of the JESD 204B specification.

2.9.3.7   TX Alignment Block

The TX data is inserted with a synchronization character for initial alignment. When the other JESD device has synchronized with these synchronization characters, we continue to output synchronization characters until the next frame boundary. This follows the replacement of IQ data with link configuration programmation at initial alignment. After initial alignment and during normal operation, IQ data is periodically replaced with alignment characters in a manner that allows for the recovery of replaced data in the JESD receiver. See section 5.3 of the JESD204B specification.

2.9.3.8   TX Encode

The TX encode block in Figure 2-29 is the conversion from the octet 8-bit data into a 10-bit implementation. The parallel connection from the JESD block is a 20-bit interface, so two octets are processed. The 8B/10B processing is described in 5.3.1 of the JESD204B specification.

2.9.3.9   Test Generator

The TX test generator replaces the 8B/10B encoded signal with a specific set of synchronization or bit-error-rate test generation. These are described in section 5.3.3.8 of the JESD204B specification.

2.9.3.10   Lane loopback

Lane loopback, a multiplexer at the JESD receive interface from the SerDes parallel data, can accept the TX lane 20-bit loopback or the SerDes 20-bit parallel data. This is used in testing, and must be programmed in the register file for the device (it is not API controlled).

2.9.3.11   Decoder

The JESD receiver has a 10B/8B decoder to convert the parallel data back to the 16-bit data field. The 16-bit data can contain synchronization characters, IQ data, or other data. The decoder helps with synchronization, clock recovery, and single-bit error detection. See JESD 204B specification section 5.3.

2.9.3.12   RX Lane Align

Each of the four RX SerDes lanes performs the initial lane alignment and sends the alignment request status to the SYNCOUT link controller. The lane alignment symbols are shown in section 5.3.3 of the JESD 204B specification (Reference 1 in Chapter 3). Each lane contains an elastic buffer that realigns the data across all lanes assigned to the same link.

2.9.3.13   RX Frame Align

After lane alignment, this logic monitors the location of the frame alignment and requests a re-synchronization if the lane detects that it is out of alignment. See Figure 2-29 and section 5.3.3 of the JESD204B specification (Reference 1 in Chapter 3).

2.9.3.14   Frame Buffer

Each lane frame buffer holds a frame of IQ data at a time. If a frame contains one or more 8b/10b decoding errors, it is replaced with the last frame that did not contain any errors.

2.9.3.15   RX/Fdbk Formatter – Loopback Selector

The frame buffers output contains the JESD transceiver-interleaved IQ, I or Q, or multiple TDM stream IQ data. The JESDRx mode converts these frames of IQ data back to the RX interface-parallel IQ TDM or feedback-parallel IQ format. The mapping loopback can select the test loopback generated earlier in Figure 2-29 for TX, or the frame buffer signals. The mapping loopback API controls both the TX and RX portions of the mapper for TX and RX signals.

2.9.4 JESD Block Synchronization Events

The SYSREF signal aligns the JESD clock and LFMC frame clocks. This synchronization event is internal to the JESD block, but can be selected.

The syncbus DL sync from the baseband interface can be selected.

The syncbus MPU sync can be selected as a software sync.

2.9.5 JESD Block Software Application Interface

> **NOTE:** See Reference 6 (Chapter 3) and for additional details.

JESD_API_LaneMapping – This API allows the TX and RX JESD lanes to be remapped after initialization (it does not change their format, only the data source or destination).

JESD_API_Resync – This API is used with the specific JESD 204B link (0 or 1) to reinitialize a bad SerDes link or multiple errors, which have not recovered automatically.

JESD_API_ReadStatus – This API provides the JESD204B controller status of the TX and RX logic.

2.9.6 JESD Block Important Programming Concepts

The JESD block receives the TX block IQ data, and sends this to the SerDes. The SerDes equivalent I or Q rate must match the SerDes programmation, including the interface rate.

The JESD formatting in the JESD block must match the JESD transceiver format for interleaved IQ, I and Q separately, or TDM-interleaved IQ. All lanes in JESD must be the same serial bit rate.

The register programming of the JESD lanes and modes is done at register programmation. The lane selection for modes or loopback can be overwritten with the mapping API.

The error status of JESD 204B link errors may need to be monitored to determine that SerDes programmation and SerDes equalization must be adjusted.

The JESD block transmits IQ data from the RX input to the RX block and feedback block. The SerDes equivalent I or Q rate must match the SerDes programmation, including the interface rate.

2.10 RX Sub-Block

Figure 2-31. DFE Block Diagram for RX

The RX sub-block, shown in Figure 2-31, is a front-end automatic gain control (feAGC) and block down converter. The RX sub-block output is forwarded to the RX DDUCs for individual RX carrier processing. In the TCI663xK2L and JESD transceiver configuration, the feAGC and block down converter- IQ imbalance correction are performed in the JESD transceiver.

Figure 2-32 shows the RX block with the feAGC and DVGA controller hidden, as the TCI663xK2L DFE application does not use these sections. The multichannel power meter is used to measure the magnitude squared complex integrated power for the RX input streams from the feAGC output.

> **NOTE:** There is a similar RX formatted output from the feedback block. It is a decimated output at the same rate as the RX block output, and is used for network listening mode (NLM).

Figure 2-32. RX Sub-Block Diagram

The JESD block outputs a TDM IQ parallel bus that contains the formatted RX streams. The RX input can have 1, 2, or 4 RX streams. The RX stream IQ rate must match the JESD RX IQ rate. In Figure 2-32, the empty box is the connection of the feAGC and DC canceller, which is not used for TCI663xK2L. The DC canceller output is routed to the RX sub-block and power meter input.

The RX sub-block transfers 1, 2, or 4 RX streams to the RX DDUCs. The JESD to RX sub-block transfers are listed in Table 2-19.

Table 2-19. JESD RX Number of RX Input Antenna Streams and Number of Clocks

JESD RX Number of Output Streams	Number of Clocks for TDM IQ Transfer
1	1
2	2
4	4

The RX DDUC have specific interface requirements for the RX output transfers, based on the number of channels in the DDUC. These are listed in Table 2-20.

Table 2-20. JESD RX Number of RX Output Antenna Streams and Number of Clocks

RX Block Number of Output Streams	Number of Clocks for TDM IQ Transfer	DDUC Number of Antenna Channels
1	2	1,2
2	4	2,3,4,6
4	8	4(special),8,12

2.10.1 RX Sub-Block Functions

The RX sub-block performs four functions, some of which are not used in the TCI663xK2L application due to the function being performed in the JESD transceiver (see Figure 2-32, Figure 2-33):

1. RX stream DC removal – Each JESD RX stream is processed to low pass filter, and subtract the filter from the RX stream signal. This function is not used in the TCI663xK2L.

2. RX stream front end automatic gain control (feAGC) – Each JESD RX stream is processed for automatic gain control (AGC), based on a predetermined integrated power to gain error, or signal above peak statistic gain error, or a signal below setpoint statistic gain error. This function is not used in the TCI663xK2L.

3. RX stream block down conversion – Each RX stream is processed for indexing to JESD input, frequency translation, decimation filtering, (II,IQ,QI,QQ) equalization, and bias subtraction.

4. RX stream IQ imbalance correction – A blind or directed adaption engine, to provide IQ gain and IQbias correction for I and Q for each stream. This function is not used in the TCI663xK2L.

2.10.2 RX Sub-Block Inputs and Outputs

Table 2-21. RX Sub-Block Inputs and Outputs

Name	I/O	Basic Description
MPU Bus	Both	Parallel data/ address/ module address synchronous bus for programming registers / memories
JESD Rx Output Bus	I	1,2,4 TDM parallel IQ bus with the RX streams
RX Output Bus	O	1,2,4 TDM interleaved IQ bus with the processed RX streams
DVGA Controller output bus	O	1,2, or 4 sets of DVGA controlled sets of bits these are connected to the DFE GPIO pin multiplexer logic (not used on TCI663xK2L)
Sync Bus	I	A group of signals that indicate the time-event to perform an operation.
Interrupt Bus	O	Signals to MISC module to indicate an RX Power meter update is available
Test Bus	Both	Signals to global capture buffer Test Bus data source for capture

2.10.3 RX Sub-Block Basic Description

The RX sub-block has specific input and output formats. In the initial register programming, the input format, output format, R2C, and decimation filters must be in a compatible arrangement to use this sub-block.

Table 2-22. RX Sub-Block Decimation Input and Output RX Streams

RX Dec. Ratio	R2C	F1 Filter (25% Band)	F2 Filter (50% Band)	Port Replication	Number /Rate Input RX Streams	Number /Rate Output RX Streams
1	no	byp	byp	no	2 complex streams 4 gated DFE clocks for all streams	2 complex streams 4 gated DFE clocks for all streams
2	no	byp	Dec2	no	2 complex streams 2 gated DFE clocks for all streams	2 complex streams 4 gated DFE clocks for all streams
2	no	byp	Dec2	yes	2 complex streams 4 gated DFE clocks for all streams	4 complex streams 8 gated DFE clocks for all streams
2	no	byp	Dec2	no	4 complex streams 4 gated DFE clocks for all streams	4 complex streams 8 gated DFE clocks for all streams

2.10.3.1 RX-R2C

The RX sub-block Figure 2-32 shows the R2C as the first RX sub-block. The RX block has two operating modes; one for real inputs, and one for complex inputs. The real input would be processed by an Fs/4 (odd Nyquist zone) or 3Fs/4 (2nd Nyquist zone) mixer, followed by one decimate-by-two fixed filter, to provide a complex output. The complex input bypasses this function. This is programmed during initial register loading. The initial use case for the TCI663xK2L uses complex inputs, so the R2C mixing and decimation filter is not used.

2.10.3.2 RX-Switch

The RX switch is a time-space switch that allows the RX complex stream processing to select any input from the JESD RX stream input. The RX sub-block processes the RX streams in a time-interleaved format. The RX switch stores and then allows selection of any input stream to any switch output channel. The RX switch is configured initially, and can be updated dynamically through an API. The 1, 2, or 4 RX streams are indexed as 0, 0/1, or 0/1/2/3.

Another feature of the RX switch is in applications requiring four RX output streams from two RX input streams. In this case, the RX switch replicates the RX input antenna stream IQ data. Later, in Section 2.10.3.4, the number of RX input and output streams must have the proper number of clocks to support the number of streams. At the RX-switch, one clock per RX output stream is needed at the switch output.

2.10.3.3 RX NCO

The complex streams can be translated in frequency. This mixer frequency translates the IF frequency to zero, for low IF configurations. In zero IF systems, this NCO is set to zero. The NCO is functionally the same as the DDUC NCO (see Section 2.2 for a detailed description). The 1, 2, or 4 Rx streams are indexed as 0, 0/1, or 0/1/2/3.

NOTE: In frequency planning for low IF complex input to RX sub-block, this RX NCO can be used for the frequency translation to zero IF for the RX stream. In frequency planning for real IF, or real inputs to RX sub-block, the RX NCO AND the R2C are used for frequency translation to zero IF for the RX stream.

2.10.3.4 RX Decimating Filter

There are two decimating filters, F1 and F2, which filter and decimate the RX stream signals. All streams must have the same decimation ratio, and all streams have the same RX output IQ rate.

Table 2-23. RX Sub-Block Decimation F1 and F2 Filter Ratios

RX Dec. Filter Ratio	F1 Dec. Ratio	F2 Dec. Ratio (With Recirculation)
1	Bypass	Bypass
2	Bypass	2
4(not used TCI663xK2L)	2	2
8(not used TCI663xK2L)	2	4
16(not used TCI663xK2L)	2	8

These filters provide 80% passband of the available decimated IQ rate. The decimate-by-two filter response is shown in Figure 2-33, The RX sub-block filtering can provide 55 Mhz of passband and 70 db of rejection at 68 Mhz.
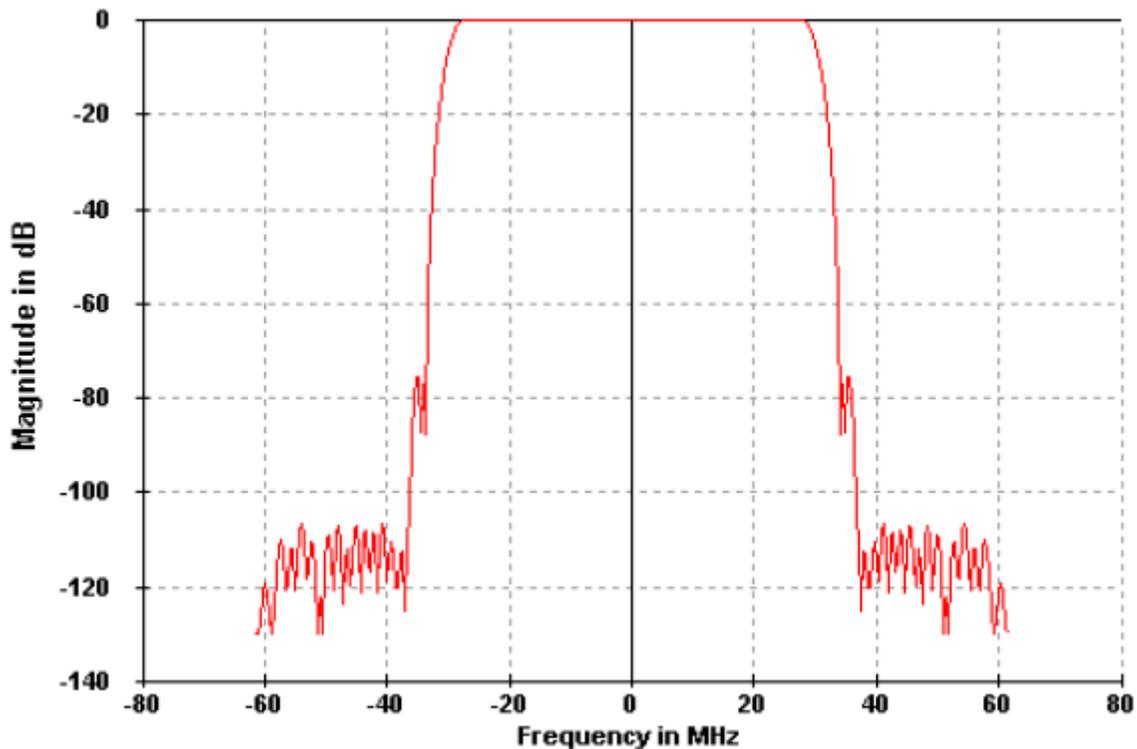
Figure 2-33. Example F2 Filter Decimate-by-Two Response, Sampled at 122.88 Mhz

> **NOTE:** In the TCI663xK2L application table, shown in Section 2.10.3, only the first two decimation filter ratios, 1 and 2, are currently used. If the RX sub-block decimation filter and R2C filters are not used, the RX stream is only filtered by the JESD transceiver. Further channel filtering is provided in the RX DDUC.

The gain of the decimation filters is optimized through the fixed coefficients and scaling, and is nominally 0 db.

2.10.3.5   RX Equalizer

The RX sub-block equalizer is a 16-tap full-complex FIR filter with additional features. The equalizer coefficients are 16 bits. The initial register configuration uses an impulse filter or an RX equalizer bypass configuration. If the hardware is programmed for bypass, the coefficients cannot be utilized while the RX equalizer is operating. There is a programmable power-of-two scaling applied to the complex FIR filter output. The initial configuration is programmed for a unity gain impulse, II[8]=1, QQ[8]=1 and 0 db gain.

The RX sub-block equalizer coefficients can be updated while running, using an API.

The RX sub-block equalizer also has an additional I bias and Q bias DC correction that can be summed with the signal at the block output.

2.10.3.6   RX IQ Imbalance Correction

> **NOTE:** In the current TCI663xK2L implementation, this block is bypassed as the JESD transceiver provides this function.

The RX IQ Imbalance correction provides for complex gain and DC bias correction of a zero IF RX stream input. The hardware has a single-tap blind estimation algorithm that operates autonomously. This block is utilized when a zero IF complex stream is input to the RX sub-block and the JESD transceiver is not providing the complex gain imbalance correction.

This block has unique settings and adaptions for each RX stream. The complex gain can be updated by an API when this block is used, for software-directed IQ imbalance correction. In this case, the software also utilizes the capture buffer of the RX output to aid in determining the complex gain and bias correction values.

2.10.3.7 RX Output Formatter

The RX sub-block output formatter provides a frame signal, and time division multiplexed (TDM) IQ data for the RX sub-block RX stream outputs. The RX sub-block can output 1, 2, or 4 RX streams to the RX DDUCs. See Figure 2-31, and Figure 2-32. Section 2.10.3 lists the output formats by mode. The frame signal identifies the start of the TDM IQ format:

- 1 antenna Frame(I0), (Q0)
- 2 antenna Frame(I0), (Q0), (I1), (Q1)
- 4 antenna Frame(I0), (Q0), (I1), (Q1), (I2), (Q2), (I3), (Q3)

2.10.3.8 RX Power Meter

The RX stream has a multichannel power meter. The power meter is identical to the type discussed in Section 2.1 for the BBTx. The power meter has a synchronization signal (typically DL sync), a predelay count, an integration time (the number of samples to be integrated), and a period to indicate the number of clock cycles before the process repeats. There is an API for power meter setup, and power meter reading.

Figure 2-34 shows the timing sequence for the magnitude squared integrated-power meter. The power meter also captures the signal peak value for the cycles since the meter was last read. The software APIs for reading the integrated power use the number of integrated samples and a TDD on percentage to scale the integrated value.
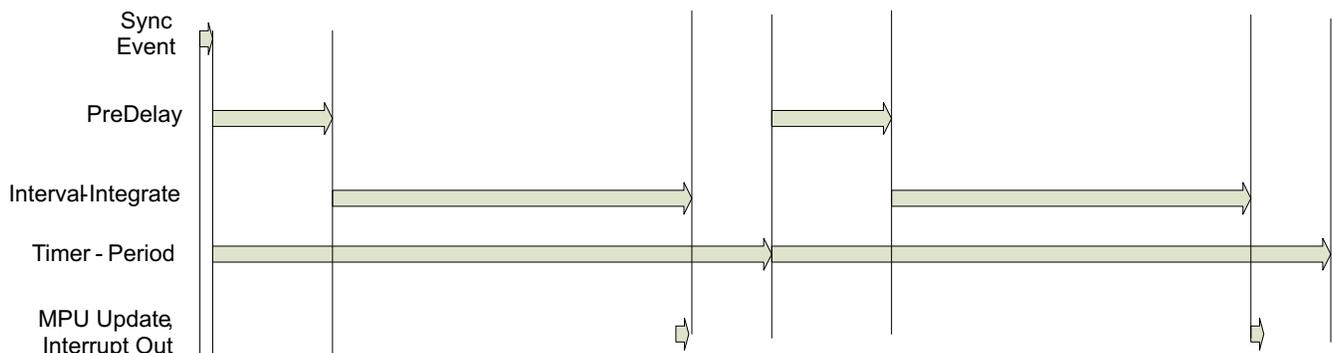
Figure 2-34. RX Sub-Block Power Meter Diagram

2.10.4 RX Sub-Block Synchronization Events

The RX sub-block can be synchronized to one of several sources:
- DownLink sync from DFE-baseband block
- One of two DFE counter timers if used to create a downlink to uplink delay sync
- The MPU software sync for an immediate update

2.10.5 Rx Sub-Block Software Application Interface

> **NOTE:** See Reference 6 (Chapter 3) and for additional details.

API_Rx_switch_select – This API provides a switch control change of the RX JESD stream to RX sub-block stream (normally programmed in linear order 0-1-2-3).

API_Rx_NCO – This API allows the RX sub-block stream to be frequency-translated. There are unique values for each RX sub-block stream.

API_Rx_Equalizer – This API controls the 8-tap complex equalizer and gain-shift for each of the 4 RX antenna streams.

API_Rx_Equalizer_bias – This API controls the bias correction for I and Q after the equalizer, for each of the four RX antenna streams.

2.10.6 RX Sub-Block Important Programming Concepts

> **NOTE:** There are special clock controls required to gate the IQ data transfer from SerDes to JESD sub-block, and JESD to RX sub-block. These are set up in the fixed configurations and are not changed dynamically, so they are not described in the user guide.

The RX block input and the JESD RX output must have compatible configurations.

The RX block real or complex input programming is set to complex for TCI663xK2L and JESD transceiver.

The RX block switch settings 0-3 correspond to the JESD RX block order. This can be adjusted after initial register programming with an API.

The RX block NCO setting should correspond to the low IF complex, or zero IF complex architecture.

The RX block decimation F1-F2 is based on supporting the RX block output rate and the corresponding DDUC RX input rate.

The RX block equalizer gain shift can be used for 16-tap equalization at 0 IF. The RX block equalizer and gain shift adjust the RX stream gain, based on the NCO-tuned, filtered, and decimated RX stream. The initial value is programmed for a unity gain impulse II[8], QQ[8]; normalized gain.

The RX block gain should be set remembering that the RX block power meter is at the RX input, not the filtered and decimated value.

The RX block output mode, 1, 2, or 4 antenna has a corresponding RX DDUC mode; check this for compatibility.

The RX block output to the RX DDUC can only be monitored using the RX output test bus available as an API.

2.11 Feedback Block

The feedback signal path is shown in Figure 2-35. The JESD receives, decodes, and routes the JESD RX inputs between the RX sub-block and the feedback sub-block. The JESD transceiver application currently has one feedback for every two TX antennas. The JESD block outputs up to two feedback signals.
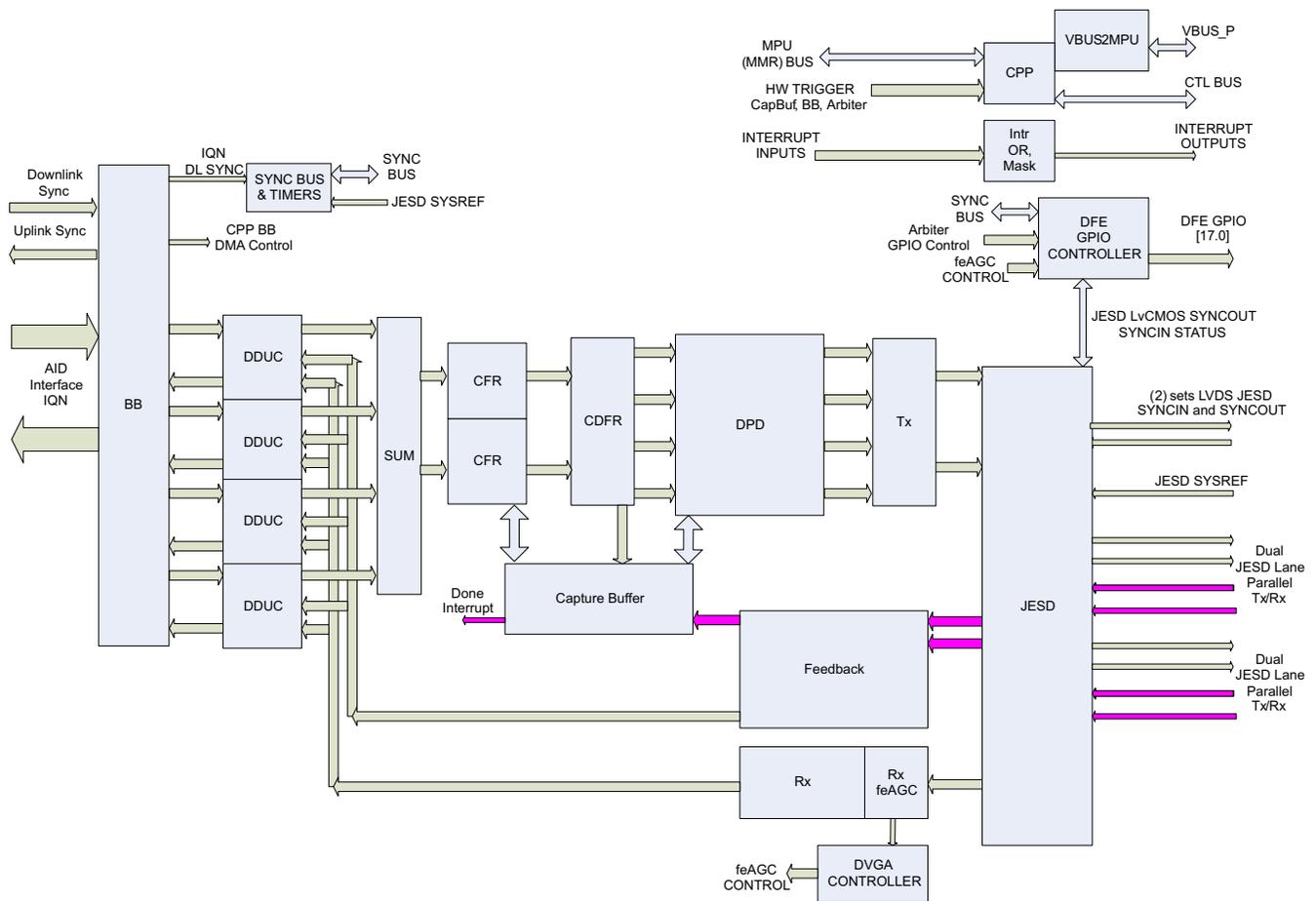
Figure 2-35. DFE Block Diagram for Feedback

The feedback block has two signals paths; one high bandwidth path is used for the DPD captured in the capture buffer (See Figure 2-36), and another decimated output is processed like an RX Stream (see Figure 2-31), discussed in Section 2.10, for network listening mode (NLM).
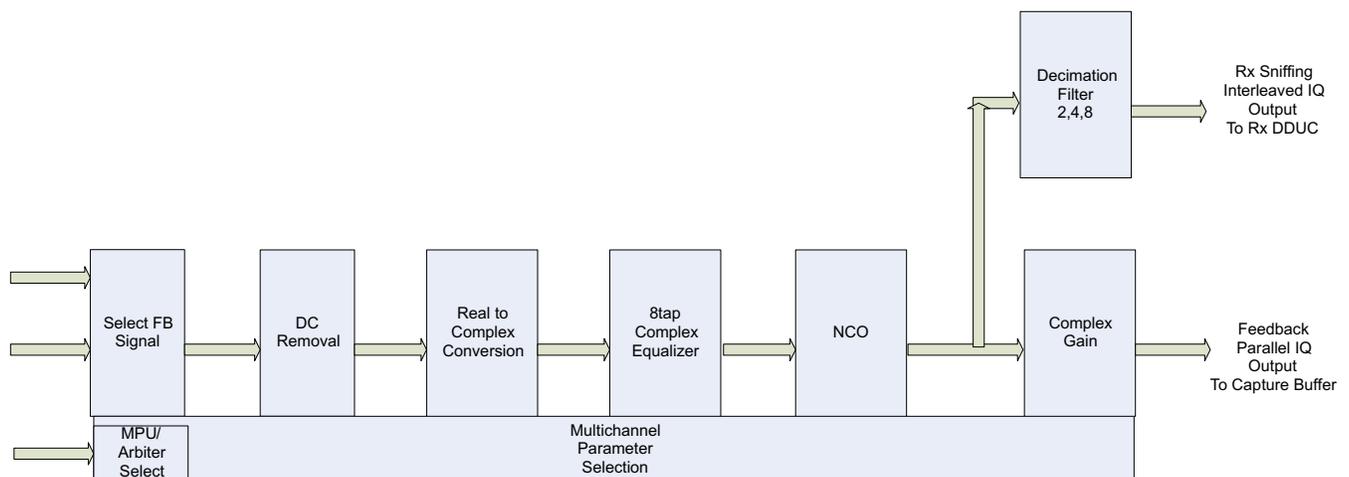

Figure 2-36. Feedback Sub-Block Diagram

2.11.1 Feedback Block Functions

The feedback block in DFE performs the following functions:

- Registers feedback parameter index, selects one of five sets of loaded values and coefficients for current processing.
- Selects one of two JESD feedback signals for processing
- DC removal signal processing block to subtract the mean signal
- Real to complex conversion for a real feedback signal, frequency translation, filtering, and decimation
- Full complex equalization and gain shift, with eight sets of coefficients

> **NOTE:** Equalizer is at the pre-NCO frequency
> - NCO translates low complex IF to zero IF
> - Gain block for the capture buffer output
> - Decimation filter, to filter and decimate the feedback signal to the RX DDUC input rate.

2.11.2 Feedback Block Inputs and Outputs

Table 2-24. Feedback Block Inputs and Outputs

Name	I/O	Basic Description
MPU Bus	Both	Parallel data/ address/ module address synchronous bus for programming registers / memories
JESD Feedback Output buses	I	Two parallel IQ signal buses for the Feedback input from JESD
Feedback output bus to Capture buffer	O	Parallel IQ Feedback output (high BW) to the capture buffer
Feedback output bus to RX DDUC	O	Interleaved IQ bus and Frame signal for the RX DDUC for the network listening stream (like an Rx sub-block output)
Sync Bus	I	A group of signals that indicate the time-event to perform an operation.
Test Bus	Both	Signals to global capture buffer Test Bus data source for capture

2.11.3 Feedback Block Basic Description

Even though the feedback signal processing path has five sets of configuration parameters, there is only one signal pipeline. When the signal source changes, the signal pipeline will have invalid results for a period of time. This period of time when using the capture buffer is the internal DFE feedback latency (DC removal, real to complex conversion, feedback equalizer). The latency for feedback in the network listening mode (RX DDUC output) is longer if the decimation filter has a ratio other than one. See Figure 2-36 for the feedback block diagram.

Indexing feedback parameters – There are five sets of parameters and equalizer taps that can be selected and applied to the five multichannel streams. The feedback select registers select one of the five sets of parameters. The initial register programming does not have the five unique sets of feedback parameters and taps, so a feedback setup API is required to initialize the parameters. Another API indexes the parameters during operation.

Feedback select 1 of 2 – One of the two JESD feedback parallel IQ buses is selected for processing.

DC removal – The DC removal block (not used for the TCI663xK2L) subtracts a mean signal from the selected JESD feedback stream. A low pass-filtered signal has a mean value. The mean value is scaled and subtracted from the I and Q input values. The second filter accumulator can be set with a software controlled bias value.

> **NOTE:** The setup parameters for all streams can be the same, unless manual I-bias and Q-bias are used.

Real-to-complex conversion – The real-to-complex conversion (R2C) is not used in TCI663xK2L. The real-to-complex conversion has an Fas/4, 3Fs/4 selectable frequency translation, and decimate-by-two filter. (See Section 2.10.3.) The feedback real-to-complex conversion is described in the RX sub-block. The setup parameters for all streams can be the same. This block is not used in the TCI663xK2L application, as the JESD transceiver provides a complex feedback stream.

Full-complex equalizer – An eight-tap, full-complex equalizer and gain shift are provided in the feedback sub-block. There are five sets of coefficients: II, QI, IQ, QQ, and sum of taps gain shift. The initial values are programmed for a unity gain impulse II[4]=1, QQ[4]=1; for 0 db gain. The complex equalizer coefficients and gain shift value can be updated while the feedback block is operated using an API.

NCO frequency translation – The NCO frequency translation is based on the JESD transceiver frequency plan and the TX sub-block NCO setting (see Section 2.8.3). The transmit and feedback NCOs should be considered locked in frequency for DPD applications. The NCO is similar to the DDUC NCO in signal processing function. There are frequency (delta phase) and phase offset terms. The NCO phase accumulator has special synchronization for zeroing the phase accumulator, and updating the delta phase computation. The delta phase (frequency translation) and phase offset can be updated during operation using a software API.

Gain adjust for capture buffer input – The signal to the capture buffer can have gain or attenuation based on fractional db resolution. The initial programming is unity gain. The gain can be adjusted for each of the five parameters sets while the gain block is operating with an API.

Decimation filters and output formatting for RX DDUC - The decimation filter performs filtering and decimation to match the RX DDUC input format. The decimation filter is identical in function to the RX sub-block decimation filter (see Section 2.10.3), but the decimation value programmed may be different than the RX block (Table 2-25). The feedback sub-block decimation must be programmed during the intial register setup. Because the JESD transceiver feedback rate can be the same or twice the JESD transceiver RX rate, the decimation filter value must be adjusted for different modes. Table 2-25 shows the desired feedback decimation for different JESD and RX DDUC conditions.

Table 2-25. RX Sub-Block and Feedback Block Decimation for RX DDUC Usage (Continued)

JESD Transceiver Mode	JESD Feedback Rate	JESD RX Rate	Number of RX Antenna Streams	Number of DDUC Channels Rx Out Clock Rate	Rx Dec.	Feedback Dec.
1	DFEPLL	DFEPLL/2	2	<=6 DFEPLL/4	2	4
1	DFEPLL	DFEPLL/2	2 or 4 with replication	4(spec),8,12 DFEPLL/8	4	8
3b	DFEPLL/2	DFEPLL/4	2	<=6 DFEPLL/4	1	2
3b	DFEPLL/2	DFEPLL/4	2 or 4 with replication	4(spec),8,12 DFEPLL/8	2	4
3b,3b	DFEPLL/2	DFEPLL/4	4 antenna stream	4(spec),8,12 DFEPLL/8	2	4
6b	DFEPLL/4	DFEPLL/4	2	<=6 DFEPLL/4	1	1
6b	DFEPLL/4	DFEPLL/4	2	4(spec),8,12 DFEPLL/8	2	2

The feedback sub-block output formatter provides a frame signal, and interleaved IQ data for the RX DDUCs. The feedback output format must conform to the 1, 2, or 4 antenna TDM-interleaved IQ discussed in Section 2.10.3. However, the feedback block only utilizes the first IQ carrier time slot. The frame signal identifies the start of the IQ frame:

• 1 antenna Frame(I0), (Q0) (every 2 DFEPLL clocks)

• 2 antenna Frame(I0), (Q0) (every 4 DFEPLL clocks)

• 4 antenna Frame(I0), (Q0) (every 8 DFEPLL clocks)

2.11.4 Feedback Block Synchronization Events

The feedback block can be synchronized to one of several sources:
- DownLink sync from DFE-baseband block
- One of two DFE counter timers if used to create a downlink delay sync
- The MPU software sync for an immediate update

2.11.5 Feedback Block Software Application Interface

> **NOTE:** See Reference 6 (Chapter 3) and for additional details.

> **NOTE:** The feedback block has five sets of configurations elements; the below description is based on individual setup functions with an index.

API_Fdbk_index_select – This API selects the one of five sets of parameters for the feedback programming.

API_Fdbk_JESD_select(0-1) – This API updates the one of two JESD selections for the one of five programming sets of registers.

API_Fdbk_Equalizer – This API updates the equalizer coefficients for the one of five programming set of registers.

API_Fdbk_IQBias – This API updates the I and Q bias for the one of five programming sets of registers.

API_Fdbk_NCO – This API updates the frequency translation for the one of five programming sets of registers.

API_Fdbk_Gain – This API updates the capture buffer gain for the one of five programming sets of registers.

2.11.6 Feedback Block Important Programming Concepts

The feedback block has several sub-blocks with configurable signal-processing parameters. The five indexed sets of parameters must be initialized before use.

The decimation table used for network listening and DDUC modes is loaded statically with the register programming. There is no API to change this decimation dynamically.

There can be up to two JESD feedback inputs for selection. In a two-antenna mode, there is one feedback input. In four-antenna mode, or for special processing, there is more than one feedback JESD input.

The NCO value programmed needs to compensate for low IF or zero IF for feedback for the TX path. In network listening mode, the NCO also has additional tuning requirements. The NCO value is stored in the indexed parameters during selection, or updated by API.

The feedback equalizer precedes the NCO in the signal processing chain. The design of the equalizer coefficients must be applied at the IF or NLM frequency.

The feedback gain for capture buffer usage is done in the feedback equalizer coefficients and scaling, or the gain block. The feedback gain in network listening mode can only be done in the feedback equalizer coefficients and scaling.

2.12 Capture Buffer Sub-Block
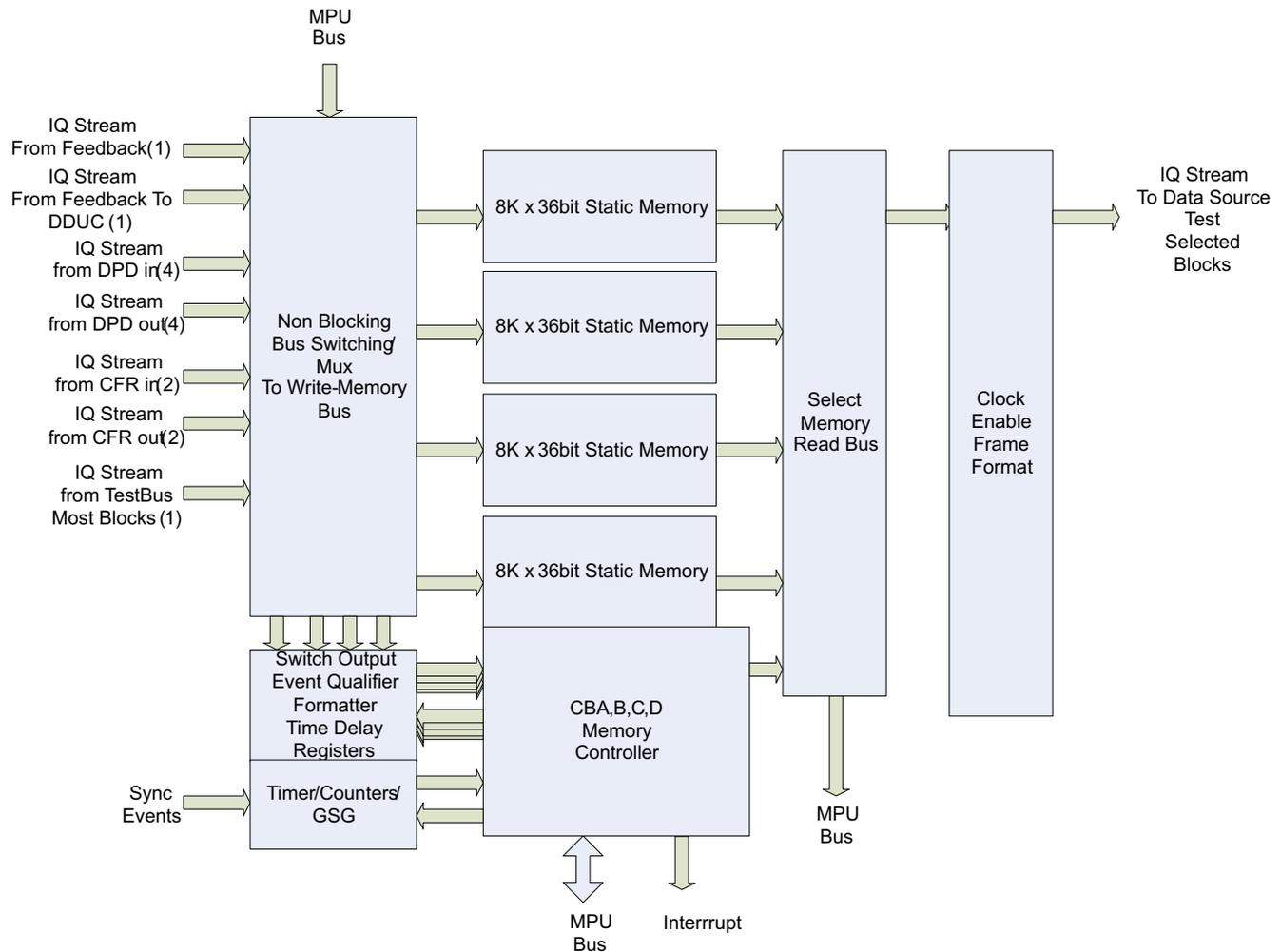
Figure 2-37. Capture Buffer Block Diagram

2.12.1 *Capture Buffer Block Functions*

The capture buffer block is primarily used for signal collection. The signal collection can occur from the fixed buses, or from a variety of special collection points in the test bus.

The capture buffer can be used in special conditions to source data to the CFR input or DPD input fixed nodes.

The capture buffer can be triggered to start looking for an event, or to count a delay and collect a specific amount of data. The MPU bus control register starts the sequence for the data collection, and the capture event is based on a multipurpose trigger block. The count delay is based on a sync bus event or MPU start.

The capture buffer collection can be several nodes at a common time, with certain programming restrictions. The capture buffer collection is a circular buffer, so that when initialized, information collecting is started. Information collecting stops after the trigger condition occurs and the appropriate number of samples have been collected. The trigger conditions are based on a number of samples > threshold. There are two different threshold levels, number of threshold event counters, and number of sample counters. Once armed, the capture buffer is continuously collecting for the designated (there are 1, 2, or 4 capture buffers controlled) buffers. After the delay counter, the size of the capture buffer controls when to stop collecting data.

The capture buffer has both a 32-bit and 64-bit memory access depending on the address used. See the register map for the capture buffer, and the software API details for reading and writing the capture buffer.

2.12.2 Capture Buffer Block Inputs and Outputs

Table 2-26. Capture Buffer Inputs and Outputs

Name	I/O	Basic Description
MPU Bus	Both	Parallel data/ address/ module address synchronous bus for programming registers / memories
IQ stream from Feedback input	I	Output of Feedback before decimation filter, parallel IQ with frame
IQ stream from Feedback output	I	Output of Feedback for Network Listening Mode to Rx-DDUC, interleaved IQ with Frame
IQ stream from CFR input	I	PreCFR signal after antenna combining, TDM IQ for 1 or 2 antennas, after sumchain and format conversion (1 of 2)
IQ stream from CFR output	I	PostCFR signal TDM IQ for 1 or 2 antennas (1 of 2)
IQ stream to CFR input	O	The two inputs to the CFR sub-blocks can be sourced from the capture buffer.
IQ stream to DPD input	I	The CDFR output to the DPD block is collected in parallel IQ format, (1 of 4)
IQ stream from DPD output	I	The DPD output from the DPD block is collected in parallel IQ format, (1 of 4)
IQ stream to DPD input	O	The two inputs to the CFR sub-blocks can be sourced from the capture buffer.
Test Bus	Both	Signals to global capture buffer Test Bus data source for capture
Sync Bus	I	A group of signals that indicate the time-event to perform an operation.
Interrupt Bus	O	Signals to MISC module to indicate a capture buffer is finished
CaptureComplete to CPP	O	Signals to CPP module to indicate a capture buffer is finished

2.12.3 Capture Buffer Block Basic Description

The capture buffer can operate with the four 8K memories operated as individual capture memories, in pairs of memories (16K), or as a single 32K memory (see Figure 2-37). Normally, the capture buffer collects data from the IQ fixed buses or the test bus; however, with special programming the capture buffer can be used for testing to source data to a specific node. In the test environment, two capture buffers can be data sources, while two capture buffers can be data sinks.

The number of capture buffer memories is based on different software operations:

(a) During the DPD time alignment functions, the DPD output and feedback input nodes are monitored. The setup parameters have a delay from start for DPD output. The software adjusts the delay from start for the feedback input to get the aligned time samples. This process uses two capture buffers of 8K samples, or all capture buffers for two captures of 16K samples.

(b) During the DPD adaption functions, the input to DPD and the feedback after equalization, tuning, and gain are monitored. The time alignment delay above (a), and fixed known delays of the internal data path delay the feedback-processed output to the DPD input. This process uses two capture buffers of 8K samples, or all capture buffers for two captures of 16K samples.

The capture buffer has a specific format programmed with a software API for CB_Setup. The different signal buses can be operated with a frame (start of IQ data), valid (this clock cycle has valid data for capture), and IQ data. Typically the top 16 of 18 bits of the 18-bit databus for I and Q, the frame, and the valid signal are captured. The capture buffer setup parameters are:

• Capture buffer mode – The capture buffer can collect data in delay-start or smart mode. The capture buffer can also source data under certain conditions. The capture buffer mode must be in MPU mode to access the memory from the MPU bus.

• Capture buffer bus select – A fixed bus or the test bus is mapped to this capture buffer (1 of 4). The I memory and Q memory of each capture buffer can be selected to the same bus for interleaved IQ bus type, or each half can be selected to the upper or lower fixed bus selection for parallel IQ bus types.

• Capture buffer frame, and valid – The buses have timing synchronization signals used with the capture

buffer logic. The frame-start identifies the start of a time-interleaved IQ bus cycle. The valid identifies a valid data signal in cases where clock gating is used. These can be programmed to select all samples, and the software can decode the captured frame and valid bits. The fsf is a frame-strobe-format bit field, the fsfm is a frame-strobe-format-and-data-mask field.

- Idelay, Qdelay – The signal buses can be parallel IQ, TDM parallel IQ, interleaved IQ, and TDM-interleaved IQ formats. Using the frame and valid bit controls above, once the valid frame is located, counters internal to each capture buffer capture the specific I or Q, or IQ sample. When the TDM or interleaved bus formats are input to the capture buffer, the Idelay and Qdelay select the specific data in the frame to collect.

- Cb_delay – Number of capture buffer clocks, after a Cb_start synchronization event where the capture will stop, in fixed capture mode.

- Cb_trigger_conditions – There are threshold comparators and count event integrators for each capture buffer. Each of two thresholds can be selected for magnitude squared, or magnitude. In the smart-trigger of the capture buffer, typically setpoint 2 is for peak event monitoring and setpoint 1 for power event monitoring. When the capture buffer has been started, the integrators are zeroed; after the cb_delay, if the trigger condition is met, the capture buffer is stopped.

The capture buffer uses the concept of pre-triggering. In this case, the capture buffer collects data until a synchronization event and the delay has occurred. The CB logic has an end counter which indicates the address where the CB stopped collecting. The software uses this address, and the number of CB sections to correctly orient the CB data for analysis.

In normal operation, the user has a API_CBSetup, response to CB Interrupt, or loop timeout, and an API_CBRead. The static delay capture buffer operation is illustrated in Figure 2-39.
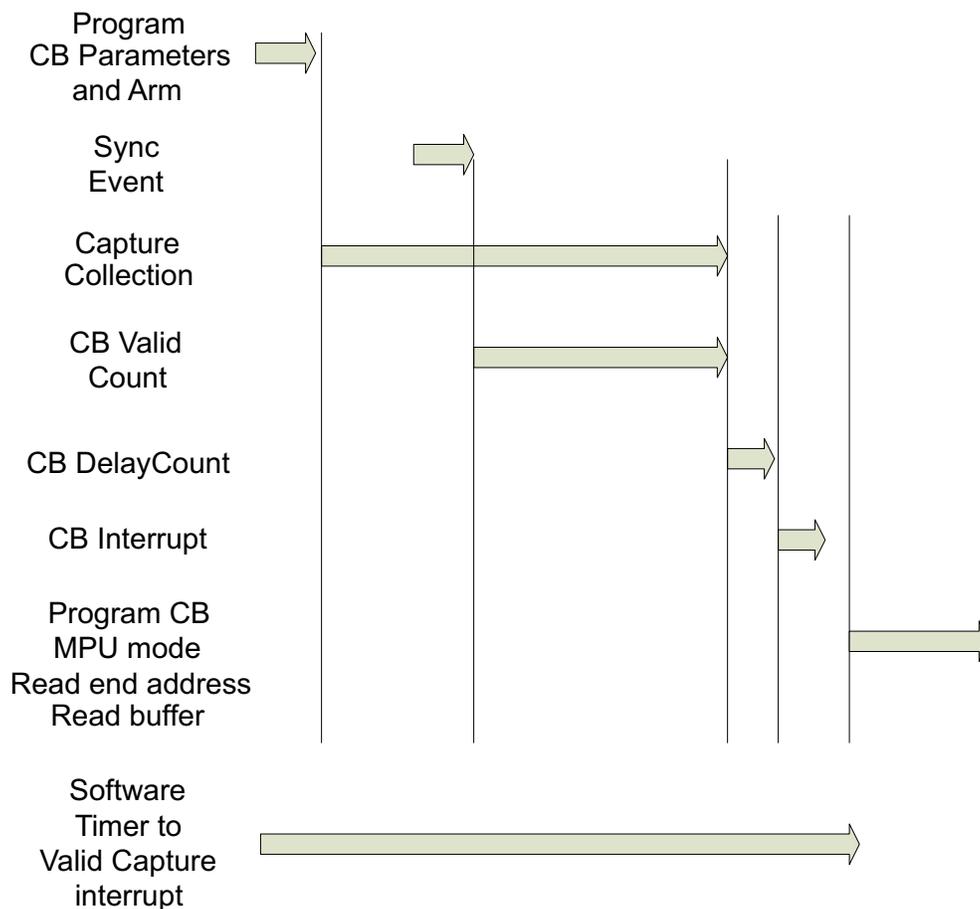
Figure 2-38. Capture Buffer Static Collection with Delay

The smart capture is different from the static collection in that if the cb trigger conditions do not occur, the smart capture does not complete. Typically, the software has a secondary loop counter to check if the capture has not completed (to indicate the capture parameters were not met). Figure 2-39 shows a valid capture found, and the CB interrupt occurs.
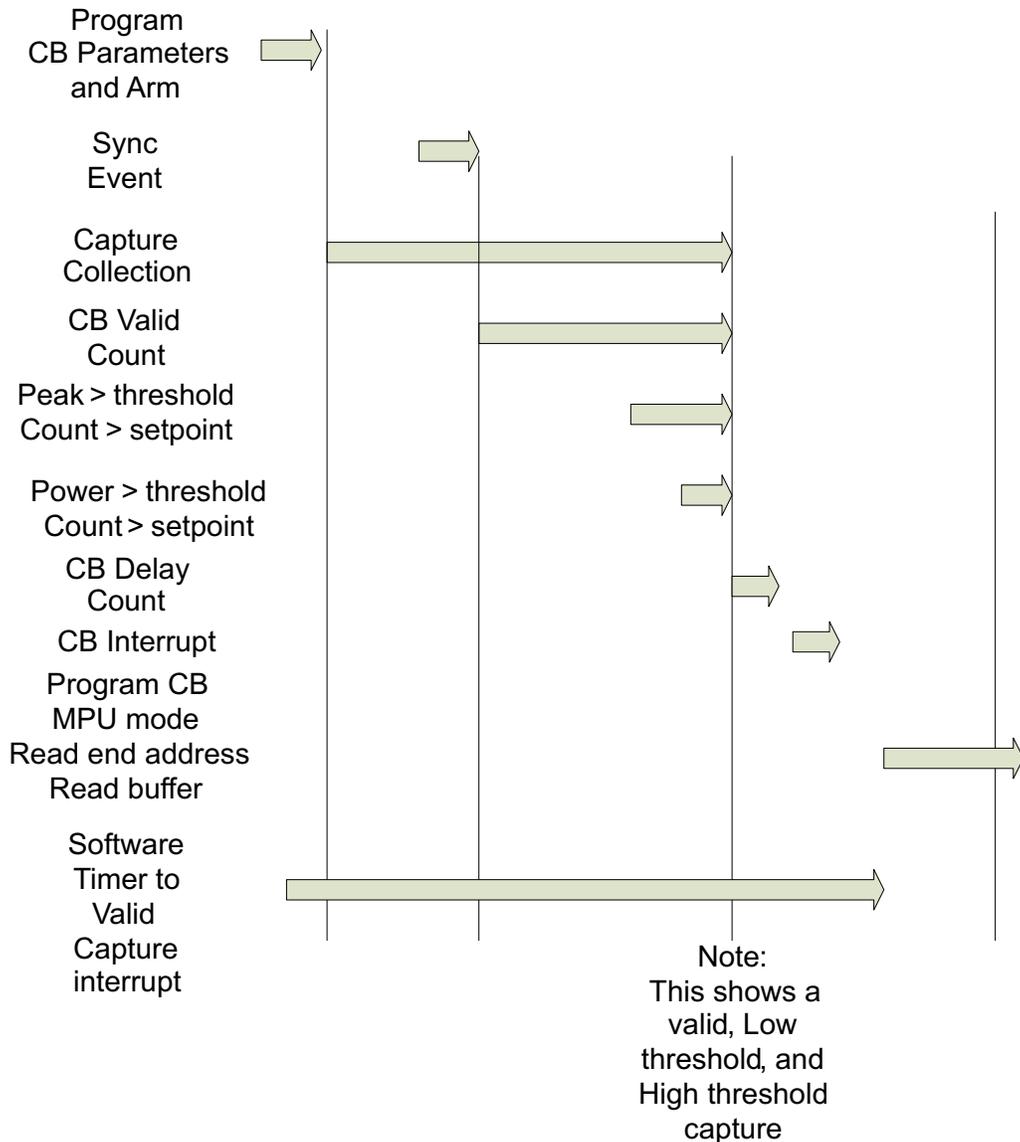
Figure 2-39. Capture Buffer Qualified Collection with Delay

2.12.4 *Capture Buffer Block Synchronization Events*

The capture buffer block can be synchronized to one of several sources:

- DownLink sync from DFE-baseband block
- One of two DFE counter timers if used to create a downlink delay sync
- The MPU software sync for an immediate update

2.12.5 *Capture Buffer Block Software Application Interface*

> **NOTE:** See Reference 6 (Chapter 3) and for additional details.

The capture buffer has both a software API, a response to interrupt, and a software timer to detect if a capture buffer interrupt should have occurred.

API_CB_Setup – This API controls the setup of a section or all of the capture buffer. Depending on the parameters described above and in the API document, the amount of data captured can be 8K, 16K, or 32K for 4, 2, or 1 selected nodes. When multiple capture buffers are synchronized, the synchronization source must be applied after all sections of the capture buffer setup are done.

API_CB_Arm – This is shown as a separate API but may be part of CB_Setup. When the capture buffer is capturing data, this API looks for the trigger to stop collecting the data and sends a capture buffer interrupt.

CB_Response to Interrupt – The software has a timer indicating an expected CB interrupt. If the timer times out before the CB interrupt is received, the CB process did not collect data. If the interrupt occurred and the timer is still running, this is a valid CB process and the user continues to get the CB data.

API_CB_Read – This API controls the setup after collection of the capture buffer. Depending on the CB_Setup parameters, the CB_Read may need to be done in several sections to concantenate the buffers collected into a larger structure of data. The CB_Read sets the CB into MPU mode for the desired capture buffer sections, to allow collection of the data and end address.

API_CB_Write – This API writes data into the capture buffer memory for data sourcing mode. It is used in diagnostic testing, not for normal TCI663xK2L operations.

2.12.6 Capture Buffer Block Important Programming Concepts

The capture buffer has four sections. In some cases, the user may want to combine the sections to make a larger 16K or 32K capture, by selecting the same input node and adjusting the cb_delay to collect 8K samples in one CB section, and more in other sections.

When the CB is used with multiple sections, program both sections' register functions, and then arm over a short period of time.

Some cases for the test bus indicate that the capture buffer parameters may need some experimentation to get the desired results. The test bus does not have the same formats as the other fixed buses. The capture buffer use for the test bus can capture the 18 databits, or can capture the top 16 bits and the flag and valid status.

The smart capture mode, used with a low-power threshold and > 80% of the samples greater than this threshold, can be used as a power enable.

In the smart capture mode, the capture buffer may not be collected. In the static capture mode, a capture buffer is always collected.

There are signal-processing magnitude-squared mean power and peak signal within a capture buffer that can be used for signal monitoring.

TI recommends using the API setup for the DPD alignment and DPD adaption process.

The capture buffer has both a 32-bit and 64-bit memory access, depending on the address used. See the register map for the capture buffer, and the software API details for reading and writing the capture buffer.
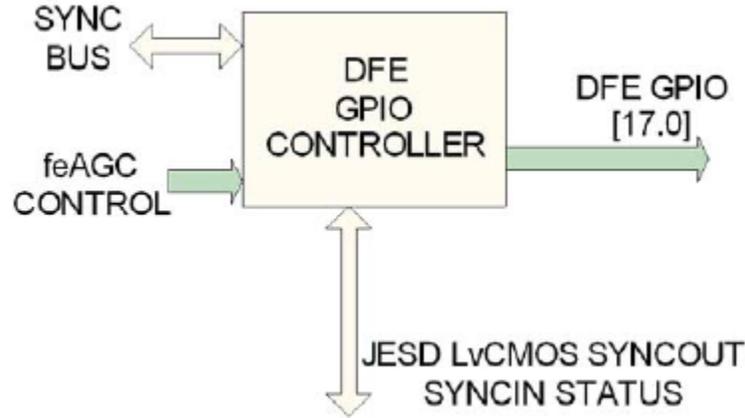
2.13   MISC (CPP, GPIO) Block

Figure 2-40. DFE GPIO Block Diagram

2.13.1   MISC GPIO Block Functions

The DFE GPIO controller provides for multifunction 1.8v CMOS control and status signals. The 18 DFE GPIO pins can be software-controlled or multiplexed to specific DFE hardware signals (see Table 2-28).

2.13.2   MISC GPIO Block Inputs and Outputs

Table 2-27. MISC GPIO Inputs and Outputs

Name	I/O	Basic Description
feAGC Control	I	DVGA controller sets of bits, for RX feAGC (function not used on TCI663xK2L)
MPU Bus	Both	GPIO read and write control for DFE GPIO
JESD LvCMOS SYNCIN, SYNCOUT (2 sets)	Both	Signals to/from JESD module for SYNCIN and SYNCOUT functions with 1.8v CMOS JESD Sync controls
JESD SYSREFREQ	O	Signal from JESD module for requesting SYSREF clock solution function to 1.8v GPIO output
DFE GPIO	Both	Bidirectional 1.8v LvCMOS signals for DFE, can also be TCI663xK2L GPIO, or other functions

2.13.3   MISC GPIO Block Basic Description

The DFE GPIO uses bidirectional muxed signals (they can be overridden outside of DFE based on TCI663xK2L SoC programming). Each DFE GPIO pin has a unique 5-bit mux field in the MISC register map, and unique 1-bit write bit (*):

Table 2-28. GPIO Mux Controls

Value	Usage
0,5,6,7	Input
1	GPIO _sync_in[0], input to SyncBus external input0
2	GPIO _sync_in[1], input to SyncBus external input1
3	JESD_SYNCIn[0] – affects JESD sub-block, input link0
4	JESD_SYNCIn[1] – affects JESD sub-block, input link1
8	GPIO _sync_out[0] – SyncBus sync0 to output
9	GPIO _sync_out[1] – SyncBus sync1 to output
10	JESD_SYNCOut[0] – from JESD sub-block, output link0

Table 2-28. GPIO Mux Controls (continued)

Value	Usage
11	JESD_SYNCOut[1] – from JESD sub-block, output link1
17:12	Arbiter(not used for TCI663xK2L) control fb_mux_cntl[5:0] output
25:18	DVGA Controller-Rx sub-block DVGACntl[7:0]
26	SYSREFREQ – from JESD sub-block output
27	MPU GPIO drive – see MISC register map for each DFE GPIO bit (*)
31:28	Output zero

The GPIO mux can be initialized in the DFE initial registers. There is no planned API to write or read the registers. In the MISC registers, there are bit fields to read the value for inputs. When these GPIO are used for control inputs, other DFE sub-block programming may need to change from other LVDS program signals (such as JESD SYNCIN0,1).

> **NOTE:** When the GPIO address is read back over the MPU access, the value written to an output or read from an input is returned.

2.13.4 MISC GPIO Block Synchronization Events

The GPIO can input or output signals, but does not normally synchronize. The DFE_GPIO can input an external sync signal and drive this to the sync bus (see Section 2.2.4).

2.13.5 MISC GPIO Block Software Application Interface

> **NOTE:** See Reference 6 (Chapter 3) and for additional details.

2.13.6 MISC GPIO Block Important Programming Concepts

The GPIO currently does not have an API. The register map in the MISC section (see) has a direct register multiplexer and bit write function.

The GPIO can be repurposed outside of DFE to a TCI663xK2L GPIO, check Reference 4 (Chapter 3) for SoC GPIO versus DFE GPIO selection.

If the GPIO are used instead of the LVDS sync signals for JESD or other features, this requires programming in the miscellaneous GPIO and the other DFE sections.
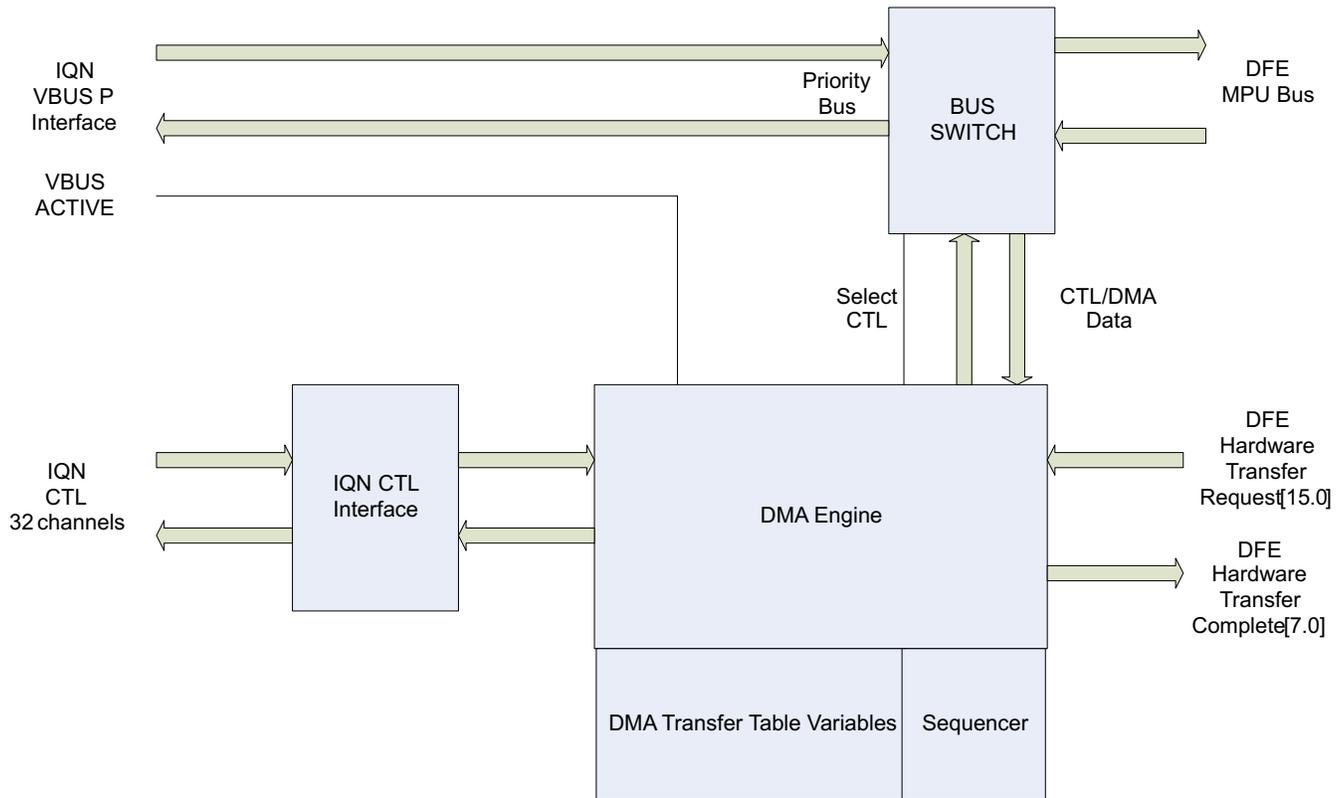
2.14 MISC CPP Block

Figure 2-41. VBUSP2MPU CPP Sub-Block Diagram

2.14.1 MISC CPP Block Functions

The CTL DMA bus can be utilized for the MPU bus when the VBusP is not accessing the bus.

The CPP sub-block can provide a local DMA control for at least 16 events in the DFE to support data forwarding to the CTL and MPU bus. The CPP sub-block allows for DMA structures of start MPU addresses, and number of transfers to implement the DMA structure on the DFE MPU bus.

The CTL and CPP can DMA access any addresses in the entire DFE. The DMA can have multiple blocks to chain accesses to multiple DFE address sections.

2.14.2 MISC CPP Block Inputs and Outputs

Table 2-29. MISC CPP Inputs and Outputs

Name	I/O	Basic Description
VBusP	Both	32-bit blocking mpu-bus, programmation bus from/to IQNet
MPU Bus	Both	DFE programmation and DMA bus (not baseband data)
CTL Bus	Both	DMA transfer bus non- blocking to/from IQNet
Sync Bus	I	A group of signals that indicate the time-event to perform an operation.
Event Trigger Bus	I	12 signals from DFE logic that can initiate the DMA-CTL transfer
Event Complete Bus	O	Eight signals to DFE indicating the DMA transfer is complete
Interrupt Bus	O	Signals to MISC module to indicate bad DMA transaction occurred

2.14.3 MISC CPP Block Basic Description

The VBUSP2 MPU arbitrates MPU access from VBusP and internal DMA. VBusP has priority.

The CPP DMA has two modes of operation: fixed and embedded.

The fixed mode has programming information for the descriptor, starting address, destination address, and number of data transfers. In the fixed mode, there are 16 DMA events. The events can be single DMA, or can be chained to multiple operations (where the end of the first event points to the start of the second event).

The embedded mode, which is writing data to DFE from IQNet, has an embedded destination address and number of transfers. This mode does not require setup; the logic automatically decodes the destination and number of transfers.

The fixed DMA modes are numbered from the highest priority 0 to the lowest 15. The DMA events are triggered by specific synchronization signals:

- Sync bus – All 16 sync bus signals can be used to trigger a DMA event
- CTL channel – CTL event can trigger a DMA
- Hardware triggers 12 signals, from DFE events

2.14.4 MISC CPP Block Synchronization Events

The CPP synchronization events are discussed in Section 2.14.3. The standard sync bus, DL sync, MPU sync, and additional CTL events and internal hardware events trigger CPP DMA events. The DMA event number is selected by the specific hardware trigger or software-triggered event.

2.14.5 MISC (CPP) Block Software Application Interface

> **NOTE:** See Reference 6 (Chapter 3) and for additional details.

The initial register programmation for DFE does not include preprogrammed CPP DMA setup.

The RFSDK software after initialization can program the CPP DMA channel, source address, destination address, and number of transfers.

2.14.6 MISC (CPP) Block Important Programming Concepts

See Reference 6 (Chapter 3) for further discussion of CPP DMA channel setup. Typical uses are:

- Capture buffer DFE -> memory
- (WCDMA only) BBRx channel power meter

2.15 Sync Bus and Sync Counter

2.15.1 Sync Bus Functions

The sync bus is a signal bus used to communicate signal events within the DFE blocks. The ssel selection for sub-blocks connects the sync for that sub-block functions with the signal in the following list. There are two dl (TX from IQNet), and two ul (delayed TX from IQNet to BB counter) syncs for dual mode access (two different IQ signal groups in one configuration). See Table 2-30.

2.15.2 Sync Bus Input and Outputs

Table 2-30. Sync Bus

ssel Value	Basic Description
0: never sync	Normal ssel setting for no resynchronization
1: mpu_sync	Manual MPU cycle sync (used for software sync)
2:ul_iq0_frame_strobe_sync0	BBRx axc group0 sync
3:ul_iq0_frame_strobe_sync1	BBRx axc group1 sync
4: dl_iq0_frame_start_sync0	BBTx axc group0 sync (used to resync blocks to Tx frame)
5: dl_iq0_frame_start_sync1	BBTx axc group1 sync
6: gpio_sync_in0	DFE GPIO pin is an input and muxed to this bus '0>1' is a sync
7: gpio_sync_in1	DFE GPIO pin is an input and muxed to this bus '0>1' is a sync
8: jesd_sync_in0	JESD SYNCIN 0 – JESD Transceiver is ready to release from sync, or has errors
9: jesd_sync_in1	JESD SYNCIN 1 – JESD Transceiver is ready to release from sync, or has errors
10: master_intr0	Internal interrupts mapped in DFE sub-blocks to MISC have an interrupt
11: master_intr1	Internal interrupts mapped in DFE sub-blocks to MISC have an interrupt
12: sync generator counter 0	See below section syncgen_counter output 0
13: sync generator counter 1	See below section syncgen_counter output 1
14: sync generator counter 2	See below section syncgen_counter output 2
15: always sync	Used to force sync to on, used to continuously set registers, override accumulators – can be a normal initialization sync value

> **NOTE:** The counter timer inputs are usually selected from the sync bus. The counter timer outputs can drive the sync bus, or can be selected in DFE GPIO multiplexers to output timers 0 and 1 to DRGE GPIO pins.

2.15.3 Basic Description

The sync bus is a signaling bus within DFE. The DL_IQ0 syncs come from IQNet and synchronize to the downlink start signal. The MPU_Sync is also important, in that a software-triggered event can cause a sync event.

There are three sync counters within the DFE. The counters are named syncgen_cntr[0,1,and 2].

The sync counters are programmed to start from a sync bus event, through the ssel register programming. The sync counter outputs can be events on the sync bus, or routed to specific DFE GPIO controls. The sync counters count the DFE PLL clock.

The sync counter has an ssel selection for starting the counter based on a sync bus event. Once the event occurs, the counter delays and outputs the invert control bit level for 'delay' number of clocks. After the delay count, the output changes to the inverse of the invert control for 'pulse' number of clocks. The repeat control and the period counter can repeat the timed event. Depending on the ssel sync input, the process can repeat on another sync event. The sync counters are in the MISC register map section.
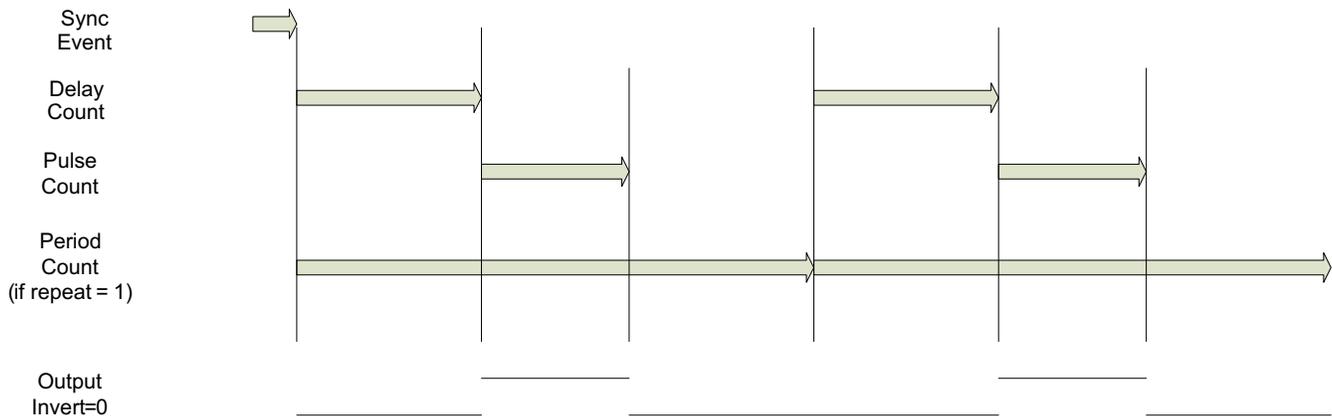
Figure 2-42. Sync Counter Operation

2.15.4 Synchronization Events

The internal counter timers can be synchronized or free-running. See Section 2.13 for sync bus synchronization sources.

2.15.5 Software API

There are currently no APIs for the sync counters. Sync counter 0 is currently used for the initialization function in software, and can be re-used after initialization.

2.15.6 Important Programming Considerations

The counter timers normally need to be synchronized initially. After the initial synchronization it is important to consider the repeat cycle and timer period. If the initial synchronization occurs before the timer period completes, the timer starts over.

The counter timers can drive signals to the sync bus, so that multiple counter timers can be chained together for sequences.

Counter timer 0 is used during DFE initialization. Any value programmed into the register programmation will be overwritten by the initialization software.

Counter timer 0 and counter timer 1 can have pulse outputs that for use on the DFE GPIO pins.

2.16 2-Level Interrupt Description

2.16.1 Interrupt Function

The different DFE interrupt status bits are generated in the DFE sub-blocks. There are approximately 180 status elements. Each sub-block sends the status to an interrupt logic module, which has mask, hold, clear, and force-on functions.

2.16.2 Interrupt Inputs and Outputs

> **NOTE:** This section is found in under the MMR registers with "interrupt" in the description

2.16.3 Basic Description

The hold and clear functions are provided in each DFE sub-block. The interrupt force ON and register status are provided in the MISC interrupt registers.

The two interrupt signals go from the MISC sub-block to IQNet as a critical DFE interrupt, and a non-critical DFE interrupt.

The software responder to the DFE interrupts must poll the MISC registers to determine which interrupts are active and have a service routine to report, clear, and change operational state.

The selection of critical and non-critical interrupts is covered in the RFSDK.

2.16.4 Synchronization

There is no special synchronization for the interrupts.

2.16.5 API Interface

There are no special APIs for the Interrupts.

2.16.6 Special Programming Concerns

There are no APIs currently for the interrupt control registers.

References

1. JESD204B Specification; JESD204B.01 January 2012, www.jedec.org
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3. TI KeyStone II Architecture SerDes User Guide, (SPRUHO3)
4. TI TCI6630K2L SoC Data manual, (SPRS893)
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7. TI TCI663xK2L DFE Configuration summary, and fixed programmation files

Revision History

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