DM38x and TMS320DM8127 DaVinci™ Digital Media Processor Face Detect

User's Guide

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About This Manual

This document describes the operation of the Face Detect in the DM38x and TMS320DM8127 DaVinci™ Digital Media Processor.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers may be shown with the suffix h or the prefix 0x. For example, the following number is 40 hexadecimal (decimal 64): 40h or 0x40
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties with default reset value below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure can have one of multiple meanings:
    - Not implemented on the device
    - Reserved for future device expansion
    - Reserved for TI testing
    - Reserved configurations of the device that are not supported
  - Writing non-default values to the Reserved bits could cause unexpected behavior and should be avoided.

Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

Related Documentation From Texas Instruments

For product information, visit the Texas Instruments website at http://www.ti.com.

SPRS821 — DM385 and DM388 DaVinci™ Digital Media Processor

SPRS712 — TMS320DM8127 DaVinci™ Video Processor

Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community— *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki— *Texas Instruments Embedded Processors Wiki.* Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

Face Detect

1 Face Detect

1.1 Overview

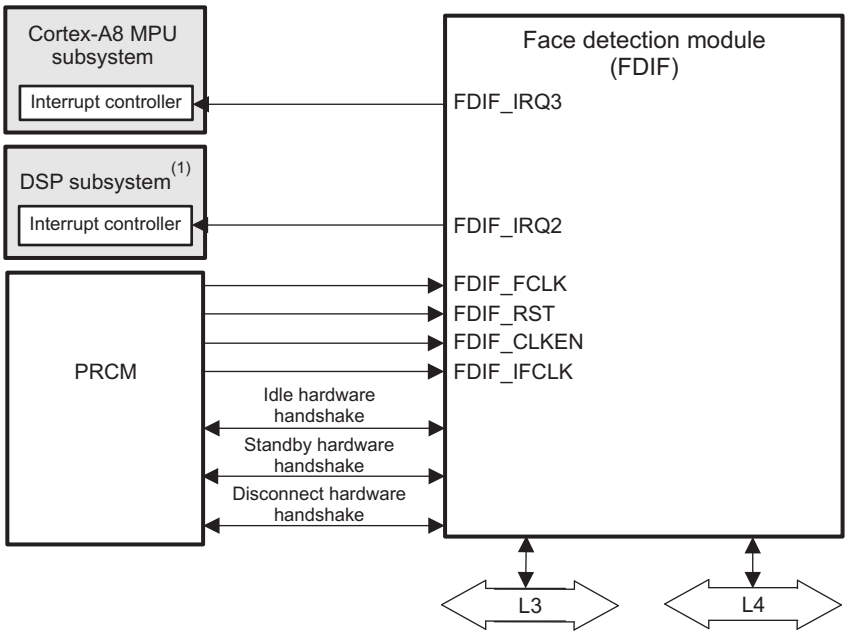
The FDIF module performs face detection within a picture stored in memory (QVGA luminance data resolution). This module is typically used for video encoding and face-based priority auto-focusing.

The face detect (FD) core is a standalone module: it embeds its own direct memory access (DMA) engine for accessing data in memory. The FD core is under microprocessor unit (MPU) control for its initialization and to start the processing operation.

The FD core supports single input resolution (QVGA) in a single format (8-bit luma). The FD core requires the input image to be stored in synchronous dynamic random access memory (SDRAM). The core also requires working memory mapped in SDRAM. The input image data (320x240) requires 75KB for the SDRAM and 51.25KB for the working memory.

Figure 1 is an overview of the FDIF. Three interrupt lines go to the three central processing units (CPUs) to allow control of the FD core module by different processors, but only one interrupt at a time can be active. The three interrupt lines provide flexibility for controlling the module.

Figure 1. Face Detect Highlight



(1) DSP subsystem available only on DM8127.

1.2 Main Features

The FDIF has the following features:

- Two interconnects interface:
  - 32-bit-wide level 4 (L4) interface for register configuration
  - 32-bit-wide level 3 (L3) interface for command
- Supports the IDLE, STANDBY, and DISCONNECT protocols
- Third party IP features: For information about the input image features and detection capabilities, see Table 1.

Table 1. Third Party IP Features

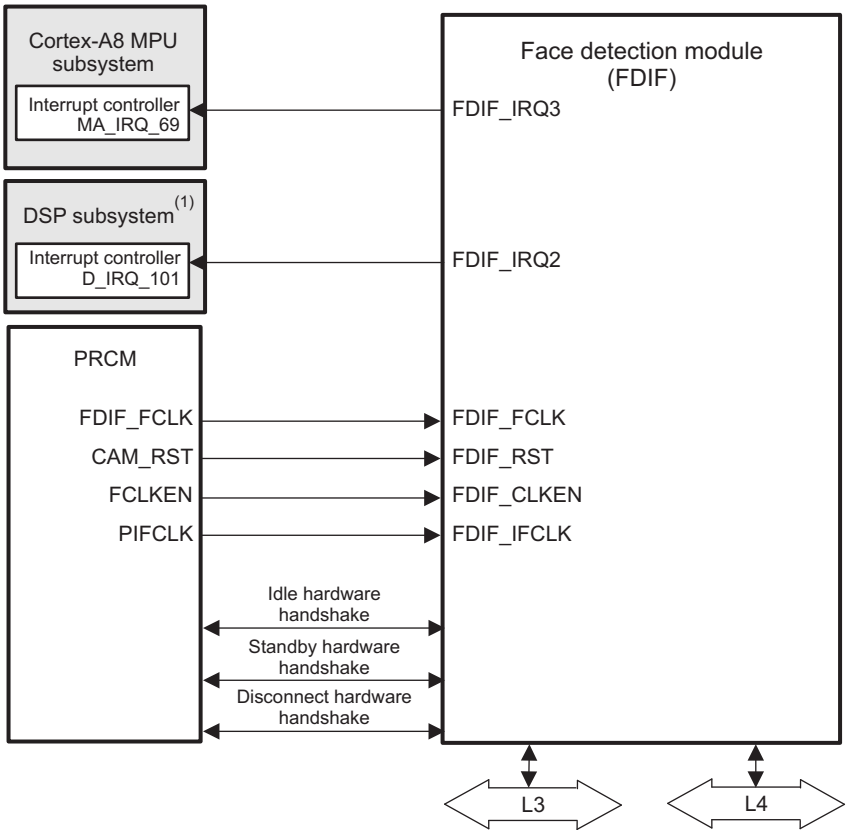
Items	Description
Input image size	QVGA input image size H x V = 320 x 240
Input data format	8-bit gray scale data in little-endian format (color pictures must be converted before FD can be applied) 0x00 = black and 0xFF = white
Face inclination	± 45 degrees
Face direction	Up/down: ± 30 degrees Left/right: ± 60 degrees
Maximum detection count	35 faces
Detection direction	The face orientation must be selected from the following possibilities: 0 degrees: Faces are vertical. + 90 degrees: Faces are rotated right by 90 degrees. – 90 degrees: Faces are rotated left by 90 degrees.
Detection minimum face size	Four grades are available: 20 pixels 25 pixels 32 pixels 40 pixels
Detection area	Detection start position: X = 0 to 160 Y = 0 to 120 Detection area size: X = 160 to 320 Y = 120 to 240
Detection result	The following information is provided by the module for each face: Size Position Angle Confidence level

2 FDIF Integration

This section describes the integration of FDIF in the device, including information about clocks, resets, and hardware requests.

Figure 2 shows the integration of the module in the device.

Figure 2. FDIF Integration



(1) DSP subsystem available only on DM8127.

NOTE: For more information about the IDLE, STANDBY, and DISCONNECT hardware handshakes, see the *Power, Reset, and Clock Management* chapter in the device-specific TRM.

Table 2 through Table 4 summarize the integration of the module in the device. For more information about the power domain or the clock and reset signals, see the *Power, Reset, and Clock Management* chapter in the device-specific TRM.

Table 2. Integration Attributes

Module Instance	Attributes		
	Power Domain	Wake-Up Capability	Interconnect
Face Detect	PD_CAM	No	L3

Table 3. Clocks and Resets

Clocks				
Module Instance	**Destination Signal Name**	**Source Signal Name**	**Source**	**Description**
Face detect	FDIF_FCLK	FDIF_FCLK	PRCM	For information about PRCM clock gating and management, see the *Power, Reset, and Clock Management* chapter in the device-specific TRM.
	FDIF_CLKEN	FCLKEN		
	FDIF_IFCLK	PIFCLK		
Resets				
Face detect	FDIF_RST	CAM_RST	PRCM	For information about PRCM reset sources and distribution, see the *Power, Reset, and Clock Management* chapter in the device-specific TRM.

Table 4. Hardware Requests

Interrupt Requests			
Module Instance	**Source Signal Name**	**Destination**	**Description**
Face detect	FDIF_IRQ3	ARM® Cortex®-A8 MPU subsystem	FDIF interrupt to the ARM Cortex-A8 MPU subsystem
	FDIF_IRQ2	DSP subsystem	FDIF interrupt to the digital signal processor (DSP) subsystem[(1)]
No DMA Requests			

(1) DSP subsystem available only on DM8127.

NOTE: For more information about interrupt sources, see Section 3.4, *Interrupts and Events*.

3 FDIF Functional Description

3.1 FDIF Block Description

The FDIF is a standalone module. It has a port connected to the L4 interconnect, which is used for configuration, and a port connected to the L3 interconnect, which is used to read and write data to the system memory.

CAUTION

These ports are accessible only in 32 bits.

The FDIF core contains the following submodules:

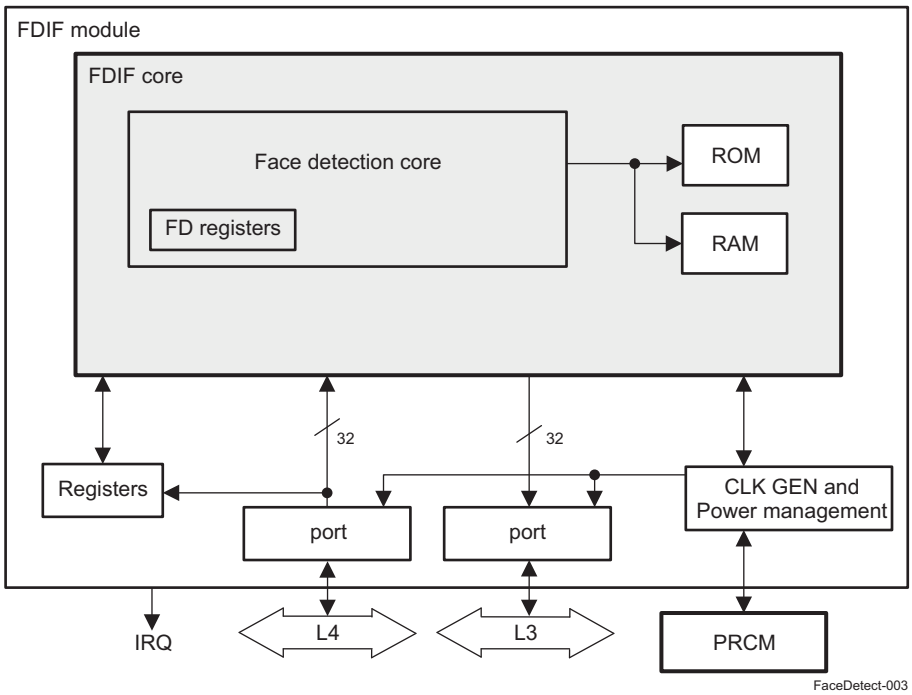
- Face detection (FD) IP core
- RAM and ROM memories

The FDIF module wraps the FD core for integration in the device. The following submodules are added:

- Clock generation
- Interrupt generation
- Power management
- L3 and L4 interface ports: Two ports required to decorrelate the FDIF clocks from other system clocks, one on the L3 port interface, and one on the L4 port interface.

Figure 3 shows the overall architecture of the FDIF.

Figure 3. FDIF Block Diagram



3.2 Software Reset

The module is reset by writing the FDIF_SYSCONFIG[0] SOFTRESET bit to 1. The bit is automatically reset by hardware. During reads, it always returns 0.

The FD core also provides a software reset setup by the FD_CTRL[0] SRST bit, but it is strongly recommended to use only the FDIF_SYSCONFIG[0] SOFTRESET bit.

3.3 System Power Management

There is one clock domain in FDIF: the L4 port domain and L3 port domain are synchronized with the module functional clock domain, FDIF_FCLK.

Table 5 lists the power-management features available for FDIF.

NOTE:

- For more information about source clock gating, see the device-specific TRM.
- For descriptions of idle mode and standby mode and the power, reset, and clock management (PRCM) power handshake, see the *Power, Reset, and Clock Management* chapter in the device-specific TRM.

Table 5. Local Power-Management Features

Feature	Registers	Description
Clock autogating	No software control for it.	It is always enabled.
Slave idle modes	FDIF_SYSCONFIG[3:2] IDLEMODE	Force-idle, no-idle, smart-idle, and smart-idle wakeup-capable modes are available (0h, 1h, 2h, and 3h, respectively).
Clock activity	N/A	
Master standby modes	FDIF_SYSCONFIG[5:4] STANDBYMODE	Force-standby, no-standby, smart-standby, and smart-standby wakeup-capable modes are available (0h, 1h, 2h, and 3h, respectively). See Section 3.3.2.1 for more information.
Global wake-up enable	N/A	
Wake-up sources enable	N/A	

3.3.1 Autogating

The FDIF performs clock autogating whenever possible. There is no software control for it; it is always enabled.

3.3.2 PRCM Hardware Handshake

The FDIF supports the IDLE protocol between the L4 port and the PRCM module and the STANDBY protocol between the L3 port and the PRCM module. The FDIF also supports the DISCONNECT protocol on the L4 and L3 ports.

The FDIF first initiates the STANDBY protocol with the PRCM module, which in turn generates the IDLE protocol with the FDIF. The functional clock is gated by the PRCM module only when the IDLE and STANDBY power-management protocols are complete.

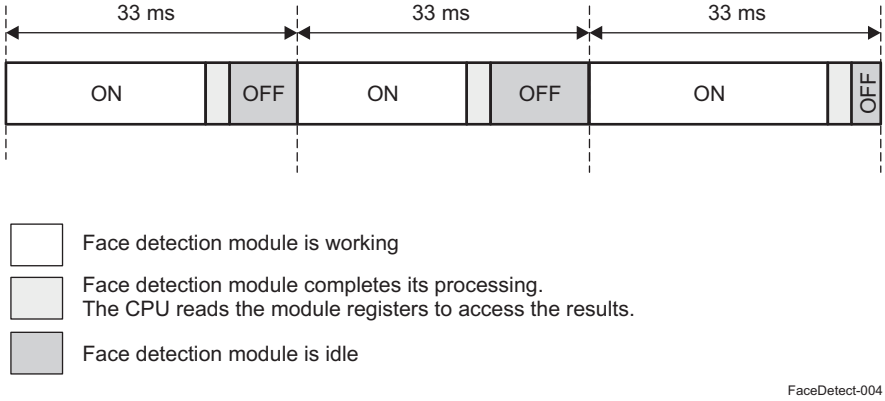
For more information about these protocols, see the device-specific TRM.

3.3.2.1 Protocol Transitions

The FDIF goes to IDLE as soon as it is done processing and the MPU has read the results of the computation.

Figure 4 shows the principle. The 33-ms period corresponds to 30 fps, which is usually the target for imaging applications. Time spent in READ state (= ON state) is always the same, and the time in OFF state depends on the time spent in ON state.

Figure 4. FDIF Power-Management Transitions



3.3.2.1.1 Normal Mode to Idle Mode

Software programs FDIF_SYSCONFIG[5:4] STANDBYMODE = 0x2 to program the power-management mode.

When its processing is complete, the FD core generates the FINISH_IRQ event. At this time the FD_CTRL[1] RUN bit reflects that the FD core is idle.

Software running on the MPU reads the results of the FD algorithm. When it finishes reading the results, it clears the FDIF_IRQSTATUS_RAW_j[8] FINISH_IRQ bit and writes FDIF_CTRL[5] MSTANDBY = 1 to initiate the MStandby signal generation. For more information about the STANDBY and IDLE hardware handshakes, see the device-specific TRM.

The FDIF clock can be gated only when the STANDBY and IDLE protocols are complete.

3.3.2.1.2 Idle Mode to Normal Mode

The PRCM module deasserts a signal to the FDIF under software control so that the module can switch back to normal mode. Then, the module functional clock is ensured and stable. Software disables the MStandby signal generation by writing FDIF_CTRL[5] MSTANDBY = 0, and then polls for FDIF_CTRL[6] MSTANDBY_HDSHK = 1 to ensure that the power-management handshaking is complete. For more information about the standby and idle modes, see the device-specific TRM.

3.4 Interrupts and Events

The FDIF has up to two interrupt lines (FDIF_IRQ2 and FDIF_IRQ3).

The FDIF generates events listed in Table 6. An interrupt can be enabled by using the FDIF_IRQENABLE_SET_j register and can be disabled by using the FDIF_IRQENABLE_CLR_j register.

Table 6. Interrupts and Events Description

Event Name	Description
FDIF_IRQSTATUS_RAW_j / FDIF_IRQSTATUS_j[8] FINISH_IRQ	This event is generated by the FD IP core. It flags the completion of the processing by the IP.
FDIF_IRQSTATUS_RAW_j / FDIF_IRQSTATUS_j[0] ERR_IRQ	This event flags that the L3 port has received an error.

The FDIF_IRQSTATUS_RAW_j and FDIF_IRQSTATUS_j registers give the interrupt status. The difference between them is that the FDIF_IRQSTATUS_RAW_j register is set even if events are not enabled.

The FDIF_IRQSTATUS_j register can be used to clear events.

3.5 Typical Use

Typically, FD processing is applied to buffers provided by the ISP module, already in the correct format.

To enable FD processing, the 32-bit address of the input image in memory must be set up in the FDIF_PICADDR register, and the 32-bit address of the working memory must be set up in the FDIF_WKADDR register.

The detection condition settings can be set with the following registers:

- FD_DCOND
- FD_STARTX
- FD_STARTY
- FD_SIZEX
- FD_STARTY

  For more information, see Section 4, *FDIF Programming Guide*.

When the FD_CTRL[1] RUN bit is set to 1, the process starts. When the process is complete (FD_CTRL[2] FINISH = 1), the results are available in the following registers:

- FD_DNUM
- FD_CENTERX_i
- FD_CENTERY_i
- FD_CONFSIZE_i
- FD_ANGLE_i

  For more information, see Section 4, *FDIF Programming Guide*.

3.6 Performance Parameters

Table 7 lists the register settings that affect performance.

Table 7. Performance Parameters

Parameter	Comments
FD_DCOND[1:0] MIN	Sets the minimum face size. The permitted values are 20x20, 25x25, 32x32, and 40x40. A high value leads to higher performance.
FD_DCOND[3:2] DIR	Sets the detection direction setting. The permitted values are UP, RIGHT, and LEFT. The UP value should lead to better performance than RIGHT and LEFT.
FD_LHIT[3:0] LHIT	Sets the detection threshold. The permitted values are in the range of 0 to 9. A low value increases the FD probability detection, but it also increases false detections.

3.7 L3 Interconnect Parameters

The FDIF is an initiator on the L3 interconnect. L3 accesses can be configured with the FDIF_CTRL[4:1] MAX_TAGS bit field and the FDIF_CTRL[0] WRNP bit. For more information about these parameters, see the device-specific TRM.

4 FDIF Programming Guide

4.1 FDIF Low-level Programming Models

This section describes the low-level hardware programming sequences for the configuration and use of the FDIF.

4.1.1 Global Initialization

4.1.1.1 Surrounding Modules Global Initialization

This section identifies the requirements for initializing the surrounding modules when the FDIF is to be used for the first time after a device reset. This initialization of the surrounding modules is based on the integration of the FDIF.

For more information, see Section 2, *FDIF Integration*.

Table 8. Global Initialization of Surrounding Modules

Surrounding Modules	Comments
PRCM	FDIF_FCLK functional clock must be enabled. See the *Power, Reset, and Clock Management* chapter in the device-specific TRM.
ARM® Cortex®-A8 MPU interrupt controller (INTC) (or DSP INTC)	The ARM Cortex-A8 MPU (or DSP) interrupt controller must be configured to enable the interrupt request generation to the Cortex-A8 MPU (or DSP) subsystem when interrupt requests are generated by the FDIF. See the respective Functional Description in the device-specific TRM.
Interconnect (L3 and L4)	For more information, see the device-specific TRM.

4.1.1.2 FDIF Global Initialization

4.1.1.2.1 Main Sequence – FDIF Global Initialization

Table 9 lists the procedure to initialize the FDIF after a power-on or software reset.

Table 9. FDIF Global Initialization

Step	Register/Bit Field/Programming Model	Value
Perform a software reset.	FDIF_SYSCONFIG[0] SOFTRESET	0x1
Wait until reset is finished.	FDIF_SYSCONFIG[0] SOFTRESET	0x0
Set the maximum interconnect tags.	FDIF_CTRL[4:1] MAX_TAGS	0xA
Enable ERROR type Interrupt.	FDIF_IRQENABLE_SET_j[0] ERR_IRQ	0x1

4.1.2 FD Operational Modes Configuration

4.1.2.1 FD Processing Modes

4.1.2.1.1 Main Sequence – FDIF Polling Method

Step	Register/Bit Field/Programming Model	Value
Set image parameters.	See Section 4.1.2.1.3, *Subsequence – Set Image Parameters*.	
Request the processing.	FD_CTRL[1] RUN	0x1
Wait until process is finished.	FD_CTRL[2] FINISH	0x1
Read the results.	See Section 4.1.2.1.4	

4.1.2.1.2 Main Sequence – FDIF Interrupt Method

Step	Register/Bit Field/Programming Model	Value
Set image parameters.	See Section 4.1.2.1.3, *Subsequence – Set Image Parameters*.	
Enable FINISH type interrupt.	FDIF_IRQENABLE_SET_j[8] FINISH IRQ	0x1
Request the processing.	FD_CTRL[1] RUN	0x1

WHEN INTERRUPT OCCURS:

Step	Register/Bit Field/Programming Model	Value
IF: This is FD Process Complete Event?	FDIF_IRQSTATUS_j[8] FINISH_IRQ	0x1
Clear (Disable) FINISH type interrupt.	FDIF_IRQENABLE_CLR_j[8] FINISH IRQ	0x1
Read the results	See Section 4.1.2.1.4, *Subsequence – Read the Results*.	
ELSE		
Clear (Disable) ERROR type Interrupt.	FDIF_IRQENABLE_CLR_j[0] ERR_IRQ	0x1
Perform a software reset.	FDIF_SYSCONFIG[0] SOFTRESET	0x1
For possible errors and the explanations of them, see the device-specific TRM.		
ENDIF		

4.1.2.1.3 Subsequence – Set Image Parameters

Step	Register/Bit Field/Programming Model	Value
Set input image 32-bit address.	FDIF_PICADDR[31:5] ADDR	0x----
Set working memory 32-bit address.	FDIF_WKADDR[31:5] ADDR	0x----
Set the minimum face size.	FD_DCOND[1:0] MIN	0x-
Set the face direction.	FD_DCOND[3:2] DIR	0x-
Set the horizontal start position of the detection area.	FD_STARTX[7:0] STARTX	0x-
Set the vertical start position of the detection area.	FD_STARTY[6:0] STARTY	0x-
Set the horizontal start size of the detection area.	FD_SIZEX[8:0] SIZEX	0x–
Set the vertical start size of the detection area.	FD_SIZEY[7:0] SIZEY	0x-
Set the detection threshold.	FD_LHIT[3:0] LHIT	0x-

4.1.2.1.4 Subsequence – Read the Results

Step	Register/Bit Field/Programming Model	Value
Read the number of found faces	FD_DNUM[5:0] DNUM	0x-
For each face detected, read the following parameters by processing loop until FD_DNUM[5:0] DNUM = 0:		
For each face read X_i coordinate	FD_CENTERX_i[8:0] CENTERX	0x–
For each face read Y_i coordinate	FD_CENTERY_i[7:0] CENTERY	0x-
For each face read confidence level	FD_CONFSIZE_i[11:8] CONF	0x-
For each face read size_i	FD_CONFSIZE_i[7:0] SIZE	0x-
For each face read the angle	FD_ANGLE_i[8:0] ANGLE	0x-

5 FDIF Registers

Table 10 is the FDIF instance.

Table 10. FDIF Instance Summary

Module Name	Base Address	Size
FDIF	0x481D 6000	4 KB

Table 11 summarizes the FDIF register mapping.

Table 11. FDIF Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	FDIF L4 Base Address
FDIF_REVISION	R	32	0x0000 0000	0x481D 6000
FDIF_HWINFO	R	32	0x0000 0004	0x481D 6004
FDIF_SYSCONFIG	RW	32	0x0000 0010	0x481D 6010
RESERVED	R	32	0x0000 0020	0x481D 6020
FDIF_IRQSTATUS_RAW_j (1)	RW	32	0x0000 0044 + (0x10 * j	0x481D 6024 + (0x10 * j)
FDIF_IRQSTATUS_j (1)	RW	32	0x0000 0048 + (0x10 * j)	0x481D 6028 + (0x10 * j)
FDIF_IRQENABLE_SET_j (1)	RW	32	0x0000 004C + (0x10 * j)	0x481D 602C + (0x10 * j)
FDIF_IRQENABLE_CLR_j (1)	RW	32	0x0000 0050 + (0x10 * j)	0x481D 6030 + (0x10 * j)
FDIF_PICADDR	RW	32	0x0000 0060	0x481D 6060
FDIF_CTRL	RW	32	0x0000 0064	0x481D 6064
FDIF_WKADDR	RW	32	0x0000 0068	0x481D 6068
FD_CTRL	RW	32	0x0000 0080	0x481D 6080
FD_DNUM	R	32	0x0000 0084	0x481D 6084
FD_DCOND	RW	32	0x0000 0088	0x481D 6088
FD_STARTX	RW	32	0x0000 008C	0x481D 608C
FD_STARTY	RW	32	0x0000 0090	0x481D 6090
FD_SIZEX	RW	32	0x0000 0094	0x481D 6094
FD_SIZEY	RW	32	0x0000 0098	0x481D 6098
FD_LHIT	RW	32	0x0000 009C	0x481D 609C
FD_CENTERX_i (2)	R	32	0x0000 0160 + (0x10 * i)	0x481D 6160 + (0x10 * i)
FD_CENTERY_i (2)	R	32	0x0000 0164 + (0x10 * i)	0x481D 6164 + (0x10 * i)
FD_CONFSIZE_i (2)	R	32	0x0000 0168 + (0x10 * i)	0x481D 6168 + (0x10 * i)
FD_ANGLE_i (2)	R	32	0x0000 016C + (0x10 * i)	0x481D 616C + (0x10 * i)

(1) j = 2 or 3. j = 2 is available only on DM8127.
(2) i = 0 to 34

5.1 FDIF_REVISION

Table 12. FDIF_REVISION

Address Offset	0x0000 0000		
Physical Address	0x481D 6000	**Instance**	FDIF
Description	IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															

Bits	Field Name	Description	Type	Reset
31:0	REVISION	IP Revision number	R	0x---- ---- TI Internal Data

5.2 FDIF_HWINFO

Table 13. FDIF_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x481D 6004	**Instance**	FDIF
Description	Information about the IP module's hardware configuration, that is, typically the module's HDL generics (if any). Actual field format and encoding is up to the module's designer to decide.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												FDIF_TAGS			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:0	FDIF_TAGS	Hardware design value. This bit field reflects the value of the FDIF_TAG generic parameter. 0x0: 1 tag supported 0x1: 2 tags supported [...] 0xF: 16 tags supported	R	0xF

5.3 FDIF_SYSCONFIG

Table 14. FDIF_SYSCONFIG

Address Offset	0x0000 0010		
Physical Address	0x481D 6010	**Instance**	FDIF
Description	Clock management configuration		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										STANDBYMODE		IDLEMODE		RESERVED	SOFTRESET

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved	R	0x0000000
5:4	STANDBYMODE	Configuration of the local initiator state management mode. By definition, initiator may generate read/write transaction as long as it is out of STANDBY state. 0x0: Force-standby mode: local initiator is unconditionally placed in standby state. Backup mode, for debug only. 0x1: No-standby mode: local initiator is unconditionally placed out of standby state. Backup mode, for debug only. 0x2: Smart-standby mode: local initiator standby status depends on local conditions, that is, the module's functional requirement from the initiator. IP module shall not generate (initiator-related) wake-up events. 0x3: Smart-standby wakeup-capable mode: local initiator standby status depends on local conditions, that is, the module's functional requirement from the initiator.	RW	0x2
3:2	IDLEMODE	Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state. 0x0: Force-idle mode: local target's idle state follows (acknowledges) the system's idle requests unconditionally, that is, regardless of the IP module's internal requirements. Backup mode, for debug only. 0x1: No-idle mode: local target never enters idle state. Backup mode, for debug only. 0x2: Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wake-up events. 0x3: Smart-idle wakeup-capable mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements.	RW	0x2
1	RESERVED	Reserved	R	0
0	SOFTRESET	Software reset. Read 0x0: Reset done, no pending action Write 0x0: No action Write 0x1: Initiate software reset Read 0x1: Reset (software or other) ongoing	RW	0

5.4 FDIF_IRQSTATUS_RAW_j

Table 15. FDIF_IRQSTATUS_RAW_j[1]

Address Offset	0x0000 0044 + (0x10 * j)		
Physical Address	0x481D 6024 + (0x10 * j)	**Instance**	FDIF
Description	Per-event raw interrupt status vector, line #n. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.		
Type	RW		

(1) j = 2 is available only on DM8127.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							FINISH_IRQ	RESERVED							ERR_IRQ

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	FINISH_IRQ	Face detection processing done. Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0
7:1	RESERVED	Reserved	R	0x00
0	ERR_IRQ	Error received by the L3 port. Write 0x0: No action Read 0x0: No event pending Read 0x1: Event pending Write 0x1: Set event (debug)	RW W1toSet	0

5.5 FDIF_IRQSTATUS_j

Table 16. FDIF_IRQSTATUS_j[(1)]

Address Offset	0x0000 0048 + (0x10 * j)		
Physical Address	0x481D 6028 + (0x10 * j)	**Instance**	FDIF
Description	Per-event "enabled" interrupt status vector, line #n. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled).		
Type	RW		

(1) j = 2 is available only on DM8127.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							FINISH_IRQ	RESERVED							ERR_IRQ

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	FINISH_IRQ	Face detection processing done. Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0
7:1	RESERVED	Reserved	R	0x00
0	ERR_IRQ	Error received by the L3 port. Write 0x0: No action Read 0x0: No (enabled) event pending Read 0x1: Event pending Write 0x1: Clear (raw) event	RW W1toClr	0

5.6 FDIF_IRQENABLE_SET_j

Table 17. FDIF_IRQENABLE_SET_j[1]

Address Offset	0x0000 002C + (0x10 * j)		
Physical Address	0x481D 602C + (0x10 * j)	**Instance**	FDIF
Description	Per-event interrupt enable bit vector, line #n. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.		
Type	RW		

[1] j = 2 is available only on DM8127.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							FINISH_IRQ	RESERVED							ERR_IRQ

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	FINISH_IRQ	Face detection processing done. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0
7:1	RESERVED	Reserved	R	0x00
0	ERR_IRQ	Error received by the L3 port. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Enable interrupt	RW W1toSet	0

5.7 FDIF_IRQENABLE_CLR_j

Table 18. FDIF_IRQENABLE_CLR_j[1]

Address Offset	0x0000 0050 + (0x10 * j)		
Physical Address	0x481D 6030 + (0x10 * j)	**Instance**	FDIF
Description	Per-event interrupt enable bit vector, line #n. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.		
Type	RW		

[1] j = 2 is available only on DM8127.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							FINISH_IRQ	RESERVED							ERR_IRQ

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8	FINISH_IRQ	Face detection processing done. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0
7:1	RESERVED	Reserved	R	0x00
0	ERR_IRQ	Error received by the L3 port. Write 0x0: No action Read 0x0: Interrupt disabled (masked) Read 0x1: Interrupt enabled Write 0x1: Disable interrupt	RW W1toClr	0

5.8 FDIF_PICADDR

Table 19. FDIF_PICADDR

Address Offset	0x0000 0060		
Physical Address	0x481D 6060	**Instance**	FDIF
Description	Picture data store address		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																											RESERVED			

Bits	Field Name	Description	Type	Reset
31:5	ADDR	Picture data store address. The 5 least significant bits are forced to 0.	RW	0x0000000
4:0	RESERVED	Read returns 0.	R	0x00

5.9 FDIF_CTRL

Table 20. FDIF_CTRL

Address Offset	0x0000 0064		
Physical Address	0x481D 6064	**Instance**	FDIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								MSTANDBY_HDSHK	MSTANDBY	MAX_TAGS					WRNP

Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Reserved	R	0x0000000
6	MSTANDBY_HDSHK	MStandby / Wait power management handshaking status bit The power management framework of the FDIF module is based on the handshaking of the MSTANDBY and WAIT signals. When going from a idle to normal power management transition, the software polls for FDIF_CTRL.MSTANDBY_HDSHK = 1 before starting the face detection processing. Read 0x0: Handshaking not completed. Do not initiate traffic on L3. Read 0x1: Handshaking completed. Can safely use the FDIF module.	R	0
5	MSTANDBY	MStandby signal generation. This bit shall be set to initiate a power management transition from NORMAL to IDLE or IDLE to NORMAL. 0x0: Write: Clear MStandby signal. One polls FDIF_CTRL.MSTANDBY_HDSHK = 1 after writing this bit to ensure that the power management handshaking is completed. 0x1: Write: Asserts MStandby signal	RW	1
4:1	MAX_TAGS	Max interconnect tags. This bit field sets the maximum number of interconnect tags that the module shall use. This number is programmable between 1 (MAX_TAGS = 0) and FDIF_TAGS (MAX_TAGS = FDIF_TAGS - 1). The value of MAX_TAGS is reflected in the FIDIF_HWINFO register setting. This register setting is expected to have impact on performance. It shall be set once at initialization. Higher value will give more bandwidth to the initiator. Lower value will give less bandwidth to the initiator. This value shall be set as low as possible such that other system initiators are not penalized.	RW	0xF
0	WRNP	L3 port non-posted write control. Dynamic usage of this feature is not supported. This bit shall be set at initialization and not modified hereafter until the processing is completed. When non-posted writes are used, tags shall be used for best performance (MAX_TAGS > 1). 0x0: All writes are non posted 0x1: All writes are posted	RW	0

5.10 FDIF_WKADDR

Table 21. FDIF_WKADDR

Address Offset	0x0000 0068		
Physical Address	0x481D 6068	**Instance**	FDIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																								RESERVED							

Bits	Field Name	Description	Type	Reset
31:5	ADDR	Work area address The 5 least significant bits are forced to 0.	RW	0x0000000
4:0	RESERVED	Read returns 0.	R	0x00

5.11 FD_CTRL

Table 22. FD_CTRL

Address Offset	0x0000 0080		
Physical Address	0x481D 6080	**Instance**	FDIF
Description	Control register Don't set more than 2 bits to "1" at the same time. Otherwise, operations cannot be guaranteed.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																													FINISH	RUN	SRST

Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	R	0x0000 0000
2	FINISH	Process Completion Flag Clear 0x0: Write: Disable Read: Process incomplete 0x1: Write: Process complete flag clear Read: Process complete	RW	0
1	RUN	Process Start Request 0x0: Write: Disable Read: No processing 0x1: Write: Process start request Read: Processing data	RW	0
0	SRST	Software Reset This bit shall not be used to reset the FDIF module. Instead, the FDIF_SYSCONFIG[0] SOFTRESET bit shall be used for complete soft reset. 0x0: Write: Disable Read: Reset cancel 0x1: Write: Reset Read: Under reset	RW	0

5.12 FD_DNUM

Table 23. FD_DNUM

Address Offset	0x0000 0084		
Physical Address	0x481D 6084	**Instance**	FDIF
Description	Face Detection Result Count Register		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DNUM							

Bits	Field Name	Description	Type	Reset
31:6	RESERVED	Reserved	R	0x0000000
5:0	DNUM	Face detection result count. Up to 35 faces can be detected. Number of face(s) detected: 0x0: 0 face detected 0x1: 1 face detected 0x2: 2 faces detected [...] 0x23: 35 faces detected 0x24 to 0x3F: unused	R	0x00

5.13 FD_DCOND

Table 24. FD_DCOND

Address Offset	0x0000 0088		
Physical Address	0x481D 6088	**Instance**	FDIF
Description	Detection Condition Setting Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												DIR		MIN	

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:2	DIR	Detection direction setting 0x0: Executes only for UP 0x1: Executes only for RIGHT 0x2: Executes only for LEFT 0x3: Reserved	RW	0x0
1:0	MIN	Reserved 0x0: Set the min face size to 20 pixels 0x1: Set the min face size to 25 pixels 0x2: Set the min face size to 32 pixels 0x3: Set the min face size to 40 pixels	RW	0x0

5.14 FD_STARTX

Table 25. FD_STARTX

Address Offset	0x0000 008C		
Physical Address	0x481D 608C	**Instance**	FDIF
Description	Detection Area Setting Register: X Start Coordinate.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STARTX							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	STARTX	Starting X coordinates Permitted values are 0<=STARTX<=160	RW	0x00

5.15 FD_STARTY

Table 26. FD_STARTY

Address Offset	0x0000 0090		
Physical Address	0x481D 6090	**Instance**	FDIF
Description	Detection Area Setting Register: Y Start Coordinate.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								STARTY							

Bits	Field Name	Description	Type	Reset
31:7	RESERVED	Reserved	R	0x0000000
6:0	STARTY	Starting Y coordinates Permitted values are 0<=STARTY<=120	RW	0x00

5.16 FD_SIZEX

Table 27. FD_SIZEX

Address Offset	0x0000 0094		
Physical Address	0x481D 6094	**Instance**	FDIF
Description	Detection Area Setting Register: X Direction Size		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SIZEX							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved	R	0x000000
8:0	SIZEX	X Direction Size	RW	0x140

5.17 FD_SIZEY

Table 28. FD_SIZEY

Address Offset	0x0000 0098		
Physical Address	0x481D 6098	**Instance**	FDIF
Description	Detection Area Setting Register: Y Direction Size		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SIZEY							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	SIZEY	Y Direction Size	RW	0xF0

5.18 FD_LHIT

Table 29. FD_LHIT

Address Offset	0x0000 009C		
Physical Address	0x481D 609C	**Instance**	FDIF
Description	Threshold Setting Register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												LHIT			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED	Reserved	R	0x0000000
3:0	LHIT	Threshold. Permitted values are 0x0 to 0x9.	RW	0x5

5.19 FD_CENTERX_i

Table 30. FD_CENTERX_i

Address Offset	0x0000 0160 + (0x10 * i)		
Physical Address	0x481D 6160 + (0x10 * i)	**Instance**	FDIF
Description	Detection Result: X Coordinate. Its value is undefined after reset.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CENTERX							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved. Read returns reset value.	R	0x–
8:0	CENTERX	Face position: center X coordinate The coordinates given by (FD_CENTERX_i, FD_CENTERY_i) give the central coordinates of the face position. Permitted values are 0x0 to 0x13F.	R	0x–

5.20 FD_CENTERY_i

Table 31. FD_CENTERY_i

Address Offset	0x0000 0164 + (0x10 * i)		
Physical Address	0x481D 6164 + (0x10 * i)	**Instance**	FDIF
Description	Detection Result: Y Coordinate. Its value is undefined after reset.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CENTERY							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved. Read returns reset value.	R	0x–
7:0	CENTERY	Face position: center Y coordinate The coordinates given by (FD_CENTERX_i, FD_CENTERY_i) give the central coordinates of the face position. Permitted values are 0x0 to 0xEF.	R	0x–

5.21 FD_CONFSIZE_i

Table 32. FD_CONFSIZE_i

Address Offset	0x0000 0168 + (0x10 * i)		
Physical Address	0x481D 6168 + (0x10 * i)	**Instance**	FDIF
Description	Detection Result: Confidence Level and Size. Its value is undefined after reset.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				CONF				SIZE							

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reserved. Read returns reset value.	R	0x-
11:8	CONF	Confidence level. Permitted values are 0x0 (high) to 0x9 (low).	R	0x-
7:0	SIZE	Detection result face size. Permitted values 0x14 to 0xF0.	R	0x–

5.22 FD_ANGLE_i

Table 33. FD_ANGLE_i

Address Offset	0x0000 016C + (0x10 * i)		
Physical Address	0x481D 616C + (0x10 * i)	**Instance**	FDIF
Description	Detection Result: Angle. Its value is undefined after reset.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ANGLE							

Bits	Field Name	Description	Type	Reset
31:9	RESERVED	Reserved. Read returns reset value.	R	0x-
8:0	ANGLE	Detection result face angle. Permitted values: When DIR = 0: 0x0 (0 deg) to 0x1E (30 deg) and 0x14A (330 deg) to 0x167 (359 deg). When DIR = 1: 0x03C (60 deg) to 0x078 (120 deg) When DIR = 2: 0x0F0 (240 deg) to 0x12C (300 deg)	R	0x–

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265