KeyStone II Architecture Serializer/Deserializer (SerDes)

User's Guide

Literature Number: SPRUHO3A
May 2013–Revised July 2016

Contents

List of Figures

List of Tables

Preface

About This Manual

The serializer-deserializer (SerDes) performs serial-to-parallel conversions on data received from a peripheral device and parallel-to-serial conversion on data received from the CPU. The SerDes includes control capability and a processor interrupt system that can be tailored to minimize software management of the communications link.

Notational Conventions

This document uses the following conventions:

- Commands and keywords are in **boldface** font.
- Arguments for which you supply values are in *italic* font.
- Terminal sessions and information the system displays are in screen font.
- Information you must enter is in **boldface screen font**.
- Elements in square brackets ([ ]) are optional.

Notes use the following conventions:

NOTE: Means reader take note. Notes contain helpful suggestions or references to material not covered in the publication.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

CAUTION

Indicates the possibility of service interruption if precautions are not taken.

WARNING

Indicates the possibility of damage to equipment if precautions are not taken.

Related Documentation from Texas Instruments

AIF1-to-AIF2 Antenna Interface Migration Guide for KeyStone Devices	SPRABH8
Antenna Interface 2 (AIF2) for KeyStone Devices User Guide	SPRUGV7
Clocking Design Guide for KeyStone Devices	SPRABI4
Connecting AIF2 with FFTC	SPRABF3
DDR3 Design Guide for KeyStone Devices	SPRABI1
General Purpose AIF2 Traffic for KeyStone Devices	SPRABH3
Gigabit Ethernet (GbE) Switch Subsystem for KeyStone Devices User Guide	SPRUGV9
Hardware Design Guide for KeyStone Devices	SPRABI2

HyperLink for KeyStone Devices User Guide	SPRUGW8
HyperLink Use Cases for KeyStone Devices	SPRABH5
Layer 2 (PA/SA/MultiCore Navigator) Applications for KeyStone Devices	SPRABH7
Network Coprocessor (NETCP) for KeyStone Devices User Guide	SPRUGZ6
Packet Accelerator (PA) for KeyStone Devices User Guide	SPRUGS4
Peripheral Component Interconnect Express (PCIe) for KeyStone Devices User Guide	SPRUGS6
Phase Locked Loop (PLL) Controller for KeyStone Devices User Guide	SPRUGV2
Serial RapidIO (SRIO) for KeyStone Devices User Guide	SPRUGW1
SRIO Migration Guide (F to N) for KeyStone Devices	SPRABI0
SRIO Usage Considerations for KeyStone Devices	SPRABH4
TMS320C6608 Multicore Fixed and Floating-Point Digital Signal Processor Data Manual	SPRS623
TMS320TCI6608 Multicore Fixed and Floating Point DSP Silicon Errata	SPRZ333
TMS320C6670 Multicore Fixed and Floating-Point System-on-Chip Data Manual	SPRS689
TMS320C6670 Multicore Fixed and Floating-Point System-on-Chip Silicon Errata	SPRZ332
TMS320C6672 Multicore Fixed and Floating-Point Digital Signal Processor Data Manual	SPRS708
TMS320C6672 Fixed and Floating-Point Digital Signal Processor Silicon Errata	SPRZ335
TMS320C6674 Multicore Fixed and Floating-Point Digital Signal Processor Data Manual	SPRS692
TMS320C6674 Fixed and Floating-Point Digital Signal Processor Silicon Errata	SPRZ341
TMS320C6678 Multicore Fixed and Floating-Point Digital Signal Processor Data Manual	SPRS691
TMS320C6678 Fixed and Floating-Point Digital Signal Processor Silicon Errata	SPRZ334
TMS320TCI6614 C ommunications Infrastructure KeyStone System-on-Chip Data Manual	SPRS671
TMS320TCI6616 C ommunications Infrastructure KeyStone System-on-Chip Data Manual	SPRS624
TMS320TCI6616 Communications Infrastructure KeyStone SOC Silicon Errata	SPRZ331
TMS320TCI6618 C ommunications Infrastructure KeyStone System-on-Chip Data Manual	SPRS688

Introduction

This document is intended to aid in the hardware design and implementation of a KeyStone II-based system. The document should be used along with the device-specific data manual and relevant user guides, application reports, standards, and specifications (see Related Documentation from Texas Instruments).

NOTE: TI KeyStone II family of devices use a different SerDes PHY from the one used on KeyStone I family devices. Users are advised to pay attention to details in this document while designing for KeyStone II family of TI SoCs.

Topic **Page**

1.1 Purpose and Scope

The goal of KeyStone II SerDes collateral material is to make system implementation easier for the user by providing the system solution. For these SerDes-based interfaces, it is not assumed that the system designer is familiar with the industry specifications, SerDes technology, or RF/microwave PCB design. However, it is still expected that the PCB design work will be supervised by a knowledgeable high-speed digital PCB designer and an assumption is made that the PCB designer is using established high-speed design rules.

This document contains implementation instructions for the serializer/deserializer (SerDes)-based interfaces on the KeyStone II family of DSP devices. These include:

- Serial RapidIO® (SRIO)
- Antenna Interface (AIF or AIL)
- HyperLink
- Serial Gigabit Media Independent Interface (SGMII) interfaces
- Peripheral Component Interconnect Express (PCIe)
- Ten Gigabit Ethernet (10GbE)
- JESD204B

Serial RapidIO is an industry-standard high-speed switched-packet interconnect. The Antenna Interface is compatible with two industry standards targeted at cellular base station solutions: Open Base Station Architecture Initiative (OBSAI) and Common Public Radio Interface (CPRI). SGMII and 10GbE are used for gigabit and 10 gigabit Ethernet connections from MAC to MAC, or MAC to PHY. Peripheral Component Interconnect Express (PCIe) is another industry standard for high speed serial interconnect. JESD204B is a serial interface standard for data converters. HyperLink is a Texas Instruments high-speed packet-based interconnect optimized and intended for chip-to-chip interconnects.

For each of these interfaces, physical layer data transmission uses analog SerDes to feed low-output-swing differential current-mode logic (CML) buffers. Proper printed circuit board (PCB) design for these interfaces resembles analog or RF design, and is very different from traditional parallel digital bus design.

Due to this analog nature of SerDes-based interfaces, it is not possible to specify the interface in a traditional DSP digital interface manner. Furthermore, it is undesirable to specify the interface in terms of the raw physical requirements laid out by the industry standard specifications. Understanding these specifications and producing a compliant PCB based on the explicit and implicit requirements demands significant time, experience, and expensive tools.

For KeyStone II SerDes-based interfaces, the approach is to reduce the specifications to a set of easy-to-follow PCB routing rules and system configurations. TI has performed the simulation and system design work to ensure the appropriate interface requirements are met. This document describes guidelines that, when followed, result in board-level implementations that meet the interface requirements.

NOTE: USB 2.0 and USB 3.0 interfaces are supported on some KeyStone family of devices. For more details on USB Interface see relevant data manuals.

1.2 Industry Standards Compatibility

All SerDes interfaces are configured as point-to-point connections. It is assumed that the connection is made between a KeyStone II SoC and another device that is compliant to the appropriate industry standard. The list of supported standards is given below.

Note that this document deals with the physical layer and, therefore, it is the electrical specifications in these standards that are relevant. For more information regarding protocol compliance (1), see the device-specific user guides in Related Documentation from Texas Instruments.

- **Serial RapidIO:** This is electrically compliant with Serial RapidIO specification revision 2.1
- **Antenna Interface:** This support both OBSAI and CIPRI interfaces
  - **OBSAI** interface is electrically compliant with the OBSAI RP3 specification version 4.1; RP1 specification version 2.1
  - **CPRI** interface is electrically compliant with the low voltage variant of the CPRI version 4.1 specification (guided by XAUI 802.3ae Clause 47). Devices with the Antenna Interface Link (AIL) peripheral may also be electrically compliant to the CPRI version 5.0 specification. Please consult the device specific datasheet for more information.
- **SGMII:** This is electrically compliant with SGMII revision 1.8 with the following clarifications
  - It does not implement the separate clock signaling
  - Electrical compatibility does not guarantee interoperability with devices.
- **JESD204B:** This is electrically compliant with the JEDEC Standards JESD204A and JESD204B.
- **Peripheral Component Interconnect Express:** This is electrically compliant with version 2.1.
- **Ten Gigabit Ethernet (10GbE):** Supports the following electrical interfaces:
  - Supports XFI SFF INF-8077i spec (no SFP/SFP+) for 10Gb
  - Supports Serial-GMII (SGMII) Specification for 10/100/1000Mb
  - Supports 10GBase-KR Specification for 10Gb
- **HyperLink:** This is a Texas Instruments interface that provides a high-speed, low-latency, and low-pin-count communication interface between two KeyStone II devices. For more details, see the *HyperLink Users Guide* in Related Documentation from Texas Instruments.

(1) Electrical compatibility does not guarantee interoperability with devices

General Information on KeyStone II SerDes

Topic **Page**

2.1 Introduction to SerDes

The simple goal of the SerDes peripheral is twofold: convert SOC parallel data into serialized data that can be output over a high-speed electrical interface, and convert high-speed serial input data into parallel data that can be processed by the SOC. To this end, the TI SerDes contains a variety of macros to handle both the external analog interface as well as the internal digital logic.

At its most basic, the SerDes is comprised of:

- Clock Multiplier Unit (CMU): The CMU handles peripheral and TX clocking of the SerDes. It consists of an internal PLL and the reference clock input buffers.
- Lanes: The lanes handle all inputs and outputs from the serial interface, and contain the TX/RX I/Os, serializers/deserializers, and CDR. A SerDes peripheral can have either two or four lanes.
- Physical Coding Sub-block (PCS): The PCS is responsible for translating data from/to the parallel interface, as well as data encoding/decoding and symbol alignment.
- WIZ: The WIZ acts as a wrapper for the SerDes peripheral, and can both send control signals to and report status signals from the SerDes.

Figure 2-1 illustrates the connections between each of the macros within a SerDes peripheral. These macros are referenced and explored in greater detail throughout this document.

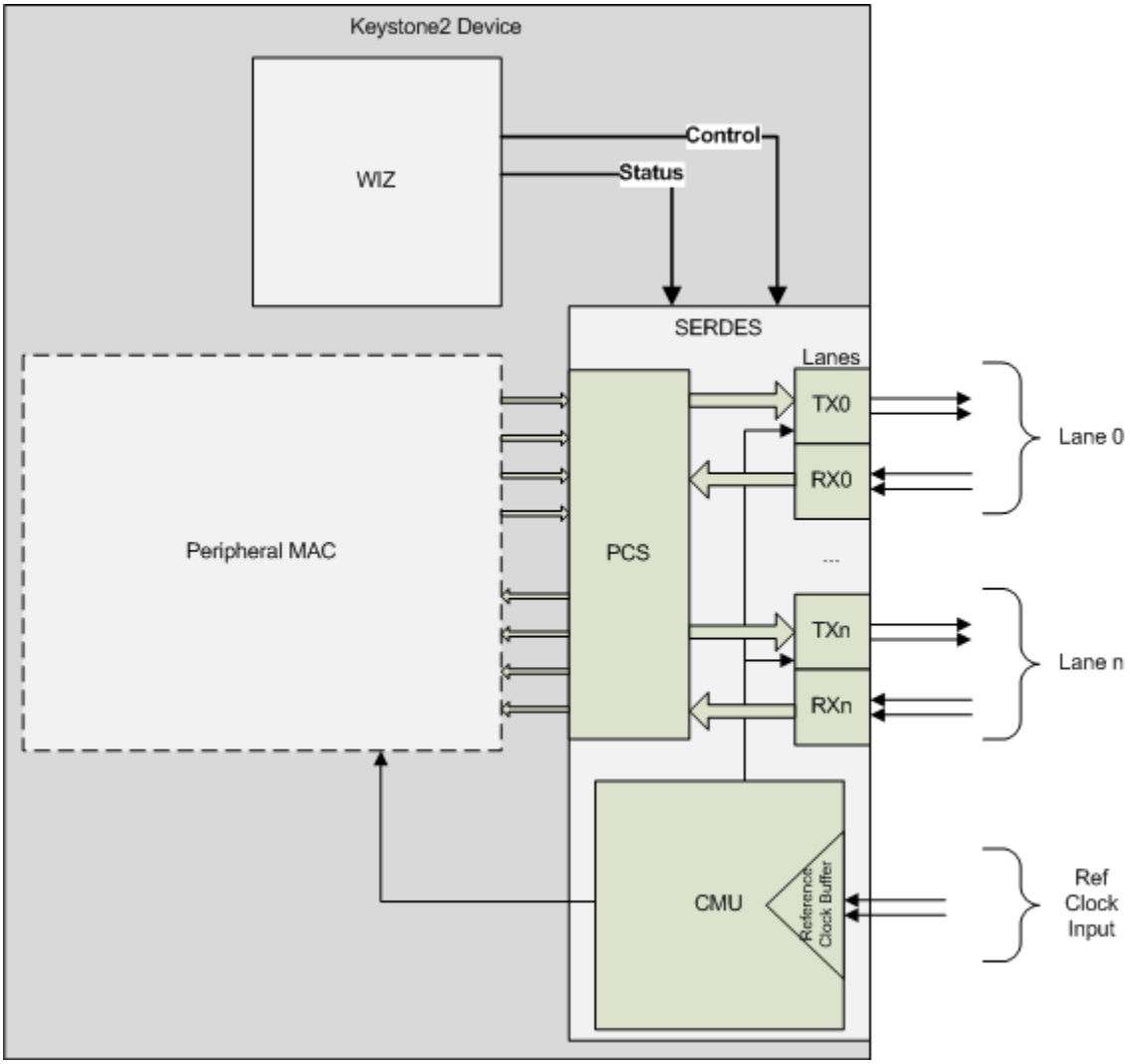


Figure 2-1. Block Diagram of 2-Lane SerDes Peripheral

2.2 SerDes Migration From KeyStone I to KeyStone II

KeyStone I family SerDes configuration involved read-modify-writes to specific SerDes configuration space while continuing to retain *reserved* fields unmodified after reset.

In KeyStone II Devices, SerDes configuration involves loading default configuration specific to an interface as a preliminary step. Configuring SerDes on KeyStone II devices requires:

1. Load default SerDes
2. PHY configurations specific to each interface through TI-provided APIs supplied as part of MCSDK (this step involves some writes to *reserved* bit-fields as well).
3. Configure the lane rate to be used by setting either 1x Rate, 1/2x Rate, or 1/4 Rate, although all rate settings may not be available for a given configuration.
4. Optimize TX and RX channel equalization parameters (such as the TX FIR Filter Coefficients or the RX ATT and BOOST) to a specific hardware platform. For this, perform register level read-modify-writes to the bit-fields you intend to modify.

NOTE: TI requires customers to use TI-generated and supported default PHY configurations (supplied as part of MCSDK) as a starting point for all SerDes programming. TI cannot directly support customer generated configuration files, only platform specific optimization based on default configurations will be supported.

2.3 SerDes PHY Mapping on KeyStone II Devices

The KeyStone II SerDes interfaces consist of two main variants of the SerDes PHYs - PHY-A and PHY-B. Within PHY-A, there are 2 variants: PHY-A 2 Lane and PHY-A 4 Lane. Table 2-1 lists the various interfaces and the PHYs used by each interface.

Table 2-1. PHY and SerDes Interface Mapping on KeyStone II Devices

PHY Name	Sub-Systems in Each PHY	Interfaces Supported	Memory Map Tables
PHY-A 2 Lane	1 CMU, 2 Lanes, 1 Comlane, 1 WIZ	JESD204A/B, AIL, AIF2 (lane 5-6), PCIe	Table 16-1
PHY-A 4 Lane	1 CMU, 4 Lanes, 1 Comlane, 1 WIZ	AIF2 (lanes 1-4), SGMII, SRIO, HyperLink	Table 16-2
PHY-B	2 CMUs, 2 Lanes, 1 Comlane, 1 WIZ	10GbE	Table 16-3

General PCB Routing Recommendations

Topic **Page**

3.1 Minimum PCB Stack up

The minimum PCB stack up for routing the KeyStone II devices is considered to be six layers, as described in Table 3-1.This assumes a minimal number of peripherals are used.

Combining of peripherals will increase PCB stack up complexity and layer count. It is possible to route all peripherals in a 12- to 14-layer board if priority is given to high performance interfaces. Otherwise, the layer count (including power planes) can grow to as many as 18 layers.

Table 3-1. Minimum PCB Stackup

Layer	Type	Description
1	Signal	Top routing
2	Plane	Ground
3	Plane	Split power
4	Signal	Internal routing
5	Plane	Ground
6	Signal	Bottom routing

Additional layers may be added as needed. All layers with SerDes traces must be able to achieve a 100-Ω differential impedance.

3.2 General Trace/Space and Via Sizes

The key concern for SerDes signal traces is the need to achieve a 100-Ω differential impedance. This differential impedance is impacted by trace width, trace spacing, distance between planes, and dielectric material. Verify with a proper PCB manufacturing tool that the trace geometry for all SerDes traces results in differential impedance traces of exactly 100-Ω.

The signal trace impedance must also remain constant across the design. Impedance discontinuities due to vias and reference voids must be mitigated. Higher rates are also concerned with impedance discontinuities from routing corners and fiber weave effects. All of these discontinuities degrade signal integrity and can impact the performance of a design.

Of secondary concern is the insertion loss caused by the traces. Due to the skin effect, wider traces have lower losses than narrower traces. Therefore, longer SerDes runs should use wider traces for lower loss. However, be aware that layers in the stack up that are set to 100-Ω differential impedance with wider traces may be less desirable for routing other signals. Trace widths up to 10 mils are permitted on long-run backplanes. SerDes applications may use trace lengths of up to 40 inches. TI highly recommends validating layout designs through simulations to ensure signal integrity is not compromised.

Standard via sizes that allow escape from a 0.8-mm pitch device can be used (i.e., 8-mil holes, 18-mil pads). Micro and/or blind/buried vias are neither required nor prohibited.

The PCB BGA pad requirements for the KeyStone II devices are documented in the *Flip Chip Ball Grid Array Package Reference Guide* (SPRU811). Most current KeyStone II DSPs are designed around a 0.8-mm ball pitch package and should follow the 0.8-mm guidelines. The PCB BGA pad requirements for the SerDes link partner device should follow its manufacturer's guidelines.

3.3 SerDes Interface General Routing Requirements

The approach for specifying suitable SerDes routing breaks the physical connection down into three component pieces:

- Receiver end
- Transmitter end
- Interconnect

The receiver and transmitter end are the pieces closest to the packages of the connected devices. The receiver end is connected to the SerDes input of the device and goes from the BGA pads to the AC-coupling capacitors. The transmitter end is connected to the SerDes output of the device and is simply the BGA escape paths for the differential pairs. The interconnect joins the receiver and transmitter ends.

NOTE: The PCIe standard recommends that the AC-coupling capacitors be close to the transmitter end and not the receiver end.

3.3.1 Receiver End

For the receiver end, it is strongly recommended to route the trace from the BGA pad to the capacitor pad on the top layer. This avoids a via escape between the BGA pad and the capacitor. On the other side of the capacitor, it is recommended to via to another layer. The trace widths and separation should be altered based on the board stack up to meet the 100-Ω differential impedance requirement. Traces may be necked down to escape the BGA, if necessary, but this length must be minimized.

3.3.2 Transmitter End

The transmitter end should use standard via escapes to internal layers. Internal layers are recommended for their superior shielding characteristics. The trace widths and separation should be selected based on the board stack up to meet the 100-Ω differential impedance requirement. Traces may be necked down to escape the BGA, if necessary, but this length must be minimized.

3.3.3 Interconnect Guidelines - General

The geometry of the traces to link the transmitter and receiver ends is determined by the placement in the target system and any board-to-board connections. The trace can be placed as required, as long as it meets the following requirements:

- Edge-coupled, matched-length differential pair
- No stubs
- The areas where desired differential pair separation cannot be maintained (connections to devices or connectors) are kept to an absolute minimum
- No routing across split planes in the neighboring reference plane
- Maintain uniform separation between complementary pairs for the entire trace length
- Whenever possible, use the majority of via length to transfer signal layers in order to avoid via stubs (back drill vias where possible to remove via stubs)
- Like pair traces must be at least 20 mils apart and unlike pair traces must be at least 30 mils apart. Tighter layouts should use simulations to validate that crosstalk is not an issue.
- SerDes routing must be adjacent to a ground reference plane
- If connectors are used, they must be of a suitable 100-Ω differential-impedance, high-speed type, and count as a minimum of 1" of trace for each connector pair (simulation and modeling is strongly recommended).

3.4 Connectors (Optional)

Any connectors used must be of the controlled-impedance type (50-Ω single ended or 100-Ω differential) and suitable for microwave transmissions. Suitable connectors are typically categorized as backplane type connectors. The connectors should have less than 1-dB insertion loss below 6 GHz. Some suggested connectors are:

- CN074 - AMC Connector
- Tyco Z-DO
- Tyco Z-PAK HM Z

3.4.1 Cabling (Optional)

Any cabling used must be of the controlled-impedance type (50-Ω single ended or 100-Ω differential) and suitable for microwave transmissions. Recommended cable types are listed below:

- 50-Ω Coaxial - commonly used with SMA connectors:
  - RG142
  - RG316
  - RG178
- Infiniband - assembled cables available in 1× and 4× widths

3.4.2 Power Supply Requirements

The power supply and bypassing requirements for SerDes power planes are documented as part of the *KeyStone II Hardware Design Guide*, see Related Documentation from Texas Instruments.

It is best to use power plane islands to connect the power supply from the filters to the pins. However, traces that are at least 20 mils wide can also be used to access the inner BGA pads.

AIF Interface

The enhanced Antenna Interface subsystem (AIF2) on KeyStone II devices consists of the Antenna Interface module and two SerDes macros. This is a six-lane SerDes interface designed to operate at up to 6.144 GBaud per lane from pin to pin. The AIF2 relies on the performance SerDes macro along with a logic layer for the OBSAI RP3 and CPRI protocols. The AIF is used to connect to the backplane for transmission and reception of antenna data, as well as to connect to additional device peripherals.

For more details on the AIF interface, see the device-specific data manuals. Specifications supported, interface specific PCB routing recommendations, and SerDes device settings accessible by register accesses are covered in later sections of this document.

Topic **Page**

4.1 Relevant Industry Standard Specification Support

Existing standards guide the parameters for the AC electrical specifications for OBSAI support. For line rates up to 3072 MBaud, the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002 is used. For the 6144-MBaud line rate, the references are OIF-CEI-02.0 Interoperability Agreement with its section 7 and related clauses and the Serial RapidIO v2 PHY specifications, which are also based on the OIF agreement, to be adapted to the specific needs in OBSAI. OBSAI support includes the interconnects that are in compliance with TYPE 1, TYPE 2, TYPE 3, TYPE 4, and TYPE 5 interconnects as specified in Chapter 5 of OBSAI RP3 Rev 4.2 Specification.

Two electrical variants of CPRI supported are LV:XAUI-based and LV-II:CEI-6G-LR-based. The LV variant is guided by IEEE 802.3-2005 clause 47 (XAUI), but with a lower bit rate. The LV-II variant is guided by OIF-CEI-02.0, clause 7, but with a lower bit rate. Table 4-1 summarizes the line rates and electrical standards supported on the CPRI interface as specified in Chapter 4 of the CPRI Interface Specification V5.0.

Table 4-1. CPRI Physical Layer Modes supported by AIF2

Line Bit Rate	Electrical Standard	LV:XAUI	LV-II:CEI-6G-LR
614.4 Mbit/s	E.6	Supported	Supported
1228.8 Mbit/s	E.12	Supported	Supported
2457.6 Mbit/s	E.24	Supported	Supported
3072.0 Mbit/s	E.30	Supported	Supported
4915.2 Mbit/s	E.48	Not applicable	Supported
6144.0 Mbit/s	E.60	Not applicable	Supported

4.2 Recommended SerDes PCB Layout Constraints

Routing requirements for the AIF (RP3) interface must adhere to good engineering practices for transmission lines. Specific attention must be paid to net classes within this group and should have a high routing priority. The device incorporates SerDes outputs, which typically connect directly to the antenna interface (through a back plane) or between devices (for serial and parallel processing).

- Each complementary device SerDes receive pair must be individually skew-matched to within 1 ps (absolute maximum). 1 ps equates to approximately 5.5 mils to 7.1 mils (depending on propagation delays). Example of AIF complementary pairs include AIFRXN0 and AIFRXP0.
- Each complementary device SerDes receive pairs must be routed on the same layer.
- Each complementary device SerDes transmit pairs must be skew-matched to within 1 ps (absolute maximum). 1 ps equates to approximately 5.5 mils to 7.1 mils (depending on propagation delays). Example of complementary SerDes pairs include: AIFTXN0 and AIFTXP0.
- Each complementary device SerDes transmit pairs must be routed on the same layer.
- All complementary device receive pairs (AIFRXN/P5:0) must be assigned to an individual net class and routing skew must not be greater than 100 ps between all receive pairs.
- All complementary device transmit pairs (AIFTXN/P5:0) must be assigned to an individual net class and routing skew must not be greater than 100 ps between all transmit pairs.
- Transmit and receive signals must be referenced to parallel ground planes.
- Vias are allowed and should never exceed four per net, all nets must be balanced and the impact of the via on timing and loading taken into account during design and layout.
- Differential signal routing must achieve a 100-Ω differential impedance.

4.3 Recommended SerDes Register Configuration Options

The AIF interface is made up of two macro instances: PHY-A, 4 Lanes (B8) and PHY-A, 2 Lane (B4).

Configuration of this PHY interface is handled through the driver code provided in the TI Multicore Software Development Kit (MCSDK) and Chip Support Library (CSL). The interface is enabled by first loading a TI generated and supported configuration that sets the config baud rate, reference clock, bit width, and common lane parameters needed for the desired operating mode. The lane rate to be used is then configured by the user by setting either 1x Rate, 1/2x Rate, or 1/4 Rate, although all rate settings may not be available for a given configuration. The configurations supported are listed below in Table 4-2. Other configurations may exist outside of this list, please consult the TI MCSDK for the latest configuration list.

Table 4-2. AIF2 Configurations supported by TI MCSDK / CSL

Config Baud Rate	1X Rate (Gbps)	1/2X Rate (Gbps)	1/4X Rate (Gbps)	Ref Clock (MHz)	Bit Width
4.9152 Gbps	4.9152	-(1)	-	122.88	20
4.9152 Gbps	4.9152	-	-	153.6	20
4.9152 Gbps	4.9152	-	-	307.2	20
6.144 Gbps	6.144	-	-	122.88	20
6.144 Gbps	6.144	-	-	153.6	20
6.144 Gbps	6.144	-	-	307.2	20

(1) Indicates that the rate is NOT supported

For details on AIF Interface configuration registers definitions and settings, see the *KeyStone Architecture Antenna Interface 2 (AIF2) User Guide* (SPRUGV7).

For the complete suite of configuration examples on this interface, see the TI Multicore Software Development Kit (MCSDK).

NOTE: TI requires customers to use TI-generated and supported, default PHY configurations for all operating modes (supplied as part of MCSDK). TI cannot directly support customer generated configuration files. The code/registers used and accessed in these configurations must be considered as the "default" for a given interface use-case and must not be modified by a customer.

AIL Interface

The Antenna Interface Link subsystem (AIL) on KeyStone II devices consists of the Antenna Interface module and a single two-lane SerDes macro. This SerDes interface is designed to operate at up to 9.83Gbps per lane from pin to pin. The AIL relies on the performance SerDes macro along with a logic layer for the OBSAI RP3 and CPRI protocols. The AIL is used to connect to the switch fabric and hardware accelerators inside the SoC for transmission and reception of antenna data.

For more details on the AIL interface, see the device-specific data manuals. Specifications supported, interface specific PCB routing recommendations, and SerDes device settings accessible by register accesses are covered in later sections of this document.

Topic **Page**

5.1 Relevant Industry Standard Specification Support

Existing standards guide the parameters for the AC electrical specifications for OBSAI support. For line rates up to 3072 MBaud, the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002 is used. For rates between 3072MBaud and 6144 MBaud line rate, the references are OIF-CEI-02.0 Interoperability Agreement with its section 7 and related clauses and the Serial RapidIO v2 PHY specifications, which are also based on the OIF agreement, to be adapted to the specific needs in OBSAI. OBSAI support includes the interconnects that are in compliance with TYPE 1, TYPE 2, TYPE 3, TYPE 4, and TYPE 5 interconnects as specified in Chapter 5 of OBSAI RP3 Rev 4.2 Specification.

Four electrical variants are recommended for CPRI usage, denoted HV (high voltage), LV (low voltage), LV-II (low voltage II) and LV-III (low voltage III) by the CPRI specification v5.0. The HV variant is guided by IEEE 802.3-2005, clause 39 (1000base-CX) but with 100 ohm impedance. The LV variant is guided by IEEE 802.3-2005 clause 47 (XAUI) but with lower bit rate. The LV-II variant is guided by OIF-CEI-02.0, clause 7, but with lower bit rate. The LV-III variant is guided by IEEE 802.3, clause 72.7 and 72.8 (10GBase-KR). See below for a summary of the supported physical layer modes and their corresponding electrical standards.

Table 5-1. CPRI Physical Layer Modes supported by AIL

Line Bit Rate	Electrical Standard	Electrical Variant / Guiding Specification
614.4 Mbit/s	E.6	HV: CX
1228.8 Mbit/s	E.12	HV: CX
2457.6 Mbit/s	E.24	LV: XAUI
3072.0 Mbit/s	E.30	LV: XAUI
4915.2 Mbit/s	E.48	LV-II: CEI-6G-LR
6144.0 Mbit/s	E.60	LV-II: CEI-6G-LR
9830.4 Mbit/s	E.96	LV-III: 10GBase-KR

5.2 Recommended SerDes PCB Layout Constraints

Routing requirements for the AIL interface must adhere to good engineering practices for transmission lines. Specific attention must be paid to net classes within this group and should have a high routing priority. The device incorporates SerDes outputs, which typically connect directly to the antenna interface (through a back plane) or between devices (for serial and parallel processing).

- Each complementary device SerDes receive pair must be individually skew-matched to within 1 ps (absolute maximum). 1 ps equates to approximately 5.5 mils to 7.1 mils (depending on propagation delays). Example of AIL complementary pairs include SHARED_SERDES_0_RXN0 and SHARED_SERDES_0_RXP0.
- Each complementary device SerDes receive pairs must be routed on the same layer.
- Each complementary device SerDes transmit pairs must be skew-matched to within 1 ps (absolute maximum). 1 ps equates to approximately 5.5 mils to 7.1 mils (depending on propagation delays). Example of complementary SerDes pairs include: SHARED_SERDES_0_TXN0 and SHARED_SERDES_0_TXP0.
- Each complementary device SerDes transmit pairs must be routed on the same layer.
- All complementary device receive pairs (SHARED_SERDES_0_RXN/P1:0) must be assigned to an individual net class and routing skew must not be greater than 100 ps between all receive pairs.
- All complementary device transmit pairs (SHARED_SERDES_0_TXN/P1:0) must be assigned to an individual net class and routing skew must not be greater than 100 ps between all transmit pairs.
- Transmit and receive signals must be referenced to parallel ground planes.
- Differential signal routing must achieve a 100-Ω differential impedance.
- Routing shall take into account propagation delays between microstrip and strip line topologies.
- To prevent crosstalk in a simple board stackup, TI recommends that the differential receive pairs be routed as a microstrip (outer layer) on one side of the board, and the differential transmit pairs be routed as a microstrip (outer layer) on the other side of the board.

- Up to two vias (absolute maximum) are allowed, but there must be no stub and the differential nature of the circuit must be maintained. This forces routing on the outer layers, unless blind via technologies or back-drilling are used.
- If a via is implemented, an adjacent ground via will be implemented to minimize the discontinuity.
- Clear ground plane under capacitor pads to reduce impedance discontinuity.
- All vias must have an adjacent ground via.
- There should be no non-functional annular rings on vias.
- Make anti-pad around vias as large as possible.
- Offset routes to avoid impedance offsets by FR4 fiber weave.

5.3 Recommended SerDes Register Configuration Options

The AIL interface is made up of a single two-lane PHY-A macro instance that is shared/multiplexed with the JESD interface.

Configuration of this PHY interface is handled through the driver code provided in the TI Multicore Software Development Kit (MCSDK) and Chip Support Library (CSL). The interface is enabled by first loading a TI generated and supported configuration that sets the config baud rate, reference clock, bit width, and common lane parameters needed for the desired operating mode. The lane rate to be used is then configured by the user by setting either 1x Rate, 1/2x Rate, or 1/4 Rate, although all rate settings may not be available for a given configuration. The configurations supported are listed below in Table 5-2. Other configurations may exist outside of this list, please consult the TI MCSDK for the latest configuration list.

Table 5-2. AIL Configurations supported by TI MCSDK / CSL

Config Baud Rate	1X Rate (Gbps)	1/2X Rate (Gbps)	1/4X Rate (Gbps)	Ref Clock (MHz)	Bit Width
4.9152 Gbps	4.9152	-(1)	-	122.88	20
4.9152 Gbps	4.9152	-	-	153.6	20
4.9152 Gbps	4.9152	-	-	307.2	20
6.144 Gbps	6.144	-	-	122.88	20
6.144 Gbps	6.144	-	-	153.6	20
6.144 Gbps	6.144	-	-	307.2	20
9.8304 Gbps	9.8304	-	-	122.88	20

(1) Indicates that the rate is NOT supported

For details on AIL Interface configuration registers definitions and settings, see the *KeyStone Architecture Antenna Interface 2 (AIF2) User Guide* (SPRUGV7).

NOTE: TI requires customers to use TI-generated and supported, default PHY configurations for all operating modes (supplied as part of MCSDK). TI cannot directly support customer generated configuration files. The code/registers used and accessed in these configurations must be considered as the "default" for a given interface use-case and must not be modified by a customer.

JESD204A/B Interface

The JESD204A/B interface on KeyStone II devices consists of two two-lane SerDes macros. This SerDes interface is designed to operate at up to 7.37Gbps per lane from pin to pin. The protocol and electrical performance of the interface is defined by the JEDEC JESD204B and JESD204A standards. The JESD204A/B interface is used as a physical link to the Digital Front End (DFE) peripheral used for digital radio signal processing, and provides a means for data converters to send or receive data out/in of a Keystone II device..

For more details on the JESD204A/B interface, see the device-specific data manuals. Specifications supported, interface specific PCB routing recommendations, and SerDes device settings accessible by register accesses are covered in later sections of this document.

Topic **Page**

6.1 Relevant Industry Standard Specification Support

6.2 Recommended SerDes PCB Layout Constraints

Routing requirements for the JESD204A/B interface must adhere to good engineering practices for transmission lines. Specific attention must be paid to net classes within this group and should have a high routing priority. The device incorporates SerDes outputs, which typically connect directly to the antenna interface (through a back plane) or between devices (for serial and parallel processing).

- Each complementary device SerDes receive pair must be individually skew-matched to within 1 ps (absolute maximum). 1 ps equates to approximately 5.5 mils to 7.1 mils (depending on propagation delays). Example of JESD complementary pairs include SHARED_SERDES_1_RXN0 and SHARED_SERDES_1_RXP0.
- Each complementary device SerDes receive pairs must be routed on the same layer.
- Each complementary device SerDes transmit pairs must be skew-matched to within 1 ps (absolute maximum). 1 ps equates to approximately 5.5 mils to 7.1 mils (depending on propagation delays). Example of complementary SerDes pairs include: SHARED_SERDES_1_TXN0 and SHARED_SERDES_1_TXN0.
- Each complementary device SerDes transmit pairs must be routed on the same layer.
- All complementary device receive pairs (SHARED_SERDES_1_RXN/P1:0) must be assigned to an individual net class and routing skew must not be greater than 100 ps between all receive pairs.
- All complementary device transmit pairs (SHARED_SERDES_1_TXN/P1:0) must be assigned to an individual net class and routing skew must not be greater than 100 ps between all transmit pairs.
- Transmit and receive signals must be referenced to parallel ground planes.
- Differential signal routing must achieve a 100-Ω differential impedance.
- Routing shall take into account propagation delays between microstrip and strip line topologies.
- To prevent crosstalk in a simple board stackup, TI recommends that the differential receive pairs be routed as a microstrip (outer layer) on one side of the board, and the differential transmit pairs be routed as a microstrip (outer layer) on the other side of the board.
- Up to two vias (absolute maximum) are allowed, but there must be no stub and the differential nature of the circuit must be maintained. This forces routing on the outer layers, unless blind via technologies or back-drilling are used.
- If a via is implemented, an adjacent ground via will be implemented to minimize the discontinuity.
- Clear ground plane under capacitor pads to reduce impedance discontinuity.
- All vias must have an adjacent ground via.
- There should be no non-functional annular rings on vias.
- Make anti-pad around vias as large as possible.
- Offset routes to avoid impedance offsets by FR4 fiber weave.

6.3 Recommended SerDes Register Configuration Options

The JESD204A/B interface is made up of 2x two-lane PHY-A macro instances, one of which is shared/multiplexed with the AIL interface.

Configuration of this PHY interface is handled through the driver code provided in the TI Multicore Software Development Kit (MCSDK) and Chip Support Library (CSL). The interface is enabled by first loading a TI generated and supported configuration that sets the config baud rate, reference clock, bit width, and common lane parameters needed for the desired operating mode. The lane rate to be used is then configured by the user by setting either 1x Rate, 1/2x Rate, or 1/4 Rate, although all rate settings may not be available for a given configuration. The configurations supported are listed below in Table 6-1. Other configurations may exist outside of this list, please consult the TI MCSDK for the latest configuration list.

Table 6-1. JESD204A/B Configurations supported by TI MCSDK / CSL

Config Baud Rate	1X Rate (Gbps)	1/2X Rate (Gbps)	1/4X Rate (Gbps)	Ref Clock (MHz)	Bit Width
6.144 Gbps	6.144	3.072	-(1)	122.88	20
6.144 Gbps	6.144	3.072	-	153.6	20
7.3728 Gbps	7.3728	3.6864	-	122.88	20
9.8304 Gbps	-	4.9152	2.4576	122.88	20

(1) Indicates that the rate is NOT supported

For details on AIL Interface configuration registers definitions and settings, see the *KeyStone Architecture Antenna Interface 2 (AIF2) User Guide* (SPRUGV7).

NOTE: TI requires customers to use TI-generated and supported, default PHY configurations for all operating modes (supplied as part of MCSDK). TI cannot directly support customer generated configuration files. The code/registers used and accessed in these configurations must be considered as the "default" for a given interface use-case and must not be modified by a customer.

SRIO Interface

The SRIO port on the KeyStone II device is a high-performance, low pin-count SerDes interconnect. This is a four-lane SerDes interface designed to operate up to 5 GBaud per lane from pin to pin. RapidIO is based on the memory and device addressing concepts of processor buses in which the transaction processing is managed completely by hardware.

For more details on the SRIO interface, see the device-specific data manuals. Specifications supported, interface specific PCB routing recommendations, and SerDes device settings accessible by register accesses are covered in later sections of this document.

Topic **Page**

7.1 Relevant Industry Standard Specification Support

The XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002 guides the LP-Serial 1.25 GBaud, 2.5 GBaud, and 3.125 GBaud Electrical specifications. The LP-Serial 5-GBaud Electrical specifications are based upon the Optical Internetworking Forum's Common Electrical Interface CEI. The SRIO interface shall support 1.25 GBaud, 2.5 GBaud, or 3.125 GBaud rates on Level I links and 5 GBaud rates on Level II links as described in Chapter 8 of RapidIO Interconnect Specification Part 6: LP-Serial Physical Layer Specification Rev. 2.1.

7.2 Recommended SerDes PCB Layout Constraints

Routing requirements for the SRIO interface to the device shall adhere to good engineering practices for transmission lines. Specific attention shall be paid to net classes within this group and should have a high routing priority.

- Each complementary SRIO SerDes receive pair shall be individually skew-matched to within 1 ps. 1 ps equates to approximately 5.464 mils to 7.092 mils (depending on propagation delays). Example of the SRIO complementary pairs include RIORXN0 & RIORXP0.
- Each complementary device SerDes receive pairs must be routed on the same layer.
- Each complementary SRIO SerDes transmit pair shall be individually skew-matched to within 1 ps. 1 ps equates to approximately 5.464 mils to 7.092 mils (depending on propagation delays). Example of the SRIO complementary pairs include RIOTXN0 & RIOTXP0.
- Each complementary device SerDes transmit pairs must be routed on the same layer.
- All four complementary receive pairs RIORXN/P3:0 shall be assigned and routed as an individual net class, routing skew shall not be greater than 100 ps between all receive pairs. (The full link budget is 3UI so lane to lane skew can be larger if additional link analysis is completed.)
- All four complementary transmit pairs RIOTXN/P3:0 shall be assigned and routed as an individual net class, routing skew shall not be greater than 100 ps between all transmit pairs. (The full link budget is 3UI so lane to lane skew can be larger if additional link analysis is completed.)
- Transmit and receive signals must be referenced to parallel ground planes.
- Vias are allowed and should never exceed four per complete net. All nets must be balanced and the impact of the via on timing and loading taken into account during design and layout.
- Differential signal routing must achieve a 100-Ω differential impedance.
- If an SRIO switch is used, the specific routing and timing requirements shall also be incorporated.

7.3 Recommended SerDes Register Configuration Options

The SRIO interface is made up of a single 4-lane PHY-A macro instance. Configuration of this PHY interface is handled through the driver code provided in the TI Multicore Software Development Kit (MCSDK) and Chip Support Library (CSL). The interface is enabled by first loading a TI generated and supported configuration that sets the config baud rate, reference clock, bit width, and common lane parameters needed for the desired operating mode. The lane rate to be used is then configured by the user by setting either 1x Rate, 1/2x Rate, or 1/4 Rate, although all rate settings may not be available for a given configuration. The configurations supported are listed below in Table 7-1. Other configurations may exist outside of this list, please consult the TI MCSDK for the latest configuration list.

Table 7-1. SRIO Configurations Supported by TI MCSDK / CSL

Config Baud Rate	1X Rate (Gbps)	1/2X Rate (Gbps)	1/4X Rate (Gbps)	Ref Clock (MHz)	Bit Width
5.0 Gbps	5.0	2.5	1.25	125	20
5.0 Gbps	5.0	2.5	1.25	156.25	20
6.25 Gbps	-(1)	3.125	-	125	20
6.25 Gbps	-	3.125	-	156.25	20

(1) Indicates that the rate is NOT supported

For details on SRIO SerDes configuration registers definitions and settings, see the *KeyStone Architecture SRIO User Guide* (SPRUGW1).

NOTE: TI requires customers to use TI-generated and supported, default PHY configurations for all operating modes (supplied as part of MCSDK). TI cannot directly support customer generated configuration files. The code/registers used and accessed in these configurations must be considered as the "default" for a given interface use-case and must not be modified by a customer.

HyperLink Interface

KeyStone II devices include a HyperLink interface for companion chip/die connections. This is a four-lane SerDes interface designed to operate up to 12.5 GBaud per lane from pin to pin. The interface is used to connect with external accelerators that are manufactured using TI libraries. HyperLink includes the data signals and the sideband control signals. The data signals are SerDes-based and the sideband control signals are LVCMOS-based. The current version of HyperLink offers point-to-point connection between two devices.

For more details on HyperLink interface, see the device specific-data manual. Specifications supported, interface specific PCB routing recommendations, and SerDes device settings accessible by register accesses are covered in later sections of this document.

Topic **Page**

8.1 Relevant Industry Standard Specification Support

HyperLink is a Texas Instruments Interface that provides a high-speed, low-latency, and low-pin-count communication interface between two KeyStone II devices. For more details, see the *HyperLink Users Guide* in Related Documentation from Texas Instruments

8.2 Recommended SerDes PCB Layout Constraints

- Each complementary device receive pair shall be individually skew matched to within 1 ps (absolute maximum). 1 ps equates to approximately 5.5 mils to 7.1 mils (depending on propagation delays). An example of a differential pair is MCMRXN0 and MCMRXP0.
- Each complementary device SerDes receive pairs shall be routed on the same layer.
- Each complementary device transmit pair shall be individually skew matched to within 1 ps (absolute maximum). 1 ps equates to approximately 5.5 mils to 7.1 mils (depending on propagation delays). An example of a differential pair is MCMTXN0 and MCMTXP0.
- Each complementary device SerDes transmit pairs shall be routed on the same layer.
- All differential receive pairs MCMRXN/P3:0 shall be assigned to an individual net class and routing skew shall not be greater than 40ps (absolute maximum) for board-to-board configuration. (The full link budget is 2UI-20ps so lane to lane skew can be larger if additional link analysis is completed.)
- All differential transmit pairs MCMTXN/P3:0 shall be assigned to an individual net class and routing skew shall not be greater than 40ps (absolute maximum) for board-to-board configuration. (The full link budget is 2UI-20ps so lane to lane skew can be larger if additional link analysis is completed.)
- All differential pairs shall be < 4.0” (101.6 mm) in total length, recommended length is 2.00” (50.8 mm).
- The MCMRXFLCLK and MCMRXFLDAT nets shall be skew-matched within 250 ps (absolute maximum) of one another.
- The MCMTXFLCLK and MCMTXFLDAT nets shall be skew-matched within 250 ps (absolute maximum) of one another.
- The MCMRXPMCLK and MCMRXPMDAT nets shall be skew-matched within 250 ps (absolute maximum) of one another.
- The MCMTXPMCLK and MCMTXPMDAT nets shall be skew-matched within 250 ps (absolute maximum) of one another.
- Transmit and receive signals must be referenced to continuous, parallel ground planes.
- Differential signal routing must achieve 100-Ω differential impedance.
- Routing shall take into account propagation delays between microstrip and strip line topologies.
- To prevent crosstalk in a simple board stackup, it is recommended that the differential receive pairs be routed as a microstrip (outer layer) on one side of the board and the differential transmit pairs be routed as a microstrip (outer layer) on the other side of the board.
- Up to two vias (absolute maximum) are allowed but there must be no stub and the differential nature of the circuit must be maintained. This forces routing on the outer layers unless blind via technologies or back-drilling are used.
- If a via is implemented, an adjacent ground via will be implemented to minimize the discontinuity.
- HyperLink lanes can be swapped to simplify routing. The differential pairing must be maintained.
- P and N connections for a single differential pair can be inverted to simplify routing.
- Use radial bends with a minimum radius of 5W (five times the width) instead of 45 and 90 degree trace bends
- Clear ground plane under capacitor pads to reduce impedance discontinuity
- Make sure all vias have an adjacent ground via
- Make sure there are no non-functional annular rings on vias
- Make anti-pad around vias as large as possible.
- Offset routes to avoid impedance offsets by FR4 fiber weave

CAUTION

Board layout simulation is a requirement for this class of circuit to validate the PCB routing.

8.3 Recommended SerDes Register Configuration Options

The Hyperlink interface is made up of a single 4-lane PHY-A macro instance. Configuration of this PHY interface is handled through the driver code provided in the TI Multicore Software Development Kit (MCSDK) and Chip Support Library (CSL). The interface is enabled by first loading a TI generated and supported configuration that sets the config baud rate, reference clock, bit width, and common lane parameters needed for the desired operating mode. The lane rate to be used is then configured by the user by setting either 1x Rate, 1/2x Rate, or 1/4 Rate, although all rate settings may not be available for a given configuration. The configurations supported are listed below in Table 8-1. Other configurations may exist outside of this list, please consult the TI MCSDK for the latest configuration list.

Table 8-1. Hyperlink Configurations supported by TI MCSDK / CSL

Config Baud Rate	1X Rate (Gbps)	1/2X Rate (Gbps)	1/4X Rate (Gbps)	Ref Clock (MHz)	Bit Width
5.0 Gbps	5.0	-(1)	-	156.25	20
5.0 Gbps	5.0	-	-	312.5	20
6.25 Gbps	6.25	3.125	-	156.25	20
6.25 Gbps	6.25	3.125	-	312.5	20
10.0 Gbps	10.0	-	-	156.25	20
10.0 Gbps	10.0	-	-	312.5	20
12.5 Gbps	12.5	-	-	156.25	20
12.5 Gbps	12.5	-	-	312.5	20

(1) Indicates that the rate is NOT supported

For details on HyperLink SerDes configuration registers definitions and settings, see the *KeyStone Architecture HyperLink User Guide*, in Related Documentation from Texas Instruments.

NOTE: TI requires customers to use TI-generated and supported, default PHY configurations for all operating modes (supplied as part of MCSDK). TI cannot directly support customer generated configuration files. The code/registers used and accessed in these configurations must be considered as the "default" for a given interface use-case and must not be modified by a customer.

SGMII Interface

The Gigabit Ethernet (GbE) switch subsystem on KeyStone II devices provides an efficient SGMII interface between the TI SoC and the networked community. The EMAC supports 10Base-T (10 Mbits/second [Mbps]), and 100BaseTX (100 Mbps), in half- or full-duplex mode, and 1000BaseT (1000 Mbps) in full-duplex mode, with hardware flow control and quality-of-service (QOS) support. The GbE switch subsystem is coupled with the network coprocessor.

For more details on GbE interface, see the device-specific data manuals. Specifications supported, interface specific PCB routing recommendations, and SerDes device settings, accessible by register accesses are covered in further sections of this document

Topic **Page**

9.1 Relevant Industry Standard Specification Support

The SGMII interface adheres with IEEE Standard for low-voltage differential signals (LVDS) for Scalable Coherent Interface (SCI) IEEE1596.3-1996.

9.2 Recommended SerDes PCB Layout Constraints

Routing requirements for the SGMII or Ethernet interface must adhere to good engineering practices for transmission lines operating at or above 1 GHz. Specific attention must be paid to net classes within this group and should have a high routing priority. The device incorporates SerDes outputs and requires the use of a PHY to interconnect to a standard RJ-45 connector.

- Each complementary device SerDes receive pair must be individually skew-matched to within 1 ps. 1 ps equates to approximately 5.5 mils to 7.1 mils (depending on propagation delays). Example of complementary pairs include SGMIIRXN0 and SGMIIRXP0.
- Each complementary device SerDes receive pairs must be routed on the same layer.
- Each complementary device SerDes transmit pairs must be skew-matched to within 1 ps. 1 ps equates to approximately 5.5 mils to 7.1 mils (depending on propagation delays). Example of complementary SerDes pairs include: SGMIITXN0 and SGMIITXP0.
- Each complementary device SerDes transmit pairs must be routed on the same layer.
- Transmit and receive signals must be referenced to parallel ground planes.
- Vias are allowed and all nets must be balanced and the impact of the via on timing and loading taken into account during design and layout.
- Differential signal routing must achieve a 100-Ω differential impedance.

9.3 Recommended SerDes Register Configuration Options

The SGMII interface is made up of a single 4-lane PHY-A macro instance. Configuration of this PHY interface is handled through the driver code provided in the TI Multicore Software Development Kit (MCSDK) and Chip Support Library (CSL). The interface is enabled by first loading a TI generated and supported configuration that sets the config baud rate, reference clock, bit width, and common lane parameters needed for the desired operating mode. The lane rate to be used is then configured by the user by setting either 1x Rate, 1/2x Rate, or 1/4 Rate, although all rate settings may not be available for a given configuration. The configurations supported are listed below in Table 9-1. Other configurations may exist outside of this list, please consult the TI MCSDK for the latest configuration list.

Table 9-1. SGMII Configurations supported by TI MCSDK / CSL

Config Baud Rate	1X Rate (Gbps)	1/2X Rate (Gbps)	1/4X Rate (Gbps)	Ref Clock (MHz)	Bit Width
5.0 Gbps	-(1)	-	1.25	125	10
5.0 Gbps	-	-	1.25	156.25	10
5.0 Gbps	-	-	1.25	312.5	10

(1) Indicates that the rate is NOT supported

For details on SGMII SerDes configuration registers, definitions and settings, see the *KeyStone Architecture GbE User Guide*, in Related Documentation from Texas Instruments.

NOTE: TI requires customers to use TI-generated and supported, default PHY configurations for all operating modes (supplied as part of MCSDK). TI cannot directly support customer generated configuration files. The code/registers used and accessed in these configurations must be considered as the "default" for a given interface use-case and must not be modified by a customer.

PCIe Interface

The PCI express (PCIe) module on KeyStone II devices provides an interface between the SoC and other PCIe-compliant devices. This is a two-lane SerDes interface designed to operate up to 5 GBaud per lane from pin to pin. The PCI express module provides a low pin count, high reliability, and high-speed data transfer at rates of 5.0 GBaud per lane on the serial links.

For more details on PCIe interface, see the device-specific data manual. Specifications supported, interface specific PCB routing recommendations, and SerDes device settings accessible by register accesses are covered in further sections of this document.

Topic **Page**

10.1 Relevant Industry Standard Specification Support

The PCIe interface on KeyStone II devices is compliant with Physical Layer Specifications referenced in Chapter 4 of the PCI Express Base Specification Revision 2.0.

10.2 Recommended SerDes PCB Layout Constraints

Routing requirements for the PCIe interface shall adhere to good engineering practices for transmission lines operating above 5 GHz. Specific attention shall be paid to net classes within this group and should have a high routing priority (if this interface is used).

- Each complementary PCIe SerDes receive pair shall be individually skew matched to within 1 ps. 1 ps equates to approximately 5.464 mils to 7.092 mils (depending on propagation delays). Example of complementary pairs include PCIERXN0 and PCIERXP0.
- Each complementary PCIe SerDes receive pairs shall be routed on the same layer.
- Each complementary PCIe SerDes transmit pair shall be individually skew matched to within 1 ps. 1 ps equates to approximately 5.464 mils to 7.092 mils (depending on propagation delays). Example of complementary pairs include PCIETXN0 and PCIETXP0.
- Each complementary PCIe SerDes transmit pairs shall be routed on the same layer.
- All complementary PCIe receive pairs PCIERXN/P1:0 shall be assigned to an individual net class where routing skew shall not be greater than 100 ps between all receive pairs. (The full link budget is 2UI+500ps so lane to lane skew can be larger if additional system analysis is completed.)
- All complementary PCIe transmit pairs PCIETXN/P1:0 shall be assigned to an individual net class and routing skew shall not be greater than 100 ps between all transmit pairs. (The full link budget is 2UI+500ps so lane to lane skew can be larger if additional system analysis is completed.)
- Transmit and receive signals must be referenced to parallel ground planes.
- Vias are allowed and should never exceed four per net, all nets must be balanced and the impact of the via on timing, reflections, and loading taken into account during design and layout. This interface should be modeled to assure functionality.
- Differential signal routing must achieve a 100-Ω differential impedance.

10.3 Recommended SerDes Register Configuration Options

The PCIe interface is made up of a single 2-lane PHY-A macro instance. Configuration of this PHY interface is handled through the driver code provided in the TI Multicore Software Development Kit (MCSDK) and Chip Support Library (CSL). The interface is enabled by first loading a TI generated and supported configuration that sets the config baud rate, reference clock, bit width, and common lane parameters needed for the desired operating mode. The lane rate to be used is then configured by the user by setting either 1x Rate, 1/2x Rate, or 1/4 Rate, although all rate settings may not be available for a given configuration. The configurations supported are listed below in Table 10-1. Other configurations may exist outside of this list, please consult the TI MCSDK for the latest configuration list.

Table 10-1. PCIe Configurations supported by TI MCSDK / CSL

Config Baud Rate	1X Rate (Gbps)	1/2X Rate (Gbps)	1/4X Rate (Gbps)	Ref Clock (MHz)	Bit Width
5.0 Gbps	5.0	2.5	-(1)	100	8

(1) Indicates that the rate is NOT supported

For details on PCIe SerDes configuration registers, definitions, and settings, see the *KeyStone Architecture PCIe User Guide*, in Related Documentation from Texas Instruments.

NOTE: TI requires customers to use TI-generated and supported, default PHY configurations for all operating modes (supplied as part of MCSDK). TI cannot directly support customer generated configuration files. The code/registers used and accessed in these configurations must be considered as the "default" for a given interface use-case and must not be modified by a customer.

Ten Gigabit Ethernet (10GbE) Interface

KeyStone II devices may includes a 3-port Ten Gigabit Ethernet Switch Subsystem that includes a standalone EMAC switch subsystem and a 2-lane SerDes macro. The 10 Gigabit Ethernet (10GbE) Subsystem purpose is to provide an interface to transfer data at both 10Gb/s and 1Gb/s between the host device and another connected device in compliance with the Ethernet protocol.

For more details on the 10-GbE interface, see the device specific-data manual. Specifications supported, interface specific PCB routing recommendations, SerDes device settings accessible by register accesses and are covered in later sections of this document.

Topic **Page**

11.1 Relevant Industry Standard Specification Support

The 10 Gigabit Ethernet subsystem conforms to the following industry standards:

- Supports IEEE 802.3 specification
  - 10GBASE-R (10G)
  - 10GBase-KR (802.3ap Clause 72) (10G)
  - 10/100/1000Base-T (1G)
- Supports IEEE 1588 (v2008) specification
- Electrical Interfaces
  - Supports XFI SFF INF-8077i spec (no SFP/SFP+) for 10Gb
  - Supports 10GBase-KR as defined in IEEE 802.3ap
  - Supports Serial-GMII (SGMII) Specification for 10/100/1000Mb

11.2 Recommended SerDes PCB Layout Constraints

- Each complementary device receive pair shall be individually skew matched to within 1 ps (absolute maximum). 1 ps equates to approximately 5.5 mils to 7.1 mils (depending on propagation delays). An example of a differential pair is XFIRXN0 & XFIRXP0.
- Each complementary device SerDes receive pairs shall be routed on the same layer.
- Each complementary device transmit pair shall be individually skew matched to within 1 ps (absolute maximum). 1 ps equates to approximately 5.5 mils to 7.1 mils (depending on propagation delays). An example of a differential pair is XFITXN0 & XFITXP0.
- Each complementary device SerDes transmit pairs shall be routed on the same layer.
- Transmit and receive signals must be referenced to continuous, parallel ground planes.
- Differential signal routing must achieve a 100-Ω differential impedance.
- Routing shall take into account propagation delays between microstrip and stripline topologies.
- To prevent crosstalk in a simple board stackup, it is recommended that the differential receive pairs be routed as microstrip (outer layer) on one side of the board and the differential transmit pairs be routed as microstrip (outer layer) on the other side of the board.
- Up to two vias (absolute maximum) are allowed but there must be no stub and the differential nature of the circuit must be maintained. This forces routing on the outer layers unless blind via technologies or back-drilling are used.
- If a via is implemented, an adjacent ground via will be implemented to minimize the discontinuity.
- No right angles are allowed on SerDes traces, the traces must be radiused.
- Clear ground plane under capacitor pads to reduce impedance discontinuity.
- All vias must have an adjacent ground via.
- There should be no non-functional annular rings on vias.
- Make anti-pad around vias as large as possible.
- Offset routes to avoid impedance offsets by FR4 fiber weave.

CAUTION

Board layout simulation is a requirement for this class of circuit to validate the PCB routing.

11.3 Recommended SerDes Register Configuration Options

The 10GbE interface is made up of a single 2-lane PHY-B macro instance. Configuration of this PHY interface is handled through the driver code provided in the TI Multicore Software Development Kit (MCSDK) and Chip Support Library (CSL). The interface is enabled by first loading a TI generated and supported configuration that sets the config baud rate, reference clock, bit width, and common lane parameters needed for the desired operating mode. The lane rate to be used is then configured by the user by setting either 1x Rate, 1/2x Rate, or 1/4 Rate, although all rate settings may not be available for a given configuration. The configurations supported are listed below in Table 11-1. Other configurations may exist outside of this list, please consult the TI MCSDK for the latest configuration list.

Table 11-1. 10GbE Configurations supported by TI MCSDK / CSL

Config Baud Rate	1X Rate (Gbps)	1/2X Rate (Gbps)	1/4X Rate (Gbps)	Ref Clock (MHz)	Bit Width
5.0 Gbps	-(1)	-	1.25	156.25	10
5.0 Gbps	-	-	1.25	312.5	10
10.3125 Gbps	10.3125	-	-	156.25	16
10.3125 Gbps	10.3125	-	-	312.5	16

(1) Indicates that the rate is NOT supported

For details on 10GbE SerDes configuration registers definitions and settings, see the *KeyStone Architecture 10GbE User Guide*, in Related Documentation from Texas Instruments.

NOTE: TI requires customers to use TI-generated and supported, default PHY configurations for all operating modes (supplied as part of MCSDK). TI cannot directly support customer generated configuration files. The code/registers used and accessed in these configurations must be considered as the "default" for a given interface use-case and must not be modified by a customer.

11.4 Support for 10GBase-KR through Firmware

The IEEE802.3ap 10GBase-KR specification includes provisions for a start-up protocol that must be supported by the 10GbE peripheral through the use of a firmware that is loaded into and executed by the SerDes. This start-up protocol provides support for auto-negotiation, link-training, and Forward Error Correction (FEC) as specified in IEEE802.3ap Clauses 73 and 74.

If a user wishes to make use of the start-up protocol, they must follow the initialization sequence for the 10G Firmware as provided by the TI MCSDK/CSL. Firmware is executed from an embedded microcontroller within the SerDes, and must be loaded and started by the user during initialization. The only setup requirement of the user is to input a series of flags from which the firmware will automatically determine how to handle the setup and configuration of the SerDes CMU and lanes.

Firmware is loaded and executed from a 64KB memory region shared between the SerDes and WIZ wrapper. This memory region is not a part of the SoC device memory map and as such is inaccessible by the device switch fabric. Alternatively, the user must utilize special WIZ registers as a window into the shared memory region. These registers allow the user to read from or write to the shared memory space and are described below:

- MEM_ADR - The Memory Address Register is used to direct the WIZ to the shared memory address to be read from or written to. Each address corresponds to a 32-bit word.
- MEM_DAT - The Memory Data Portal Register is used to read or write to the shared memory addressed by MEM_ADR. The data width is 32-bits.
- MEM_DATINC - The Memory Data Portal Increment Portal Register is used to read or write to the shared memory addressed by MEM_ADR. After reading or writing this register the MEM_ADR is auto-incremented.

Terminations

All SerDes-based interfaces must be AC-coupled. As long as the SerDes link partner uses CML logic, the AC-coupling capacitor is the only external termination required. For AC-coupling, the recommendation is to use an 0402 or smaller 0.1-µF ceramic capacitor placed closest to the receiver BGA for all SerDes interfaces except PCIe. For PCIe, the AC-coupling capacitor should be placed closest to the transmitter BGA. This should be the case for the Serial RapidIO because that standard calls for CML signals. The SGMII specification calls for low-voltage differential signaling (LVDS), so additional terminations may be required. The need for terminations is dependent on the internal terminations in the link partner device.

See *Clocking Design Guide for KeyStone Devices* in Related Documentation from Texas Instruments for recommendations on connecting two different clocking techniques together.

SerDes PLL Calibration

This section provides guidelines for calibrating the CMU and CDR PLL and also includes some background information on PLL functionality.

CAUTION

Users are advised to use TI-generated default SerDes configurations specific to each interface (supplied as part of MCSDK). TI cannot directly support customer generated configuration files.

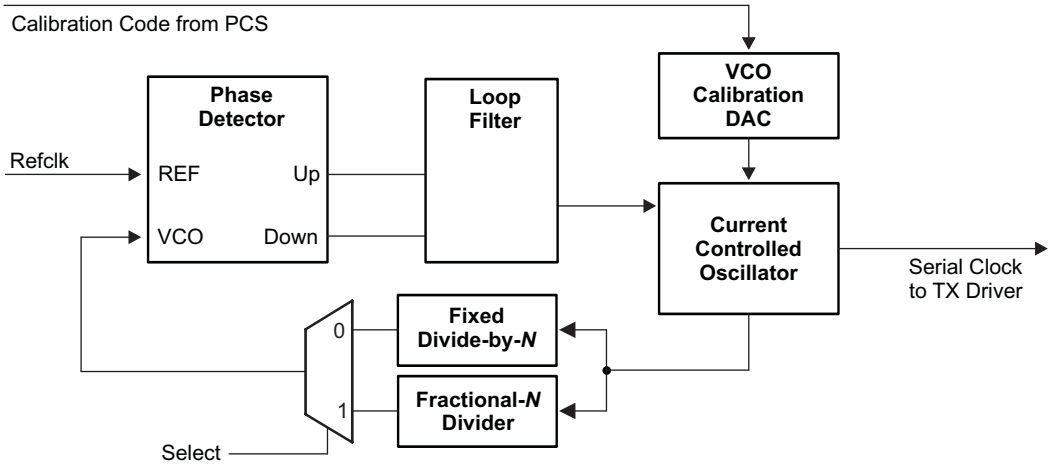
NOTE: Certain material in this chapter is reprinted with permission of Semtech Corporation – Snowbush IP Group © 2012

Topic **Page**

13.1 Introduction

Figure 13-1 shows a block diagram of the CMU PLL. It consists of a Phase detector, a loop filter and a DAC. VCO acts as a current-controlled oscillator, which sums currents from both these paths.

Figure 13-1. CMU PLL Block Diagram

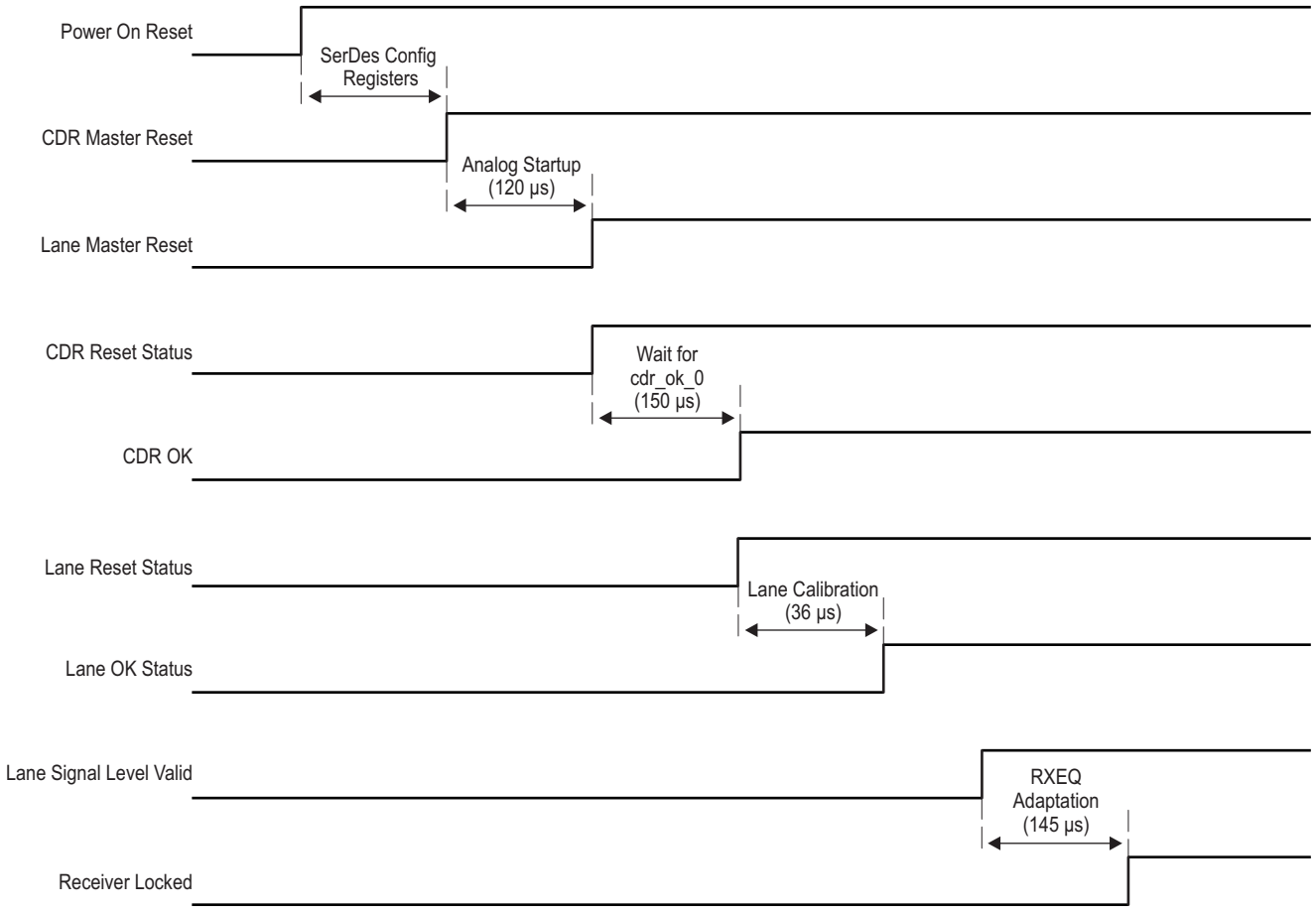


The CDR PLL design is very similar in functionality to the CMU PLL shown in Figure 13-1.

13.2 Calibrating CMU/CDR PLL Frequency

The CMU PLL frequency is calibrated during startup of the CMU and the CDR PLL is calibrated during the startup of the lanes. Figure 13-2 shows a diagram of the startup sequence for both CMU and CDR PLLs. The intent of this timing diagram is to ensure that customers get an understanding of the various events during a CMU/CDR PLL calibration phase. All the timing requirements mentioned in this figure are set and met by loading default SerDes configurations provided as part of the MCSDK package specific to each interface.

Figure 13-2. Startup Sequence Showing CMU/CDR PLL Calibration Phase



All supported reference clocks and lane rates specific to each interface are listed in their specific interface chapter in this document.

13.3 Programming CMU/CDR PLL Frequency

CMU/CDR PLL programming and frequency setting is handled entirely inside the TI-generated SerDes configuration files provided in the MCSDK. These configuration files are supplied directly by TI in order to maximize performance settings at the supported frequencies. To startup and calibrate the CMU and CDR PLLs, a user only needs to load the TI-generated SerDes configuration file using their application level code.

SerDes Transmitter Configuration

This section provides guidelines for configuring the SerDes Transmitter side of the SerDes Macro.

CAUTION

Users are advised to use TI-generated default SerDes configurations specific to each interface (supplied as part of MCSDK). TI cannot directly support customer generated configuration files.

NOTE: Certain material in this chapter is reprinted with permission of Semtech Corporation – Snowbush IP Group © 2012

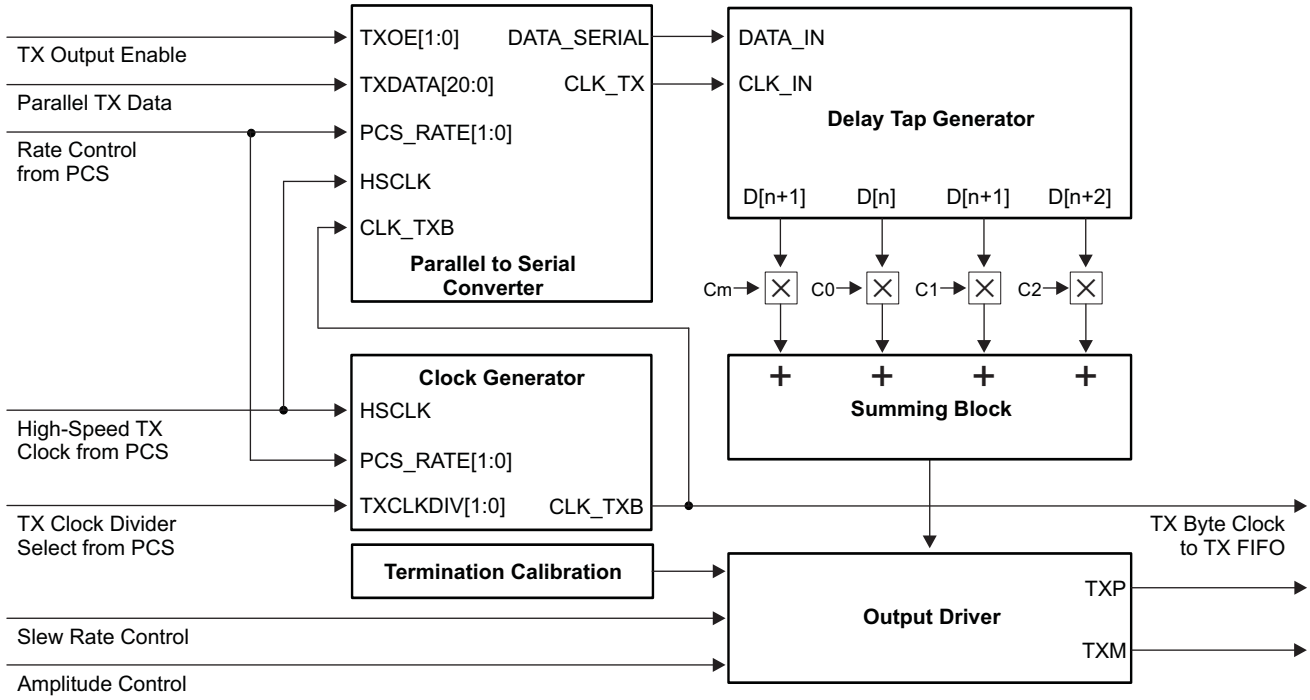
Topic **Page**

14.1 Introduction

This section provides guidelines on adjusting TX driver equalization and voltage amplitude levels in the KeyStone II SerDes PHY. The following sections include guidelines on equalization functions and register settings to adjust for a given equalization setting. Also, the method of adjusting TX driver amplitude levels is discussed along with register settings to use.

The SerDes IPs use a voltage-mode driver to drive high speed differential signals onto the transmission channel. A basic block diagram of the TX driver along with the parallel to serial converter is shown in Figure 14-1. The parallel data from the PCS layer is converted to serial data in the parallel-to-serial converter (P2S) block. The resulting serial data goes through a delay tap generator, which controls the feeding of serial data through the TX driver taps used to add equalization to the transmit signal. The output of all taps is summed and driven onto the transmission line.

Figure 14-1. TX Driver and P2S Converter Block Diagram



14.2 TX Driver Output Swing and Slew

14.2.1 Generic Mode

The TX driver output swing voltage and slew rates can be adjusted via register settings. Figure 14-2 shows a diagram of the output driver swing levels with different amounts of post and pre-cursor emphasis.

Figure 14-2. TX Driver Output Swing with Added Post and Pre-Cursor De-Emphasis

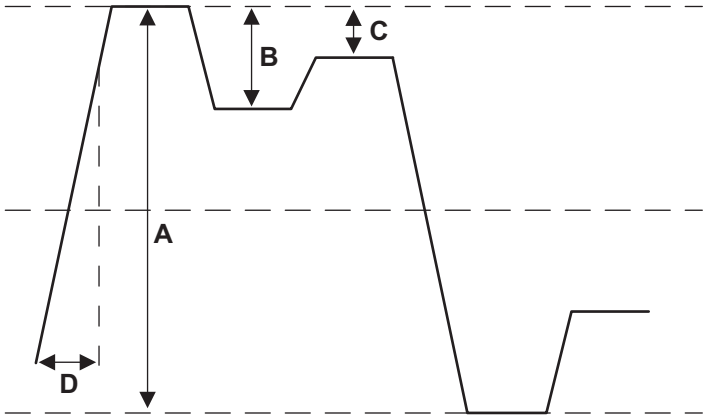


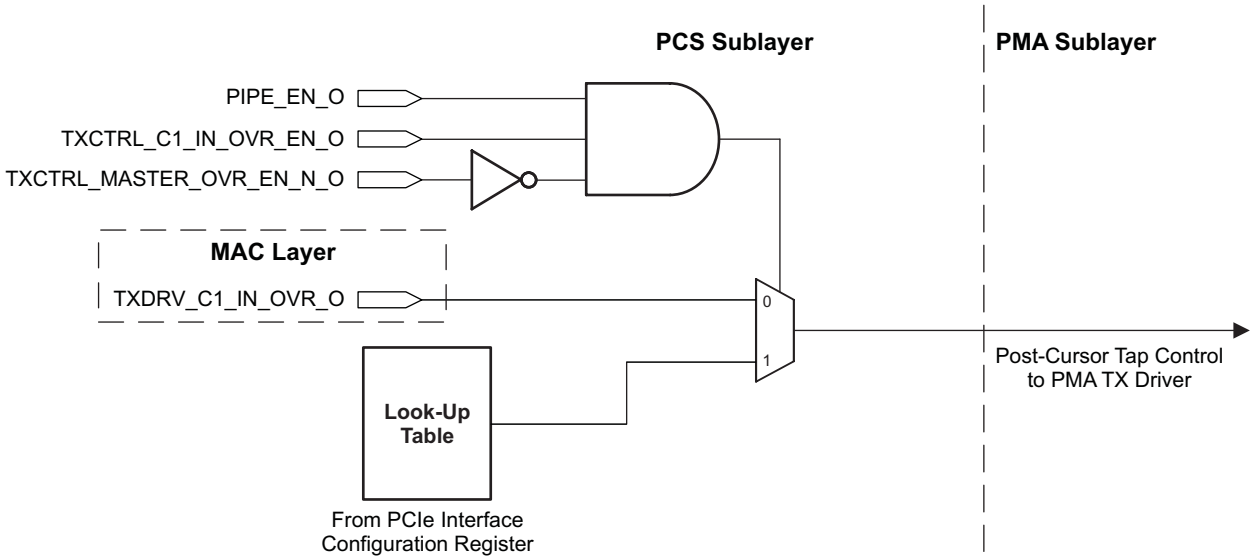
Table 14-1. TX Driver Output Swing with Added Post and Pre-Cursor De-Emphasis Registers

Parameter	Name	Description
A	Output swing level	Set by TXDRV_ATT_IN_OVR_O[3:0] and PMA_LN_TX_VREG_LEV_O[2:0]. TXDRV_ATT_IN_OVR_O[3:0] controls the number of voltage mode slices dedicated to driving output. Increasing this value increases the number of slices, thus increasing the output voltage swing. PMA_LN_TX_VREG_LEV_O[2:0] controls the regulator voltage output level that is fed to each slice.
B	Post-cursor de-emphasis	Set by TXDRV_C1_IN_OVR_O[4:0] The maximum output swing A is unaffected by this register setting. See Equalization section for more details.
C	Pre-cursor de-emphasis	Set by TXDRV_CM_IN_OVR_O[3:0] The maximum output swing A is unaffected by this register setting. See Equalization section for more details.
D	Slew rate	Slew rate settings are set by loading the default SerDes configuration that TI provides as part of the MCSDK package.

14.2.2 PCIe Mode

In PCIe mode, TX driver equalization and swing/slew settings are controlled by a Look-Up table (LUT). For any reason, if these setting need to be controlled through registers then the override enable (see Table 14-2) must be asserted. A block diagram of PCS functionality for the post-cursor tap C1 is shown in Figure 14-3. The controls for pre-cursor Cm, C2, TX driver slew settings, etc. are controlled in a similar manner.

Figure 14-3. TX Driver Settings for C1 Post Cursor De-Emphasis Control in PCIe Mode



The C1 setting that controls the TX driver post-cursor emphasis is controlled by a multiplexer that chooses the setting of register TXDRV_C1_IN_OVR_O in non-PCIe mode and chooses the LUT controlled by the MAC layer in PCIe mode. A full description of relevant registers in PHY-A is shown in Table 14-2.

Table 14-2. Register Descriptions for PCIe Mode TX Driver Slew, Equalization and Amplitude Settings

Register Signal	Address	Description
General Control		
PIPE_EN_O	ComLane_000	PCIe mode enable register signal. • 1 = Enable PCIe mode • 0 = Disable PCIe mode
TXCTRL_C1_IN_OVR_EN_O	Lane_0A0	Override enable for TX ctrl for c1 post-cursor emphasis in PCIe mode. • 1 = Enable PCIe lookup table mode • 0 = Disable PCIe lookup table mode
TXCTRL_MASTER_OVR_EN_N_O	Lane_0A8	Master override enable for TX ctrl in PCIe mode. • 1 = Disable PCIe lookup table mode for all TX driver settings • 0 = Enable PCIe lookup table mode for all TX driver settings

14.2.3 TX Driver Equalization

The SerDes interface features a highly programmable transmit equalization strategy to enable high data rate transfer over long channels. The 8/10/16/20 bit parallel data is serialized by the parallel to serial (P2S) block, using the high-speed transmit clock from the CMU PLL. The serialized data is then passed to the tap delay generator block, which generates four streams of serial data:

- D[n+1]: The *next* or pre-cursor bit in the data stream.
- D[n]: The *current* or cursor bit in the data stream.
- D[n-1]: The *last* or first post-cursor bit in the data stream.
- D[n-2]: The *delay by 2* or second post-cursor bit in the data stream.

These four data streams are then fed into a 4-tap FIR filter with coefficients Cm, C0, C1, and C2, implementing the following equation:

$$y(n) = c_m d_m + c_0 d_0 + c_1 d_1 + c_2 d_2 \quad (1)$$

where:

$$d_m = d(n + 1);\ d_0 = d(n);\ d_1 = d(n - 1);\ d_2 = d(n - 2) \quad (2)$$

The Cm, C0, C1, and C2 coefficients can be positive or negative, based on the lane control register bits PMA_LN_TXEQ_POLARITY[0], PMA_LN_TXEQ_POLARITY[1], PMA_LN_TXEQ_POLARITY[2], and PMA_LN_TXEQ_POLARITY[3] **,** respectively. It should also be noted that the following expression for these coefficients always applies:

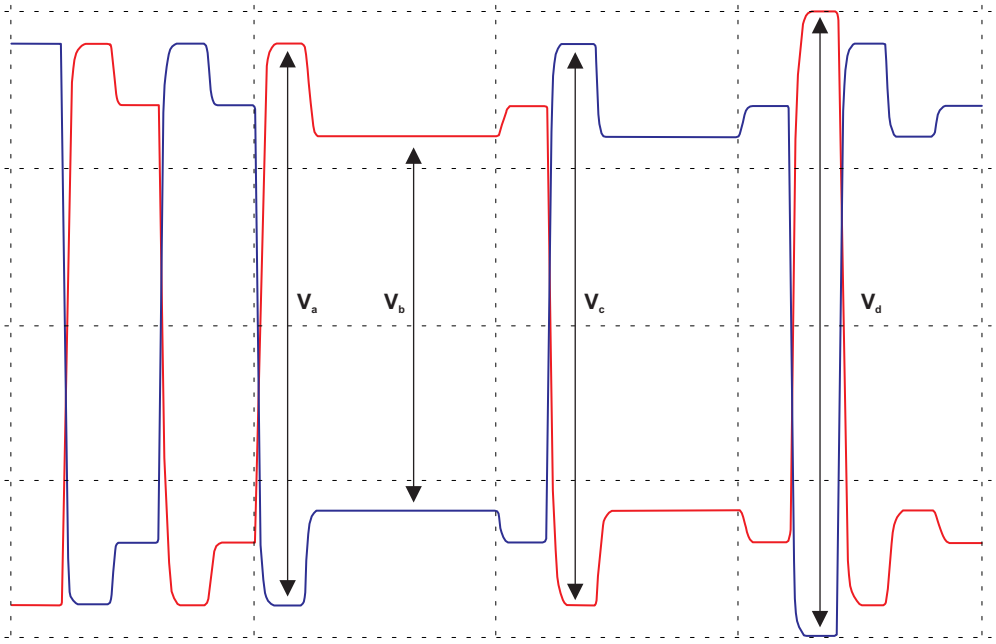
$$|c_m| + |c_0| + |c_1| + |c_2| = 1 \quad (3)$$

As the values of any of Cm, C1, or C2 are increased, C0 is automatically decreased to maintain this equality.

The three tap coefficients are provided as three registers: TXDRV_C1_IN_OVR_O[4:0], TXDRV_C2_IN_OVR_O [3:0] and TXDRV_CM_IN_OVR[:0], and are assumed to be normalized such that the TX coefficient space FS (full scale) = 36. The tap coefficients are constrained such that $C_m + C_0 + C_1 = 1$. This constraint is enforced by ignoring C0 and inferring its value from the Cm and C1. The equalization ratios implemented by the transmitter can be calculated from the PCIe tap-coefficients in PCIe mode or register settings in generic mode.

These ratios are computed based on the voltage levels defined in Figure 14-4.

Figure 14-4. Definition of TX Voltage Levels and Equalization Ratios



de-emphasis = $20\log_{10}(V_b/V_a)$

preshoot = $20\log_{10}(V_c/V_b)$

boost = $20\log_{10}(V_d/V_b)$

Normalize the transmitter output so the maximum pulse amplitude (V_d) equals 1.0. Then the other pulse amplitudes can be calculated as:

$V_a = C_0 - C_m + C_1$

$V_b = C_0 - C_m - C_1$

$V_c = C_0 + C_m - C_1$

Where the coefficients are real numbers, when using TX coefficient space FS (full scale) = 36, divide by 36.

Example 14-1. Cm = 4, C0 = 25, C1 = 7

$V_a = C_0 - C_m + C_1 = 28$

$V_b = C_0 - C_m - C_1 = 14$

$V_c = C_0 + C_m - C_1 = 22$

preshoot = $20\log_{10}(22/14) = 3.9$ dB

de-emphasis = $20\log_{10}(14/28) = -6$ dB

14.2.4 TX Driver Register Settings for PHY-A/PHY-B

Table 14-3 shows a list of important registers for the TX driver for PHY-A. Included are signal names, addresses, and a brief description of functionality.

Table 14-3. TX Driver Register Signals for PHY-A

Register Signal	Address	Description	
Amplitude			
TXDRV_ATT_IN_OVR_O[3:0]	Lane_004	Selects attenuator setting for TX driver (binary coded). Increasing this register value increases the transmitter amplitude. The attenuator register works by setting slices to drive out fixed 0s, therefore reducing output amplitude.	
PMA_LN_TX_VREG_LEV_O[2:0]	Lane_084	Selects regulator voltage setting for TX driver slices. Transmit voltage increases with increase in register setting as follows:	
		Register Value	**Regulator Output**
		000	0.75
		001	0.8
		010	0.85
		011	0.9
		100	0.95
		101	1
		110	1.05
		111	1.1
		Note: PMA_LN_TX_VREG_LEV setting should not be set higher than 0.95 V for long-term reliability reasons.	
Equalization			
TXDRV_CM_IN_OVR_O[3:0]	Lane_008	Selects magnitude of the Cm1 equalization tap (binary coded). Increasing the value of this register increases the magnitude of the tap. The polarity of this tap is set with the PMA_LN_TXEQ_POLARITY[0] register bit. Valid Settings: • TXDRV_PREEM_1LSB_MODE_0_OVR_O = 0: 0x0 to 0x7 • TXDRV_PREEM_1LSB_MODE_0_OVR_O = 1: 0x0 to 0xD	
TXDRV_C1_IN_OVR_0[4:0]	Lane_008	Selects magnitude of the C1 equalization tap (binary coded). Increasing the value of this register increases the magnitude of the tap. The polarity of this tap is set with the PMA_LN_TXEQ_POLARITY[2] register bit. Valid Settings: • TXDRV_PREEM_1LSB_MODE_0_OVR_O = 0: 0x0 to 0xF • TXDRV_PREEM_1LSB_MODE_0_OVR_O = 1: 0x0 to 0x17	
TXDRV_C2_IN_OVR_O[3:0]	Lane_008	Selects magnitude of the C2 equalization tap (binary coded). Increasing the value of this register increases the magnitude of the tap. The polarity of this tap is set with the PMA_LN_TXEQ_POLARITY[3] register bit. Valid Settings: • TXDRV_PREEM_1LSB_MODE_0_OVR_O = 0: 0x0 to 0x7 • TXDRV_PREEM_1LSB_MODE_0_OVR_O = 1: 0x0 to 0xB	

Table 14-3. TX Driver Register Signals for PHY-A (continued)

Register Signal	Address	Description
PMA_LN_TXEQ_POLARITY_O[3:0]	Lane_078	Controls sign of each of the TX data taps, with 0 indicating positive polarity and 1 indicating negative polarity: • Bit 0 = Pre-cursor bit • Bit 1 = Current bit • Bit 2 = Post-cursor bit • Bit 3 = Second post-cursor bit
TXDRV_PREEM_1LSB_MODE_0 _OVR_O	Lane_004	If asserted, enables the 1LSB mode for tap equalization settings. This gives finer control of equalization settings: • 1 = Enable 1 lsb mode. In this state, the control is finer grained and tap settings may not map to the same emphasis settings as in non-1lsb mode. • 0 = Disable 1 lsb mode. In this mode, cm, c1 and c2 settings are decoded based on termination calibration and attenuator setting. The settings are adjusted so as to maintain correct emphasis settings over corners and att register settings.

Table 14-4 shows a list of important registers for TX driver for PHY-B. Included are signal names, addresses and a brief description of functionality.

Table 14-4. TX Driver Register Signals for PHY-B

Register Signal	Address	Description
		Amplitude
TXDRV_ATT_IN_OVR_O[3:0]	Lane_004	Selects attenuator setting for TX driver (binary coded). Increasing this register value increases the transmitter amplitude. The attenuator register works by setting slices to drive out fixed 0s, therefore reducing output amplitude.
PMA_LN_TX_VREG_LEV_O[4:0]	Lane_0A4	Selects regulator voltage setting for TX driver slices. Transmit voltage increases with increase in register setting according to the following equation: • 730 mV + 12.5 mV*PMA_LN_TX_VREG_LEV Note: PMA_LN_TX_VREG_LEV setting should not be set higher than 0.95 V for long-term reliability reasons.
		Equalization
TXDRV_CM_IN_OVR_O[3:0]	Lane_008	Selects magnitude of the Cm1 equalization tap (binary coded). Increasing the value of this register increases the magnitude of the tap. The polarity of this tap is set with the PMA_LN_TXEQ_POLARITY[0] register bit. Valid Settings: • TXDRV_PREEM_1LSB_MODE_0_OVR_O = 0: 0x0 to 0x7 • TXDRV_PREEM_1LSB_MODE_0_OVR_O = 1: 0x0 to 0xD
TXDRV_C1_IN_OVR_0[4:0]	Lane_008	Selects magnitude of the C1 equalization tap (binary coded). Increasing the value of this register increases the magnitude of the tap. The polarity of this tap is set with the PMA_LN_TXEQ_POLARITY[2] register bit. Valid Settings: • TXDRV_PREEM_1LSB_MODE_0_OVR_O = 0: 0x0 to 0xF • TXDRV_PREEM_1LSB_MODE_0_OVR_O = 1: 0x0 to 0x17
TXDRV_C2_IN_OVR_O[3:0	Lane_008	Selects magnitude of the C2 equalization tap (binary coded). Increasing the value of this register increases the magnitude of the tap. The polarity of this tap is set with the PMA_LN_TXEQ_POLARITY[3] register bit. Valid Settings: • TXDRV_PREEM_1LSB_MODE_0_OVR_O = 0: 0x0 to 0x7 • TXDRV_PREEM_1LSB_MODE_0_OVR_O = 1: 0x0 to 0xB
PMA_LN_TXEQ_POLARITY_O[3:0]	Lane_078	Controls sign of each of the TX data taps, with 0 indicating positive polarity and 1 indicating negative polarity: • Bit 0 = Pre-cursor bit • Bit 1 = Current bit • Bit 2 = Post-cursor bit • Bit 3 = Second post-cursor bit
TXDRV_PREEM_1LSB_MODE	Lane_008	If asserted, enables the 1LSB mode for tap equalization settings. This gives finer control of equalization settings: • 1 = Enable 1 lsb mode. In this state, the control is finer grained and tap settings may not map to the same emphasis settings as in non-1lsb mode. • 0 = Disable 1 lsb mode. In this mode, cm, c1 and c2 settings are decoded based on termination calibration and attenuator setting. The settings are adjusted so as to maintain correct emphasis settings over corners and att register settings.

SerDes Receiver Calibration

This section provides guidelines for configuring the SerDes Receiver side of the SerDes Macro.

CAUTION

Users are advised to use TI-generated default SerDes configurations specific to each interface (supplied as part of MCSDK). TI cannot directly support customer generated configuration files.

NOTE: Certain material in this chapter is reprinted with permission of Semtech Corporation – Snowbush IP Group © 2012

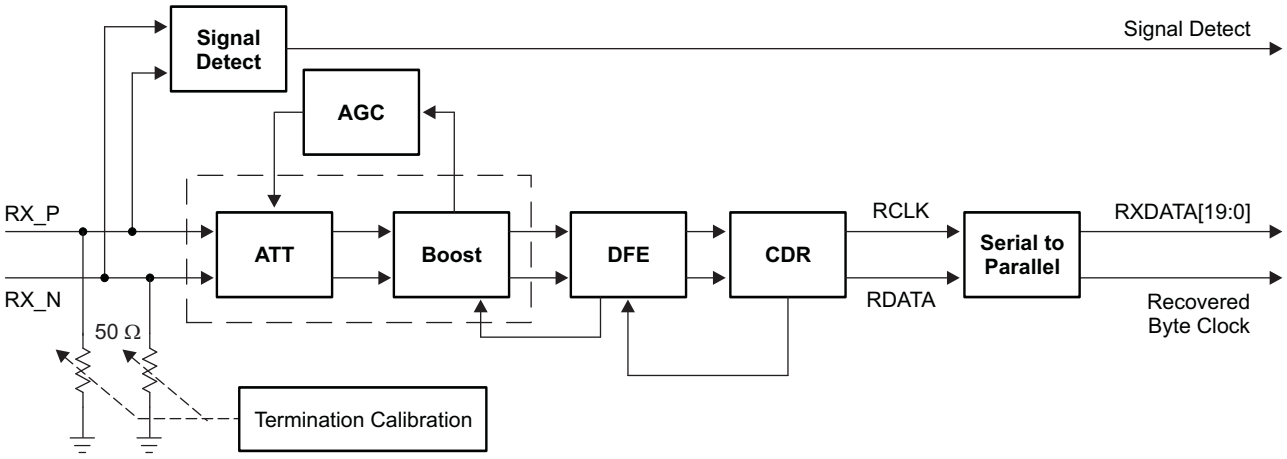
Topic **Page**

15.1 Introduction

This section provides guidelines on adjusting RX equalization settings to equalize a channel in the TI SerDes PHY. It includes details on equalization functions, a brief description of equalization blocks, and how to perform adaptation and override adapted values. Also, a list of relevant registers and their descriptions is included.

Figure 15-1 shows the entire RX path of KeyStone II SerDes PHY platform. The first stage is an Attenuator (ATT). This stage is required to reduce signal amplitude received from channel before entering the BOOST stage in order to not saturate the BOOST input. The ATT stage is adapted automatically by an in-built PHY algorithm but may be overridden to a fixed value through register settings.

Figure 15-1. RX Path Block Diagram



The next stage is BOOST. This stage is used to provide high-frequency gain to the received channel signal in order to mitigate the high frequency loss incurred in the channel. The boost stage consists of four gain stages. Each stage is a programmable gain peaking equalizer. The BOOST stage is automatically adapted by an in-built PHY algorithm but may be overridden to a fixed value through register settings.

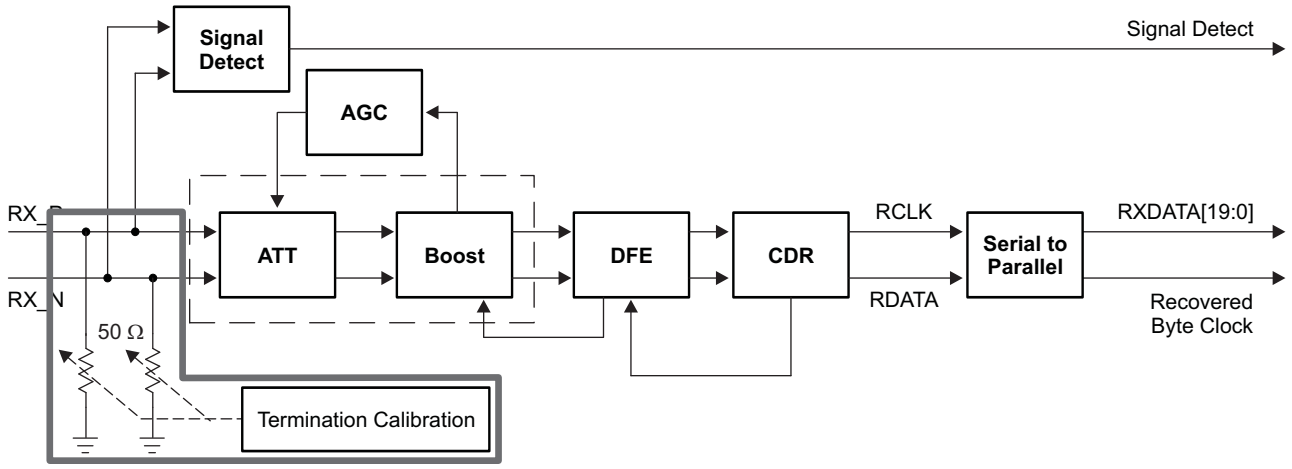
The next stage is DFE. The DFE is a tap-based decision feedback equalizer and helps to remove any remaining ISI after the BOOST stage. These tap values are automatically adapted by in-built algorithms in the PHY. The next stage is CDR. The VCO with-in the CDR is initially calibrated to the reference clock frequency. After initial calibration, on exit from electrical idle, the CDR VCO will move to lock to the input signal frequency and the recovered clock will be passed out to the PCS layer.

15.2 RX Stages

15.2.1 Termination Calibration

RX termination is automatically calibrated on startup. The target differential impedance is set by loading the SerDes configuration file provided by TI as part of the MCSDK. Figure 15-2 shows RX path termination diagram.

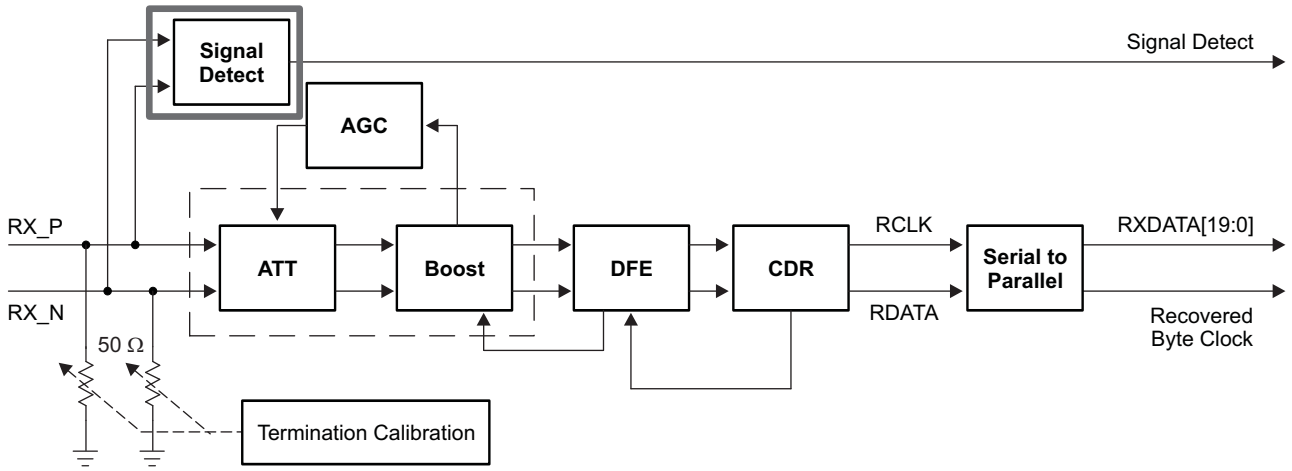
Figure 15-2. RX Path Termination Calibration Block Diagram



15.2.2 Signal Detect

The signal detect is an analog block that compares the incoming signal envelope to a programmable threshold to determine whether valid signaling is present on the RX_P/N input pins. An optimal signal detect threshold is set by loading the SerDes configuration file provided by TI as part of the MCSDK. The signal detect can also be manually triggered/overridden by the user as a means to reset the RX stage and force RX re-calibration (electrical idle exit calibration must be enabled). This manual override can be found in the lane_004 register.Figure 15-3 shows the RX path signal detect block diagram.

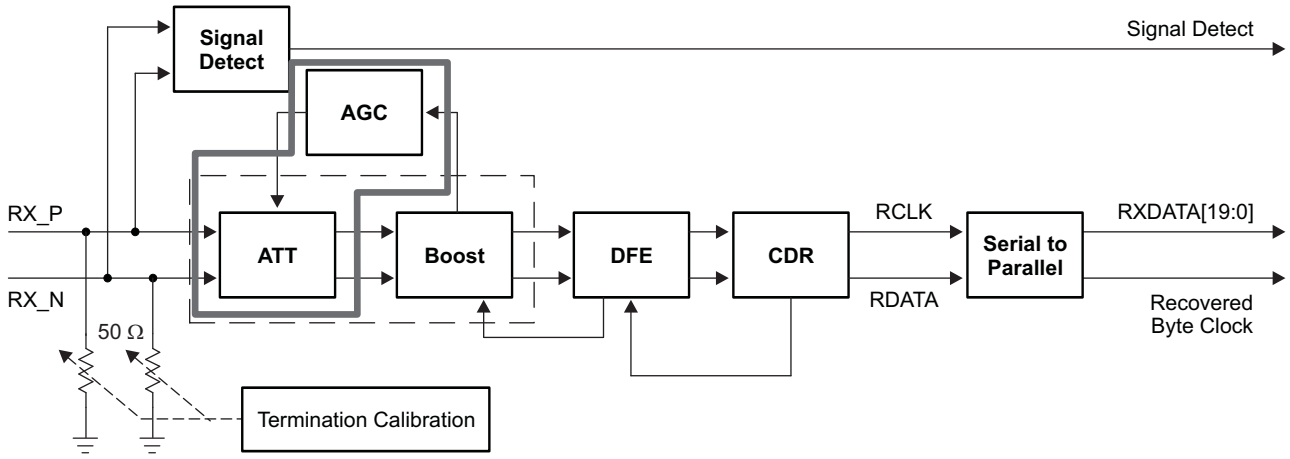
Figure 15-3. RX Path Signal Detect Block Diagram



15.3 Attenuator

Due to the wide range of supported serial standards, the receive voltage swing can vary anywhere between 100 mVpp and 1.2 Vpp. The ATT is used to provide the analog boost sub-block with 100 mVpp-400 mVpp voltage swings, so the block acts primarily as a programmable analog attenuator. The voltage swing of the analog boost must be fixed at a low enough level to avoid saturation. Figure 15-4 shows RX path attenuator block diagram.

Figure 15-4. RX Path Attenuator Block Diagram



The ATT settings is adapted automatically (default setting on TI provided SerDes configuration) by an in-built PHY algorithm but may be overridden to a fixed value through register settings. If ATT adaptation is enabled, the AGC block is used to measure the average signal envelope from the ATT block and adjusts the ATT gain to achieve a configurable amplitude at the output of the BOOST block. The AGC is enabled only if ATT adaptation is being performed. If ATT adaptation is not being performed, the AGC block is powered off.

15.3.1 Calibration Modes

There are **three** modes used to trigger an automatic adaptation for ATT, BOOST, and DFE TAP values. Each of these modes of operation can be enabled/disabled via register settings:

- **Initial calibration**
- Automatic adaptation will be performed after PHY startup sequence has completed and link has exited from electrical idle. This adaptation will be performed only once.
- **Rate change calibration**
- Automatic adaptation will be performed whenever a rate change is requested.
- **Electrical idle exit calibration**
- Automatic adaptation will be performed whenever the lane exits from the electrical idle state.

NOTE: Due to timing restrictions in certain standards e.g. PCIe, certain calibrations such as electrical idle exit calibration are turned off by default in these modes.

Relevant registers for calibrating RX ATT adaptation are shown in Table 15-1.

Table 15-1. Register Settings to Control ATT Adaptation

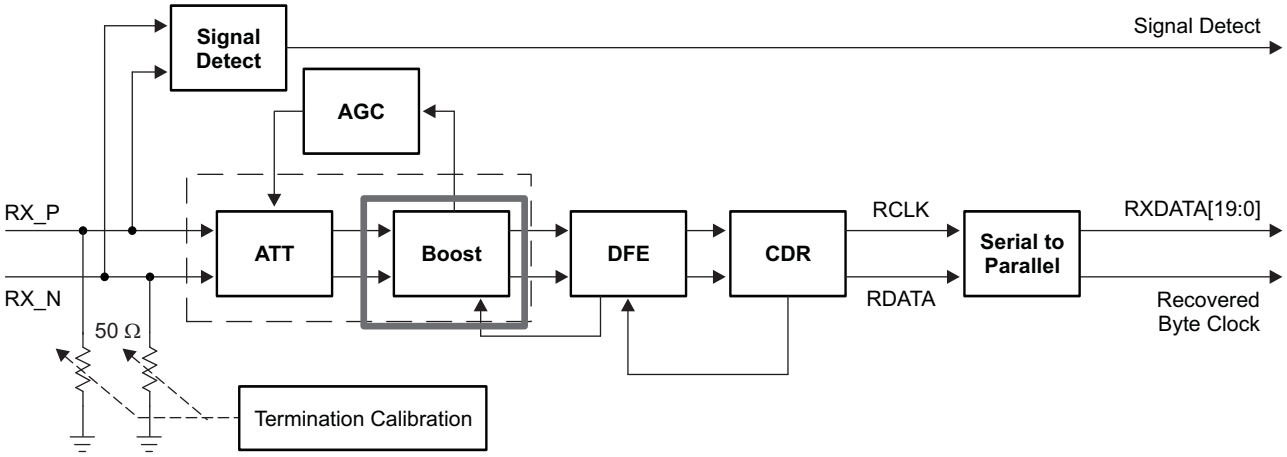
Register Signal	Address PHY-A PHY-B	Description
General Controls		
RXEQ_RATE1_CAL_EN_O	Comlane_084 Lane_098	Master enable for adaptation rate 1 (i.e. Non-PCIe mode - Quarter Rate, PCIe mode - Gen1). The master enable supersedes all other enables • 1 = Adaptation is enabled for rate 1 • 0 = Adaptation is disabled for rate 1
RXEQ_RATE2_CAL_EN_O	Comlane_084 Lane_098	Master enable for adaptation rate 2 (i.e. Non-PCIe mode - Half Rate, PCIe mode - Gen2). The master enable supersedes all other enables • 1 = Adaptation is enabled for rate 2 • 0 = Adaptation is disabled for rate 2
RXEQ_RATE3_CAL_EN_O	Comlane_084 Lane_098	Master enable for adaptation rate 3 (i.e. Non-PCIe mode - Full Rate, PCIe mode -N/A). The master enable supersedes all other enables • 1 = Adaptation is enabled for rate 3 • 0 = Adaptation is disabled for rate 3
ATT		
RXEQ_RATE1_ATT_START_O[3:0]	Lane_084	ATT start value for adaptation for rate 1 (i.e. Non-PCIe mode - Quarter Rate, PCIe mode - Gen1). Valid range of values is 0x0 - 0xA. Larger values results in less attenuation. If ATT adaptation is turned off for rate1, this value will be stored as ATT value.
RXEQ_RATE2_ATT_START_O[3:0]	Lane_084	ATT start value for adaptation for rate 2 (i.e. Non-PCIe mode - Half Rate, PCIe mode - Gen2). Valid range of values is 0x0 - 0xA. Larger values results in less attenuation. If ATT adaptation is turned off for rate2, this value will be stored as ATT value.
RXEQ_RATE3_ATT_START_O[3:0]	Lane_08C	ATT start value for adaptation for rate 3 (i.e. Non-PCIe mode - Full Rate, PCIe mode -N/A). Valid range of values is 0x0 - 0xA. Larger values results in less attenuation. If ATT adaptation is turned off for rate3, this value will be stored as ATT value.
RXEQ_INIT_CAL_O[0]	Comlane_084	Enable signal for ATT adaptation during initial calibration • 1 = Enables ATT adaptation for rate1/rate3 on initial bring-up • 0 = Disables ATT adaptation for rate1/rate3 on initial bring-up
RXEQ_RATE2_INIT_CAL_O[0]	Comlane_08C	Enable signal for ATT adaptation during initial calibration • 1 = Enables ATT adaptation for rate2 on initial bring-up • 0 = Disables ATT adaptation for rate2 on initial bring-up
RXEQ_RECAL_O[0]	Comlane_08C	Enable signal for ATT adaptation during rate change • 1 = Enables ATT adaptation for rate1/rate3 on rate change • 0 = Disables ATT adaptation for rate1/rate3 on rate change
RXEQ_RATE2_RECAL_O[0]	Comlane_090	Enable signal for ATT adaptation during rate change • 1 = Enables ATT adaptation for rate2 on rate change • 0 = Disables ATT adaptation for rate2 on rate change

15.4 BOOST

The analog boost sub-block provides primarily high-frequency gain to the input to compensate for the low-pass characteristic of channels.

The Receiver equalization employs a multi-stage programmable amplifier. This allows varying amounts of high-frequency gain to be applied depending on the overall frequency response of the channel loss. Figure 15-5 shows RX path boost block diagram.

Figure 15-5. RX Path Boost Block Diagram



The BOOST settings is adapted automatically (default setting on TI provided SerDes configuration) by an in-built PHY algorithm but may be overridden to a fixed value through register settings. Relevant registers for calibrating RX BOOST adaptation are shown in Table 15-2.

Table 15-2. Register Settings to Control BOOST Adaptation

Register Signal	Address PHY-A PHY-B	Description
General Controls		
RXEQ_RATE1_CAL_EN_O	Comlane_084 Lane_098	Master enable for adaptation for rate 1 (i.e. Non-PCIe mode - Quarter Rate, PCIe mode - Gen1). The master enable supersedes all other enables • 1 = Adaptation is enabled for rate 1 • 0 = Adaptation is disabled for rate 1
RXEQ_RATE2_CAL_EN_O	Comlane_084 Lane_098	Master enable for adaptation for rate 2 (i.e. Non-PCIe mode - Half Rate, PCIe mode - Gen2). The master enable supersedes all other enables • 1 = Adaptation is enabled for rate 2 • 0 = Adaptation is disabled for rate 2
RXEQ_RATE3_CAL_EN_O	Comlane_084 Lane_098	Master enable for adaptation for rate 3 (i.e. Non-PCIe mode - Full Rate, PCIe mode -N/A). The master enable supersedes all other enables • 1 = Adaptation is enabled for rate 3 • 0 = Adaptation is disabled for rate 3
Boost		
RXEQ_RATE1_BOOST_START_O[3:0]	Lane_084	BOOST start value for adaptation for rate 1 (i.e. Non-PCIe mode - Quarter Rate, PCIe mode - Gen1). Valid range of values is 0x0 – 0xA. Larger values results in more high frequency gain. If BOOST adaptation is turned off for rate1, this value will be stored as BOOST value.

Table 15-2. Register Settings to Control BOOST Adaptation (continued)

Register Signal	Address PHY-A PHY-B	Description
RXEQ_RATE2_BOOST_START_O[3:0]	Lane_084	BOOST start value for adaptation for rate 2 (i.e. Non-PCIe mode - Half Rate, PCIe mode - Gen2). Valid range of values is 0x0 – 0xA. Larger values results in more high frequency gain. If BOOST adaptation is turned off for rate2, this value will be stored as BOOST value.
RXEQ_RATE3_BOOST_START_O[3:0]	Lane_08C	BOOST start value for adaptation for rate 3 (i.e. Non-PCIe mode - Full Rate, PCIe mode -N/A). Valid range of values is 0x0 – 0xA. Larger values results in more high frequency gain. If BOOST adaptation is turned off for rate3, this value will be stored as BOOST value.
RXEQ_INIT_CAL_O[1]	Comlane_084	Enable signal for BOOST adaptation during initial calibration. • 1 = Enables BOOST adaptation for rate1/rate3 on initial bring-up • 0 = Disables BOOST adaptation for rate1/rate3 on initial bring-up
RXEQ_RATE2_INIT_CAL_O[1]	Comlane_090	Enable signal for BOOST adaptation during initial calibration. • 1 = Enables BOOST adaptation for rate2 on initial bring-up • 0 = Disables BOOST calibration for rate2 on initial bring-up
RXEQ_RECAL_O[1]	Comlane_08C	Enable signal for BOOST adaptation during rate change • 1 = Enables BOOST adaptation for rate1/rate3 on rate change • 0 = Disables BOOST adaptation for rate1/rate3 on rate change
RXEQ_RATE2_RECAL_O[1]	Comlane_090	Enable signal for BOOST adaptation during rate change • 1 = Enables BOOST adaptation for rate2 on rate change • 0 = Disables BOOST adaptation for rate2 on rate change

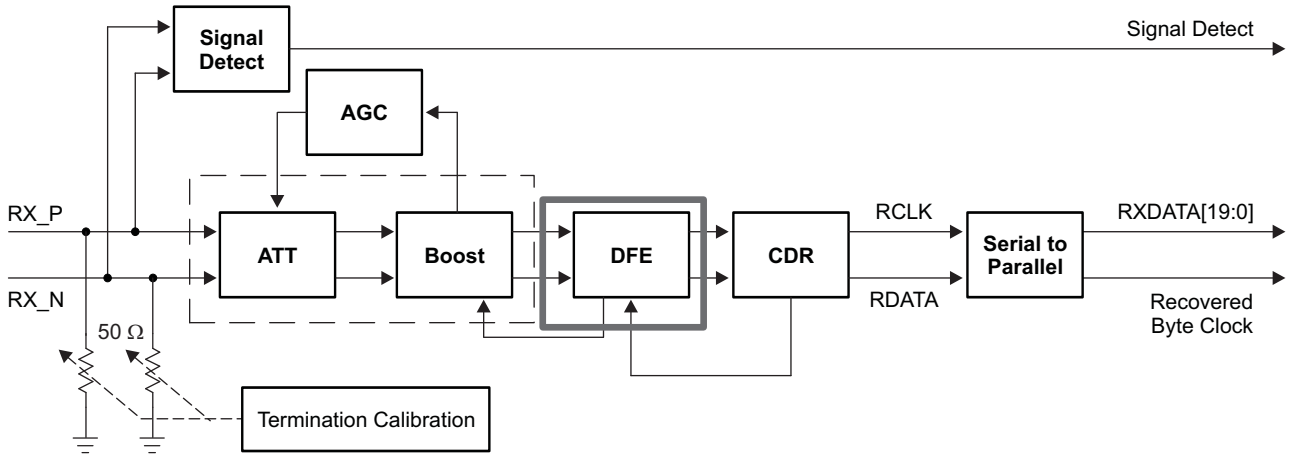
15.5 DFE

Although having a programmable analog boost is an effective method of equalizing a received signal, it has the drawback of also amplifying high-frequency noise such as crosstalk. The DFE is a filter that equalizes the signal without amplifying this high-frequency noise.

The DFE employs an auto-adaptation algorithm (default setting on TI provided SerDes configuration) that determines the optimum tap weights necessary to equalize any channel impulse response. This step comes after the auto-adaptation of the ATT and the receive equalizer.

Figure 15-6 shows RX path DFE block diagram.

Figure 15-6. RX Path DFE Block Diagram



The tap auto-adaptation on PHY-A and PHY-B is performed using one of the two available algorithms:

- The Center DFE algorithm calibrates the taps to ensure that the eye height at the sampled point of the input data is at an optimal level. The only taps modified for Central DFE are the taps of the data sample comparators. (Available only on PHY-B)
- The Edge DFE algorithm calibrates the taps to ensure that the eye is correctly equalized on the edge samples. The Edge DFE modifies the tap values for both centre and edge comparators.

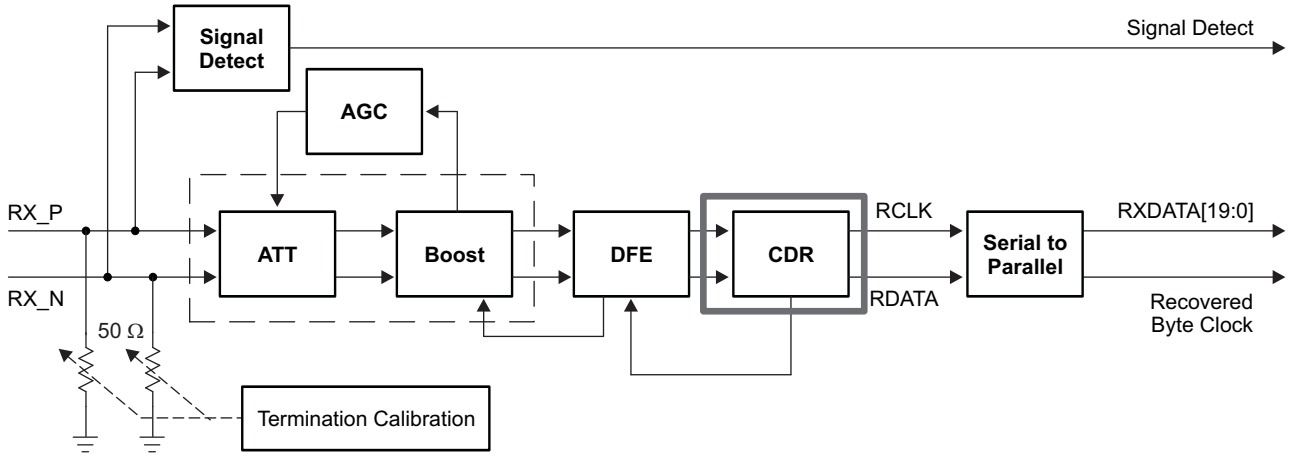
NOTE: The default setting on TI provided SerDes configuration control the DFE registers settings. TI recommends customers to NOT modify any of the DFE register settings.

15.6 CDR

The CDR is responsible for extracting a recovered clock from the input data stream. The PHY CDR is a PLL based receiver that utilizes a completely digital phase-detector and loop-filter. By design, the CDR bandwidth scales with data-rate, so users need not adjust CDR loop parameters for various data rates.

Figure 15-7 shows RX path CDR diagram.

Figure 15-7. RX Path CDR Block Diagram



NOTE: The default setting on TI provided SerDes configuration control the CDR registers settings. TI recommends customers to NOT modify any of the CDR register settings.

SerDes PHY Memory Map

Table 16-1, Table 16-2 and Table 16-3 shows relative offsets to each of the PHYs and their sub-modules used in KeyStone II Devices. The offset address values provided are relative to the associated base address of the Interface SerDes Configuration space. See the device-specific data manuals for the interface specific SerDes configuration base address.

Topic **Page**

16.1 Memory Mapping for PHY-A 2 Lane Sub-Systems

Table 16-1. Memory Mapping for PHY-A 2 Lane Sub-Systems

Sub-System	Offset Address [1]	Register Name	Description	Section
CMU0	0x0000 - 0x0004	Reserved	Reserved	Reserved
	0x0008	cmu_008	Register at 008	Section 17.1.1
	0x000C - 0x00E8	Reserved	Reserved	Reserved
	0x00EC	cmu_0EC	Register at 0EC	Section 17.1.2
	0x00F0	Reserved	Reserved	Reserved
	0x00FC	cmu_0FC	Register at 0FC	Section 17.1.3
LANE0	0x0200	lane_000	Register at 000	Section 17.2.1
	0x0204	lane_004	Register at 004	Section 17.2.2
	0x0208	lane_008	Register at 008	Section 17.2.3
	0x020C - 0x0228	Reserved	Reserved	Reserved
	0x022C	lane_02C	Register at 02C	Section 17.2.4
	0x0230	lane_030	Register at 030	Section 17.2.5
	0x0234	lane_034	Register at 034	Section 17.2.6
	0x0238	lane_038	Register at 038	Section 17.2.7
	0x023C	lane_03C	Register at 03C	Section 17.2.8
	0x0240	lane_040	Register at 040	Section 17.2.9
	0x0244	lane_044	Register at 044	Section 17.2.10
	0x0248	lane_048	Register at 048	Section 17.2.11
	0x024C - 0x0254	Reserved	Reserved	Reserved
	0x0258	lane_058	Register at 058	Section 17.2.12
	0x025C	lane_05C	Register at 05C	Section 17.2.13
	0x0260 - 0x0274	Reserved	Reserved	Reserved
	0x0278	lane_078	Register at 078	Section 17.2.14
	0x027C - 0x0280	Reserved	Reserved	Reserved
	0x0284	lane_084	Register at 084	Section 17.2.15
	0x0288	Reserved	Reserved	Reserved
	0x028C	lane_08c	Register at 08c	Section 17.2.16
	0x0290 - 0x0294	Reserved	Reserved	Reserved
	0x02A0	lane_0a0	Register at 0a0	Section 17.2.17
	0x02A4	Reserved	Reserved	Reserved
	0x02A8	lane_0a8	Register at 0a8	Section 17.2.18
	0x02AC - 0x03FC	Reserved	Reserved	Reserved

(1) The addresses provided in the table are offsets from a device specific base address. To determine the base address of these registers, see the device-specific data manual.

Table 16-1. Memory Mapping for PHY-A 2 Lane Sub-Systems (continued)

Sub-System	Offset Address (1)	Register Name	Description	Section
LANE1	0x0400	lane_000	Register at 000	Section 17.2.1
	0x0404	lane_004	Register at 004	Section 17.2.2
	0x0408	lane_008	Register at 008	Section 17.2.3
	0x040C - 0x0428	Reserved	Reserved	Reserved
	0x042C	lane_02C	Register at 02C	Section 17.2.4
	0x0430	lane_030	Register at 030	Section 17.2.5
	0x0434	lane_034	Register at 034	Section 17.2.6
	0x0438	lane_038	Register at 038	Section 17.2.7
	0x043C	lane_03C	Register at 03C	Section 17.2.8
	0x0440	lane_040	Register at 040	Section 17.2.9
	0x0444	lane_044	Register at 044	Section 17.2.10
	0x0448	lane_048	Register at 048	Section 17.2.11
	0x044C - 0x0454	Reserved	Reserved	Reserved
	0x0458	lane_058	Register at 058	Section 17.2.12
	0x045C	lane_05C	Register at 05C	Section 17.2.13
	0x0460 - 0x0474	Reserved	Reserved	Reserved
	0x0478	lane_078	Register at 078	Section 17.2.14
	0x047C - 0x0480	Reserved	Reserved	Reserved
	0x0484	lane_084	Register at 084	Section 17.2.15
	0x0488	Reserved	Reserved	Reserved
	0x0490 -0x0494	Reserved	Reserved	Reserved
	0x04A0	lane_0a0	Register at 0a0	Section 17.2.17
	0x04A4	Reserved	Reserved	Reserved
	0x04A8	lane_0a8	Register at 0a8	Section 17.2.18
	0x04AC - 0x05FC	Reserved	Reserved	Reserved
COMLANE	0x0A00	comlane_000	Register at 000	Section 17.3.1
	0x0A04 - 0x0A10	Reserved	Reserved	Reserved
	0x0A14	comlane_014	Register at 014	Section 17.3.2
	0x0A18 - 0x0A80	Reserved	Reserved	Reserved
	0x0A84	comlane_084	Register at 084	Section 17.3.3
	0x0A88	Reserved	Reserved	Reserved
	0x0A8C	comlane_08c	Register at 08c	Section 17.3.4
	0x0A90	comlane_090	Register at 090	Section 17.3.5
	0x0A94 - 0x0AEC	Reserved	Reserved	Reserved
	0x0AF0	comlane_0f0	Register at 0f0	Section 17.3.6
	0x0AFC - 0x0BF4	Reserved	Reserved	Reserved
	0x0BF8	comlane_1F8	Register at 1F8	Section 17.3.7
	0x0BFC	Reserved	Reserved	Reserved
WIZ	0x1FC0 - 0x1FDC	Reserved	Reserved	Reserved
	0x1FE0	LANE1CTL_STS	Lane 1 Control and status	Section 17.4.1
	0x1FE4	LANE2CTL_STS	Lane 2 Control and status	Section 17.4.1
	0x1FE8 - 0x1FF0	Reserved	Reserved	Reserved
	0x1FF4	PLL_CTRL	PLL Control	Section 17.4.2
	0x1FF8 - 0x1FFC	Reserved	Reserved	Reserved

16.2 Memory Mapping for PHY-A 4 Lane Sub-Systems

Table 16-2. Memory Mapping for PHY-A 4 Lane Sub-Systems

Sub-System	Offset Address [1]	Register Name	Description	Section
CMU0	0x0000 - 0x0004	Reserved	Reserved	Reserved
	0x0008	cmu_008	Register at 008	Section 17.1.1
	0x000C - 0x00E8	Reserved	Reserved	Reserved
	0x00EC	cmu_0EC	Register at 0EC	Section 17.1.2
	0x00F0	Reserved	Reserved	Reserved
	0x00FC	cmu_0FC	Register at 0FC	Section 17.1.3
LANE0	0x0200	lane_000	Register at 000	Section 17.2.1
	0x0204	lane_004	Register at 004	Section 17.2.2
	0x0208	lane_008	Register at 008	Section 17.2.3
	0x020C - 0x0228	Reserved	Reserved	Reserved
	0x022C	lane_02C	Register at 02C	Section 17.2.4
	0x0230	lane_030	Register at 030	Section 17.2.5
	0x0234	lane_034	Register at 034	Section 17.2.6
	0x0238	lane_038	Register at 038	Section 17.2.7
	0x023C	lane_03C	Register at 03C	Section 17.2.8
	0x0240	lane_040	Register at 040	Section 17.2.9
	0x0244	lane_044	Register at 044	Section 17.2.10
	0x0248	lane_048	Register at 048	Section 17.2.11
	0x024C-0x0254	Reserved	Reserved	Reserved
	0x0258	lane_058	Register at 058	Section 17.2.12
	0x025C	lane_05C	Register at 05C	Section 17.2.13
	0x0260 - 0x0274	Reserved	Reserved	Reserved
	0x0278	lane_078	Register at 078	Section 17.2.14
	0x027C - 0x0280	Reserved	Reserved	Reserved
	0x0284	lane_084	Register at 084	Section 17.2.15
	0x0288	Reserved	Reserved	Reserved
	0x028C	lane_08c	Register at 08c	Section 17.2.16
	0x0290 - 0x0294	Reserved	Reserved	Reserved
	0x02A0	lane_0a0	Register at 0a0	Section 17.2.17
	0x02A4	Reserved	Reserved	Reserved
	0x02A8	lane_0a8	Register at 0a8	Section 17.2.18
	0x20AC - 0x03FC	Reserved	Reserved	Reserved

(1) The addresses provided in the table are offsets from a device specific base address. To determine the base address of these registers, see the device-specific data manual.

Table 16-2. Memory Mapping for PHY-A 4 Lane Sub-Systems (continued)

Sub-System	Offset Address (1)	Register Name	Description	Section
LANE1	0x0400	lane_000	Register at 000	Section 17.2.1
	0x0404	lane_004	Register at 004	Section 17.2.2
	0x0408	lane_008	Register at 008	Section 17.2.3
	0x040C - 0x0428	Reserved	Reserved	Reserved
	0x042C	lane_02c	Register at 02c	Section 17.2.4
	0x0430	lane_030	Register at 030	Section 17.2.5
	0x0434	lane_034	Register at 034	Section 17.2.6
	0x0438	lane_038	Register at 038	Section 17.2.7
	0x043C	lane_03C	Register at 03C	Section 17.2.8
	0x0440	lane_040	Register at 040	Section 17.2.9
	0x0444	lane_044	Register at 044	Section 17.2.10
	0x0448	lane_048	Register at 048	Section 17.2.11
	0x044C - 0x0454	Reserved	Reserved	Reserved
	0x0458	lane_058	Register at 058	Section 17.2.12
	0x045C	lane_05C	Register at 05C	Section 17.2.13
	0x0460 - 0x0474	Reserved	Reserved	Reserved
	0x0478	lane_078	Register at 078	Section 17.2.14
	0x047C - 0x0480	Reserved	Reserved	Reserved
	0x0484	lane_084	Register at 084	Section 17.2.15
	0x0488	Reserved	Reserved	Reserved
	0x048C	lane_08c	Register at 08c	Section 17.2.16
	0x0490 - 0x0494	Reserved	Reserved	Reserved
	0x04A0	lane_0a0	Register at 0a0	Section 17.2.17
	0x04A4	Reserved	Reserved	Reserved
	0x04A8	lane_0a8	Register at 0a8	Section 17.2.18
	0x04AC - 0x05FC	Reserved	Reserved	Reserved

Table 16-2. Memory Mapping for PHY-A 4 Lane Sub-Systems (continued)

Sub-System	Offset Address (1)	Register Name	Description	Section
LANE2	0x0600	lane_000	Register at 000	Section 17.2.1
	0x0604	lane_004	Register at 004	Section 17.2.2
	0x0608	lane_008	Register at 008	Section 17.2.3
	0x060C - 0x0628	Reserved	Reserved	Reserved
	0x062C	lane_02C	Register at 02C	Section 17.2.4
	0x0630	lane_030	Register at 030	Section 17.2.5
	0x0634	lane_034	Register at 034	Section 17.2.6
	0x0638	lane_038	Register at 038	Section 17.2.7
	0x063C	lane_03C	Register at 03C	Section 17.2.8
	0x0640	lane_040	Register at 040	Section 17.2.9
	0x0644	lane_044	Register at 044	Section 17.2.10
	0x0648	lane_048	Register at 048	Section 17.2.11
	0x064C-0x0654	Reserved	Reserved	Reserved
	0x0658	lane_058	Register at 058	Section 17.2.12
	0x065C	lane_05C	Register at 05C	Section 17.2.13
	0x0660 - 0x0674	Reserved	Reserved	Reserved
	0x0678	lane_078	Register at 078	Section 17.2.14
	0x067C - 0x0680	Reserved	Reserved	Reserved
	0x0684	lane_084	Register at 084	Section 17.2.15
	0x0688	Reserved	Reserved	Reserved
	0x068C	lane_08c	Register at 08c	Section 17.2.16
	0x0690 - 0x0694	Reserved	Reserved	Reserved
	0x06A0	lane_0a0	Register at 0a0	Section 17.2.17
	0x06A4	Reserved	Reserved	Reserved
	0x06A8	lane_0a8	Register at 0a8	Section 17.2.18
	0x06AC - 0x07FC	Reserved	Reserved	Reserved

Table 16-2. Memory Mapping for PHY-A 4 Lane Sub-Systems (continued)

Sub-System	Offset Address (1)	Register Name	Description	Section
LANE3	0x0800	lane_000	Register at 000	Section 17.2.1
	0x0804	lane_004	Register at 004	Section 17.2.2
	0x0808	lane_008	Register at 008	Section 17.2.3
	0x080C - 0x0828	Reserved	Reserved	Reserved
	0x082C	lane_02C	Register at 02C	Section 17.2.4
	0x0830	lane_030	Register at 030	Section 17.2.5
	0x0834	lane_034	Register at 034	Section 17.2.6
	0x0838	lane_038	Register at 038	Section 17.2.7
	0x083C	lane_03C	Register at 03C	Section 17.2.8
	0x0840	lane_040	Register at 040	Section 17.2.9
	0x0844	lane_044	Register at 044	Section 17.2.10
	0x0848	lane_048	Register at 048	Section 17.2.11
	0x084C-0x0854	Reserved	Reserved	Reserved
	0x0858	lane_058	Register at 058	Section 17.2.12
	0x085C	lane_05C	Register at 05C	Section 17.2.13
	0x0860 - 0x0874	Reserved	Reserved	Reserved
	0x0878	lane_078	Register at 078	Section 17.2.14
	0x087C - 0x0880	Reserved	Reserved	Reserved
	0x0884	lane_084	Register at 084	Section 17.2.15
	0x0888	Reserved	Reserved	Reserved
	0x088C	lane_08c	Register at 08c	Section 17.2.16
	0x0890 - 0x0894	Reserved	Reserved	Reserved
	0x08A0	lane_0a0	Register at 0a0	Section 17.2.17
	0x08A4	Reserved	Reserved	Reserved
	0x08A8	lane_0a8	Register at 0a8	Section 17.2.18
	0x08AC - 0x09FC	Reserved	Reserved	Reserved
COMLANE	0x0A00	comlane_000	Register at 000	Section 17.3.1
	0x0A04 - 0x0A10	Reserved	Reserved	Reserved
	0x0A14	comlane_014	Register at 014	Section 17.3.2
	0x0A18 - 0x0A80	Reserved	Reserved	Reserved
	0x0A84	comlane_084	Register at 084	Section 17.3.3
	0x0A88	Reserved	Reserved	Reserved
	0x0A8C	comlane_08c	Register at 08c	Section 17.3.4
	0x0A90	comlane_090	Register at 090	Section 17.3.5
	0x0A94 - 0x0AEC	Reserved	Reserved	Reserved
	0x0AF0	comlane_0F0	Register at 0F0	Section 17.3.6
	0x0AFC - 0x0BF4	Reserved	Reserved	Reserved
	0x0BF8	comlane_1F8	Register at 1F8	Section 17.3.7
	0x0BFC	Reserved	Reserved	Reserved
WIZ	0x1FC0 - 0x1FDC	Reserved	Reserved	Reserved
	0x1FE0	LANE1CTL_STS	Lane 1 Control and status	Section 17.4.1
	0x1FE4	LANE2CTL_STS	Lane 2 Control and status	Section 17.4.1
	0x1FE8	LANE3CTL_STS	Lane 3 Control and status	Section 17.4.1
	0x1FEC	LANE4CTL_STS	Lane 4 Control and status	Section 17.4.1
	0x1FF0	Reserved	Reserved	Reserved
	0x1FF4	PLL_CTRL	PLL Control	Section 17.4.2
	0x1FF8 - 0x1FFC	Reserved	Reserved	Reserved

16.3 Memory Mapping for PHY-B 2 Lane Sub-Systems

Table 16-3. Memory Mapping for PHY-B 2 Lane Sub-Systems

Sub-System	Offset Address (1)	Register Name	Description	Section
CMU0	0x0000 - 0x00F4	Reserved	Reserved	Reserved
	0x00F8	cmu_0F8	Register at 0F8	Section 18.1.2
	0x00FC	cmu_0FC	Register at 0FC	Section 18.1.3
LANE0	0x0200	lane_000	Register at 000	Section 18.2.1
	0x0204	lane_004	Register at 004	Section 18.2.2
	0x0208	lane_008	Register at 008	Section 18.2.3
	0x020C - 0x0228	Reserved	Reserved	Reserved
	0x022C	lane_02C	Register at 02C	Section 18.2.4
	0x0230	lane_030	Register at 030	Section 18.2.5
	0x0234	lane_034	Register at 034	Section 18.2.6
	0x0238	lane_038	Register at 038	Section 18.2.7
	0x023C	lane_03C	Register at 03C	Section 18.2.8
	0x0240	lane_040	Register at 040	Section 18.2.9
	0x0244	lane_044	Register at 044	Section 18.2.10
	0x0248	lane_048	Register at 048	Section 18.2.11
	0x024C-0x0254	Reserved	Reserved	Reserved
	0x0258	lane_058	Register at 058	Section 18.2.12
	0x025C	lane_05C	Register at 05C	Section 18.2.13
	0x0260	lane_060	Register at 060	Section 18.2.14
	0x0264 - 0x0274	Reserved	Reserved	Reserved
	0x0278	lane_078	Register at 078	Section 18.2.15
	0x027C - 0x0280	Reserved	Reserved	Reserved
	0x0284	lane_084	Register at 084	Section 18.2.16
	0x0288	Reserved	Reserved	Reserved
	0x028C	lane_08c	Register at 08c	Section 18.2.17
	0x0290 - 0x0294	Reserved	Reserved	Reserved
	0x0298	lane_098	Register at 090	Section 18.2.18
	0x029C	lane_09C	Register at 09C	Section 18.2.19
	0x02A0	Reserved	Reserved	Reserved
	0x02A4	lane_0a4	Register at 0a4	Section 18.2.20
	0x02A8 - 0x3FC	Reserved	Reserved	Reserved

(1) The addresses provided in the table are offsets from a device specific base address. To determine the base address of these registers, see the device-specific data manual.

Table 16-3. Memory Mapping for PHY-B 2 Lane Sub-Systems (continued)

Sub-System	Offset Address (1)	Register Name	Description	Section
LANE1	0x0400	lane_000	lane_000	Section 18.2.1
	0x0404	lane_004	Register at 004	Section 18.2.2
	0x0408	lane_008	Register at 008	Section 18.2.3
	0x040C - 0x0428	Reserved	Reserved	Reserved
	0x042C	lane_02c	Register at 02C	Section 18.2.4
	0x0430	lane_030	Register at 030	Section 18.2.5
	0x0434	lane_034	Register at 034	Section 18.2.6
	0x0438	lane_038	Register at 038	Section 18.2.7
	0x043C	lane_03C	Register at 03C	Section 18.2.8
	0x0440	lane_040	Register at 040	Section 18.2.9
	0x0444	lane_044	Register at 044	Section 18.2.10
	0x0448	lane_048	Register at 048	Section 18.2.11
	0x044C - 0x0454	Reserved	Reserved	Reserved
	0x0458	lane_058	Register at 058	Section 18.2.12
	0x045C	lane_05C	Register at 05C	Section 18.2.13
	0x0460	lane_060	Register at 060	Section 18.2.14
	0x0464 - 0x0474	Reserved	Reserved	Reserved
	0x0478	lane_078	Register at 078	Section 18.2.15
	0x047C - 0x0480	Reserved	Reserved	Reserved
	0x0484	lane_084	Register at 084	Section 18.2.16
	0x0488	Reserved	Reserved	Reserved
	0x048C	lane_08c	Register at 08c	Section 18.2.17
	0x0490 - 0x0494	Reserved	Reserved	Reserved
	0x0498	lane_098	Register at 090	Section 18.2.18
	0x049C	lane_09C	Register at 09C	Section 18.2.19
	0x04A0	Reserved	Reserved	Reserved
	0x04A4	lane_0a4	Register at 0a4	Section 18.2.20
	0x04A8 - 0x5FC	Reserved	Reserved	Reserved
COMLANE	0x0A00 - 0x0A10	Reserved	Reserved	Reserved
	0x0A14	comlane_014	Register at 014	Section 18.3.1
	0x0A18 - 0x0A88	Reserved	Reserved	Reserved
	0x0A8C	comlane_08c	Register at 08c	Section 18.3.1
	0x0A90	comlane_090	Register at 090	Section 18.3.3
	0x0A94	Reserved	Reserved	Reserved
	0x0A98	comlane_098	Register at 098	Section 18.3.4
	0x0A9C	comlane_09C	Register at 09C	Section 18.3.5
	0x0A9C - 0xAB8	Reserved	Reserved	Reserved
	0x0ABC	comlane_0BC	Register at 0BC	Section 18.3.6
	0x0AC0 - 0x0AEC	Reserved	Reserved	Reserved
	0x0AF0	comlane_0F0	Register at 0F0	Section 18.3.7
	0x0B08 - 0x0BF4	Reserved	Reserved	Reserved
	0x0BF8	comlane_1F8	Register at 1F8	Section 18.3.8
	0x0BFC	Reserved	Reserved	Reserved
CMU1	0x0C00 - 0x0CF4	Reserved	Reserved	Reserved
	0x0CF8	cmu_0F8	Register at 0F8	Section 18.1.2
	0x0CFC	cmu_0FC	Register at 0FC	Section 18.1.3

Table 16-3. Memory Mapping for PHY-B 2 Lane Sub-Systems (continued)

Sub-System	Offset Address [1]	Register Name	Description	Section
WIZ	0x1FC0	Reserved	Reserved	Reserved
	0x1FC4	MEM_ADR	Memory Address Register	Section 18.4.1
	0x1FC8	MEM_DAT	Memory Data Portal Register	Section 18.4.2
	0x1FCC	MEM_DATINC	Memory Data Increment Portal	Section 18.4.3
	0x1FD0	CPU_CTRL	CPU Control Register	Section 18.4.4
	0x1FD4 - 0x1FDC	Reserved	Reserved	Reserved
	0x1FE0	LANE1CTL_STS	Lane 1 Control and status	Section 18.4.5
	0x1FE4	LANE2CTL_STS	Lane 2 Control and status	Section 18.4.5
	0x1FE8 - 0x1FF0	Reserved	Reserved	Reserved
	0x1FF4	PLL_CTRL	PLL Control	Section 18.4.6

PHY A Register Definitions (Both 4 Lane/2 Lane PHYs)

This chapter describes the register definitions for PHY-A, 2 Lane and PHY-A, 4 Lane.

NOTE: For the 2 lane PHY the bit-fields relevant to Lane 3 and Lane 4 in the register definitions in this chapter must be treated as “Reserved” bit-fields. Bit-fields specific to Lane 3 and Lane 4 are applicable only to 4 lane PHY.

Topic **Page**

17.1 PHY-A CMU Subsystem Register Definition

17.1.1 Cmu_008 - Register at 008

Figure 17-1. Register at 008 (cmu_008)

31 24	23 0
TBUS_ADDR_OVR_O_7_0	Reserved
R/W+00000000	R/W+00000000

Legend: R/W = Read/Write; -n = value after reset

Table 17-1. Register at 008 (cmu_008) Field Descriptions

Bits	Name	Description
31 - 24	TBUS_ADDR_OVR_O_7_0	Snapshot TestBus address
23 - 0	Reserved	Reserved - writes are ignored, always reads 0s.

17.1.2 Cmu_0ec - Register at 0ec

Figure 17-2. Register at 0ec (cmu_0ec)

31	24	23	0
TBUS_DATA_SMPL_7_0		Reserved	
R+X		R+0	

Legend: R = Read only; -n = value after reset

Table 17-2. Register at 0ec (cmu_0ec) Field Descriptions

Bits	Name	Description
31 - 24	TBUS_DATA_SMPL_7_0	Snapshot of TestBus data
23 - 0	Reserved	Reserved - writes are ignored, always reads 0s.

17.1.3 Cmu_0fc - Register at 0fc

Figure 17-3. Register at 0fc (cmu_0fc)

31 28	27 24	23 0
Reserved	TBUS_DATA_SMPL_11_8	Reserved
R+0	R+X	R+0

Legend: R = Read only; -n = value after reset

Table 17-3. Register at 0fc (cmu_0fc) Field Descriptions

Bits	Name	Description
31 - 28	Reserved	Reserved - writes are ignored, always reads 0s.
27 - 24	TBUS_DATA_SMPL_11_8	Snapshot of tbus data
23 - 0	Reserved	Reserved - writes are ignored, always reads 0s.

17.2 PHY-A Lane Subsystem Register Definition

17.2.1 Lane_000 - Register at 000

Figure 17-4. Register at 000 (lane_000)

31	30	29 24	23	22 20	19 16
RXCLK_LB_ENA_O	NES_LB_ENA_O	Reserved	CKTRANS_EN_O	DMUX_TXB_SEL_O_2_0	Reserved
R/W +0	R/W +0	R/W +000001	R/W +0	R/W +000	R/W +00

15 8	7 6	5 2	1	0
Reserved	DMUX_TXA_SEL_O_1_0	Reserved	RX_CLK_SRC_O	TX_CLK_SRC_O
R/W +0	R/W +00	R/W +0	R/W +1	R/W +0

Legend: R/W = Read/Write; -n = value after reset

Table 17-4. Register at 000 (lane_000) Field Descriptions

Bit	Field	Description
31	RXCLK_LB_ENA_O	HS recovered clock to transmit loopback enable
30	NES_LB_ENA_O	NES loopback enable.
29 - 24	Reserved	Reserved
23	CKTRANS_EN_O	Final transmit path output stage clock select. • 0 - Use normal transmit clock. • 1 - Use recovered RX clock as transmit clock. Used in FEP loopback only.
22 - 20	DMUX_TXB_SEL_O_2_0	Transmit mux B data input select enable - selects data passed to the TX FIFO. Effects of dmux_txb_sel_o[2:0]: • 0 = If interface PCIe loopback control=0, choose main data path (output of 8b/10b encoder). Otherwise choose recovered RX data from elastic buffer • 1 = Select output of 8b/10b encoder (main data path). • 2 = If interface PCIe loopback control=0, choose main data path (output of 8b/10b encoder). Otherwise choose recovered RX data from elastic buffer • 3 = Select BIST generator data • 4 = If interface PCIe loopback control=0, choose main data path (output of 8b/10b encoder). Otherwise choose recovered RX data from elastic buffer • 5 = Select recovered RX data from PMA • 6 = If interface PCIe loopback control=0, choose main data path (output of 8b/10b encoder). Otherwise choose recovered RX data from elastic buffer • 7 = Select recovered RX data from elastic buffer
19 - 8	Reserved	Reserved
7 - 6	DMUX_TXA_SEL_O_1_0	Transmit mux A data input select - selects data passed to the 8b/10b encoder: • 0 = Main TX data from SOC interface • 1 = Recovered RX data from output of 10b/8b decoder • 2 = BIST generator data • 3 = Reserved
5 - 2	Reserved	Reserved
1	RX_CLK_SRC_O	RX path clock select (Used only for LB_FEP mode)
0	TX_CLK_SRC_O	TX path clock select (Used only for LB_FEP mode)

17.2.2 Lane_004 - Register at 004

Figure 17-5. Register at 004 (lane_004)

31	30	29	28	25	24
TXDRV_PREEM_1LSB_MODE_0_OVR _O	Reserved		TXDRV_ATT_IN_OVR_O_3_0		Reserved
R/W +0	R/W +11		R/W +1010		R +0

23 8	7	6 5	4	3	2 1	0
Reserved	BCHK_CK_SRC_O	BCHK_SRC_O_1_0	BCHK_CLR_O	BCHK_EN_O	SIGDET_OVR _O_1_0	SOC_CK_EN _O
R/W +0000	R/W +0	R/W +00	R/W +0	R/W +0	R/W +00	R/W +0

Legend: R = Read only; R/W = Read/Write; -n = value after reset

Table 17-5. Register at 004 (lane_004) Field Descriptions

Bit	Field	Description
31	TXDRV_PREEM_1LSB_MODE_0_OVR_O	Value for TX driver 1 lsb pre emphasis setting
30 - 29	Reserved	Reserved
28 - 25	TXDRV_ATT_IN_OVR_O_3_0	Override value for TX driver attenuator setting
24 - 8	Reserved	Reserved
7	BCHK_CK_SRC_O	BIST checker, cdn is synchronized to: • 0 = RX byte Clock (PMA_LN_CLK_RXB_I) • 1 = RX lane Clock (RX_LN_CLK_I)
6 - 5	BCHK_SRC_O_1_0	BIST checker source. • 0 = BIST uses output of initial RX polbit (before Symbol Aligner) • 1 = BIST uses output of Symbol Aligner (before Elastic Buffer) • 2 = BIST uses output of RX loopback mux (before Decoder and Polbits) • 3 = BIST uses output of reg1 flop bank (before Interface blocks)
4	BCHK_CLR_O	BIST checker clear signal. Zeroes error counter output. Does NOT go through the RX BIST control block.
3	BCHK_EN_O	BIST checker enable. Enables BIST RX Control block, which enables the actual BIST RX block when appropriate.
2 - 1	SIGDET_OVR_O_1_0	Override signal detect output. Bit 1 is override enable, bit 0 is override value.
0	SOC_CK_EN_O	Select signal for TX_LNX_CLK_O (Used only for LB_FEP mode)

17.2.3 Lane_008 - Register at 008

Figure 17-6. Register at 008 (lane_008)

31 16	15 12	11 8	7 5	4 0
Reserved	TXDRV_CM_IN_3_0 _OVR_O	TXDRV_C2_IN_3_0 _OVR_O	AHB_TXDRV_SLEW_SLD3F _2_0_OVR_O	TXDRV_C1_IN_4_0 _OVR_O
R +0	R/W +0000	R/W +0000	R/W +001	R/W +00000

Legend: R = Read only; R/W = Read/Write; -n = value after reset

Table 17-6. Register at 008 (lane_008) Field Descriptions

Bit	Field	Description
31 - 16	Reserved	Reserved
15 - 12	TXDRV_CM_IN_OVR_O_3_0	Override value for TX driver CM coefficient setting
11 - 8	TXDRV_C2_IN_OVR_O_3_0	Override value for TX driver C2 coefficient setting
7 - 5	AHB_TXDRV_SLEW_SLD3F_2_0_OVR_O	Override value for tx driver sld3f setting
4 - 0	TXDRV_C1_IN_OVR_O_4_0	Override value for TX driver C1 coefficient setting

17.2.4 Lane_02C - Register at 02C

Figure 17-7. Register at 02C (lane_02C)

31	24	23	22	21	20	19	18	16
PMA_LN_EYE_DLY_O_7_0		PMA_LN_PHD_ENA_O_1_0		PMA_LN_DFE_BW_SCALE		PMA_LN_PD_DFE_BIAS	RXEQ_OVR_LOAD_EN_O_6_4	
R/W +00000000		R/W +00		R/W +11		R/W +0	R/W +000	

15	12	11	10	9	8	7	3	2	1	0
RXEQ_OVR_LOAD_EN_O_3_0		CDR_CONTROL_ATT_CTRL_O	RXEQ_OVR_LATCH_O	RXEQ_OVR_LOAD_O_6_5		RXEQ_OVR_LOAD_O_4_0		RXEQ_OVR_EN_O	RXEQ_EN_O	RXEQ_WAIT_EN_O
R/W +000		R/W +0	R/W +0	R/W +00		R/W +00000		R/W +0	R/W +1	R/W +1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 17-7. Register at 02C (lane_02C) Field Descriptions

Bit	Field	Description
31 - 24	PMA_LN_EYE_DLY_O_7_0	On-chip eye diagram X-direction offset control: Bit 9: unused Bits 8-7: Coarse x-direction offset, in steps of 1/2UI Bits 6-0: Fine x-direction offset
23 - 22	PMA_LN_PHD_ENA_O_1_0	• Bit 1: 1 - disables updates from D4/D3 data/edge samplers to VCO 0 - enables updates from D4/D3 data/edge samplers to VCO • Bit 0: 1 - disables updates from D1/D2 data/edge samplers to VCO 0 - enables updates from D1/D2 data/edge samplers to VCO
21 - 20	PMA_LN_DFE_BW_SCALE	DFE Bandwidth Selection: DFE_BW_SCALE[1:0] DFE comparator BW compared to full speed • 2'b00: 1/4 speed • 2'b01: 1/2 speed • 2'b10: 3/4 speed • 2'b11: Full speed
19	PMA_LN_PD_DFE_BIAS	Override for DFE bias powerdown from MSM. Enabled through assertion of msm_out_ovr_en. Assertion disables DFE. Allow >5us recovery time after de-assertion.
18 - 16	RXEQ_OVR_LOAD_EN_O_6_4	Override enable for AFE dfe tap1 inputs
15 - 12	RXEQ_OVR_LOAD_EN_O_3_0	Override enable for AFE dfe tap1 inputs
11	CDR_CONTROL_ATT_CTRL_O	ATT wait control. Upon detection of signal, DFE ATT calibration is enabled, without CISEL being asserted to the CDR. • 0 - CDR control block will wait for ATT calibration before proceeding • 1 - CDR control block will not wait for ATT calibration
10	RXEQ_OVR_LATCH_O	Override for DFE latch signal. Negative edge causes AFE to store values of DFE output registers.
9 - 8	RXEQ_OVR_LOAD_O_6_5	Override for DFE output register load value.
7 - 3	RXEQ_OVR_LOAD_O_4_0	Override for DFE output register load value.
2	RXEQ_OVR_EN_O	Override enable for DFE signals.
1	RXEQ_EN_O	DFE block enable signal.
0	RXEQ_WAIT_EN_O	CDR control block wait for DFE signal. • 0 - Do not wait for DFE calibration before enabling rx data • 1 - Wait for DFE calibration before enabling rx data

17.2.5 Lane_030 - Register at 030

Figure 17-8. Register at 030 (lane_030)

31 – 24	23	22	21 – 19	18	17	16
BIST_CHK_PREAM0_O_7_0	BIST_RX_CLOCK_ENABLE	BIST_TX_CLOCK_ENABLE	BIST_CHK_LFSR_LENGTH_O_2_0	BIST_CHK_DATA_MODE_O	Rsvd	BIST_GEN_MODE8B_O
R/W +00000000	R/W +0	R/W +0	R/W +000	R/W +0	R/W +0	R/W +0

15 – 14	13 – 12	11	10 – 8	7 – 5	4 – 0
Reserved	RXEQ_ATT_GAIN_OVR	RXEQ_ATT_GAIN_AUTOCAL_DIS	Reserved	RXEQ_DFE_CMP_SEL_OVR_O_2_0	Reserved
R/W +00	R/W +00	R/W +0	R/W +000	R/W +000	R/W +00000

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 17-8. Register at 030 (lane_030) Field Descriptions

Bit	Field	Description
31 - 24	BIST_CHK_PREAM0_O_7_0	BIST checker preamble word 0. When in 8b mode, and prior to the 8b/10b encoder, bit 8 is expected to be the K indicator. This word should correspond to the alignment character used for the symbol alignment block.
23	BIST_RX_CLOCK_ENABLE	Active HIGH clock enable signal for the BIST receive clock.
22	BIST_TX_CLOCK_ENABLE	Active HIGH clock enable signal for the BIST transmit clock
21 - 19	BIST_CHK_LFSR_LENGTH_O_2_0	BIST PRBS pattern selector. bist_gen_mode8b_o=0, bist_gen_word_o=0: • 0 = PRBS7 with 10-bit bus width • 1 = PRBS15 with 10-bit bus width • 2 = PRBS23 with 10-bit bus width • 3 = PRBS31 with 10-bit bus width bist_gen_mode8b_o=0,bist_gen_word_o=1: • 0 = PRBS7 with 20-bit bus width • 1 = PRBS15 with 20-bit bus width • 2 = PRBS23 with 20-bit bus width • 3 = PRBS31 with 20-bit bus width bist_gen_mode8b_o=1, bist_gen_word_o=0: • 0 = PRBS7 with 8-bit bus width • 1 = PRBS15 with 8-bit bus width • 2 = PRBS23 with 8-bit bus width • 3 = PRBS31 with 8-bit bus width bist_gen_mode8b_o=1, bist_gen_word_o=1: • 0 = PRBS7 with 16-bit bus width • 1 = PRBS15 with 16-bit bus width • 2 = PRBS23 with 16-bit bus width • 3 = PRBS31 with 16-bit bus width
18	BIST_CHK_DATA_MODE_O	BIST checker mode select. • 0x0 = UDP pattern. • 0x1 = PRBS pattern
17	Reserved	Reserved - writes are ignored, always reads 0s
16	BIST_GEN_MODE8B_O	BIST generator 8b mode control • 0 - Generated data word is 10 bits • 1 - Generated data word is 8 bits
15 - 14	Reserved	Reserved
13 - 12	RXEQ_ATT_GAIN_OVR	Override for the value of rx_att_gain output to PMA when rxeq_att_gain_autocal_dis=1

Table 17-8. Register at 030 (lane_030) Field Descriptions (continued)

11	RXEQ_ATT_GAIN_AUTOCAL_DIS	Disable auto cal of RXEQ gain control (rx_att_gain).
10 - 8	Reserved	Reserved
7 - 5	RXEQ_DFE_CMP_SEL_OVR_O_2_0	Override value for comparator calibration select. Enabled by rxeq_ovr_en_o: • 1: Calibrate DFE comparator 1 • 2: Calibrate DFE comparator 2 • 3: Calibrate DFE comparator 3 • 4: Calibrate DFE comparator 4
4 - 0	Reserved	Reserved

17.2.6 Lane_034 - Register at 034

Figure 17-9. Register at 034 (lane_034)

31	30	28	27
Reserved	BIST_GEN_INSERT_COUNT_O_2_0		BIST_GEN_SEND_PREAM_O
R +0	R/W +000		R/W +0

26	18	17	16	15	8	7
Reserved		BIST_CHK_PREAM1_O_9_8		BIST_CHK_PREAM1_O_7_0		BIST_GEN_EN_O
R +00000		R/W +00		R/W +00000000		R/W +0

6	5	4	2	1	0
BIST_GEN_WORD_O	BIST_GEN_CDN_O	BIST_CHK_INSERT_LENGTH_O_2_0		BIST_CHK_PREAM0_O_9_8	
R/W +0	R/W +0	R/W +000		R/W +00	

Legend: R = Read only; R/W = Read/Write; -n = value after reset

Table 17-9. Register at 034 (lane_034) Field Descriptions

Bit	Field	Description
31	Reserved	Reserved - writes are ignored, always reads 0s
30 - 28	BIST_GEN_INSERT_COUNT_O_2_0	BIST generator - Number of BIST_CHK_INSERT_WORD_I words to insert at a time. If 0, no word is ever inserted into the stream. In 20-bit mode, the product of (BIST_GEN_INSERT_LENGTH x BIST_GEN_INSERT_COUNT) must be even.
27	BIST_GEN_SEND_PREAM_O	BIST generator preamble send. Valid only if generator enabled. • 0 = BIST generator sends normal data. • 1 = BIST generator sends preamble.
26 - 18	Reserved	Reserved - writes are ignored, always reads 0s
17 - 16	BIST_CHK_PREAM1_O_9_8	BIST Check Preamble word 1.
15 - 8	BIST_CHK_PREAM1_O_7_0	BIST Check Preamble word 1.
7	BIST_GEN_EN_O	BIST generator enable. • 0 = BIST generator idle. • 1=- BIST generator generates data
6	BIST_GEN_WORD_O	BIST generator word enable. • 0 = BIST generator generates single word (8 or 10) • 1 = BIST generator generates double word (16 or 20)
5	BIST_GEN_CDN_O	BIST generator master reset. 0 = Assert reset 1= De-assert reset
4 - 2	BIST_CHK_INSERT_LENGTH_O_2_0	BIST Checker Insert word length. • 0 = no insertion done • 1 = insertion length=10-bit • 2 = insertion length=20-bit • 3 = insertion length=30-bit • 4 = insertion length=40-bit The same value is applied to the BIST RX and TX.
1 - 0	BIST_CHK_PREAM0_O_9_8	BIST checker preamble word 0. When in 8b mode, and prior to the 8b/10b encoder, bit 8 is expected to be the K indicator. This word should correspond to the alignment character used for the symbol alignment block.

17.2.7 Lane_038 - Register at 038

Figure 17-10. Register at 038 (lane_038)

31 24	23 16	15 8	7 0
BIST_CHK_UDP_O_31_24	BIST_CHK_UDP_O_23_16	BIST_CHK_UDP_O_15_8	BIST_CHK_UDP_O_7_0
R/W +00000000	R/W +00000000	R/W +00000000	R/W +00000000

Legend: R/W = Read/Write; -n = value after reset

Table 17-10. Register at 038 (lane_038) Field Descriptions

Bit	Field	Description
31 - 24	BIST_CHK_UDP_O_31_24	BIST checker 40-bit user defined data pattern. In 10-bit mode, corresponds to 4 10-bit words. In 8-bit mode, corresponds to 5 8-bit words. K code is assumed to be 0 in 8-bit mode.
23 - 16	BIST_CHK_UDP_O_23_16	BIST checker 40-bit user defined data pattern. In 10-bit mode, corresponds to 4 10-bit words. In 8-bit mode, corresponds to 5 8-bit words. K code is assumed to be 0 in 8-bit mode.
15 - 8	BIST_CHK_UDP_O_15_8	BIST checker 40-bit user defined data pattern. In 10-bit mode, corresponds to 4 10-bit words. In 8-bit mode, corresponds to 5 8-bit words. K code is assumed to be 0 in 8-bit mode.
7 - 0	BIST_CHK_UDP_O_7_0	BIST checker 40-bit user defined data pattern. In 10-bit mode, corresponds to 4 10-bit words. In 8-bit mode, corresponds to 5 8-bit words. K code is assumed to be 0 in 8-bit mode.

17.2.8 Lane_03c - Register at 03c

Figure 17-11. Register at 03c (lane_03c)

31 24	23 16	15 8	7 0
BIST_CHK_INSERT_WORD_O_23_16	BIST_CHK_INSERT_WORD_O_15_8	BIST_CHK_INSERT_WORD_O_7_0	BIST_CHK_UDP_O_39_32
R/W +00000000	R/W +00000000	R/W +00000000	R/W +00000000

Legend: R/W = Read/Write; -n = value after reset

Table 17-11. Register at 03c (lane_03c) Field Descriptions

Bit	Field	Description
31 - 24	BIST_CHK_INSERT_WORD_O_23_16	BIST checker insertion word. The bottom 1,2,3, or 4 10-bit bytes are inserted into the transmitted BIST data under control of BIST_CHK_INSERT_LENGTH_O. The same word is applied to the BIST RX and TX.
23 - 16	BIST_CHK_INSERT_WORD_O_15_8	BIST checker insertion word. The bottom 1,2,3, or 4 10-bit bytes are inserted into the transmitted BIST data under control of BIST_CHK_INSERT_LENGTH_O. The same word is applied to the BIST RX and TX.
15 - 8	BIST_CHK_INSERT_WORD_O_7_0	BIST checker insertion word. The bottom 1,2,3, or 4 10-bit bytes are inserted into the transmitted BIST data under control of BIST_CHK_INSERT_LENGTH_O. The same word is applied to the BIST RX and TX.
7 - 0	BIST_CHK_UDP_O_39_32	BIST checker 40-bit user defined data pattern. In 10-bit mode, corresponds to 4 10-bit words. In 8-bit mode, corresponds to 5 8-bit words. K code is assumed to be 0 in 8-bit mode.

17.2.9 Lane_040 - Register at 040

Figure 17-12. Register at 040 (lane_040)

31 24	23 16	15 8	7 0
BIST_GEN_EN_LOW_O_15_8	BIST_GEN_EN_LOW_O_7_0	BIST_CHK_INSERT_WORD_O_39_32	BIST_CHK_INSERT_WORD_O_31_24
R/W +00000000	R/W +00000000	R/W +00000000	R/W +00000000

Legend: R/W = Read/Write; -n = value after reset

Table 17-12. Register at 040 (lane_040) Field Descriptions

Bit	Field	Description
31 - 24	BIST_GEN_EN_LOW_O_15_8	BIST generator low-period control. If not 0, output data enable will be low for this number of words, and then high for en_high_i_X:0 number of words, repeating. If 0, data output enable will be asserted for entire test.
23 - 16	BIST_GEN_EN_LOW_O_7_0	BIST generator low-period control. If not 0, output data enable will be low for this number of words, and then high for en_high_i_X:0 number of words, repeating. If 0, data output enable will be asserted for entire test.
15 - 8	BIST_CHK_INSERT_WORD_O_39_32	BIST checker insertion word. The bottom 1,2,3, or 4 10-bit bytes are inserted into the transmitted BIST data under control of BIST_CHK_INSERT_LENGTH_O. The same word is applied to the BIST RX and TX.
7 - 0	BIST_CHK_INSERT_WORD_O_31_24	BIST checker insertion word. The bottom 1,2,3, or 4 10-bit bytes are inserted into the transmitted BIST data under control of BIST_CHK_INSERT_LENGTH_O. The same word is applied to the BIST RX and TX.

17.2.10 Lane_044 - Register at 044

Figure 17-13. Register at 044 (lane_044)

31	28
Reserved	
R +0000	

27 24	23 16	15 8	7 0
BIST_GEN_INSERT_DELAY_O_11_8	BIST_GEN_INSERT_DELAY_O_7_0	BIST_GEN_EN_HIGH_O_15_8	BIST_GEN_EN_HIGH_O_7_0
R/W +00000000	R/W +00000000	R/W +00000000	R/W +00000000

Legend: R = Read only; R/W = Read/Write; -n = value after reset

Table 17-13. Register at 044 (lane_044) Field Descriptions

Bit	Field	Description
31 - 28	Reserved	Reserved - writes are ignored, always reads 0s
27 - 24	BIST_GEN_INSERT_DELAY_O_11_8	BIST generator - Number of words between insert word insertions. Insertions are done in both pream and data transmission. In 20-bit mode, this number must be even.
23 - 16	BIST_GEN_INSERT_DELAY_O_7_0	BIST generator - Number of words between insert word insertions. Insertions are done in both pream and data transmission. In 20-bit mode, this number must be even.
15 - 8	BIST_GEN_EN_HIGH_O_15_8	BIST generator high-period control. See BIST_GEN_EN_LOW_O for further information.
7 - 0	BIST_GEN_EN_HIGH_O_7_0	BIST generator high-period control. See BIST_GEN_EN_LOW_O for further information.

17.2.11 Lane_048 - Register at 048

Figure 17-14. Register at 048 (lane_048)

31	30	29	28 24	17	23 16
Reserved		GCFSM_LANE_PMA_LATCH_OVR_O	GCFSM_LANE_PMA_DATA_OVR_O_11_7		GCFSM_LANE_PMA_DATA_OVR_O_6_0	GCFSM_LANE_OUT_OVR_EN_O
R/W + 0		R/W +0			R/W +0000000	R/W +0

15 8	7 0
BIST_CHK_ERROR_15_8	BIST_CHK_ERROR_7_0
R +X	R +X

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 17-14. Register at 048 (lane_048) Field Descriptions

Bits	Name	Description
31 - 30	Reserved	Reserved
29	GCFSM_LANE_PMA_LATCH_OVR_O	GCFSM pma_latch_o override
28 - 24	GCFSM_LANE_PMA_DATA_OVR_O_11_7	GCFSM pma_data_o override data. Bits applied to PMA are [7:0]
23 - 17	GCFSM_LANE_PMA_DATA_OVR_O_6_0	GCFSM pma_data_o override data. Bits applied to PMA are [7:0]
16	GCFSM_LANE_OUT_OVR_EN_O	General Calibration Finite State Machine (GCFSM) output override enable - assertion causes data stored in gcfsm_lane_pma_data_ovr_o to override calibration values for the block selected by gcfsm_lane_pma_cal_ovr_o
15 - 8	BIST_CHK_ERROR_15_8	BIST errors detected
7 - 0	BIST_CHK_ERROR_7_0	BIST errors detected

17.2.12 Lane_058 - Register at 058

Figure 17-15. Register at 058 (lane_058)

31	30 24	23 19	18	17	16
Rsvd	DFE_TAP1_OVR_VAL_O_6_0	DFE_OFFSET_CAL_TAP_EN_OVR_O_7_3	DFE_CMP_CAL_EN_OVR_O_2	DFE_OFFSET_CAL_EN_OVR_O_1	DFE_OFFSET_CAL_VAL_OVR_EN_O_0
R/W+0	R/W +0000000	R/W +00000	R/W +0	R/W +0	R/W +0

15 0
Reserved
R +X

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 17-15. Register at 058 (lane_058) Field Descriptions

Bits	Name	Description
31	Reserved	Reserved
30 - 24	DFE_TAP1_OVR_VAL_O_6_0	DFE Tap 1 Value
23 - 19	DFE_OFFSET_CAL_TAP_EN_OVR_O_7_3	DFE offset calibration TAP enable override
18	DFE_CMP_CAL_EN_OVR_O_2	DFE comparator cal enable override
17	DFE_OFFSET_CAL_EN_OVR_O_1	DFE offset cal enable override
16	DFE_OFFSET_CAL_VAL_OVR_EN_O_0	DFE offset calibrated value override enable
15 - 0	Reserved	Reserved

17.2.13 Lane_05C - Register at 05C

Figure 17-16. Register at 05C (lane_05C)

31	30	29 24	23 22	21 16
DFE_TAP_OVR_EN_O_7	Rsvd	DFE_TAP5_OVR_VAL_O_5_0	Reserved	DFE_TAP4_OVR_VAL_O_5_0
R/W +0	R/W +0	R/W +000000	R/W +00	R/W +000000

15 14	13 8	7 6	5 0
Reserved	DFE_TAP3_OVR_VAL_O_5_0	Reserved	DFE_TAP2_OVR_VAL_O_5_0
R/W +00	R/W +000000	R/W +00	R/W +000000

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 17-16. Register at 05C (lane_05C) Field Descriptions

Bits	Name	Description
31	DFE_TAP_OVR_EN_O_7	DFE TAP override enable
30	Reserved	Reserved
29 - 24	DFE_TAP5_OVR_VAL_O_5_0	DFE Tap 5 Value
23 - 22	Reserved	Reserved
21 - 16	DFE_TAP4_OVR_VAL_O_5_0	DFE Tap 4 Value
15 - 14	Reserved	Reserved
13 - 8	DFE_TAP3_OVR_VAL_O_5_0	DFE Tap 3 Value
7 - 6	Reserved	Reserved
5 - 0	DFE_TAP2_OVR_VAL_O_5_0	DFE Tap 2 Value

17.2.14 Lane_078 - Register at 078

Figure 17-17. Register at 078 (lane_078)

31	30 24	23 15	12 11 0
Reserved	CMP_OFFSET _AVG_MAX _NUMSAMPLES _6_0	Reserved	PMA_LN_TXEQ _POLARITY _O_3_0	Reserved
R/W +1	R/W +0001111	R/W +0000	R/W +0101	R +0

Legend: R = Read only; R/W = Read/Write; -n = value after reset

Table 17-17. Register at 078 (lane_078) Field Descriptions

Bit	Field	Description
31 - 16	Reserved	Reserved
30 - 24	CMP_OFFSET_AVG_MAX _NUMSAMPLES_6 _0	Max number of samples to be used for CMP Offset Noise Averaging. The gcfsm cycle length and start length should be set to allow the averaging to complete based on the number of samples.
23 - 16	Reserved	Reserved
15 - 12	PMA_LN_TXEQ_POLARITY_O_3_0	Controls sign of each of the TX data taps, with 0 indicating positive polarity and 1 indicating negative polarity: • Bit 0 = Pre-cursor bit • Bit 1 = Current bit • Bit 2 = Post-cursor bit • Bit 3 = Second post-cursor bit
11 - 0	Reserved	Reserved

17.2.15 Lane_084 - Register at 084

Figure 17-18. Register at 084 (lane_084)

31 28	27 24	23 20	19 16
RXEQ_RATE2_BOOST_START_O_3_0	RXEQ_RATE2_ATT_START_O_3_0	RXEQ_RATE1_BOOST_START_O_3_0	RXEQ_RATE1_ATT_START_O_3_0
R/W +0110	R/W +1101	R/W +0100	R/W +1001

15 8	7 5	4 0
Reserved	PMA_LN_TX_VREG_LEV_O_2_0	Reserved
R/W +1	R/W +100	R/W +0

Legend: R/W = Read/Write; -n = value after reset

Table 17-18. Register at 084 (lane_084) Field Descriptions

Bit	Field	Description
31 - 28	RXEQ_RATE2_BOOST_START_O_3_0	Boost start value for rate2.
27 - 24	RXEQ_RATE2_ATT_START_O_3_0	ATT start value for rate2.
23 - 20	RXEQ_RATE1_BOOST_START_O_3_0	Boost start value for rate1.
19 - 16	RXEQ_RATE1_ATT_START_O_3_0	ATT start value for rate1.
15 - 8	Reserved	Reserved
7 - 5	PMA_LN_TX_VREG_LEV_O_2_0	Selects the output level for the 0.95-V TX regulator as follows. Transmit amplitude will increase in proportion to the TX regulator voltage. • 3'b000 = 0.75 V` • 3'b001 = 0.80 V • 3'b010 = 0.85 V • 3'b011 = 0.90 V • 3'b100 = 0.95 V (default) • 3'b101 = 1.00 V • 3'b110 = 1.05 V • 3'b111 = 1.10 V
4 - 0	Reserved	Reserved

17.2.16 Lane_08c - Register at 08c

Figure 17-19. Register at 08c (lane_08c)

31 16	15 12	11 8	7 0
Reserved	RXEQ_RATE3 _BOOST _START_O_3_0	RXEQ_RATE3 _ATT _START_O_3_0	Reserved
R +0	R/W +0100	R/W +1000	R +0

Legend: R = Read only; R/W = Read/Write; -n = value after reset

Table 17-19. Register at 08c (lane_08c) Field Descriptions

Bit	Field	Description
31 - 16	Reserved	Reserved
15 - 12	RXEQ_RATE3_BOOST_START_O_3_0	Boost start value for rate3.
11 - 8	RXEQ_RATE3_ATT_START_O_3_0	ATT start value for rate3.
7 - 0	Reserved	Reserved

17.2.17 Lane_0a0 - Register at 0a0

Figure 17-20. Register at 0a0 (lane_0a0)

31	30	0
TXCTRL_C1_IN_OVR_EN_O	Reserved	
R/W +0	R/W +0	

Legend: R/W = Read/Write; -n = value after reset

Table 17-20. Register at 0a0 (lane_0a0) Field Descriptions

Bit	Field	Description
31	TXCTRL_C1_IN_OVR_EN_O	Enable for register override of txctrl c1 equalizer setting during PCIe mode • 1 = enable override • 0 = disable override
30 - 0	Reserved	Reserved

17.2.18 Lane_0a8 - Register at 0a8

Figure 17-21. Register at 0a8 (lane_0a8)

31	17	16	15	0
Reserved		TXCTRL_MASTER_OVR_EN_N_O	Reserved	
R +0		R/W +0	R/W +0	

Legend: R = Read only; R/W = Read/Write; -n = value after reset

Table 17-21. Register at 0a8 (lane_0a8)Field Descriptions

Bit	Field	Description
31 - 17	Reserved	Reserved
16	TXCTRL_MASTER_OVR_EN_N_O	Master enable for override of TX controls during PCIe mode
15 - 0	Reserved	Reserved

17.3 PHY-A Common Lane Subsystem Register Definition

17.3.1 Comlane_000 - Register at 000

Figure 17-22. Register at 000 (comlane_000)

31 5	4	3	2	1	0
Reserved	L3_MASTER_CDN_O	L2_MASTER_CDN_O	L1_MASTER_CDN_O	L0_MASTER_CDN_O	LC_MASTER_CDN_O
R/W +0	R/W +0	R/W +0	R/W +0	R/W +0	R/W +0

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 17-22. Register at 000 (comlane_000) Field Descriptions

Bit	Field	Description
31 - 5	Reserved	Reserved
4	L3_MASTER_CDN_O	Lane3 master reset
3	L2_MASTER_CDN_O	Lane2 master reset
2	L1_MASTER_CDN_O	Lane1 master reset
1	L0_MASTER_CDN_O	Lane0 master reset
0	LC_MASTER_CDN_O	Common lane block master reset

17.3.2 Comlane_014 - Register at 014

Figure 17-23. Register at 014 (comlane_014)

31 25	25	24	23 0
Reserved	BIST_GEN_INV_PRBS_O	BIST_CHK_INV_PRBS_O	Reserved
R +0	R/W +0	R/W +0	R +0

Legend: R = Read only; R/W = Read/Write; -n = value after reset

Table 17-23. Register at 014 (comlane_014) Field Descriptions

Bit	Field	Description
31 - 26	Reserved	Reserved - writes are ignored, always reads 0s
25	BIST_GEN_INV_PRBS_O	Enable/Disable the internal PRBS data pattern inverter. • 0x0 = Invert the PRBS data pattern for PRBS-31 and not invert the PRBS data pattern for the other PRBS types. • 0x1 = Not invert the PRBS data pattern for PRBS-31 and invert the PRBS data pattern for the other PRBS types.
24	BIST_CHK_INV_PRBS_O	Enable/Disable the internal PRBS data pattern inverter. • 0x0 = Invert the PRBS data pattern for PRBS-31 and not invert the PRBS data pattern for the other PRBS types. • 0x1 = Not invert the PRBS data pattern for PRBS-31 and invert the PRBS data pattern for the other PRBS types.
23 - 0	Reserved	Reserved - writes are ignored, always reads 0s

17.3.3 Comlane_084 - Register at 084

Figure 17-24. Register at 084 (comlane_084)

31	11	10	9
Reserved		RXEQ_RATE3_CAL_EN_O	RXEQ_RATE2_CAL_EN_O
R/W +0		R/W +1	R/W +1

8	7	2	1	0
RXEQ_RATE1_CAL_EN_O	Reserved		RXEQ_INIT_CAL_O_1	RXEQ_INIT_CAL_O_0
R/W +1	R/W +00		R/W +1	R/W +1

Legend: R/W = Read/Write; -n = value after reset

Table 17-24. Register at 084 (comlane_084) Field Descriptions

Bit	Field	Description
31 - 11	Reserved	Reserved
10	RXEQ_RATE3_CAL_EN_O	Master enable for adaptation on rate3 (i.e. Non-PCIe mode - Full Rate, PCIe mode -N/A). The master enable supersedes all other enables
9	RXEQ_RATE2_CAL_EN_O	Master enable for adaptation on rate2 (i.e. Non-PCIe mode - Half Rate, PCIe mode - Gen2). The master enable supersedes all other enables
8	RXEQ_RATE1_CAL_EN_O	Master enable for adaptation on rate1 (i.e. Non-PCIe mode - Quarter Rate, PCIe mode - Gen1). The master enable supersedes all other enables
7 - 2	Reserved	Reserved
1	RXEQ_INIT_CAL_O_1	Enable signal for BOOST adaptation during initial calibration (for rate1/rate3)
0	RXEQ_INIT_CAL_O_0	Enable signal for ATT adaptation during initial calibration (for rate1/rate3)

17.3.4 Comlane_08c - Register at 08c

Figure 17-25. Register at 08c (comlane_08c)

31	30 26	25	24
RXEQ_RATE2_INIT_CAL_O_0	Reserved	RXEQ_RECAL_O_1	RXEQ_RECAL_O_0
R/W +1	R/W +0	R/W +1	R/W +1

23 21	20 0
TBUS_DFE_CMP_SEL_O_2_0	Reserved
R/W +000	R/W +0

Legend: R/W = Read/Write; -n = value after reset

Table 17-25. Register at 08c (comlane_08c) Field Descriptions

Bit	Field	Description
31	RXEQ_RATE2_INIT_CAL_O_0	Enables ATT calibration when asserted (rate2)
30 - 26	Reserved	Reserved
25	RXEQ_RECAL_O_1	Enable signal for BOOST adaptation during rate change (rate1/rate3)
24	RXEQ_RECAL_O_0	Enable signal for ATT adaptation during rate change (rate1/rate3)
23 - 21	TBUS_DFE_CMP_SEL_O_2_0	Selects which comparator offsets come out on tbus: • 0x1: DFE comparator 1 • 0x2: DFE Comparator 2 • 0x3: DFE comparator 3 • 0x4: DFE comparator 4 • All other values: None
20 - 0	Reserved	Reserved

17.3.5 Comlane_090 - Register at 090

Figure 17-26. Register at 090 (comlane_090)

31	15	14	13
Reserved		RXEQ_RATE2_RECAL_O_6_3	RXEQ_RATE2_RECAL_O_2_0
R/W +01010000000000000		R/W +0	R/W +1

12	1	0
Reserved		RXEQ_RATE2_INIT_CAL_O_1
R/W +00000		R/W +0

Legend: R/W = Read/Write; -n = value after reset

Table 17-26. Register at 090 (comlane_090) Field Descriptions

Bit	Field	Description
31 - 15	Reserved	Reserved
14	RXEQ_RATE2_RECAL_O_1	Enables BOOST Recal calibration when asserted (rate2)
13	RXEQ_RATE2_RECAL_O_0	Enables ATT Recal calibration when asserted (rate2)
12 - 1	Reserved	Reserved
0	RXEQ_RATE2_INIT_CAL_O_1	Enables BOOST Initial calibration when asserted (rate2)

17.3.6 Comlane_0F0 - Register at 0F0

Figure 17-27. Register at 0F0 (comlane_0F0)

31 29	28	27 26	25	24	23 0
Reserved	DFE_SHADOW_OFST_RD_SEL	DFE_SHADOW_LANE_SEL	DFE_TAP_CMP_NO_OFST_OVR_EN_O	DFE_TAP_OVR_EN_O	Reserved
R +000	R/W +0	R/W +00	R/W +0	R/W +0	R +0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 17-27. Register at 0F0 (comlane_0F0) Field Descriptions

Bit	Field	Description
31 - 29	Reserved	Reserved
28	DFE_SHADOW_OFST_RD_SEL	DFE shadow offset read select
27 - 26	DFE_SHADOW_LANE_SEL	DFE TAP shadow register lane select
25	DFE_TAP_CMP_NO_OFST_OVR_EN_O	DFE TAP CMP no offset override enable
24	DFE_TAP_OVR_EN_O	DFE TAP override enable
23 - 0	Reserved	Reserved

17.3.7 Comlane_1F8 - Register at 1F8

Figure 17-28. Register at 1F8 (comlane_1F8)

31	30	29	28	27	26	25	24	23 - 17	16
LN3_OK	LN2_OK	LN1_OK	LN0_OK	LN3_SIG_LEVEL_VALID	LN2_SIG_LEVEL_VALID	LN1_SIG_LEVEL_VALID	LN0_SIG_LEVEL_VALID	Reserved	CMU_OK
R +X	R +X	R +X	R +X	R +X	R +X	R +X	R +X	R +0000000	R +X

15 - 0
Reserved
R +0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 17-28. Register at 1f8 (lane_1f8) Field Descriptions

Bit	Field	Description
31	LN3_OK	Lane 3 OK Status
30	LN2_OK	Lane 2 OK Status
29	LN1_OK	Lane 1 OK Status
28	LN0_OK	Lane 0 OK Status
27	LN3_SIG_LEVEL_VALID	Lane 3 Signal Detect Valid Status
26	LN2_SIG_LEVEL_VALID	Lane 2 Signal Detect Valid Status
25	LN1_SIG_LEVEL_VALID	Lane 1 Signal Detect Valid Status
24	LN0_SIG_LEVEL_VALID	Lane 0 Signal Detect Valid Status
23 - 17	Reserved	Reserved
16	CMU_OK	CMU Status OK
15 - 0	Reserved	Reserved

17.4 PHY-A WIZ Subsystem Register Definition

17.4.1 LANExCTL_STS - Lane x Control and Status

The lane x control and status provides the ability to override SerDes configuration settings. It is mainly provided for test, but sometime used for mission setup as well.

Figure 17-29. Lane x Control and Status Registers (LANExCTL_STS)

31	30 29	28	27 26	25	24	23	22 21
TX0_ENABLE_OVL	TX0_ENABLE_VAL	TX0_RATE_OVL	TX0_RATE_VAL	TX0_IDLE_OVL	TX0_IDLE_VAL	TX0_WIDTH_OVL	TX0_WIDTH_VAL
R/W +0	R/W +00	R/W +0	R/W +00	R/W +0	R/W +0	R/W +0	R/W +00

20 16	15	14 13	12	11 10	9	8
Reserved	RX0_ENABLE_OVL	RX0_ENABLE_VAL	RX0_RATE_OVL	RX0_RATE_VAL	RX0_POLARITY_OVL	RX0_POLARITY_VAL
R +0	R/W +0	R/W +00	R/W +0	R/W +0	R/W +0	R/W +0

7	6	5 4	3	2	1	0
RX0_ALIGN_OVL	RX0_ALIGN_VAL	RXO_WIDTH_OVL	RX0_WIDTH_VAL	Reserved	RXO_OK	RXO_LOSS
R/W +0	R/W +0	R/W +0	R/W +00	R +0	R +0	R +0

Legend: R = Read only; R/W = Read/Write; -n = value after reset

Table 17-29. Lane x Control and Status Registers (LANExCTL_STS) Field Descriptions

Bit	Field	Description
31	TX0_ENABLE_OVL	The TX Enable Overlay bit when set allows the TX Enable Value to override the CFGTX. Enable input.
30 - 29	TX0_ENABLE_VAL	The TX Enable Value when used allows the TX lane to be placed in a • 0 = Disable state. • 1 = Sleep state. • 2 = Snooze state. • 3 = Enabled state.
28	TX0_RATE_OVL	The TX Rate Overlay bit when set allows the TX Rate Value to override the CFGTX.Rate input.
27 - 26	TX0_RATE_VAL	The TX Rate Value when used allows the TX lane to be placed into • 0 = Full Rate mode. • 1 = Half Rate mode. • 2= Quarter Rate mode.
25	TX0_IDLE_OVL	The TX Idle Overlay bit when set allows the TX Idle Value to override the CFGTX.Idle input.
24	TX0_IDLE_VAL	The TX Idle Value when used allows the TX lane to be placed electrical Idle state in non PCIe mode.
23	TX0_WIDTH_OVL	The TX Width Overlay bit when set allows the TX Width Value to override the CFGTX.Width input.
22 - 21	TX0_WIDTH_VAL	The TX Width Value when used allows the TX lane to be placed into • 0 = 10 bit mode • 2 = 20 bit mode • 3 = 16 bit mode.
20 - 16	Reserved	Reserved - writes are ignored, always reads zeros.
15	RX0_ENABLE_OVL	The RX Enable Overlay bit when set allows the RX Enable Value to override the CFGRX.Enable input.
14 - 13	RX0_ENABLE_VAL	The RX Enable Value when used allows the RX lane to be placed in a • 0 = Disable state. • 1 = Sleep state. • 2 = Snooze state. • 3 = Enabled state.
12	RX0_RATE_OVL	The RX Rate Overlay bit when set allows the RX Rate Value to override the CFGRX.Rate input.
11 - 10	RX0_RATE_VAL	The RX Rate Value when used allows the RX lane to be placed into • 0 = Full Rate mode. • 1 = Half Rate mode. • 2 = Quarter Rate mode.

Table 17-29. Lane x Control and Status Registers (LANExCTL_STS) Field Descriptions (continued)

9	RX0_POLARITY_OVL	The RX Polarity Overlay bit when set allows the RX Polarity Value to override the CFGRX.Polarity input.
8	RX0_POLARITY_VAL	The RX Polarity Value when used allows the lane RX Polarity to be inverted.
7	RX0_ALIGN_OVL	The RX Align Overlay bit when set allows the RX Align Value to override the CFGRX.Align input.
6	RX0_ALIGN_VAL	The RX Align Value when used allows the RX lane to align to K28.1, K28.5 and K28.7 characters otherwise known as Comma Characters.
5	RX0_WIDTH_OVL	The RX Width Overlay bit when set allows the RX Width Value to override the CFGRX.Width input.
4 - 3	RX0_WIDTH_VAL	The RX Width Value when used allows the RX lane to be placed into • 0 = 10 bit mode • 2 = 20 bit mode • 3 = 16 bit mode.
2	Reserved	Reserved - writes are ignored, always reads zeros.
1	RX0_OK	The RX OK indicate that the lane is in a functional state.
0	RX0_LOSS	The RX Signal Loss Indicates that the data has not been detected or the CDR is not locked.

17.4.2 PLL_CTRL - PLL Control

The PLL Control register provides the ability to override the PLL state and control events for debug purposes.

Figure 17-30. PLL Control Registers (PLL_CTRL)

31	30	29	28	27	16
PLL_ENABLE_OVL	PLL_ENABLE_VAL		PLL_OK	Reserved	
R/W +0	R/W +00		R +0	R +0	

15	12	11	8	7	4	3	0
Reserved		LN3_OK_STATE - LN0_OK_STATE		Reserved		LN3_SD_STATE - LN0_SD_STATE	
R/W +0		R +0		R/W +0		R +0	

Legend: R = Read only; R/W = Read/Write; -n = value after reset

Table 17-30. PLL Control Registers (PLL_CTRL) Field Descriptions

Bit	Field	Description
31	PLL_ENABLE_OVL	The PLL Enable Overlay bit when set allows the PLL Enable Value to override the CFGPLL.Enable input.
30 - 29	PLL_ENABLE_VAL	The PLL Enable Value when used allows the PLL to be placed in a • 0 = Disable state. • 1 = Sleep state. • 2 = Snooze state. • 3 = Enabled state.
28	PLL_OK	The PLL OK indicate that the transmit clocks are valid and the PLL circuits are ready for use.
27 - 12	Reserved	Reserved - writes are ignored, always reads zeros.
12	Reserved	Reserved
11	LN3_OK_STATE	The ln3_ok_state indicate the current state of the lane OK signal for lane 3.
10	LN2_OK_STATE	The ln2_ok_state indicate the current state of the lane OK signal for lane 2.
9	LN1_OK_STATE	The ln1_ok_state indicate the current state of the lane OK signal for lane 1.
8	LN0_OK_STATE	The ln0_ok_state indicate the current state of the lane OK signal for lane 0.
7 - 4	Reserved	Reserved
3	LN3_SD_STATE	The ln3_sd_state indicate the current state of the signal detect signal for lane 3.
2	LN2_SD_STATE	The ln2_sd_state indicate the current state of the signal detect signal for lane 2.
1	LN1_SD_STATE	The ln1_sd_state indicate the current state of the signal detect signal for lane 1.
0	LN0_SD_STATE	The ln0_sd_state indicate the current state of the signal detect signal for lane 0.

PHY B Register Definitions

This chapter describes the register definitions for PHY-B.

Topic **Page**

18.1 PHY-B CMU Subsystem Register Definition

18.1.1 Cmu_000 - Register at 000

Figure 18-1. Register at 000 (cmu_000)

31	2	1	0
Reserved		PLL_CTRL_GOOD_STATE_O	CMU_MASTER_CDN_O
R/W+1000		R/W+0	R/W+0

Legend: R = Read only; R/W = Read/Write; - *n* = value after reset

Table 18-1. Register at 000 (cmu_000) Field Descriptions

Bits	Name	Description
31 - 2	Reserved	Reserved - writes are ignored, always reads 0s.
1	PLL_CTRL_GOOD_STATE_O	State of qsample for PLL to be considered locked
0	CMU_MASTER_CDN_O	Master reset for CMU

18.1.2 Cmu_0f8 - Register at 0f8

Figure 18-2. Register at 0f8 (cmu0_0f8)

31 28	27 24	23 16	15 0
Reserved	TBUS_DATA_SMPL_11_8	TBUS_DATA_SMPL_7_0	Reserved
R+0	R+X	R+0	R+0

Legend: R = Read only; -n = value after reset

Table 18-2. Register at 0f8 (cmu0_0f8) Field Descriptions

Bits	Name	Description
31 - 28	Reserved	Reserved - writes are ignored, always reads 0s.
27 - 24	TBUS_DATA_SMPL_11_8	Snapshot of TestBus data
23 - 16	TBUS_DATA_SMPL_7_0	Snapshot of TestBus data
15 - 0	Reserved	Reserved - writes are ignored, always reads 0s.

18.1.3 Cmu_0fc - Register at 0fc

Figure 18-3. Register at 0fc (cmu0_0fc)

31 27	26 24	23 16	15 0
Reserved	TBUS_ADDR_OVR_O_10_8	TBUS_ADDR_OVR_O_7_0	Reserved
R+0	R/W-0	R/W-0	R+0

Legend: R = Read only; R/W = Read/Write; -n = value after reset

Table 18-3. Register at 0fc (cmu0_0fc) Field Descriptions

Bits	Name	Description
31 - 27	Reserved	Reserved - writes are ignored, always reads 0s.
26 - 24	TBUS_ADDR_OVR_O_10_8	Snapshot of TestBus address
23 - 16	TBUS_ADDR_OVR_O_7_0	Snapshot of TestBus address
15 - 0	Reserved	Reserved - writes are ignored, always reads 0s.

18.2 PHY-B Lane Subsystem Register Definition

18.2.1 Lane_000 - Register at 000

Figure 18-4. Register at 000 (lane_000)

31	30	29 24	23	22 20	19 16
RXCLK_LB_ENA_O	NES_LB_ENA_O	Reserved	CKTRANS_EN_O	DMUX_TXB_SEL_O_2_0	Reserved
R/W +0	R/W +0	R/W +000001	R/W +0	R/W +000	R/W +0

15 8	7 6	5 2	1	0
Reserved	DMUX_TXA_SEL_O_1_0	Reserved	RX_CLK_SRC_O	TX_CLK_SRC_O
R/W +0	R/W +00	R/W +0	R/W +1	R/W +0

Legend: R/W = Read/Write; -n = value after reset

Table 18-4. Register at 000 (lane_000) Field Descriptions

Bit	Field	Description
31	RXCLK_LB_ENA_O	HS recovered clock to transmit loopback enable
30	NES_LB_ENA_O	NES loopback enable.
29 - 24	Reserved	Reserved
23	CKTRANS_EN_O	Final transmit path output stage clock select. • 0 - Use normal transmit clock. • 1 - Use recovered RX clock as transmit clock. Used in FEP loopback only.
22 - 20	DMUX_TXB_SEL_O_2_0	Transmit mux B data input select enable - selects data passed to the TX FIFO. Effects of dmux_txb_sel_o[2:0]: • 0 = If interface PCIe loopback control=0, choose main data path (output of 8b/10b encoder). Otherwise choose recovered RX data from elastic buffer • 1 = Select output of 8b/10b encoder (main data path). • 2 = If interface PCIe loopback control=0, choose main data path (output of 8b/10b encoder). Otherwise choose recovered RX data from elastic buffer • 3 = Select BIST generator data • 4 = If interface PCIe loopback control=0, choose main data path (output of 8b/10b encoder). Otherwise choose recovered RX data from elastic buffer • 5 = Select recovered RX data from PMA • 6 = If interface PCIe loopback control=0, choose main data path (output of 8b/10b encoder). Otherwise choose recovered RX data from elastic buffer • 7 = Select recovered RX data from elastic buffer
19-8	Reserved	Reserved
7 - 6	DMUX_TXA_SEL_O_1_0	Transmit mux A data input select - selects data passed to the 8b/10b encoder: • 0 = Main TX data from SOC interface • 1 = Recovered RX data from output of 10b/8b decoder • 2 = BIST generator data • 3 = Reserved
5-2	Reserved	Reserved
1	RX_CLK_SRC_O	RX path clock select (Used only for LB_FEP mode)
0	TX_CLK_SRC_O	TX path clock select (Used only for LB_FEP mode)

18.2.2 Lane_004 - Register at 004

Figure 18-5. Register at 004 (lane_004)

31	30	29	26	25
Reserved		TXDRV_ATT_IN_OVR_O_3_0		Reserved
R/W +11		R/W +1100		R/W +00

20	19	18	17	12
Reserved		TXDRV_C2_IN_OVR_O_3	Reserved	
R +0		R/W +0	R/W +00	

11	8	7	6	5	4	3	2	1	0
Reserved		BCHK_CK_SRC_O	BCHK_SRC_O_1_0		BCHK_CLR_O	BCHK_EN_O	SIGDET_OVR_O_1_0		SOC_CK_EN_O
R/W +0000		R/W +0	R/W +0		R/W +0	R/W +0	R/W +00		R/W +0

Legend: R = Read only; R/W = Read/Write; -n = value after reset

Table 18-5. Register at 004 (lane_004) Field Descriptions

Bit	Field	Description
31 - 30	Reserved	Reserved
29 - 26	TXDRV_ATT_IN_OVR_O_3_0	Override value for TX driver ATT setting
25 - 19	Reserved	Reserved
18	TXDRV_C2_IN_OVR_O_3	Override value for TX driver c2 coefficient setting bit[3]
17 - 8	Reserved	Reserved
7	BCHK_CK_SRC_O	BIST checker, cdn is synchronized to: • 0 = RX byte Clock (PMA_LN_CLK_RXB_I) • 1 = RX lane Clock (RX_LN_CLK_I)
6 - 5	BCHK_SRC_O_1_0	BIST checker source. • 0 = BIST uses output of initial RX polbit (before Symbol Aligner) • 1 = BIST uses output of Symbol Aligner (before Elastic Buffer) • 2 = BIST uses output of RX loopback mux (before Decoder and Polbits) • 3 = BIST uses output of reg1 flop bank (before Interface blocks)
4	BCHK_CLR_O	BIST checker clear signal. Zeroes error counter output. Does NOT go through the RX BIST control block.
3	BCHK_EN_O	BIST checker enable. Enables BIST RX Control block, which enables the actual BIST RX block when appropriate.
2 - 1	SIGDET_OVR_O_1_0	Override signal detect output. Bit 1 is override enable, bit 0 is override value.
0	SOC_CK_EN_O	Select signal for TX_LNX_CLK_O (Used only for LB_FEP mode)

18.2.3 Lane_008 - Register at 008

Figure 18-6. Register at 008 (lane_008)

31	16	15	0
Reserved		TXDRV_PREEM_1LSB_MODE_0_OVR _O	
R +0		R +0	

14	12	11	8	7	5	4	0
Reserved		TXDRV_CM_IN_OVR_O_3_0		TXDRV_C2_IN_OVR_O_4_0		TXDRV_C1_IN_OVR_O_2_0	
R +001		R/W +0000		R/W +000		R/W +00010	

Legend: R/W = Read/Write; -n = value after reset

Table 18-6. Register at 008 (lane_008) Field Descriptions

Bit	Field	Description
31 - 16	Reserved	Reserved
15	TXDRV_PREEM_1LSB_MODE_0_OVR_O	Value for TX driver 1 lsb pre emphasis setting
14 - 12	Reserved	Reserved
11 - 8	TXDRV_CM_IN_OVR_O_3_0	Override value for TX driver CM coefficient setting
7- 5	TXDRV_C2_IN_OVR_O_4_0	Override value for TX driver C2 coefficient setting bits[2:0]
4 - 0	TXDRV_C1_IN_OVR_O_2_0	Override value for TX driver C1 coefficient setting

18.2.4 Lane_02C - Register at 02C

Figure 18-7. Register at 02C (lane_02C)

31	24	23	22	21	20	19	18	16
PMA_LN_EYE_DLY_O_7_0		PMA_LN_PHD_ENA_O_1_0		PMA_LN_DFE_BW_SCALE		PMA_LN_PD_DFE_BIAS	RXEQ_OVR_LOAD_EN_O_6_4	
R/W +00000000		R/W +00		R/W +00		R/W +0	R/W +000	

15	12	11	10	9	8	7	3	2	1	0
RXEQ_OVR_LOAD_EN_O_3_0		CDR_CONTROL_ATT_CTRL_O	RXEQ_OVR_LATCH_O	RXEQ_OVR_LOAD_O_6_5		RXEQ_OVR_LOAD_O_4_0		RXEQ_OVR_EN_O	RXEQ_EN_O	RXEQ_WAIT_EN_O
R/W +000		R/W +1	R/W +0	R/W +00		R/W +00000		R/W +0	R/W +1	R/W +1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18-7. Register at 02C (lane_02C) Field Descriptions

Bit	Field	Description
31 - 24	PMA_LN_EYE_DLY_O_7_0	On-chip eye diagram X-direction offset control: Bit 9: unused Bits 8-7: Coarse x-direction offset, in steps of 1/2UI Bits 6-0: Fine x-direction offset
23 - 22	PMA_LN_PHD_ENA_O_1_0	• Bit 1: 1 - disables updates from D4/D3 data/edge samplers to VCO 0 - enables updates from D4/D3 data/edge samplers to VCO • Bit 0: 1 - disables updates from D1/D2 data/edge samplers to VCO 0 - enables updates from D1/D2 data/edge samplers to VCO
21 - 20	PMA_LN_DFE_BW_SCALE	DFE Bandwidth Selection: DFE_BW_SCALE[1:0] DFE comparator BW compared to full speed • 2'b00: 1/4 speed • 2'b01: 1/2 speed • 2'b10: 3/4 speed • 2'b11: Full speed
19	PMA_LN_PD_DFE_BIAS	Override for DFE bias powerdown from MSM. Enabled through assertion of msm_out_ovr_en. Assertion disables DFE. Allow >5us recovery time after de-assertion.
18 - 16	RXEQ_OVR_LOAD_EN_O_6_4	Override enable for AFE dfe tap1 inputs
15 - 12	RXEQ_OVR_LOAD_EN_O_3_0	Override enable for AFE dfe tap1 inputs
11	CDR_CONTROL_ATT_CTRL_O	ATT wait control. Upon detection of signal, DFE ATT calibration is enabled, without CISEL being asserted to the CDR. • 0 - CDR control block will wait for ATT calibration before proceeding • 1 - CDR control block will not wait for ATT calibration
10	RXEQ_OVR_LATCH_O	Override for DFE latch signal. Negative edge causes AFE to store values of DFE output registers.
9 - 8	RXEQ_OVR_LOAD_O_6_5	Override for DFE output register load value.
7 - 3	RXEQ_OVR_LOAD_O_4_0	Override for DFE output register load value.
2	RXEQ_OVR_EN_O	Override enable for DFE signals.
1	RXEQ_EN_O	DFE block enable signal.
0	RXEQ_WAIT_EN_O	CDR control block wait for DFE signal. • 0 - Do not wait for DFE calibration before enabling rx data • 1 - Wait for DFE calibration before enabling rx data

18.2.5 Lane_030 - Register at 030

Figure 18-8. Register at 030 (lane_030)

31	24	23	22	21 19	18	17	16
BIST_CHK_PREAM0_O_7_0		BIST_RX_CLOCK_ENABLE	BIST_TX_CLOCK_ENABLE	BIST_CHK_LFSR_LENGTH_O_2_0	BIST_CHK_DATA_MODE_O	Rsvd	BIST_GEN_MODE8B_O
R/W +00000000		R/W +0	R/W +0	R/W +000	R/W +0	R+0	R/W +0

15 14	13 12	11	10 0
Reserved	RXEQ_ATT_GAIN_OVR	RXEQ_ATT_GAIN_AUTOCAL_DIS	Reserved
R/W +00	R/W +00	R/W +0	R/W +0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18-8. Register at 030 (lane_030) Field Descriptions

Bit	Field	Description
31 - 24	BIST_CHK_PREAM0_O_7_0	BIST checker preamble word 0. When in 8b mode, and prior to the 8b/10b encoder, bit 8 is expected to be the K indicator. This word should correspond to the alignment character used for the symbol alignment block.
23	BIST_RX_CLOCK_ENABLE	Active HIGH clock enable signal for the BIST receive clock.
22	BIST_TX_CLOCK_ENABLE	Active HIGH clock enable signal for the BIST transmit clock
21 - 19	BIST_CHK_LFSR_LENGTH_O_2_0	BIST PRBS pattern selector. bist_gen_mode8b_o=0, bist_gen_word_o=0: • 0 = PRBS7 with 10-bit bus width • 1 = PRBS15 with 10-bit bus width • 2 = PRBS23 with 10-bit bus width • 3 = PRBS31 with 10-bit bus width bist_gen_mode8b_o=0,bist_gen_word_o=1: • 0 = PRBS7 with 20-bit bus width • 1 = PRBS15 with 20-bit bus width • 2 = PRBS23 with 20-bit bus width • 3 = PRBS31 with 20-bit bus width bist_gen_mode8b_o=1, bist_gen_word_o=0: • 0 = PRBS7 with 8-bit bus width • 1 = PRBS15 with 8-bit bus width • 2 = PRBS23 with 8-bit bus width • 3 = PRBS31 with 8-bit bus width bist_gen_mode8b_o=1, bist_gen_word_o=1: • 0 = PRBS7 with 16-bit bus width • 1 = PRBS15 with 16-bit bus width • 2 = PRBS23 with 16-bit bus width • 3 = PRBS31 with 16-bit bus width
18	BIST_CHK_DATA_MODE_O	BIST checker mode select. • 0x0 = UDP pattern. • 0x1 = PRBS pattern
17	Reserved	Reserved - writes are ignored, always reads 0s
16	BIST_GEN_MODE8B_O	BIST generator 8b mode control • 0 - Generated data word is 10 bits • 1 - Generated data word is 8 bits
15 - 14	Reserved	Reserved
13 - 12	RXEQ_ATT_GAIN_OVR	Override for the value of rx_att_gain when rxeq_att_gain_autocal_dis=1
11	RXEQ_ATT_GAIN_AUTOCAL_DIS	Disable auto cal of RXEQ gain control (rx_att_gain).

Table 18-8. Register at 030 (lane_030) Field Descriptions (continued)

10 - 0	Reserved	Reserved

18.2.6 Lane_034 - Register at 034

Figure 18-9. Register at 034 (lane_034)

31	30	28	27
Reserved	BIST_GEN_INSERT_COUNT_O_2_0		BIST_GEN_SEND_PREAM_O
R +0	R/W +000		R/W +0

26	24	23	18	17	16	15	8	7
Reserved		Reserved		BIST_CHK_PREAM1_O_9_8		BIST_CHK_PREAM1_O_7_0		BIST_GEN_EN_O
R/W +000		R +00000		R/W +00		R/W +00000000		R/W +0

6	5	4	2	1	0
BIST_GEN_WORD_O	BIST_GEN_CDN_O	BIST_CHK_INSERT_LENGTH_O_2_0		BIST_CHK_PREAM0_O_9_8	
R/W +0	R/W +0	R/W +000		R/W +00	

Legend: R = Read only; R/W = Read/Write; -n = value after reset

Table 18-9. Register at 034 (lane_034) Field Descriptions

Bit	Field	Description
31	Reserved	Reserved - writes are ignored, always reads 0s
30 - 28	BIST_GEN_INSERT_COUNT_O_2_0	BIST generator - Number of BIST_CHK_INSERT_WORD_I words to insert at a time. If 0, no word is ever inserted into the stream. In 20-bit mode, the product of (bist_gen_insert_length x bist_gen_insert_count) must be even.
27	BIST_GEN_SEND_PREAM_O	BIST generator preamble send. Valid only if generator enabled. • 0 = BIST generator sends normal data. • 1 = BIST generator sends preamble.
26 - 18	Reserved	Reserved - writes are ignored, always reads 0s
17 - 16	BIST_CHK_PREAM1_O_9_8	BIST Check Preamble word 1.
15 - 8	BIST_CHK_PREAM1_O_7_0	BIST Check Preamble word 1.
7	BIST_GEN_EN_O	BIST generator enable. • 0 = BIST generator idle. • 1=- BIST generator generates data
6	BIST_GEN_WORD_O	BIST generator word enable. • 0 = BIST generator generates single word (8 or 10) • 1 = BIST generator generates double word (16 or 20)
5	BIST_GEN_CDN_O	BIST generator master reset. 0 = Assert reset 1= De-assert reset
4 - 2	BIST_CHK_INSERT_LENGTH_O_2_0	BIST Checker Insert word length. • 0 = no insertion done • 1 = insertion length=10-bit • 2 = insertion length=20-bit • 3 = insertion length=30-bit • 4 = insertion length=40-bit The same value is applied to the BIST RX and TX.
1 - 0	BIST_CHK_PREAM0_O_9_8	BIST checker preamble word 0. When in 8b mode, and prior to the 8b/10b encoder, bit 8 is expected to be the K indicator. This word should correspond to the alignment character used for the symbol alignment block.

18.2.7 Lane_038 - Register at 038

Figure 18-10. Register at 038 (lane_038)

31 24	23 16	15 8	7 0
BIST_CHK_UDP_O_31_24	BIST_CHK_UDP_O_23_16	BIST_CHK_UDP_O_15_8	BIST_CHK_UDP_O_7_0
R/W +00000000	R/W +00000000	R/W +00000000	R/W +00000000

Legend: R/W = Read/Write; -n = value after reset

Table 18-10. Register at 038 (lane_038) Field Descriptions

Bit	Field	Description
31 - 24	BIST_CHK_UDP_O_31_24	BIST checker 40-bit user defined data pattern. In 10-bit mode, corresponds to 4 10-bit words. In 8-bit mode, corresponds to 5 8-bit words. K code is assumed to be 0 in 8-bit mode.
23 - 16	BIST_CHK_UDP_O_23_16	BIST checker 40-bit user defined data pattern. In 10-bit mode, corresponds to 4 10-bit words. In 8-bit mode, corresponds to 5 8-bit words. K code is assumed to be 0 in 8-bit mode.
15 - 8	BIST_CHK_UDP_O_15_8	BIST checker 40-bit user defined data pattern. In 10-bit mode, corresponds to 4 10-bit words. In 8-bit mode, corresponds to 5 8-bit words. K code is assumed to be 0 in 8-bit mode.
7 - 0	BIST_CHK_UDP_O_7_0	BIST checker 40-bit user defined data pattern. In 10-bit mode, corresponds to 4 10-bit words. In 8-bit mode, corresponds to 5 8-bit words. K code is assumed to be 0 in 8-bit mode.

18.2.8 Lane_03c - Register at 03c

Figure 18-11. Register at 03c (lane_03c)

31 24	23 16	15 8	7 0
BIST_CHK_INSERT_WORD_O_23_16	BIST_CHK_INSERT_WORD_O_15_8	BIST_CHK_INSERT_WORD_O_7_0	BIST_CHK_UDP_O_39_32
R/W +00000000	R/W +00000000	R/W +00000000	R/W +00000000

Legend: R/W = Read/Write; -n = value after reset

Table 18-11. Register at 03c (lane_03c) Field Descriptions

Bit	Field	Description
31 - 24	BIST_CHK_INSERT_WORD_O_23_16	BIST checker insertion word. The bottom 1,2,3, or 4 10-bit bytes are inserted into the transmitted BIST data under control of BIST_CHK_INSERT_LENGTH_O. The same word is applied to the BIST RX and TX.
23 - 16	BIST_CHK_INSERT_WORD_O_15_8	BIST checker insertion word. The bottom 1,2,3, or 4 10-bit bytes are inserted into the transmitted BIST data under control of BIST_CHK_INSERT_LENGTH_O. The same word is applied to the BIST RX and TX.
15 - 8	BIST_CHK_INSERT_WORD_O_7_0	BIST checker insertion word. The bottom 1,2,3, or 4 10-bit bytes are inserted into the transmitted BIST data under control of BIST_CHK_INSERT_LENGTH_O. The same word is applied to the BIST RX and TX.
7 - 0	BIST_CHK_UDP_O_39_32	BIST checker 40-bit user defined data pattern. In 10-bit mode, corresponds to 4 10-bit words. In 8-bit mode, corresponds to 5 8-bit words. K code is assumed to be 0 in 8-bit mode.

18.2.9 Lane_040 - Register at 040

Figure 18-12. Register at 040 (lane_040)

31 24	23 16	15 8	7 0
BIST_GEN_EN_LOW_O_15_8	BIST_GEN_EN_LOW_O_7_0	BIST_CHK_INSERT_WORD_O_39_32	BIST_CHK_INSERT_WORD_O_31_24
R/W +00000000	R/W +00000000	R/W +00000000	R/W +00000000

Legend: R/W = Read/Write; -n = value after reset

Table 18-12. Register at 040 (lane_040) Field Descriptions

Bit	Field	Description
31 - 24	BIST_GEN_EN_LOW_O_15_8	BIST generator low-period control. If not 0, output data enable will be low for this number of words, and then high for en_high_i_X:0 number of words, repeating. If 0, data output enable will be asserted for entire test.
23 - 16	BIST_GEN_EN_LOW_O_7_0	BIST generator low-period control. If not 0, output data enable will be low for this number of words, and then high for en_high_i_X:0 number of words, repeating. If 0, data output enable will be asserted for entire test.
15 - 8	BIST_CHK_INSERT_WORD_O_39_32	BIST checker insertion word. The bottom 1,2,3, or 4 10-bit bytes are inserted into the transmitted BIST data under control of BIST_CHK_INSERT_LENGTH_O. The same word is applied to the BIST RX and TX.
7 - 0	BIST_CHK_INSERT_WORD_O_31_24	BIST checker insertion word. The bottom 1,2,3, or 4 10-bit bytes are inserted into the transmitted BIST data under control of BIST_CHK_INSERT_LENGTH_O. The same word is applied to the BIST RX and TX.

18.2.10 Lane_044 - Register at 044

Figure 18-13. Register at 044 (lane_044)

31	28
Reserved	
R +0000	

27 24	23 16	15 8	7 0
BIST_GEN_INSERT_DELAY_O_11_8	BIST_GEN_INSERT_DELAY_O_7_0	BIST_GEN_EN_HIGH_O_15_8	BIST_GEN_EN_HIGH_O_7_0
R/W +00000000	R/W +00000000	R/W +00000000	R/W +00000000

Legend: R = Read only; R/W = Read/Write; -n = value after reset

Table 18-13. Register at 044 (lane_044) Field Descriptions

Bit	Field	Description
31 - 28	Reserved	Reserved - writes are ignored, always reads 0s
27 - 24	BIST_GEN_INSERT_DELAY_O_11_8	BIST generator - Number of words between insert word insertions. Insertions are done in both pream and data transmission. In 20-bit mode, this number must be even.
23 - 16	BIST_GEN_INSERT_DELAY_O_7_0	BIST generator - Number of words between insert word insertions. Insertions are done in both pream and data transmission. In 20-bit mode, this number must be even.
15 - 8	BIST_GEN_EN_HIGH_O_15_8	BIST generator high-period control. See BIST_GEN_EN_LOW_O for further information.
7 - 0	BIST_GEN_EN_HIGH_O_7_0	BIST generator high-period control. See BIST_GEN_EN_LOW_O for further information.

18.2.11 Lane_048 - Register at 048

Figure 18-14. Register at 048 (lane_048)

31 30	29	28 24	23 17	16	15 8	7 0
Reserved	GCFSM_LANE_PMA _LATCH_OVR_O	Reserved	GCFSM_LANE_PMA _DATA_OVR_O_6_0	GCFSM_LANE_OUT _OVR_EN_O	BIST_CHK_ERROR_15_8	BIST_CHK_ERROR_7_0
R/W+0	R/W+0	R/W+00000	R/W+0000000	R/W+0	R+X	R+X

Legend: R = Read only; R/W = Read/Write; -n = value after reset

Table 18-14. Register at 048 (lane_048) Field Descriptions

Bits	Name	Description
31 - 30	Reserved	Reserved
29	GCFSM_LANE_PMA_LATCH_OVR_O	GCFSM pma_latch_o override
28 - 24	Reserved	Reserved
23 -17	GCFSM_LANE_PMA_DATA_OVR_O_6_0	GCFSM pma_data_o override data
16	GCFSM_LANE_OUT_OVR_EN_O	General Calibration Finite State Machine (GCFSM) output override enable - assertion causes data stored in gcfsm_lane_pma_data_ovr_o to override calibration values for the block selected by gcfsm_lane_pma_cal_ovr_o
15 - 8	BIST_CHK_ERROR_15_8	BIST errors detected
7 - 0	BIST_CHK_ERROR_7_0	BIST errors detected

18.2.12 Lane_058 - Register at 058

Figure 18-15. Register at 058 (lane_058)

31	30 24	23 19	18	17	16
Rsvd	DFE_TAP1_OVR_VAL_O_6_0	DFE_OFFSET_CAL_TAP_EN_OVR_O_7_3	DFE_CMP_CAL_EN_OVR_O_2	DFE_OFFSET_CAL_EN_OVR_O_1	DFE_OFFSET_CAL_VAL_OVR_EN_O_0
R/W+0	R/W +0000000	R/W +00000	R/W +0	R/W +0	R/W +0

15 0
Reserved
R +0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18-15. Register at 058 (lane_058) Field Descriptions

Bits	Name	Description
31	Reserved	Reserved
30 - 24	DFE_TAP1_OVR_VAL_O_6_0	DFE Tap 1 Value
23 - 19	DFE_OFFSET_CAL_TAP_EN_OVR_O_7_3	DFE offset calibration TAP enable override
18	DFE_CMP_CAL_EN_OVR_O_2	DFE comparator cal enable override
17	DFE_OFFSET_CAL_EN_OVR_O_1	DFE offset cal enable override
16	DFE_OFFSET_CAL_VAL_OVR_EN_O_0	DFE offset calibrated value override enable
15 - 0	Reserved	Reserved

18.2.13 Lane_05C - Register at 05C

Figure 18-16. Register at 05C (lane_05C)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DFE_TAP_OVR_EN_O_7	Rsvd	DFE_TAP5_OVR_VAL_O_5_0						Reserved		DFE_TAP4_OVR_VAL_O_5_0					
R/W +0	R/W +0	R/W +000000						R/W +00		R/W +000000					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		DFE_TAP3_OVR_VAL_O_5_0						Reserved		DFE_TAP2_OVR_VAL_O_5_0					
R/W +00		R/W +000000						R/W +00		R/W +000000					

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18-16. Register at 05C (lane_05C) Field Descriptions

Bits	Name	Description
31	DFE_TAP_OVR_EN_O_7	DFE TAP override enable
30	Reserved	Reserved
29 - 24	DFE_TAP5_OVR_VAL_O_5_0	DFE Tap 5 Value
23 - 22	Reserved	Reserved
21 - 16	DFE_TAP4_OVR_VAL_O_5_0	DFE Tap 4 Value
15 - 14	Reserved	Reserved
13 - 8	DFE_TAP3_OVR_VAL_O_5_0	DFE Tap 3 Value
7 - 6	Reserved	Reserved
5 - 0	DFE_TAP2_OVR_VAL_O_5_0	DFE Tap 2 Value

18.2.14 Lane_060 - Register at 060

Figure 18-17. Register at 060 (lane_060)

31	16
Reserved	
R/W +00	

15	2	1	0
Reserved		PMA_TXCLK_SEL_O_1	PMA_CMU_SEL_O_0
R +0		R/W +0	R/W +0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18-17. Register at 05C (lane_05C) Field Descriptions

Bits	Name	Description
31 - 2	Reserved	Reserved. Always reads 0, writes are ignored.
1	PMA_TXCLK_SEL_O_1	PMA TX Clock Select for TX CDR VCO • 0 -> CMU0 Clock • 1 -> CMU1 Clock
0	PMA_CMU_SEL_O_0	CMU Select for lane • 0 -> Select CMU0 (set to this value for single- CMU implementation) • 1 -> Select CMU1

18.2.15 Lane_078 - Register at 078

Figure 18-18. Register at 078 (lane_078)

31	17
Reserved	
R +0	

16	15	12	11	0
Reserved	PMA_LN_TXEQ_POLARITY_O_3_0		Reserved	
R/W +0	R/W +0101		R/W +0	

Legend: R = Read only; R/W = Read/Write; -n = value after reset

Table 18-18. Register at 078 (lane_078) Field Descriptions

Bit	Field	Description
31 - 16	Reserved	Reserved
15 - 12	PMA_LN_TXEQ_POLARITY_O_3_0	Controls sign of each of the TX data taps, with 0 indicating positive polarity and 1 indicating negative polarity: • Bit 0 = Pre-cursor bit • Bit 1 = Current bit • Bit 2 = Post-cursor bit • Bit 3 = Second post-cursor bit
11 - 0	Reserved	Reserved

18.2.16 Lane_084 - Register at 084

Figure 18-19. Register at 084 (lane_084)

31 28	27 24	23 20	19 16
RXEQ_RATE2_BOOST_START_O_3_0	RXEQ_RATE2_ATT_START_O_3_0	RXEQ_RATE1_BOOST_START_O_3_0	RXEQ_RATE1_ATT_START_O_3_0
R/W +0110	R/W +1011	R/W +0010	R/W _+1001

15 0
Reserved
R +0

Legend: R = Read only; R/W = Read/Write; -n = value after reset

Table 18-19. Register at 084 (lane_084) Field Descriptions

Bit	Field	Description
31 - 28	RXEQ_RATE2_BOOST_START_O_3_0	Boost start value for rate2.
27 - 24	RXEQ_RATE2_ATT_START_O_3_0	ATT start value for rate2.
23 - 20	RXEQ_RATE1_BOOST_START_O_3_0	Boost start value for rate1.
19 - 16	RXEQ_RATE1_ATT_START_O_3_0	ATT start value for rate1.
15 - 0	Reserved	Reserved

18.2.17 Lane_08c - Register at 08c

Figure 18-20. Register at 08c (lane_08c)

31 16	15 12	11 8	7 0
Reserved	RXEQ_RATE3 _BOOST _START_O_3_0	RXEQ_RATE3 _ATT _ START_O_3_0	Reserved
R +0	R/W +1001	R/W +1111	R +0

Legend: R = Read only; R/W = Read/Write; -n = value after reset

Table 18-20. Register at 08c (lane_08c) Field Descriptions

Bit	Field	Description
31 - 16	Reserved	Reserved
15 - 12	RXEQ_RATE3_BOOST_START_O_3_0	BOOST start value for rate3.
11 - 8	RXEQ_RATE3_ATT_START_O_3_0	ATT start value for rate3.
7 - 0	Reserved	Reserved

18.2.18 lane_098 - Register at 098

Figure 18-21. Register at 098 (lane_098)

31	17
Reserved	
R/W +0	

16	15	14	13	12	11
Reserved		RXEQ_LN_FORCE_CAL_O_6	RXEQ_RATE3_CAL_EN_O	RXEQ_RATE2_CAL_EN_O	RXEQ_RATE1_CAL_EN_O
R/W +0		R/W +0	R/W +1	R/W +1	R/W +1

10	3	2	1	0
Reserved				
R/W +0				

Legend: R = Read only; R/W = Read/Write; -n = value after reset

Table 18-21. Register at 098 (lane_098) Field Descriptions

Bit	Field	Description
31 - 15	Reserved	Reserved
14	RXEQ_LN_FORCE_CAL_O_6	Force enable for RX ATT/BOOST re-adaptation. Bit must be set then cleared to force RX re-adaptation.
13	RXEQ_RATE3_CAL_EN_O	Master enable for adaptation rate 3 (i.e. Full Rate). The master enable supersedes all other enables
12	RXEQ_RATE2_CAL_EN_O	Master enable for adaptation rate 2 (i.e.Half Rate). The master enable supersedes all other enables
11	RXEQ_RATE1_CAL_EN_O	Master enable for adaptation rate 1 (i.e. Quarter Rate). The master enable supersedes all other enables
10 - 0	Reserved	Reserved

18.2.19 Lane_09c - Register at 09c

Figure 18-22. Register at 09c (lane_09c)

31	2	1	0
Reserved		RXEQ_INIT_CAL_O_1	RXEQ_INIT_CAL_O_0
R+0		R/W +1111111	R/W +1111111

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18-22. Register at 09c (lane_09c) Field Descriptions

Bit	Field	Description
31 - 2	Reserved	Reserved
1	RXEQ_INIT_CAL_O_1	Enable signal for BOOST adaptation during initial calibration (for rate1/rate3)
0	RXEQ_INIT_CAL_O_0	Enable signal for ATT adaptation during initial calibration (for rate1/rate3)

18.2.20 Lane_0a4 - Register at 0a4

Figure 18-23. Register at 0a4 (lane_0a4)

31	5	4	0
Reserved		PMA_LN_TX_VREG_LEV_O_4_0	
R/W +0		R/W +01010	

Legend: R = Read only; R/W = Read/Write; -n = value after reset

Table 18-23. Register at 0a4 (lane_0a4) Field Descriptions

Bit	Field	Description
31 - 5	Reserved	Reserved
4 - 0	PMA_LN_TX_VREG_LEV_O_4_0	Selects regulator voltage setting for TX driver slices. Transmit voltage increases with increase in register setting according to the following equation: 730 mV + 12.5 mV*PMA_LN_TX_VREG_LEV_O Note: PMA_LN_TX_VREG_LEV setting should not be set higher than 0.95V for long term reliability reasons.

18.3 PHY-B Common Lane Subsystem Register Definition

18.3.1 Comlane_014 - Register at 014

Figure 18-24. Register at 014 (comlane_014)

31	26	25	24	23	0
Reserved		BIST_GEN_INV_PRBS_O	BIST_CHK_INV_PRBS_O	Reserved	
R +0		R/W +0	R/W +0	R +0	

Legend: R = Read only; R/W = Read/Write; -n = value after reset

Table 18-24. Register at 014 (comlane_014) Field Descriptions

Bit	Field	Description
31 - 26	Reserved	Reserved - writes are ignored, always reads 0s
25	BIST_GEN_INV_PRBS_O	Enable/Disable the internal PRBS data pattern inverter. • 0x0 = Invert the PRBS data pattern for PRBS-31 and not invert the PRBS data pattern for the other PRBS types. • 0x1 = Not invert the PRBS data pattern for PRBS-31 and invert the PRBS data pattern for the other PRBS types.
24	BIST_CHK_INV_PRBS_O	Enable/Disable the internal PRBS data pattern inverter. • 0x0 = Invert the PRBS data pattern for PRBS-31 and not invert the PRBS data pattern for the other PRBS types. • 0x1 = Not invert the PRBS data pattern for PRBS-31 and invert the PRBS data pattern for the other PRBS types.
23 - 0	Reserved	Reserved - writes are ignored, always reads 0s

18.3.2 Comlane_08c - Register at 08c

Figure 18-25. Register at 08c (comlane_08c)

31	30 26	25	24
RXEQ_RATE2_INIT_CAL_O_0	Reserved	RXEQ_RECAL_O_1	RXEQ_RECAL_O_0
R/W +1	R/W +1111	R/W +1	R/W +1

23 0
Reserved
R/W +0011

Legend: R/W = Read/Write; -n = value after reset

Table 18-25. Register at 08c (comlane_08c) Field Descriptions

Bit	Field	Description
31	RXEQ_RATE2_INIT_CAL_O_0	Enables ATT Initial calibration when asserted (rate2)
30 - 26	Reserved	Reserved
25	RXEQ_RECAL_O_1	Enable signal for BOOST Recal adaptation during rate change (rate1/rate3)
24	RXEQ_RECAL_O_0	Enable signal for ATT Recal adaptation during rate change (rate1/rate3)
23 - 0	Reserved	Reserved

18.3.3 Comlane_090 - Register at 090

Figure 18-26. Register at 090 (comlane_090)

31				15
Reserved				
R/W +0101				
14	13	12	1	0
RXEQ_RATE2_RECAL_O_1	RXEQ_RATE2_RECAL_O_0	Reserved		RXEQ_RATE2_INIT_CAL_O_1
R/W +1	R/W +1	R/W +00		R/W +0

Legend: R/W = Read/Write; -n = value after reset

Table 18-26. Register at 090 (comlane_090) Field Descriptions

Bit	Field	Description
31 - 15	Reserved	Reserved
14	RXEQ_RATE2_RECAL_O_1	Enables BOOST Recal calibration when asserted (rate 2)
13	RXEQ_RATE2_RECAL_O_0	Enables ATT Recal calibration when asserted (rate 2)
12 - 1	Reserved	Reserved
0	RXEQ_RATE2_INIT_CAL_O_1	Enables BOOST Initial calibration when asserted (rate 2)

18.3.4 Comlane_098 - Register at 098

Figure 18-27. Register at 098 (comlane_098)

31 25	24	23 0
Reserved	CMP_OFFSET_OVR_EN_O	Reserved
R +0	R/W +0	R+0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18-27. Register at 098 (comlane_098) Field Descriptions

Bit	Field	Description
31 - 25	Reserved	Reserved
24	CMP_OFFSET_OVR_EN_O	Comparator Offset Override enable
23 - 0	Reserved	Reserved

18.3.5 Comlane_09C - Register at 09C

Figure 18-28. Register at 09C (comlane_09c)

31	8	7	0
Reserved		CMP_OFFSET_OVR_O_7_0	
R +0		R/W +00000000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18-28. Register at 09C (comlane_09C) Field Descriptions

Bit	Field	Description
31 - 8	Reserved	Reserved - writes are ignored, always reads zeros.
7 - 0	CMP_OFFSET_OVR_O_7_0	Comparator Offset Override Values

18.3.6 Comlane_0BC - Register at 0BC

Figure 18-29. Register at 0BC (comlane_0BC)

31 29	28 24	23 20	19 18 17 16
Reserved	RXEQ_RATE3_DFE_TAP_PD_O_4_0	Reserved	EYE_SCAN_WAIT_LEN_O_15_12
R/W +111	R/W +11111	R/W +0000	R/W +0000

15 8	7 4	3 0
EYE_SCAN_WAIT_LEN_O_11_4	EYE_SCAN_WAIT_LEN_O_3_0	EYE_SCAN_MASK_O_18_15
R/W +00000000	R/W +0000	R/W +0000

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18-29. Register at 0BC (comlane_0BC) Field Descriptions

Bit	Field	Description
31 - 29	Reserved	Reserved
28 - 24	RXEQ_RATE3_DFE_TAP_PD_O_4_0	Sets the DFE tap powerdown for rate3 • Bit [0]: Powers down tap 1 • Bit [1]: Powers down tap 2 • Bit [2]: Powers down tap 3 • Bit [3]: Powers down tap 4 • Bit [4]: Powers down tap 5
23 -20	Reserved	Reserved
19 - 16	EYE_SCAN_WAIT_LEN_O_15_12	Bits 15-12 of eye scan wait time used by the eye scan counter block
15 - 8	EYE_SCAN_WAIT_LEN_O_11_4	Bits 11-4 of eye scan wait time used by the eye scan counter block
7 - 4	EYE_SCAN_WAIT_LEN_O_3_0	Bits 3-0 of eye scan wait time used by the eye scan counter block
3 - 0	EYE_SCAN_MASK_O_18_15	Mask for eye scan results

18.3.7 Comlane_0F0- Register at 0F0

Figure 18-30. Register at 0F0 (comlane_0F0)

31 28	27 26	25 0
Reserved	DFE _SHADOW _LANE_SEL	Reserved
R/W +0000	R/W +00	R/W +00000000001010010100000001

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18-30. Register at 0F0 (comlane_0F0) Field Descriptions

Bit	Field	Description
31 - 28	Reserved	Reserved
27 - 26	DFE_SHADOW_LANE_SEL	DFE TAP shadow register lane select
25 - 0	Reserved	Reserved

18.3.8 Comlane_1F8 - Register at 1F8

Figure 18-31. Register at 1F8 (comlane_1F8)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		LN1_OK_I_5	LN0_OK_I_4	Reserved		LN1_SIG_LEVEL_VALID_I_1	LN0_SIG_LEVEL_VALID_I_0	Reserved						CMU1_OK_I_1	CMU_OK_I_0
R +X		R +X	R +X	R +X		R +X	R +X	R +0						R +X	R +X

15	0
Reserved	
R +0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18-31. Register at 1f8 (comlane_1f8) Field Descriptions

Bit	Field	Description
31 - 30	Reserved	Reserved
29	LN1_OK_I_5	Lane 1 OK Status
28	LN0_OK_I_4	Lane 0 OK Status
27 - 26	Reserved	Reserved
25	LN1_SIG_LEVEL_VALID_I_1	Lane 1 Signal Detect Valid Status
24	LN0_SIG_LEVEL_VALID_I_0	Lane 0 Signal Detect Valid Status
23 - 18	Reserved	Reserved
17	CMU1_OK	CMU1 Status OK
16	CMU0_OK	CMU0 Status OK
15 - 0	Reserved	Reserved

18.4 PHY-B WIZ Subsystem Register Definition

18.4.1 MEM_ADR - Memory Address Register

Figure 18-32. Memory Address Register (MEM_ADR)

31	16	15	2	1	0
Reserved		MEM_ADR		Rsvd	
R +0		R/W +00000000000000		R +0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18-32. Memory Address Register (MEM_ADR) Field Descriptions

Bit	Field	Description
31 - 16	Reserved	Reserved - writes are ignored, always reads zeros.
15 - 2	MEM_ADR	Defines the word index used to access the internal memory
1 - 0	Reserved	Reserved - writes are ignored, always reads zeros.

18.4.2 MEM_DAT - Memory Data Portal Register

Figure 18-33. Memory Data Portal Register (MEM_DAT)

31	0
MEM_DAT	
R/W +00000000000000000000000000000000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18-33. Memory Data Portal Register (MEM_DAT) Field Descriptions

Bit	Field	Description
31 - 0	MEM_DAT	Defines the data written to or read from the address MEM_ADR

18.4.3 MEM_DATINC - Memory Data Increment Portal Register

Figure 18-34. Memory Data Increment Portal Register (MEM_DATINC)

31	0
MEM_DATINC	
R/W +00000000000000000000000000000000	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18-34. Memory Data Increment Portal Register (MEM_DATINC) Field Descriptions

Bit	Field	Description
31 - 0	MEM_DATINC	Defines the data written to or read from the address MEM_ADR. After reading or writing this register the MEM_ADR is auto-incremented

18.4.4 CPU_CTRL - CPU Control Register

Figure 18-35. CPU Control Register (CPU_CTRL)

31	30	29	28	27	26	25 23	22 0
CPU_EN	CPU_GO	POR_EN	CPUREG_EN	AUTONEG_CTL	DATA SPLIT	Rsvd	CPUMEMADDRESS
R/W +0	R/W+0	R/W +0	R/W+0	R/W +0	R/W+0	R +0	R +00000000000000000000000

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18-35. Register at 108 (comlane_108) Field Descriptions

Bit	Field	Description
31	CPU_EN	Disables the CMU Wait control and allow the CPU to take control of the delays
30	CPU_GO	Enables the CPU to read or write the program/data memory.
29	POR_EN	Allows the system to place the SERDES in a reset state, Access to the SERDES registers is ignored.
28	CPUREG_EN	Enables the internal CPU to have access to the registers. • 1 - CPU has control of SERDES registers • 0 - External SoC has control of registers This bit should only be changed when the cpu_go bit is clear.
27	AUTONEG_CTL	The autoneg_ctl enables the ability for the SERDES to set the rate, width, align and cmu selection. • 0 rate/width/align/cmu_sel set by overlay controls or pins • 1 rate/width/align/cmu_sel set by 1G/10G autoneg speed detection. Note: The WIZ controls for rate, width, align and pcs must be inactive.
26	DATASPLIT	Enables the ability for the CPU data to be in a separate space from the code. If the datasplit is set, the data address is 65535-dataaddress. This allows program plus data to be 65536 bytes in length but both can start at 0x0000
25 - 23	Reserved	Reserved - writes are ignored, always reads zeros
22 - 0	CPUMEMADDRESS	The current CPU memory address being presented to the memory for read or write. If cpu_go is clear the address is for the CPU pending address for read or write

18.4.5 LANExCTL_STS - Lane x Control and Status

The lane x control and status provides the ability to override SerDes configuration settings. It is mainly provided for test, but sometime used for mission setup as well.

Figure 18-36. Lane x Control and Status Registers (LANExCTL_STS)

31	30	29	28	27	26	25	24
TX0_ENABLE_OVL	TX0_ENABLE_VAL		TX0_RATE_OVL	TX0_RATE_VAL		TX0_IDLE_OVL	TX0_IDLE_VAL
R/W +0	R/W +0		R/W +0	R/W +0		R/W +0	R/W +0
23	22	21	20	19	18	17	16
TX0_WIDTH_OVL	TX0_WIDTH_VAL		LN0_10G_LINKED	LN0_PCS_OVL	LN0_TX_PAUSE	LN0_RX_PAUSE	LN0_SEL_10G
R/W +0	R/W +0		R+0	R/W +0	R/W +0	R/W +0	R/W +0
15	14	13	12	11	10	9	8
RX0_ENABLE_OVL	RX0_ENABLE_VAL		RX0_RATE_OVL	RX0_RATE_VAL		RX0_POLARITY_OVL	RX0_POLARITY_VAL
R/W +0	R/W +0		R/W +0	R/W +0		R/W +0	R/W +0
7	6	5	4	3	2	1	0
RX0_ALIGN_OVL	RX0_ALIGN_VAL	RX0_WIDTH_OVL	RX0_WIDTH_VAL		LN0_1G_LINKED	RX0_OK	RX0_LOSS
R/W +0	R/W +0	R/W +0	R/W +0		R+0	R+0	R+0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18-36. Lane x Control and Status Registers (LANExCTL_STS) Field Descriptions

Bit	Field	Description
31	TX0_ENABLE_OVL	The TX Enable Overlay bit when set allows the TX Enable Value to override the CFGTX.Enable input.
30 - 29	TX0_ENABLE_VAL	The TX Enable Value when used allows the TX lane to be placed in a • 0 = Disable state. • 1 = Sleep state. • 2 = Snooze state. • 3 = Enabled state.
28	TX0_RATE_OVL	The TX Rate Overlay bit when set allows the TX Rate Value to override the CFGTX.Rate input.
27 - 26	TX0_RATE_VAL	The TX Rate Value when used allows the TX lane to be placed into • 0 = Full rate mode. • 1 = Half rate mode. • 2 = Quarter rate mode.
25	TX0_IDLE_OVL	The TX Idle Overlay bit when set allows the TX Idle Value to override the CFGTX.Idle input.
24	TX0_IDLE_VAL	The TX Idle Value when used allows the TX lane to be placed electrical Idle state in non PCIe mode.
23	TX0_WIDTH_OVL	The TX Width Overlay bit when set allows the TX Width Value to override the CFGTX.Width input.
22 - 21	TX0_WIDTH_VAL	The TX Width Value when used allows the TX lane to be placed into • 0 = 10-bit mode • 2 = 20-bit mode • 3 = 16-bit mode.
20	LN0_10G_LINKED	The lnX_10g_linked indicates that the 10G MAC/PCS layer has Linked
19	LN0_PCS_OVL	The PCS Overlay bit when set overrides the PCS control bits from the SerDes to the MAC with values from this register. • 0 = Use SerDes PCS Auto-negotiation values • 1 = Use lnX_sel_10g, lnX_tx_pause, lnX_rx_pause.

Table 18-36. Lane x Control and Status Registers (LANExCTL_STS) Field Descriptions (continued)

Bit	Field	Description
18	LN0_TX_PAUSE	The TX Pause bit will inform the MAC that TX Pause frames are supported. This bit is enabled by setting the lnX_pcs_ovl overlay bit. • 0 = TX Pause frames disabled • 1 = TX Pause frames enabled
17	LN0_RX_PAUSE	The RX Pause bit will inform the MAC that RX Pause frames are supported. This bit is enabled by setting the lnX_pcs_ovl overlay bit. • 0 = RX Pause frames disabled • 1 = RX Pause frames enabled
16	LN0_SEL_10G	The Lane Select 10G selects the CMU1 clock source for the lane. This bit is enabled by setting the lnX_pcs_ovl overlay bit. • 0 = Selects 1GKX, • 1 = Selects 10GKR
15	RX0_ENABLE_OVL	The RX Enable Overlay bit when set allows the RX Enable Value to override the CFGRX.Enable input.
14 - 13	RX0_ENABLE_VAL	The RX Enable Value when used allows the RX lane to be placed in a • 0 = Disable state. • 1 = Sleep state. • 2 = Snooze state. • 3 = Enabled state.
12	RX0_RATE_OVL	The RX Rate Overlay bit when set allows the RX Rate Value to override the CFGRX.Rate input.
11 - 10	RX0_RATE_VAL	The RX Rate Value when used allows the RX lane to be placed into • 0 = Full Rate mode. • 1 = Half Rate mode. • 2 = Quarter Rate mode.
9	RX0_POLARITY_OVL	The RX Polarity Overlay bit when set allows the RX Polarity Value to override the CFGRX.Polarity input.
8	RX0_POLARITY_VAL	The RX Polarity Value when used allows the lane RX Polarity to be inverted.
7	RX0_ALIGN_OVL	The RX Align Overlay bit when set allows the RX Align Value to override the CFGRX.Align input.
6	RX0_ALIGN_VAL	The RX Align Value when used allows the RX lane to align to K28.1, K28.5 and K28.7 characters otherwise known as Comma Characters.
5	RX0_WIDTH_OVL	The RX Width Overlay bit when set allows the RX Width Value to override the CFGRX.Width input.
4 - 3	RX0_WIDTH_VAL	The RX Width Value when used allows the RX lane to be placed into • 0 = 10 bit mode • 2 = 20 bit mode • 3 = 16 bit mode.
2	LN0_1G_LINKED	The lnX_1g_linked indicates that the 1G MAC/PCS layer has linked
1	RX0_OK	The RX OK indicate that the lane is in a functional state.
0	RX0_LOSS	The RX Signal Loss Indicates that the data has not been detected or the CDR is not locked.

18.4.6 PLL_CTRL - PLL Control

The PLL Control register provides the ability to override the PLL state and control events for debug purposes.

Figure 18-37. PLL Control Registers (PLL_CTRL)

31	30 29	28	27	26 25	24	23 10
PLL_ENABLE_OVL	PLL_ENABLE_VAL	PLL_OK	PLL2_ENABLE_OVL	PLL2_ENABLE_VAL	PLL2_OK	Reserved
R/W +0	R/W +00	R +0	R/W +1	R/W +00	R +0	R/W +0

9	8	7 2	1	0
LN1_OK_STATE	LN0_OK_STATE	Reserved	LN1_SD_STATE	LN0_SD_STATE
R +0	R +0	R/W +0	R +0	R +0

Legend: R = Read only; R/W = Read/Write; -n = value after reset

Table 18-37. PLL Control Registers (PLL_CTRL) Field Descriptions

Bit	Field	Description
31	PLL_ENABLE_OVL	The PLL Enable Overlay bit when set allows the PLL Enable Value to override the CFGPLL.Enable input.
30 - 29	PLL_ENABLE_VAL	The PLL Enable Value when used allows the PLL to be placed in a • 0 = Disable state. • 1 = Sleep state. • 2 = Snooze state. • 3 = Enabled state.
28	PLL_OK	The PLL Ok indicate that the transmit clocks are valid and the PLL circuits are ready for use.
27	PLL2_ENABLE_OVL	The PLL2 Enable Overlay bit when set allows the PLL2 Enable Value to override the CFGPLL.Enable input.
26 - 25	PLL2_ENABLE_VAL	The PLL2 Enable Value when used allows the PLL2 to be placed in a • 0 = Disable state. • 1 = Sleep state. • 2 = Snooze state. • 3 = Enabled state.
24	PLL2_OK	The PLL2 Ok indicate that the transmit clocks are valid and the PLL circuits are ready for use.
23 - 10	Reserved	Reserved - writes are ignored, always reads zeros.
9	LN1_OK_STATE	The ln1_ok_state indicate the current state of the lane OK signal for lane 1.
8	LN0_OK_STATE	The ln0_ok_state indicate the current state of the lane OK signal for lane 0.
7 - 2	Reserved	Reserved
1	LN1_SD_STATE	The ln1_sd_state indicate the current state of the signal detect signal for lane 1.
0	LN0_SD_STATE	The ln0_sd_state indicate the current state of the signal detect signal for lane 0.

Optimization and Test Features

Topic **Page**

19.1 PRBS Generator and Checker

19.1.1 Introduction

The default SerDes configurations provided for KeyStone II family are expected to work on user platforms with no changes. However, to fully optimize a link that is established using the SerDes, it is recommended that a user optimize their TX and RX equalization parameters with respect to their board design. Two features that can enable a user to optimize these equalization parameters are the PRBS Generator and PRBS Checker.

The PHY contains a PRBS generator on the TX path that is configurable with multiple PRBS patterns. This can be used for transmitting PRBS patterns into a JBERT tester to measure transmit jitter. It can also be used in loop-back mode with the PRBS checker in order to perform on-chip bit-error rate tests. The PRBS generator and checker are fully configurable using registers and can be configured independently between lanes.

NOTE: Example C APIs supporting SerDes PRBS Generator and Checker features and applications showcasing their use are included in the TI MCSDK package and are filed under '/diag/'

19.1.2 PRBS Generator

Each lane includes an internal PRBS generator. Table 19-1 shows the different PRBS patterns that can be generated in 8/10/16/20 bit modes.

Table 19-1. PRBS Polynomial Patterns That May Be Configured In Generator

PRBS Type	PRBS Polynomial
PRBS-7	X7 + X6 + 1
PRBS-15	X15 + X14 + 1
PRBS-23	X23 + X18 + 1
PRBS-31	X31 + X28 + 1

The BIST generator can be programmed to transmit any of the 4 PRBS polynomial patterns as shown in Table 19-1.

19.1.3 Transmitting a UDP Pattern

The BIST generator may also be programmed to transmit a user defined pattern of 40 bit length. The user defined register is **bist_chk_udp[39:0]** in the lane registers. In 10-bit mode, four 10-bit words are sent. In 8-bit mode, five 8-bit words are sent. K code is assumed to be 0 in 8-bit mode. The words are transmitted in the order listed in Table 19-2 **.**

Table 19-2. 40-Bit Pattern Generator Transmission

10-bit mode	8-bit Mode	20-bit Mode	16-bit Mode
Bits [9:0] (transmitted 1st)	Bits [7:0] (transmitted 1st)	Bits [19:0] (transmitted 1st)	Bits [15:0] (transmitted 1st)
Bits [19:10] (transmitted 2nd)	Bits [15:8] (transmitted 2nd)	Bits [39:20] (transmitted 2nd)	Bits [31:16] (transmitted 2nd)
Bits [29:20] (etc.)	Bits [23:16] (etc.)	Bits [19:0] (etc.)	Bits [15:0] (etc.)
Bits [39:30]	Bits [31:24]	Bits [39:20]	Bits [31:16]

19.1.4 PRBS Checker

Each lane includes a PRBS checker block. This block checks the PRBS pattern transmitted from the PRBS generator matches the correct polynomial. If errors are detected in the polynomial pattern, the error check counter is incremented.

19.1.5 Performing On-Chip Byte-Error Rate (BER) Testing

The on-chip BERT is used to check for byte errors on the incoming received data. This can be used in conjunction with the transmit pattern generator and TX-to-RX on-chip loopback for built-in self-test (BIST) in production testing.

Each lane of the PHY includes a byte-error rate detector that can be used for on-chip BERT testing. The on-chip BERT can verify and measure byte error rate for any recovered patterns generated by the on-chip transmit pattern generator. The BERT can verify user-defined 40-bit transmitted patterns as well as PRBS patterns generated by the transmit pattern generator, or using off-chip pattern generators.

The following is a step-by-step example of a complete PRBS15 BER test without preamble that stresses the entire PHY when its internal main data path is set to 20 bits:

Step 1. Set the PHY to operate in the Normal state, with a data width of 20-bits. At this point, BIST_CHK_ERRORS is static.

Step 2. Set the following registers (Table 19-3) for the transmit pattern generator.

Table 19-3. Registers Involved in Step 2

Register	Location	Value
BIST_GEN_CDN	Lane_034	0x0
BIST_TX_CLOCK_ENABLE	Lane_030	0x1
BIST_RX_CLOCK_ENABLE	Lane_030	0x1
BIST_CHK_DATA_MODE	Lane_030	0x1
BIST_GEN_MODE8B	Lane_030	0x0
BIST_GEN_WORD	Lane_034	0x1
BIST_GEN_EN	Lane_034	0x0
BIST_GEN_SEND_PREAM	Lane_034	0x0
BIST_CHK_LFSR_LENGTH	Lane_030	0x1
BIST_GEN_INV_PRBS	Comlane_014	0x0
BIST_CHK_INV_PRBS	Comlane_014	0x0
BIST_CHK_PREAM0	Lane_030, Lane_034	0x283
BIST_CHK_PREAM1	Lane_034	0x17C
BIST_CHK_UDP	Lane_03C	0x0
BIST_GEN_EN_LOW	Lane_040	0x0
BIST_GEN_EN_HIGH	Lane_044	0x0
BIST_CHK_INSERT_WORD	Lane_03C, Lane_040	0x0
BIST_CHK_INSERT_LENGTH	Lane_034	0x0
BIST_GEN_INSERT_COUNT	Lane_034	0x0
BIST_GEN_INSERT_DELAY	Lane_044	0x0

Step 3. Wait a minimum of 20 ns, then deassert BIST_GEN_CDN.

Step 4. Connect the TX pins to the RX pins through a length of cable.

Step 5. Set the following for each lane (Table 19-4).

Table 19-4. Registers Involved in Step 5

Register	Location	Value
DMUX_TXA_SEL	Lane_000	0x2
DMUX_TXB_SEL	Lane_000	0x0

Step 6. Wait a minimum of 20 ns, then assert BIST_GEN_EN.

Step 7. Wait a minimum of 2 μs for the analog transmit and receive paths to obtain bit lock on to the training pattern. While this is occurring, set:

Table 19-5. Registers Involved in Step 7

Register	Location	Value
BCHK_EN	Lane_004	0x0
BCHK_CLR	Lane_004	0x1
BCHK_SRC	Lane_004	0x2

Step 8. After 20 ns, deassert BCHK_CLR. This will clear the error checker counters.

Step 9. Assert BCHK_EN to enable the receive BER test.

Step 10. The PHY will indicate that it has successfully detected the PRBS data when BIST_CHK_SYNCH is asserted. To check if BIST_CHK_SYNCH is asserted perform the following steps

For PHY-A

- Write (lane_num+1) << 5)+0xC)to TBUS_ADDR_OVR_O[7:0] (CMU_008)
- Wait for TBUS_DATA_SMPL[10] to be set (CMU_0ec and CMU_0fc) and then exit to next step
  For PHY-B
- Write (lane_num+1) << 8)+0x0C) to TBUS_ADDR_OVR_O[10:0] (CMU_0fc)
- Wait for TBUS_DATA_SMPL[10] to be set (CMU_0f8) and then exit to next step
  lane_num = 0, 1, 2, 3 depending on the lane being setup for BERT

Step 11. Wait the desired test length. The longer the test time, the more bits are able to be tested and that corresponds with a higher measured bit error rate.
Table 19-6 shows relation between test time and corresponding BER measured.

Table 19-6. Relation Between Test Time and BER

Corresponding Bit Error Rate	Elapsed Test Time
10^{-3}	320 ns
10^{-6}	320 µs – Recommended
10^{-7}	3.2 ms
10^{-9}	0.32 s
10^{-10}	3.2 s
10^{-11}	32 s
10^{-12}	320 s

Step 12. Once the desired test time has elapsed, deassert BCHK_EN first, then BIST_GEN_EN.

Step 13. Within 50 ns, the PHY will indicate a successful exit from the BIST by de-asserting BIST_CHK_SYNCH. To check if BIST_CHK_SYNCH is de-asserted perform the following steps

For PHY-A

- Write (lane_num+1) << 5)+0xC)to TBUS_ADDR_OVR_O[7:0] (CMU_008)
- Wait for TBUS_DATA_SMPL[10] to be clear (CMU_0ec and CMU_0fc) and then exit to next step
  For PHY-B
- Write (lane_num+1) << 8)+0x0C) to TBUS_ADDR_OVR_O[10:0] (CMU_0fc)
- Wait for TBUS_DATA_SMPL[10] to be clear (CMU_0f8) and then exit to next step
  lane_num = 0, 1, 2, 3 depending on the lane being setup for BERT

Step 14. At this point, BIST_CHK_ERRORS is static.

Step 15. Verify BIST_CHK_ERRORS is 0. This verifies that no bit errors were measured during the testing sequence.

Step 16. To return to normal, set (Table 19-7):

Table 19-7. Registers Involved in Step 15

Register	Location	Value
DMUX_TXA_SEL	Lane_000	0x0
DMUX_TXB_SEL	Lane_000	0x0

After 100 ns, the PHY should be back in normal mode.

19.2 Loopbacks

The loopback features present in the PHYs are shown in Figure 19-1.

Figure 19-1. Internal Loopback Modes

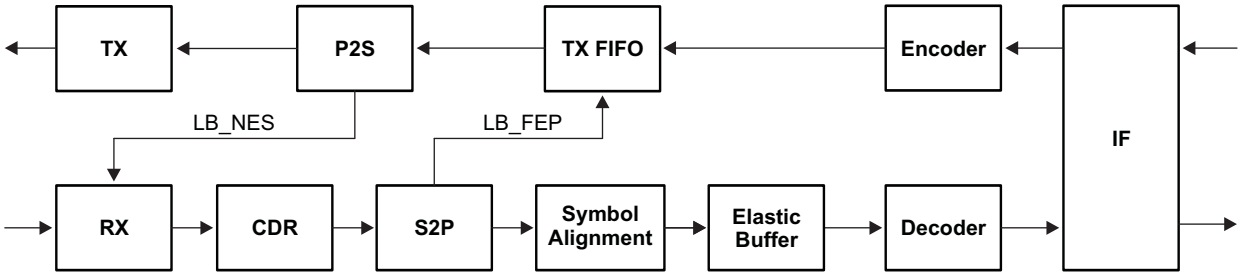


Table 19-8 shows a description of loopback mode and how to program each mode using registers.

Table 19-8. Description of Each Loopback Mode

Loopback Timing Requirements	Loopback Name	Loopback Description	Enabling Register(s) (per lane)	Notes / Constraints
async	**LB_NES**	Near-End Serial loopback: digital, serial, un-timed loopback from Serializer (P2S) output to receive phase detector.	NES_LB_ENA_O = 0x1 in Lane_000	Is restricted to < 5 Gbps data rate.
async – requires reset	**LB_FEP**	Far-End loopback: Digital, parallel loopback from Deserializer (S2P) to Serializer (P2S).	DMUX_TXB_SEL_O = 5 DMUX_TXA_SEL_O = 0 CKTRANS_EN_O = 1 RX_CLK_SRC_O = 1 TX_CLK_SRC_O = 0 SOC_CK_EN_O = 0 RXCLK_LB_ENA_O = 1	See steps below for using this loopback mode. Synchronized internally to the PHY.

When attempting to use the PMA layer parallel loopback, LB_FEP, follow these steps:

Step 1. Ensure the PHY is successfully placed into power state Normal. Valid data must be transmitted into the lnX_rx_p / lnX_rx_m pins.

Step 2. Set RXCLK_LB_ENA = 0x1 to drive the transmit path with the recovered, receive bit clock. This is required to synchronize transmit and receive paths for PMA layer parallel loopback testing.

Step 3. Wait 2 μs to allow the CDR to fully lock on to the incoming data.

Step 4. Enable the PMA layer parallel loopback by setting dmux_txb_sel = 0x0 and cktrans_en = 0x1.

Step 5. Run the desired parallel loopback test.

Step 6. Disable the loopback test by setting DMUX_TX_BSEL = 0x0, CKTRANS_EN = 0x0 and RXCLK_LB_ENA = 0x0.

Step 7. Wait 100 ns for settling.

Step 8. The PHY should now be successfully transitioned back into the Normal state.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2013) to A Revision **Page**

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265