TMS320VC5505 DSP System

User's Guide

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About This Manual

This document describes the operation of the external memory interface (EMIF) in the TMS320VC5505/5504 Digital Signal Processor (DSP). The purpose of the EMIF is to provide a means to connect to a variety of external asynchronous devices including NOR Flash, NAND Flash, and SRAM.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320C5515/14/05/04 Digital Signal Processor (DSP) Digital Signal Processor (DSP). Copies of these documents are available on the internet at http://www.ti.com.

SWPU073 — **TMS320C55x 3.0 CPU Reference Guide.** This manual describes the architecture, registers, and operation of the fixed-point TMS320C55x digital signal processor (DSP) CPU.

SPRU652 — **TMS320C55x DSP CPU Programmer's Reference Supplement.** This document describes functional exceptions to the CPU behavior.

SPRUFO0 — **TMS320VC5505/5504 Digital Signal Processor (DSP) Universal Serial Bus 2.0 (USB) User's Guide.** This document describes the universal serial bus 2.0 (USB) in the TMS320VC5505/5504 Digital Signal Processor (DSP) devices. The USB controller supports data throughput rates up to 480 Mbps. It provides a mechanism for data transfer between USB devices.

SPRUFO1A — **TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Inter-Integrated Circuit (I2C) Peripheral User's Guide.** This document describes the inter-integrated circuit (I2C) peripheral in the TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) devices. The I2C peripheral provides an interface between the device and other devices compliant with Phillips Semiconductors Inter-IC bus (I2C-bus) specification version 2.1 and connected by way of an I2C-bus. This document assumes the reader is familiar with the I2C-bus specification.

SPRUFO2 — **TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Timer/Watchdog Timer User's Guide.** This document provides an overview of the three 32-bit timers in the TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) devices. The 32-bit timers of the device are software programmable timers that can be configured as general-purpose (GP) timers. Timer 2 can be configured as a GP, a Watchdog (WD), or both simultaneously.

SPRUFO3 — **TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Serial Peripheral Interface (SPI) User's Guide.** This document describes the serial peripheral interface (SPI) in the TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) devices. The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 32 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI supports multi-chip operation of up to four SPI slave devices. The SPI can operate as a master device only.

SPRUFO4 — **TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) General-Purpose Input/Output (GPIO) User's Guide.** This document describes the general-purpose input/output (GPIO) on the TMS320C5515/14/05/04/VC05/VC04 digital signal processor (DSP) devices. The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an input, you can detect the state of an internal register. When configured as an output you can write to an internal register to control the state driven on the output pin.

SPRUFO5 — **TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Universal Asynchronous Receiver/Transmitter (UART) User's Guide.** This document describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) devices. The UART performs serial-to-parallel conversions on data received from a peripheral device and parallel-to-serial conversion on data received from the CPU.

SPRUFO6 — **TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Multimedia Card (MMC)/Secure Digital (SD) Card Controller User's Guide.** This document describes the Multimedia Card (MMC)/Secure Digital (SD) Card Controller on the TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) devices. The multimedia card (MMC)/secure digital (SD) card is used in a number of applications to provide removable data storage. The MMC/SD card controller provides an interface to external MMC and SD cards.

SPRUF07 — **TMS320VC5505/5504 Digital Signal Processor (DSP) Real-Time Clock (RTC) User's Guide.** This document describes the operation of the Real-Time Clock (RTC) module in the TMS320VC5505/5504 Digital Signal Processor (DSP) devices. The RTC also has the capability to wake-up the power management and apply power to the rest of the device through an alarm, periodic interrupt, or external WAKEUP signal.

SPRUFO8A — **TMS320VC5505/5504 Digital Signal Processor (DSP) External Memory Interface (EMIF) User's Guide.** This document describes the operation of the external memory interface (EMIF) in the TMS320VC5505/5504 Digital Signal Processor (DSP) devices. The purpose of the EMIF is to provide a means to connect to a variety of external devices.

SPRUFO9 — **TMS320VC5505/5504 Digital Signal Processor (DSP) Direct Memory Access (DMA) Controller User's Guide.** This document describes the features and operation of the DMA controller that is available on the TMS320VC5505/5504 Digital Signal Processor (DSP) devices. The DMA controller is used to move data among internal memory, external memory, and peripherals without intervention from the CPU and in the background of CPU operation.

SPRUFP0 — **TMS320VC5505 Digital Signal Processor (DSP) System User's Guide.** This document describes various aspects of the TMS320VC5505/5504 digital signal processor (DSP) including: system memory, device clocking options and operation of the DSP clock generator, power management features, interrupts, and system control.

SPRUGL6 — **TMS320VC5504 Digital Signal Processor (DSP) System User's Guide.** This document describes various aspects of the TMS320VC5505/5504 digital signal processor (DSP) including: system memory, device clocking options and operation of the DSP clock generator, power management features, interrupts, and system control.

SPRUFP1 — TMS320C5515/05/VC05 Digital Signal Processor (DSP) Successive Approximation (SAR) Analog to Digital Converter (ADC) User's Guide. This document provides an overview of the Successive Approximation (SAR) Analog to Digital Converter (ADC) on the TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) devices. The SAR is a 10-bit ADC using a switched capacitor architecture which converts an analog input signal to a digital value.

SPRUFP3 — TMS320C5515/05/VC05 Digital Signal Processor (DSP) Liquid Crystal Display Controller (LCDC) User's Guide. This document describes the liquid crystal display controller (LCDC) in the TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) devices. The LCD controller includes a LCD Interface Display Driver (LIDD) controller.

SPRUFP4 — TMS320VC5505/5504 Digital Signal Processor (DSP) Inter-IC Sound (I2S) Bus User's Guide. This document describes the features and operation of Inter-IC Sound (I2S) Bus in the TMS320VC5505/5504 Digital Signal Processor (DSP) devices. This peripheral allows serial transfer of full duplex streaming data, usually streaming audio, between DSP and an external I2S peripheral device such as an audio codec.

System Control

1.1 Introduction

The TMS320VC5505 digital signal processor (DSP) contains a high-performance, low-power DSP to efficiently handle tasks required by portable audio, wireless audio devices, industrial controls, software defined radio, fingerprint biometrics, and medical applications. The C5505 DSP consists of the following primary components:

- A C55x CPU and associated memory
- FFT hardware accelerator
- Four DMA controllers and external memory interface
- Power management module
- A set of I/O peripherals that includes I2S, I2C, SPI, UART, Timers, EMIF, 10-bit SAR ADC, LCD Controller, USB 2.0

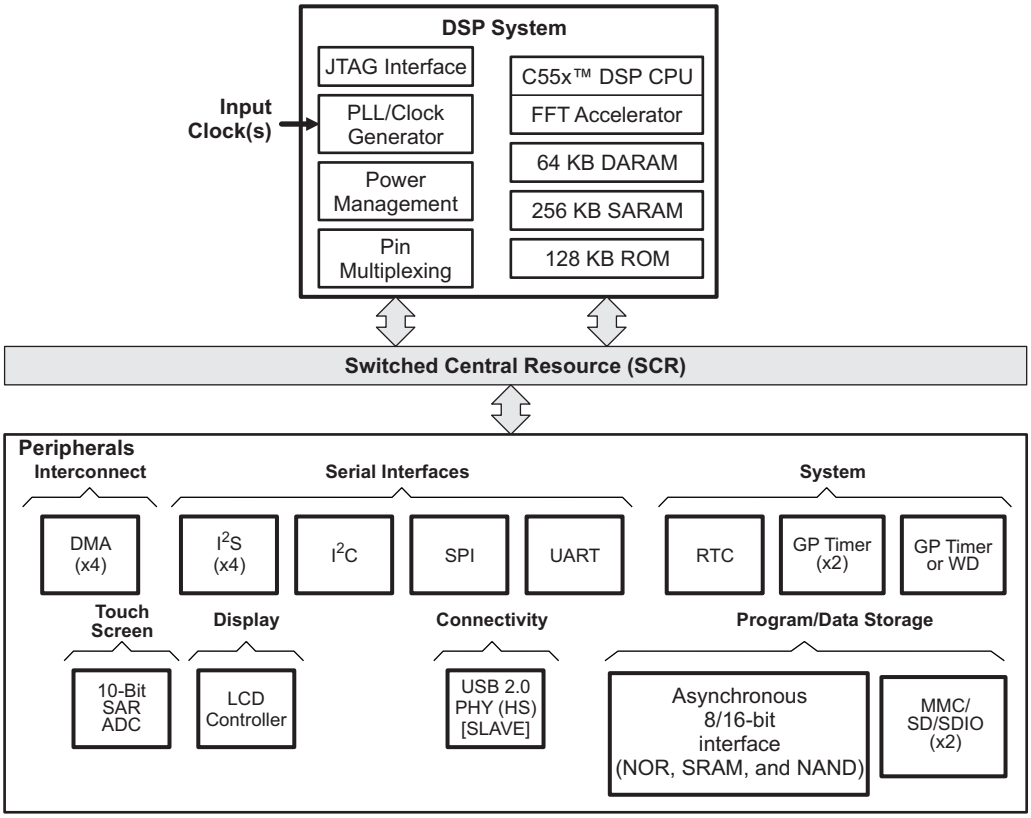
For more information on these components see the following documents:

- *TMS320C55x 3.0 CPU Reference Guide* (SWPU073).
- *TMS320C55x DSP Peripherals Overview Reference Guide* (SPRU317).

1.1.1 Block Diagram

The C5505 DSP block diagram is shown in Figure 1-1 .

Figure 1-1. Functional Block Diagram



1.1.2 CPU Core

The device CPU is responsible for performing the digital signal processing tasks required by the application. In addition, the CPU acts as the overall system controller, responsible for handling many system functions such as system-level initialization, configuration, user interface, user command execution, connectivity functions, and overall system control.

Tightly coupled to the CPU are the following components:

- DSP internal memories
  - Dual-access RAM (DARAM)
  - Single-access RAM (SARAM)
  - Read-only memory (ROM)
- FFT hardware accelerator
- Ports and buses

The CPU also manages/controls all peripherals on the device. For the full list of peripherals, see the device-specific data manual.

Figure 1-1 shows the functional block diagram of the DSP and how it connects to the rest of the device. The DSP architecture uses the switched central resource (SCR) to transfer data within the system.

1.1.3 Power FFT Hardware Accelerator

The device CPU includes a tightly-coupled FFT hardware accelerator that communicates with the device CPU through the use of C-callable ROM routines. The main features of the FFT hardware accelerator are:

- Support for 8 to 1024-point (in powers of 2) real and complex-valued FFTs and IFFTs.
- An internal twiddle factor generator for optimal use of memory bandwidth and more efficient programming.
- Basic and software-driven auto-scaling feature provides good precision vs cycle count trade-off.
- Single-stage and double-stage modes enabling computation of one or two stages in one pass, thus handling odd power of two FFT widths.

1.1.3.1 Using FFT Accelerator ROM Routines

The C5505 includes C-callable routines in ROM to execute FFT and IFFT using the tightly coupled FFT accelerator. The routines reside in the following address:

Table 1-1.

Address	Name	Description	Calling Convention
0x00ff80c2	hwafft 1024pts	1024-pt FFT/IFFT	Uint16 hwafft_1024pts(Int32 *data,Int32 *scratch, Uint16 fft_flag, Uint16 scale_flag);
0x00ff7a39	hwafft 128pts	128-pt FFT/IFFT	Uint16 hwafft_128pts(Int32 *data,Int32 *scratch, Uint16 fft_flag, Uint16 scale_flag);
0x00ff7445	hwafft 16pts	16-pt FFT/IFFT	Uint16 hwafft_16pts(Int32 *data,Int32 *scratch, Uint16 fft_flag, Uint16 scale_flag);
0x00ff7c4a	hwafft 256pts	256-pt FFT/IFFT	Uint16 hwafft_256pts(Int32 *data,Int32 *scratch, Uint16 fft_flag, Uint16 scale_flag);
0x00ff759b	hwafft 32pts	32-pt FFT/IFFT	Uint16 hwafft_32pts(Int32 *data,Int32 *scratch, Uint16 fft_flag, Uint16 scale_flag);
0x00ff7e48	hwafft 512pts	512-pt FFT/iFFT	Uint16 hwafft_512pts(Int32 *data,Int32 *scratch, Uint16 fft_flag, Uint16 scale_flag);
0x00ff78a4	hwafft 64pts	64-pt FFT/iFFT	Uint16 hwafft_64pts(Int32 *data,Int32 *scratch, Uint16 fft_flag, Uint16 scale_flag);
0x00ff7356	hwafft 8pts	8-pt FFT/IFFT	Uint16 hwafft_8pts(Int32 *data,Int32 *scratch, Uint16 fft_flag, Uint16 scale_flag);
0x00ff7342	hwafft br	Bit reverse input data	void hwafft_br(Int32 *data, Int32 *data_br, Uint16 data_len);

Note that for the FFT routines, output data is dependent on the return value (T0). If return = 0 output data is in-placed, meaning the result will overwrite the input buffer. If return =1, output data is placed in the scratch buffer. The 32-bit input and output data consist of 16-bit real and 16-bit imaginary data. If only real data is used, the imaginary part can be zeroed. Scale flag determines if the butterfly output is divided by 2 to prevent overflow at the expense of resolution.

1.1.4 Power Management

Integrated into the C5505 DSP are the following power management features:

- One low dropout (LDO) regulator for analog portions of the device.
- Idle controller with several clock domains:
  - CPU domain
  - Clock generator domain.
  - Peripheral domain.
  - USB domain.
  - Real-time clock (RTC) domain.
- Independent voltage and power domains.

1.1.5 DSP Peripherals

The DSP includes the following peripherals:

- Four direct memory access (DMA) controllers, each with four independent channels.
- One 21-bit address, 16-bit data asynchronous external memory interface with support for mobile SDRAM, single-level cell (SCL) NAND with 1-bit ECC, and multi-level cell (MLC) NAND with 4-bit ECC.
- Two serial busses each configurable to support one Multimedia Card (MMC) / Secure Digital (SD/SDIO) controller, one inter-IC sound bus (I2S) interface with GPIO, or a full GPIO interface.
- One parallel bus configurable to support a 16-bit LCD bridge or a combination of an 8-bit LCD bridge, a serial peripheral interface (SPI), an I2S, a universal asynchronous receiver/transmitter (UART), and GPIO.
- One inter-integrated circuit (I2C) multi-master and slave interface with 7-bit and 10-bit addressing modes.
- Three 32-bit timers with 16-bit prescaler; one timer supports watchdog functionality.
- A USB 2.0 slave.
- A 10-bit successive approximation (SAR) analog-to-digital converter with touchscreen conversion capability.
- One real-time clock (RTC) with separated power supply and isolation logic.

1.2 System Memory

The DSP supports a unified memory map (program and data accesses are made to the same physical space) composed of both on-chip and external memory. The total on-chip memory is 448 K-bytes (160 K-byte 16-bit words of RAM and 64K-byte 16-bit words of ROM).

The external memory interface (EMIF) port provides the means for the DSP to access external memory and devices including: mobile single data rate (SDR) SDRAM, NOR Flash, NAND Flash and SRAM. The EMIF port can address up to 8M-bytes of mobile SDRAM and up to 4M-bytes of asynchronous memory, including flash.

Separate from the program and data space, the DSP also includes a 64K-byte I/O space for the registers of the DSP peripherals.

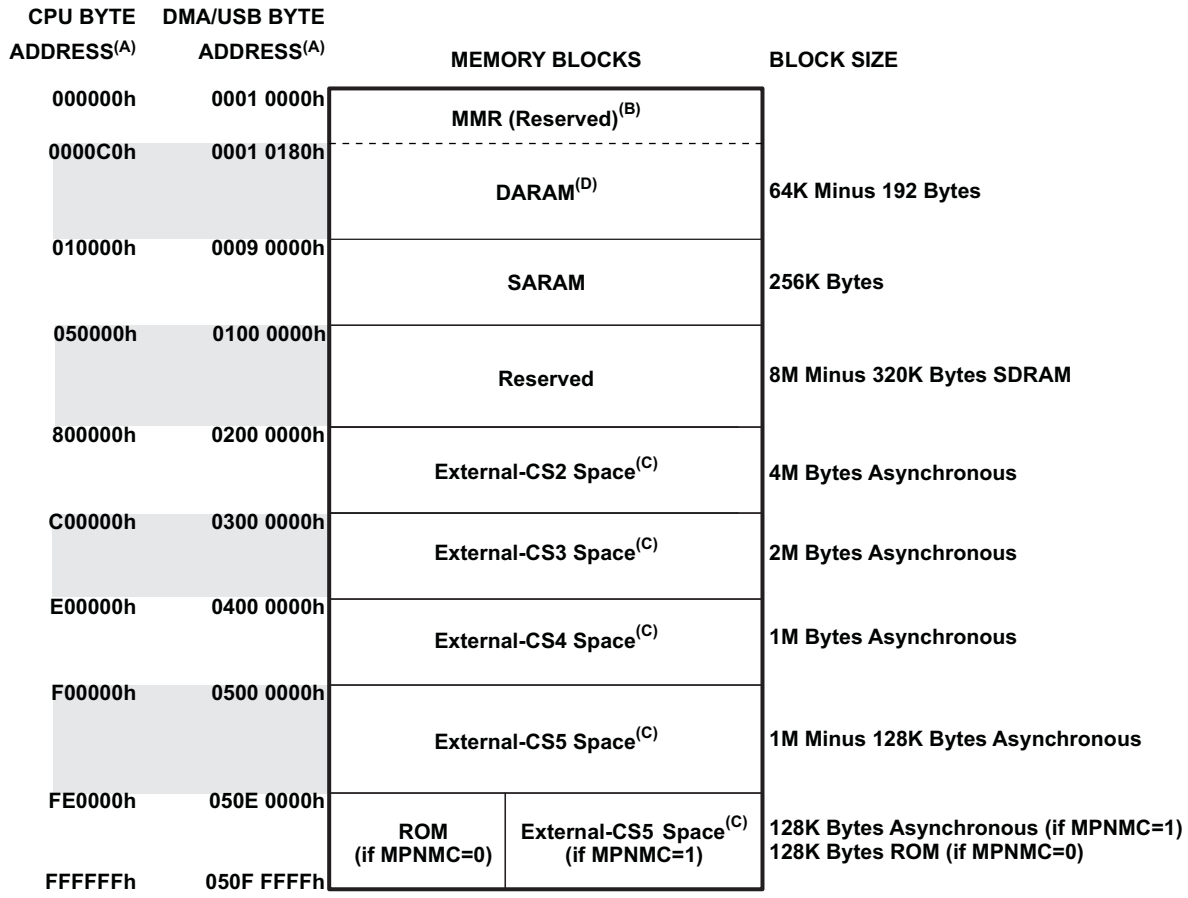
1.2.1 Program/Data Memory Map

The device provides 16MB of total address space composed of on-chip RAM, on-chip ROM, and external memory space supporting a variety of memory types. The on-chip, dual-access RAM allows two accesses to a given block during the same cycle. The device has 8 blocks of 8K-bytes of dual-access RAM. The on-chip, single-access RAM allows one access to a given block per cycle. The device has 32 blocks of 8K-bytes of single-access RAM.

The remainder of the memory map is external space that is divided into five spaces. Each space has a chip select decode signal (called CS) that indicates an access to the selected space. The external memory interface (EMIF) supports access to asynchronous memories such as SRAM Flash, and mobile single data rate (SDR) SDRAM.

The DSP memory is accessible by different master modules within the DSP, including the device CPU, the four DMA controllers, and the USB. The DSP memory map as seen by these modules is illustrated in Figure 1-2 .

Figure 1-2. DSP Memory Map



A Address shown represents the first byte address in each block.

B The first 192 bytes are reserved for memory-mapped registers (MMRs).

C Out of the four DMA controllers, *only* DMA controller 3 has access to the external memory space.

D The USB controller does not have access to DARAM.

1.2.1.1 On-Chip Dual-Access RAM (DARAM)

The DARAM is located in the byte address range 00 0000h - 00 FFFFh and is composed of eight blocks of 4K words each (see Table 1-2). Each DARAM block can perform two accesses per cycle (two reads, two writes, or a read and a write). DARAM can be accessed by the internal program, data, or DMA buses

Table 1-2. DARAM Blocks

Memory Block	CPU Byte Address Range	DMA/USB Controller Byte Address Range
DARAM 0(1)	00 0000h - 00 1FFFh	0001 0000h - 0001 1FFFh
DARAM 1	00 2000h - 00 3FFFh	0001 2000h - 0001 3FFFh
DARAM 2	00 4000h - 00 5FFFh	0001 4000h - 0001 5FFFh
DARAM 3	00 6000h - 00 7FFFh	0001 6000h - 0001 7FFFh
DARAM 4	00 8000h - 00 9FFFh	0001 8000h - 0001 9FFFh
DARAM 5	00 A000h - 00 BFFFh	0001 A000h - 0001 BFFFh
DARAM 6	00 C000h - 00 DFFFh	0001 C000h - 0001 DFFFh

(1) First 192 bytes are reserved for memory-mapped registers (MMRs).

Table 1-2. DARAM Blocks (continued)

Memory Block	CPU Byte Address Range	DMA/USB Controller Byte Address Range
DARAM 7	00 E000h - 00 FFFFh	0001 E000h - 0001 FFFFh

1.2.1.2 On-Chip Single-Access RAM (SARAM)

The SARAM is located at the byte address range 01 0000h - 04 FFFFh and is composed of 32 blocks of 4K words each (see Table 1-3). Each SARAM block can perform one access per cycle (one read or one write). SARAM can be accessed by the internal program, data, or DMA buses.

Table 1-3. SARAM Blocks

Memory Block	CPU Byte Address Range	DMA/USB Controller Byte Address Range
SARAM 0	01 0000h - 01 1FFFh	0009 0000h - 0009 1FFFh
SARAM 1	01 2000h - 01 3FFFh	0009 2000h - 0009 3FFFh
SARAM 2	01 4000h - 01 5FFFh	0009 4000h - 0009 5FFFh
SARAM 3	01 6000h - 01 7FFFh	0009 6000h - 0009 7FFFh
SARAM 4	01 8000h - 01 9FFFh	0009 8000h - 0009 9FFFh
SARAM 5	01 A000h - 01 BFFFh	0009 A000h - 0009 BFFFh
SARAM 6	01C000h - 01 DFFFh	0009 C000h - 0009 DFFFh
SARAM 7	01 E000h - 01 FFFFh	0009 E000h - 0009 FFFFh
SARAM 8	02 0000h - 02 1FFFh	000A 0000h - 000A 1FFFh
SARAM 9	02 2000h - 02 3FFFh	000A 2000h - 000A 3FFFh
SARAM 10	02 4000h - 02 5FFFh	000A 4000h - 000A 5FFFh
SARAM 11	02 6000h - 02 7FFFh	000A 6000h - 000A 7FFFh
SARAM 12	02 8000h - 02 9FFFh	000A 8000h - 000A 9FFFh
SARAM 13	02 A000h - 02 BFFFh	000A A000h - 000A BFFFh
SARAM 14	02 C000h - 02 DFFFh	000A C000h - 000A DFFFh
SARAM 15	02 E000h - 02 FFFFh	000A E000h - 000A FFFFh
SARAM 16	03 0000h - 03 1FFFh	000B 0000h - 000B 1FFFh
SARAM 17	03 2000h - 03 3FFFh	000B 2000h - 000B 3FFFh
SARAM 18	03 4000h - 03 5FFFh	000B 4000h - 000B 5FFFh
SARAM 19	03 6000h - 03 7FFFh	000B 6000h - 000B 7FFFh
SARAM 20	03 8000h - 03 9FFFh	000B 8000h - 000B 9FFFh
SARAM 21	03 A000h - 03 BFFFh	000B A000h - 000B BFFFh
SARAM 22	03 C000h - 03 DFFFh	000B C000h - 000B DFFFh
SARAM 23	03 E000h - 03 FFFFh	000B E000h - 000B FFFFh
SARAM 24	04 0000h - 04 1FFFh	000C 0000h - 000C 1FFFh
SARAM 25	04 2000h - 04 3FFFh	000C 2000h - 000C 3FFFh
SARAM 26	04 4000h - 04 5FFFh	000C 4000h - 000C 5FFFh
SARAM 27	04 6000h - 04 7FFFh	000C 6000h - 000C 7FFFh
SARAM 28	04 8000h - 04 9FFFh	000C 8000h - 000C 9FFFh
SARAM 29	04 A000h - 04 BFFFh	000C A000h - 000C BFFFh
SARAM 30	04 C000h - 04 DFFFh	000C C000h - 000C DFFFh
SARAM 31	04 E000h - 04 FFFFh	000C E000h - 000C FFFFh

1.2.1.3 On-Chip Read-Only Memory (ROM)

The zero-wait-state ROM is located at the byte address range FE 0000h - FF FFFFh. The ROM is composed of four 16K-word blocks, for a total of 128K-bytes of ROM. Each ROM block can perform one access per cycle (one read or one write). ROM can be accessed by the internal program or data buses. The ROM address space can be mapped by software to the external memory or to the internal ROM via the MPNMC bit in the ST3 status register.

The standard device includes a Bootloader program resident in the ROM. When the MPNMC bit field of the ST3 status register is set through software, the on-chip ROM is disabled and not present in the memory map, and byte address range FE 0000h - FF FFFFh is directed to external memory space. A hardware reset always clears the MPNMC bit, so it is not possible to disable the ROM at reset. However, the software reset instruction does not affect the MPNMC bit. The ROM can be accessed by the program and data buses. The on-chip ROM is a one cycle per word access memory.

1.2.1.4 External Memory

The external memory space of the device is located at the byte address range 05 0000h - FF FFFFh. The external memory space is divided into five chip select spaces: one is reserved, and the remainder (EMIF CS2-5) dedicated to asynchronous devices including flash. Each chip select space has a corresponding chip select pin (called $\overline{\text{EMIF\_CSn}}$) that is activated during an access to the chip select space.

The external memory interface (EMIF) provides the means for the DSP to access external memories and other devices including: NOR Flash, NAND Flash and SRAM. Before accessing external memory, you must configure the EMIF through its registers. For more detail on the EMIF, see the *TMS320VC5505/5504 DSP External Memory Interface (EMIF) User's Guide* (SPRUFO8).

As described in Section 1.2.1.3, when the MPNMC bit field of the ST3 status register is cleared (default), the byte address range FE 0000h - FF FFFFh is reserved for the on-chip ROM.

The EMIF provides a configurable 16- or 8-bit data bus, an address bus width of up to 21-bits, and four dedicated chip selects, along with memory control signals. To maximize power savings, the I/O pin of the EMIF can be operated at low voltages independently of other I/O pins on the DSP.

1.2.1.4.1 Asynchronous EMIF Interface

The EMIF provides a configurable 16- or 8-bit data bus, an address bus width of up to 21-bits, and 4 dedicated chip selects, along with memory control signals. The cycle timings of the asynchronous interface are fully programmable, allowing for access to a wide range of devices including NAND flash, NOR flash, and SRAM as well as other asynchronous devices such as a TI DSP HPI interface. In NAND mode, the asynchronous interface supports 1-bit ECC for 8- and 16-bit NAND flash and 4-bit ECC for 8-bit NAND flash.

1.2.2 I/O Memory Map

The DSP includes a 64K-byte I/O space for the registers of the DSP peripherals and system registers used for idle control, status monitoring and system configuration.

Table 1-4 through Table 1-29 list registers of the device. Not all addresses in the 64K-word I/O space are used; these addresses should be treated as reserved.

Some DMA controllers have access to some of the peripherals registers, namely the I2C, UART, I2S, and SAR. The register tables for these peripherals include a CPU I/O word address as well as a DMA address.

NOTE: The CPU access latency to the peripheral registers is 2 CPU cycles. Following peripheral register update(s), the CPU must wait at least 2 CPU cycles before attempting to use that peripheral. When more than one peripheral register is updated in a sequence, the CPU only needs to wait following the final register write. For example, if the EMIF is being reconfigured, the CPU must wait until the very last EMIF register update takes effect before trying to access the external memory. The users should consult the respective peripheral user's guide to determine if a peripheral requires additional time to initialize itself to the new configuration after the register updates take effect.

Before accessing any peripheral register, make sure the peripheral being accessed is out of reset and its internal clock is enabled. The peripheral reset control register (Section 1.7.5.2) and the peripheral clock gating control registers (Section 1.5.5.2.1) control these functions.

Table 1-4. Idle Control, Status, and System Registers

CPU Word Address	Acronym	Register Description	Section
0001h	ICR	Idle Control Register	Section 1.5.5.1.1
0002h	ISTR	Idle Status Register	Section 1.5.5.1.1
1C00h	EBSR	External Bus Selection Register	Section 1.7.3.1.3
1C02h	PCGCR1	Peripheral Clock Gating Control Register 1	Section 1.5.5.2.1
1C03h	PCGCR2	Peripheral Clock Gating Control Register 2	Section 1.5.5.2.1
1C04h	PSRCR	Peripheral Software Reset Counter Register	Section 1.7.5.1
1C05h	PRCR	Peripheral Reset Control Register	Section 1.7.5.2
1C14h	TIAFR	Timer Interrupt Aggregation Flag Register	Section 1.6.3
1C16h	ODSCR	Output Drive Strength Control Register	Section 1.7.3.2
1C17h	PDINHIBR1	Pull-Down Inhibit Register 1	Section 1.7.3.3
1C18h	PDINHIBR2	Pull-Down Inhibit Register 2	Section 1.7.3.3
1C19h	PDINHIBR3	Pull-Down Inhibit Register 3	Section 1.7.3.3
1C1Ah	DMA0CESR1	DMA0 Channel Event Source Register 1	Section 1.7.4.2.2
1C1Bh	DMA0CESR2	DMA0 Channel Event Source Register 2	Section 1.7.4.2.2
1C1Ch	DMA1CESR1	DMA1 Channel Event Source Register 1	Section 1.7.4.2.2
1C1Dh	DMA1CESR2	DMA1 Channel Event Source Register 2	Section 1.7.4.2.2
1C26h	ECDR	EMIF Clock Divider Register	Section 1.7.7
1C28h	RAMSLPMDCNTLR1	RAM Sleep Mode Control Register 1	Section 1.5.6.3.1
1C30h	DMAIFR	DMA Interrupt Flag Register	Section 1.7.4.2.1
1C31h	DMAIER	DMA Interrupt Enable Register	Section 1.7.4.2.1
1C32h	USBSCR	USB System Control Register	Section 1.5.5.4.2
1C33h	ESCR	EMIF System Control Register	Section 1.7.6.1
1C36h	DMA2CESR1	DMA2 Channel Event Source Register 1	Section 1.7.4.2.2
1C37h	DMA2CESR2	DMA2 Channel Event Source Register 2	Section 1.7.4.2.2
1C38h	DMA3CESR1	DMA3 Channel Event Source Register 1	Section 1.7.4.2.2
1C39h	DMA3CESR2	DMA3 Channel Event Source Register 2	Section 1.7.4.2.2
1C3Ah	CLKSTOP	Peripheral Clock Stop Request/Acknowledge Register	Section 1.5.5.2.2

Table 1-5. Clock Generator Registers

CPU Word Address	Acronym	Register Description	Section
1C20h	CGCR1	Clock Generator Control Register 1	Section 1.4.4.1
1C21h	CGCR2	Clock Generator Control Register 2	Section 1.4.4.2
1C22h	CGCR3	Clock Generator Control Register 3	Section 1.4.4.3
1C23h	CGCR4	Clock Generator Control Register 4	Section 1.4.4.4
1C24h	CCSSR	CLKOUT Control Source Select Register	Section 1.4.4.5
1C1Eh	CCR1	Clock Configuration Register 1	Section 1.4.4.6
1C1Fh	CCR2	Clock Configuration Register 2	Section 1.4.4.7

Table 1-6. Die ID Registers

CPU Word Address	Acronym	Register Description	Section
1C40h	DIEIDR0	Die ID Register 0	Section 1.7.2.1

Table 1-6. Die ID Registers (continued)

CPU Word Address	Acronym	Register Description	Section
1C41h	DIEIDR1	Die ID Register 1	Section 1.7.2.2
1C42h	DIEIDR2	Die ID Register 2	Section 1.7.2.3
1C43h	DIEIDR3	Die ID Register 3	Section 1.7.2.4
1C44h	DIEIDR4	Die ID Register 4	Section 1.7.2.5
1C45h	DIEIDR5	Die ID Register 5	Section 1.7.2.6
1C46h	DIEIDR6	Die ID Register 6	Section 1.7.2.7
1C47h	DIEIDR7	Die ID Register 7	Section 1.7.2.8

Table 1-7. GPIO Registers[(1)]

CPU Word Address	Acronym	Register Description
1C06h	IODIR1	GPIO Direction Register 1
1C07h	IODIR2	GPIO Direction Register 2
1C08h	IOINDATA1	GPIO Data In Register 1
1C09h	IOINDATA2	GPIO Data In Register 2
1C0Ah	IODATAOUT1	GPIO Data Out Register 1
1C0Bh	IODATAOUT2	GPIO Data Out Register 2
1C0Ch	IOINTEDG1	GPIO Interrupt Edge Trigger Enable Register 1
1C0Dh	IOINTEDG2	GPIO Interrupt Edge Trigger Enable Register 2
1C0Eh	IOINTEN1	GPIO Interrupt Enable Register 1
1C0Fh	IOINTEN2	GPIO Interrupt Enable Register 2
1C10h	IOINTFLG1	GPIO Interrupt Flag Register 1
1C11h	IOINTFLG2	GPIO Interrupt Flag Register 2

(1) For more information on the GPIO module and its registers please, see the *TMS320C5515/14/05/04/VC05/VC04 DSP General-Purpose Input/Output (GPIO) User's Guide* (SPRUFO4).

Table 1-8. DMA Controller 0 (DMA0) Registers[(1)]

CPU Word Address	Acronym	Register Description
0C00h	DMACH0SSAL	Channel 0 Source Start Address (Lower Part) Register
0C01h	DMACH0SSAU	Channel 0 Source Start Address (Upper Part) Register
0C02h	DMACH0DSAL	Channel 0 Destination Start Address (Lower Part) Register
0C03h	DMACH0DSAU	Channel 0 Destination Start Address (Upper Part) Register
0C04h	DMACH0TCR1	Channel 0 Transfer Control Register 1
0C05h	DMACH0TCR2	Channel 0 Transfer Control Register 2
0C20h	DMACH1SSAL	Channel 1 Source Start Address (Lower Part) Register
0C21h	DMACH1SSAU	Channel 1 Source Start Address (Upper Part) Register
0C22h	DMACH1DSAL	Channel 1 Source Start Address (Lower Part) Register
0C23h	DMACH1DSAU	Channel 1 Destination Start Address (Upper Part) Register
0C24h	DMACH1TCR1	Channel 1 Transfer Control Register 1
0C25h	DMACH1TCR2	Channel 1 Transfer Control Register 2
0C40h	DMACH2SSAL	Channel 2 Source Start Address (Lower Part) Register
0C41h	DMACH2SSAU	Channel 2 Source Start Address (Upper Part) Register
0C42h	DMACH2DSAL	Channel 2 Destination Start Address (Lower Part) Register
0C43h	DMACH2DSAU	Channel 2 Destination Start Address (Upper Part) Register

(1) For more information on the DMA controllers and their registers, see the *TMS320VC5505/5504 DSP Direct Memory Access (DMA) Controller User's Guide* (SPRUFO9).

Table 1-8. DMA Controller 0 (DMA0) Registers[1] (continued)

CPU Word Address	Acronym	Register Description
0C44h	DMACH2TCR1	Channel 2 Transfer Control Register 1
0C45h	DMACH2TCR2	Channel 2 Transfer Control Register 2
0C60h	DMACH3SSAL	Channel 3 Source Start Address (Lower Part) Register
0C61h	DMACH3SSAU	Channel 3 Source Start Address (Upper Part) Register
0C62h	DMACH3DSAL	Channel 3 Destination Start Address (Lower Part) Register
0C63h	DMACH3DSAU	Channel 3 Destination Start Address (Upper Part) Register
0C64h	DMACH3TCR1	Channel 3 Transfer Control Register 1
0C65h	DMACH3TCR2	Channel 3 Transfer Control Register 2

Table 1-9. DMA Controller 1 (DMA1) Registers[1]

CPU Word Address	Acronym	Register Description
0D00h	DMACH0SSAL	Channel 0 Source Start Address (Lower Part) Register
0D01h	DMACH0SSAU	Channel 0 Source Start Address (Upper Part) Register
0D02h	DMACH0DSAL	Channel 0 Destination Start Address (Lower Part) Register
0D03h	DMACH0DSAU	Channel 0 Destination Start Address (Upper Part) Register
0D04h	DMACH0TCR1	Channel 0 Transfer Control Register 1
0D05h	DMACH0TCR2	Channel 0 Transfer Control Register 2
0D20h	DMACH1SSAL	Channel 1 Source Start Address (Lower Part) Register
0D21h	DMACH1SSAU	Channel 1 Source Start Address (Upper Part) Register
0D22h	DMACH1DSAL	Channel 1 Destination Start Address (Lower Part) Register
0D23h	DMACH1DSAU	Channel 1 Destination Start Address (Upper Part) Register
0D24h	DMACH1TCR1	Channel 1 Transfer Control Register 1
0D25h	DMACH1TCR2	Channel 1 Transfer Control Register 2
0D40h	DMACH2SSAL	Channel 2 Source Start Address (Lower Part) Register
0D41h	DMACH2SSAU	Channel 2 Source Start Address (Upper Part) Register
0D42h	DMACH2DSAL	Channel 2 Destination Start Address (Lower Part) Register
0D43h	DMACH2DSAU	Channel 2 Destination Start Address (Upper Part) Register
0D44h	DMACH2TCR1	Channel 2 Transfer Control Register 1
0D45h	DMACH2TCR2	Channel 2 Transfer Control Register 2
0D60h	DMACH3SSAL	Channel 3 Source Start Address (Lower Part) Register
0D61h	DMACH3SSAU	Channel 3 Source Start Address (Upper Part) Register
0D62h	DMACH3DSAL	Channel 3 Destination Start Address (Lower Part) Register
0D63h	DMACH3DSAU	Channel 3 Destination Start Address (Upper Part) Register
0D64h	DMACH3TCR1	Channel 3 Transfer Control Register 1
0D65h	DMACH3TCR2	Channel 3 Transfer Control Register 2

[1] For more information on the DMA controllers and their registers, see the *TMS320VC5505/5504 DSP Direct Memory Access (DMA) Controller User's Guide* (SPRUFO9).

Table 1-10. DMA Controller 2 (DMA2) Registers[1]

CPU Word Address	Acronym	Register Description
0E00h	DMACH0SSAL	Channel 0 Source Start Address (Lower Part) Register
0E01h	DMACH0SSAU	Channel 0 Source Start Address (Upper Part) Register
0E02h	DMACH0DSAL	Channel 0 Destination Start Address (Lower Part) Register

[1] For more information on the DMA controllers and their registers, see the *TMS320VC5505/5504 DSP Direct Memory Access (DMA) Controller User's Guide* (SPRUFO9).

Table 1-10. DMA Controller 2 (DMA2) Registers[1] (continued)

CPU Word Address	Acronym	Register Description
0E03h	DMACH0DSAU	Channel 0 Destination Start Address (Upper Part) Register
0E04h	DMACH0TCR1	Channel 0 Transfer Control Register 1
0E05h	DMACH0TCR2	Channel 0 Transfer Control Register 2
0E20h	DMACH1SSAL	Channel 1 Source Start Address (Lower Part) Register
0E21h	DMACH1SSAU	Channel 1 Source Start Address (Upper Part) Register
0E22h	DMACH1DSAL	Channel 1 Destination Start Address (Lower Part) Register
0E23h	DMACH1DSAU	Channel 1 Destination Start Address (Upper Part) Register
0E24h	DMACH1TCR1	Channel 1 Transfer Control Register 1
0E25h	DMACH1TCR2	Channel 1 Transfer Control Register 2
0E40h	DMACH2SSAL	Channel 2 Source Start Address (Lower Part) Register
0E41h	DMACH2SSAU	Channel 2 Source Start Address (Upper Part) Register
0E42h	DMACH2DSAL	Channel 2 Destination Start Address (Lower Part) Register
0E43h	DMACH2DSAU	Channel 2 Destination Start Address (Upper Part) Register
0E44h	DMACH2TCR1	Channel 2 Transfer Control Register 1
0E45h	DMACH2TCR2	Channel 2 Transfer Control Register 2
0E60h	DMACH3SSAL	Channel 3 Source Start Address (Lower Part) Register
0E61h	DMACH3SSAU	Channel 3 Source Start Address (Upper Part) Register
0E62h	DMACH3DSAL	Channel 3 Destination Start Address (Lower Part) Register
0E63h	DMACH3DSAU	Channel 3 Destination Start Address (Upper Part) Register
0E64h	DMACH3TCR1	Channel 3 Transfer Control Register 1
0E65h	DMACH3TCR2	Channel 3 Transfer Control Register 2

Table 1-11. DMA Controller 3 (DMA3) Registers[1]

CPU Word Address	Acronym	Register Description
0F00h	DMACH0SSAL	Channel 0 Source Start Address (Lower Part) Register
0F01h	DMACH0SSAU	Channel 0 Source Start Address (Upper Part) Register
0F02h	DMACH0DSAL	Channel 0 Destination Start Address (Lower Part) Register
0F03h	DMACH0DSAU	Channel 0 Destination Start Address (Upper Part) Register
0F04h	DMACH0TCR1	Channel 0 Transfer Control Register 1
0F05h	DMACH0TCR2	Channel 0 Transfer Control Register 2
0F20h	DMACH1SSAL	Channel 1 Source Start Address (Lower Part) Register
0F21h	DMACH1SSAU	Channel 1 Source Start Address (Upper Part) Register
0F22h	DMACH1DSAL	Channel 1 Destination Start Address (Lower Part) Register
0F23h	DMACH1DSAU	Channel 1 Destination Start Address (Upper Part) Register
0F24h	DMACH1TCR1	Channel 1 Transfer Control Register 1
0F25h	DMACH1TCR2	Channel 1 Transfer Control Register 2
0F40h	DMACH2SSAL	Channel 2 Source Start Address (Lower Part) Register
0F41h	DMACH2SSAU	Channel 2 Source Start Address (Upper Part) Register
0F42h	DMACH2DSAL	Channel 2 Destination Start Address (Lower Part) Register
0F43h	DMACH2DSAU	Channel 2 Destination Start Address (Upper Part) Register
0F44h	DMACH2TCR1	Channel 2 Transfer Control Register 1
0F45h	DMACH2TCR2	Channel 2 Transfer Control Register 2
0F60h	DMACH3SSAL	Channel 3 Source Start Address (Lower Part) Register
0F61h	DMACH3SSAU	Channel 3 Source Start Address (Upper Part) Register

(1) For more information on the DMA controllers and their registers, see the *TMS320VC5505/5504 DSP Direct Memory Access (DMA) Controller User's Guide* (SPRUFO9).

Table 1-11. DMA Controller 3 (DMA3) Registers[1] (continued)

CPU Word Address	Acronym	Register Description
0F62h	DMACH3DSAL	Channel 3 Destination Start Address (Lower Part) Register
0F63h	DMACH3DSAU	Channel 3 Destination Start Address (Upper Part) Register
0F64h	DMACH3TCR1	Channel 3 Transfer Control Register 1
0F65h	DMACH3TCR2	Channel 3 Transfer Control Register 2

Table 1-12. External Memory Interface (EMIF) Registers[1] [2]

CPU Word Address	Acronym	Register Description
1000h	REV	Revision Register
1001h	STATUS	Status Register
1004h	AWCCR1	Asynchronous Wait Cycle Configuration Register 1
1005h	AWCCR2	Asynchronous Wait Cycle Configuration Register 2
1010h	ACS2CR1	Asynchronous CS2 Configuration Register 1
1011h	ACS2CR2	Asynchronous CS2 Configuration Register 2
1014h	ACS3CR1	Asynchronous CS3 Configuration Register 1
1015h	ACS3CR2	Asynchronous CS3 Configuration Register 2
1018h	ACS4CR1	Asynchronous CS4 Configuration Register 1
1019h	ACS4CR2	Asynchronous CS4 Configuration Register 2
101Ch	ACS5CR1	Asynchronous CS5 Configuration Register 1
101Dh	ACS5CR2	Asynchronous CS5 Configuration Register 2
1040h	EIRR	EMIF Interrupt Raw Register
1044h	EIMR	EMIF Interrupt Mask Register
1048h	EIMSR	EMIF Interrupt Mask Set Register
104Ch	EIMCR	EMIF Interrupt Mask Clear Register
1060h	NANDFCR	NAND Flash Control Register
1064h	NANDFSR1	NAND Flash Status Register 1
1065h	NANDFSR2	NAND Flash Status Register 2
1068h	PGMODECTRL1	Page Mode Control Register 1
1069h	PGMODECTRL2	Page Mode Control Register 2
1070h	NCS2ECC1	NAND Flash CS2 1-Bit ECC Register 1
1071h	NCS2ECC2	NAND Flash CS2 1-Bit ECC Register 2
1074h	NCS3ECC1	NAND Flash CS3 1-Bit ECC Register 1
1075h	NCS3ECC2	NAND Flash CS3 1-Bit ECC Register 2
1078h	NCS4ECC1	NAND Flash CS4 1-Bit ECC Register 1
1079h	NCS4ECC2	NAND Flash CS4 1-Bit ECC Register 2
107Ch	NCS5ECC1	NAND Flash CS5 1-Bit ECC Register 1
107Dh	NCS5ECC2	NAND Flash CS5 1-Bit ECC Register 2
10BCh	NAND4BITECCLOAD	NAND Flash 4-Bit ECC Load Register
10C0h	NAND4BITECC1	NAND Flash 4-Bit ECC Register 1
10C1h	NAND4BITECC2	NAND Flash 4-Bit ECC Register 2
10C4h	NAND4BITECC3	NAND Flash 4-Bit ECC Register 3
10C5h	NAND4BITECC4	NAND Flash 4-Bit ECC Register 4
10C8h	NAND4BITECC5	NAND Flash 4-Bit ECC Register 5

(1) Before reading or writing to the EMIF registers, be sure to set the BYTEMODE bits to 00b in the EMIF system control register to enable word accesses to the EMIF registers.

(2) For more information on the EMIF and its registers, see the *TMS320VC5505/5504 DSP External Memory Interface (EMIF) User's Guide* (SPRUFO8).

Table 1-12. External Memory Interface (EMIF) Registers[1] [2] (continued)

CPU Word Address	Acronym	Register Description
10C9h	NAND4BITECC6	NAND Flash 4-Bit ECC Register 6
10CCh	NAND4BITECC7	NAND Flash 4-Bit ECC Register 7
10CDh	NAND4BITECC8	NAND Flash 4-Bit ECC Register 8
10D0h	NANDERRADD1	NAND Flash 4-Bit ECC Error Address Register 1
10D1h	NANDERRADD2	NAND Flash 4-Bit ECC Error Address Register 2
10D4h	NANDERRADD3	NAND Flash 4-Bit ECC Error Address Register 3
10D5h	NANDERRADD4	NAND Flash 4-Bit ECC Error Address Register 4
10D8h	NANDERRVAL1	NAND Flash 4-Bit ECC Error Value Register 1
10D9h	NANDERRVAL2	NAND Flash 4-Bit ECC Error Value Register 2
10DCh	NANDERRVAL3	NAND Flash 4-Bit ECC Error Value Register 3
10DDh	NANDERRVAL4	NAND Flash 4-Bit ECC Error Value Register 4

Table 1-13. Watchdog Timer Registers[1]

CPU Word Address	Acronym	Register Description
1880h	WDKCKLK	Watchdog Kick Lock Register
1882h	WDKICK	Watchdog Kick Register
1884h	WDSVLR	Watchdog Start Value Lock Register
1886h	WDSVR	Watchdog Start Value Register
1888h	WDENLOK	Watchdog Enable Lock Register
188Ah	WDEN	Watchdog Enable Register
188Ch	WDPSLR	Watchdog Prescale Lock Register
188Eh	WDPS	Watchdog Prescale Register

(1) For more information on the DMA controllers and their registers, see the *TMS320C5515/14/05/04/VC05/VC04 DSP 32-Bit Timer/Watchdog Timer User's Guide* (SPRUFO2).

Table 1-14. General-Purpose Timer 0 Registers[1]

CPU Word Address	Acronym	Register Description
1810h	TCR	Timer 0 Control Register
1812h	TIMPRD1	Timer 0 Period Register 1
1813h	TIMPRD2	Timer 0 Period Register 2
1814h	TIMCNT1	Timer 0 Counter Register 1
1815h	TIMCNT2	Timer 0 Counter Register 2
1816h	TIMINT	Timer 0 Interrupt Register

(1) For more information on the general-purpose timers and their registers, see the *TMS320C5515/14/05/04/VC05/VC04 DSP 32-Bit Timer/Watchdog Timer User's Guide* (SPRUFO2).

Table 1-15. General-Purpose Timer 1 Registers[1]

CPU Word Address	Acronym	Register Description
1850h	TCR	Timer 1 Control Register
1852h	TIMPRD1	Timer 1 Period Register 1
1853h	TIMPRD2	Timer 1 Period Register 2
1854h	TIMCNT1	Timer 1 Counter Register 1
1855h	TIMCNT2	Timer 1 Counter Register 2
1856h	TIMINT	Timer 1 Interrupt Register

(1) For more information on the general-purpose timers and their registers, see the *TMS320C5515/14/05/04/VC05/VC04 DSP 32-Bit Timer/Watchdog Timer User's Guide* (SPRUFO2).

Table 1-16. General-Purpose Timer 2 Registers[1]

CPU Word Address	Acronym	Register Description
1890h	TCR	Timer 2 Control Register
1892h	TIMPRD1	Timer 2 Period Register 1
1893h	TIMPRD2	Timer 2 Period Register 2
1894h	TIMCNT1	Timer 2 Counter Register 1
1895h	TIMCNT2	Timer 2 Counter Register 2
1896h	TIMINT	Timer 2 Interrupt Register

(1) For more information on the general-purpose timers and their registers, see the *TMS320C5515/14/05/04/VC05/VC04 DSP Timer/Watchdog Timer User's Guide* (SPRUFO2).

Table 1-17. Real Time Clock (RTC) Registers[1]

CPU Word Address	Acronym	Register Description
1900h	RTCINTEN	RTC Interrupt Enable Register
1901h	RTCUPDATE	RTC Update Register
1904h	RTCMIL	Milli Seconds Register
1905h	RTCMILA	Milli Seconds Alarm Register
1908h	RTCSEC	Seconds Register
1909h	RTCSECA	Seconds Alarm Register
190Ch	RTCMIN	Minutes Register
190Dh	RTCMINA	Minutes Alarm Register
1910h	RTCHOUR	Hours Register
1911h	RTCHOURA	Hours Alarm Register
1914h	RTCDAY	Days Register
1915h	RTCDAYA	Days Alarm Register
1918h	RTCMONTH	Months Register
1919h	RTCMONTHA	Months Alarm Register
191Ch	RTCYEAR	Years Register
191Dh	RTCYEARA	Years Alarm Register
1920h	RTCINTFL	RTC Interrupt Flag Register (See Section 1.5.6.2.)
1921h	RTCNOPWR	RTC Lost Power Status Register
1924h	RTCINTREG	RTC Interrupt Register
1928h	RTCDRIFT	RTC Compensation Register
192Ch	RTCOSC	RTC Oscillator Register
1930h	RTCPMGT	RTC Power Management Register (See Section 1.5.6.1.)

(1) For more information on RTC and its registers, see the *TMS320VC5505/5504 DSP Real-Time Clock (RTC) User's Guide* (SPRUFO7).

Table 1-17. Real Time Clock (RTC) Registers[1] (continued)

CPU Word Address	Acronym	Register Description
1960h	RTCSCR1	RTC LSW Scratch Register 1
1961h	RTCSCR2	RTC MSW Scratch Register 2
1964h	RTCSCR3	RTC LSW Scratch Register 3
1965h	RTCSCR4	RTC MSW Scratch Register 4

Table 1-18. Inter-Integrated Circuit (I2C) Registers[1]

CPU Word Address	Acronym	Register Description
1A00h	ICOAR	I2C Own Address Register
1A04h	ICIMR	I2C Interrupt Mask Register
1A08h	ICSTR	I2C Interrupt Status Register
1A0Ch	ICCLKL	I2C Clock Low-Time Divider Register
1A10h	ICCLKH	I2C Clock High-Time Divider Register
1A14h	ICCNT	I2C Data Count Register
1A18h	ICDRR	I2C Data Receive Register
1A1Ch	ICSAR	I2C Slave Address Register
1A20h	ICDXR	I2C Data Transmit Register
1A24h	ICMDR	I2C Mode Register
1A28h	ICIVR	I2C Interrupt Vector Register
1A2Ch	ICEMDR	I2C Extended Mode Register
1A30h	ICPSC	I2C Prescaler Register
1A34h	ICPID1	I2C Peripheral Identification Register 1
1A38h	ICPID2	I2C Peripheral Identification Register 2

(1) For more information on I2C and its registers, see the *TMS320C5515/14/05/04/VC05/VC04 DSP Inter-Integrated Circuit (I2C) User's Guide* (SPRUFO1).

Table 1-19. UART Registers[1]

CPU Word Address	Acronym	Register Description
1B00h	RBR	Receiver Buffer Register (read only)
1B00h	THR	Transmitter Holding Register (write only)
1B02h	IER	Interrupt Enable Register
1B04h	IIR	Interrupt Identification Register (read only)
1B04h	FCR	FIFO Control Register (write only)
1B06h	LCR	Line Control Register
1B08h	MCR	Modem Control Register
1B0Ah	LSR	Line Status Register
1B0Eh	SCR	Scratch Register
1B10h	DLL	Divisor LSB Latch
1B12h	DLH	Divisor MSB Latch
1B18h	PWREMU_MGMT	Power and Emulation Management Register

(1) For more information on UART and its registers, see the *TMS320C5515/14/05/04/VC05/VC04 DSP Universal Asynchronous Receiver/Transmitter (UART) User's Guide* (SPRUFO5).

Table 1-20. I2S0 Registers[1]

CPU Word Address	Acronym	Description
2800h	I2SSCTRL	I2S Serializer Control Register
2804h	I2SSRATE	I2S Sample Rate Generator Register
2808h	I2STXLT0	I2S Transmit Left Data 0 Register
2809h	I2STXLT1	I2S Transmit Left Data 1 Register
280Ch	I2STXRT0	I2S Transmit Right Data 0 Register
280Dh	I2STXRT1	I2S Transmit Right Data 1 Register
2810h	I2SINTFL	I2S Interrupt Flag Register
2814h	I2SINTMASK	I2S Interrupt Mask Register
2828h	I2SRXLT0	I2S Receive Left Data 0 Register
2829h	I2SRXLT1	I2S Receive Left Data 1 Register
282Ch	I2SRXRT0	I2S Receive Right Data 0 Register
282Dh	I2SRXRT1	I2S Receive Right Data 1 Register

(1) For more information on I2S0 and its registers, see the *TMS320VC5505/5504 DSP Inter-IC Sound (I2S)* User's Guide (SPRUFP4).

Table 1-21. I2S1 Registers[1]

CPU Word Address	Acronym	Description
2900h	I2SSCTRL	I2S Serializer Control Register
2904h	I2SSRATE	I2S Sample Rate Generator Register
2908h	I2STXLT0	I2S Transmit Left Data 0 Register
2909h	I2STXLT1	I2S Transmit Left Data 1 Register
290Ch	I2STXRT0	I2S Transmit Right Data 0 Register
290Dh	I2STXRT1	I2S Transmit Right Data 1 Register
2910h	I2SINTFL	I2S Interrupt Flag Register
2914h	I2SINTMASK	I2S Interrupt Mask Register
2928h	I2SRXLT0	I2S Receive Left Data 0 Register
2929h	I2SRXLT1	I2S Receive Left Data 1 Register
292Ch	I2SRXRT0	I2S Receive Right Data 0 Register
292Dh	I2SRXRT1	I2S Receive Right Data 1 Register

(1) For more information on I2S1 and its registers, see the *TMS320VC5505/5504 DSP Inter-IC Sound (I2S) User's Guide* (SPRUFP4).

Table 1-22. I2S2 Registers[1]

CPU Word Address	Acronym	Description
2A00h	I2SSCTRL	I2S Serializer Control Register
2A04h	I2SSRATE	I2S Sample Rate Generator Register
2A08h	I2STXLT0	I2S Transmit Left Data 0 Register
2A09h	I2STXLT1	I2S Transmit Left Data 1 Register
2A0Ch	I2STXRT0	I2S Transmit Right Data 0 Register
2A0Dh	I2STXRT1	I2S Transmit Right Data 1 Register
2A10h	I2SINTFL	I2S Interrupt Flag Register
2A14h	I2SINTMASK	I2S Interrupt Mask Register
2A28h	I2SRXLT0	I2S Receive Left Data 0 Register
2A29h	I2SRXLT1	I2S Receive Left Data 1 Register

(1) For more information on I2S2 and its registers, see the *TMS320VC5505/5504 DSP Inter-IC Sound (I2S)* User's Guide (SPRUFP4).

Table 1-22. I2S2 Registers[1] (continued)

CPU Word Address	Acronym	Description
2A2Ch	I2SRXRT0	I2S Receive Right Data 0 Register
2A2Dh	I2SRXRT1	I2S Receive Right Data 1 Register

Table 1-23. I2S3 Register[1]

CPU Word Address	Acronym	Description
2B00h	I2SSCTRL	I2S Serializer Control Register
2B04h	I2SSRATE	I2S Sample Rate Generator Register
2B08h	I2STXLT0	I2S Transmit Left Data 0 Register
2B09h	I2STXLT1	I2S Transmit Left Data 1 Register
2B0Ch	I2STXRT0	I2S Transmit Right Data 0 Register
2B0Dh	I2STXRT1	I2S Transmit Right Data 1 Register
2B10h	I2SINTFL	I2S Interrupt Flag Register
2B14h	I2SINTMASK	I2S Interrupt Mask Register
2B28h	I2SRXLT0	I2S Receive Left Data 0 Register
2B29h	I2SRXLT1	I2S Receive Left Data 1 Register
2B2Ch	I2SRXRT0	I2S Receive Right Data 0 Register
2B2Dh	I2SRXRT1	I2S Receive Right Data 1 Register

(1) For more information on I2S3 and its registers, see the *TMS320VC5505/5504 DSP Inter-IC Sound (I2S)* User's Guide (SPRUFP4).

Table 1-24. LCD Controller Registers[1]

CPU Word Address	Acronym	Register Description
0000h	LCDREVMIN	LCD Minor Revision Register
0001h	LCDREVMAJ	LCD Major Revision Register
0004h	LCDCR	LCD Control Register
0008h	LCDSR	LCD Status Register
000Ch	LCDLIDDCR	LCD LIDD Control Register
0010h	LCDLIDDCS0CONFIG0	LCD LIDD CS0 Configuration Register 0
0011h	LCDLIDDCS0CONFIG1	LCD LIDD CS0 Configuration Register 1
0014h	LCDLIDDCS0ADDR	LCD LIDD CS0 Address Read/Write Register
0018h	LCDLIDDCS0DATA	LCD LIDD CS0 Data Read/Write Register
001Ch	LCDLIDDCS1CONFIG0	LCD LIDD CS1 Configuration Register 0
001Dh	LCDLIDDCS1CONFIG1	LCD LIDD CS1 Configuration Register 1
0020h	LCDLIDDCS1ADDR	LCD LIDD CS1 Address Read/Write Register
0024h	LCDLIDDCS1DATA	LCD LIDD CS1 Data Read/Write Register
0040h	LCDDMACR	LCD DMA Control Register
0044h	LCDDMAFB0BAR0	LCD DMA Frame Buffer 0 Base Address Register 0
0045h	LCDDMAFB0BAR1	LCD DMA Frame Buffer 0 Base Address Register 1
0048h	LCDDMAFB0CAR0	LCD DMA Frame Buffer 0 Ceiling Address Register 0
0049h	LCDDMAFB0CAR1	LCD DMA Frame Buffer 0 Ceiling Address Register 1
004Ch	LCDDMAFB1BAR0	LCD DMA Frame Buffer 1 Base Address Register 0
004Dh	LCDDMAFB1BAR1	LCD DMA Frame Buffer 1 Base Address Register 1
0050h	LCDDMAFB1CAR0	LCD DMA Frame Buffer 1 Ceiling Address Register 0

(1) For more information on LCD controller and its registers, see the *TMS320C5515/05/VC05 Liquid Crystal Display Controller (LCDC) User's Guide* (SPRUFP3).

Table 1-24. LCD Controller Registers[1] (continued)

CPU Word Address	Acronym	Register Description
0051h	LCDDMAFB1CAR1	LCD DMA Frame Buffer 1 Ceiling Address Register 1

Table 1-25. SPI Registers[1]

CPU Word Address	Acronym	Register Description
3000h	SPICDR	Clock Divider Register
3001h	SPICCR	Clock Control Register
3002h	SPIDCR1	Device Configuration Register 1
3003h	SPIDCR2	Device Configuration Register 2
3004h	SPICMD1	Command Register 1
3005h	SPICMD2	Command Register 2
3006h	SPISTAT1	Status Register 1
3007h	SPISTAT2	Status Register 2
3008h	SPIDAT1	Data Register 1
3009h	SPIDAT2	Data Register 2

(1) For more information on SPI and its registers, see the *TMS320C5515/14/05/04/VC05/VC04 DSP Serial Peripheral Interface (SPI) User's Guide* (SPRUF03).

Table 1-26. MMC/SD0 Registers

CPU Word Address	Acronym	Register Description
3A00h	MMCCTL	MMC Control Register
3A04h	MMCCLK	MMC Memory Clock Control Register
3A08h	MMCST0	MMC Status Register 0
3A0Ch	MMCST1	MMC Status Register 1
3A10h	MMCIM	MMC Interrupt Mask Register
3A14h	MMCTOR	MMC Response Time-Out Register
3A18h	MMCTOD	MMC Data Read Time-Out Register
3A1Ch	MMCBLEN	MMC Block Length Register
3A20h	MMCNBLK	MMC Number of Blocks Register
3A24h	MMCNBLC	MMC Number of Blocks Counter Register
3A28h	MMCDRR1	MMC Data Receive Register 1
3A29h	MMCDRR2	MMC Data Receive Register 2
3A2Ch	MMCDXR1	MMC Data Transmit Register 1
3A2Dh	MMCDXR2	MMC Data Transmit Register 2
3A30h	MMCCMD1	MMC Command Register 1
3A31h	MMCCMD2	MMC Command Register 2
3A34h	MMCARG1	MMC Argument Register 1
3A35h	MMCARG2	MMC Argument Register 2
3A38h	MMCRSP0	MMC Response Register 0
3A39h	MMCRSP1	MMC Response Register 1
3A3Ch	MMCRSP2	MMC Response Register 2
3A3Dh	MMCRSP3	MMC Response Register 3
3A40h	MMCRSP4	MMC Response Register 4
3A41h	MMCRSP5	MMC Response Register 5
3A44h	MMCRSP6	MMC Response Register 6

Table 1-26. MMC/SD0 Registers (continued)

CPU Word Address	Acronym	Register Description
3A45h	MMCRSP7	MMC Response Register 7
3A48h	MMCDRSP	MMC Data Response Register
3A50h	MMCCIDX	MMC Command Index Register
3A64h	SDIOCTL	SDIO Control Register
3A68h	SDIOST0	SDIO Status Register 0
3A6Ch	SDIOIEN	SDIO Interrupt Enable Register
3A70h	SDIOIST	SDIO Interrupt Status Register
3A74h	MMCFIFOCTL	MMC FIFO Control Register

Table 1-27. MMC/SD1 Registers[(1)]

CPU Word Address	Acronym	Register Description
3B00h	MMCCTL	MMC Control Register
3B04h	MMCCLK	MMC Memory Clock Control Register
3B08h	MMCST0	MMC Status Register 0
3B0Ch	MMCST1	MMC Status Register 1
3B10h	MMCIM	MMC Interrupt Mask Register
3B14h	MMCTOR	MMC Response Time-Out Register
3B18h	MMCTOD	MMC Data Read Time-Out Register
3B1Ch	MMCBLEN	MMC Block Length Register
3B20h	MMCNBLK	MMC Number of Blocks Register
3B24h	MMCNBLC	MMC Number of Blocks Counter Register
3B28h	MMCDRR1	MMC Data Receive Register 1
3B29h	MMCDRR2	MMC Data Receive Register 2
3B2Ch	MMCDXR1	MMC Data Transmit Register 1
3B2Dh	MMCDXR2	MMC Data Transmit Register 2
3B30h	MMCCMD1	MMC Command Register 1
3B31h	MMCCMD2	MMC Command Register 2
3B34h	MMCARG1	MMC Argument Register 1
3B35h	MMCARG2	MMC Argument Register 2
3B38h	MMCRSP0	MMC Response Register 0
3B39h	MMCRSP1	MMC Response Register 1
3B3Ch	MMCRSP2	MMC Response Register 2
3B3Dh	MMCRSP3	MMC Response Register 3
3B40h	MMCRSP4	MMC Response Register 4
3B41h	MMCRSP5	MMC Response Register 5
3B44h	MMCRSP6	MMC Response Register 6
3B45h	MMCRSP7	MMC Response Register 7
3B48h	MMCDRSP	MMC Data Response Register
3B50h	MMCCIDX	MMC Command Index Register
3B64h	SDIOCTL	SDIO Control Register
3B68h	SDIOST0	SDIO Status Register 0
3B6Ch	SDIOIEN	SDIO Interrupt Enable Register
3B70h	SDIOIST	SDIO Interrupt Status Register
3B74h	MMCFIFOCTL	MMC FIFO Control Register

(1) For more information on MMC/SD1 and its registers, see the *TMS320VC5505/5504 DSP Multimedia Card (MMC)/Secure Digital (SD) Card Controller User's Guide* (SPRUFO6).

Table 1-28. Analog Control Registers[1]

CPU Word Address	Acronym	Register Description
7012h	SARCTRL	SAR A/D Control Register
7014h	SARDATA	SAR A/D Data Register
7016h	SARCLKCTRL	SAR A/D Clock Control Register
7018h	SARPINCTRL	SAR A/D Reference and Pin Control Register
701Ah	SARGPOCTRL	SAR A/D GPO Control Register

(1) For more information on analog control registers, see the *TMS320C5515/05/VC05 DSP Successive Approximation A/D Converter (SAR) User's Guide* (SPRUFP1).

Table 1-29. Universal Serial Bus (USB) Registers[1] [2]

CPU Word Address	Acronym	Register Description
8000h	REVID1	Revision Identification Register 1
8001h	REVID2	Revision Identification Register 2
8004h	CTRLR	Control Register
8008h	STATR	Status Register
800Ch	EMUR	Emulation Register
8010h	MODER1	Mode Register 1
8011h	MODER2	Mode Register 2
8014h	AUTOREQ	Auto Request Register
8018h	SRPFIXTIME1	SRP Fix Time Register 1
8019h	SRPFIXTIME2	SRP Fix Time Register 2
801Ch	TEARDOWN1	Teardown Register 1
801Dh	TEARDOWN2	Teardown Register 2
8020h	INTSRCR1	USB Interrupt Source Register 1
8021h	INTSRCR2	USB Interrupt Source Register 2
8024h	INTSETR1	USB Interrupt Source Set Register 1
8025h	INTSETR2	USB Interrupt Source Set Register 2
8028h	INTCLRR1	USB Interrupt Source Clear Register 1
8029h	INTCLRR2	USB Interrupt Source Clear Register 2
802Ch	INTMSKR1	USB Interrupt Mask Register 1
802Dh	INTMSKR2	USB Interrupt Mask Register 2
8030h	INTMSKSETR1	USB Interrupt Mask Set Register 1
8031h	INTMSKSETR2	USB Interrupt Mask Set Register 2
8034h	INTMSKCLRR1	USB Interrupt Mask Clear Register 1
8035h	INTMSKCLRR2	USB Interrupt Mask Clear Register 2
8038h	INTMASKEDR1	USB Interrupt Source Masked Register 1
8039h	INTMASKEDR2	USB Interrupt Source Masked Register 2
803Ch	EOIR	USB End of Interrupt Register
8040h	INTVECTR1	USB Interrupt Vector Register 1
8041h	INTVECTR2	USB Interrupt Vector Register 2
8050h	GREP1SZR1	Generic RNDIS EP1Size Register 1
8051h	GREP1SZR2	Generic RNDIS EP1Size Register 2
8054h	GREP2SZR1	Generic RNDIS EP2 Size Register 1
8055h	GREP2SZR2	Generic RNDIS EP2 Size Register 2

(1) Before reading or writing to the USB registers, be sure to set the BYTEMODE bits to 00b in the USB system control register (Section 1.5.5.4.2) to enable word accesses to the USB registers.

(2) For more information on USB and its registers, see the *TMS320VC5505/5504 DSP Universal Serial Bus (USB) User's Guide* (SPRUFO0).

Table 1-29. Universal Serial Bus (USB) Registers[1] [2] (continued)

CPU Word Address	Acronym	Register Description
8058h	GREP3SZR1	Generic RNDIS EP3 Size Register 1
8059h	GREP3SZR2	Generic RNDIS EP3 Size Register 2
805Ch	GREP4SZR1	Generic RNDIS EP4 Size Register 1
805Dh	GREP4SZR2	Generic RNDIS EP4 Size Register 2
		Common USB Registers
8400h	FADDR_POWER	Function Address Register, Power Management Register
8401h	INTRTX	Interrupt Register for Endpoint 0 plus Transmit Endpoints 1 to 4
8404h	INTRRX	Interrupt Register for Receive Endpoints 1 to 4
8405h	INTRTXE	Interrupt enable register for INTRTX
8408h	INTRRXE	Interrupt Enable Register for INTRRX
8409h	INTRUSB_INTRUSBE	Interrupt Register for Common USB Interrupts, Interrupt Enable Register
840Ch	FRAME	Frame Number Register
840Dh	INDEX_TESTMODE	Index Register for Selecting the Endpoint Status and Control Registers, Register to Enable the USB 2.0 Test Modes
		USB Indexed Registers
8410h	TXMAXP_INDX	Maximum Packet Size for Peripheral/Host Transmit Endpoint. (Index register set to select Endpoints 1-4)
8411h	PERI_CSR0_INDX	Control Status Register for Endpoint 0 in Peripheral Mode. (Index register set to select Endpoint 0)
	PERI_TXCSR_INDX	Control Status Register for Peripheral Transmit Endpoint. (Index register set to select Endpoints 1-4)
8414h	RXMAXP_INDX	Maximum Packet Size for Peripheral/Host Receive Endpoint. (Index register set to select Endpoints 1-4)
8415h	PERI_RXCSR_INDX	Control Status Register for Peripheral Receive Endpoint. (Index register set to select Endpoints 1-4)
8418h	COUNT0_INDX	Number of Received Bytes in Endpoint 0 FIFO. (Index register set to select Endpoint 0)
	RXCOUNT_INDX	Number of Bytes in Host Receive Endpoint FIFO. (Index register set to select Endpoints 1- 4)
8419h	-	Reserved
841Ch	-	Reserved
841Dh	CONFIGDATA_INDC (Upper byte of 841Dh)	Returns details of core configuration. (index register set to select Endpoint 0)
		USB FIFO Registers
8420h	FIFO0R1	Transmit and Receive FIFO Register 1 for Endpoint 0
8421h	FIFO0R2	Transmit and Receive FIFO Register 2 for Endpoint 0
8424h	FIFO1R1	Transmit and Receive FIFO Register 1 for Endpoint 1
8425h	FIFO1R2	Transmit and Receive FIFO Register 2 for Endpoint 1
8428h	FIFO2R1	Transmit and Receive FIFO Register 1 for Endpoint 2
8429h	FIFO2R2	Transmit and Receive FIFO Register 2 for Endpoint 2
842Ch	FIFO3R1	Transmit and Receive FIFO Register 1 for Endpoint 3
842Dh	FIFO3R2	Transmit and Receive FIFO Register 2 for Endpoint 3
8430h	FIFO4R1	Transmit and Receive FIFO Register 1 for Endpoint 4
8431h	FIFO4R2	Transmit and Receive FIFO Register 2 for Endpoint 4
		Dynamic FIFO Control Registers
8460h	-	Reserved
8461h	TXFIFOSZ_RXFIFOSZ	Transmit Endpoint FIFO Size, Receive Endpoint FIFO Size (Index register set to select Endpoints 1-4)
8464h	TXFIFOADDR	Transmit Endpoint FIFO Address (Index register set to select Endpoints 1-4)
8465h	RXFIFOADDR	Receive Endpoint FIFO Address (Index register set to select Endpoints 1-4)

Table 1-29. Universal Serial Bus (USB) Registers[1] [2] (continued)

CPU Word Address	Acronym	Register Description
846Ch	HWVERS	Hardware Version Register
8500h	-	Reserved
8501h	PERI_CSR0	Control Status Register for Peripheral Endpoint 0
8504h	-	Reserved
8505h	-	Reserved
8508h	COUNT0	Number of Received Bytes in Endpoint 0 FIFO
8509h	-	Reserved
850Ch	-	Reserved
850Dh	CONFIGDATA (Upper byte of 842Dh)	Returns details of core configuration.
	Control and Status Register for Endpoint 1	
8510h	TXMAXP	Maximum Packet Size for Peripheral/Host Transmit Endpoint
8511h	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
8514h	RXMAXP	Maximum Packet Size for Peripheral/Host Receive Endpoint
8515h	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
8518h	RXCOUNT	Number of Bytes in Host Receive endpoint FIFO
8519h	-	Reserved
851Ch	-	Reserved
851Dh	-	Reserved
	Control and Status Register for Endpoint 2	
8520h	TXMAXP	Maximum Packet Size for Peripheral/Host Transmit Endpoint
8521h	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
8524h	RXMAXP	Maximum Packet Size for Peripheral/Host Receive Endpoint
8525h	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
8528h	RXCOUNT	Number of Bytes in Host Receive endpoint FIFO
8529h	-	Reserved
852Ch	-	Reserved
852Dh	-	Reserved
	Control and Status Register for Endpoint 3	
8530h	TXMAXP	Maximum Packet Size for Peripheral/Host Transmit Endpoint
8531h	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
8534h	RXMAXP	Maximum Packet Size for Peripheral/Host Receive Endpoint
8535h	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
8538h	RXCOUNT	Number of Bytes in Host Receive endpoint FIFO
8539h	-	Reserved
853Ch	-	Reserved
853Dh	-	Reserved
	Control and Status Register for Endpoint 4	
8540h	TXMAXP	Maximum Packet Size for Peripheral/Host Transmit Endpoint
8541h	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
8544h	RXMAXP	Maximum Packet Size for Peripheral/Host Receive Endpoint
8545h	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
8548h	RXCOUNT	Number of Bytes in Host Receive endpoint FIFO
8549h	-	Reserved
854Ch	-	Reserved
854Dh	-	Reserved
9000h	DMAREVID1	CDMA Revision Identification Register 1

Table 1-29. Universal Serial Bus (USB) Registers[1] [2] (continued)

CPU Word Address	Acronym	Register Description
9001h	DMAREVID2	CDMA Revision Identification Register 2
9004h	TDFDQ	CDMA Teardown Free Descriptor Queue Control Register
9008h	DMAEMU	CDMA Emulation Control Register
9800h	TXGCR1[0]	Transmit Channel 0 Global Configuration Register 1
9801h	TXGCR2[0]	Transmit Channel 0 Global Configuration Register 2
9808h	RXGCR1[0]	Receive Channel 0 Global Configuration Register 1
9809h	RXGCR2[0]	Receive Channel 0 Global Configuration Register 2
980Ch	RXHPCR1A[0]	Receive Channel 0 Host Packet Configuration Register 1 A
980Dh	RXHPCR2A[0]	Receive Channel 0 Host Packet Configuration Register 2 A
9810h	RXHPCR1B[0]	Receive Channel 0 Host Packet Configuration Register 1 B
9811h	RXHPCR2B[0]	Receive Channel 0 Host Packet Configuration Register 2 B
9820h	TXGCR1[1]	Transmit Channel 1 Global Configuration Register 1
9821h	TXGCR2[1]	Transmit Channel 1 Global Configuration Register 2
9828h	RXGCR1[1]	Receive Channel 1 Global Configuration Register 1
9829h	RXGCR2[1]	Receive Channel 1 Global Configuration Register 2
982Ch	RXHPCR1A[1]	Receive Channel 1 Host Packet Configuration Register 1 A
982Dh	RXHPCR2A[1]	Receive Channel 1 Host Packet Configuration Register 2 A
9830h	RXHPCR1B[1]	Receive Channel 1 Host Packet Configuration Register 1 B
9831h	RXHPCR2B[1]	Receive Channel 1 Host Packet Configuration Register 2 B
9840h	TXGCR1[2]	Transmit Channel 2 Global Configuration Register 1
9841h	TXGCR2[2]	Transmit Channel 2 Global Configuration Register 2
9848h	RXGCR1[2]	Receive Channel 2 Global Configuration Register 1
9849h	RXGCR2[2]	Receive Channel 2 Global Configuration Register 2
984Ch	RXHPCR1A[2]	Receive Channel 2 Host Packet Configuration Register 1 A
984Dh	RXHPCR2A[2]	Receive Channel 2 Host Packet Configuration Register 2 A
9850h	RXHPCR1B[2]	Receive Channel 2 Host Packet Configuration Register 1 B
9851h	RXHPCR2B[2]	Receive Channel 2 Host Packet Configuration Register 2 B
9860h	TXGCR1[3]	Transmit Channel 3 Global Configuration Register 1
9861h	TXGCR2[3]	Transmit Channel 3 Global Configuration Register 2
9868h	RXGCR1[3]	Receive Channel 3 Global Configuration Register 1
9869h	RXGCR2[3]	Receive Channel 3 Global Configuration Register 2
986Ch	RXHPCR1A[3]	Receive Channel 3 Host Packet Configuration Register 1 A
986Dh	RXHPCR2A[3]	Receive Channel 3 Host Packet Configuration Register 2 A
9870h	RXHPCR1B[3]	Receive Channel 3 Host Packet Configuration Register 1 B
9871h	RXHPCR2B[3]	Receive Channel 3 Host Packet Configuration Register 2 B
A000h	DMA_SCHED_CTRL1	CDMA Scheduler Control Register 1
A001h	DMA_SCHED_CTRL2	CDMA Scheduler Control Register 1
A800h + 4 × *N*	ENTRYLSW[*N*]	CDMA Scheduler Table Word *N* Registers LSW (*N* = 0 to 63)
A801h + 4 × *N*	ENTRYMSW[*N*]	CDMA Scheduler Table Word *N* Registers MSW (*N* = 0 to 63)
	Queue Manager (QMGR) Registers	
C000h	QMGRREVID1	Queue Manager Revision Identification Register 1
C001h	QMGRREVID2	Queue Manager Revision Identification Register 2
C008h	DIVERSION1	Queue Manager Queue Diversion Register 1
C009h	DIVERSION2	Queue Manager Queue Diversion Register 2
C020h	FDBSC0	Queue Manager Free Descriptor/Buffer Starvation Count Register 0
C021h	FDBSC1	Queue Manager Free Descriptor/Buffer Starvation Count Register 1
C024h	FDBSC2	Queue Manager Free Descriptor/Buffer Starvation Count Register 2

Table 1-29. Universal Serial Bus (USB) Registers[1] [2] (continued)

CPU Word Address	Acronym	Register Description
C025h	FDBSC3	Queue Manager Free Descriptor/Buffer Starvation Count Register 3
C028h	FDBSC4	Queue Manager Free Descriptor/Buffer Starvation Count Register 4
C029h	FDBSC5	Queue Manager Free Descriptor/Buffer Starvation Count Register 5
C02Ch	FDBSC6	Queue Manager Free Descriptor/Buffer Starvation Count Register 6
C02Dh	FDBSC7	Queue Manager Free Descriptor/Buffer Starvation Count Register 7
C080h	LRAM0BASE1	Queue Manager Linking RAM Region 0 Base Address Register 1
C081h	LRAM0BASE2	Queue Manager Linking RAM Region 0 Base Address Register 2
C084h	LRAM0SIZE	Queue Manager Linking RAM Region 0 Size Register
C085h	-	Reserved
C088h	LRAM1BASE1	Queue Manager Linking RAM Region 1 Base Address Register 1
C089h	LRAM1BASE2	Queue Manager Linking RAM Region 1 Base Address Register 2
C090h	PEND0	Queue Manager Queue Pending 0
C091h	PEND1	Queue Manager Queue Pending 1
C094h	PEND2	Queue Manager Queue Pending 2
C095h	PEND3	Queue Manager Queue Pending 3
C098h	PEND4	Queue Manager Queue Pending 4
C099h	PEND5	Queue Manager Queue Pending 5
D000h + 16 × *R*	QMEMRBASE1[*R*]	Queue Manager Memory Region *R* Base Address Register 1 (*R* = 0 to 15)
D001h + 16 × *R*	QMEMRBASE2[*R*]	Queue Manager Memory Region *R* Base Address Register 2 (*R* = 0 to 15)
D004h + 16 × *R*	QMEMRCTRL1[*R*]	Queue Manager Memory Region *R* Control Register (*R* = 0 to 15)
D005h + 16 × *R*	QMEMRCTRL2[*R*]	Queue Manager Memory Region *R* Control Register (*R* = 0 to 15)
E00Ch + 16 × *N*	CTRL1D	Queue Manager Queue *N* Control Register 1 (*N* = 0 to 63)
E00Dh + 16 × *N*	CTRL2D	Queue Manager Queue *N* Control Register 2 (*N* = 0 to 63)
E800h + 16 × *N*	QSTATA	Queue Manager Queue *N* Status Register A (*N* = 0 to 63)
E804h + 16 × *N*	QSTAT1B	Queue Manager Queue *N* Status Register 1 B (*N* = 0 to 63)
E805h + 16 × *N*	QSTAT2B	Queue Manager Queue *N* Status Register 2 B (*N* = 0 to 63)
E808h + 16 × *N*	QSTATC	Queue Manager Queue *N* Status Register C (*N* = 0 to 63)

1.3 Device Clocking

1.3.1 Overview

The DSP requires two primary reference clocks: a system reference clock and a USB reference clock. The system reference clock can be driven by either the real-time clock (RTC) on-chip oscillator or by an external oscillator via the CLKIN pin. The on-chip oscillator requires a 32.768 kHz external crystal connected to the RTC_XI and RTC_XO pins. The USB reference clock is generated using a dedicated on-chip oscillator with a 12 MHz external crystal connected to the USB_MXI and USB_MXO pins. This crystal is not required if the USB peripheral is not being used.

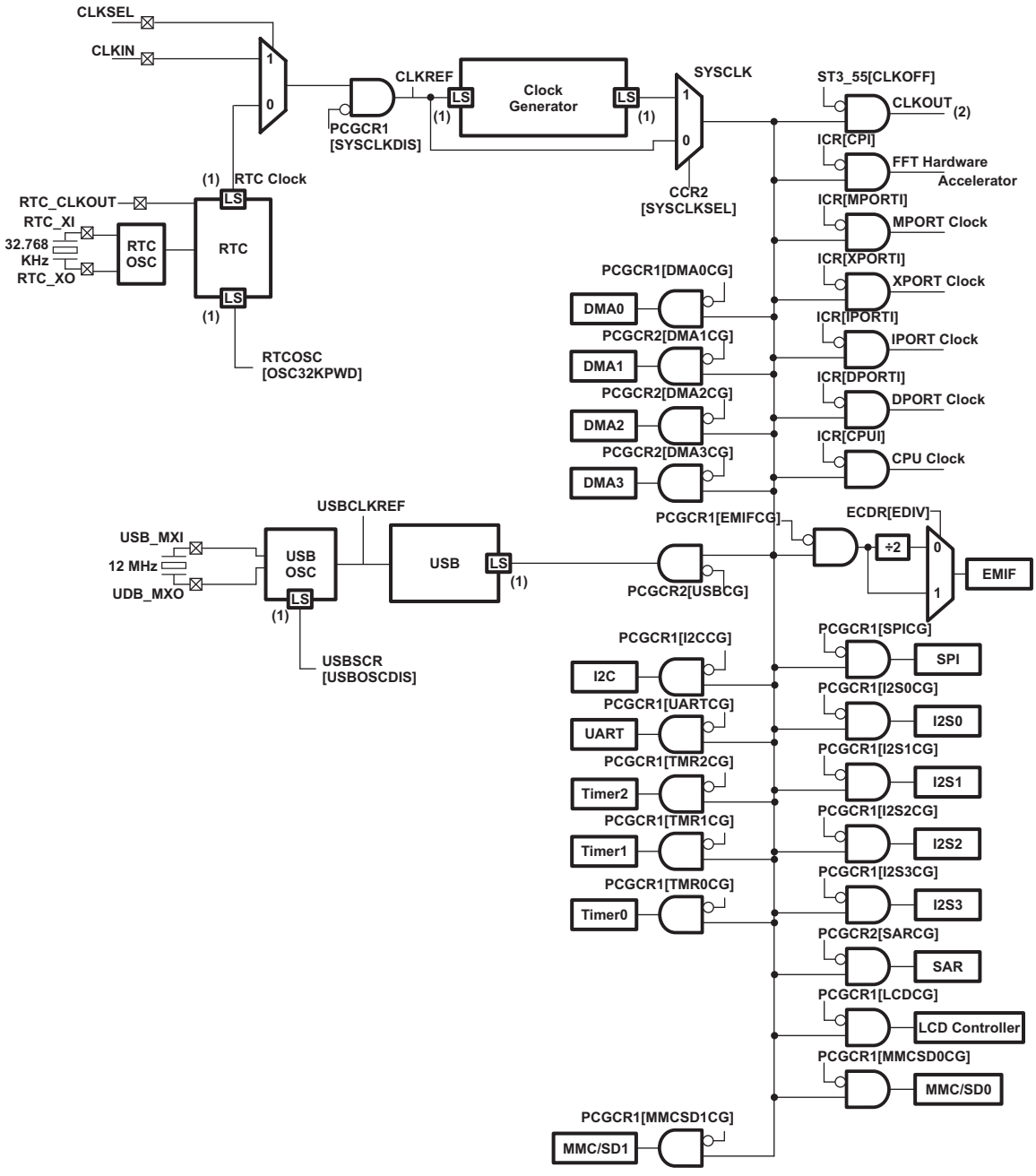
The crystal for the RTC oscillator is not required if CLKIN is used as the system reference clock, however the RTC must still be powered and the RTC registers starting at I/O address 1900h will not be accessible. This includes the RTC Power Management Register which provides control to the on-chip LDOs and WAKEUP and RTC_CLKOUT pins.

See the device-specific data manual for more details on the USB and RTC oscillator connections and crystal requirements.

The system clock generator can be used to modify the system reference clock signal according to software-programmable multiplier and dividers. The resulting clock output, the DSP system clock, is passed to the CPU, peripherals, and other modules inside the DSP. Alternatively, the system clock generator can be fully bypassed and the system reference clock can be passed directly to the DSP system clock.

Figure 1-3 shows the overall DSP clock structure. For detailed specifications on clock frequency and voltage requirements, see the device-specific data manual.

Figure 1-3. DSP Clocking Diagram



(1) LS = Level Shifter

(2) The CLKOUT pin is enabled/disabled through the CLKOFF bit of the CPU ST3_55 register. At the beginning of the boot sequence, the on-chip Bootloader sets CLKOFF = 1 and CLKOUT pin is disabled (high-impedance). For more information on the ST3_55 register, see the *TMS320C55x 3.0 CPU Reference Guide* (SWPU073).

1.3.2 Clock Domains

The DSP has several clock domains that individually disable portions of the clock tree structure so as to minimize the power consumption of those portions of the device that are not being used. The following clock domains exist:

- CPU Domain
  - This domain includes the device CPU and its ports: MPORT, IPORT, DPORT, and XPORT. The FFT hardware accelerator is also included in this clock domain. The CPU clock domain is driven directly by the DSP system clock.
- Peripheral Domain
  - All the DSP peripherals are included in this domain. The internal clock of each peripheral can be disabled individually. The peripheral clocks are driven directly from the DSP system clock; although in some cases peripherals include internal dividers which are used to generate required frequencies. For example, the UART has internal dividers that are used to generate particular baud rates.
- Clock Generator Domain
  - The clock generator can be powered-down when not being used. When powered-down, the DSP system clock must be set equal to the system reference clock. The clock generator is driven by the system reference clock. The system clock generator is described in detail in Section 1.4.
- USB Domain
  - The USB peripheral has its own on-chip oscillator and PLL, both of which can be disabled when not being used.
- Real-Time Clock (RTC) Domain
  - The RTC domain is driven by the on-chip oscillator and external 32.768 kHz crystal. The clock output of the RTC domain can be used to drive the system reference clock—this is specified through the CLKSEL pin.
  - The RTC clock domain can remain active irrespective of the status of the other clock domains. The RTC can be used to generate periodic wake-up events while the rest of the DSP is idle.

1.4 System Clock Generator

1.4.1 Overview

The system clock generator (Figure 1-4) features a software-programmable PLL multiplier and several dividers. The clock generator accepts an input clock from the CLKIN pin or the output clock of the real-time clock (RTC) oscillator. The clock generator offers flexibility and convenience by way of software-configurable multiplier and dividers to modify the input signal internally. The resulting clock output, SYSCLK, is passed to the CPU, peripherals, and other modules inside the DSP.

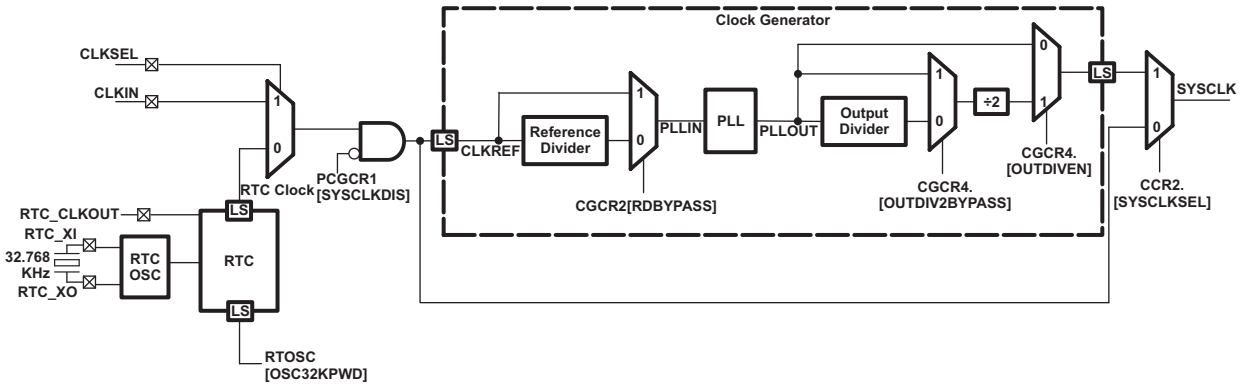
A set of registers (see Table 1-5) are provided for controlling and monitoring the activity of the clock generator. For example, you can write to the SYSCLKSEL bit in the clock configuration register 2 to toggle between the two main modes of operation:

- In the bypass mode (see Section 1.4.3.1), the entire clock generator is bypassed, and the frequency of SYSCLK is determined by CLKIN or the RTC oscillator output. Because the PLL can be disabled in this mode, this mode can be used to save power.
- In the PLL mode (see Section 1.4.3.2), the input frequency can be both multiplied and divided to produce the desired SYSCLK frequency, and the SYSCLK signal is phase-locked to the input clock signal (CLKREF).

Logic exists inside the clock generator to prevent glitches when switching between these two modes.

For debug purposes, the CLKOUT pin can be used to see different clocks within the clock generator. For details, see Section 1.4.2.3.

Figure 1-4. Clock Generator



1.4.2 Functional Description

The following sections describe the multiplier and dividers of the clock generator.

1.4.2.1 Multiplier and Dividers

The clock generator has a one multiplier and a total of three dividers, two programmable and one fixed. The PLL can be programmed to multiply the PLL input clock, PLLIN, using a x4 to x4099 multiplier rate. The reference clock divider can be programmed to divide the clock generator input clock from a /4 to /4099 divider ratio and may be bypassed. The PLLIN clock range is 32.786 KHz to 170 KHz. At the output of the PLL, the output divider can be used to divide the PLL output clock, PLLOUT, from a /4 to a /67 divider ratio and may also be bypassed. Finally, a fixed /2 divider can be used to divide either the clock generated by the output divider or the output of the PLL. The fixed divider can also be bypassed. The PLLIN clock range is 32,786 KHz to 170 KHz.

The multiplier and divider ratios are controlled through the PLL control registers. The MH and ML bits define the multiplier rate. The RDRATIO and ODRATIO bits define the divide ratio of the reference divider and programmable output divider, respectively. The RDBYPASS, OUTDIVEN, and OUTDIV2BYPASS bits are used to enable or bypass the dividers. Table 1-30 lists the formulas for the output frequency based on the setting of these bits.

Table 1-30. PLL Output Frequency Configuration

RDBYPASS	OUTDIVEN	OUTDIV2BYPASS	SYSCLK Frequency
0	0	X	$CLKREF \times \frac{(MH \ll 2 + ML + 4)}{RD + 4}$
0	1	0	$CLKREF \times \frac{(MH \ll 2 + ML + 4)}{RD + 4} \times \frac{1}{OD + 4} \times \frac{1}{2}$
0	1	1	$CLKREF \times \frac{(MH \ll 2 + ML + 4)}{RD + 4} \times \frac{1}{2}$
1	0	X	$CLKREF \times [MH \ll 2 + ML + 4]$
1	1	0	$CLKREF \times [MH \ll 2 + ML + 4] \times \frac{1}{OD + 4} \times \frac{1}{2}$
1	1	1	$CLKREF \times [MH \ll 2 + ML + 4] \times \frac{1}{2}$

1.4.2.2 Powering Down and Powering Up the System PLL

To save power, you can put the PLL in its power down mode. You can power down the PLL by setting the PLLPWRDN = 1 in the clock generator control register 1. However, before powering down the PLL, you must first place the clock generator in bypass mode.

When the PLL is powered up (PLLPWRDN = 0), the PLL will start its phase-locking sequence. You must keep the clock generator in bypass mode while the phase-locking sequence is ongoing. This process takes at least 4 ms. See Section 1.4.3.2 for more details on the lock mode of the clock generator.

1.4.2.3 CLKOUT Pin

For debug purposes, the DSP includes a CLKOUT pin which can be used to tap different clocks within the clock generator. The SRC bits of the CLKOUT control source register (CCSSR) can be used to specify the source for the CLKOUT pin (see Table 1-31).

NOTE: There is no internal logic to prevent glitches while changing the CLKOUT source.

The CLKOUT pin is enabled/disabled through the CLKOFF bit of the CPU ST3_55 register. At the beginning of the boot sequence, the on-chip Bootloader sets CLKOFF = 1 and CLKOUT pin is disabled (high-impedance). For more information on the ST3_55 register, see the *TMS320C55x 3.0 CPU Reference Guide* (SWPU073).

The drive strength of the CLKOUT pin can be controlled by the output drive strength control register (ODSCR). This feature allows for additional power savings when the CLKOUT pin does not need to drive large loads.

Table 1-31. Effect of SRC Bits on CLKOUT

SRC	CLKOUT Status
0000b	CLKOUT pin outputs System PLL output clock, PLLOUT.
0001b	CLKOUT pin is set high.
0010b	CLKOUT pin outputs System PLL output clock, PLLOUT.
0011b	CLKOUT pin is set low.
0100b	CLKOUT pin outputs System PLL output clock, PLLOUT.
0101b	CLKOUT pin is set low.
0110b	CLKOUT pin outputs System PLL output clock, PLLOUT.
0111b	CLKOUT pin outputs USB PLL output clock.
1000b	CLKOUT pin outputs System PLL output clock, PLLOUT.
1001b	CLKOUT pin outputs SAR clock.

Table 1-31. Effect of SRC Bits on CLKOUT (continued)

SRC	CLKOUT Status
1010b	CLKOUT pin outputs System PLL output clock, PLLOUT.
1011b	CLKOUT pin outputs system clock, SYSCLK (default mode).
1100b	CLKOUT pin outputs System PLL output clock, PLLOUT.
1101b	Reserved, do not use.
1110b	CLKOUT pin outputs System PLL output clock, PLLOUT.
1111b	CLKOUT pin outputs USB PLL output clock.

1.4.2.4 DSP Reset Conditions of the System Clock Generator

The following sections describe the operation of the system clock generator when the DSP is held in reset state and the DSP is removed from its reset state.

1.4.2.4.1 Clock Generator During Reset

During reset, the PLL_STANDBY bit of the clock generator control register 1 (CGCR1) is set to 1, and the PLL does not generate an output clock. Furthermore, the SYSCLKSEL bit of the clock configuration register 2 (CCR2) defaults to 0 (bypass mode), and the system clock (SYSCLK) is driven by either the CLKIN pin or the real-time clock (RTC). See Section 1.4.3.1 for more information on the bypass mode of the clock generator.

1.4.2.4.2 Clock Generator After Reset

After reset, the clock generator is bypassed altogether and the frequency of the system clock (SYSCLK) is set equal to either the CLKIN pin or the output of the real-time clock, as determined by the CLKSEL pin. The PLL is set to standby and does not generate an output clock.

NOTE: The on-chip Bootloader programs the DSP clock generator during the DSP boot sequence. This configuration takes place before the Bootloader transfers control to your application. For more information on the on-chip bootloader, see the device-specific data manual.

1.4.3 Configuration

1.4.3.1 Bypass Mode

When the system clock generator is in the bypass mode, the clock generator is not used and the system clock (SYSCLK) is driven by either the CLKIN pin or the real-time clock (RTC).

NOTE: In bypass mode, the PLL is not automatically powered down and will still consume power. For maximum power savings, the PLL should be placed in its power-down mode. See Section 1.4.2.2 for more details.

1.4.3.1.1 Entering and Exiting the Bypass Mode

To enter the bypass mode, write a 0 to the SYSCLKSEL bit in the clock configuration register 2 (CCR2). In bypass mode, the frequency of the system clock (SYSCLK) is determined by the CLK_SEL pin. If CLK_SEL = 0, SYSCLK is driven by the output of the RTC. Otherwise, SYSCLK will be driven by the CLKIN pin.

To exit the bypass mode, ensure the PLL has completed its phase-locking sequence waiting at least 4 ms and then write a 1 to the SYSCLKSEL bit. The frequency of SYSCLK is determined by the multiplier and divider ratios of the PLL and the output dividers.

If the clock generator is in the PLL mode and you want to reprogram the PLL or any of the dividers, you must set the clock generator to bypass mode before changing the PLL and divider settings.

Logic within the clock generator ensures that there are no clock glitches during the transition from PLL mode to bypass mode and vice versa.

1.4.3.1.2 Register Bits Used in the Bypass Mode

Table 1-32 describes the bits of the clock generator control registers that are used in the bypass mode. For detailed descriptions of these bits, see Section 1.4.4.

Table 1-32. Clock Generator Control Register Bits Used In Bypass Mode

Register Bit	Role in Bypass Mode
SYSCLKSEL	Allows you to switch to the PLL or bypass modes.
PLLPWRDN	Allows you to power down the PLL.

1.4.3.1.3 Setting the System Clock Frequency In Bypass Mode

The frequency of SYSCLK is determined by the CLK_SEL pin. If CLK_SEL = 0, SYSCLK is driven by the output of the RTC. Otherwise, SYSCLK will be driven by the CLKIN pin.

NOTE: The CLK_SEL pin must be statically tied high or low; it cannot be changed after the device has been powered up.

Table 1-33. Output Frequency in Bypass Mode

CLK_SEL	SYSCLK Source / Frequency
1	CLKIN / (11.2896 MHz, 12.0MHz, or 12.288 MHz)
0	RTC clock / (32.768 kHz)

1.4.3.2 PLL Mode

In PLL mode, the frequency of the input clock signal (CLKREF) can be both multiplied and divided to produce the desired output frequency, and the output clock signal is phase-locked to the input clock signal.

1.4.3.2.1 Entering and Exiting the PLL Mode

To enter the PLL mode, program the PLL to the desired frequency. After waiting 4msec for the PLL to lock, the frequency of SYSCLK will be set equal to the frequency of the clock generated by the combination of the PLL and the output dividers. You must always ensure the PLL has completed its phase-locking sequence before switching to PLL mode. Once the PLL has locked, write a 1 to the SYSCLKSEL bit in the clock configuration register 2 (CCR2) to set the system clock to the output of the PLL. After 4 ms, the frequency of SYSCLK will be set equal to the frequency of the clock generated by the combination of the PLL and the output dividers. You must always ensure the PLL has completed its phase-locking sequence before switching to PLL mode.

If the clock generator is in the PLL mode and you want to reprogram the PLL, you must set the clock generator to bypass mode before changing the PLL settings. After waiting 4ms, the PLL has completed its phase-locking sequence and you can place the clock generator back in PLL mode.

To exit the PLL mode (enter the bypass mode), write a 0 to the SYSCLKSEL bit. The frequency of the system clock (SYSCLK) will be immediately set equal to the frequency of either CLKIN or the RTC oscillator clock.

Logic within the DSP ensures that there are no clock glitches during the transition from bypass mode to PLL mode and vice versa.

1.4.3.2.2 Register Bits Used in the PLL Mode

Table 1-34 describes the bits of the clock generator control registers that are used in the PLL mode. For detailed descriptions of these bits, see Section 1.4.4.

Table 1-34. Clock Generator Control Register Bits Used In PLL Mode

Register Bit	Role in Bypass Mode
SYSCLKSEL	Allows you to switch to the PLL or bypass modes.
RDBYPASS	Determines whether reference divider should be bypassed or used.
RDRATIO	Specifies the divider ratio of the reference divider.
MH, ML	Specify the multiplier value for the PLL.
OUTDIVEN	Determines whether the output divider and the fixed /2 divider are bypassed.
OUTDIV2BYPASS	Determines whether the output divider is bypassed. The fixed /2 divider is used regardless of the setting of this bit.
ODRATIO	Specifies the divider ratio of the output divider.

1.4.3.2.3 Frequency Ranges for Internal Clocks

There are specific minimum and maximum frequencies for all the internal clocks. Table 1-35 lists the minimum and maximum frequencies for the internal clocks for the DSP.

NOTE: For actual maximum operating frequencies, see the device-specific data sheet.

Table 1-35. Frequency Ranges for Internal Clock

Clock Signal Name	CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		UNIT
	MIN	MAX	MIN	MAX	
CLKIN[1]		11.2896 12 12.288		11.2896 12 12.288	MHz
RTC Clock		32.768		32.768	KHz
PLLIN	32.768	170	32.768	170	KHz
PLLOUT	60	120	60	120	MHz
SYSCLK	0.032768	60 or 75	0.032768	100 or 120	MHz
PLL_LOCKTIME	4		4		ms

(1) These CLKIN values are used when the CLK_SEL pin = 1.

1.4.3.2.4 Setting the Output Frequency for the PLL Mode

The clock generator output frequency is multiplied and divided according to the settings programmed in the clock generator control registers. The output frequency depends on several factors, including the use of the reference divider and the output dividers (see Figure 1-4). These dividers are controlled through the RDBYPASS, OUTDIVEN, and OUTDIV2BYPASS bits. Based on the setting of these bits, you can calculate the frequency of the output clock using the formulas listed in Table 1-30.

Follow these steps to determine the values for the different dividers and multipliers of the system clock generator:

1. With the desired clock frequency in mind, choose a PLLOUT frequency that falls within the range listed in Table 1-35. Keep in mind that you can use the programmable and fixed output dividers to divide the output frequency of the PLL.
2. Determine a multiplier value that generates the PLLOUT frequency from step 1 and also meets the CLKREF requirements listed in Table 1-35. If the DSP is being clocked by the RTC oscillator output, CLKREF will be 32.768 kHz.
3. Using the multiplier, figure out the values for MH and ML (PLL multiplier = 4 x MH + ML + 4).
4. Determine the divider ratio for the reference divider that will generate the CLKREF frequency from step 2. If the DSP is being clocked by the RTC oscillator output, the reference divider can be bypassed (set RDBYPASS = 1); CLKREF will be 32.768 kHz.

Table 1-36 shows programming examples for different PLL mode frequencies.

Table 1-36. Examples of Selecting a PLL Mode Frequency

RDBYPASS	OUTDIVEN	OUTDIV2BYPASS	MH	ML	RDRATIO	ODRATIO	PLL Output Frequency
1	1	0	2EDh	0	X	0	32.768 kHz x (2EDh << 2 + 0 + 4) / (0 + 4) /2 =12.288 MHz
1	1	1	262h	0	X	X	32.768 kHz x (262h << 2 + 0 + 4) / 2 = 40.04 MHz
1	0	X	1C8h	3	X	0	32.768 kHz x (1C8h << 2 + 2 + 4) = 59.998 MHz
1	0	X	23Bh	1	X	0	32.768 kHz x (23Bh << 2 + 1 + 4) = 75.01 MHz
1	0	X	2FAh	0	X	0	32.768 kHz x (2FAh << 2 + 0 + 4) = 100.01 MHz

1.4.3.2.5 Lock Time

As previously discussed, you must place the clock generator in bypass mode before changing the PLL settings. The time it takes the PLL to complete its phase-locking sequence is referred to as the lock time. The PLL has a lock time of 4 ms.

1.4.3.2.6 Software Steps To Modify Multiplier and Divider Ratios

You can follow the steps below to program the PLL of the DSP clock generator. The recommendation is to stop all peripheral operation before changing the PLL frequency, with the exception of the device CPU and USB. The device CPU must be operational to program the PLL controller. The USB operates off of the clock from its own PLL.

1. Make sure the clock generator is in bypass mode by setting SYSCLKSEL = 0.
2. Set CLR_CNTL = 0 in CGCR1.
3. Program RDRATIO, ML, and RDBYPASS in CGCR2 according to your required settings.
4. Program ODRATIO, OUTDIV2BYPASS, and OUTDIVEN in CGCR4 according to your required settings.
5. Write 0806h to the INIT field of CGCR3.
6. Set PLL_PWRDN = 0, PLL_STANDBY = 0, CLR_CNTL = 1 and program MH in CGCR1 according to your required settings.
7. Wait for the PLL to complete its phase-locking sequence.
8. Place the clock generator in its PLL mode by setting SYSCLKSEL = 1.

1.4.4 Clock Generator Registers

Table 1-37 lists the registers associated with the clock generator of the DSP. The clock generator registers can be accessed by the CPU at the 16-bit addresses specified in Table 1-37. Note that the CPU accesses all peripheral registers through its I/O space. All other register addresses not listed in Table 1-37 should be considered as reserved locations and the register contents should not be modified.

Table 1-37. Clock Generator Registers

CPU Word Address	Acronym	Register Description	Section
1C20h	CGCR1	Clock Generator Control Register 1	Section 1.4.4.1
1C21h	CGCR2	Clock Generator Control Register 2	Section 1.4.4.2
1C22h	CGCR3	Clock Generator Control Register 3	Section 1.4.4.3
1C23h	CGCR4	Clock Generator Control Register 4	Section 1.4.4.4
1C24h	CCSSR	CLKOUT Control Source Select Register	Section 1.4.4.5
1C1Eh	CCR1	Clock Configuration Register 1	Section 1.4.4.6
1C1Fh	CCR2	Clock Configuration Register 2	Section 1.4.4.7

1.4.4.1 Clock Generator Control Register 1 (CGCR1) [1C20h]

The clock generator control register 1 (CGCR1) is shown in Figure 1-5 and described in Table 1-38.

Figure 1-5. Clock Generator Control Register 1 (CGCR1) [1C20h]

15	14	13	12	11	10	9	8
CLR_CNTL	Reserved	PLL_STANDBY	PLL_PWRDN	Reserved		MH	
R/W-0	R-0	R/W-0	R/W-1	R-0		R/W-0	

7	6	5	4	3	2	1	0
MH							
R/W-0							

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 1-38. Clock Generator Control Register 1 (CGCR1) Field Descriptions

Bit	Field	Value	Description
15	CLR_CNTL		Clear control bit. This bit is used to clear digital flip flops within the clock generator. This bit must be cleared to 0 while changing the PLL settings.
		0	Digital flip-flops cleared.
		1	Digital flip-flops not cleared (normal operation).
14	Reserved	0	Reserved.
13	PLL_STANDBY		PLL standby bit. This bit is used to place the PLL in standby mode. This bit is used for test purposes only and must always be cleared to 0.
		0	PLL is active (normal operation).
		1	PLL is in standby mode.
12	PLL_PWRDN		PLL power down bit. This bit is used to power down the PLL when it is not being used.
		0	PLL is powered up.
		1	PLL is powered down.
11-10	Reserved	0	Reserved.
9-0	MH	0-3FFh	PLL multiplier value bits. These bits along with the ML bits in CGCR2 define the PLL multiplier value. Multiplier value = MH x 4 + ML + 4. For example, MH = 23Bh and ML = 1h means multiply by 2289 (8F1h).

1.4.4.2 Clock Generator Control Register 2 (CGCR2) [1C21h]

The clock generator control register 2 (CGCR2) is shown in Figure 1-6 and described in Table 1-39.

Figure 1-6. Clock Generator Control Register 2 (CGCR2) [1C21h]

15	14	13 12	11 0
RDBYPASS	Reserved	ML	RDRATIO
R/W-0	R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 1-39. Clock Generator Control Register 2 (CGCR2) Field Descriptions

Bit	Field	Value	Description
15	RDBYPASS		Reference divider bypass bit. When this bit is set to 1 the reference divider in the DSP clock generator is bypassed. When this bit is set to 0, the reference clock to the DSP clock generator is divided by the reference divider. The RD bits specify the divider value.
		0	Use the reference divider.
		1	Bypass the reference divider.
14	Reserved	0	Reserved.
13-12	ML	0-3h	PLL multiplier value bits. These bits along with the MH bits in CGCR1 define the PLL multiplier value. Multiplier value = MH x 4 + ML + 4. For example, MH = 23Bh and ML = 1h means multiply by 2289 (8F1h).
11-0	RDRATIO	0-FFFh	Divider ratio bits for the reference divider. Divider value = RD_DIV + 4. For example, setting RD_DIV = 0 means divide by 4.

1.4.4.3 Clock Generator Control Register 3 (CGCR3) [1C22h]

The clock generator control register 3 (CGCR3) is shown in Figure 1-7 and described in Table 1-40.

Figure 1-7. Clock Generator Control Register 3 (CGCR3) [1C22h]

15 4	3	2 0
INIT	Lock Status Monitor	INIT
R/W-0x080	R/W-0	R/W-0x6

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 1-40. Clock Generator Control Register 3 (CGCR3) Field Descriptions

Bit	Field	Value	Description
15-4	INIT	0-FFFFh	Initialization bits for DSP clock generator. These bits must be initialized with 0x806 during PLL configuration.
3	Lock Status Monitor	0	64 PLL clock cycles have not passed since PLL powerup or reset
		1	64 PLL clock cycles have passed since PLL powerup or reset
2-0	INIT		

1.4.4.4 Clock Generator Control Register 4 (CGCR4) [1C23h]

The clock generator control register 4 (CGCR4) is shown in Figure 1-8 and described in Table 1-41.

Figure 1-8. Clock Generator Control Register 4 (CGCR4) [1C23h]

15	10	9	8	7	6	5	0
Reserved		OUTDIVEN	OUTDIV2BYPASS	Reserved		ODRATIO	
R-0		R/W-0	R/W-0	R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 1-41. Clock Generator Control Register 4 (CGCR4) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9	OUTDIVEN		Output divider and fixed /2 divider enable bit. This bit determines whether the output divider and the fixed /2 divider are enabled or bypassed.
		0	The output divider and the fixed /2 divider are bypassed.
		1	The output divider and the fixed /2 divider are enabled.
8	OUTDIV2BYPASS		Output divider bypass bit. This bit determines whether the output divider is bypassed. The fixed /2 divider is used regardless of the setting of this bit.
		0	The output divider is bypassed.
		1	The output divider is enabled.
7-6	Reserved	0	Reserved.
5-0	ODRATIO	0-3Fh	Divider ratio bits for the output divider.
			Divider value = ODRATIO + 4.
			For example, setting ODRATIO = 2 means divide by 6. Note: The divider output is further divided by the fixed /2 divider.

1.4.4.5 CLKOUT Control Source Select Register (CCSSR) [1C24h]

The CLKOUT pin is enabled/disabled through the CLKOFF bit of the CPU ST3_55 register. At the beginning of the boot sequence, the on-chip Bootloader sets CLKOFF = 1 and CLKOUT pin is disabled (high-impedance). For more information on the ST3_55 register, see the *TMS320C55x 3.0 CPU Reference Guide* (SWPU073).

The CLKOUT control source select register (CCSSR) is shown in Figure 1-9 and described in Table 1-42.

Figure 1-9. CLKOUT Control Source Select Register (CCSSR) [1C24h]

15	4	3	0
Reserved		SRC	
R-0		R/W-Bh	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 1-42. CLKOUT Control Source Select Register (CCSSR) Field Descriptions

Bit	Field	Value	Description
15-4	Reserved	0	Reserved.
3-0	SRC		CLKOUT source bits. These bits specify the source clock for the CLKOUT pin.
		0	CLKOUT pin outputs System PLL output clock, PLLOUT.
		1h	CLKOUT pin is set high.
		2h	CLKOUT pin outputs System PLL output clock, PLLOUT.
		3h	CLKOUT pin is set low.
		4h	CLKOUT pin outputs System PLL output clock, PLLOUT.
		5h	CLKOUT pin is set low.
		6h	CLKOUT pin outputs System PLL output clock, PLLOUT.
		7h	CLKOUT pin outputs USB PLL output clock.
		8h	CLKOUT pin outputs System PLL output clock, PLLOUT.
		9h	CLKOUT pin outputs SAR clock.
		Ah	CLKOUT pin outputs System PLL output clock, PLLOUT.
		Bh	CLKOUT pin outputs system clock, SYSCLK (default mode).
		Ch	CLKOUT pin outputs System PLL output clock, PLLOUT.
		Dh	Reserved, do not use.
		Eh	CLKOUT pin outputs System PLL output clock, PLLOUT.
		Fh	CLKOUT pin outputs USB PLL output clock.

1.4.4.6 Clock Configuration Register 1 (CCR1) [1C1Eh]

The clock configuration register 1 (CCR1) is shown in Figure 1-10 and described in Table 1-43.

Figure 1-10. Clock Configuration Register 1 (CCR1) [1C1Eh]

15	0
Reserved	
R-0	

LEGEND: R = Read only; -*n* = value after reset

Table 1-43. Clock Configuration Register 1 (CCR1) Field Descriptions

Bit	Field	Value	Description
15-0	Reserved	0	Reserved. This bit must be kept as 0 during writes to this register.

1.4.4.7 Clock Configuration Register 2 (CCR2) [1C1Fh]

The clock configuration register 2 (CCR2) is shown in Figure 1-11 and described in Table 1-44.

Figure 1-11. Clock Configuration Register 2 (CCR2) [1C1Fh]

15	6	5	4	3	2	1	0
Reserved		SYSCLKSRC		TIMER0CLKSEL	CLKSELSTAT	Reserved	SYSCLKSEL
R-0		R-0		R-0	R-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 1-44. Clock Configuration Register 2 (CCR2) Field Descriptions

Bit	Field	Value	Description
15-6	Reserved	0	Reserved.
5-4	SYSCLKSRC		System clock source bits. These read-only bits reflect the source for the system clock.
		0	The system clock generator is in bypass mode; SYSCLK is driven by the RTC oscillator output.
		1h	The system clock generator is in PLL mode; the RTC oscillator output provides the input clock.
		2h	The system clock generator is in bypass mode; SYSCLK is driven by CLKIN.
		3h	The system clock generator is in PLL mode; the CLKIN pin provides the input clock.
3	TIMER0CLKSEL		Timer 0 clock source select bit. This bit specifies the input clock to Timer 0.
		0	Timer 0 uses SYSCLK as input clock.
		1	Timer 0 uses PLL output clock (PLLOUT) as input clock.
2	CLKSELSTAT		CLK_SEL pin status bit. This reflects the state of the CLK_SEL pin.
		0	CLK_SEL pin is low (RTC input clock selected).
		1	CLK_SEL pin is high (CLKIN input clock selected).
1	Reserved	0	Reserved.
0	SYSCLKSEL		System clock source select bit. This bit is used to select between the two main clocking modes for the DSP: bypass and PLL mode. In bypass mode, the DSP clock generator is bypassed and the system clock is set to either CLKIN or the RTC output (as determined by the CLKSEL pin). In PLL mode, the system clock is set to the output of the DSP clock generator. Logic in the system clock generator prevents switching from bypass mode to PLL mode if the PLL is powered down.
		0	Bypass mode is selected.
		1	PLL mode is selected.

1.5 Power Management

1.5.1 Overview

In many applications there may be specific requirements to minimize power consumption for both power supply (and battery) and thermal considerations. There are two components to power consumption: active power and leakage power. Active power is the power consumed to perform work and scales roughly with clock frequency and the amount of computations being performed. Active power can be reduced by controlling the clocks in such a way as to either operate at a clock setting just high enough to complete the required operation in the required time-line or to run at a clock setting until the work is complete and then drastically cut the clocks (that is, to bypass mode or clock gate) until additional work must be performed.

Leakage power is due to static current leakage and occurs regardless of the clock rate. Leakage, or standby power, is unavoidable while power is applied and scales roughly with the operating junction temperatures. Leakage power can only be avoided by removing power completely from a device or subsystem.

The DSP has several means of managing the power consumption, as detailed in the following sections. There is extensive use of automatic clock gating in the design as well as software-controlled module clock gating to not only reduce the clock tree power, but to also reduce module power by basically freezing its state while not operating. Clock management enables you to slow the clocks down on the chip in order to reduce switching power. Independent power domains allow you to shut down parts of the DSP to reduce static power consumption. When not being used, the internal memory of the DSP can also be placed in a low leakage power mode while preserving the memory contents. The operating voltage and drive strength of the I/O pins can also be reduced to decrease I/O power consumption.

Table 1-45 summarizes all of the power management features included in the DSP.

Table 1-45. Power Management Features

Power Management Features	Description
Clock Management	
PLL power-down	The system PLL can be powered-down when not in use to reduce switching power.
Peripheral clock idle	Peripheral clocks can be idled to reduce switching power.
Dynamic Power Management	
Core Voltage Scaling	The DSP LDO and DSP logic support two voltage ranges to allow voltage adjustments on-the-fly, increasing voltage during peak processing power demand and decreasing during low demand.
Static Power Management	
DARAM/SARAM low power modes	The internal memory of the DSP can be placed in a low leakage power mode while preserving memory contents.
Independent power domains	Independent power domains allow you to shut down parts of the DSP to reduce static power consumption.
I/O Management	
I/O voltage selection	The operating voltage and/or slew rate of the I/O pins can be reduced (at the expense of performance) to decrease I/O power consumption.
USB power-down	The USB peripheral can be powered-down when not being used.

1.5.2 Architectural Blocks for Power Management

1.5.2.1 Clock Domains

A clock domain is a group of modules fed with the same gated clock signal (see Figure 1-12). By gating the clock to each domain, it is possible to cut a clock to a group of inactive modules to lower their active power consumption. Thus, a clock domain allows control of dynamic power consumption by the device.

Figure 1-12. Generic Clock Domain

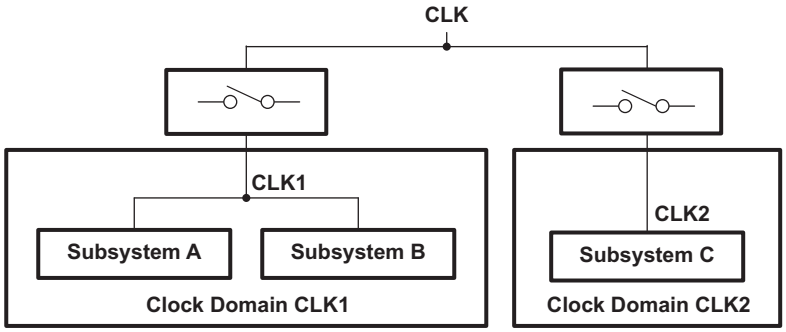


Table 1-46. States of a Clock Domain

State	Description
Active	The domain clock is running.
Idle	The domain clock is stopped or gated.

1.5.2.2 Power Domain

To minimize power consumption by the device, the modules are placed in power domains. A power domain is a section of the device with independent and dedicated power rails (see Figure 1-13). A power domain can be turned on/off without affecting the other parts of the device.

Figure 1-13. Generic Power Domain

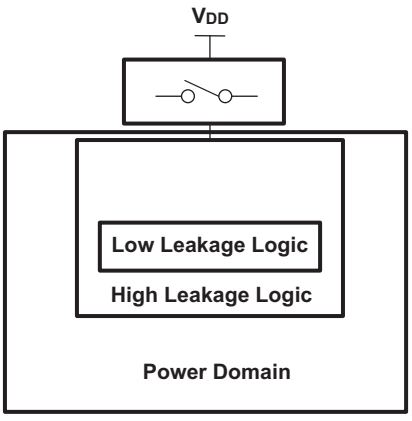


Table 1-47 lists the possible states of the power domain with the corresponding status of the V_{DD} switch.

Table 1-47. Power Domain States

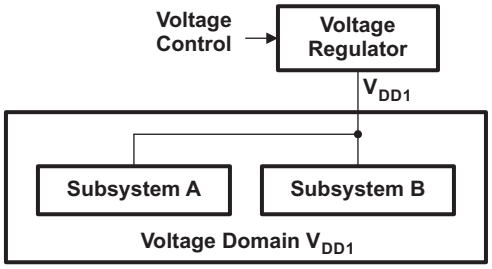
State	V_{DD} Switch
Active	Close
Off	Open

1.5.2.3 Voltage Domain

A voltage domain is a group of modules supplied by the same voltage regulator (embedded or external). The power consumption of this group can be controlled by regulating its voltage independently.

Figure 1-14 shows the voltage domain.

Figure 1-14. Generic Voltage Domain



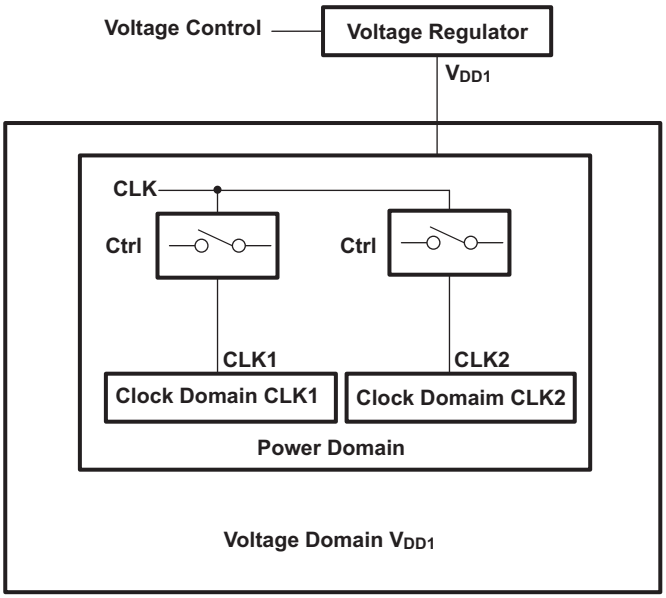
By partitioning the device into independent voltage domains, it is possible to assign different operating voltages to the different modules. The independent voltage control allows voltage scaling of device subsections to ensure that each module operates at the optimized operating voltage level based on the application performance requirements. When all modules within a voltage domain are inactive, the domain voltage can be lowered or shut off completely to reduce power consumption and then be switched back to normal operating voltage when a wake-up event is received.

1.5.3 Device Power-Management Architecture

The device architecture integrates the power-management architectural blocks for power-management support. It is composed of scalable/switchable voltage domains (their voltage can be controlled) and switchable power domains. Figure 1-15 shows the general hierarchical architecture scheme of the voltage, power, and clock domains.

A clock domain is a subset of a power domain. This avoids unnecessary dependencies between power domains caused by clocks covering multiple power domains. Each clock within a power domain, with an independent gating control, is a separate clock domain.

Figure 1-15. Voltage, Power, and Clock Domain Hierarchical Architecture



Each power domain is supplied by one or more voltage domains that can be scaled down or switched off to save power. On-chip internal memory and logic can be put in standby or retention mode independently. In these states, memory is not operational, but the content is retained with minimized leakage. This feature allows power consumption to be reduced when the device is in sleep mode while maintaining memory contents for fast context restore. The memory standby feature is software-controllable.

1.5.4 Power Domains

The DSP has separate power domains which provide power to different portions of the device. The separate power domains allow the user to select the optimal voltage to achieve the lowest power consumption at the best possible performance. Note that several power domains have similar voltage requirements and, therefore, could be grouped under a single voltage domain.

Table 1-48. DSP Power Domains

Power Domains	Description
Real-Time Clock Power Domain (CV_{DDRTC})	This domain powers the real-time clock digital circuits and oscillator pins (RTC_XI, RTC_XO). Supply voltage can be 1.05-V thru 1.3-V. This domain is not regulated internally, external regulation must be provided. This domain must be powered before any of the other power domains.
Core Power Domain (CV_{DD})	This domain powers the digital circuits that include the C55x CPU, on-chip memory, and peripherals. Supply voltage is either 1.05 V or 1.3 V. This domain is not regulated internally, external regulation must be provided. This domain must be powered before any of the other I/O domains are powered: DV_{DDIO}, DV_{DDEMIF}, DV_{DDRTC}, USB_V_{DDOSC}, USB_V_{DDA3P3}, and USB_V_{DDPLL}.
Digital I/O Power Domain 1 (DV_{DDEMIF})	This domain powers all I/Os, except the EMIF I/O pin, USB I/O pins, USB oscillator I/O pins and the real-time clock power domain I/O pins. Supply voltage can be 1.8, 2.5, 2.8, or 3.3 V. This domain is not regulated internally, external regulation must be provided. This domain must be powered after the core domains are powered: ANA_LDOI, CV_{DDRTC}, CV_{DD}, USB_V_{DD1P3}, USB_V_{DDA1P3}, V_{DDA_ANA}, and V_{DDA_PLL}.
Digital I/O Power Domain 2 (DV_{DDIO})	This domain powers all EMIF I/O pins only. Supply voltage can be 1.8, 2.5, 2.8, or 3.3 V. This domain is not regulated internally, external regulation must be provided. This domain must be powered after the core domains are powered: ANA_LDOI, CV_{DDRTC}, CV_{DD}, USB_V_{DD1P3}, USB_V_{DDA1P3}, V_{DDA_ANA}, and V_{DDA_PLL}.
RTC I/O Power Domain (DV_{DDRTC})	This domain powers the WAKEUP and RTC_CLKOUT pins. Supply voltage can be 1.8, 2.5, 2.8, or 3.3 V. This domain is not regulated internally, external regulation must be provided.
PLL Power Domain (V_{DDA_PLL})	This domain powers the system clock generator PLL. Supply voltage is 1.3 V. This domain can be powered from the on-chip analog LDO.
Analog Power Domain (V_{DDA_ANA})	This domain powers the power management circuits and the 10-bit SAR. Supply voltage is 1.3 V. This domain can be powered from the on-chip analog LDO.
USB Analog Power Domain (USB_V_{DDA1P3})	This domain powers the USB analog PHY. Supply voltage is 1.3 V. This domain is not regulated internally, external regulation must be provided.
USB Digital Power Domain (USB_V_{DD1P3})	This domain powers the USB digital module. Supply voltage is 1.3 V. This domain is not regulated internally, external regulation must be provided.
USB Oscillator Power Domain	This domain powers the USB oscillator. Supply voltage is 3.3 V. This domain is not regulated internally and external regulation must be provided.

Table 1-48. DSP Power Domains (continued)

Power Domains	Description
USB Transceiver Power Domain	This domain powers the USB transceiver. Supply voltage is 3.3 V. This domain is not regulated internally and external regulation must be provided.
USB PLL Power Domain (USB_V_{DDPLL})	This domain powers the USB PLL. Supply voltage is 3.3 V. This domain is not regulated internally and external regulation must be provided.

1.5.5 Clock Management

As mentioned in Section 1.3.2, there are several clock domains within the DSP. The DSP supports a clock gating feature which allows software to disable clocks to entire clock domains or modules within that domain in order to reduce the domain's active power consumption to zero.

NOTE: Stopping clocks to a domain or a module within that domain only affects active power consumption; it does not affect leakage power consumption.

NOTE: The on-chip Bootloader idles all peripherals and CPU ports at startup. It enables some peripherals as it uses them. Your application code should check the idle configuration of peripherals and CPU ports before using them to be sure these are not idle.

1.5.5.1 CPU Domain Clock Gating

Two registers provide the means for you to individually configure and monitor the clock gating modes of the CPU domain: the idle configuration register (ICR) and the idle status register (ISTR).

ICR lets you configure how the CPU domain will respond the next time the idle instruction is executed. When you execute the idle instruction, the content of ICR is copied to ISTR. Then the ISTR values are propagated to the different portions of the CPU domain.

1.5.5.1.1 Idle Configuration Register (ICR) [0001h] and IDLE Status Register (ISTR) [0002h]

describes the read/write bits of ICR, and Table 1-50 describes the read-only bits of ISTR.

NOTE: To prevent an emulation lock up, idle requests to these domains may be overridden or ignored when an emulator is connected to the JTAG port of the DSP.

Figure 1-16. Idle Configuration Register (ICR) [0001h]

15							10	9	8
Reserved								HWAI	IPORTI
R/W-0								R/W-0	R/W-0
7	6	5	4				1		0
MPORTI	XPORTI	DPORTI	IDLECFG						CPUI
R/W-0	R/W-0	R/W-0	R/W-0						R/W-0

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 1-49. Idle Configuration Register (ICR) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9	HWAI		FFT hardware accelerator idle control bit.
		0	Hardware accelerator remains active after execution of an IDLE instruction.
		1	Hardware accelerator is disabled after execution of an IDLE instruction.
8	IPORTI		Instruction port idle control bit. The IPORT is used for all external memory instruction accesses.
		0	IPORT remains active after execution of an IDLE instruction.
		1	IPORT is disabled after execution of an IDLE instruction.
7	MPORTI		Memory port idle control bit. The memory port is used for all DMA and USB transactions into on-chip memory.
		0	MPORT remains active after execution of an IDLE instruction.
		1	MPORT is disabled after execution of an IDLE instruction.
6	XPORTI		I/O port idle control bit. The XPORT is used for all CPU I/O memory transactions.
		0	XPORT remains active after execution of an IDLE instruction.
		1	XPORT is disabled after execution of an IDLE instruction.
5	DPORTI		Data port idle control bit. The data port is used for all CPU external memory data accesses.
		0	DPORT remains active after execution of an IDLE instruction.
		1	DPORT is disabled after execution of an IDLE instruction.
4-1	IDLECFG	0-Fh	Idle configuration bits. You must always set bit 1, 2 and 3 to 1 and bit 4 to 0 before executing the idle instruction.
0	CPUI		CPU idle control bit.
		0	CPU remains active after execution of an IDLE instruction.
		1	CPU is disabled after execution of an IDLE instruction.

Figure 1-17. Idle Status Register (ISTR) [0002h]

15				10	9	8
Reserved					HWAIS	IPORTIS
R-0					R-0	R-0
7	6	5	4	1	0	
MPORTIS	XPORTIS	DPORTIS	Reserved		CPUIS	
R-0	R-0	R-0	R-0		R-0	

LEGEND: R = Read only; -*n* = value after reset

Table 1-50. Idle Status Register (ISTR) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9	HWAIS		FFT hardware accelerator idle status bit.
		0	Hardware accelerator is active.
		1	Hardware accelerator is disabled.
8	IPORTIS		Instruction port idle status bit. The IPORT is used for all external memory instruction accesses.
		0	IPORT is active.
		1	IPORT is disabled.
7	MPORTIS		Memory port idle status bit. The memory port is used for all DMA and USB transactions into on-chip memory.
		0	MPORT is active.
		1	MPORT is disabled.
6	XPORTIS		I/O port idle status bit. The XPORT is used for all CPU I/O memory transactions.
		0	XPORT is active.
		1	XPORT is disabled.

Table 1-50. Idle Status Register (ISTR) Field Descriptions (continued)

Bit	Field	Value	Description
5	DPORTIS		Data port idle status bit. The data port is used for all CPU external memory data accesses.
		0	DPORT is active.
		1	DPORT is disabled.
4-1	Reserved	0	Reserved.
0	CPUIS		CPU idle status bit.
		0	CPU is active.
		1	CPU is disabled.

1.5.5.1.2 Valid Idle Configurations

Not all of the values that you can write to the idle configuration register (ICR) provide valid idle configurations. The valid configurations are limited by dependencies within the system. For example, the XPORT cannot be idled unless the CPU is also requested to go to idle and the IDLECFG bit 1, 2 and 3 of ICR are set 1, bit 4 of ICR is set to 0. Before any part of the CPU domain is idled, you must observe the requirements outlined in Table 1-51.

A bus error will be generated (BERR = 1 in IFR1) if you execute the idle instruction under any of the following conditions and the idle command will not take effect:

1. If you fail to set IDLECFG=1111 while setting any of these bits: DPORTI, XPORTI, IPORTI or MPORTI.
2. If you set DPORTI, XPORTI, or IPORTI without also setting CPUI.

Table 1-51. CPU Clock Domain Idle Requirements

CPU Clock Domain Module/Port	Requirements Before Going to Idle
CPU	No requirements.
FFT Hardware Accelerator	No requirements.
MPORT	DMA controllers, LCD, and USB must be idled. IDLECFG bit 1, 2 and 3 of ICR are set to 1 and bit 4 of ICR is set to 0.
XPORT DPORT IPORT	CPU must be idled. IDLECFG bit 1, 2 and 3 of ICR are set to 1 and bit 4 of ICR is set to 0.

1.5.5.1.3 Clock Configuration Process

The clock configuration indicates which portions of the CPU clock domain will be idle, and which will be active. The basic steps to the clock configuration process are:

1. Wait for completion of all DMA transfers. You can poll the DMA transfer status and disable DMA transfers through the DMA registers.
2. Clear all interrupts by writing ones to the CPU interrupt flag registers (IFR0 and IFR1).
3. If you intend to idle the CPU, enable the appropriate wake-up interrupt in the CPU interrupt enable registers (IER0 and IER1).
4. Define a new clock configuration for the CPU domain by writing to the bits in the idle configuration register (ICR). Make sure that you use a valid idle configuration (see Section 1.5.5.1.2).
5. Flush the CPU pipeline by executing 6 NOP instructions.
6. Apply the new idle configuration by executing the IDLE instruction. The content of ICR is copied to the idle status register (ISTR). The bits of ISTR are then propagated through the CPU domain system to enable or disable the specified clocks.

The IDLE instruction cannot be executed in parallel with another instruction.

1.5.5.2 Peripheral Domain Clock Gating

The peripheral clock gating feature allows software to disable clocks to the DSP peripherals, in order to reduce the peripheral's dynamic power consumption to zero. Aside from the analog logic, the DSP is designed in static CMOS; thus, when a peripheral clock stops, the peripheral's state is preserved. When the clock is restarted the peripheral resumes operating from the stopping point.

NOTE: Stopping clocks to a peripheral only affects active power consumption; it does not affect leakage power consumption.

If a peripheral's clock(s) is stopped while being accessed, the access may not occur, and could potentially lock-up the device. User must ensure that all of the transactions to the peripheral are finished prior to stopping the clocks.

The procedure to turn peripheral clocks on/off is described in Section 1.5.5.2.3.

Some peripherals provide additional power saving features by clock gating components within its peripheral boundary. See the peripheral-specific user's guide for more details on these additional power saving features.

1.5.5.2.1 Peripheral Clock Gating Configuration Registers (PCGCR1 and PCGCR2) [1C02 - 1C03h]

The peripheral clock gating configuration registers (PCGRC1 and PCGCR2) are used to disable the clocks of the DSP peripherals. In contrast to the idle control register (ICR), these bits take effect within 6 SYSCLK cycles and do not require an idle instruction.

The Peripheral Clock Gating Configuration Register 1 (PCGCR1) is shown in Figure 1-18 and described in Table 1-52.

Figure 1-18. Peripheral Clock Gating Configuration Register 1 (PCGCR1) [1C02h]

15	14	13	12	11	10	9	8
SYSCLKDIS	I2S2CG	TMR2CG	TMR1CG	EMIFCG	TMR0CG	I2S1CG	I2S0CG
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
MMCSD1CG	I2CCG	Reserved	MMCSD0CG	DMA0CG	UARTCG	SPICG	I2S3CG
R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 1-52. Peripheral Clock Gating Configuration Register 1 (PCGCR1) Field Descriptions

Bit	Field	Value	Description
15	SYSCLKDIS		System clock disable bit. This bit can be used to turn off the system clock. Setting the WAKEUP pin high enables the system clock. Since the WAKEUP pin is used to re-enable the system clock, the WAKEUP pin must be low to disable the system clock.
			Note: Disabling the system clock disables the clock to most parts of the DSP, including the CPU.
		0	System clock is active.
		1	System clock is disabled.
14	I2S2CG		I2S2 clock gate control bit. This bit is used to enable and disable the I2S2 peripheral clock.
		0	Peripheral clock is active.
		1	Peripheral clock is disabled.
13	TMR2CG		Timer 2 clock gate control bit. This bit is used to enable and disable the Timer 2 peripheral clock.
		0	Peripheral clock is active.
		1	Peripheral clock is disabled.
12	TMR1CG		Timer 1 clock gate control bit. This bit is used to enable and disable the Timer 1 peripheral clock.
		0	Peripheral clock is active.
		1	Peripheral clock is disabled.
11	EMIFCG		EMIF clock gate control bit. This bit is used to enable and disable the EMIF peripheral clock. NOTE: You must request permission before stopping the EMIF clock through the peripheral clock stop request/acknowledge register (CLKSTOP).
		0	Peripheral clock is active.
		1	Peripheral clock is disabled.
10	TMR0CG		Timer 0 clock gate control bit. This bit is used to enable and disable the Timer 0 peripheral clock.
		0	Peripheral clock is active.
		1	Peripheral clock is disabled.
9	I2S1CG		I2S1 clock gate control bit. This bit is used to enable and disable the I2S1 peripheral clock.
		0	Peripheral clock is active.
		1	Peripheral clock is disabled.
8	I2S0CG		I2S0 clock gate control bit. This bit is used to enable and disable the I2S0 peripheral clock.
		0	Peripheral clock is active.
		1	Peripheral clock is disabled.
7	MMCSD1CG		MMC/SD1 clock gate control bit. This bit is used to enable and disable the MMC/SD1 peripheral clock.
		0	Peripheral clock is active.
		1	Peripheral clock is disabled.

Table 1-52. Peripheral Clock Gating Configuration Register 1 (PCGCR1) Field Descriptions (continued)

Bit	Field	Value	Description
6	I2CCG		I2C clock gate control bit. This bit is used to enable and disable the I2C peripheral clock.
		0	Peripheral clock is active.
		1	Peripheral clock is disabled.
5	Reserved	0	Reserved, you must always write 1 to this bit.
4	MMCSD0CG		MMC/SD0 clock gate control bit. This bit is used to enable and disable the MMC/SD0 peripheral clock.
		0	Peripheral clock is active.
		1	Peripheral clock is disabled.
3	DMA0CG		DMA controller 0 clock gate control bit. This bit is used to enable and disable the peripheral clock the DMA controller 0.
		0	Peripheral clock is active.
		1	Peripheral clock is disabled.
2	UARTCG		UART clock gate control bit. This bit is used to enable and disable the UART peripheral clock. NOTE: You must request permission before stopping the UART clock through the peripheral clock stop request/acknowledge register (CLKSTOP).
		0	Peripheral clock is active.
		1	Peripheral clock is disabled.
1	SPICG		SPI clock gate control bit. This bit is used to enable and disable the SPI controller peripheral clock.
		0	Peripheral clock is active.
		1	Peripheral clock is disabled.
0	I2S3CG		I2S3 clock gate control bit. This bit is used to enable and disable the I2S3 peripheral clock.
		0	Peripheral clock is active.
		1	Peripheral clock is disabled.

The Peripheral Clock Gating Configuration Register 2 (PCGCR2) is shown in Figure 1-19 and described in Table 1-53.

Figure 1-19. Peripheral Clock Gating Configuration Register 2 (PCGCR2) [1C03h]

15							8
Reserved							
R-0							

7	6	5	4	3	2	1	0
Reserved	ANAREGCG	DMA3CG	DMA2CG	DMA1CG	USBCG	SARCG	LCDCG
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 1-53. Peripheral Clock Gating Configuration Register 2 (PCGCR2) Field Descriptions

Bit	Field	Value	Description
15-7	Reserved	0	Reserved.
6	ANAREGCG		Analog registers clock gate control bit. This bit is used to enable and disable the clock to the registers that control the analog domain of the device, i.e. registers in the 7000h-70FFh I/O space address range. NOTE: When SARCG = 0, the clocks to the analog domain registers are enabled regardless of the ANAREGCG setting.
		0	Clock is active.
		1	Clock is disabled.
5	DMA3CG		DMA controller 3 clock gate control bit. This bit is used to enable and disable the DMA controller 3 peripheral clock.
		0	Peripheral clock is active.
		1	Peripheral clock is disabled.

Table 1-53. Peripheral Clock Gating Configuration Register 2 (PCGCR2) Field Descriptions (continued)

Bit	Field	Value	Description
4	DMA2CG		DMA controller 2 clock gate control bit. This bit is used to enable and disable the DMA controller 2 peripheral clock.
		0	Peripheral clock is active.
		1	Peripheral clock is disabled.
3	DMA1CG		DMA controller 1 clock gate control bit. This bit is used to enable and disable the DMA controller 1 peripheral clock.
		0	Peripheral clock is active.
		1	Peripheral clock is disabled.
2	USBCG		USB clock gate control bit. This bit is used to enable and disable the USB controller peripheral clock. NOTE: You must request permission before stopping the USB clock through the peripheral clock stop request/acknowledge register (CLKSTOP).
		0	Peripheral clock is active.
		1	Peripheral clock is disabled.
1	SARCG		SAR clock gate control bit. This bit is used to enable and disable the SAR peripheral clock. NOTE: When SARCG = 0, the clock to the analog domain registers is enabled regardless of the ANAREGCG setting.
		0	Peripheral clock is active.
		1	Peripheral clock is disabled.
0	LCDCG		LCD controller clock gate control bit. This bit is used to enable and disable the LCD controller peripheral clock.
		0	Peripheral clock is active.
		1	Peripheral clock is disabled.

1.5.5.2.2 Peripheral Clock Stop Request/Acknowledge Register (CLKSTOP) [1C3Ah]

You must execute a handshaking procedure before stopping the clock to the EMIF, USB, and UART. This handshake procedure ensures that current bus transactions are completed before the clock is stopped. The peripheral clock stop request/acknowledge register (CLKSTOP) enables this handshaking mechanism.

To stop the clock to the EMIF, USB, or UART, set the corresponding clock stop request bit in the CLKSTOP register, then wait for the peripheral to set the corresponding clock stop acknowledge bit. Once this bit is set, you can idle the corresponding clock in the PCGCR1 and PCGCR2.

To enable the clock to the EMIF, USB, or UART, first enable the clock the peripheral through PCGCR1 or PCGCR2, then clear the corresponding clock stop request bit in the CLKSTOP register.

The peripheral clock stop request/acknowledge register (CLKSTOP) is shown in Figure 1-20 and described in Table 1-54.

Figure 1-20. Peripheral Clock Stop Request/Acknowledge Register (CLKSTOP) [1C3Ah]

15							8
Reserved							
R-0							
7	6	5	4	3	2	1	0
Reserved		URTCLKSTPACK	URTCLKSTPREQ	USBCLKSTPACK	USBCLKSTPREQ	EMFCLKSTPACK	EMFCLKSTPREQ
R-0		R-1	R/W-1	R-1	R/W-1	R-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 1-54. Peripheral Clock Stop Request/Acknowledge Register (CLKSTOP) Field Descriptions

Bit	Field	Value	Description
15-6	Reserved	0	Reserved.
5	URTCLKSTPACK		UART clock stop acknowledge bit. This bit is set to 1 when the UART has acknowledged a request for its clock to be stopped. The UART clock should not be stopped until this bit is set to 1.
		0	The request to stop the peripheral clock has not been acknowledged.
		1	The request to stop the peripheral clock has been acknowledged, the clock can be stopped.
4	URTCLKSTPREQ		UART peripheral clock stop request bit. When disabling the UART internal peripheral clock, you must set this bit to 1 to request permission to stop the clock. After the UART acknowledges the request (URTCLKSTPACK = 1) you can stop the clock through the peripheral clock gating control register 1 (PCGCR1). When enabling the UART internal clock, enable the clock through PCGCR1, then set URTCKLSTPREQ to 0.
		0	Normal operating mode.
		1	Request permission to stop the peripheral clock.
3	USBCLKSTPACK		USB clock stop acknowledge bit. This bit is set to 1 when the USB has acknowledged a request for its clock to be stopped. The USB clock should not be stopped until this bit is set to 1.
		0	The request to stop the peripheral clock has not been acknowledged.
		1	The request to stop the peripheral clock has been acknowledged, the clock can be stopped.
2	USBCLKSTPREQ		USB peripheral clock stop request bit. When disabling the USB internal peripheral clock, you must set this bit to 1 to request permission to stop the clock. After the USB acknowledges the request (USBCLKSTPACK = 1) you can stop the clock through the peripheral clock gating control register 2 (PCGCR2). When enabling the USB internal clock, enable the clock through PCGCR2, then set USBCKLSTPREQ to 0.
		0	Normal operating mode.
		1	Request permission to stop the peripheral clock.
1	EMFCLKSTPACK		EMIF clock stop acknowledge bit. This bit is set to 1 when the EMIF has acknowledged a request for its clock to be stopped. The EMIF clock should not be stopped until this bit is set to 1.
		0	The request to stop the peripheral clock has not been acknowledged.
		1	The request to stop the peripheral clock has been acknowledged, the clock can be stopped.
0	EMFCLKSTPREQ		EMIF peripheral clock stop request bit. When disabling the EMIF internal peripheral clock, you must set this bit to 1 to request permission to stop the clock. After the EMIF acknowledges the request (EMFCLKSTPACK = 1) you can stop the clock through the peripheral clock gating control register 1 (PCGCR1). When enabling the EMIF internal clock, enable the clock through PCGCR1, then set EMFCKLSTPREQ to 0.
		0	Normal operating mode.
		1	Request permission to stop the peripheral clock.

1.5.5.2.3 Clock Configuration Process

The clock configuration indicates which portions of the peripheral clock domain will be idle, and which will be active. The basic steps to the clock configuration process are:

1. Wait for completion of all DMA transfers. You can poll the DMA transfer status and disable DMA transfers through the DMA registers.
2. If idling the EMIF, USB, and UART clock, set the corresponding clock stop request bit in CLKSTOP.
3. Wait for confirmation from the module that its clock can be stopped by polling the clock stop acknowledge bits of CLKSTOP.
4. Set the clock configuration for the peripheral domain through PCGCR1 and PCGCR2. The clock configuration takes place as soon as you write to these registers; the idle instruction is not required

1.5.5.3 Clock Generator Domain Clock Gating

To save power, the system clock generator can be placed in its bypass mode and its PLL can be placed in power down mode. When the system clock generator is in the bypass mode, the clock generator is not used and the system clock (SYSCLK) is driven by either the CLKIN pin or the real-time clock (RTC). For more information entering and exiting the bypass mode of the clock generator, see Section 1.4.3.1.1.

When the clock generator is placed in its bypass mode, the PLL continues to generate a clock output. You can save additional power by powering down the PLL. Section 1.4.2.2 provides more information on powering down the PLL.

1.5.5.4 USB Domain Clock Gating

The USB clock domain is composed of core logic, a USB PHY, and an on-chip oscillator. These modules can be clock gated when not used to reduce the peripheral's active power consumption to zero.

NOTE: Stopping clocks to a peripheral only affects active power consumption; it does not affect leakage power consumption. USB leakage power consumption can be reduced to zero by not powering the USB.

1.5.5.4.1 Clock Configuration Process

The clock configuration process for the USB clock domain consists of disabling the USB peripheral clock followed by disabling the USB on-chip oscillator.

To set the clock configuration of the USB clock domain to idle follow these steps:

1. Set the USB clock stop request bit (USBCLKSTREQ) in the CLKSTOP register to request permission to shut off the USB peripheral clock.
2. Wait until the USB acknowledges the clock stop request by polling the USB clock stop acknowledge bit (USBCLKSTPACK) in the CLKSTOP register.
3. Disable the USB peripheral clock by setting USBCG = 1 in the peripheral clock gating control register 2 (PCGCR2).
4. Disable the USB oscillator by setting USBOSCDIS = 1 in the USB system control register (USBSCR).

To enable the USB clock domain, follow these steps:

1. Enable the USB oscillator by setting USBOSCDIS = 0 in USBSCR.
2. Wait for the oscillator to stabilize. For oscillator stabilization time, see the device-specific data manual.
3. Enable the USB peripheral clock by setting USBCG = 0 in the peripheral clock gating control register 2 (PCGCR2).
4. Clear the USB clock stop request bit (USBCLKSTREQ) in the CLKSTOP register.

1.5.5.4.2 USB System Control Register (USBSCR) [1C32h]

The USB system control register is used to disable the USB on-chip oscillator and to power-down the USB.

The USB System Control Register (USBSCR) is shown in Figure 1-21 and described in Table 1-55.

Figure 1-21. USB System Control Register (USBSCR) [1C32h]

15	14	13	12	11	8
USBPWDN	USBSESSEND	USBVBUSDET	USBPLLEN	Reserved	
R/W-1	R/W-0	R/W-1	R/W-0	R-0	

7	6	5	4	3	2	1	0
Reserved	USBDATPOL	Reserved		USBOSCBIASDIS	USBOSCDIS	BYTEMODE	
R-0	R/W-1	R-0		R/W-1	R/W-1	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 1-55. USB System Control Register (USBSCR) Field Descriptions

Bit	Field	Value	Description
15	USBPWDN		USB module power.
		0	USB module is powered.
		1	USB module is powered-down.
14	USBSESSEND		USB VBUS session end comparator enable.
		0	USB VBUS session end comparator is disabled.
		1	USB VBUS session end comparator is enabled.
13	USBVBUSDET		USB VBUS detect enable.
		0	USB VBUS detect comparator is disabled.
		1	USB VBUS detect comparator is enabled.
12	USBPLLEN		USB PLL enable.
		0	Normal USB operation.
		1	Override USB suspend end behavior and force release of PLL from suspend state.
11-7	Reserved	0	Reserved. Always write 0 to these bits.
6	USBDATPOL		USB data polarity bit.
		0	Reverse polarity on DP and DM signals.
		1	Normal polarity.
5-4	Reserved	0	Reserved.
3	USBOSCBIASDIS		USB internal oscillator bias resistor disable.
		0	Internal oscillator bias resistor enabled (normal operating mode).
		1	Internal oscillator bias resistor disabled.
2	USBOSCDIS		USB oscillator disable bit.
		0	USB internal oscillator enabled.
		1	USB internal oscillator disabled.
1-0	BYTEMODE		USB byte mode select bits.
		0	Word accesses by the CPU are allowed.
		1h	Byte accesses by the CPU are allowed (high byte is selected).
		2h	Byte accesses by the CPU are allowed (low byte is selected).
		3h	Reserved.

1.5.5.5 RTC Domain Clock Gating

Dynamic RTC domain clock gating is not supported. Note that the RTC oscillator, and by extension the RTC domain, can be permanently disabled by not connecting a crystal to the RTC oscillator. However, in this configuration, the RTC must still be powered and the RTC registers starting at I/O address 1900h will not be accessible. This includes the RTC Power Management Register which provides control to the on-chip LDOs and WAKEUP and RTC_CLKOUT pins. See the device-specific data manual for more details on permanently disabling the RTC oscillator.

1.5.6 Static Power Management

1.5.6.1 RTC Power Management Register (RTCPMGT) [1930h]

The RTC power management register (RTCPMGT) is shown in Figure 1-22 and described in Table 1-56.

Figure 1-22. RTC Power Management Register (RTCPMGT) [1930h]

15	5	4	3	2	1	0
Reserved		WU_DOUT	WU_DIR	BG_PD	LDO_PD	RTCCLKOUTEN
R-0		RW-0	RW-0	RW-0	RW-0	RW-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 1-56. RTC Power Management Register (RTCPMGT) Field Descriptions

Bit	Field	Value	Description
15-5	Reserved	0	Reserved
4	WU_DOUT		Wakeup output, active low/Open-drain.
		0	WAKEUP pin driven low.
		1	WAKEUP pin is in high impedance.
3	WU_DIR		Wakeup pin direction control.
		0	WAKEUP pin is configured as input.
		1	WAKEUP pin is configured as output.
			Note: The WAKEUP pin, when configured as an input, is active high. When it is configured as an output, it is open-drain and thus it should have an external pull-up and it is active low.
2-1	Reserved	0	Reserved
0	RTCCLKOUTEN		Clock-out output enable.
		0	Clock output disabled.
		1	Clock output enabled.

1.5.6.2 RTC Interrupt Flag Register (RTCINTFL) [1920h]

The RTC interrupt flag register (RTCINTFL) is shown in Figure 1-23 and described in Table 1-57.

Figure 1-23. RTC Interrupt Flag Register (RTCINTFL) [1920h]

15	14	8
ALARMFL	Reserved	
R-0	R-0	

7	6	5	4	3	2	1	0
Reserved		EXTFL	DAYFL	HOURFL	MINFL	SECFL	MSFL
R-0		R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 1-57. RTC Interrupt Flag Register (RTCINTFL) Field Descriptions

Bit	Field	Value	Description
15	ALARMFL		Indicates that an alarm interrupt has been generated.
		0	Alarm interrupt did not occur.
		1	Alarm interrupt occurred (write 1 to clear).
14-6	Reserved	0	Reserved.
5	EXTFL		External event has occurred.
		0	External event interrupt has not occurred.
		1	External event interrupt occurred (write 1 to clear).

Table 1-57. RTC Interrupt Flag Register (RTCINTFL) Field Descriptions (continued)

Bit	Field	Value	Description
4	DAYFL		Day event has occurred.
		0	Periodic Day event has not occurred.
		1	Periodic Day event occurred (write 1 to clear).
3	HOURFL		Hour event has occurred.
		0	Periodic Hour event has not occurred.
		1	Periodic Hour event occurred (write 1 to clear).
2	MINFL		Minute Event has occurred.
		0	Periodic Minute event has not occurred.
		1	Periodic Minute event occurred (write 1 to clear).
1	SECFL		Second Event occurred.
		0	Periodic Second event has not occurred.
		1	Periodic Second event occurred (write 1 to clear).
0	MSFL		Millisecond event occurred.
		0	Periodic Millisecond event has not occurred.
		1	Periodic Millisecond event occurred (write 1 to clear).

1.5.6.3 Internal Memory Low Power Modes

To save power, software can place on-chip memory (DARAM or SARAM) in one of two power modes: memory retention mode and active mode. These power modes are activated through the SLPZVDD and SLPZVSS bits of the RAM sleep mode control register 1 (RAMSLPMDCNTLR1). The power mode of the DARAM is independent from that of the SARAM.

When either type of memory is placed in memory retention, read and write accesses are not allowed. In memory retention mode, the memory is placed in a low power mode while maintaining its contents. The contents are retained as long as the CPU does not try to access that memory. In active mode, the memory is readily accessible by the CPU, but consumes more power .

Before placing memory in retention mode, you must ensure the CPU is not accessing that memory either through data or program access

NOTE: You must wait at least 10 CPU clock cycles after taking memory out of a low power mode before initiating any read or write access.

Table 1-58 summarizes the power modes for both DARAM and SARAM.

Table 1-58. On-Chip Memory Standby Modes

SLPZVDD	SLPZVSS	Mode	CV_{DD} Voltage
1	1	Active - Normal operational mode - Read and write accesses are allowed	1.05v or 1.3V
1	0	Retention - Low power mode - Contents are retained - No read or write access is allowed	1.05v or 1.3V

1.5.6.3.1 RAM Sleep Mode Control Register 1 (RAMSLPMDCNTLR1) [1C28h]

The RAM Sleep Mode Control Register 1 (RAMSLPMDCNTLR1) is shown in Figure 1-24 and described in Table 1-59.

Figure 1-24. RAM Sleep Mode Control Register 1 (RAMSLPMDCNTLR1) [1C28h]

15 4	3	2	1	0
Reserved	SARAMSLPZVDD	SARAMSLPZVSS	DARAMSLPZVDD	DARAMSLPZVSS
R-0	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 1-59. RAM Sleep Mode Control Register 1 (RAMSLPMDCNTLR1) Field Descriptions

Bit	Field	Value	Description
15-4	Reserved	0	Reserved.
3	SARAMSLPZVDD	0-1	SLPZVDD control for SARAM. The SARAM SLPZVDD and SLPZVSS bits define the mode of operation for the entire SARAM of the device (see Table 1-58).
2	SARAMSLPZVSS	0-1	SLPZVSS control for SARAM. The SARAM SLPZVDD and SLPZVSS bits define the mode of operation for the entire SARAM of the device (see Table 1-58).
1	DARAMSLPZVDD	0-1	SLPZVDD control for DARAM. The DARAM SLPZVDD and SLPZVSS bits define the mode of operation for the entire DARAM of the device (see Table 1-58).
0	DARAMSLPZVSS	0-1	SLPZVSS control for DARAM. The DARAM SLPZVDD and SLPZVSS bits define the mode of operation for the entire DARAM of the device (see Table 1-58).

1.5.7 Power Configurations

The power-saving features described in the previous sections, such as peripheral clock gating, and on-chip memory power down to name a few, can be combined to form a power configuration. Many different power configurations can be created by enabling and disabling different power domains and clock domains, however, this section defines some basic power configurations. These are shown and described in Table 1-60. Please note that there is no single instruction or register that can place the device in these power configurations. Instead, these power configurations are achieved by modifying multiple registers.

NOTE: Before you change the power configuration, make sure that there is a method for the DSP to exit the power configuration. After exiting a power configuration, your software may have to take additional steps to change the clock and power configuration for other domains.

NOTE: The on-chip Bootloader idles all peripherals and CPU ports at startup. It enables some peripherals as it uses them. Your application code should check the idle configuration of peripherals and CPU ports before using them to be sure these are not idle.

Table 1-60. Power Configurations

Power Configuration	Power Domain State	Clock Domain State	Steps to Enter Clock and Power Configuration	Available Methods for Changing/Exiting Clock and Power Configuration
		Disabled	RTCPMGT register	RTC interrupt
IDLE3	All power domains on	RTC clock domain enabled Other clock domains disabled	Idle peripheral domain Idle the clock generator domain Idle CPU domain Execute idle instruction	A. Use the WAKEUP pin. B. Generate an RTC interrupt. C. Use an unmasked hardware interrupt (INT0z or INT1z). D. Initiate a DSP hardware reset.
IDLE2	All power domains on	RTC clock domain enabled Clock generator domain enabled Other clock domains disabled	Idle peripheral domain Idle CPU domain Execute idle instruction	A. Use the WAKEUP pin. B. Generate an RTC interrupt. C. Use an unmasked hardware interrupt (INT0z, INT1z). D. Use an unmasked peripheral interrupt. E. Initiate a DSP hardware reset.
Active	All power domains on	All clock domains enabled	Turn on all power domains Enable all clock domains	A. Use the WAKEUP pin. B. Generate an RTC interrupt. C. Use an unmasked hardware interrupt (INT0z, INT1z). D. Use an unmasked peripheral interrupt. E. Initiate a DSP hardware reset.

1.5.7.1 IDLE2 Procedure

In this power configuration all the power domains are turned on, the RTC and clock generator domains are enabled, and the CPU domain is disabled. The DSP peripherals and the USB can also be disabled in this mode; however, this is not required. When you enter this power configuration all CPU and peripheral activity in the DSP is stopped. Leaving the clock generator domain enabled allows the DSP to quickly exit this power configuration since there is no need to wait for power domains to turn on or for the PLL to re-lock.

Follow these steps to enter the IDLE2 power configuration:

1. Wait for completion of all DMA transfers. You can poll the DMA transfer status and disable DMA transfers through the DMA registers.
2. If desired, disable the USB clock domain as described in Section 1.5.5.4.
3. Idle all the desired peripherals in the peripheral clock domain by modifying the peripheral clock gating configuration registers (PCGCR1 and PCGCR2). See Section 1.5.5.2 for more details on setting the DSP peripherals to idle mode.
4. Wait at least 6 CPU clock cycles to ensure all settings are completed.
5. Clear all interrupts by writing ones to the CPU interrupt flag registers (IFR0 and IFR1).
6. Enable the appropriate wake-up interrupt in the CPU interrupt enable registers (IER0 and IER1). If using the WAKEUP pin to exit this mode, configure the WAKEUP pin as input by setting WU_DIR = 1 in the RTC power management register (RTCPMGT). If using the RTC alarm or periodic interrupt as a wake-up event, the RTCINTEN bit must be set in the RTC interrupt enable register (RTCINTEN).
7. Disable the CPU domain by setting to 1 the CPUI, MPORTI, XPORTI, DPORTI, IPORTI, and CPI bits of the idle configuration register (ICR). Note that the MPORT will not go into idle mode if the USB, LCD, and DMA controllers are not idled.
8. Flush the CPU pipeline by executing 6 NOP instructions.
9. Apply the new idle configuration by executing the “IDLE” instruction. The content of ICR is copied to the idle status register (ISTR). The bits of ISTR are then propagated through the CPU domain system to enable or disable the specified clocks.

The IDLE instruction cannot be executed in parallel with another instruction.

To exit the IDLE2 power configuration, follow these steps:

1. Generate the wake-up interrupt you specified during the IDLE2 power down procedure.
2. After the interrupt is generated, the DSP will execute the interrupt service routine.
3. After exiting the interrupt service routine, code execution will resume from the point where the “IDLE” instruction was originally executed.

You can also exit the IDLE2 power configuration by generating a hardware reset. However, in this case, the DSP is completely reset and the state of the DSP before going into IDLE2 is lost.

1.5.7.2 IDLE3 Procedure

In this power configuration all the power domains are turned on, the CPU and clock generator domains are disabled, and the RTC clock domain is enabled. The DSP peripherals and the USB are also disabled in this mode. When you enter this power configuration, all CPU and peripheral activity in the DSP is stopped.

Since the clock generator domain is disabled, you must allow enough time for the PLL to re-lock before exiting this power configuration.

Follow these steps to enter the IDLE3 power configuration:

1. Wait for completion of all DMA transfers. You can poll the DMA transfer status and disable DMA transfers through the DMA registers.
2. Disable the USB clock domain as described in Section 1.5.5.4.
3. Idle all the desired peripherals in the peripheral clock domain by modifying the peripheral clock gating configuration registers (PCGCR1 and PCGCR2). See Section 1.5.5.2 for more details on setting the DSP peripherals to idle mode.
4. Wait at least 6 CPU clock cycles to ensure all settings are completed.
5. Disable the clock generator domain as described in Section 1.5.5.3.
6. Clear all interrupts by writing ones to the CPU interrupt flag registers (IFR0 and IFR1).
7. Enable the appropriate wake-up interrupt in the CPU interrupt enable registers (IER0 and IER1). If using the WAKEUP pin to exit this mode, configure the WAKEUP pin as input by setting WU_DIR = 1 in the RTC power management register (RTCPMGT). If using the RTC alarm or periodic interrupt as a wake-up event, the RTCINTEN bit must be set in the RTC interrupt enable register (RTCINTEN).

8. Disable the CPU domain by setting to 1 the CPUI, MPORTI, XPORTI, DPORTI, IPORTI, and CPI bits of the idle configuration register (ICR).
9. Flush the CPU pipeline by executing 6 NOP instructions.
10. Apply the new idle configuration by executing the IDLE instruction. The content of ICR is copied to the idle status register (ISTR). The bits of ISTR are then propagated through the CPU domain system to enable or disable the specified clocks.

The IDLE instruction cannot be executed in parallel with another instruction.

To exit the IDLE3 power configuration, follow these steps:

1. Generate the wake-up interrupt you specified during the IDLE3 power down procedure.
2. After the interrupt is generated, the DSP will execute the interrupt service routine.
3. After exiting the interrupt service routine, code execution will resume from the point where the “IDLE” instruction was originally executed.
4. Enable the clock generator domain as described in Section 1.5.5.3. You can also enable the clock generator domain inside the interrupt service routine.

You can also exit the IDLE3 power configuration by generating a hardware reset, however, in this case the DSP is completely reset and the state of the DSP before going into IDLE3 is lost.

1.5.7.3 Core Voltage Scaling

In the active power configuration, the core voltage can be reduced during periods of low processing demand and increased during high demand.

When the core voltage is decreased (1.3 V to 1.05 V) while the I/O voltage is maintained constant, device stability is determined by the voltage at the core voltage supply pins (CV_{DD}) and the clock speed of the device. The system designer must take into account the following fact:

- Software must ensure that the clock speed of the device does not exceed the maximum speed of the device at the lower voltage before making the voltage transition. For example, if the device is running at 100 MHz @ 1.3 V, then the PLL must be changed to 60 MHz before changing the core voltage to 1.05 V.

When the core voltage is increased (1.05V to 1.3V) while I/O voltage is maintained constant, device stability is determined by the voltage at the core voltage supply pins (CV_{DD}). Clock speed is not an issue since the device can operate faster at the higher voltage. However, when switching from 1.05 V to 1.3 V, the regulators might produce an overshoot that must not pass the maximum operational voltage of the core supply (see the *Recommended Operating Conditions* section in device-specific data manual). Otherwise, the device will be operating out of specification. This could happen if large current draw occurs while the regulator transitions to the higher voltage.

To prevent a large current draw, the voltage should be changed in a small uninterruptible routine that provides several NOP operations after the change to allow the voltage drop to stabilize. This stabilization time depends on the response of the regulators to its capacitive load and current draw.

For external LDO, this varies greatly and it is up to the system designer to ensure that the ringing is maintained within the DSP's core supply high voltage operational tolerance (see the *Recommended Operating Conditions* section in device-specific data manual).

1.6 Interrupts

Vector-relative locations and priorities for all internal and external interrupts are shown in Table 1-61.

Table 1-61. Interrupt Table

NAME	SOFTWARE (TRAP) EQUIVALENT	RELATIVE LOCATION (HEX BYTES) (1)	PRIORITY	FUNCTION
RESET	SINT0	0	0	Reset (hardware and software)
NMI (2)	SINT1	8	1	Non-maskable interrupt
INT0	SINT2	10	3	External user interrupt #0
INT1	SINT3	18	5	External user interrupt #1
TINT	SINT4	20	6	Timer aggregated interrupt
PROG0	SINT5	28	7	Programmable transmit interrupt 0 (I2S0 transmit or MMC/SD0 interrupt)
UART	SINT6	30	9	UART interrupt
PROG1	SINT7	38	10	Programmable receive interrupt 1 (I2S0 receive or MMC/SD0 SDIO interrupt)
DMA	SINT8	40	11	DMA aggregated interrupt
PROG2	SINT9	48	13	Programmable transmit interrupt 1 (I2S1 transmit or MMC/SD1 interrupt)
-	SINT10	50	14	Software interrupt
PROG3	SINT11	58	15	Programmable receive interrupt 3 (I2S1 Receive or MMC/SD1 SDIO interrupt)
LCD	SINT12	60	17	LCD interrupt
SAR	SINT13	68	18	10-bit SAR A/D conversion or pin interrupt
XMT2	SINT14	70	21	I2S2 transmit interrupt
RCV2	SINT15	78	22	I2S2 receive interrupt
XMT3	SINT16	80	4	I2S3 transmit interrupt
RCV3	SINT17	88	8	I2S3 receive interrupt
RTC	SINT18	90	12	Wakeup or real-time clock interrupt
SPI	SINT19	98	16	SPI interrupt
USB	SINT20	A0	19	USB Interrupt
GPIO	SINT21	A8	20	GPIO aggregated interrupt
EMIF	SINT22	B0	23	EMIF error interrupt
I2C	SINT23	B8	24	I2C interrupt
BERR	SINT24	C0	2	Bus error interrupt
DLOG	SINT25	C8	25	Data log interrupt
RTOS	SINT26	D0	26	Real-time operating system interrupt
-	SINT27	D8	14	Software interrupt #27
-	SINT28	E0	15	Software interrupt #28
-	SINT29	E8	16	Software interrupt #29
-	SINT30	F0	17	Software interrupt #30
-	SINT31	F8	18	Software interrupt #31

(1) Absolute addresses of the interrupt vector locations are determined by the contents of the IVPD and IVPH registers. Interrupt vectors for interrupts 0-15 and 24-31 are relative to IVPD. Interrupt vectors for interrupts 16-23 are relative to IVPH.

(2) The NMI pin is internally tied high. However, NMI interrupt vector can be used for SINT1.

1.6.1 IFR and IER Registers

The IFR0 (Interrupt Flag Register 0) and IER0 (Interrupt Enable Register 0) bit layouts are shown in Figure 1-25 and described in Table 1-62 .

Figure 1-25. IFR0 and IER0 Bit Locations

15	14	13	12	11	10	9	8
RCV2	XMT2	SAR	LCD	PROG3	Reserved	PROG2	DMA
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
PROG1	UART	PROG0	TINT	INT1	INT0	Reserved	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 1-62. IFR0 and IER0 Bit Descriptions

Bit	Field	Value	Description
15	RCV2	1-0	I2S2 receive interrupt flag/mask bit.
14	XMT2	1-0	I2S2 transmit interrupt flag/mask bit.
13	SAR	1-0	10-BIT SAR A/D conversion or pen interrupt flag/mask bit.
12	LCD	1-0	LCD interrupt bit.
11	PROG3	1-0	Programmable receive interrupt 3 flag/mask bit. This bit is used as either the I2S1 receive interrupt flag/mask bit or the MMC/SD1 SDIO interrupt flag/mask bit. The function of this bit is selected depending on the setting of the SP1MODE bit is in external bus selection register. If SP1MODE = 00b, this bit supports MMC/SD1 SDIO interrupts. If SP1MODE = 01, this bit supports I2S1 interrupts.
10	Reserved	0	Reserved. This bit should always be written with 0.
9	PROG2	1-0	Programmable transmit interrupt 2 flag/mask bit. This bit is used as either the I2S1 transmit interrupt flag/mask bit or the MMC/SD1 interrupt flag/mask bit. The function of this bit is selected depending on the setting of the SP1MODE bit in the external bus selection register. If SP1MODE = 00b, this bit supports MMC/SD1 interrupts. If SP1MODE = 01, this bit supports I2S1 interrupts.
8	DMA	1-0	DMA aggregated interrupt flag/mask bit.
7	PROG1	1-0	Programmable receive interrupt 1 flag/mask bit. This bit is used as either the I2S0 receive interrupt flag/mask bit or the MMC/SD0 SDIO interrupt flag/mask bit. The function of this bit is selected depending on the setting of the SP0MODE bit in the external bus selection register. If SP0MODE = 00b, this bit supports MMC/SD0 SDIO interrupts. If SP0MODE = 01, this bit supports I2S0 interrupts.
6	UART	1-0	UART interrupt flag/mask bit.
5	PROG0	1-0	Programmable transmit interrupt 0 flag/mask bit. This bit is used as either the I2S0 transmit interrupt flag/mask bit or the MMC/SD0 interrupt flag/mask bit. The function of this bit is selected depending on the setting of the SP0MODE bit in the external bus selection register. If SP0MODE = 00b, this bit supports MMC/SD0 interrupts. If SP0MODE = 01, this bit supports I2S0 interrupts.
4	TINT	1-0	Timer aggregated interrupt flag/mask bit.
3	INT1	1-0	External user interrupt #1 flag/mask bit.
2	INT0	1-0	External user interrupt #0 flag/mask bit.
1-0	Reserved	0	Reserved. This bit should always be written with 0.

The IFR1 (Interrupt Flag Register 1) and IER1 (Interrupt Enable Register 1) bit layouts are shown in Figure 1-26 and described in Table 1-63.

Figure 1-26. IFR1 and IER1 Bit Locations

15					11	10	9	8
Reserved						RTOS	DLOG	BERR
R-0						R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0	
I2C	EMIF	GPIO	USB	SPI	RTC	RCV3	XMT3	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 1-63. IFR1 and IER1 Bit Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved. This bit should always be written with 0.
10	RTOS	1-0	Real-Time operating system interrupt flag/mask bit.
9	DLOG	1-0	Data log interrupt flag/mask bit.
8	BERR	1-0	Bus error interrupt flag/mask bit.
7	I2C	1-0	I2C interrupt flag/mask bit.
6	EMIF	1-0	EMIF error interrupt flag/mask bit.
5	GPIO	1-0	GPIO aggregated interrupt flag/mask bit.
4	USB	1-0	USB interrupt flag/mask bit.
3	SPI	1-0	SPI interrupt flag/mask bit.
2	RTC	1-0	Wakeup or real-time clock interrupt flag/mask bit.
1	RCV3	1-0	I2S3 receive interrupt flag/mask bit.
0	XMT3	1-0	I2S3 transmit interrupt flag/mask bit.

1.6.2 Interrupt Timing

The external interrupts pins ($\overline{INT0}$ and $\overline{INT1}$) are synchronized to the core CPU by way of a two-flip-flop synchronizer. The interrupt pins are sampled on the falling edges of CLKOUT. A sequence of 1-0-0 on consecutive cycles on the interrupt pin is required for an interrupt to be detected. Therefore, the minimum low pulse duration on the external interrupts on the device is two CLKOUT periods.

To define the minimum low pulse width in nanoseconds scale, you should take into account that the on-chip PLL of the device is software programmable and that your application may be dynamically changing the frequency of PLL. You should use the slowest frequency that will be used by your application to calculate the minimum interrupt pulse duration in nanoseconds.

1.6.3 Timer Interrupt Aggregation Flag Register (TIAFR) [1C14h]

The timer interrupt aggregation flag register (TIAFR) latches each timer (Timer 0, Timer 1, and Timer 2) interrupt signal when the timer counter expires. Using this register, the programmer can determine which timer generated the timer aggregated CPU interrupt signal (TINT). Each Timer flag in TIAFR needs to be cleared by the CPU with a write of 1. Note that the corresponding timer interrupt register must also be cleared. For more information, see the *TMS320C5515/14/05/04/VC05/VC04 DSP Timer/Watchdog Timer User's Guide* (SPRUFO2).

The Timer Interrupt Aggregation Flag Register (TIAFR) is shown in Figure 1-27 and described in Table 1-64.

Figure 1-27. Timer Interrupt Aggregation Flag Register (TIAFR) [1C14h]

15	3	2	1	0
Reserved		TIM2FLAG	TIM1FLAG	TIM0FLAG
R-0		R/W1C	R/W1C	R/W1C

LEGEND: R/W1C = Read/Write 1 to Clear; R = Read only; *-n* = value after reset

Table 1-64. Timer Interrupt Aggregation Flag Register (TIAFR) Field Descriptions

Bit	Field	Value	Description
15-3	Reserved	0	Reserved.
2	TIM2FLAG		Timer 2 interrupt flag bit. This bit latches the timer interrupt signal when the timer counter expires. You can clear this flag bit by writing a 1 to it.
		0	Timer has not generated an interrupt.
		1	Timer interrupt has occurred.
1	TIM1FLAG		Timer 1 interrupt flag bit. This bit latches the timer interrupt signal when the timer counter expires. You can clear this flag bit by writing a 1 to it.
		0	Timer has not generated an interrupt.
		1	Timer interrupt has occurred.
0	TIM0FLAG		Timer 0 interrupt flag bit. This bit latches the timer interrupt signal when the timer counter expires. You can clear this flag bit by writing a 1 to it.
		0	Timer has not generated an interrupt.
		1	Timer interrupt has occurred.

1.7 System Configuration and Control

1.7.1 Overview

The DSP includes system-level registers for controlling and configuring top-level control logic required by the device. These system-level registers are accessible by the CPU and support the following features:

- Device Identification
- Device Configuration
  - Pin multiplexing control
  - Output drive strength configuration
  - Internal pull-up and pull-down enable/disable
- DMA Controller Configuration
- Peripheral Reset
- EMIF and USB Byte Access

1.7.2 Device Identification

The DSP includes a readable device ID that is readable via a set of memory map registers for easy access during operation. These registers are summarized in the following table.

Table 1-65. Die ID Registers

CPU Word Address	Acronym	Register Description	Section
1C40h	DIEIDR0	Die ID Register 0	Section 1.7.2.1
1C41h	DIEIDR1	Die ID Register 1	Section 1.7.2.2
1C42h	DIEIDR2	Die ID Register 2	Section 1.7.2.3
1C43h	DIEIDR3	Die ID Register 3	Section 1.7.2.4
1C44h	DIEIDR4	Die ID Register 4	Section 1.7.2.5
1C45h	DIEIDR5	Die ID Register 5	Section 1.7.2.6
1C46h	DIEIDR6	Die ID Register 6	Section 1.7.2.7
1C47h	DIEIDR7	Die ID Register 7	Section 1.7.2.8

1.7.2.1 Die ID Register 0 (DIEIDR0) [1C40h]

The Die ID Register 0 (DIEIDR0) is shown in Figure 1-28 and described in Table 1-66.

Figure 1-28. Die ID Register 0 (DIEIDR0) [1C40h]

15	0
DIEID0	
R-0	

LEGEND: R = Read only; -*n* = value after reset

Table 1-66. Die ID Register 0 (DIEIDR0) Field Descriptions

Bit	Field	Value	Description
15-0	DIEID0	0-FFFFh	Die ID bits.

1.7.2.2 Die ID Register 1 (DIEIDR1) [1C41h]

The Die ID Register 1 (DIEIDR1) is shown in Figure 1-29 and described in Table 1-67.

Figure 1-29. Die ID Register 1 (DIEIDR1) [1C41h]

15	14	13	0
Reserved		DIEID1	
R-0		R-0	

LEGEND: R = Read only; -*n* = value after reset

Table 1-67. Die ID Register 1 (DIEIDR1) Field Descriptions

Bit	Field	Value	Description
15-14	Reserved	0	Reserved.
13-0	DIEID1	0-3FFFh	Die ID bits.

1.7.2.3 Die ID Register 2 (DIEIDR2) [1C42h]

The Die ID Register 2 (DIEIDR2) is shown in Figure 1-30 and described in Table 1-68.

Figure 1-30. Die ID Register 2 (DIEIDR2) [1C42h]

15	0
DIEID2	
R-0	

LEGEND: R = Read only; -*n* = value after reset

Table 1-68. Die ID Register 2 (DIEIDR2) Field Descriptions

Bit	Field	Value	Description
15-0	DIEID2	0-FFFFh	Die ID bits.

1.7.2.4 Die ID Register 3 (DIEIDR3) [1C43h]

The Die ID Register 3 (DIEIDR3) is shown in Figure 1-31 and described in Table 1-69.

Figure 1-31. Die ID Register 3 (DIEIDR3) [1C43h]

15 12	11 0
DesignRev	DIEID3
R-0101	R-0

LEGEND: R = Read only; -*n* = value after reset

Table 1-69. Die ID Register 3 (DIEIDR3) Field Descriptions

Bit	Field	Value	Description
15-12	DesignRev	0-Fh	Silicon Revision
		0	Silicon Revision 1.0
		1	Silicon Revision 1.1
		2	Silicon Revision 1.2
		3	Silicon Revision 1.3
		4	Silicon Revision 1.4
11-0	DIEID3	0-FFFFh	Die ID bits.

1.7.2.5 Die ID Register 4 (DIEIDR4) [1C44h]

The Die ID Register 4 (DIEIDR4) is shown in Figure 1-32 and described in Table 1-70.

Figure 1-32. Die ID Register 4 (DIEIDR4) [1C44h]

15 6	5 0
Reserved	DIEID4
R-0	R-0

LEGEND: R = Read only; -*n* = value after reset

Table 1-70. Die ID Register 4 (DIEIDR4) Field Descriptions

Bit	Field	Value	Description
15-6	Reserved	0	Reserved.
5-0	DIEID4	0-3Fh	Die ID bits.

1.7.2.6 Die ID Register 5 (DIEIDR5) [1C45h]

The Die ID Register 5 (DIEIDR5) is shown in Figure 1-33 and described in Table 1-71.

Figure 1-33. Die ID Register 5 (DIEIDR5) [1C45h]

15 0
Reserved
R-0

LEGEND: R = Read only; -*n* = value after reset

Table 1-71. Die ID Register 5 (DIEIDR5) Field Descriptions

Bit	Field	Value	Description
15-0	Reserved	0	Reserved.

1.7.2.7 Die ID Register 6 (DIEIDR6) [1C46h]

The Die ID Register 6 (DIEIDR6) is shown in Figure 1-34 and described in Table 1-72.

Figure 1-34. Die ID Register 6 (DIEIDR6) [1C46h]

15	0
Reserved	
R-0	

LEGEND: R = Read only; -*n* = value after reset

Table 1-72. Die ID Register 6 (DIEIDR6) Field Descriptions

Bit	Field	Value	Description
15-0	Reserved	0	Reserved.

1.7.2.8 Die ID Register 7 (DIEIDR7) [1C47h]

The Die ID Register 7 (DIEIDR7) is shown in Figure 1-35 and described in Table 1-73.

Figure 1-35. Die ID Register 7 (DIEIDR7) [1C47h]

15	14	1	0
Reserved	CHECKSUM		Reserved
R-0	R-0		R-0

LEGEND: R = Read only; -*n* = value after reset

Table 1-73. Die ID Register 7 (DIEIDR7) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved.
14-1	CHECKSUM	0-3FFFh	Checksum bits.
0	Reserved	0	Reserved.

1.7.3 Device Configuration

The DSP includes registers for configuring pin multiplexing, the pin output drive strength, and the internal pull-ups and pull-downs.

1.7.3.1 Configurable External Buses

The DSP offers several combinations of configurations for its external parallel port and two serial ports. This allows the system designer to choose the appropriate media interface for its application without the need of a large-pin-count package. The external bus selection register (EBSR) controls the routing of the parallel and serial port signals.

1.7.3.1.1 Serial Port Pin Multiplexing

The DSP's serial port 0 and serial port 1 consists of 6 signals each that support three different modes:

- Mode 0 (MMC/SD)
  All 6 signals of the MMC/SD port are routed to the 6 external signals of the serial port.
- Mode 1 (I2S)
  All 4 signals of the I2S module and 2 GPIO signals are routed to the 6 external signals of the serial port.
- Mode 2 (GPIO)
  6 GPIO signals are routed to the 6 external signals of the serial port.

The mode selection of serial port 0 and serial port 1 is controlled through the SP0MODE and SP1MODE bits of the external bus selection register (EBSR). Table 1-74 and Table 1-75 illustrate the individual signal routing of the serial ports based on the configuration of the SP0MODE and SP1MODE bits.

Table 1-74. Serial Port 0 Signal Routing

PDINHIBR1 REGISTER BIT FIELDS [1]	PIN MUX SIGNAL NAME	EBSR SP0MODE BITS		
		MODE 0	MODE 1	MODE 2
		00	01	10
S00PD	MMC0_CLK/I2S0_CLK/GP[0]	MMC0_CLK	I2S0_CLK	GP[0]
S01PD	MMC0_CMD/I2S0_FS/GP[1]	MMC0_CMD	I2S0_FS	GP[1]
S02PD	MMC0_D0/I2S0_DX/GP[2]	MMC0_D0	I2S0_DX	GP[2]
S03PD	MMC0_D1/I2S0_RX/GP[3]	MMC0_D1	I2S0_RX	GP[3]
S04PD	MMC0_D2/GP[4]	MMC0_D2	GP[4]	GP[4]
S05PD	MMC0_D3/GP[5]	MMC0_D3	GP[5]	GP[5]

(1) The pin mux signals names with PDINHIBR1 register bit field references can have the pulldown register enabled or disabled via this register.

Table 1-75. Serial Port 1 Signal Routing

PDINHIBR1 REGISTER BIT FIELDS [1]	PIN MUX SIGNAL NAME	EBSR SP1MODE BITS		
		MODE 0	MODE 1	MODE 2
		00	01	10
S10PD	MMC1_CLK/I2S1_CLK/GP[6]	MMC1_CLK	I2S1_CLK	GP[6]
S11PD	MMC1_CMD/I2S1_FS/GP[7]	MMC1_CMD	I2S1_FS	GP[7]
S12PD	MMC1_D0/I2S1_DX/GP[8]	MMC1_D0	I2S1_DX	GP[8]
S13PD	MMC1_D1/I2S1_RX/GP[9]	MMC1_D1	I2S1_RX	GP[9]
S14PD	MMC1_D2/GP[10]	MMC1_D2	GP[10]	GP[10]
S15PD	MMC1_D3/GP[11]	MMC1_D3	GP[11]	GP[11]

(1) The pin mux signals names with PDINHIBR1 register bit field references can have the pulldown register enabled or disabled via this register.

1.7.3.1.2 Parallel Port Multiplexing

The DSP's 16-bit parallel port consists of 21 signals that support seven different modes:

- Mode 0 (16-bit LCD controller)

  All 21 signals of the LCD controller module are routed to the 21 external signals of the parallel port.
- Mode 1 (GPIO, SPI, UART, and I2S2)

  6 GPIO signals, 7 signals of the SPI module, 4 signals of the UART module and 4 signals of the I2S2 module are routed to the 21 external signals of the parallel port.
- Mode 2 (8-bit LCD controller and GPIO)

  8-bits of pixel data of the LCD controller module and 8 bits of GPIO are routed to the 21 external signals on the parallel port.
- Mode 3 (8-bit LCD controller, SPI, and I2S3)

  8-bits of pixel data of the LCD controller module, 4 signals of the SPI module, and 4 signals of the I2S3 module are routed to the 21 external signals on the parallel port.
- Mode 4 (8-bit LCD controller, I2S2, and UART)

  8-bits of pixel data of the LCD controller module, 4 signals of the I2S2 module, and 4 signals of the UART module are routed to the 21 external signals on the parallel port.
- Mode 5 (8-bit LCD controller, UART, and SPI)

  8-bits of pixel data of the LCD controller module, 4 signals of the SPI module and 4 signals of the UART module are routed to the 21 external signals on the parallel port.
- Mode 6 (GPIO, SPI, and I2S3)

  6 GPIO, 7 signals of the SPI module, and two sets of 4 signals of the I2S2 and I2S3 module are routed to the 21 external signals of the parallel port.

The mode selection of the parallel port is controlled through the PPMODE bits of the external bus selection register (EBSR). Table 1-76 illustrates the individual signal routing of the parallel port based on the configuration of the PPMODE bits.

Table 1-76. Parallel Port Signal Routing

PDINHIBR3 REGISTER BIT FIELDS (1)	PIN MUX SIGNAL NAME	EBSR PPMODE BITS						
		MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6
		000	001	010	011	100	101	110
	LCD_PCLK_RS/SPI_CLK	LCD_PCLK_RS	SPI_CLK	LCD_PCLK_RS	LCD_PCLK_RS	LCD_PCLK_RS	LCD_PCLK_RS	SPI_CLK
P0PD	LCD_D[0]/SPI_RX	LCD_D[0]	SPI_RX	LCD_D[0]	LCD_D[0]	LCD_D[0]	LCD_D[0]	SPI_RX
P1PD	LCD_D[1]/SPI_TX	LCD_D[1]	SPI_TX	LCD_D[1]	LCD_D[1]	LCD_D[1]	LCD_D[1]	SPI_TX
P2PD	LCD_D[2]/GP[12]	LCD_D[2]	GP[12]	LCD_D[2]	LCD_D[2]	LCD_D[2]	LCD_D[2]	GP[12]
P3PD	LCD_D[3]/GP[13]	LCD_D[3]	GP[13]	LCD_D[3]	LCD_D[3]	LCD_D[3]	LCD_D[3]	GP[13]
P4PD	LCD_D[4]/GP[14]	LCD_D[4]	GP[14]	LCD_D[4]	LCD_D[4]	LCD_D[4]	LCD_D[4]	GP[14]
P5PD	LCD_D[5]/GP[15]	LCD_D[5]	GP[15]	LCD_D[5]	LCD_D[5]	LCD_D[5]	LCD_D[5]	GP[15]
P6PD	LCD_D[6]/GP[16]	LCD_D[6]	GP[16]	LCD_D[6]	LCD_D[6]	LCD_D[6]	LCD_D[6]	GP[16]
P7PD	LCD_D[7]/GP[17]	LCD_D[7]	GP[17]	LCD_D[7]	LCD_D[7]	LCD_D[7]	LCD_D[7]	GP[17]
P8PD	LCD_D[8]/I2S2_CLK/GP[18]/SPI_CLK	LCD_D[8]	I2S2_CLK	GP[18]	SPI_CLK	I2S2_CLK	SPI_CLK	I2S2_CLK
P9PD	LCD_D[9]/I2S2_FS/GP[19]/SPI_CS0	LCD_D[9]	I2S2_FS	GP[19]	SPI_CS0	I2S2_FS	SPI_CS0	I2S2_FS
P10PD	LCD_D[10]/I2S2_RX/GP[20]/SPI_RX	LCD_D[10]	I2S2_RX	GP[20]	SPI_RX	I2S2_RX	SPI_RX	I2S2_RX
P11PD	LCD_D[11]/I2S2_DX/GP[27]/SPI_TX	LCD_D[11]	I2S2_DX	GP[27]	SPI_TX	I2S2_DX	SPI_TX	I2S2_DX
P12PD	LCD_D[12]/UART_RTS/GP[28]/I2S3_CLK	LCD_D[12]	UART_RTS	GP[28]	I2S3_CLK	UART_RTS	UART_RTS	I2S3_CLK
P13PD	LCD_D[13]/UART_CTS/GP[29]/I2S3_FS	LCD_D[13]	UART_CTS	GP[29]	I2S3_FS	UART_CTS	UART_CTS	I2S3_FS
P14PD	LCD_D[14]/UART_RXD/GP[30]/I2S3_RX	LCD_D[14]	UART_RXD	GP[30]	I2S3_RX	UART_RXD	UART_RXD	I2S3_RX
P15PD	LCD_D[15]/UART_TXD/GP[31]/I2S3_DX	LCD_D[15]	UART_TXD	GP[31]	I2S3_DX	UART_TXD	UART_TXD	I2S3_DX
	LCD_BIAS_CS0/SPI_CS0	LCD_BIAS_CS0	SPI_CS0	LCD_BIAS_CS0	LCD_BIAS_CS0	LCD_BIAS_CS0	LCD_BIAS_CS0	SPI_CS0
	LCD_MCLK/SPI_CS1	LCD_MCLK	SPI_CS1	LCD_MCLK	LCD_MCLK	LCD_MCLK	LCD_MCLK	SPI_CS1
	LCD_HSYNC_WS/SPI_CS2	LCD_HSYNC	SPI_CS2	LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	SPI_CS2
	LCD_VSYNC_ALE/SPI_CS3	LCD_VSYNC	SPI_CS3	LCD_VSYNC	LCD_VSYNC	LCD_VSYNC	LCD_VSYNC	SPI_CS3

(1) The pin mux signals names with PDINHIBR3 register bit field references can have the pulldown resister enabled or disabled via this register.

1.7.3.1.3 External Bus Selection Register (EBSR) [1C00h]

The external bus selection register (EBSR) determines the mapping of the LCD controller, I2S, UART, and SPI signals to the 21 signals of the external parallel port. It also determines the mapping of the I2S or MMC/SD ports to serial port 1 and serial port 2. The EBSR is located at port address 1C00h. Once the bit fields of this register are changed, the routing of the signals takes place on the next CPU clock cycle.

Additionally, the EBSR controls the function of the upper bits of the EMIF address bus. Pin EM_A[20:15] can be individually configured as GPIO pins through the Axx_MODE bits. When Axx_MODE = 1, the EM_A[xx] pin functions as a GPIO pin. When Axx_MODE = 0, the EM_A[xx] pin retains its EMIF functionality.

Before modifying the values of the external bus selection register, you must clock gate all affected peripherals (see Section 1.5.5.2 for more information on clock gating peripherals). After the external bus selection register has been modified, you must reset the peripherals before using them.

After the boot process is complete, the external bus selection register must be modified only once, during device configuration. Continuously switching the EBSR configuration is not supported.

The External Bus Selection Register (EBSR) is shown in Figure 1-36 and described in Table 1-77.

Figure 1-36. External Bus Selection Register (EBSR) [1C00h]

15	14	12	11	10	9	8
Reserved	PPMODE		SP1MODE		SP0MODE	
R-0	R/W-0		R/W-0		R/W-0	

7	6	5	4	3	2	1	0
Reserved		A20_MODE	A19_MODE	A18_MODE	A17_MODE	A16_MODE	A15_MODE
R-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 1-77. External Bus Selection Register (EBSR) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved
14-12	PPMODE		Parallel port mode bits. These bits control the pin muxing on the parallel port.
		0	Mode 0 (16-bit LCD controller. All 21 signals of the LCD controller module are routed to the 21 external signals of the parallel port.
		1h	Mode 1 GPIO, SPI, UART, and I2S2: 6 GPIO signals, 7 signals of the SPI module, 4 signals of the UART module and 4 signals of the I2S2 module are routed to the 21 external signals of the parallel port.
		2h	Mode 2 8-bit LCD controller and GPIO: 8-bits of pixel data of the LCD controller module and 8 bits of GPIO are routed to 21 external signals on the parallel port.
		3h	Mode 3 3 8-bit LCD controller, SPI, and I2S3: 8-bits of pixel data of the LCD controller module, 4 signals of the SPI module, and 4 signals of the I2S3 module are routed to the 21 external signals on the parallel port.
		4h	Mode 4 4 8-bit LCD controller, I2S2, and UART: 8-bits of pixel data of the LCD controller module, 4 signals of the I2S2 module, and 4 signals of the UART module are routed to the 21 external signals on the parallel port.
		5h	Mode 5 8-bit LCD controller, UART, and SPI: 8-bits of pixel data of the LCD controller module, 4 signals of the U ART module, and 4 signals of the SPI module are routed to the 21 external signals on the parallel port.
		6h	Mode 6 GPIO, SPI, and I2S3: 6 PIO, 7 signals of the SPI module, and two sets of 4 signals of the I2S2 and I2S3 module are routed to the 21 external signals of the parallel port.
			The mode selection of the parallel port is controlled.
		7h	Reserved, do not use.
11-10	SP1MODE		Serial port 1 mode bits. These bits control the pin muxing on serial port 1.
		0	Mode0 (MMC/SD) All 6 signals of the MMC/SD port are routed to the 6 external signals of the serial port.
		1h	Mode 1 (I2S) All 4 signals of the I2S module and 2 GPIO signals are routed to the 6 external signals of the serial port.
		2h	Mode 2 (GPIO) 6 GPIO signals are routed to the 6 external signals of the serial port. The mode selection of serial port 0 and serial port 1 is controlled through the
		3h	Mode 3
9-8	SP0MODE		Serial port 0 mode bits. These bits control the pin muxing on serial port 0.
		0	Mode 0
		1h	Mode 1
		2h	Mode 2
		3h	Mode 3
7-6	Reserved	0	Reserved
5	A20_MODE		This bit controls the pin multiplexing on EM_A[20].
		0	Pin behaves as EM_A[20].
		1	Pin behaves as GP[26].
4	A19_MODE		This bit controls the pin multiplexing on EM_A[19].
		0	Pin behaves as EM_A[19].
		1	Pin behaves as GP[25].

Table 1-77. External Bus Selection Register (EBSR) Field Descriptions (continued)

Bit	Field	Value	Description
3	A18_MODE		This bit controls the pin multiplexing on EM_A[18].
		0	Pin behaves as EM_A[18].
		1	Pin behaves as GP[24].
2	A17_MODE		This bit controls the pin multiplexing on EM_A[17].
		0	Pin behaves as EM_A[17].
		1	Pin behaves as GP[23].
1	A16_MODE		This bit controls the pin multiplexing on EM_A[16].
		0	Pin behaves as EM_A[16].
		1	Pin behaves as GP[22].
0	A15_MODE		This bit controls the pin multiplexing on EM_A[15].
		0	Pin behaves as EM_A[15].
		1	Pin behaves as GP[21].

1.7.3.2 Output Slew Rate Control Register (OSRCR) [1C16h]

To provide the lowest power consumption setting, the DSP has configurable slew rate on its EMIF and CLKOUT output pins. You can use the output slew rate register (ODSCR) to set a subset of the device I/O pins to quarter, minimum or maximum drive strength.

The output slew rate control register (OSRCR) is shown in Figure 1-37 and described inTable 1-78.

Figure 1-37. Output Slew Rate Control Register (OSRCR) [1C16h]

15	3	2	1	0
Reserved		CLKOUTSR	Reserved	EMIFSR
R-0		RW-1	R-0	RW-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 1-78. Output Slew Rate Control Register (OSRCR) Field Descriptions

Bit	Field	Value	Description
15-3	Reserved	0	Reserved.
2	CLKOUTSR		CLKOUT pin output slew rate bits. These bits set the slew rate for the CLKOUT pin.
		0	Minimum slew rate.
		1	Maximum slew rate.
1	Reserved	0	Reserved.
0	EMIFSR		EMIF pin output slew rate bits. These bits set the slew rate for the EMIF pins.
		0	Minimum slew rate.
		1	Maximum slew rate.

1.7.3.3 Pull-up/Pull-down Inhibit Register (PDINHIBR1, PDINHIBR2, and PDINHIBR3 [1C17h, 1C18h, and 1C19h]

The DSP allows you to individually enable or disable the internal pull-up and pull-down resistors. You can individually inhibit the pull-up and pull-down resistors of the I/O pins through the pull-down/up inhibit registers (PDINHIBRn).

The Pull-Down Inhibit Register 1 (PDINHIBR1) is shown in Figure 1-38 and described in Table 1-79.

Figure 1-38. Pull-Down Inhibit Register 1 (PDINHIBR1) [1C17h]

15	14	13	12	11	10	9	8
Reserved		S15PD	S14PD	S13PD	S12PD	S11PD	S10PD
R-0		R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
7	6	5	4	3	2	1	0
Reserved		S05PD	S04PD	S03PD	S02PD	S01PD	S00PD
R-0		R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 1-79. Pull-Down Inhibit Register 1 (PDINHIBR1) Field Descriptions

Bit	Field	Value	Description
15-14	Reserved	0	Reserved.
13	S15PD		Serial port 1 pin 5 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
12	S14PD		Serial port 1 pin 4 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.

Table 1-79. Pull-Down Inhibit Register 1 (PDINHIBR1) Field Descriptions (continued)

Bit	Field	Value	Description
11	S13PD		Serial port 1 pin 3 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
10	S12PD		Serial port 1 pin 2 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
9	S11PD		Serial port 1 pin 1 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
8	S10PD		Serial port 1 pin 0 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
7-6	Reserved	0	Reserved.
5	S05PD		Serial port 0 pin 5 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
4	S04PD		Serial port 0 pin 4 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
3	S03PD		Serial port 0 pin 3 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
2	S02PD		Serial port 0 pin 2 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
1	S01PD		Serial port 0 pin 1 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
0	S00PD		Serial port 0 pin 0 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.

The Pull-Down Inhibit Register 2 (PDINHIBR2) is shown in Figure 1-39 and described in Table 1-80.

Figure 1-39. Pull-Down Inhibit Register 2 (PDINHIBR2) [1C18h]

15	14	13	12	11	10	9	8
Reserved	INT1PU	INT0PU	RESETPU	EMU01PU	TDIPU	TMSPU	TCKPU
R-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
Reserved		A20PD	A19PD	A18PD	A17PD	A16PD	A15PD
R-0		R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 1-80. Pull-Down Inhibit Register 2 (PDINHIBR2) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved.
14	INT1PU		Interrupt 1 pin pull-up inhibit bit. Setting this bit to 1 disables the pin's internal pull-up.
		0	Pin pull-up is enabled.
		1	Pin pull-up is disabled.
13	INT0PU		Interrupt 0 pin pull-up inhibit bit. Setting this bit to 1 disables the pin's internal pull-up.
		0	Pin pull-up is enabled.
		1	Pin pull-up is disabled.
12	RESETPU		Reset pin pull-up inhibit bit. Setting this bit to 1 disables the pin's internal pull-up.
		0	Pin pull-up is enabled.
		1	Pin pull-up is disabled.
11	EMU01PU		EMU1 and EMU0 pin pull-up inhibit bit. Setting this bit to 1 disables the pin's internal pull-up.
		0	Pin pull-up is enabled.
		1	Pin pull-up is disabled.
10	TDIPU		TDI pin pull-up inhibit bit. Setting this bit to 1 disables the pin's internal pull-up.
		0	Pin pull-up is enabled.
		1	Pin pull-up is disabled.
9	TMSPU		TMS pin pull-up inhibit bit. Setting this bit to 1 disables the pin's internal pull-up.
		0	Pin pull-up is enabled.
		1	Pin pull-up is disabled.
8	TCKPU		TCK pin pull-up inhibit bit. Setting this bit to 1 disables the pin's internal pull-up.
		0	Pin pull-up is enabled.
		1	Pin pull-up is disabled.
7-6	Reserved	0	Reserved.
5	A20PD		EMIF A[20] pin pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
4	A19PD		EMIF A[19] pin pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
3	A18PD		EMIF A[18] pin pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
2	A17PD		EMIF A[17] pin pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
1	A16PD		EMIF A[16] pin pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
0	A15PD		EMIF A[15] pin pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.

The Pull-Down Inhibit Register 3 (PDINHIBR3) is shown in Figure 1-40 and described in Table 1-81.

Figure 1-40. Pull-Down Inhibit Register 3 (PDINHIBR3) [1C19h]

15	14	13	12	11	10	9	8
PD15PD	PD14PD	PD13PD	PD12PD	PD11PD	PD10PD	PD9PD	PD8PD
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
7	6	5	4	3	2	1	0
PD7PD	PD6PD	PD5PD	PD4PD	PD3PD	PD2PD	Reserved	
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 1-81. Pull-Down Inhibit Register 3 (PDINHIBR3) Field Descriptions

Bit	Field	Value	Description
15	PD15PD		Parallel port pin 15 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
14	PD14PD		Parallel port pin 14 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
13	PD13PD		Parallel port pin 13 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
12	PD12PD		Parallel port pin 12 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
11	PD11PD		Parallel port pin 11 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
10	PD10PD		Parallel port pin 10 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
9	PD9PD		Parallel port pin 9 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
8	PD8PD		Parallel port pin 8 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
7	PD7PD		Parallel port pin 7 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
6	PD6PD		Parallel port pin 6 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
5	PD5PD		Parallel port pin 5 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
4	PD4PD		Parallel port pin 4 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.

Table 1-81. Pull-Down Inhibit Register 3 (PDINHIBR3) Field Descriptions (continued)

Bit	Field	Value	Description
3	PD3PD		Parallel port pin 3 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
2	PD2PD		Parallel port pin 2 pull-down inhibit bit. Setting this bit to 1 disables the pin's internal pull-down.
		0	Pin pull-down is enabled.
		1	Pin pull-down is disabled.
1-0	Reserved	0	Reserved.

1.7.4 DMA Controller Configuration

The DSP includes four DMA controllers which allow movement of data among internal memory, external memory, and peripherals to occur without intervention from the CPU and in the background of CPU operation. Each DMA controller is programmed through a set of registers located in the DSP I/O space. Those registers and their function are described in the *TMS320VC5505/5504 DSP Direct Memory Access (DMA) Controller User's Guide* (SPRUFO9).

Several features of the DMA controllers (synchronization events and interrupts) are configured at the system level. The following sections provide more details on these features.

1.7.4.1 DMA Synchronization Events

The DMA controllers allow activity in their channels to be synchronized to selected events. The DSP supports 20 separate synchronization events and each channel can be tied to separate sync events independent of the other channels. Synchronization events are selected by programming the CHnEVT field in the DMAn channel event source registers (DMAnCESR1 and DMAnCESR2). The synchronization events available to each DMA controller are shown in Table 1-82.

Table 1-82. Channel Synchronization Events for DMA Controllers

CH*m*EVT Options	DMA0 Synchronization Event	DMA1 Synchronization Event	DMA2 Synchronization Event	DMA3 Synchronization Event
0000b	Reserved.	Reserved.	Reserved.	Reserved.
0001b	I2S0 transmit event.	I2S2 transmit event.	I2C transmit event.	I2S1 transit event.
0010b	I2S0 receive event.	I2S2 receive event.	I2C receive event.	I2S1 receive event.
0011b	Reserved.	Reserved.	SAR A/D event.	Reserved.
0100b	Reserved.	Reserved.	I2S3 transmit event.	Reserved.
0101b	MMC/SD0 transmit event.	UART transmit event.	I2S3 receive event.	Reserved.
0110b	MMC/SD0 receive event.	UART receive event.	Reserved.	Reserved.
0111b	MMC/SD1 transmit event.	Reserved.	Reserved.	Reserved.
1000b	MMC/SD1 receive event.	Reserved.	Reserved.	Reserved.
1001b	Reserved.	Reserved.	Reserved.	Reserved.
1010b	Reserved.	Reserved.	Reserved.	Reserved.
1011b	Reserved.	Reserved.	Reserved.	Reserved.
1100b	Timer 0 event.	Timer 0 event.	Timer 0 event.	Timer 0 event.
1101b	Timer 1 event.	Timer 1 event.	Timer 1 event.	Timer 1 event.
1110b	Timer 2 event.	Timer 2 event.	Timer 2 event.	Timer 2 event.
1111b	Reserved.	Reserved.	Reserved.	Reserved.

1.7.4.2 DMA Configuration Registers

There are several system-level registers that affect the operation of the DMA controllers (see Table 1-83). These registers are not part of the DMA controllers; they are part of the DSP system. The DMA interrupt flag and enable registers (DMAIFR and DMAIER) are used to control the interrupt generation of the four DMA controllers. In addition, there are two registers per DMA controller which control event synchronization in each channel; the DMAn channel event source registers (DMAnCESR1 and DMAnCESR2).

Table 1-83. System Registers Related to the DMA Controllers

CPU Word Address	Acronym	Register Description
1C30h	DMAIFR	DMA Interrupt Flag Register
1C31h	DMAIER	DMA Interrupt Enable Register
1C1Ah	DMA0CESR1	DMA0 Channel Event Source Register 1
1C1Bh	DMA0CESR2	DMA0 Channel Event Source Register 2
1C1Ch	DMA1CESR1	DMA1 Channel Event Source Register 1
1C1Dh	DMA1CESR2	DMA1 Channel Event Source Register 2
1C36h	DMA2CESR1	DMA2 Channel Event Source Register 1
1C37h	DMA2CESR2	DMA2 Channel Event Source Register 2
1C38h	DMA3CESR1	DMA3 Channel Event Source Register 1
1C39h	DMA3CESR2	DMA3 Channel Event Source Register 2

1.7.4.2.1 DMA Interrupt Flag Register (DMAIFR) [1C30h] and DMA Interrupt Enable Register (DMAIER) [1C31h]

The DSP includes two registers for controlling the channel interrupts of the four DMA controllers. Use the DMA interrupt enable register (DMAIER) to enable channel interrupts. At the end of a block transfer, if the DMA controller channel interrupt enable (DMA*n*CH*m*IE) bit is 1, an interrupt request is sent to the DSP CPU, where it can be serviced or ignored. Each channel can generate an interrupt, although all channel interrupts are aggregated into a single DMA interrupt.

To see which channel generated an interrupt, your program can read the DMA interrupt flag register (DMAIFR). The DMA controller channel interrupt flag (DMA*n*CH*m*IF) bits are set to 1 when a DMA channel generates an interrupt. Your program must manually clear the bits of DMAIFR by writing a 1 to its bits.

Figure 1-41. DMA Interrupt Flag Register (DMAIFR) [1C30h]

15	14	13	12	11	10	9	8
DMA3CH3IF	DMA3CH2IF	DMA3CH1IF	DMA3CH0IF	DMA2CH3IF	DMA2CH2IF	DMA2CH1IF	DMA2CH0IF
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
7	6	5	4	3	2	1	0
DMA1CH3IF	DMA1CH2IF	DMA1CH1IF	DMA1CH0IF	DMA0CH3IF	DMA0CH2IF	DMA0CH1IF	DMA0CH0IF
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 1-42. DMA Interrupt Enable Register (DMAIER) [1C31h]

15	14	13	12	11	10	9	8
DMA3CH3IE	DMA3CH2IE	DMA3CH1IE	DMA3CH0IE	DMA2CH3IE	DMA2CH2IE	DMA2CH1IE	DMA2CH0IE
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
7	6	5	4	3	2	1	0
DMA1CH3IE	DMA1CH2IE	DMA1CH1IE	DMA1CH0IE	DMA0CH3IE	DMA0CH2IE	DMA0CH1IE	DMA0CH0IE
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 1-84. DMA Interrupt Flag Register (DMAIFR) Field Descriptions

Bit	Field	Value	Description
15-0	DMA*n*CH*m*IF		Channel interrupt status bits.
		0	DMA controller *n,* channel *m* has not completed its block transfer.
		1	DMA controller *n,* channel *m* block transfer complete.

Table 1-85. DMA Interrupt Enable Register (DMAIER) Field Descriptions

Bit	Field	Value	Description
15-0	DMA*n*CH*m*IE		Channel interrupt enable bits.
		0	DMA controller *n,* channel *m* interrupt is disabled.
		1	DMA controller *n,* channel *m* interrupt is enabled.

1.7.4.2.2 DMAn Channel Event Source Registers (DMAnCESR1 and DMAnCESR2) [1C1Ah, 1C1Bh, 1C1Ch, 1C1Dh, 1C36h, 1C37h, 1C38h, and 1C39h]

When SYNCMODE = 1 in a channel's DMACH*m*TCR2, activity in the DMA controller is synchronized to a DSP event. You can specify the synchronization event used by the DMA channels be programming the CH*m*EVT bits of the DMA*n*CESR registers.

Each DMA controller contains two channel event source registers (DMA*n*CESR1 and DMA*n*CESR2). DMA*n*CESR1 controls the synchronization event for DMA*n* channel 0 and 1 while DMA*n*CESR2 controls the synchronization event for DMA*n* channel 2 and 3.

The synchronization events available to each DMA controller are shown in Table 1-82. Each channel in a DMA controller can have the same synchronization event.

Figure 1-43. DMA*n* Channel Event Source Register 1 (DMA*n*CESR1) [1C1Ah, 1C1Ch, 1C36h, and 1C38h]

15 12	11 8	7 4	3 0
Reserved	CH1EVT	Reserved	CH0EVT
R-0	RW-0	R-0	RW-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 1-44. DMA*n* Channel Event Source Register 2 (DMA*n*CESR2) [1C1Bh, 1C1Dh, 1C37h, and 1C39h]

15 12	11 8	7 4	3 0
Reserved	CH3EVT	Reserved	CH2EVT
R-0	RW-0	R-0	RW-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 1-86. DMA*n* Channel Event Source Register 1 (DMA*n*CESR1) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-8	CH1EVT	0-Fh	Channel 1 synchronization events. When SYNCMODE = 1 in a channel's DMACH*m*TCR2, the CH1EVT bits in the DMA*n*CESR registers specify the synchronization event for activity in the DMA controller. See Table 1-82 for a list of available synchronization event options.
7-4	Reserved	0	Reserved.
3-0	CH0EVT	0-Fh	Channel 0 synchronization events. when SYNCMODE = 1 in a channel's DMACH*m*TCR2, the CH0EVT bits in the DMA*n*CESR registers specify the synchronization event for activity in the DMA controller. See Table 1-82 for a list of available synchronization event options.

Table 1-87. DMA*n* Channel Event Source Register 2 (DMA*n*CESR2) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved.
11-8	CH3EVT	0-Fh	Channel 3 synchronization events. When SYNCMODE = 1 in a channel's DMACH*m*TCR2, the CH3EVT bits in the DMA*n*CESR registers specify the synchronization event for activity in the DMA controller. See Table 1-82 for a list of available synchronization event options.
7-4	Reserved	0	Reserved.
3-0	CH2EVT	0-Fh	Channel 2 synchronization events. When SYNCMODE = 1 in a channel's DMACH*m*TCR2, the CH2EVT bits in the DMA*n*CESR registers specify the synchronization event for activity in the DMA controller. See Table 1-82 for a list of available synchronization event options.

1.7.5 Peripheral Reset

All peripherals can be reset through software using the peripheral reset control register (PRCR). The peripheral software reset counter register (PSRCR) controls the number of system clock cycles that a peripheral reset signal will be asserted low once activated by the bits in PRCR.

To reset a peripheral or group of peripherals, follow these steps:

1. Set COUNT = 20h in PSRCR.
2. Initiate the desired peripheral reset by setting to 1 the bits of PRCR.

In some cases, a single reset is used for multiple peripherals. For example, PG4_RST controls the reset to the LCD controller, I2S2, I2S3, UART, and SPI.

1.7.5.1 Peripheral Software Reset Counter Register (PSRCR) [1C04h]

The Peripheral Software Reset Counter Register (PSRCR) is shown in Table 1-88 and described in Table 1-88.

Figure 1-45. Peripheral Software Reset Counter Register (PSRCR) [1C04h]

15		0
COUNT		
R/W-0		

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 1-88. Peripheral Software Reset Counter Register (PSRCR) Field Descriptions

Bit	Field	Value	Description
15-0	COUNT	0-FFFFh	Count bits. These bits specify the number of system clock (SYSCLK) cycles the software reset bits are asserted. When the software counter reaches 0, the software reset bits will be cleared to 0. Always initialize this field with 20h.

1.7.5.2 Peripheral Reset Control Register (PRCR) [1C05h]

The Peripheral Reset Control Register (PRCR) is shown in Figure 1-46 and described in Table 1-89.

Figure 1-46. Peripheral Reset Control Register (PRCR) [1C05h]

15	14	13	12	11	10	9	8
Reserved							
R-0							

7	6	5	4	3	2	1	0
PG4_RST	Reserved	PG3_RST	DMA_RST	USB_RST	Reserved	PG1_RST	I2C_RST
R/W-0	R-0	R/W-0	R/W-0	R/W-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 1-89. Peripheral Reset Control Register (PRCR) Field Descriptions

Bit	Field	Value	Description
15-8	Reserved	0	Reserved. Always write 0 to these bits.
7	PG4_RST		Peripheral group 4 software reset bit. Drives the LCD, I2S2, I2S3, UART, and SPI reset signal.
		0	Reset deasserted, modules out of reset.
		1	Reset asserted, modules in reset.
6	Reserved	0	Reserved, always write 0 to this bit.
5	PG3_RST		Peripheral group 3 software reset bit. Drives the MMC/SD0, MMC/SD1, I2S0, and I2S1 reset signal.
		0	Reset deasserted, modules out of reset.
		1	Reset asserted, modules in reset.
4	DMA_RST		DMA software reset bit. Drives the reset signal to the DMA controllers.
		0	Reset deasserted, modules out of reset.
		1	Reset asserted, modules in reset.
3	USB_RST		USB software reset bit. Drives the USB reset signal.
		0	Reset deasserted, module out of reset.
		1	Reset asserted, module in reset.
2	Reserved	0	Reserved. Always write 0 to these bits.

Table 1-89. Peripheral Reset Control Register (PRCR) Field Descriptions (continued)

Bit	Field	Value	Description
1	PG1_RST		Peripheral group 1 software reset bit. Drives the EMIF and timers reset signal.
		0	Reset deasserted, modules out of reset.
		1	Reset asserted, modules in reset.
0	I2C_RST		I2C software reset bit. Drives the I2C reset signal.
		0	Reset deasserted, module out of reset.
		1	Reset asserted, module in reset.

1.7.6 EMIF and USB Byte Access

The CPU cannot generate 8-bit accesses to its data or I/O space. In some cases, it is necessary to access a single byte of data. For example, when writing byte commands to NAND Flash devices or when enabling the EMIF SDRAM self-refresh mode (to enable this mode you must only write to the upper byte in the SDRAM configuration register 2 to avoid triggering the SDRAM auto-initialization procedure).

For these situations, the upper or lower byte of a CPU word access can be masked using the BYTEMODE bits of the EMIF system control register (ESCR) and the USB system control register (USBSCR). The BYTEMODE bits of ESCR only affect accesses to the external memory and the EMIF registers. The BYTEMODE bits of USBSCR only affect CPU accesses to the USB registers. Table 1-90 and Table 1-91 summarize the effect of the BYTEMODE bits for different CPU operations.

NOTE: The BYTEMODE bits of the EMIF system control register should only be used for controlling CPU accesses to NAND Flash devices and EMIF registers.

Table 1-90. Effect of BYTEMODE Bits on EMIF Accesses

BYTEMODE Setting	CPU Access to EMIF Register	CPU Access To External Memory
BYTEMODE = 00b (16-bit word access)	Entire register contents are accessed	ASIZE = 01b (16-bit data bus): EMIF generates a single 16-bit access to external memory for every CPU word access. ASIZE = 00b (8-bit data bus): EMIF generates two 8-bit accesses to external memory for every CPU word access.
BYTEMODE = 01b (8-bit access with high byte selected)	Only the upper byte of the register is accessed.	ASIZE = 01b (16-bit data bus): EMIF generates a 16-bit access to external memory for every CPU word access; only the high byte of the EMIF data bus is used. ASIZE = 00b (8-bit data bus): EMIF generates a single 8-bit access to external memory for every CPU word access.
BYTEMODE = 10b (8-bit access with low byte selected)	Only the lower byte of the register is accessed.	ASIZE = 01b (16-bit data bus): EMIF generates a 16-bit access to external memory for every CPU word access; only the low byte of the EMIF data bus is used. ASIZE = 00b (8-bit data bus): EMIF generates a single 8-bit access to external memory for every CPU word access.

The USB system control register (USBSCR) is described in Section 1.5.5.4.2.

Table 1-91. Effect of USBSCR BYTEMODE Bits on USB Access

BYTEMODE Setting	CPU Access to USB Register
BYTEMODE = 00b (16-bit word access)	Entire register contents are accessed
BYTEMODE = 01b (8-bit access with high byte selected)	Only the upper byte of the register is accessed
BYTEMODE = 10b (8-bit access with low byte selected)	Only the lower byte of the register is accessed

1.7.6.1 EMIF System Control Register (ESCR) [1C33h]

The EMIF system control register (ESCR) is shown in Figure 1-47 and described in Table 1-92.

Figure 1-47. EMIF System Control Register (ESCR) [1C33h]

15	2	1	0
Reserved		BYTEMODE	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 1-92. EMIF System Control Register (ESCR) Field Descriptions

Bit	Field	Value	Description
15-2	Reserved	0	Reserved.
1-0	BYTEMODE		EMIF byte mode select bits. These bits control CPU data and program accesses to external memory as well as CPU accesses the EMIF registers.
		0	Word accesses by the CPU are allowed.
		1h	Byte accesses by the CPU are allowed (high byte is selected).
		2h	Byte accesses by the CPU are allowed (low byte is selected).
		3h	Reserved.

1.7.7 EMIF Clock Divider Register (ECDR) [1C26h]

The EMIF clock divider register (ECDR) controls the input clock frequency to the EMIF module. When EDIV = 1 (default), the EMIF operates at the same clock rate as the system clock (SYSCLK). When EDIV = 0, the EMIF operates at half the clock rate of the system clock.

The EMIF clock divider register (ECDR) is shown in Figure 1-48 and described in Table 1-93.

Figure 1-48. EMIF Clock Divider Register (ECDR) [1C26h]

15	1	0
Reserved		EDIV
R-0		R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 1-93. EMIF Clock Divider Register (ECDR) Field Descriptions

Bit	Field	Value	Description
15-1	Reserved	0	Reserved.
0	EDIV		EMIF clock divider select bits. The EMIF module can internally divide its input peripheral clock. When this bit is set to 0, the EMIF operates at half the clock rate of its peripheral clock. When this bit is set to 1 the EMIF operates at the full rate of its peripheral clock.
		0	EMIF operates at half the peripheral clock rate.
		1	EMIF operates at the same rate as the peripheral clock.

Revision History

This revision history reflects the changes made to this document from its original version.

Table A-1. Revision History

See	Revision
Table 1-40	Clock Generator Control Register 3 Field Descriptions: Updated bit values.
Table 1-82	Updated *Channel Synchronization Events for DMA Controllers*.

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