TMS320DM36x Digital Media System-on-Chip (DMSoC) Power Management and Real-Time Clock Subsystem (PRTCSS)

User's Guide

Literature Number: SPRUFJ0B
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About this Manual

This document provides a functional description of the Power Management and Real-Time Clock Subsystem (PRTCSS) in the TMS320DM36x Digital Media System-on-Chip (DMSoC) and PRTC interface (PRTCIF).

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320DM36x Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the internet.

SPRUFG5 — ***TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide*** This document describes the ARM Subsystem in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the components of the ARM Subsystem, the peripherals, and the external memories.

SPRUFG8 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Video Processing Front End (VPFE) Users Guide*** This document describes the Video Processing Front End (VPFE) in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFG9 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Video Processing Back End (VPBE) Users Guide*** This document describes the Video Processing Back End (VPBE) in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH0 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) 64-bit Timer Users Guide*** This document describes the operation of the software-programmable 64-bit timers in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH1 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Serial Peripheral Interface (SPI) Users Guide*** This document describes the serial peripheral interface (SPI) in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communication between the DMSoC and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EPROMs and analog-to-digital converters.

SPRUFH2 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Asynchronous Receiver/Transmitter (UART) Users Guide*** This document describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The UART peripheral performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data received from the CPU.

SPRUFH3 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Inter-Integrated Circuit (I2C) Peripheral Users Guide*** This document describes the inter-integrated circuit (I2C) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The I2C peripheral provides an interface between the DMSoC and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus.

SPRUFH5 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Multimedia Card (MMC)/Secure Digital (SD) Card Controller Users Guide*** This document describes the multimedia card (MMC)/secure digital (SD) card controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH6 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Pulse-Width Modulator (PWM) Users Guide*** This document describes the pulse-width modulator (PWM) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH7 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Real-Time Out (RTO) Controller Users Guide*** This document describes the Real Time Out (RTO) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH8 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) General-Purpose Input/Output (GPIO) Users Guide*** This document describes the general-purpose input/output (GPIO) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.

SPRUFH9 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Serial Bus (USB) Controller Users Guide*** This document describes the universal serial bus (USB) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The USB controller supports data throughput rates up to 480 Mbps. It provides a mechanism for data transfer between USB devices and also supports host negotiation.

SPRUFI0 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Enhanced Direct Memory Access (EDMA) Controller Users Guide*** This document describes the operation of the enhanced direct memory access (EDMA3) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The EDMA controller's primary purpose is to service user-programmed data transfers between two memory-mapped slave endpoints on the DMSoC.

SPRUFI1 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Asynchronous External Memory Interface (EMIF) Users Guide*** This document describes the asynchronous external memory interface (EMIF) in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The EMIF supports a glueless interface to a variety of external devices.

SPRUFI2 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) DDR2/Mobile DDR (DDR2/mDDR) Memory Controller Users Guide*** This document describes the DDR2/mDDR memory controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The DDR2/mDDR memory controller is used to interface with JESD79D-2A standard compliant DDR2 SDRAM and mobile DDR devices.

SPRUFI3 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Multibuffered Serial Port Interface (McBSP) User's Guide*** This document describes the operation of the multibuffered serial host port interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The primary audio modes that are supported by the McBSP are the AC97 and IIS modes. In addition to the primary audio modes, the McBSP supports general serial port receive and transmit operation.

SPRUFI4 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Host Port Interface (UHPI) User's Guide*** This document describes the operation of the universal host port interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI5 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Ethernet Media Access Controller (EMAC) User's Guide*** This document describes the operation of the ethernet media access controller interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI7 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Analog to Digital Converter (ADC) User's Guide*** This document describes the operation of the analog to digital conversion in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI8 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Key Scan User's Guide*** This document describes the key scan peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI9 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Voice Codec User's Guide*** This document describes the voice codec peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). This module can access ADC/DAC data with internal FIFO (Read FIFO/Write FIFO). The CPU communicates to the voice codec module using 32-bit-wide control registers accessible via the internal peripheral bus.

SPRUFJ0 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Power Management and Real-Time Clock Subsystem (PRTCSS) User's Guide*** This document provides a functional description of the Power Management and Real-Time Clock Subsystem (PRTCSS) in the TMS320DM36x Digital Media System-on-Chip (DMSoC) and PRTC interface (PRTCIF).

SPRUGG8 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Face Detection User's Guide*This document describes the face detection capabilities for the TMS320DM36x Digital Media System-on-Chip (DMSoC).

TMS320DM36x DMSoC Power Management and Real-Time Clock Subsystem (PRTCSS)

1 Purpose of the PRTC Subsystem

The Power Management and Real Time Clock Subsystem (PRTCSS) is used for calendar applications and to manage the DM36x power supply. The PRTCSS has an independent power supply, and hence can remain ON even while the rest of the DM36x power supply is turned OFF. Therefore, the PRTCSS can be operated without supplying the power supply of the entire device. The PRTCSS has a real-time clock, timers, general-purpose I/Os, and a simple sequencer.

1.1 Features of the PRTCSS

The PRTCSS has the following features:

- General purpose I/O (GPIO) with anti-chattering 4-output pins (PWRCTRO[3:0]), and 7-Input/Output pins (PWRCTRIO[6:0])
- Simple real-time clock (RTC) count, up to 89 years
- Alarm event generated to check the RTC count
- Watch-dog timer
- 16-bit simple timer

1.2 Signal Descriptions

The PRTCSS signal descriptions are shown in Table 1. Refer to the *TMS320DM365 DMSoC Data Manual* (SPRS457) for more information on these pins.

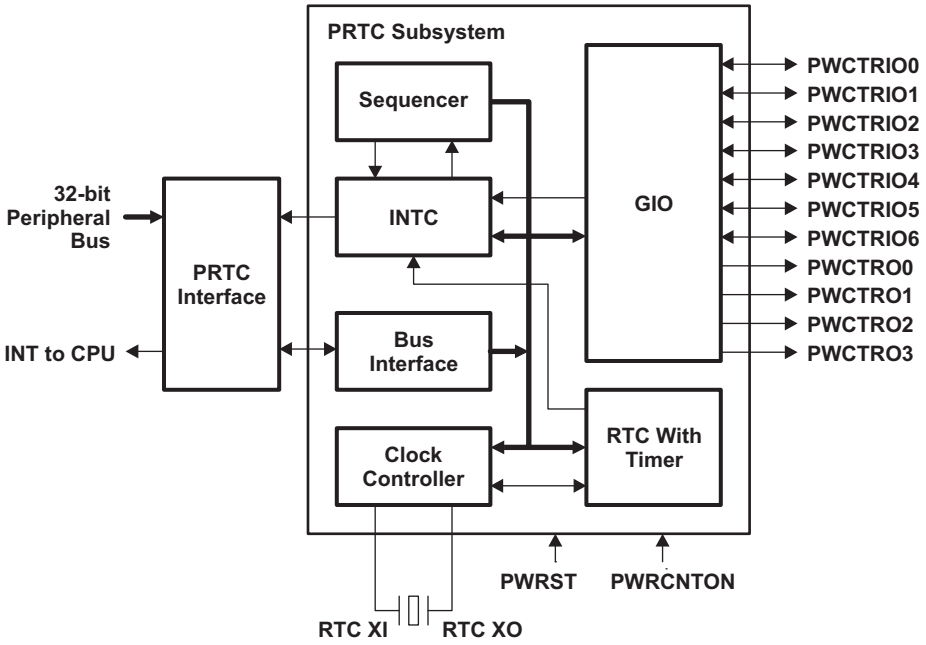
Table 1. PRTCSS Signals

Signal name	Signal Type	Function
PWCTRIO0	Input/Output	General Input / Output Signal 0
PWCTRIO1	Input/Output	General Input / Output Signal 1
PWCTRIO2	Input/Output	General Input / Output Signal 2
PWCTRIO3	Input/Output	General Input / Output Signal 3
PWCTRIO4	Input/Output	General Input / Output Signal 4
PWCTRIO5	Input/Output	General Input / Output Signal 5
PWCTRIO6	Input/Output	General Input / Output Signal 6
PWCTRO0	Output	General Output Signal 0
PWCTRO1	Output	General Output Signal 1
PWCTRO2	Output	General Output Signal 2
PWCTRO3	Output	General Output Signal 3
RTCXI	Input	Crystal Input for PRTCSS oscillator
RTCXO	Output	Crystal Output for PRTCSS oscillator
PWRST	Input	Reset signal for PRTCSS
PWRCNTON	Input	Reset pin for system power sequencing

1.3 Configuration of PRTCSS and PRTCIF

A block diagram of the PRTC subsystem module is shown in Figure 1 .

Figure 1. PRTC Subsystem Block Diagram



The DM36x device can access the PRTCIF registers; however, it cannot directly access the PRTCSS registers.

Table 2 shows the various PRTCSS configuration bus masters and slaves.

Table 2. PRTCSS Configuration Bus Masters and Slaves

PRTCSS Masters	PRTCSS Slaves
PRTCIF	CLKC, INTC, GIO, RTC with Timer

1.4 PRTCSS Reset and Configuration

The PWRST and PWRCNTON input pins control the reset of the module. PRTCSS can operate in either normal mode or external reset mode.

For normal mode operation, see Section 1.4.1; for external reset mode operation, see Section 1.4.2.

1.4.1 Normal Mode

In the normal mode of operation, the PRTCSS submodules' reset is controlled by the state of PWCTRO0 pin. When the PWCTRO0 pin is in logic level 0, then the PRTCSS submodules will be in reset and the DM36x device will not be able to access the PRTCSS registers.

When the PRTCSS module operates in normal mode, irrespective of the whether the PWCTRO0 is connected to the RESET of the device or not, the DM36x device must reset the WDT of PRTCSS so that the PWCTRO0 pin state will be retained at logic 1.

This normal mode of operation of PRTCSS will be the preferred mode of operation, where the PRTCSS is powered with backup power and where the PRTCSS calendar/RTC contents will be retained even when the DM36x is reset. In this case, the PRTCSS submodule must be battery-powered.

Figure 2 explains the recommended reset sequencing of PRTCSS using the PWRST and PWRCNTON input pins. In this mode the sequencer and the PRTCSS block are powered ON. The sequencer executes the initialization sequence as discussed in Section 3.4.2. In normal mode, the DM36x reset is controlled by the PRTCSS (through PWCTRO0). The main device must reset the PRTCSS WDT using the PRTCIF to complete the initialization sequence. Failure to reset the PRTCSS WDT will result in a RESET of the DM36x device when the PRTCSS WDT expires. Figure 3 shows an example of the PRTCSS external connections for the DM36x power lines and control signals in the normal mode. See Section 3 for an overview of each major block of the PRTCSS.

1.4.1.1 PRTCSS Initialization Sequence in Normal Mode

The following section provides the procedure for initializing the PRTCSS in normal mode:

1. Ensure the PRTCSS module is in reset by clearing the PWRST and PWRCNTON signals to 0.
2. Provide the power for the PRTCSS block.
3. Set PWCTRIO0 pin to '0'.
4. Input '1' to the reset signal for PRTCSS (PWRST) after the 32.768 kHz oscillator is stable.
5. Input '1' to the reset pin for system power sequencing (PWRCNTON) to start the sequencer of the power control block.

   The Sequencer performs the following steps:
6. Outputs '1' on the PWCTRO1 pin. This signal must be used to control the power IC that supplies power to the DM36x device.
7. Outputs '1' on the PWCTRO0 pin. This signal connects to the DM36x RESETz pin after the stable time of the main clock oscillator.
8. Enables the PRTCSS WDT.
9. Outputs '0's (after expiration of WDT (16 sec)) on the PWCTRO0/1 to control power off.
   The DM36x device must stop the PRTCSS WDT by clearing the WEN bit in the RTC control register (RTC_CTRL) within 16 sec after DM36x comes out of reset. Otherwise, the sequencer will execute the power-off sequence for the device.

Figure 2. PRTCSS Initialization Sequence - Normal Mode

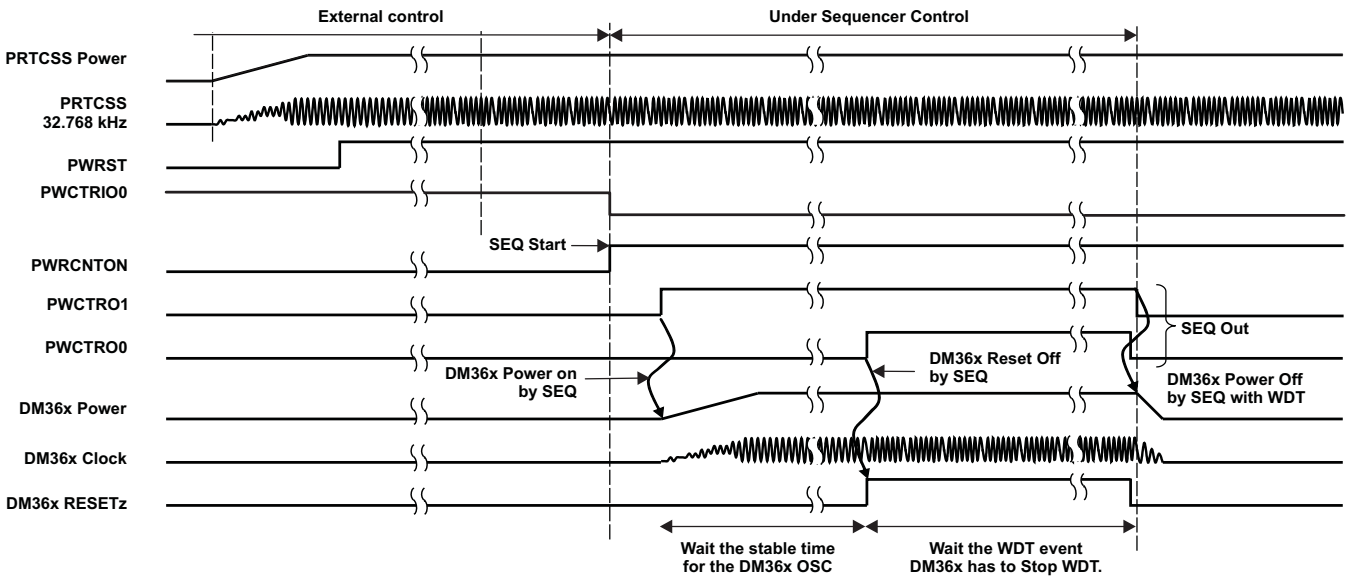
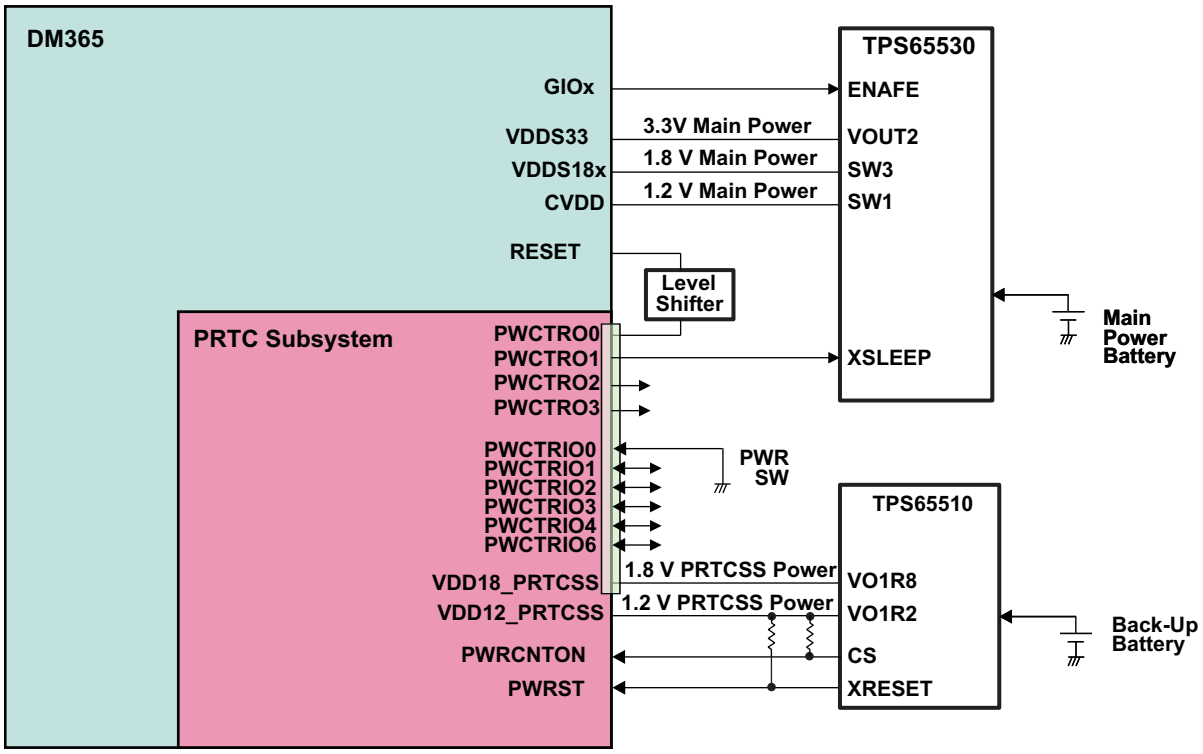


Figure 3. PRTCSS External Circuit Example for Normal Mode



1.4.2 External Reset Mode

The PRTCSS will work in this mode if the PWRCNTON input pin is held at 1 and the PWRST pin is held at 0. Power on/off and reset for the DM36x device should be done externally, as the PRTCSS has no control over them. The device reset signal (RESETz) will reset the PRTCSS. The SEQ cannot be used in this mode.

1.5 Industry Standards Compliance Statement

The PRTCSS module does not conform to any recognized industry standards.

1.6 Interrupt Support

The PRTCIF combines an interrupt from the PRTCSS INTC and the PRTCIF and generates a single interrupt to the DM36x. For further details on the PRTCSS INTC refer to Section 3.2, and for information on the PRTCIF DMA completion interrupt, refer to Section 2.3.

Multiple interrupt sources can be assigned to the same CPU interrupt. To identify the interrupt source, the CPU reads the PRTCIF interrupt flag register (PRTCIF_INTFLG). For more information on the System Control Module and ARM Interrupt Controller, refer to the*TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem User's Guide* (SPRUFG5).

1.7 Clock Controller

1.7.1 Clock Source Selection

The PRTCSS module can operate from two clock sources. Clock source selection for the PRTCSS module is based on the configuration of the PRTCCLKS field of the PERI_CLKCTL register. For more information on device clocking, refer to the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem User's Guide* (SPRUFG5).

The CLKC_CNT register is used to set WDT and Peripheral Clocks divider values.

1.7.2 Clock Controller

CLKC_CNT register is used to control the clock divider values for PERI_CLK and WDT clock. Divide values range from 1 to 4096.

1.8 EDMA Event Support

The PRTCSS module does not generate an EDMA event.

1.9 Emulation Considerations

The PRTCSS module controller is not affected by emulation halt events, such as breakpoints.

2 PRTC Interface (PRTCIF)

The PRTC interface (PRTCIF) is the bridge to connect the 32-bit DM36x bus to the 8-bit PRTCSS bus. The device can access the PRTCSS module through the PRTCIF.

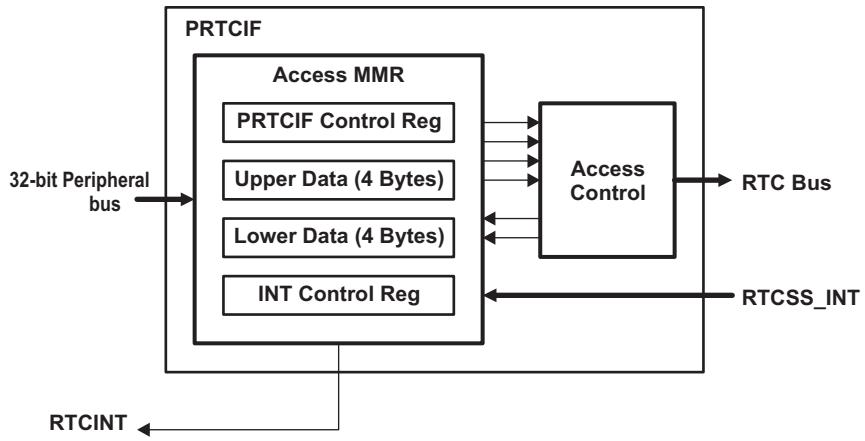
2.1 Features of the PRTC Interface

The PRTCIF interface has the following features:

- PRTCSS memory map space is accessed through PRTCIF registers
- Busy bit that indicates the data access status
- Interrupt generated on the read/write complete
- Synchronizers for PRTCSS interrupt with the DM36x interrupt

Figure 4 shows the functional diagram for the PRTCIF interface.

Figure 4. PRTCIF Functional Diagram



2.2 PRTC Interface Functional Operation

The following steps provides the functional operation of the PRTC Interface:

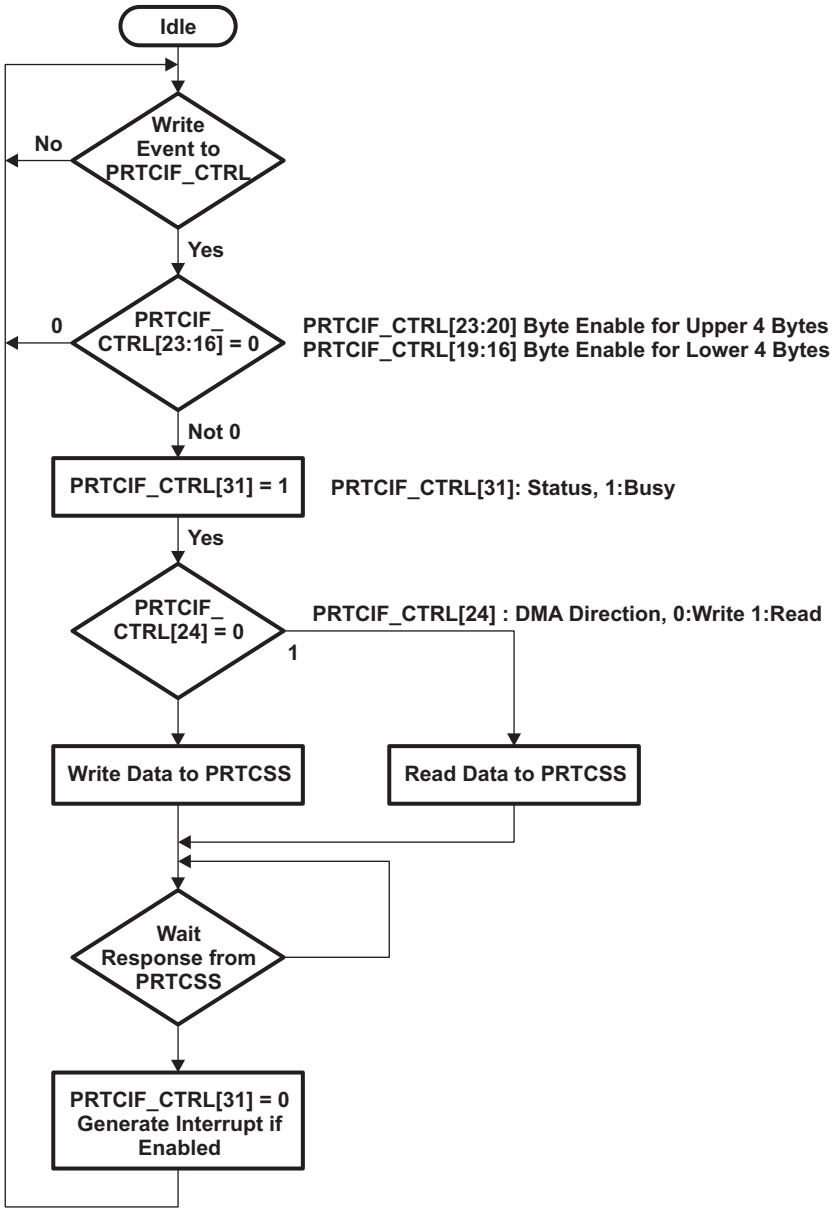
- Wait until the BUSY bit in the PRTCIF control register (PRTCIF_CTRL) is "0"
- Configure the desired data format in the PRTCIF control register (PRTCIF_CTRL)
  - Program the data access direction in the DIR bit
  - Program the data access size in the SIZE bit
  - Program the access byte enable for PRTCIF_UDATA in the BENU bits
  - Program the access byte enable for PRTCIF_LDATA in the BENL bits
- Set the PRTCSS target memory address that the PRTCIF needs to access read/write by configuring the ADRS bits in the PRTCIF control register (PRTCIF_CTRL)
- Enable the desired interrupts, if any, in the PRTCIF interrupt enable register (PRTCIF_INTEN)

- If DIR is 1, then:
  - Write the first 4 bytes of PRTCSS data through the PRTCIF access lower data (PRTCIF_LDATA) register
  - If SIZE is 1, then write the second 4 bytes of PRTCSS data through the PRTCIF access upper data (PRTCIF_UDATA) register
- If DIR is 0, then
  - Read the first 4 bytes of PRTCSS data through the PRTCIF access lower data (PRTCIF_LDATA) register
  - If SIZE is 1, then read the second 4 bytes of PRTCSS data through the PRTCIF access upper data (PRTCIF_UDATA) register
- Wait until the BUSY bit in the PRTCIF control register (PRTCIF_CTRL) is "0" before updating the PRTCIF_UDATA/PRTCIF_LDATA
- PRTCIF generates an interrupt once the DMA access to PRTCSS from PRTCIF is completed

2.2.1 Flow of the PRTCIF Function

Figure 5 shows the flow of the PRTCIF function.

Figure 5. PRTCIF Function Flow



A Must not update the PRTCIF_UDATA/PRTCIF_LDATA registers during PRTCIF_CTRL[31] == '1'(PRTCIF is Busy)

B There will be no response from the PRTCSS module if clocks are not supplied to PRTCSS

2.3 Interrupt Status of PRTCSS Events

The PRTCSS_INT_FLAG and PRTCIF_INT_FLAG bits in the PRTCIF interrupt flag register (PRTCIF_INTFLG) indicate the interrupt for PRTCSS events and the access state of the PRTCIF interface, respectively.

The PRTCIF interface generates the following interrupt events:

- PRTCSS_INT_FLAG: PRTCSS interrupt flag
  PRTCSS_INT_FLAG = 1 in the PRTCIF interrupt flag register (PRTCIF_INTFLG) indicates there is a PRTCSS interrupt to PRTCIF.
- PRTCIF_INT_FLAG: PRTCIF interrupt flag
  PRTCIF_INT_FLAG = 1 in the PRTCIF Interrupt Flag Register (PRTCIF_INTFLG) indicates the end of DMA access to PRTCSS from PRTCIF

2.4 Power Management

The PRTCIF interface can be placed in reduced-power modes to conserve power during periods of low activity. For detailed information on power management procedures using the PSC, see the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Users Guide* (SPRUFG5).

3 PRTCSS Modules

3.1 General Purpose I/O (GIO)

The GIO module provides dedicated pins that can be configured as either inputs or outputs. When configured as an output, you can write to an internal register to control the state of the output pin. When configured as an input, you can detect the state of the input by reading the state of an internal register.

NOTE: For detailed information on the GIO module and registers, see Section 4.2.

The GIO module supports the following features:

- Basic GIO function for each of the 11 pins
  - PWCTRO[3:0] pins are used as output only
  - PWCTRIO[6:0] pins are used as either input or output
- Anti-chattering for input pins
- PWCTRO2 can be configured to output 32.768 KHz Clock or PWM
- Two interrupt enable bits control the GIO functions

3.1.1 Using the GIO Signal as an Output or Input

GIO signals are configured to operate as input or output pins by clearing the value to the GO2_FUNC bit of the general purpose in/out function register (GIO_FUNC).

3.1.1.1 Configuring a GIO Output Signal

To configure a given GIO signal as an output, clear the bit in GIO_DIR register that is associated with the desired GIO signal.

The GIO output data register (GIO_OUT) contains the current state of the output signals. Reading GIO_OUT returns the output state (not necessarily the actual signal state) since some signals may be configured as inputs. The actual signal state is read using the GIO input data register (GIO_IN) associated with the desired GIO signal. GIO_IN contains the actual logic state on the external signal.

To modify the bit in the GIO_OUT register associated with the desired GIO signal, use the read-modify-write operation. The logic states driven on the GIO output signals match the logic values written to all bits in the GIO_OUT register. For GIO signals configured as inputs, the values written to the GIO_OUT bits have no effect.

3.1.1.2 Configuring a GIO Input Signal

To configure a given GIO signal as an input, set the bit in GIO_DIR that is associated with the desired GIO signal.

The current state of the GIO signals is read using the GIO input data register (GIO_IN). For GIO signals configured as inputs, reading GIO_IN returns the state of the input signal synchronized to the GIO peripheral clock.

For GIO signals configured as outputs, reading GIO_IN returns the output value being driven by the device.

Some signals may utilize open-drain output buffers for wired-logic operations. For open-drain GIO signals, reading GIO_IN returns the wired-logic value on the signal (which will not be driven by the device alone). Information on any signals using open-drain outputs is available in the device data manual.

3.1.2 Configuring GIO Interrupt Edge Triggering

Each GIO interrupt source can be configured to generate an interrupt on the GIO signal rising edge, falling edge, both edges, or neither edge (no event). The edge detection is synchronized to the GIO peripheral module clock.

The following registers control the configuration of the GIO interrupt edge detection:

- The GIO rise interrupt enable register (GIO_RISE_INT_ENA) enables GIO interrupts on the occurrence of a rising edge on the GIO signal.
- The GIO fall interrupt enable register (GIO_FALL_INT_ENA) enables GIO interrupts on the occurrence of a falling edge on the GIO signal.

To configure a GIO interrupt to occur only on rising edges of the GIO signal:

- Write a logic 1 to the associated bit in GIO_RISE_INT_ENA

To configure a GIO interrupt to occur only on falling edges of the GIO signal:

- Write a logic 1 to the associated bit in GIO_FALL_INT_ENA

To configure a GIO interrupt to occur on both the rising and falling edges of the GIO signal:

- Write a logic 1 to the associated bit in GIO_RISE_INT_ENA
- Write a logic 1 to the associated bit in GIO_FALL_INT_ENA

To disable a specific GIO interrupt:

- Write a logic 0 to the associated bit in GIO_RISE_INT_ENA
- Write a logic 0 to the associated bit in GIO_FALL_INT_ENA

You must clear the GIO_RISE_INT_FLG and GIO_FALL_INT_FLG registers before configuring the GIO_RISE_INT_ENA or GIO_FALL_INT_ENA register. These detectors for the GIO rise/fall edge are active at the input direction. So, GIO_RISE_INT_FLG and GIO_FALL_INT_FLG registers keep the change conditions of input pins. When the flag is '1' and the interrupt enable is set, the interrupt is generated.

3.1.2.1 GIO Interrupt Status

The status of GIO interrupt events can be monitored by reading the GIO interrupt flag register for the rise edge (GIO_RISE_INT_FLG) and GIO interrupt flag register for fall edge (GIO_FALL_INT_FLG). Pending GIO interrupts are indicated with a logic 1 in the associated bit position; interrupts that are not pending are indicated with a logic 0. For individual GIO interrupts that are directly routed to the INTC. Pending GIO interrupt flags can be cleared by writing a logic 1 to the associated bit position in GIO_RISE_INT_FLG and GIO_FALL_INT_FLG.

3.1.3 Using the PWCTRO2 Signal as a Clock or PWM Output Function

3.1.3.1 Configuring PWCTRO2 Signal as Clock Output

To configure the PWCTRO2 signal as a clock output, write the appropriate value to the GO2_FUNC bit of the general purpose in/out function register (GIO_FUNC). In this configuration, GIO will drive the PWCTRO2 pin as a 32.768 KHz clock out function.

3.1.3.2 Configuring PWCTRO2 Signal as PWM Output Function

To configure the PWCTRO2 signal as PWM output, write the appropriate value to the GO2_FUNC bit of general purpose in/out function register (GIO_FUNC). In this configuration, GIO will drive the PWCTRO2 pin as a PWM out function. The PWM width can be configured, as shown in Table 3, by writing to the PWM_WIDTH bits of the general purpose in/out function register (GIO_FUNC).

Table 3. PWM Output Width

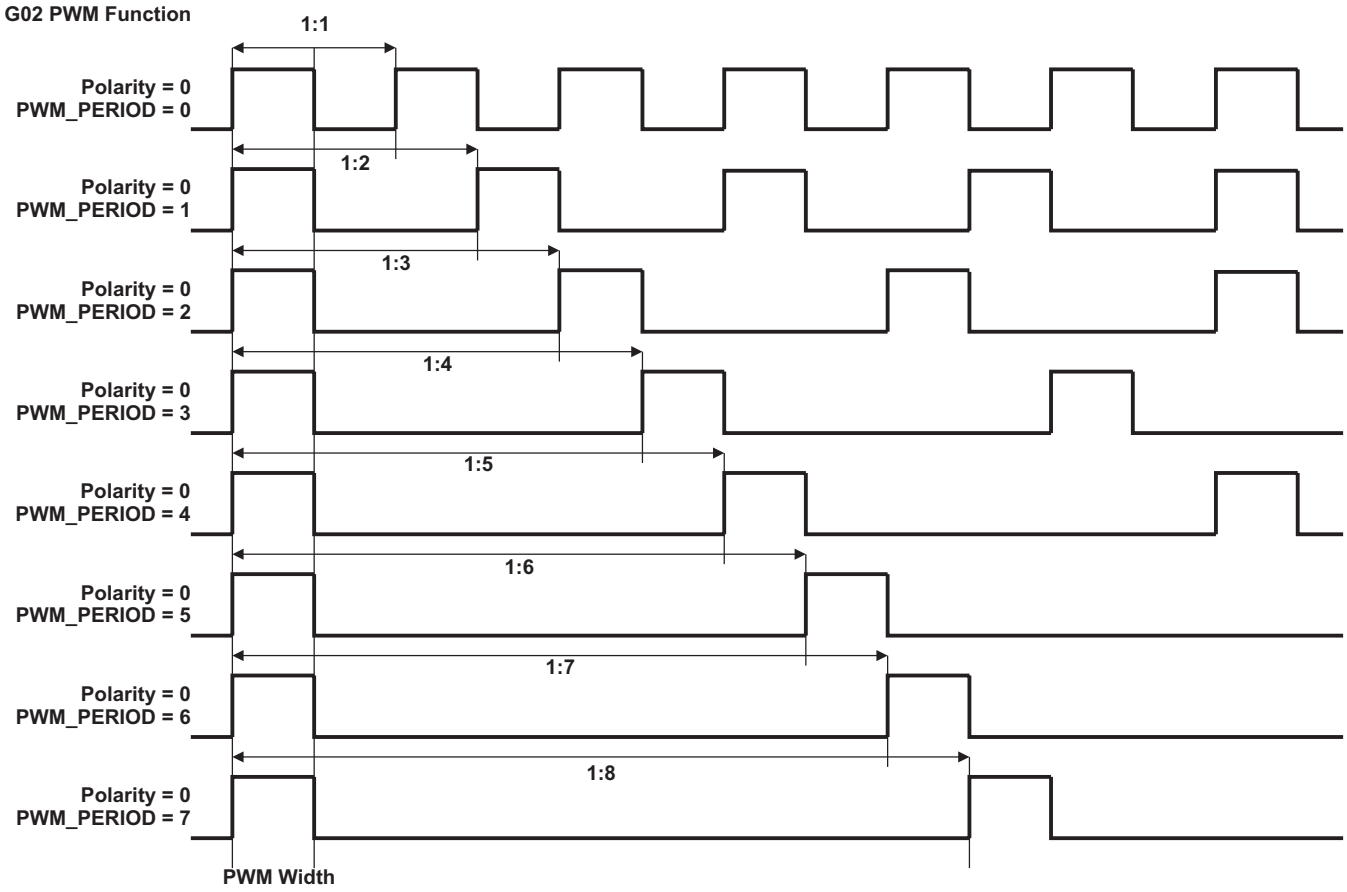
Clk_Peri = Frequency/CLKC_PERI			**PWM Width (mSec) = ($2^{(PWM\_WIDTH + 4)}$)/ Clk_Peri**							
Freqency	CLKC_PERI	Clk_Peri (Hz)	PWM_WIDTH = 00	PWM_WIDTH = 01	PWM_WIDTH = 02	PWM_WIDTH = 03	PWM_WIDTH = 04	PWM_WIDTH = 05	PWM_WIDTH = 06	PWM_WIDTH = 07

Table 3. PWM Output Width (continued)

Clk_Peri = Frequency/CLKC_PERI			PWM Width (mSec) = ($2^{(PWM\_WIDTH + 4)}$)/ Clk_Peri							
32,768 Hz	1	32,768	0.49	0.98	1.95	3.91	7.81	15.63	31.25	62.50
	2	16,384	0.98	1.95	3.91	7.81	15.63	31.25	62.50	125
	4	8,192	1.95	3.91	7.81	15.63	31.25	62.50	125	250
	8	4,096	3.91	7.81	15.63	31.25	62.50	125	250	500
	16	2,048	7.81	15.63	31.25	62.50	125	250	500	1,000
	32	1,024	15.63	31.25	62.50	125	250	500	1,000	2,000
	64	512	31.25	62.50	125	250	500	1,000	2,000	4,000
	128	256	62.50	125	250	500	1,000	2,000	4,000	8,000
	256	128	125	250	500	1,000	2,000	4,000	8,000	16,000
	512	64	250	500	1,000	2,000	4,000	8,000	16,000	32,000
	1024	32	500	1,000	2,000	4,000	8,000	16,000	32,000	64,000
	2048	16	1,000	2,000	4,000	8,000	16,000	32,000	64,000	128,000
	4096	8	2,000	4,000	8,000	16,000	32,000	64,000	128,000	256,000

You can configure the PWM period by writing PWM_PERIOD bits of the general purpose in/out function register (GIO_FUNC) and the same has been shown in Figure 6 for a given PWM width.

Figure 6. GO2 PWM Output Period



3.2 PRTCSS INTC

The PRTCSS module outputs a single interrupt RTCINT that is routed to the DM36x interrupt controller. The INTC supports interrupts from GIO signals and interrupts from RTC signals.

The INTC module generates an interrupt to DM36x for GIO and RTC if enabled. Interrupt mapping from the GIO and RTC to the DM36x is shown in Section 4.

3.2.1 Configuring the INTC Interrupt

The following registers control the configuration of the INTC interrupt to DM36x:

- The EXT Event Enable 0 register (INTC_EXTENA0) enables INTC interrupts to DM36x on the occurrence of interrupts from the GIO signals and DM36x.
- The EXT Event Enable 1 register (INTC_EXTENA1) enables INTC interrupts to DM36x on the occurrence of interrupts from the RTC signals.

3.2.2 INTC Interrupt Status

The status of INTC interrupt events can be monitored by reading the Interrupt flag 0 register (INTC_FLG0) and Interrupt flag 1 register (INTC_FLG1). Pending INTC interrupts are indicated with a logic 1 in the associated bit position; interrupts that are not pending are indicated with a logic 0.

PRTCSS individual INTC interrupts are not directly routed to the ARM device. ARM has to check the individual interrupt status by reading the INTC_FLG0 and INTC_FLG1 registers using the PRTCIF. Pending INTC interrupt flags can be cleared by writing a logic 1 to the associated module Flag bit.

For detailed information on INTC_FLG0 and INTC_FLG1, see Section 4.

3.3 Real Time Clock (RTC)

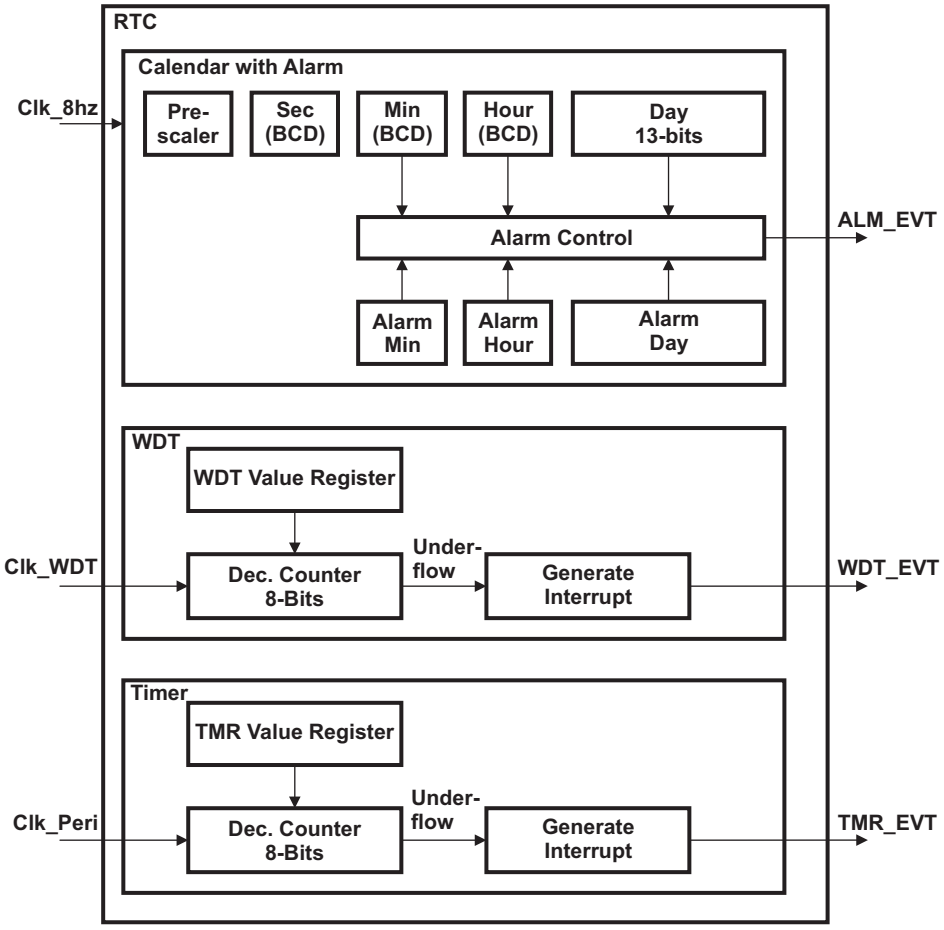
The RTC module supports the following features:

- Simple RTC is configured to count the following
  - Sec : 0 - 59 : BCD count
  - Min : 0 - 59 : BCD count
  - Hour : 0 - 23 : BCD count
  - Day : 0 - 0x7FFF(32767) : binary count (over 89 years)
- Alarm
  - Generate event signal with RTC count value
- Free running watchdog timer
  - 8-bit decrement counter with re-load control bit
  - Initial load value is "FF." Initial period is 256 x 16Hz : 16sec
  - When count value reaches 0, generate the event and reload a specified period value
- 16-bit decrement timer
  - One-shot, free-run mode
  - Generate event signal to INTC

3.3.1 RTC Functional Block Diagram

The RTC module functional block diagram is shown in Figure 7.

Figure 7. RTC Functional Block Diagram



3.3.2 RTC Initialization

The following procedures will initialize the Timer , Watch Dog Timer, and Calendar in RTC.

3.3.2.1 Initializing the Timer

To initialize the RTC in timer mode:

- Wait for the WDTBUSY bit in the RTC_CTRL register to become ’0’ before configuring the timer registers.
- Enable the timer by setting the TE bit in the RTC_CTRL register.
- Program the CLKC_PERI bit in the CLKC_CNT register to set the Clk_Peri clock.
- Enable the desired interrupts by setting the TIEN bit in the RTC_CTRL register.
- Configure the desired timer mode by setting the TMMD bit in the RTC_CTRL register.
  - In one-shot mode operation, the timer stops after the countdown period is completed.
  - In free-run mode operation, the timer runs continuously without stopping.
- Set the timer countdown value (TMR) in the RTC_TMR0 register and RTC_TMR1 register.
- Configure both RTC_TMR0 and RTC_TMR1 registers; first the RTC_TMR0 register and then the RTC_TMR1 register.
  - When the RTC_TMR1 register is set, the timer countdown value is set in the 16-bit down counter running at the timer clock.
- After countdown period = TMR[15:0]/Clk_Peri, set the TMRFLG bit in the RTC_CTRL register to enable the timer interrupt to occur.

3.3.2.2 Initializing the Watchdog Timer

To initialize the RTC in watchdog timer mode:

- Wait for the WDTBUSY bit in the RTC_CTRL register to become ’0’ before configuring the WDT registers.
- Enable the watchdog timer countdown value (WDT) by setting the WE bit in the RTC_CTRL register.
- Program the CLKC_WDT bit in the CLKC_CNT register to set the CLK_WDT clock.
- Enable the WDT interrupts by setting the WEN bit in the RTC_CTRL register.
- Set the watchdog timer countdown value (WDT) in the RTC_WDT register.
- When the RTC_WDT register is set, the watchdog countdown value is set in the 8-bit down counter running at the watchdog timer clock.
- Set the WDRT bit to '1' in the RTC_CTRL register to reset the watch dog timer value; it will be cleared automatically.
- After countdown period = WDT/Clk_WDT, set the WDTFLG bit in RTC_CTRL register to enable the timer interrupt to occur.

3.3.2.3 Initializing the Calendar with Alarm

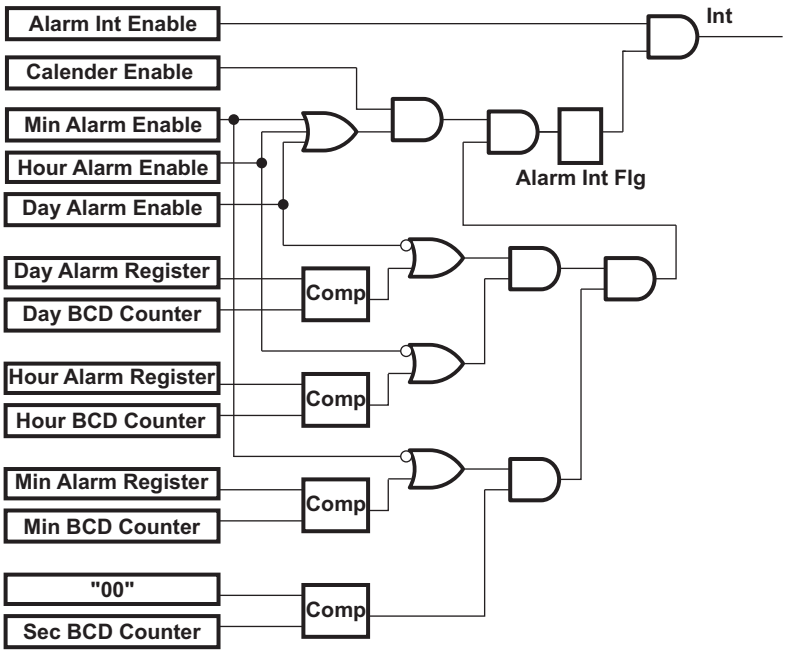
To initialize the RTC in calendar with alarm mode:

- Wait for the CALBUSY bit in the RTC_CCTRL register to become ’0’ after configuring the calendar registers.
- Enable the calendar mode by setting the CAEN bit in the RTC_CCTRL register.
- Enable the alarm interrupt by setting the AIEN bit in the RTC_CCTRL register.
- Enable the desired interrupts by setting the DAEN, HAEN and MAEN bits in the RTC_CCTRL register.
- To read and write the calendar value, access the calendar registers in the following order:
  - RTC_SEC
  - RTC_MIN
  - RTC_HOUR
  - RTC_DAY0
  - RTC_DAY1
- To set the calendar value:
  - Configure the seconds value from 00 to 59 in the RTC_SEC register.
  - Configure the minutes value from 00 to 59 in the RTC_MIN register.
  - Configure the hour value from 00 to 23 in the RTC_HOUR register.
  - Configure the days value from 0000 to 7FFF in the RTC_DAY0 and RTC_DAY1 registers.
- To configure the desired alarm:
  - Configure the minutes alarm value from 00 to 59 in the RTC_AMIN register.
  - Configure the hour alarm value from 00 to 23 in the RTC_AHOUR register
  - Configure the days alarm value from 0000 to 7FFF in the RTC_ADAY0 and RTC_ADAY1 registers.
- Enable the alarm interrupt by setting the AIEN bit in RTC_CCTRL register.
- Configure the alarm interrupt by setting the DAEN, HAEN and MAEN bits in RTC_CCTRL register. This step will clear the alarm interrupt flag bit (ALMFLG) before setting the DAEN, HAEN and MAEN bits. Table 4 describes the RTC alarm enable bits configuration for the alarm interrupt and Figure 8 illustrates the diagram for alarm interrupt.

Table 4. RTC Alarm Enable Bits

DAEN	HAEN	MAEN	Function
1	1	1	The interrupt will be generated at hour, minute, and day register setting.
0	1	1	The interrupt will be generated at hour and minute register on every day.
0	0	1	The interrupt will be generated at minute register setting on every hour.
0	0	0	No interrupt is generated.

Figure 8. Alarm Interrupt Diagram



3.4 Sequencer

3.4.1 Sequencer Features

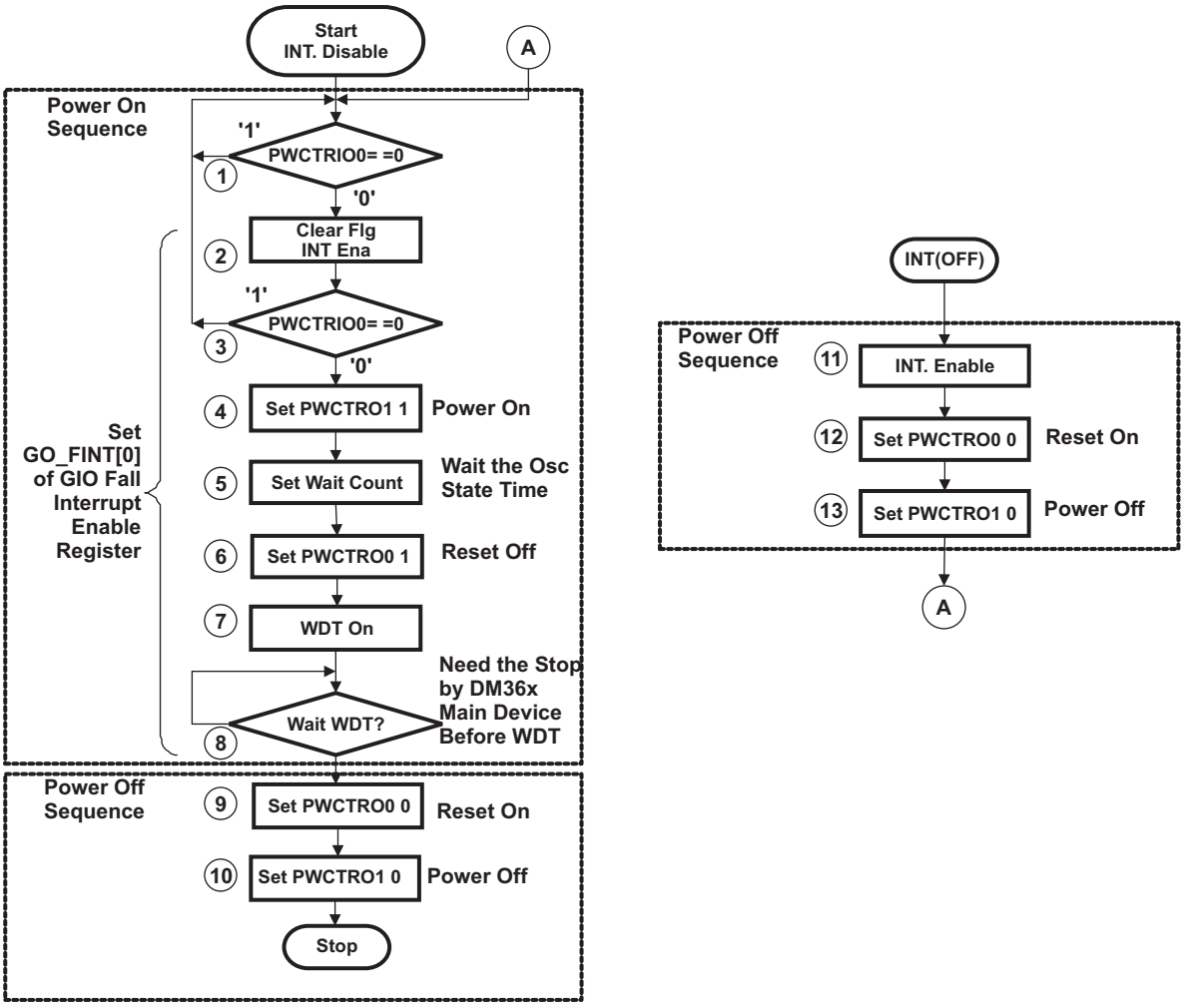
The sequencer controls the DM36x power and reset by generating the control signals on the PWCTRO1 and PWCTRO0 pins, respectively.

The sequencer module drives the PWCTRO1 and PWCTRO0 pins to control the power on/off and reset for the DM36x device.

3.4.2 Initial Sequencer Flow in Normal Mode

Figure 9 shows the flow of the Sequencer Initial Program. First, the power for the RTC block will be on. After the 32.768kHz oscillator is stable, reset for the RTC block is de-asserted by the external circuit. Finally, the RTC's sequencer will output the DM36x's power control signal and reset signal.

Figure 9. Sequencer Initial Program Flow in Normal mode



4 Registers

This section describes the memory-mapped registers for the PRTC interface (PRTCIF) and the Power Management and Real Time Clock Subsystem (PRTCSS).

4.1 PRTC Interface (PRTCIF) Registers

Table 5 lists the memory-mapped registers for the PRTCIF. For the memory address of these registers, see the device-specific data manual.

Table 5. PRTC Interface (PRTCIF) Registers

Offset	Acronym	Register Description	See
0x0	PID	PRTCIF peripheral ID register	Section 4.1.1
0x4	PRTCIF_CTRL	PRTCIF control register	Section 4.1.2
0x8	PRTCIF_LDATA	PRTCIF access lower data register	Section 4.1.3
0xC	PRTCIF_UDATA	PRTCIF access upper data register	Section 4.1.4
0x10	PRTCIF_INTEN	PRTCIF interrupt enable register	Section 4.1.5
0x14	PRTCIF_INTFLG	PRTCIF interrupt flag register	Section 4.1.6

4.1.1 PRTCIF Peripheral ID (PID) Register

The PRTCIF peripheral ID (PID) register is shown in Figure 10 and described in Table 6.

Figure 10. PRTCIF Peripheral ID Register (PID)

31	0
PID	
R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6. PRTCIF Peripheral ID Register (PID) Field Descriptions

Bit	Field	Value	Description
31-0	PID		Peripheral ID

4.1.2 PRTCIF Control (PRTCIF_CTRL) Register

The PRTCIF control (PRTCIF_CTRL) register is shown in Figure 11 and described in Table 7.

Figure 11. PRTCIF Control (PRTCIF_CTRL) Register

31	30 26	25	24	23 20	19 16
BUSY	Reserved	SIZE	DIR	BENU	BENL
R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0

15 8	7 0
Reserved	ADRS
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 7. PRTCIF Control (PRTCIF_CTRL) Field Descriptions

Bit	Field	Value	Description
31	BUSY		Status
		1	Busy
30-26	Reserved		Any writes to these bit(s) must always have a value of 0.
25	SIZE		Access size
		0	4 bytes
		1	8 bytes
24	DIR		Access direction
		0	Write
		1	Read
23-20	BENU		Access byte enable for PRTCIF_UDATA. Each PRTCIF_UDATA's byte corresponding to the enable bit is transmitted.
		xxx0	No access for the LSB
		xx0x	No access for the 2nd Byte
		x0xx	No access for the 3rd Byte
		0xxx	No access for the MSB
		xxx1	Access for the LSB
		xx1x	Access for the 2nd Byte
		x1xx	Access for the 3rd Byte
		1xxx	Access for the MSB
19-16	BENL		Access byte enable for PRTCIF_LDATA. Each PRTCIF_LDATA's byte corresponding to the enable bit is transmitted.
		xxx0	No access for the LSB
		xx0x	No access for the 2nd Byte
		x0xx	No access for the 3rd Byte
		0xxx	No access for the MSB
		xxx1	Access for the LSB
		xx1x	Access for the 2nd Byte
		x1xx	Access for the 3rd Byte
		1xxx	Access for the MSB
15-8	Reserved		Any writes to these bit(s) must always have a value of 0.
7-0	ADRS		PRTCSS target memory address

4.1.3 PRTCIF Access Lower Data (PRTCIF_LDATA) Register

The PRTCIF access lower data (PRTCIF_LDATA) register is shown in Figure 12 and descried in Table 8.

Figure 12. PRTCIF Access Lower Data (PRTCIF_LDATA) Register

31	0
DAT	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 8. PRTCIF Access Lower Data (PRTCIF_LDATA) Field Descriptions

Bit	Field	Value	Description
31-0	DAT		PRTCIF access data for lower 4 bytes

4.1.4 PRTCIF Access Upper Data (PRTCIF_UDATA) Register

The PRTCIF access upper data (PRTCIF_UDATA) register is shown in Figure 13 and described in Table 9.

Figure 13. PRTCIF Access Upper Data (PRTCIF_UDATA) Register

31	0
DAT	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 9. PRTCIF Access Upper Data (PRTCIF_UDATA) Field Descriptions

Bit	Field	Value	Description
31-0	DAT		PRTCIF access data for upper 4 bytes

4.1.5 PRTCIF Interrupt Enable (PRTCIF_INTEN) Register

The PRTCIF interrupt enable (PRTCIF_INTEN) register is shown in Figure 14 and described in Table 10.

Figure 14. PRTCIF Interrupt Enable (PRTCIF_INTEN) Register

31	2	1	0
Reserved		PRTCSS_INT_EN	PRTCIF_INT_EN
R-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 10. PRTCIF Interrupt Enable (PRTCIF_INTEN) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved		Any writes to these bit(s) must always have a value of 0.
1	PRTCSS_INT_EN		PRTCSS interrupt enable
0	PRTCIF_INT_EN		PRTCIF interrupt enable

4.1.6 PRTCIF Interrupt Flag (PRTCIF_INTFLG) Register

The PRTCIF interrupt flag register is shown in Figure 15 and described in Table 11.

Figure 15. PRTCIF Interrupt Enable (PRTCIF_INTFLG) Register

31	2	1	0
Reserved		PRTCSS_INT_FLAG	PRTCIF_INT_FLAG
R-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 11. PRTCIF Interrupt Flag (PRTCIF_INTFLG) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved		Any writes to these bit(s) must always have a value of 0.
1	PRTCSS_INT_FLAG		PRTCSS interrupt flag. Cleared by writing 1.
0	PRTCIF_INT_FLAG		PRTCIF interrupt flag. Cleared by writing 1.

4.2 Power Management and Real Time Clock Subsystem (PRTCSS) Registers

Table 12 lists the memory-mapped registers for the Power Management and Real-Time Clock Subsystem (PRTCSS). For the memory address of these registers, see the device-specific data manual.

Table 12. Power Management and Real Time Clock Subsystem (PRTCSS) Registers

Offset	Acronym	Register Description	See
0x0	GO_OUT	Global output pin output data register	Section 4.2.1
0x1	GIO_OUT	Global input/output pin output data register	Section 4.2.2
0x2	GIO_DIR	Global input/output pin direction register	Section 4.2.3
0x3	GIO_IN	Global input/output pin input data register	Section 4.2.4
0x4	GIO_FUNC	Global input/output pin function register	Section 4.2.5
0x5	GIO_RISE_INT_EN	GIO rise interrupt enable register	Section 4.2.6
0x6	GIO_FALL_INT_EN	GIO fall interrupt enable register	Section 4.2.7
0x7	GIO_RISE_INT_FLG	GIO rise interrupt flag register	Section 4.2.8
0x8	GIO_FALL_INT_FLG	GIO fall interrupt flag register	Section 4.2.9
0x9-0xA	Reserved	Reserved	
0xB	INTC_EXTENA0	EXT interrupt enable 0 register	Section 4.2.10
0xC	INTC_EXTENA1	EXT interrupt enable 1 register	Section 4.2.11
0xD	INTC_FLG0	Event interrupt flag 0 register	Section 4.2.12
0xE	INTC_FLG1	Event interrupt flag 1 register	Section 4.2.13
0xF	Reserved	Reserved	
0x10	RTC_CTRL	RTC control register	Section 4.2.14
0x11	RTC_WDT	Watchdog timer counter register	Section 4.2.15
0x12	RTC_TMR0	Timer counter 0 register	Section 4.2.16
0x13	RTC_TMR1	Timer counter 1 register	Section 4.2.17
0x14	RTC_CCTRL	Calendar control register	Section 4.2.18
0x15	RTC_SEC	Seconds register	Section 4.2.19
0x16	RTC_MIN	Minutes register	Section 4.2.20
0x17	RTC_HOUR	Hours register	Section 4.2.21
0x18	RTC_DAY0	Days[[7:0] register	Section 4.2.22
0x19	RTC_DAY1	Days[14:8] register	Section 4.2.23
0x1A	RTC_AMIN	Minutes Alarm register	Section 4.2.24
0x1B	RTC_AHOUR	Hour Alarm register	Section 4.2.25
0x1C	RTC_ADAY0	Days[7:0] Alarm register	Section 4.2.26
0x1D	RTC_ADAY1	Days[14:8] Alarm register	Section 4.2.27
0x1F-0x1E	Reserved	Reserved	
0x20	CLKC_CNT	Clock control register	Section 4.2.28
0x21-0x31	Reserved	Reserved	

4.2.1 Global Output Pin Output Data (GO_OUT) Register

The global output pin output data (GO_OUT) register is shown in Figure 16 and described in Table 13.

Figure 16. Global Output Pin Output Data (GO_OUT) Register

7	4	3	2	1	0
Reserved		PWCTRO_O3	PWCTRO_O2	PWCTRO_O1	PWCTRO_O0
R-1		R/W-1			

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 13. Global Output Pin Output Data (GO_OUT) Field Descriptions

Bit	Field	Value	Description
7-4	Reserved		Any writes to these bit(s) must always have a value of 0.
3-0	PWCTRO_On		PWCTRO output data
		0	PWCTRO pin n is driven low
		1	PWCTRO pin n is driven high

4.2.2 Global Input/Output Pin Output Data (GIO_OUT) Register

The global input/output pin output data (GIO_OUT) register is shown in Figure 17 and described in Table 14.

Figure 17. Global Input/Output Pin Output Data (GIO_OUT) Register

7	6	5	4	3	2	1	0
Reserved	PWCTRIO_O6	PWCTRIO_O5	PWCTRIO_O4	PWCTRIO_O3	PWCTRIO_O2	PWCTRIO_O1	PWCTRIO_O0
R-0				R/W-0			

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 14. Global Input/Output Pin Output Data (GIO_OUT) Field Descriptions

Bit	Field	Value	Description
7	Reserved		Any writes to these bit(s) must always have a value of 0.
6-0	PWCTRIO_On		PWCTRIO output data
		0	PWCTRIO pin n is driven low
		1	PWCTRIO pin n is driven high

4.2.3 Global Input/Output Pin Direction (GIO_DIR) Register

The global input/output pin direction (GIO_DIR) register is shown in Figure 18 and described in Table 15.

Figure 18. Global Input/Output Pin Direction (GIO_DIR) Register

7	6	5	4	3	2	1	0
Reserved	PWCTRIO_DIR6	PWCTRIO_DIR5	PWCTRIO_DIR4	PWCTRIO_DIR3	PWCTRIO_DIR2	PWCTRIO_DIR1	PWCTRIO_DIR0
R-0	R/W-0						

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 15. Global Input/Output Pin Direction (GIO_DIR) Field Descriptions

Bit	Field	Value	Description
7	Reserved		Any writes to these bit(s) must always have a value of 0.
6-0	PWCTRIO_DIRn		This bit is used to control the direction of pin n.
		0	PWCTRIO pin n is an input.
		1	PWCTRIO pin n is an output.

4.2.4 Global Input/Output Pin Input Data (GIO_IN) Register

The global input/output pin input data (GIO_IN) register is shown in Figure 19 and described in Table 16.

Figure 19. Global Input/Output Pin Input Data (GIO_IN) Register

7	6	5	4	3	2	1	0
Reserved	PWCTRIO_IN6	PWCTRIO_IN5	PWCTRIO_IN4	PWCTRIO_IN3	PWCTRIO_IN2	PWCTRIO_IN1	PWCTRIO_IN0
R-0				R-0			

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 16. Global Input/Output Pin Input Data (GIO_IN) Field Descriptions

Bit	Field	Value	Description
7	Reserved		Any writes to these bit(s) must always have a value of 0.
6-0	PWCTRIO_INn		PWCTRIO input data
		0	PWCTRIO pin n is logic low
		1	PWCTRIO pin n is logic high

4.2.5 Global Input/Output Pin Function (GIO_FUNC) Register

The global input/output pin function (GIO_FUNC) register is shown in Figure 20 and described in Table 17.

Figure 20. Global Input/Output Pin Function (GIO_FUNC) Register

7 5	4 2	1 0
PWM_PERIOD	PWM_WIDTH	GO2_FUNC
R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 17. Global Input/Output Pin Function (GIO_FUNC) Field Descriptions

Bit	Field	Value	Description
7-5	PWM_PERIOD		PWM period
		000	2 x pwm_width
		001	3 x pwm_width
		010	4 x pwm_width
		011	5 x pwm_width
		100	6 x pwm_width
		101	7 x pwm_width
		110	8 x pwm_width
		111	9 x pwm_width
4-2	PWM_WIDTH		PWM width
		000	16 x Clk_Peri period
		001	32 x Clk_Peri period
		010	64 x Clk_Peri period
		011	128 x Clk_Peri period
		100	256 x Clk_Peri period
		101	512 x Clk_Peri period
		110	1024 x Clk_Peri period
		111	2048 x Clk_Peri period
1-0	GO2_FUNC		Function enable
		000	PWCTRO function
		001	32.768 kHz clockout function
		010	PWM output (Polarity=0)
		011	PWM output (Polarity=1)

4.2.6 GIO Rise Interrupt Enable (GIO_RISE_INT_EN) Register

The GIO rise interrupt enable (GIO_RISE_INT_EN) register is shown in Figure 21 and described in Table 18.

Figure 21. GIO Rise Interrupt Enable (GIO_RISE_INT_EN) Register

7	6	5	4	3	2	1	0
Reserved	PWCTRIO_RINT6	PWCTRIO_RINT5	PWCTRIO_RINT4	PWCTRIO_RINT3	PWCTRIO_RINT2	PWCTRIO_RINT1	PWCTRIO_RINT0
R-0	R/W-0						

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18. GIO Rise Interrupt Enable (GIO_RISE_INT_EN) Field Descriptions

Bit	Field	Value	Description
7	Reserved		Any writes to these bit(s) must always have a value of 0.
6-0	PWCTRIO_RINTn		Enable rising edge interrupt detection on PWCTRIO pin n
		0	No effect
		1	Generate interrupt for the rise edge

4.2.7 GIO Fall Interrupt Enable (GIO_FALL_INT_EN) Register

The GIO fall interrupt enable (GIO_FALL_INT_EN) register is shown in Figure 22 and described in Table 19.

Figure 22. GIO Fall Interrupt Enable Register (GIO_FALL_INT_EN)

7	6	5	4	3	2	1	0
Reserved	PWCTRIO_FINT6	PWCTRIO_FINT5	PWCTRIO_FINT4	PWCTRIO_FINT3	PWCTRIO_FINT2	PWCTRIO_FINT1	PWCTRIO_FINT0
R-0	R/W-0						

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 19. GIO Fall Interrupt Enable Register (GIO_FALL_INT_EN) Field Descriptions

Bit	Field	Value	Description
7	Reserved		Any writes to these bit(s) must always have a value of 0.
6-0	PWCTRIO_FINTn		Enable falling edge interrupt detection on PWCTRIO pin n
		0	No effect
		1	Generate interrupt for the fall edge

4.2.8 GIO Rise Interrupt Flag (GIO_RISE_INT_FLG) Register

The GIO rise interrupt flag (GIO_RISE_INT_FLG) register is shown in Figure 23 and described in Table 20.

Figure 23. GIO Rise Interrupt Flag (GIO_RISE_INT_FLG) Register

7	6	5	4	3	2	1	0
Reserved	PWCTRIO_RFLG6	PWCTRIO_RFLG5	PWCTRIO_RFLG4	PWCTRIO_RFLG3	PWCTRIO_RFLG2	PWCTRIO_RFLG1	PWCTRIO_RFLG0
R-0	R/C-0						

LEGEND: R/W = Read/Write; R = Read only; R/C = Read/Clear; *-n* = value after reset

Table 20. GIO Rise Interrupt Flag (GIO_RISE_INT_FLG) Field Descriptions

Bit	Field	Value	Description
7	Reserved		Any writes to these bit(s) must always have a value of 0.
6-0	PWCTRIO_RFLGn		Interrupt flag register for rising edge for PWCTRIO pin n; cleared by writing 1.

4.2.9 GIO Fall Interrupt Flag (GIO_FALL_INT_FLG) Register

The GIO fall interrupt flag (GIO_FALL_INT_FLG) register is shown in Figure 24 and described in Table 21.

Figure 24. GIO Fall Interrupt Flag (GIO_FALL_INT_FLG) Register

7	6	5	4	3	2	1	0
Reserved	PWCTRIO_FFLG6	PWCTRIO_FFLG5	PWCTRIO_FFLG4	PWCTRIO_FFLG3	PWCTRIO_FFLG2	PWCTRIO_FFLG1	PWCTRIO_FFLG0
R-0				R/C-0			

LEGEND: R/W = Read/Write; R = Read only; R/C = Read/Clear; -*n* = value after reset

Table 21. GIO Fall Interrupt Flag (GIO_FALL_INT_FLG) Field Descriptions

Bit	Field	Value	Description
7	Reserved		Any writes to these bit(s) must always have a value of 0.
6-0	PWCTRIO_FFLGn		Interrupt flag register for falling edge for PWCTRIO pin n; cleared by writing 1.

4.2.10 EXT Interrupt Enable 0 (INTC_EXTENA0) Register

The EXT interrupt enable 0 (INTC_EXTENA0) register is shown in Figure 25 and described in Table 22.

Figure 25. EXT Interrupt Enable 0 (INTC_EXTENA0) Register

7	6	5	4	3	2	1	0
Reserved	PWCTRIO6	PWCTRIO5	PWCTRIO4	PWCTRIO3	PWCTRIO2	PWCTRIO1	PWCTRIO0
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 22. EXT Interrupt Enable 0 (INTC_EXTENA0) Field Descriptions

Bit	Field	Value	Description
7	Reserved		Any writes to these bit(s) must always have a value of 0.
6	PWCTRIO6		PWCTRIO6 interrupt enable
		0	Disable
		1	Enable
5	PWCTRIO5		PWCTRIO5 interrupt enable
		0	Disable
		1	Enable
4	PWCTRIO4		PWCTRIO4 interrupt enable
		0	Disable
		1	Enable
3	PWCTRIO3		PWCTRIO3 interrupt enable
		0	Disable
		1	Enable
2	PWCTRIO2		PWCTRIO2 interrupt enable
		0	Disable
		1	Enable
1	PWCTRIO1		PWCTRIO1 interrupt enable
		0	Disable
		1	Enable
0	PWCTRIO0		PWCTRIO0 interrupt enable
		0	Disable
		1	Enable

4.2.11 EXT Interrupt Enable 1 (INTC_EXTENA1) Register

The ext interrupt enable 1 (INTC_EXTENA1) register is shown in Figure 26 and described in Table 23 .

Figure 26. EXT Interrupt Enable 1 (INTC_EXTENA1) Register

7	3	2	1	0
Reserved		TIMER	ALARM	WDT
R-0		R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 23. EXT Interrupt Enable 1 (INTC_EXTENA1) Field Descriptions

Bit	Field	Value	Description
7-3	Reserved		Any writes to these bit(s) must always have a value of 0.
2	TIMER		Timer interrupt enable for DM36x main device
		0	Disable
		1	Enable
1	ALARM		Alarm interrupt enable for DM36x main device
		0	Disable
		1	Enable
0	WDT		WDT interrupt enable for DM36x main device
		0	Disable
		1	Enable

4.2.12 Event Interrupt Flag 0 (INTC_FLG0) Register

The event Interrupt flag 0 (INTC_FLG0) register is shown in Figure 27 and described in Table 24.

Figure 27. Event Interrupt Flag 0 (INTC_FLG0) Register

7	6	5	4	3	2	1	0
Reserved	PWCTRIO6	PWCTRIO5	PWCTRIO4	PWCTRIO3	PWCTRIO2	PWCTRIO1	PWCTRIO0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 24. Event Interrupt Flag 0 (INTC_FLG0) Field Descriptions

Bit	Field	Value	Description
7	Reserved		Any writes to these bit(s) must always have a value of 0.
6	PWCTRIO6		PWCTRIO6 interrupt flag
		0	No interrupt
		1	Interrupt
5	PWCTRIO5		PWCTRIO5 interrupt flag
		0	No interrupt
		1	Interrupt
4	PWCTRIO4		PWCTRIO4 interrupt flag
		0	No interrupt
		1	Interrupt
3	PWCTRIO3		PWCTRIO3 interrupt flag
		0	No interrupt
		1	Interrupt
2	PWCTRIO2		PWCTRIO2 interrupt flag
		0	No interrupt
		1	Interrupt
1	PWCTRIO1		PWCTRIO1 interrupt flag
		0	No interrupt
		1	Interrupt
0	PWCTRIO0		PWCTRIO0 interrupt flag
		0	No interrupt
		1	Interrupt

4.2.13 Event Interrupt Flag 1 (INTC_FLG1) Register

The event interrupt flag 1 (INTC_FLG1) register is shown in Figure 28 and described in Table 25 .

Figure 28. Event Interrupt Flag 1 (INTC_FLG1) Register

7	3	2	1	0
Reserved		TIMER	ALARM	WDT
R-0		R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 25. Event Interrupt Flag 1 (INTC_FLG1) Field Descriptions

Bit	Field	Value	Description
7-3	Reserved		Any writes to these bit(s) must always have a value of 0.
2	TIMER		Timer interrupt flag
		0	No interrupt
		1	interrupt
1	ALARM		Alarm interrupt flag
		0	No interrupt
		1	interrupt
0	WDT		WDT interrupt flag
		0	No interrupt
		1	interrupt

4.2.14 RTC Control (RTC_CTRL) Register

The RTC control (RTC_CTRL) register is shown in Figure 29 and described in Table 26.

Figure 29. RTC Control (RTC_CTRL) Register

7	6	5	4	3	2	1	0
WDTBUSY	WEN	WDRT	WDTFLG	TE	TIEN	TMRFLG	TMMD
R-0	R/W-0	R/W-0	R/C-0	R/W-0	R/W-0	R/C-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; R/C = Read/Clear; *-n* = value after reset

Table 26. RTC Control (RTC_CTRL) Field Descriptions

Bit	Field	Value	Description
7	WDTBUSY		WDT access busy flag. This bit value must be a 0 before any WDT/Timer register is to be written.
6	WEN		Watchdog timer enable
		0	Disable
		1	Enable
5	WDRT		Watchdog timer reset. Writing 1 resets the watchdog timer value, then it is cleared automatically.
4	WDTFLG		Watchdog timer interrupt flag bit. Writing 1 to this bit clears the watchdog timer interrupt flag, then it is cleared automatically. At read time, the watchdog timer interrupt status can be read.
		0	No interrupt
		1	Interrupt
3	TE		Timer enable
		0	Disable
		1	Enable
2	TIEN		Timer interrupt enable
		0	Disable
		1	Enable
1	TMRFLG		Timer interrupt flag bit Writing 1 to this bit clears the timer interrupt flag, then it is cleared automatically. At read time, the timer interrupt status can be read.
		0	No interrupt
		1	Interrupt
			To run the timer in one-shot/free-run mode after an interrupt occurs, the timer interrupt flag (TMRFLG) should be cleared in advance.
0	TMMD		Timer run mode
		0	One-shot
		1	Free-run

4.2.15 Watchdog Timer Counter (RTC_WDT) Register

The RTC watchdog timer counter (RTC_WDT) register is shown in Figure 30 and described in Table 27.

Figure 30. RTC Watchdog Timer Counter (RTC_WDT) Register

7							0
WDT							
R/W-0xFF							

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 27. RTC Watchdog Timer Counter (RTC_WDT) Field Descriptions

Bit	Field	Value	Description
7-0	WDT		Watchdog timer counter value Watchdog timer countdown value = WDT Countdown period = WDT/ WDT peripheral clock frequency WDT peripheral clock frequency (Clk_WDT) = 32.768 kHz / CLKC_WDT

4.2.16 Timer Counter 0 (RTC_TMR0) Register

The timer counter 0 (RTC_TMR0) register is shown in Figure 31 and described in Table 28.

Figure 31. Timer Counter 0 (RTC_TMR0) Register

7							0
TMR[7:0]							
R/W-0xFF							

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 28. Timer Counter 0 (RTC_TMR0) Field Descriptions

Bit	Field	Value	Description
7-0	TMR[7:0]		Timer counter value [7:0]

4.2.17 Timer Counter 1 (RTC_TMR1) Register

The RTC timer counter 1 (RTC_TMR1) register is shown in Figure 32 and described in Table 29.

Figure 32. Timer Counter 1 (RTC_TMR1) Register

7	0
TMR[15:8]	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 29. Timer Counter 1 (RTC_TMR1) Field Descriptions

Bit	Field	Value	Description
7-0	TMR[15:8]		Timer countdown value [15:8]. Timer countdown value is set to the 16-bit down counter when the RTC_TMR1 is set. You must set both registers; RTC_TMR0 first and then RTC_TMR1. The read access to the TMR registers should be done; first TMR0 and then TMR1. Countdown value = TMR[15:0] Countdown period = TMR[15:0]/ timer peripheral clock frequency Timer peripheral clock frequency (Clk_Peri) = 32.768 kHz / CLKC_PERI

4.2.18 RTC Calendar Control (RTC_CCTRL) Register

The RTC calendar control (RTC_CCTRL) register is shown in Figure 33 and described in Table 30.

Figure 33. RTC Calendar Control (RTC_CCTRL) Register

7	6	5	4	3	2	1	0
CALBUSY	Reserved	DAEN	HAEN	MAEN	ALMFLG	AIEN	CAEN
R-0	R-0	R/W-0	R/W-0	R/W-0	R/C-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; R/C = Read/Clear; *-n* = value after reset

Table 30. RTC Calendar Control (RTC_CCTRL) Field Descriptions

Bit	Field	Value	Description
7	CALBUSY		Calendar access busy flag. This bit value must be a 0, before any calendar register is to be written.
6	Reserved		Any writes to these bit(s) must always have a value of 0.
5	DAEN		Day alarm enable
		0	Disable
		1	Enable
4	HAEN		Hour alarm enable
		0	Disable
		1	Enable
3	MAEN		Minute alarm enable
		0	Disable
		1	Enable
2	ALMFLG		Alarm interrupt flag bit. Writing 1 to this bit clears alarm interrupt flag, then it is cleared automatically. At read time, the alarm interrupt status can be read.
		0	No interrupt
		1	Interrupt
1	AIEN		Alarm interrupt enable
		0	Disable
		1	Enable
0	CAEN		Calendar enable
		0	Disable
		1	Enable

4.2.19 RTC Seconds (RTC_SEC) Register

The RTC seconds (RTC_SEC) register is shown in Figure 34 and described in Table 31.

Figure 34. RTC Seconds (RTC_SEC) Register

7	6	0
Reserved	SEC	
R-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 31. RTC Seconds (RTC_SEC) Field Descriptions

Bit	Field	Value	Description
7	Reserved		Any writes to these bit(s) must always have a value of 0.
6-0	SEC		Seconds counter Seconds 00 to 59 coded in BCD. If 59 seconds are set to SEC, then SEC will become 7'b1011001. When the value is written to this register, the counter of less than one second is cleared.

4.2.20 RTC Minutes (RTC_MIN) Register

The RTC minutes (RTC_MIN) register is shown in Figure 35 and described in Table 32.

Figure 35. RTC Minutes (RTC_MIN) Register

7	6	0
Reserved	MIN	
R-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 32. RTC Minutes (RTC_MIN) Field Descriptions

Bit	Field	Value	Description
7	Reserved		Any writes to these bit(s) must always have a value of 0.
6-0	MIN		Minutes counter. Minutes 00 to 59 coded in BCD. If 59 minutes are set to MIN, then MIN will become 7'b1011001.

4.2.21 RTC Hours (RTC_HOUR) Register

The RTC hours (RTC_HOUR) register is shown in Figure 36 and described in Table 33.

Figure 36. RTC Hours Register (RTC_HOUR)

7	6	5	0
Reserved		HOUR	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 33. RTC Hours (RTC_HOUR) Field Descriptions

Bit	Field	Value	Description
7-6	Reserved		Any writes to these bit(s) must always have a value of 0.
5-0	HOUR		Hours counter Hours 00 to 23 coded in BCD. If 23 hours are set to HOUR, then HOUR will become 6'b100011.

4.2.22 RTC Days[7:0] (RTC_DAY0) Register

The RTC days[7:0] (RTC_DAY0) register is shown in Figure 37 and described in Table 34.

Figure 37. RTC Days[7:0] (RTC_DAY0) Register

7							0
DAY[7:0]							
R/W-0							

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 34. RTC Days[7:0] (RTC_DAY0) Field Descriptions

Bit	Field	Value	Description
7-0	DAY[7:0]		Days counter [7:0]

4.2.23 RTC Days[14:8] (RTC_DAY1) Register

The RTC days[14:8] (RTC_DAY1) register is shown in Figure 38 and described in Table 35.

Figure 38. RTC Days[14:8] (RTC_DAY1) Register

7	6	0
Reserved	DAY[14:8]	
R-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 35. RTC Days[14:8] (RTC_DAY1) Field Descriptions

Bit	Field	Value	Description
7	Reserved		Any writes to these bit(s) must always have a value of 0.
6-0	DAY[14:8]		Days counter [14:8]. Days 0000 to 7FFF coded in hexadecimal format. If 32,767 days are set to DAY[14:0] then DAY[14:0] will become 15'b111_1111_1111_1111. For reading and writing the calendar value, access calendar registers in the following order : RTC_SEC -> RTC_MIN -> RTC_HOUR -> RTC_DAY0 -> RTC_DAY1

4.2.24 RTC Minutes Alarm (RTC_AMIN) Register

The RTC minutes alarm (RTC_AMIN) register is shown in Figure 39 and described in Table 36.

Figure 39. RTC Minutes Alarm (RTC_AMIN) Register

7	6	0
Reserved	AMIN	
R-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 36. RTC Minutes Alarm (RTC_AMIN) Field Descriptions

Bit	Field	Value	Description
7	Reserved		Any writes to these bit(s) must always have a value of 0.
6-0	AMIN		Minutes alarm. Minutes alarm 00 to 59 coded in BCD. If 59 minutes are set to AMIN, then AMIN will become 7'b1011001.

4.2.25 RTC Hours Alarm (RTC_AHOUR) Register

The RTC hours alarm (RTC_AHOUR) register is shown in Figure 40 and described in Table 37.

Figure 40. RTC Hours Alarm (RTC_AHOUR) Register

7	6	5	0
Reserved		AHOUR	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 37. RTC Hours Alarm (RTC_AHOUR) Field Descriptions

Bit	Field	Value	Description
7-6	Reserved		Any writes to these bit(s) must always have a value of 0.
5-0	AHOUR		Hours alarm Hours alarm 00 to 23 coded in BCD. If 23 hours are set to AHOUR, then AHOUR will become 6'b100011.

4.2.26 RTC Days[7:0] Alarm (RTC_ADAY0) Register

The RTC days[7:0] alarm (RTC_ADAY0) register shown in Figure 41 and described in Table 38.

Figure 41. RTC Days[7:0] Alarm (RTC_ADAY0) Register

7	6						0
ADAY[7:0]							
R/W-0							

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 38. RTC Days[7:0] Alarm (RTC_ADAY0) Field Descriptions

Bit	Field	Value	Description
7-0	ADAY[7:0]		Days alarm [7:0]

4.2.27 RTC Days[14:8] Alarm (RTC_ADAY1) Register

The RTC days[14:8] alarm (RTC_ADAY1) register is shown in Table 39 and described in Table 39.

Figure 42. RTC Days[14:8] Alarm (RTC_ADAY1) Register

7	6 0
Reserved	ADAY[14:8]
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 39. RTC Days[14:8] Alarm (RTC_ADAY1) Field Descriptions

Bit	Field	Value	Description
7	Reserved		Any writes to these bit(s) must always have a value of 0.
6-0	ADAY[14:8]		Days alarm [14:8]. Days alarm 0000 to 7FFF coded in hexadecimal format. If 32,767 days are set to ADAY[14:0,] then ADAY[14:0] will become 15'b111_1111_1111_1111.

4.2.28 Clock Control (CLKC_CNT) Register

The clock control (CLKC_CNT) register is shown in Figure 43 and described in Table 40.

Figure 43. Clock Control (CLKC_CNT) Register

7	4	3	0
CLKC_WDT		CLKC_PERI	
R/W-0xB		R/W-0x8	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 40. Clock Control (CLKC_CNT) Field Descriptions

Bit	Field	Value	Description
7-4	CLKC_WDT		Divide value for WDT clock (Clk_WDT)
		0000	1/1 32.768 kHz
		0001	1/2 for 16.384 kHz
		0010	1/4 for 8.192 kHz
		0011	1/8 for 4.096 kHz
		0100	1/16 for 2.048 kHz
		0101	1/32 for 1.024 kHz
		0110	1/64 for 512 Hz
		0111	1/128 for 256 Hz
		1000	1/256 for 128 Hz
		1001	1/512 for 64 Hz
		1010	1/1024 for 32 Hz
		1011	1/2048 for 16 Hz
		1100-1111	1/4096 for 8 Hz
3-0	CLKC_PERI		Divide value for peripheral clock (Clk_Peri)
		0000	1/1 32.768 kHz
		0001	1/2 for 16.384 kHz
		0010	1/4 for 8.192 kHz
		0011	1/8 for 4.096 kHz
		0100	1/16 for 2.048 kHz
		0101	1/32 for 1.024 kHz
		0110	1/64 for 512 Hz
		0111	1/128 for 256 Hz
		1000	1/256 for 128 Hz
		1001	1/512 for 64 Hz
		1010	1/1024 for 32 Hz
		1011	1/2048 for 16 Hz
		1100-1111	1/4096 for 8 Hz

4.2.29 Sequencer Loop Counter Value (SEQ_LOOP) Register

The sequencer loop counter value (SEQ_LOOP) register is shown in Figure 44 and described in Table 41.

Figure 44. Sequencer Loop Counter Value (SEQ_LOOP) Register

7							0
LOOP							
R/W-0x04							

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 41. Sequencer Loop Counter Value (SEQ_LOOP) Field Descriptions

Bit	Field	Value	Description
7-0	LOOP		Sequencer loop counter value

Appendix A Revision History

This document has been revised from SPRUFJ0A to SPRUFJ0**B** because of the following technical change(s).

Table 42. Changes Made in This Revision

Location	Additions, Deletions, Changes
Figure 2	Added PWCTRIO0 to figure.
Section 4.2.3	Corrected the description for bits 6-0 in the GIO_DIR register.

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