TMS320DM35x
Digital Media System-on-Chip (DMSoC)
Video Processing Back End

Reference Guide

Literature Number: SPRUF72C
October 2008

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Read This First

About This Manual

Describes the operation of the Video Processing Back End in the TMS320DM35x Digital Media System-on-Chip (DMSoC).

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320DM35x Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the internet at www.ti.com.

SPRS463 — ***TMS320DM355 Digital Media System-on-Chip (DMSoC) Data Manual*** This document describes the overall TMS320DM355 system, including device architecture and features, memory map, pin descriptions, timing characteristics and requirements, device mechanicals, etc.

SPRZ264 — ***TMS320DM355 DMSoC Silicon Errata*** Describes the known exceptions to the functional specifications for the TMS320DM355 DMSoC.

SPRUFB3 — ***TMS320DM35x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide*** This document describes the ARM Subsystem in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the components of the ARM Subsystem, the peripherals, and the external memories.

SPRUED1 — ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Asynchronous External Memory Interface (EMIF) Reference Guide*** This document describes the asynchronous external memory interface (EMIF) in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The EMIF supports a glueless interface to a variety of external devices.

SPRUED2 — ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Universal Serial Bus (USB) Controller Reference Guide*** This document describes the universal serial bus (USB) controller in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The USB controller supports data throughput rates up to 480 Mbps. It provides a mechanism for data transfer between USB devices and also supports host negotiation.

SPRUED3 — ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Audio Serial Port (ASP) Reference Guide*** This document describes the operation of the audio serial port (ASP) audio interface in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The primary audio modes that are supported by the ASP are the AC97 and IIS modes. In addition to the primary audio modes, the ASP supports general serial port receive and transmit operation, but is not intended to be used as a high-speed interface.

SPRUED4 — ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Serial Peripheral Interface (SPI) Reference Guide*** This document describes the serial peripheral interface (SPI) in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communication between the DMSoC and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EPROMs and analog-to-digital converters.

SPRUED9 — ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Universal Asynchronous Receiver/Transmitter (UART) Reference Guide*** This document describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The UART peripheral performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data received from the CPU.

SPRUEE0 — ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Inter-Integrated Circuit (I2C) Peripheral Reference Guide*** This document describes the inter-integrated circuit (I2C) peripheral in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The I2C peripheral provides an interface between the DMSoC and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus. External components attached to this 2-wire serial bus can transmit and receive up to 8-bit wide data to and from the DMSoC through the I2C peripheral. This document assumes the reader is familiar with the I2C-bus specification.

SPRUEE2 — ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Multimedia Card (MMC)/Secure Digital (SD) Card Controller Reference Guide*** This document describes the multimedia card (MMC)/secure digital (SD) card controller in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The MMC/SD card is used in a number of applications to provide removable data storage. The MMC/SD controller provides an interface to external MMC and SD cards. The communication between the MMC/SD controller and MMC/SD card(s) is performed by the MMC/SD protocol.

SPRUEE4 — ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Enhanced Direct Memory Access (EDMA) Controller Reference Guide*** This document describes the operation of the enhanced direct memory access (EDMA3) controller in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The EDMA controller's primary purpose is to service user-programmed data transfers between two memory-mapped slave endpoints on the DMSoC.

SPRUEE5 — ***TMS320DM35x Digital Media System-on-Chip (DMSoC) 64-bit Timer Reference Guide*** This document describes the operation of the software-programmable 64-bit timers in the TMS320DM35x Digital Media System-on-Chip (DMSoC). Timer 0, Timer 1, and Timer 3 are used as general-purpose (GP) timers and can be programmed in 64-bit mode, dual 32-bit unchained mode, or dual 32-bit chained mode; Timer 2 is used only as a watchdog timer. The GP timer modes can be used to generate periodic interrupts or enhanced direct memory access (EDMA) synchronization events and Real Time Output (RTO) events (Timer 3 only). The watchdog timer mode is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

SPRUEE6 — ***TMS320DM35x Digital Media System-on-Chip (DMSoC) General-Purpose Input/Output (GPIO) Reference Guide*** This document describes the general-purpose input/output (GPIO) peripheral in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an input, you can detect the state of the input by reading the state of an internal register. When configured as an output, you can write to an internal register to control the state driven on the output pin.

SPRUEE7 — ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Pulse-Width Modulator (PWM) Reference Guide*** This document describes the pulse-width modulator (PWM) peripheral in the TMS320DM35x Digital Media System-on-Chip (DMSoC).

SPRUEH7 — ***TMS320DM35x Digital Media System-on-Chip (DMSoC) DDR2/Mobile DDR (DDR2/mDDR) Memory Controller Reference Guide*** This document describes the DDR2/mDDR memory controller in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The DDR2/mDDR memory controller is used to interface with JESD79D-2A standard compliant DDR2 SDRAM and mobile DDR devices.

SPRUF71 — ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Video Processing Front End (VPFE) Reference Guide*** This document describes the Video Processing Front End (VPFE) in the TMS320DM35x Digital Media System-on-Chip (DMSoC).

SPRUF72 — ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Video Processing Back End (VPBE) Reference Guide*** This document describes the Video Processing Back End (VPBE) in the TMS320DM35x Digital Media System-on-Chip (DMSoC).

SPRUF74 — ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Real-Time Out (RTO) Controller Reference Guide*** This document describes the Real Time Out (RTO) controller in the TMS320DM35x Digital Media System-on-Chip (DMSoC).

SPRUFC8 — ***TMS320DM35x Digital Media System-on-Chip (DMSoC) Peripherals Overview Reference Guide*** This document provides an overview of the peripherals in the TMS320DM35x Digital Media System-on-Chip (DMSoC).

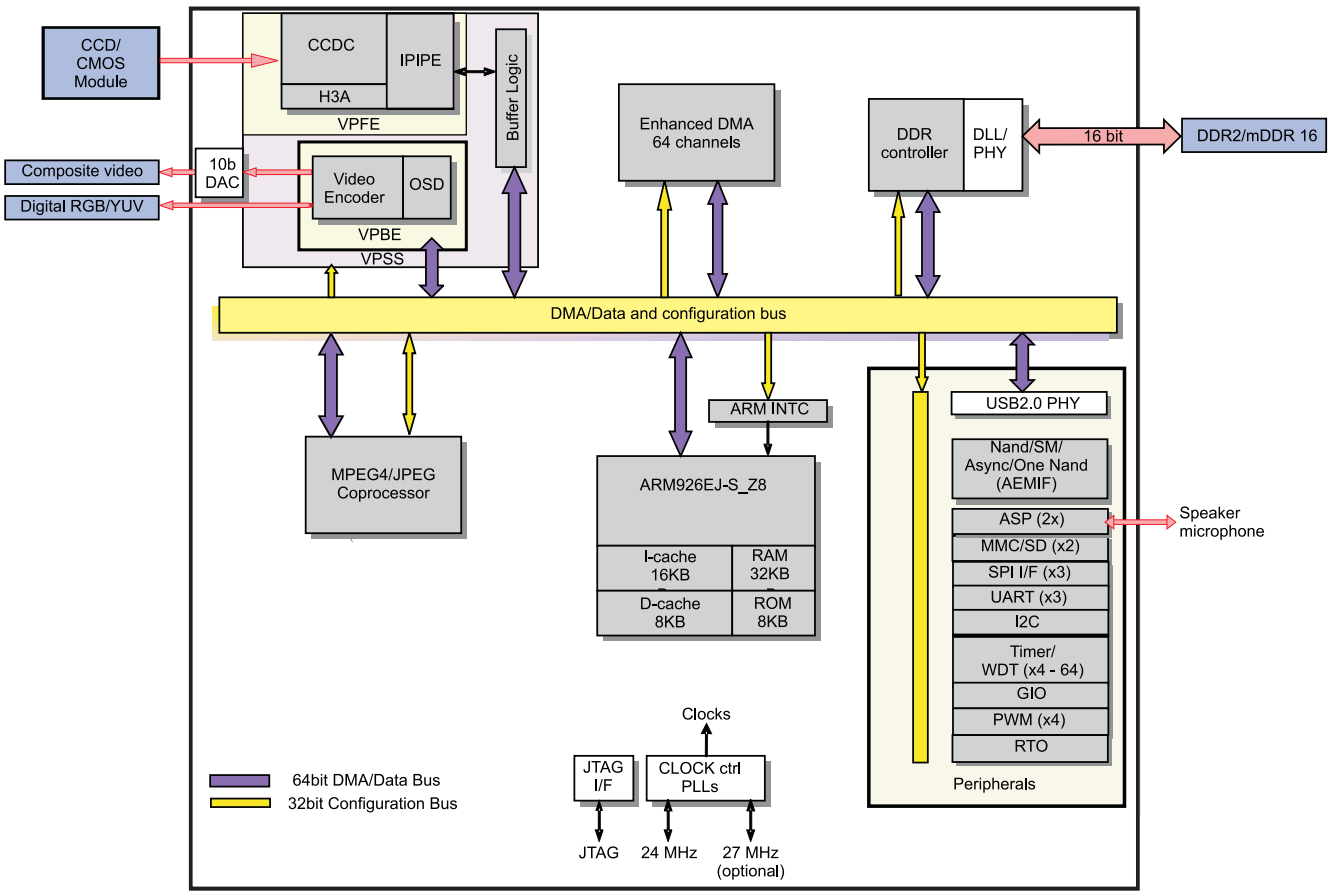
SPRAAR3 — ***Implementing DDR2/mDDR PCB Layout on the TMS320DM35x DMSoC*** This provides board design recommendations and guidelines for DDR2 and mobile DDR.

Trademarks

Video Processing Back End

TMS320DM35x is a highly integrated, programmable platform for digital still/video cameras and other mobile imaging devices. Designed to offer camera manufacturers the ability to produce affordable DSC products with high picture quality, the device combines programmable image processing capability with a highly integrated imaging peripheral set. The device contains an ARM9 RISC CPU, a proprietary DSP-based imaging co-processor subsystem, and a powerful video processing subsystem. Together, they enable device manufacturers to implement high-speed hardware enabled image pipelines as well as their own proprietary image processing algorithms in software. The device also enables seamless interface to many external display devices required for a complete digital camera digital implementation via the Video Processing Back End Subsystem or VPBE. The interface is flexible enough to support various types of digital as well as analog (NTSC/PAL) displays. A block diagram is shown in Figure 1.

Figure 1. Functional Block Diagram

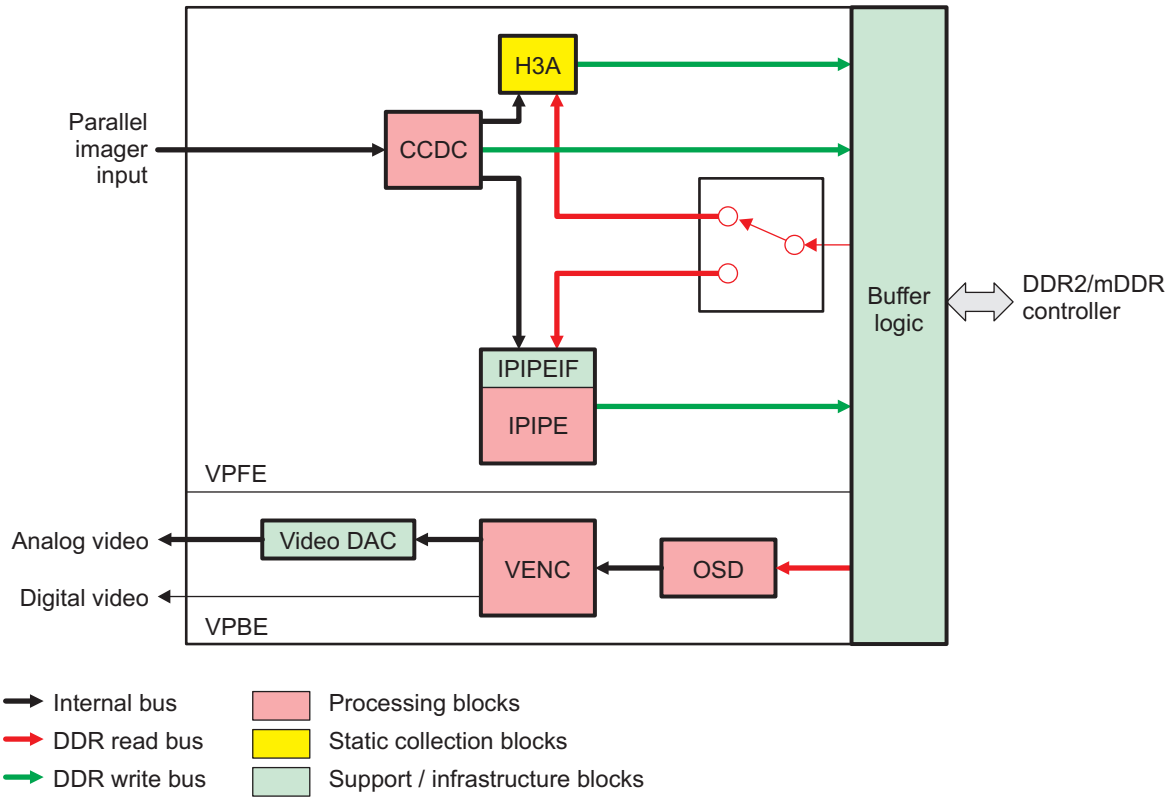


1 Purpose of the Video Processing Back End

The device contains a Video Processing Subsystem (VPSS) that provides an input interface (Video Processing Front End or VPFE) for external imaging peripherals such as image sensors, video decoders, etc., and an output interface, Video Processing Back End (VPBE) for display devices, such as analog SDTV displays, digital LCD panels, HDTV video encoders, etc.

In addition to these peripherals, there is a set of common buffer logic/memory and DMA control to ensure efficient use of the DDR2/mDDR burst bandwidth. The shared buffer logic/memory is a unique block that is tailored for seamlessly integrating the VPSS into an image/video processing system. It acts as the primary source or sink to all the VPFE and VPBE modules that are either requesting or transferring data from/to DDR2/mDDR. In order to efficiently utilize the external DDR2/mDDR bandwidth, the shared buffer logic/memory interfaces with the DMA system via a high bandwidth bus (64-bit wide). The shared buffer logic/memory also interfaces with all the VPFE and VPBE modules via a 128-bit wide bus. The shared buffer logic/memory (divided into the read & write buffers and arbitration logic) is capable of performing the following functions. It is imperative that the VPSS utilize DDR2/mDDR bandwidth efficiently due to both its large bandwidth requirements and the real-time requirements of the VPSS modules.

Figure 2. Video Processing Subsystem Block Diagram



1.1 Features

The video processing back-end (VPBE) block is comprised of the on-screen display (OSD) and the video encoder (VENC) modules. Together, these modules provide the device with a powerful and flexible back-end display interface. These are described below:

- The on-screen display (OSD) graphic accelerator manages display data in various formats for several types of hardware display windows and handles the blending of the display windows into a single display frame, which is then output by the video encoder module.
- The video encoder (VENC) takes the display frame from the OSD and formats it into the desired output format and output signals, including data, clocks, sync, etc. required to interface to display devices. The VENC consists of three primary sub-blocks:
  - The analog video encoder generates the signaling, including video A/D conversion, to interface to

NTSC/PAL television displays.
  - The digital LCD controller supports interfaces to various digital LCD display formats as well as standard digital YUV outputs to interface to Hi-Def video encoders and/or DVI/HDMI interface devices.
  - The timing generator to generate the specific timing required for analog video output as well as various digital video output modes.

1.1.1 On Screen Display (OSD) Features

The primary function of the OSD module is to gather and blend video data and display/bitmap data and then pass it to the video encoder (VENC) in YCbCr format. The video and display data is read from external DDR2/mDDR memory. The OSD is programmed via control and parameter registers. The following are the primary features that are supported by the OSD:

- Support for two video windows and two OSD bitmapped windows that can be displayed simultaneously (VIDWIN0/VIDWIN1 and OSDWIN0/OSDWIN1)
- Video windows support YCbCr data in 422 format from external memory, with the ability to interchange the order of the CbCr component in the 32-bit word
- OSD bitmap windows support 1/2/4/8 bit width index data of color palette
- In addition, one OSD bitmap window at a time can be configured to one of the following:
  - YUV422 (same as video data)
  - RGB format data in 16-bit mode (R=5bit, G=6bit, B=5bit)
  - 24-bit mode (each R/G/B=8bit) with pixel level blending with video windows
- Programmable color palette with the ability to select between a RAM/ROM table with support for 256 colors.
- Support for two ROM tables, one of which can be selected at a given time
- Separate enable/disable control for each window
- Programmable width, height, and base starting coordinates for each window
- External memory address and offset registers for each window
- Support for x2 and x4 zoom in both the horizontal and vertical direction
- Pixel-level blending/transparency/blinking attributes can be defined for OSDWIN0 when OSDWIN1 is configured as an attribute window for OSDWIN0
- Support for blinking intervals to the attribute window
- Ability to select either field/frame mode for the windows (interlaced/progressive)
- An eight-step blending process between the bitmap and video windows
- Transparency support for the bitmap and video data (when a bitmap pixel is zero, there will be no blending for that corresponding video pixel)
- Ability to resize from VGA to NTSC/PAL (640x480 to 720x576) for both the OSD and video windows
- Horizontal rescaling x1.5 is supported
- Support for a rectangular cursor window and a programmable background color selection
- The width, height, and color of the cursor is selectable
- The display priority is: Rectangular-Cursor > OSDWIN1 > OSDWIN0 > VIDWIN1 > VIDWIN0 > background color
- Support for attenuation of the YCbCr values for the REC601 standard.

The following restrictions exist in the OSD module:

- If the vertical resize filter is enabled for either of the video windows, the maximum horizontal window dimension cannot be greater than 720 currently. This is due to the limitation in the size of the line memory.
- It is not possible to use both of the CLUT ROMs at the same time. However, a window can use RAM while another uses ROM.

1.1.2 Video Encoder (VENC) Features

The VENC/DLCD consists of three major blocks: a) the video encoder that generates analog video output, b) the digital LCD controller that generates digital RGB/YCbCr data output and timing signals, and c) the timing generator.

The analog video encoder features are described below

- Master clock Input-27MHz (x2 upsampling)
- SDTV Support
  - Composite NTSC-M, PAL-B/D/G/H/I
  - CGMS/WSS attribute insertion
  - Line 21 Closed caption data encoding
  - Chroma low-pass filter 1.5 MHz/3 MHz
  - Programmable SC-H phase
- 10-bit oversampling D/A converters (27 MHz)
- Optional 7.5% pedestal
- 16-235/0-255 input amplitude selectable
- Programmable luma delay
- Master/slave operation
- Internal color bar generation (100%/75%)

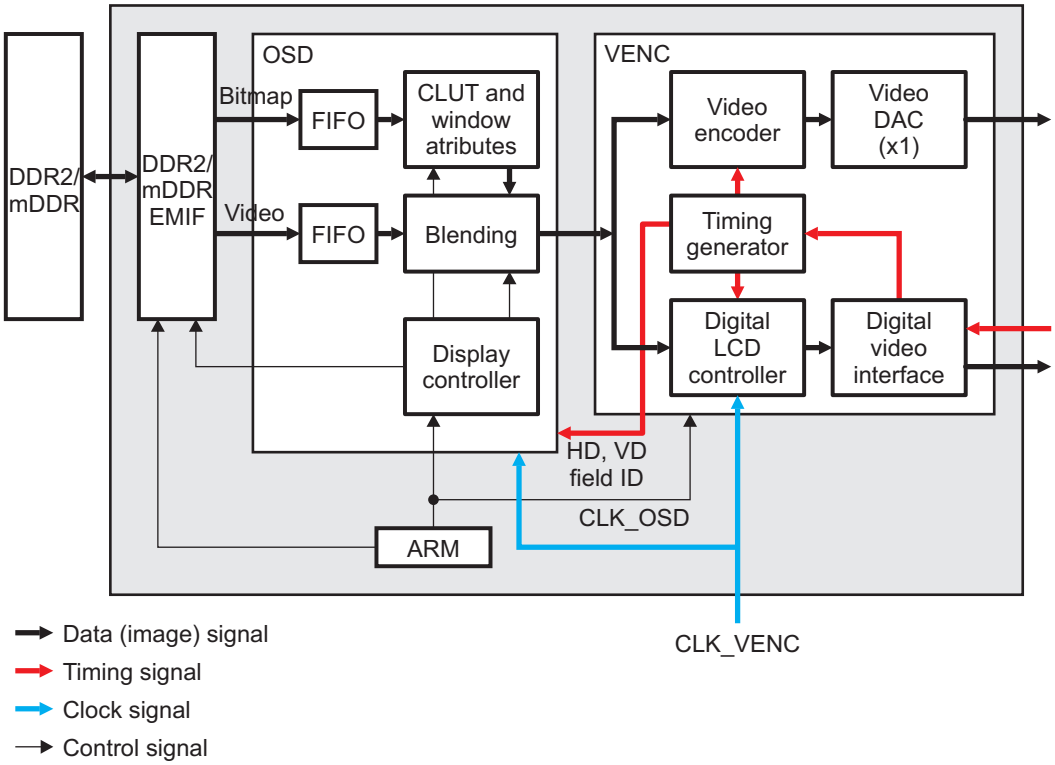
The digital LCD interface features are described below

- Programmable DCLK
- Various output formats
  - YCbCr 16-bit
  - YCbCr 8-bit
  - ITU-R BT. 656
  - Parallel RGB (16/18 bit)
  - Serial RGB
- Low-pass filter for digital RGB output
- Programmable timing generator
- Master/slave operation
- Internal color bar generation (100%/75%)
- 8-bit programable gamma correction

1.2 Functional Block Diagram

Figure 3 shows a high-level functional block diagram of the VPBE functional blocks, along with the different data flow paths.

Figure 3. Video Processing Back End Block Diagram



1.3 Supported Use Case Statement

The VPBE supports image (2-D window) compositing and blending from data stored in DDR2/mDDR memory in various display formats by the OSD module and then data formatting and conversion for display to analog SDTV displays and to digital display devices various modes/formats by the VENC module. YUV output modes have minimal data processing applied and can be passed through directly from YUV input sources to VPFE. Digital RGB and LCD display formats are generated from the OSD's YUV422 output format, as are the analog outputs. The analog DAC outputs supports SDTV with composite output format only.

1.4 Industry Standard(s) Compliance Statement

Analog television standards supported:

- SDTV
  - 525-line / 60 Hz (NTSC-M) or
  - 625-line / 50 Hz (PAL-B/D/G/H/I)

2 Display Subsystem Environment

The VPBE signals are shown in Table 1 below. Note that these signals can take on different meanings depending on the specific interface chosen. In addition, some of these signals are multiplexed with other SoC functions (GIO, PWM, etc.). Pin multiplexing is controlled from the DM35x system module described in the *TMS320DM35x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFB3). The following sections will describe each of the scenarios supported.

Table 1. Interface Signals for Video Processing Back End

Name	Type	PU PD	Reset State	Description	Mux Control
VPBE Digital Signals					
YOUT7-R7	inout		in	Digital Video Out: VENC settings determine function	
YOUT6-R6	inout		in	Digital Video Out: VENC settings determine function	
YOUT5-R5	inout		in	Digital Video Out: VENC settings determine function	
YOUT4-R4	inout		in	Digital Video Out: VENC settings determine function	
YOUT3-R3	inout		in	Digital Video Out: VENC settings determine function	
YOUT2-G7	inout		in	Digital Video Out: VENC settings determine function	
YOUT1-G6	inout		in	Digital Video Out: VENC settings determine function	
YOUT0-G5	inout		in	Digital Video Out: VENC settings determine function	
COUT7-G4 / GIO081 / PWM0	inout		in	Digital Video Out: VENC settings determine function GIO: GIO[081], PWM0	PINMUX1[1:0].COUT_7
COUT6-G3 / GIO080 / PWM1	inout		in	Digital Video Out: VENC settings determine function GIO: GIO[080], PWM1	PINMUX1[3:2].COUT_6
COUT5-G2 / GIO079 / PWM2A / RTO0	inout		in	Digital Video Out: VENC settings determine function GIO: GIO[079], PWM2A, RTO0	PINMUX1[5:4].COUT_5
COUT4-B7 / GIO078 / PWM2B / RTO1	inout		in	Digital Video Out: VENC settings determine function GIO: GIO[078], PWM2B, RTO1	PINMUX1[7:6].COUT_4
COUT3-B6 / GIO077 / PWM2C / RTO2	inout		in	Digital Video Out: VENC settings determine function GIO: GIO[077], PWM2C, RTO2	PINMUX1[9:8].COUT_3
COUT2-B5 / GIO076 / PWM2D / RTO3	inout		in	Digital Video Out: VENC settings determine function GIO: GIO[076], PWM2D, RTO3	PINMUX1[11:10].COUT_2
COUT1-B4 / GIO075 / PWM3A	inout		in	Digital Video Out: VENC settings determine function GIO: GIO[075], PWM3A	PINMUX1[13:12].COUT_1
COUT0-B3 / GIO074 / PWM3B	inout		in	Digital Video Out: VENC settings determine function GIO: GIO[074], PWM3B	PINMUX1[15:14].COUT_0
HSYNC / GIO073	inout	PD	in	Video Encoder: Horizontal Sync GIO: GIO[073]	PINMUX1[16].HVSYNC
VSYNC / GIO072	inout	PD	in	Video Encoder: Vertical Sync GIO: GIO[072]	PINMUX1[16].HVSYNC
LCD_OE / GIO071	inout		in	Video Encoder: Signals valid Video Encoder output GIO: GIO[071]	PINMUX1[17].LCD_OE
FIELD / GIO070 / R2 / PWM3C	inout		in	Video Encoder: Field identifier for interlaced display formats GIO: GIO[070] Digital Video Out: R2 PWM3C	PINMUX1[19:18].FIELD

Table 1. Interface Signals for Video Processing Back End (continued)

Name	Type	PU PD	Reset State	Description	Mux Control
EXTCLK / GIO069 / B2 / PWM3D	inout	PD	in	Video Encoder: External clock input, used if clock rates > 27 MHz are needed, e.g., 74.25 MHz for HDTV digital output GIO: GIO[069] Digital Video Out: B2 PWM3D	PINMUX1[21:20].EXTCLK
VCLK / GIO068	inout		out L	Video Encoder: Video Output Clock GIO: GIO[068]	PINMUX1[22].VCLK
VPBE Analog Signals					
VREF	A inout			Video DAC, Reference voltage output (0.5 V, 0.1 µF to gnd)	
IOUT	A inout			Video DAC: Pre-video buffer DAC output (1000 Ω to VFB)	
IBIAS	A inout			Video DAC: External resistor (2500 Ω to gnd) connection to current bias configuration	
VFB	A inout			Video DAC: Pre-video buffer DAC output (1000 Ω to IOUT, 1070 Ω to TVOUT)	
TVOUT	A inout			Video DAC: Analog Composite NTSC/PAL output (Output of 75 Ω driver, AC couple to TV)	
VDDA18V_DAC	pwr			Video DAC: Analog 1.8 V power	
VSSA_DAC	gnd			Video DAC: Analog 1.8 V ground	

2.1 Analog Display Interface

The analog interface is used for driving NTSC/PAL compatible television displays, video decoders, and other devices with NTSC/PAL compatible display interfaces

2.1.1 Analog Display Signal Interface

Table 2 shows the interface connections for the analog display interface.

Table 2. Interface Signals for Analog Displays

Name	Type	PU PD	Reset State	Description	Mux Control
VREF	A inout			Video DAC: Reference voltage output (0.5V, 0.1uF to gnd)	
IOUT	A inout			Video DAC: Pre-video buffer DAC output (1000 Ω to VFB)	
IBIAS	A inout			Video DAC: External resistor (2550 Ω to gnd) connection for current bias configuration	
VFB	A inout			Video DAC: Pre-video buffer DAC output (1000 Ω to IOUT, 1070 Ω to TVOUT)	
TVOUT	A inout			Video DAC: Analog Composite NTSC/PAL output (Output of 75 Ω driver, AC couple to TV)	
VDDA18V_DAC	pwr			Video DAC: Analog 1.8V power	
VSSA_DAC	gnd			Video DAC: Analog 1.8V ground	

2.1.2 Analog Display Signal Interface Description

The VPBE analog interface includes a single Video DAC signal, a DAC voltage reference and R Bias signals, and separate 1.8v and core power/ground signals. Only 1 DAC is available, supporting composite television signals. The DAC operates at a 27 MHz sampling rate to support SDTV (interlaced, 6.5 MHz bandwidth) signals.

Note: See Section 3.3 for proper configuration of Video DAC. See the data sheet for recommended hardware configuration for the Video DAC and buffer.

2.1.3 Analog Display Signal Interface Timing

This section describes master mode timings. For slave mode timings, please refer to Section 4.5.4.3.

2.1.3.1 Horizontal Timing

The timings, such as location of horizontal sync pulses, color burst position and active video position, are automatically calculated by hardware. Figure 4 shows horizontal timing characteristics. Table 3 shows the parameters of the timing chart. Each parameter is set to conform to standard but can be adjusted by user registers. Independent timing configurations can be available for CVBS and component/RGB output.

Figure 4. Horizontal Timing

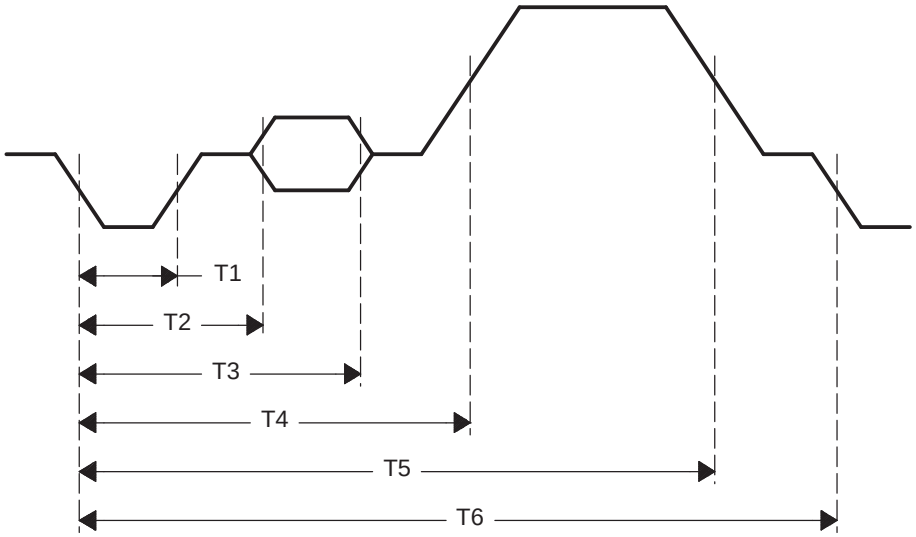


Table 3. Horizontal Timing Parameters (SDTV)

Parameter	Item	NTSC[1]	PAL[1]	CVBS Adjust
T1	Horizontal Sync Pulse Width	127	127	ETMG0.CLSW
T2	H ref to burst start	141	151	ETMG1.CBST
T3	H ref to burst end	210	212	ETMG1.CBSE
T4	H ref to H blanking end	243	263	ETMG1.CLBI
T5	H ref to H blanking start	1683	1703	ETMG1.CFPW
T6	1H	1716	1728	-

(1) Units are in ENC clocks

2.1.3.2 Horizontal Blanking Timing

Some pixels around the horizontal video blanking edge are clipped so that the output video has the proper blanking transition.

This feature is enabled by default but can be disabled by setting the parameter CVBS.CBLS to 1. Table 3 shows the waveforms when blanking edge shaping is enabled and disabled. Section 2.1.3.3 shows the difference of T4 and T5 (see Figure 4 for T4 and T5).

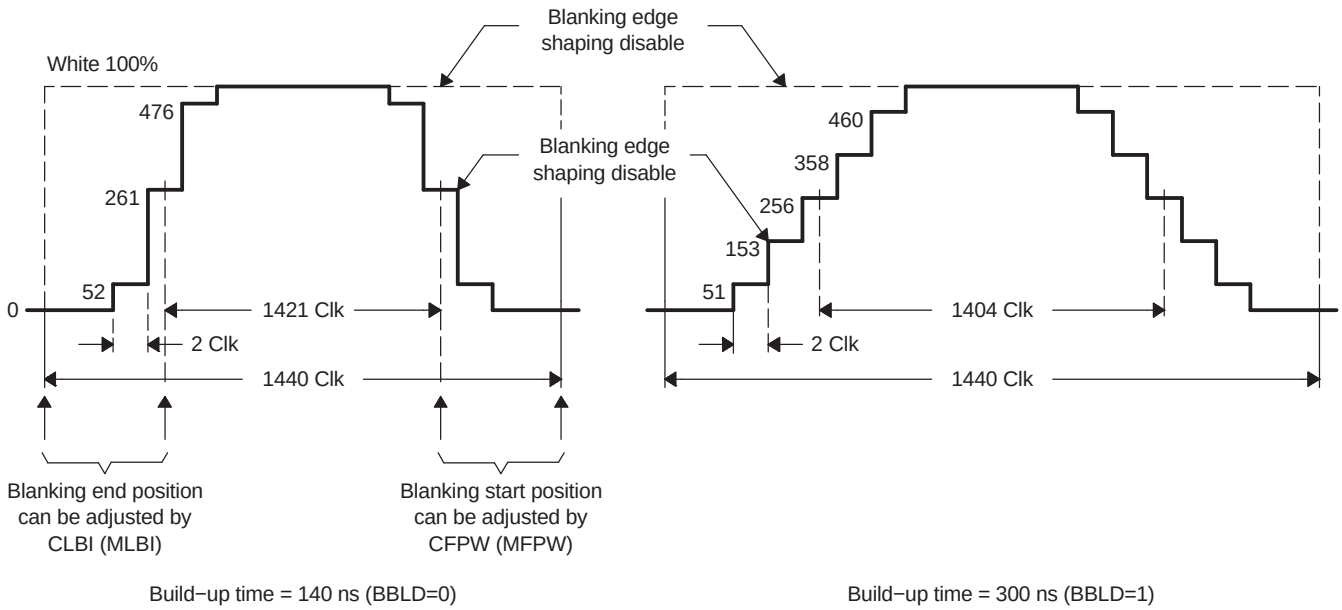
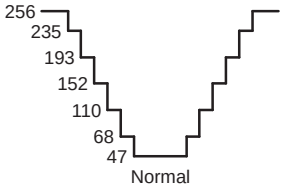


Table 4. Blanking Shaping On/Off

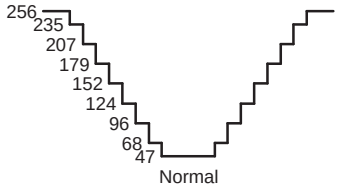
Parameter	NTSC		PAL	
	CVBS.CBLS = 0	CVBS.CBLS = 1	CVBS.CBLS = 0	CVBS.CBLS = 1
T4	252	243	282	263
T5	1673	1683	1686	1703

2.1.3.4 Horizontal Sync Timing

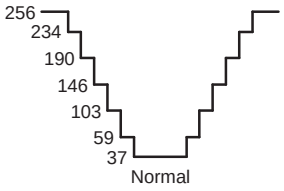
The detail waveform of horizontal sync pulse to be inserted on the luma signal is shown inSection 2.1.3.5. The levels in Section 2.1.3.5 are the internal digital values. The duration of each step is one ENC clock period. The register name in this figure is for CVBS output.



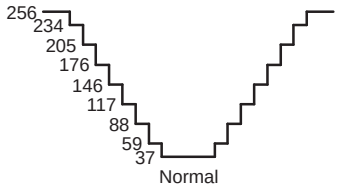
(1) CSBLD=0 (140 ns), CVLVL=0 (286 mV)
(NTSC default)



(2) CSBLD=1 (200 ns), CVLVL=0 (286 mV)



(3) CSBLD=0 (140 ns), CVLVL=1 (300 mV)



(4) CSBLD=1 (200 ns), CVLVL=1 (300 mV)
(PAL default)

2.1.3.6 Vertical Timing

The vertical timing is also controlled by hardware automatically for each mode (NTSC or PAL). Serration and equalization pulses are generated for appropriate lines. The color burst is automatically disabled on appropriate lines.

Figure 5 and Figure 6 show the vertical timing characteristics of NTSC and PAL.

Section 2.1.3.7 and Section 2.1.3.8 show the non-interlaced mode for NTSC and PAL. The non-interlaced mode is activated when VMOD.ITLC = 1. The line number in a field can be selected by VMOD.ITLCL, as shown in Table 5.

Table 5. Number of Lines for Each Scan Mode

VMOD.ITLC	VMOD.ITLCL	Line	
		NTSC	PAL
0	-	262.5	312.5
1	0	262	312
	1	263	313

In these figures, the color burst is denoted as |, ↑ or ↓ marks. For NTSC, | denotes the color burst position. For PAL, ↑ means +135 = , while ↓ means-135 = relative to U. For interlaced NTSC, the video encoder operation starts with the field I in master mode. For interlaced PAL, it starts with the field II.

Figure 5. NTSC Vertical Timing

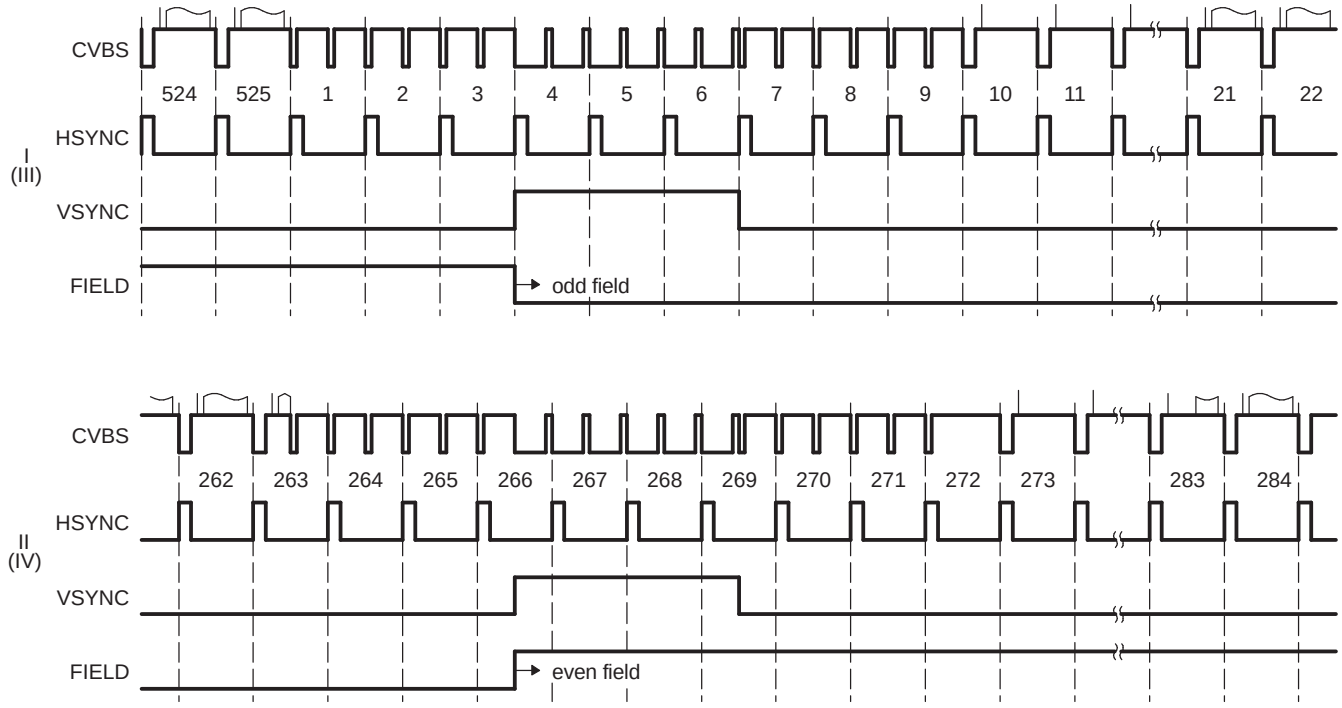
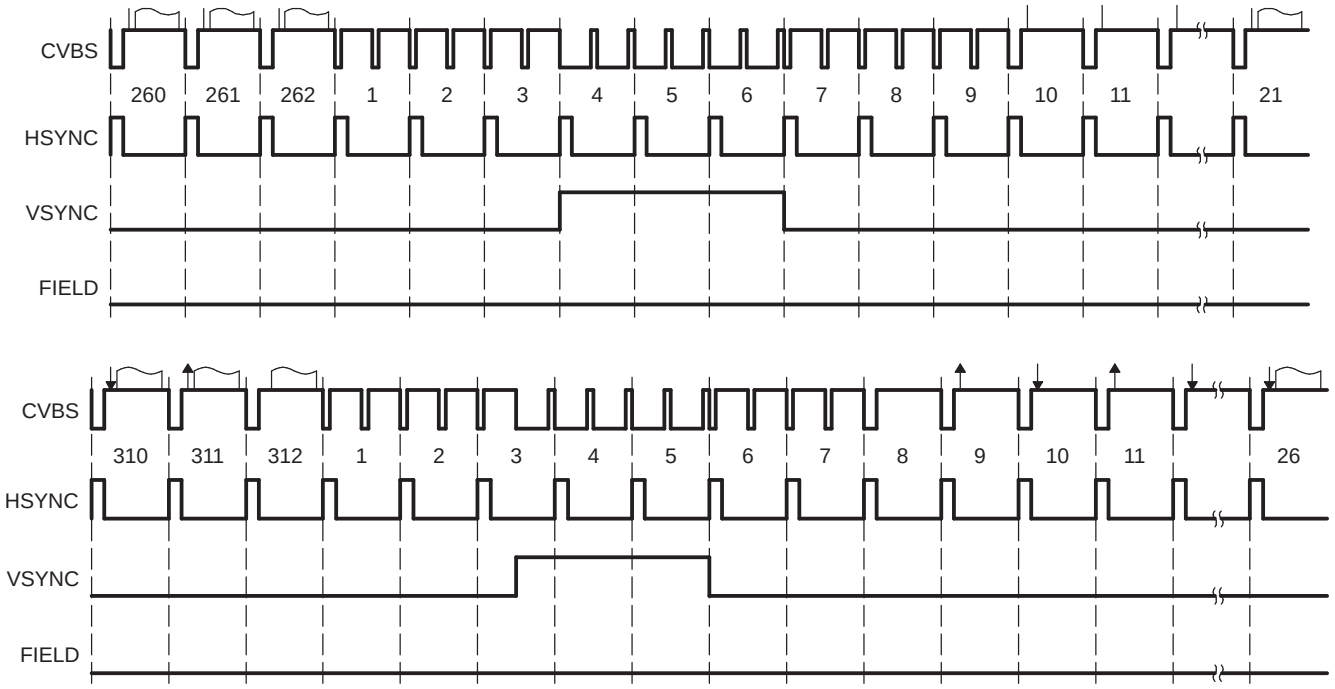


Figure 6. PAL Vertical Timing



2.1.3.9 Internal Color Bar Output Level

The NTSC/PAL encoder can internally generate color bars. Setting VDPRO.CBMD = 1 enables the internal color bar generator. The VDPRO.CBTYP field switches the saturation of the color bar; 0 for 75%, 1 for 100%. Figure 7 and Figure 8 show the digital level of the video encoder when the internal color bar is enabled for each mode.

Figure 7. 100% Color Bar Output Level

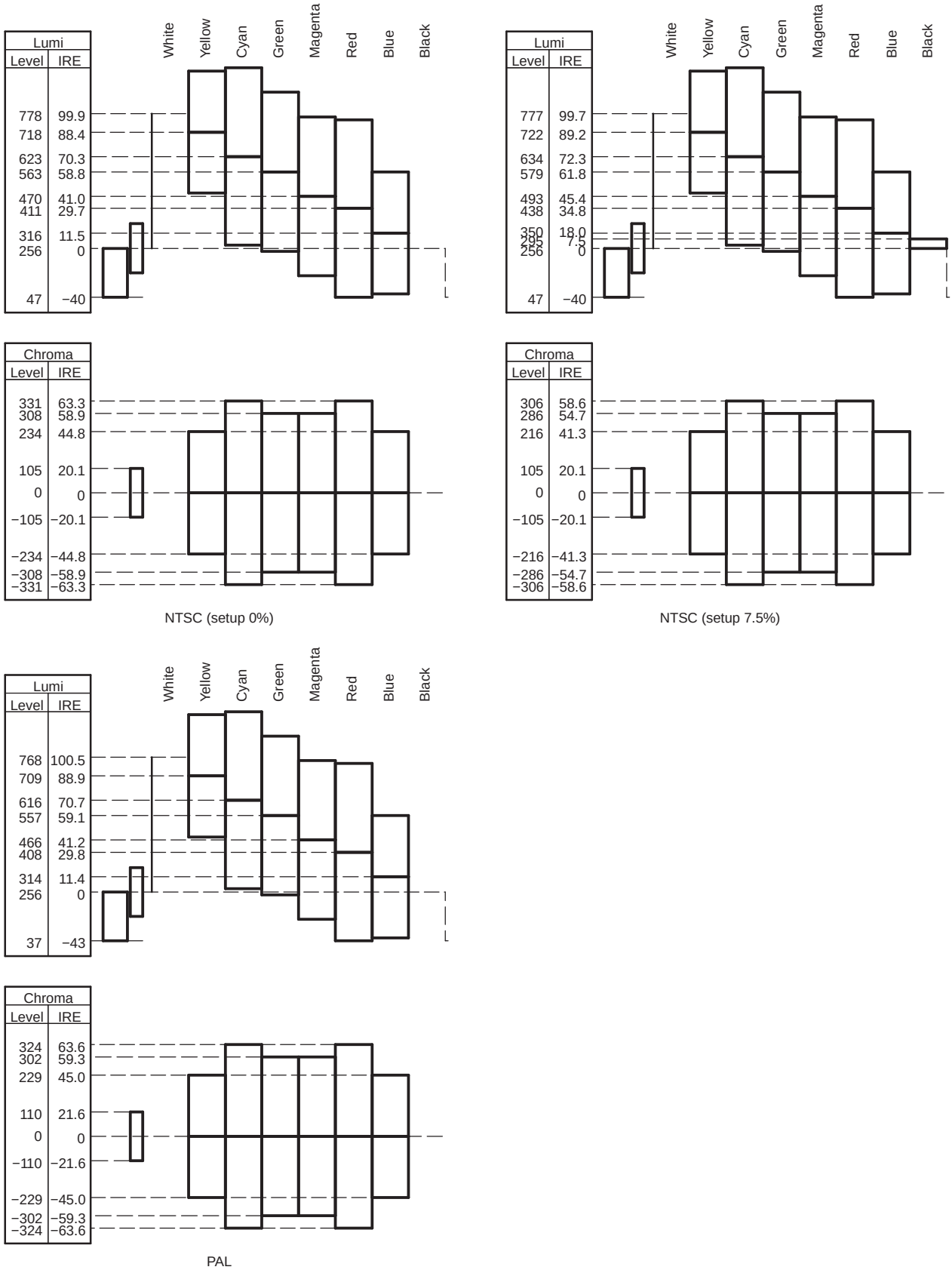
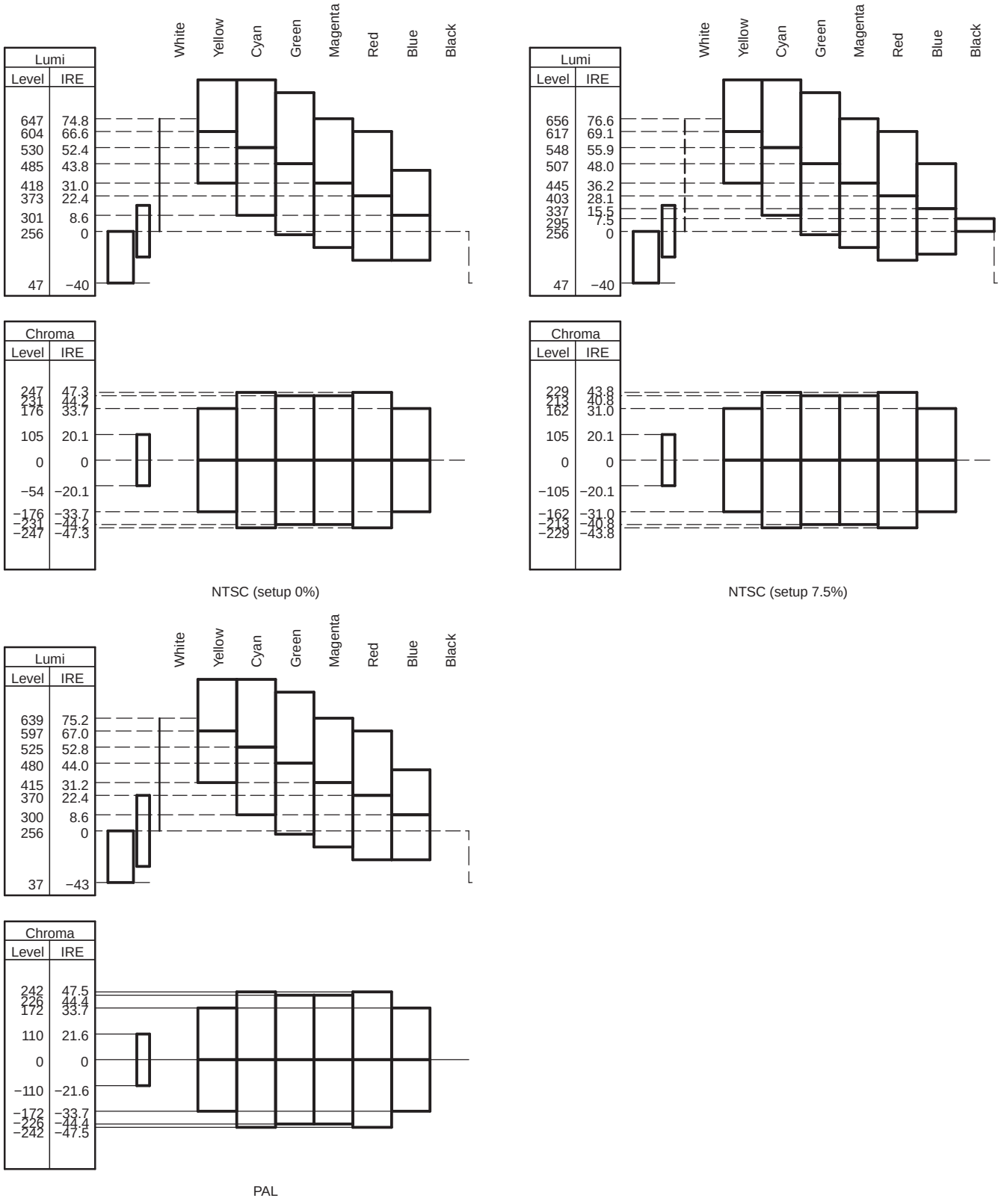


Figure 8. 75% Color Bar Output Level



2.2 Digital Display Interface

The digital display interface is used for driving various types of digital display devices.

Table 6. Digital Display Modes

VDMD	Mode	Description
0	YCC16	16-bit YCbCr output mode. Y and C are output separately on 16bit bus.
1	YCC8	8-bit YCbCr output mode. 422 YCbCr is time-multiplexed on the 8bit bus. Optionally supports ITU-R BT.656 output.
2	PRGB	Parallel RGB mode to output RGB separately.
3	SRGB	Serial RGB mode to output RGB sequentially.

The digital image data output signals support multiple functions / interfaces, depending on the display mode selected. Table 7 describes these modes. Note that Parallel RGB mode with more than 16-bit RGB565 signals requires enabling pin multiplexing to support (i.e., for RGB666 mode).

Table 7. Signals for VPBE Digital Display Modes

Pin Name	YCC16	YCC8 / REC656	PRGB	SRGB
HSYNC GIO073	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC GIO072	VSYNC	VSYNC	VSYNC	VSYNC
LCD_OE GIO071	As needed	As needed	As needed	As needed
FIELD GIO070, R2, PWM3C	As needed	As needed	As needed	As needed
EXTCLK GIO069, B2, PWM3D	As needed	As needed	As needed	As needed
VCLK GIO068	VCLK	VCLK	VCLK	VCLK
YOUT7	Y7	Y7, Cb7, Cr7	R7	DATA 7
YOUT6	Y6	Y6, Cb6, Cr6	R6	DATA 6
YOUT5	Y5	Y5, Cb5, Cr5	R5	DATA 5
YOUT4	Y4	Y4, Cb4, Cr4	R4	DATA 4
YOUT3	Y3	Y3, Cb3, Cr3	R3	DATA 3
YOUT2	Y2	Y2, Cb2, Cr2	G7	DATA 2
YOUT1	Y1	Y1, Cb1, Cr1	G6	DATA 1
YOUT0	Y0	Y0, Cb0, Cr0	G5	DATA 0
COUT7 GIO081, PWM0	C7	Optional	G4	LCD_AC
COUT6 GIO080, PWM1	C6	Optional	G3	LCD_OE
COUT5 GIO079, PWM2A, RTO0	C5	Optional	G2	BRIGHT
COUT4 GIO078, PWM2B, RTO1	C4	Optional	B7	PWM

Table 7. Signals for VPBE Digital Display Modes (continued)

Pin Name	YCC16	YCC8 / REC656	PRGB	SRGB
COUT3 GIO077, PWM2C, RTO2	C3	Optional	B6	CSYNC
COUT2 GIO076, PWM2D, RTO3	C2	Optional	B5	-
COUT1 GIO075, PWM3A	C1	Optional	B4	-
COUT0 GIO074, PWM3B	C0	Optional	B3	-

2.2.1 YCC16 Signal Interface

In YCC16 mode, the Y (luma) signal is output to YOUT[7:0] at every VCLK rising edge, while Cb and Cr (chroma) are alternately multiplexed onto COUT[7:0]. The order of chroma output is controlled by YCCCTL.YCP. Data is only output when the LCD_OE signal is asserted. Otherwise the output signals are held low. Table 8 shows the interface connections for the YCC16 digital display interface.

Table 8. Interface Signals For YCC16 Digital Displays

Name	TYPE	PU PD	Reset State	Description	Function Control / Mux Control
YOUT7-R7	inout		in	YOUT7 signal	VENC.VDMD = 0
YOUT6-R6	inout		in	YOUT6 signal	VENC.VDMD = 0
YOUT5-R5	inout		in	YOUT5 signal	VENC.VDMD = 0
YOUT4-R4	inout		in	YOUT4 signal	VENC.VDMD = 0
YOUT3-R3	inout		in	YOUT3 signal	VENC.VDMD = 0
YOUT2-G7	inout		in	YOUT2 signal	VENC.VDMD = 0
YOUT1-G6	inout		in	YOUT1 signal	VENC.VDMD = 0
YOUT0-G5	inout		in	YOUT0 signal	VENC.VDMD = 0
COUT7-G4 / GIO081 / PWM0	inout		in	COUT7 signal	VENC.VDMD = 0 PINMUX1[1:0], COUT_7 = 1
COUT6-G3 / GIO080 / PWM1	inout		in	COUT6 signal	VENC.VDMD = 0 PINMUX1[3:2], COUT_6 = 1
COUT5-G2 / GIO079 / PWM2A / RTO0	inout		in	COUT5 signal	VENC.VDMD = 0 PINMUX1[5:4], COUT_5 = 1
COUT4-B7 / GIO078 / PWM2B / RTO1	inout		in	COUT4 signal	VENC.VDMD = 0 PINMUX1[7:6], COUT_4 = 1
COUT3-B6 / GIO077 / PWM2C / RTO2	inout		in	COUT3 signal	VENC.VDMD = 0 PINMUX1[9:8], COUT_3 = 1
COUT2-B5 / GIO076 / PWM2D / RTO3	inout		in	COUT2 signal	VENC.VDMD = 0 PINMUX1[11:10], COUT_2 = 1

Table 8. Interface Signals For YCC16 Digital Displays (continued)

Name	TYPE	PU PD	Reset State	Description	Function Control / Mux Control
COUT1-B4 / GIO075 / PWM3A	inout		in	COUT1 signal	VENC.VDMD = 0 PINMUX1[13:12], COUT_1 = 1
COUT0-B3 / GIO074 / PWM3B	inout		in	COUT0 signal	VENC.VDMD = 0 PINMUX1[15:14], COUT_0 = 1
HSYNC / GIO073	inout	PD	in	Video encoder: Horizontal SYNC GIO: GIO[073]	PINMUX1[16], HVSYNC = 0
VSYNC / GIO072	inout	PD	in	Video encoder: Vertical SYNC GIO: GIO[072]	PINMUX1[16], HVSYNC = 0
LCD_OE / GIO071	inout		in	Video encoder: Signals valid Video Encoder output GIO: GIO[071]	PINMUX1[17], LCD_OE = 0 (if needed)
FIELD / GIO070 / R2 / PWM3C	inout		in	Video encoder: Field identifier for interlaced display formats GIO: GIO[070], Digital Video Out: R2, PWM3C	PINMUX1[19:18], FIELD = 1 (if needed)
EXTCLK / GIO069 / B2 / PWM3D	inout	PD	in	Video encoder: External clock input, used if clock rates > 27MHz are needed, e.g., 74.25 MHz for HDTV digital output. GIO: GIO[069], Digital Video Out: B2, PWM3D	PINMUX1[21:20], EXTCLK = 1 (if needed)
VCLK / GIO068	inout		out L	Video encoder: Video output clock GIO: GIO[068]	PINMUX1[22], VCLK = 0

2.2.1.1 YCC16 Signal Interface Description

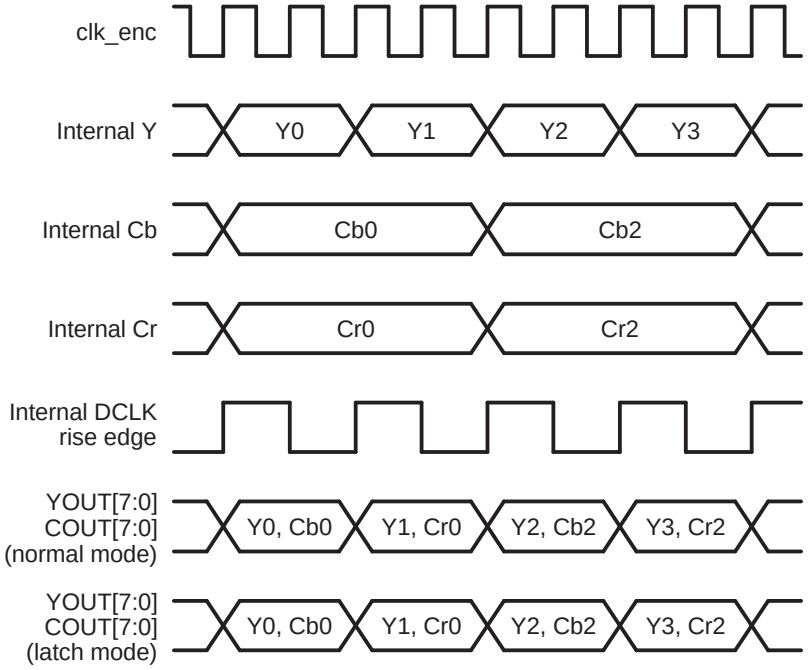
The YCC16 interface includes the 8-bit YOUT[7:0] and COUT[7:0] signals, along with the HSYNC, VSYNC, and VCLK signals. An optional EXTCLK input clock can be used if the internally generated VPBE clock is not fast enough (i.e., to support HDTV display rates or any clock > 54 MHz).

Note that the YOUT/COUT busses can be swapped via the VIDCTL.YCSWAP register setting.

2.2.1.2 YCC16 Protocol and Data Formats

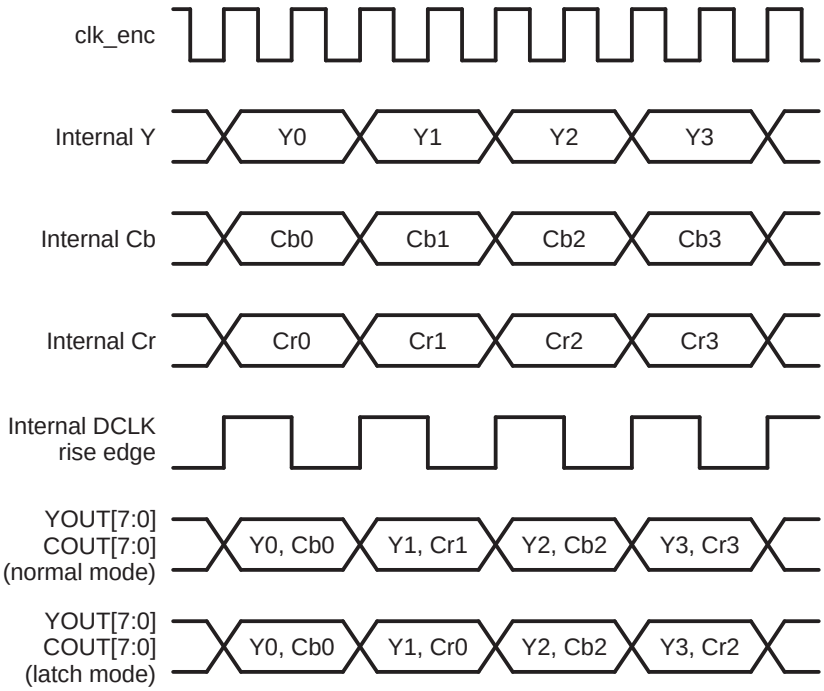
Figure 9 shows the output data sampling of the input YUV422 resolution signal from the OSD module for video windows. Video window input data is YUV422 format natively and RGB888 input data is chroma subsampled via boxcar averaging to YUV422 resolution.

Figure 9. YCC16 Output for Normal OSD Operation



The OSD also includes support for window data in bitmap format, either 1,2,4, or 8-bit resolution via a YUV Color Look Up Table (CLUT) or via RGB565 bitmap format. Data corresponding to bitmap pixels is in full YUV444 resolution and is overlaid onto the YUV422 resolution video window pixel output. In this case, chroma blurring can occur at the edge between bitmap windows and the rest of the OSD image. In normal operation, the chroma value output from VENC is the immediate value at the sampling time. However, to alleviate this chroma blurring, a “latch” mode is provided where the chroma output for the second pixel in a UV pair can be the data latched at the first pixel. The latch mode is enabled by setting YCCCTL.CHM to 1.

Figure 10. YCC16 Output When OSD Window in RGB565



2.2.2 YCC8 Signal Interface, Including ITU-R-BT.656

In YCC8 mode, each component of the OSD YCbCr signal is alternately output from YOUT[7:0]. The default output order is Cb-Y-Cr-Y but this can be modified by YCCCTL.YCP. Table 9 shows the interface connections for the YCC8 digital display interface.

Table 9. Interface Signals For YCC8 Digital Displays

Name	TYPE	PU PD	Reset State	Description	Function Control / Mux Control
YOUT7-R7	inout		in	YOUT7/COUT7 signal	VENC.VDMD = 1 Use YOUT, but for 8-bit data: VENC.VIDCTL.YCSWAP = 0
YOUT6-R6	inout		in	YOUT6/COUT6 signal	
YOUT5-R5	inout		in	YOUT5/COUT5 signal	
YOUT4-R4	inout		in	YOUT4/COUT4 signal	
YOUT3-R3	inout		in	YOUT3/COUT3 signal	
YOUT2-G7	inout		in	YOUT2/COUT2 signal	
YOUT1-G6	inout		in	YOUT1/COUT1 signal	
YOUT0-G5	inout		in	YOUT0/COUT0 signal	
COUT7-G4 / GIO81 / PWM0	inout		in	YOUT7/COUT7 signal	VENC.VDMD = 0 Use YOUT, but for 8-bit data: VENC.VIDCTL.YCSWAP = 1 PINMUX1[1:0]. COUT_7 = 1 PINMUX1[3:2]. COUT_6 = 1 PINMUX1[5:4].COUT_5 = 1 PINMUX1[7:6]. COUT_4 = 1 PINMUX1[9:8]. COUT_3 = 1 PINMUX1[11:10]. COUT_2 = 1 PINMUX1[13:12]. COUT_1 = 1 PINMUX1[15:14]. COUT_0 = 1
COUT6-G3 / GIO80 / PWM1	inout		in	YOUT6/COUT6 signal	
COUT5-G2 / GIO79 / PWM2A / RTO0	inout		in	YOUT5/COUT5 signal	
COUT4-B7 / GIO78 / PWM2B / RTO1	inout		in	YOUT4/COUT4 signal	
COUT3-B6 / GIO77 / PWM2C / RTO2	inout		in	YOUT3/COUT3 signal	
COUT2-B5 / GIO76 / PWM2D / RTO3	inout		in	YOUT2/COUT2 signal	
COUT1-B4 / GIO75 / PWM3A	inout		in	YOUT1/COUT1 signal	
COUT0-B3 / GIO74 / PWM3B	inout		in	YOUT0/COUT0 signal	
HSYNC / GIO073	inout	PD	in	Video encoder: Horizontal Sync GIO: GIO[073]	PINMUX1[16]. HVSYNC = 0
VSYNC / GIO072	inout	PD	in	Video encoder: Vertical Sync GIO: GIO[072]	PINMUX1[16]. HVSYNC = 0
LCD_OE / GIO071	inout		in	Video Encoder: Signals valid video encoder output GIO: GIO[071]	PINMUX1[17]. LCD_OE = 0 (if needed)

Table 9. Interface Signals For YCC8 Digital Displays (continued)

Name	TYPE	PU PD	Reset State	Description	Function Control / Mux Control
FIELD / GIO070 / R2 / PWM3C	inout		in	Video encoder: Field identifier for interlaced display formats GIO: GIO[070], Digital video out: R2, PWM3C	PINMUX1[19:18]. FIELD = 1 (if needed)
EXTCLK / GIO069 / B2 / PWM3D	inout	PD	in	Video encoder: External clock input, used if clock rates > 27MHz are needed, e.g., 74.25 MHz for HDTV digital output. GIO: GIO[069], Digital video out: B2, PWM3D	PINMUX1[21:20]. EXTCLK = 1 (if needed)
VCLK / GIO068	inout		out L	Video encoder: Video output clock GIO: GIO[068]	PINMUX1[22]. VCLK = 1

2.2.2.1 YCC8 Signal Interface Description

The YCC8 interface includes the 8-bit YOUT[7:0] or the 8-bit COUT[7:0] signals, along with the HSYNC, VSYNC, and VCLK signals. An optional EXTCLK input clock can be used if the internally generated VPBE clock is not fast enough (i.e., to support HDTV display rates or any clock > 27 MHz).

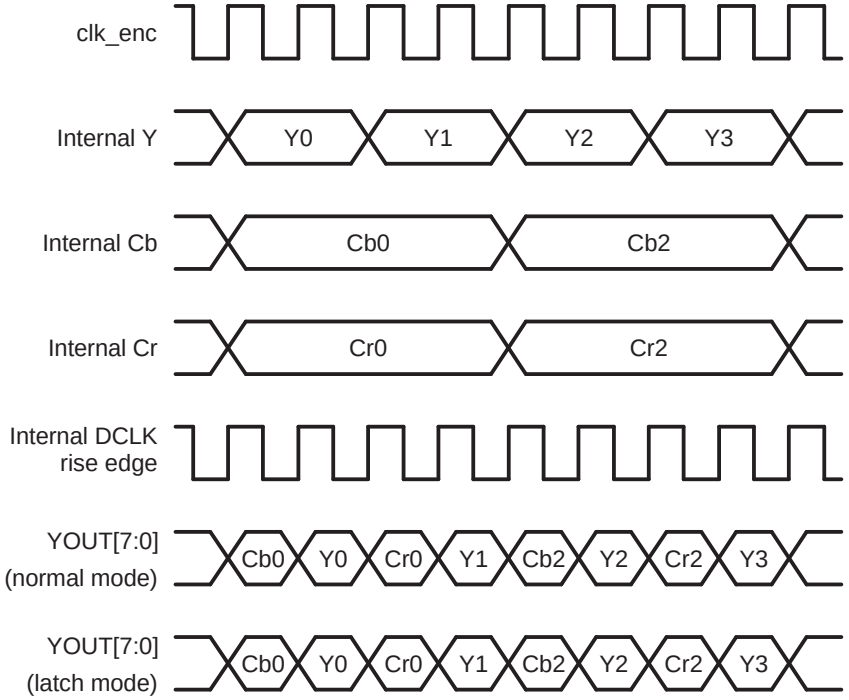
Note that in YCC8 mode, data is normally output on the YOUT bus. However, the YOUT/COUT busses can be swapped via the VIDCTL.YCSWAP register setting to output the YCC8 data on the COUT bus.

ITU-R BT.656 format output is optionally available in YCC8 mode and is enabled via YCCCTL.R656. In this mode, the YCbCr output timing and output order is fixed by hardware in order to conform to the standard and they cannot be altered by the user. To use BT656 mode, the VENC must operate in the standard mode (VIDCTL.VDMD=0). Note that this mode operates correctly only when the pixel clock frequency is half of the VENC clock. In this mode, the sync signals are embedded within the data stream and HSYNC/VSYNC are inactive.

2.2.2.2 YCC8 Protocol and Data Formats

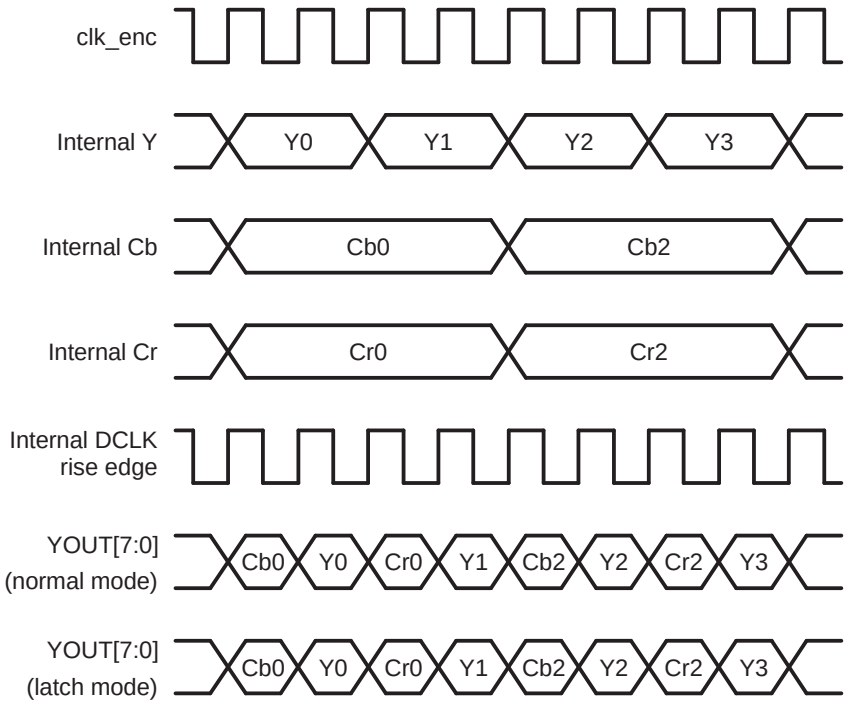
Figure 11 shows the output data sampling of the input YUV422 resolution signal from the OSD module for video windows. Video window input data is YUV422 format natively and RGB888 input data is chroma subsampled via boxcar averaging to YUV422 resolution.

Figure 11. YCC8 Output for Normal OSD Operation



The OSD also includes support for window data in bitmap format, either 1,2,4, or 8-bit resolution via a YUV Color Look Up Table (CLUT) or via RGB565 format. Data corresponding to bitmap pixels is in full YUV444 resolution and is overlaid onto the YUV422 resolution video window pixel output. In this case, chroma blurring can occur at the edge between bitmap windows and the rest of the OSD image. In normal operation, the chroma value output from VENC is the immediate value at the sampling time. However, to alleviate this chroma blurring, a “latch” mode is provided where the chroma output for the second pixel in a UV pair can be the data latched at the first pixel. The latch mode is enabled by setting YCCCTL.CHM to 1.

Figure 12. YCC8 Output When OSD Window in RGB565



2.2.3 Parallel RGB Signal Interface

For parallel RGB modes, up to 18-bit RGB display data is output in parallel. The upper bits of the RGB samples are multiplexed onto the YOUT and COUT pins, with the lower bits assigned to GIO pins. Output data is subsampled at the DCLK rising edge when the data valid signal (LCD_OE) is asserted and output signals are held low when LCD_OE is deasserted.

Table 10. Interface Signals For Parallel RGB Digital Displays

Name	TYPE	PU PD	Reset State	Description	Function Control / Mux Control
VPBE Digital Signals					
YOUT7-R7	inout		in	R7 signal	VENC.VDMD = 2
YOUT6-R6	inout		in	R6 signal	
YOUT5-R5	inout		in	R5 signal	
YOUT4-R4	inout		in	R4 signal	
YOUT3-R3	inout		in	R3 signal	
YOUT2-G7	inout		in	G7 signal	
YOUT1-G6	inout		in	G6 signal	
YOUT0-G5	inout		in	G5 signal	
COUT7-G4 / GIO081 / PWM0	inout		in	G4 signal	VENC.VDMD = 2 PINMUX1[1:0]. COUT_7 = 1 PINMUX1[3:2]. COUT_6 = 1 PINMUX1[5:4]. COUT_5 = 1 PINMUX1[7:6]. COUT_4 = 1 PINMUX1[9:8]. COUT_3 = 1 PINMUX1[11:10]. COUT_2 = 1 PINMUX1[13:12]. COUT_1 = 1 PINMUX1[15:14]. COUT_0 = 1
COUT6-G3 / GIO080 / PWM1	inout		in	G3 signal	
COUT5-G2 / GIO079 / PWM2A / RTO0	inout		in	G2 signal	
COUT4-B7 / GIO078 / PWM2B / RTO1	inout		in	B7 signal	
COUT3-B6 / GIO077 / PWM2C / RTO2	inout		in	B6 signal	
COUT2-B5 / GIO076 / PWM2D / RTO3	inout		in	B5 signal	
COUT1-B4 / GIO075 / PWM3A	inout		in	B4 signal	
COUT0-B3 / GIO074 / PWM3B	inout		in	B3 signal	
HSYNC / GIO073	inout	PD	in	Video encoder: Horizontal Sync GIO: GIO[073]	PINMUX1[16]. HVSYNC = 0
VSYNC / GIO072	inout	PD	in	Video encoder: Vertical Sync GIO: GIO[072]	PINMUX1[16]. HVSYNC = 0
LCD_OE / GIO071	inout		in	Video encoder: Signals valid video encoder output GIO: GIO[071]	PINMUX1[17]. LCD_OE = 0 (if needed)
FIELD / GIO070 / R2 / PWM3C	inout		in	Video encoder: Field identifier for interlaced display formats GIO: GIO[070], Digital video out: R2, PWM3C	PINMUX1[19:18], FIELD = 1 or PINXMUX1[19:18].FIELD = 2 (if needed)

Table 10. Interface Signals For Parallel RGB Digital Displays (continued)

Name	TYPE	PU PD	Reset State	Description	Function Control / Mux Control
VPBE Digital Signals					
EXTCLK / GIO069 / B2 / PWM3D	inout	PD	in	Video encoder: External clock input, used if clock rates > 27MHz are needed (e.g., 74.25 MHz for HDTV digital output). GIO: GIO[069], Digital video out: B2, PWM3D	PINMUX1[21:20], EXTCLK = 1 or PINMUX1[21:20], EXTCLK = 2 (if needed)
VCLK / GIO068	inout		out L	Video encoder: Video output clock GIO: GIO[068]	PINMUX1[22], VCLK = 0

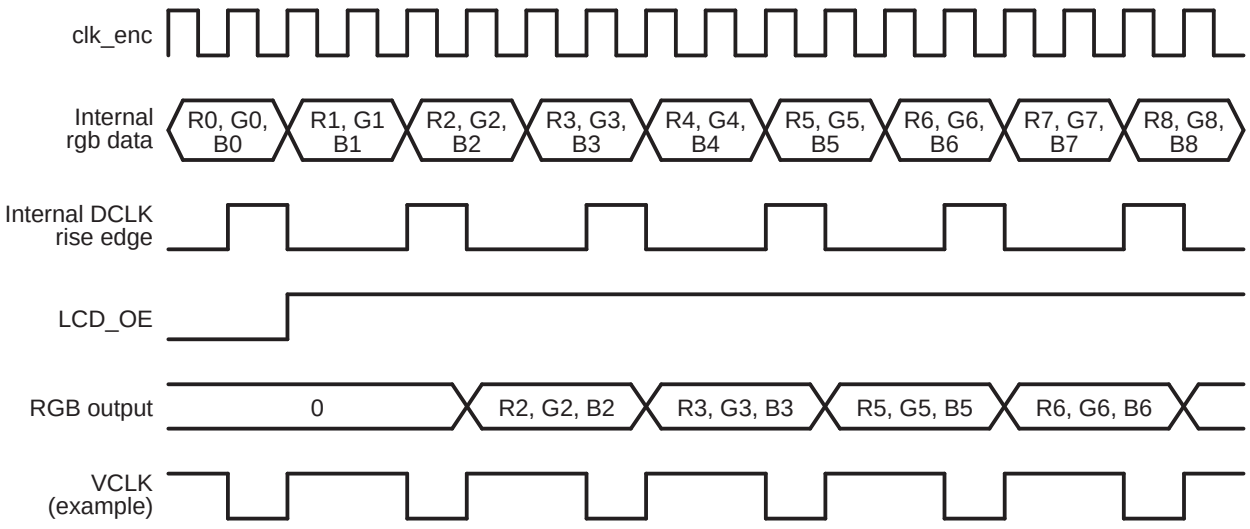
2.2.3.1 Parallel RGB Signal Interface Description

In parallel RGB mode, an RGB565 interface (5-bits Red, 6-bits Green, 5-bits Blue) can be supported via the normal YOUT/COUT signals without requiring additional GIO signals. In addition to this, RGB666 mode can be supported by assigning additional GIO pins to the display interface. Note that RGB666 mode precludes use of the EXTCLK and FIELD signals since the multiplexed functions overlap with the same GIO signals. This assignment is done via the pin multiplexing is controlled from the DM35x system module described in the *TMS320DM35x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFB3). In addition to these signals, the HSYNC, VSYNC, and VCLK signals are also output. An optional EXTCLK input clock can also be used in RGB565 mode.

2.2.3.2 Parallel RGB Protocol and Data Formats

Figure 13 shows the output data sampling of the input YUV422 signal from the OSD module converted by the VENC to parallel RGB format. In this diagram, the values R0, G0, B0, etc. refer to pixel locations.

Figure 13. RGB Output in Parallel RGB Mode



2.2.4 Serial RGB Signal Interface

For serial RGB modes, the RGB data samples are output serially, multiplexed onto the 8-bit YOUT bus. Output data is subsampled at DCLK rising edge when data valid signal (LCD_OE) is asserted and output signals are held low when LCD_OE is deasserted.

Table 11. Interface Signals For Serial RGB Digital Displays

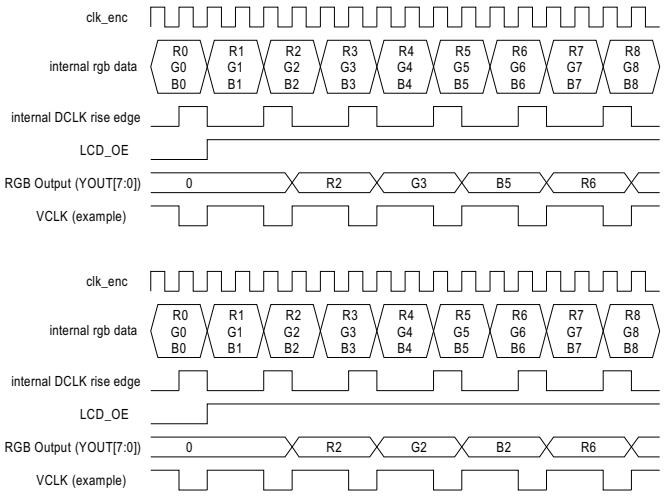
Name	TYPE	PU PD	Reset State	Description	Function Control / Mux Control
VPBE Digital Signals					
YOUT7-R7	inout		in	Data7 signal	VENC.VDMD = 3
YOUT6-R6	inout		in	Data6 signal	
YOUT5-R5	inout		in	Data5 signal	
YOUT4-R4	inout		in	Data4 signal	
YOUT3-R3	inout		in	Data3 signal	
YOUT2-G7	inout		in	Data2 signal	
YOUT1-G6	inout		in	Data1 signal	
YOUT0-G5	inout		in	Data0 signal	
COUT7-G4 / GIO081 / PWM0	inout		in	LCD_AC	VENC.LCDOUT.ACE = 1 PINMUX1[1:0].COUT_7 = 1
COUT6-G3 / GIO080 / PWM1	inout		in	LCD_OE	VENC.LCDOUT.OEE = 1 PINMUX1[3:2].COUT_6 = 1
COUT5-G2 / GIO079 / PWM2A / RTO0	inout		in	BRIGHT	VENC.LCDOUTBRE = 1 PINMUX1[5:4].COUT_5 = 1
COUT4-B7 / GIO078 / PWM2B / RTO1	inout		in	PWM	VENC.LCDOUT.PWME = 1 PINMUX1[7:6].COUT_4 = 1
COUT3-B6 / GIO077 / PWM2C / RTO2	inout		in	CSYNC	PINMUX1[9:8].COUT_3 = 1
COUT2-B5 / GIO076 / PWM2D / RTO3	inout		in		
COUT1-B4 / GIO075 / PWM3A	inout		in		
COUT0-B3 / GIO074 / PWM3B	inout		in		
HSYNC / GIO073	inout	PD	in	Video encoder: Horizontal SYNC GIO: GIO[073]	PINMUX1[16] .HVSYNC = 0
VSYNC / GIO072	inout	PD	in	Video encoder: Vertical SYNC GIO: GIO[072]	PINMUX1[16]. HVSYNC = 0
LCD_OE / GIO071	inout		in	Video encoder: Signals valid video encoder output GIO: GIO[071]	PINMUX1[17]. LCD_OE = 0 (if needed)
FIELD / GIO070 / R2 / PWM3C	inout		in	Video encoder: Field identifier for interlaced display formats GIO: GIO[070], Digital video out: R2, PWM3C	PINMUX1[19:18]. FIELD = 1 (if needed)
EXTCLK / GIO069 / B2 / PWM3D	inout	PD	in	Video encoder: External clock input, used if clock rates > 27MHz are needed (e.g., 74.25 MHz for HDTV digital output). GIO: GIO[069], Digital video out: B2, PWM3D	PINMUX1[21:20]. EXTCLK = 1 (if needed)
VCLK / GIO068	inout		out L	Video encoder: Video output clock GIO: GIO[068]	PINMUX1[22]. VCLK = 1

2.2.4.1 Serial RGB Signal Interface Description

In Serial RGB mode, each component of RGB is output from YOUT[7:0] in rotation. The rotation order can be specified by the RGBOF or RGBEF fields in RGBCTL and different orders can be set for two different line IDs. RGBOF is for odd fields (line ID=0) while RGBEF is for even fields (Line ID=1). The order is reset at HSYNC and rotated at the internal DCLK rising edge on valid data duration (LCD_OE=1). While LCD_OE is de-asserted, the output data is tied to zero.

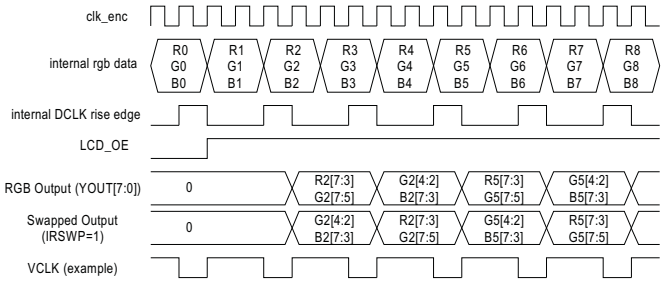
2.2.4.1.1 Serial RGB Protocol and Data Formats

Section 2.2.4.1.2 shows the output data sampling of the input YUV422 signal from the OSD module converted by the VENC to RGB format.



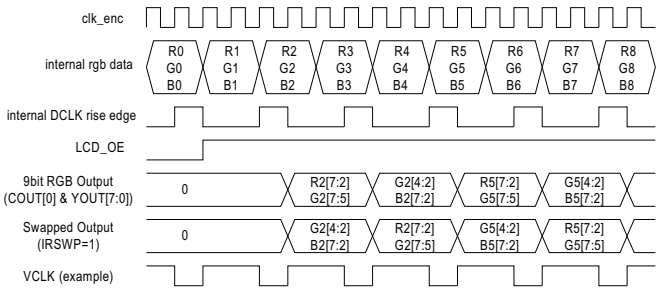
2.2.4.1.4 IronMan Mode

Optionally, IronMan-type rotation is provided. Setting RGBCTL.IRONM to 1 activates IronMan mode. In this mode, R[7:3], G[7:2] and B[7:3] are concatenated into a 16-bit bus signal, then output in a time-multiplexed fashion as shown in Section 2.2.4.1.5. The time-multiplexed order can be swapped by setting RGBCTL.IRSWP to 1.



2.2.4.1.6 9-Bit IronMan Mode

The 9-bit IronMan mode is enabled when RGBCTL.IRONM and RGBCTL.IR9 are set to 1. In this mode, R[7:2], G[7:2] and B[7:2] are concatenated into a 18-bit bus then output as shown in Section 2.2.4.1.7. The MSB is assigned to COUT0. As in 8-bit IronMan mode, the order can be swapped by RGBCTL.IRSWP.

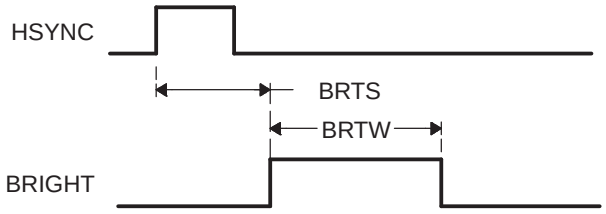


2.2.5 Other Digital LCD Interface Signals

The following LCD signals can be optionally generated. Utilize them as appropriate. See Table 7 for the signal availability in each mode.

2.2.5.1 Bright

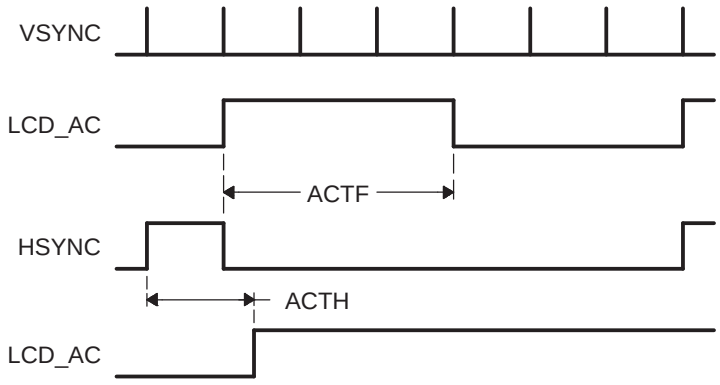
- Polarity can be inverted via LCDOUT.BRP.
- When using the BRIGHT signal, set LCDOUT.BRE to 1.
- The units of BRTS and BRTW are in VCLK periods.



2.2.5.3 LCD_AC

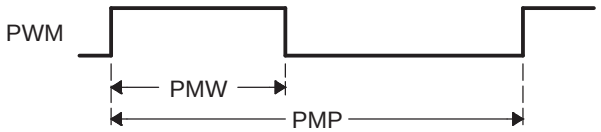
When using the LCD_AC signal, set LCDOUT.ACE to 1.

The units of ACCTL.ACTH and ACCTL.ACTF are VCLK and line, respectively.



2.2.5.5 Pulse Width Modulation (PWM) Signal

To use the PWM signal, set LCDOUT.PWME to 1. Polarity can be inverted by LCDOUT.PWMP. This is a free-run signal and not synchronized to any sync signals. The unit is VCLK. In Section 2.2.5.6, PWM = register PWMW and PMP = register PWMP.



2.3 VPBE Display Subsystem I/O Multiplexing

The various VPBE digital display modes have unique pin multiplexing options as shown in Table 12. Some of these settings are controlled in the System Module, described in detail in the *TMS320DM35x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFB3). The remaining settings are controlled via the mode in which the controller is placed.

Table 12. Signals for VPBE Digital Display Modes

Pin Name	YCC16	YCC8/REC656	PRGB	SRGB
HSYNC GIO073	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC GIO072	VSYNC	VSYNC	VSYNC	VSYNC
LCD_OE GIO071	As needed	As needed	As needed	As needed
FIELD GIO070, R2, PWM3C	As needed	As needed	As needed	As needed
EXTCLK GIO069, B2, PWM3D	As needed	As needed	As needed	As needed
VCLK GIO068	VCLK	VCLK	VCLK	VCLK
YOUT7	Y7	Y7,Cb7,Cr7	R7	Data7
YOUT6	Y6	Y6,Cb6,Cr6	R6	Data6
YOUT5	Y5	Y5,Cb5,Cr5	R5	Data5
YOUT4	Y4	Y4,Cb4,Cr4	R4	Data4
YOUT3	Y3	Y3,Cb3,Cr3	R3	Data3
YOUT2	Y2	Y2,Cb2,Cr2	G7	Data2
YOUT1	Y1	Y1,Cb1,Cr1	G6	Data1
YOUT0	Y0	Y0,Cb0,Cr0	G5	Data0
COUT7 GIO081, PWM0	C7	optional	G4	LCD_AC
COUT6 GIO080, PWM1	C6	optional	G3	LCD_OE
COUT5 GIO079, PWM2A, RTO0	C5	optional	G2	BRIGHT
COUT4 GIO078, PWM2B, RTO1	C4	optional	B7	PWM
COUT3 GIO077, PWM2C, RTO2	C3	optional	B6	CSYNC
COUT2 GIO076, PWM2D, RTO3	C2	optional	B5	-
COUT1 GIO075, PWM3A	C1	optional	B4	-
COUT0 GIO074, PWM3B	C0	optional	B3	-

2.3.1 RGB666 Output Mode Pin Muxing

Allocation of GIO signals for the RGB666 mode of the parallel RGB video out is done in the system module via the PINMUX1 register as shown in Table 13. Enabling PWM3x or PEXTCLK/FIELD options usurps the B2 or R2 pin, respectively, and prevents proper RGB666 operation.

Proper RGB666 operation requires setting PINMUX1.EXTCLK to 10 and PINMUX1.FIELD to 10.

Table 13. RGB666 Pin Multiplexing Control

EXTCLK	FIELD	EXTCLK / GIO[69] / B2 / PWM3D	FIELD / GIO[70] / R2 / PWM3DC
00	x	GIO[69]	x
01	x	EXTCLK	x
10	x	B2	x
11	x	PWM3D	x
x	00	x	GIO[70]
x	01	x	FIELD
x	10	x	R2
x	11	x	PWM3DC

2.3.2 CCD and LCD Control Signal Multiplexing

The LCD controller in the VPBE requires additional control signals for certain modes of operation multiplexed to some of the COUT signals. Each of these signals has a separate enable bit in the VENC.LCDOUT register which selects between the control signal function and other VPBE functions. Note that for these controls to be effective, the signals must first be configured to be VPBE pins via the PINMUX1 register.

2.3.3 Pin Multiplexing Control Registers

2.3.3.1 PINMUX1 Register

The PINMUX1 register is shown in Figure 14 and described in Table 14. The address for this register is 0x01C4:0004.

Figure 14. PINMUX1 Register

31	23	22	21	20	19	18	17	16
Reserved		VCLK	EXTCLK		FIELD		DLCD	HYSYNC
R-0		R/W-0	R/W-0		R/W-0		R/W-0	R/W-0

15	14	13	12	11	10	9	8
COUT_0		COUT_1		COUT_2		COUT_3	
R/W-0		R/W-0		R/W-0		R/W-0	

7	6	5	4	3	2	1	0
COUT_4		COUT_5		COUT_6		COUT_7	
R/W-0		R/W-0		R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 14. PINMUX1 Register Field Descriptions

Bit	Field	Value	Description
31-23	Reserved		Reserved. Must be set to zero.
22	VCLK		Enable VCLK
		0	VCLK
		1	GIO[68]
21-20	EXTCLK		Enable EXTCLK (Video Out pin mux)
		0	GIO[69]
		1h	EXTCLK
		2h	B2
		3h	PWM3
19-18	FIELD		Enable FIELD (Video Out pin mux)
		0	GIO[70]
		1h	FIELD
		2h	R2
		3h	PWM3
17	DCLD		Enable DLCD signal output (Video Out pin mux)
		0	LCD_OE or BRIGHT (set by LDCOUT.OES)
		1	GIO[71]
16	HYSYNC		Enable HVSYNC (Video Out pin mux)
		0	HVSYNC and VSYNC
		1	GIO[73:72]
15-14	COUT_0		Enable COUT[0] (Video Out pin mux)
		0	GIO[74]
		1h	COUT[0]
		2h	PWM3
13-12	COUT_1		Enable COUT[1] (Video Out pin mux)
		0\	GIO[75]
		1h	COUT[1]
		2h	PWM3
		3h	Reserved
11-10	COUT_2		Enable COUT[2] (Video Out pin mux)
		0	GIO[76]
		1h	COUT[2]
		2h	PWM2
		3h	RTO3
9-8	COUT_3		Enable COUT[3] (Video Out pin mux)
		0	GIO[77]
		1h	COUT[3]
		2h	PWM2
		3h	RTO2
7-6	COUT_4		Enable COUT[4] (Video Out pin mux)
		0	GIO[78]
		1h	COUT[4]
		2h	PWM2
		3h	RTO1

Table 14. PINMUX1 Register Field Descriptions (continued)

Bit	Field	Value	Description
5-4	COUT_5		Enable COUT[5] (Video Out pin mux)
		0	GIO[79]
		1h	COUT[5]
		2h	PWM2
		3h	RTO0
3-2	COUT_6		Enable COUT[6] (Video Out pin mux)
		0	GIO[80]
		1h	COUT[6]
		2h	PWM1
		3h	Reserved
1-0	COUT_7		Enable COUT[7] (Video Out pin mux)
		0	GIO[81]
		1h	COUT[7]
		2h	PWM0
		3h	Reserved

3 VPBE Integration

This section describes how the VPBE subsystem in integrated into the DMSoC.

3.1 Clocking, Reset, and Power Management Scheme

3.1.1 Clocks

3.1.1.1 Processing and DMA Clock

The device VPBE module is a DMA master and resides in the PLL1/4 clock domain. This clock is the VPSS Master module in the Power Sleep Controller (PSC) and it is shared with the VPFE. Thus, this clock can be gated off to conserve power, but this will also preclude use of the VPFE. The VPBE modules utilize auto clock gating on a clock-by- clock basis to conserve dynamic power during periods of inactivity.

In addition, the VPBE clocks can be gated off via the VPSS Clock Control register VPSSCLK.CLKCTRL.VPBE_CLK. Note that the clock should only be disabled when the VPBE is not operational. The clocks should be enabled prior to any other operations on the VPBE (including reading/writing other registers).

3.1.1.2 Register Interface Clock

The VPBE module includes a slave port for the control registers that reside in the PLL1/4 clock domain. This clock is the VPSS slave module in the PSC and it is shared with the VPFE. Thus, this clock can be gated off to conserve power, but this will also preclude use of the VPFE.

3.1.1.3 DAC and External Clock

The device must interface with a variety of LCDs, as well as the video DAC module. There are many different types of LCDs, which require many different specific frequencies. The range of frequencies that the pin interface needs to run is 6.25 MHz to 75 MHz.

The external clock domain (6.25 MHz to 75 MHz) is asynchronous to the internal or system clock domain, which is at the PLL1/4 clock rate. The external clock domain can get its clock from four sources:

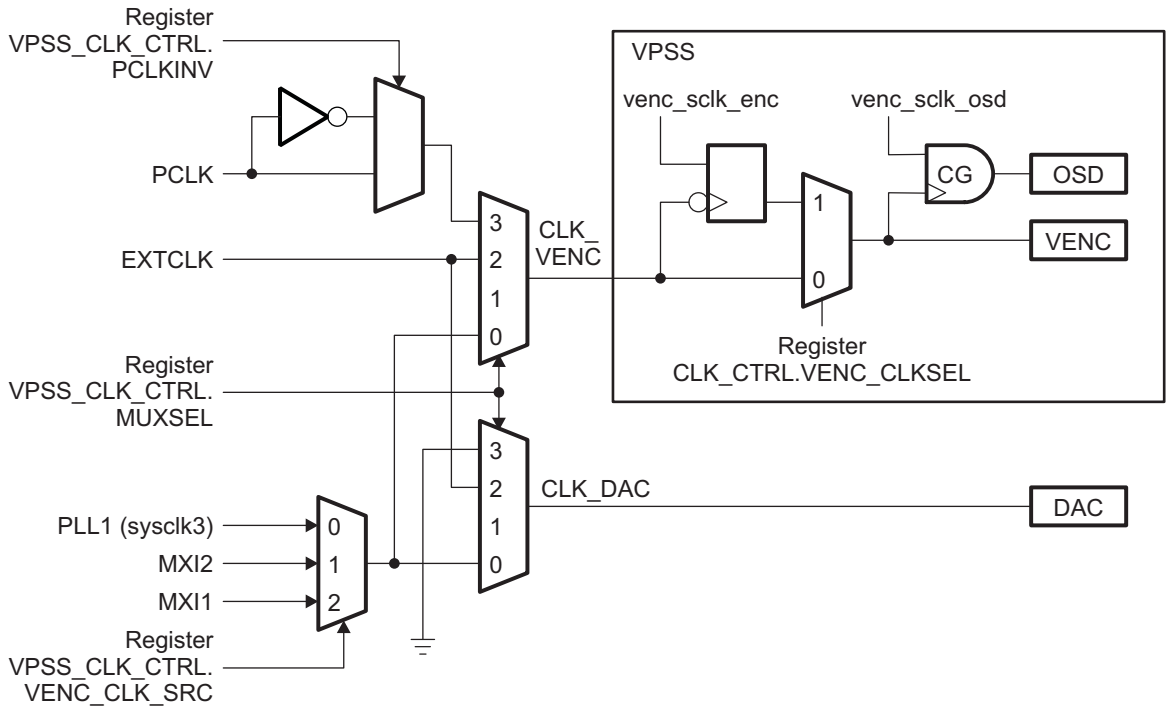
- The PLL1 SYSCLK3 domain (1/n PLL1). Note: Use the proper 1/n divisor to get 27 MHz from the input clock if the video DAC is used.)

- MXI1 crystal/oscillator
- MXI2 crystal/oscillator (backup option if 27 MHz derived from PLL1 is not usable)
- EXTCLK input pin, or the VPFE pixel clock input (PCLK)

The video DAC is hooked up to the VENC module that is inside the VPBE. The data flow between the VPBE and DACs is synchronous. The various clocking modes possible are shown in Figure 15.

The DACs can also have their clocks independently gated off when the DACs are not being used.

Figure 15. VPBE/DAC Clocking Options



The VPBE clock control is in the System module in the VPSS_CLK_CTRL register.

- **Primary Clock mode, MUXSEL = 0:** Both the VENC and DAC get their clock from the source selected by VPSS_CLK_SRC.
  1. 0: PLL1 divided down
  2. 1: MXI2 (27 MHz backup option, see: USB_PHY_CTRL.VPSS_OSCPWDN)
  3. 2: MXI1 (24 MHz, or 27 MHz without USB)
- **Reserved MUXSEL = 1:** Reserved mode
- **EXTCLK mode, MUXSEL = 2:** Both the DAC and VENC receive the EXTCLK. The VENC optionally can divide this frequency by 2, for the VENC, which allows use of the DAC at 27 MHz if driving in 54 MHz on EXTCLK via **VPSSCLK.CLKCTRL.VENC_CLKSEL**.
- **PCLK mode, MUXSEL = 3:** The VENC receives the PCLK. The video DAC receives no clock, and should be disabled. PCLK can be inverted for negative edge support, selectable by the MMR bit.

In addition to the clock multiplex control, the VPSS_CLK_CTRL register also includes controls for enable/disable of the DAC clock – DACCLKEN and enable/disable of the VPBE clock – VENCCLKEN. Finally, the VPBE clock itself can be separately gated via VPBE Clock Control register VPSSCLK.CLKCTRL.VPBE_CLK.

3.1.1.4 VPSS Clock Mux Control Register (VPSS_CLK_CTRL)

The VPSS clock mux control register (VPSS_CLK_CTRL) is shown in Figure 16 and described in Table 15. The address for this register is 0x01C7:0004.

Figure 16. VPSS Clock Mux Control Register (VPSS_CLK_CTRL)

31	16
Reserved	
R-0	

15	7	6	5	4	3	2	1	0
Reserved		VENC_CLK_SRC		DACCLKEN	VENCLKEN	PCLKINV	MUXSEL	
R-0		R/W-0		R/W-0	R/W-0	R/W-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 15. VPSS Clock Mux Control Register (VPSS_CLK_CTRL) Field Descriptions

Bit	Field	Value	Description
31-7	Reserved	0	Reserved
6-5	VENC_CLK_SRC		27 MHz input source
		0	PLL1 divided down
		1	(EXTCRYSTAL2) External crystal 2
		2h	(EXTCRYSTAL1) External crystal 1
		3h	Reserved
4	DACCLKEN		Video DAC clock enable
		0	Disabled
		1	Enabled
3	VENCLKEN		VPBE/Video encoder clock enable
		0	Disabled
		1	Enabled
2	PCLK_INV		Invert VPFE pixel clock (PCLK)
		0	Disable VENC clock mux and CCDC receive normal PCLK
		1	Enable VENC clock mux and CCDC receive inverted PCLK
1-0	VPSS_MUXSEL	0-3h	VPSS clock selection
		0	Use input set by VENC_CLK_SRC (typically 27 MHZ).
		1h	Reserved
		2h	EXTCLK mode. Use external VPBE clock input (DAC clock = EXTCLK).
		3h	PCLK mode. Use PCLK from VPFE (DAC clock = off).

3.1.1.5 MXI2 Oscillator Power Control

When using the alternate oscillator input for the VPBE, power on the oscillator via the VPSS_OSCPDWN field in the USB_PHY_CTRL register. The register address is 0x01C4:0034.

Figure 17. USB Physical Control Register (USB_PHY_CTRL)

31	16
Reserved	
R - 0	

15	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		DATAPOL	PHYCLKSRC		PHYCLKGD	SESNDEN	VBDTCTEN	VBUSENS	PHYPLLON	Reserved	VPSSOSCPDWN	OTGPDWN	PHYPDWN
R - 0		R/W- 0	R/W-0		R/W-0	R/W-1	R/W-1	R-0	R/W-0	R-0	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 16. USB Physical Control Register (USB_PHY_CTRL) Field Descriptions

Bit	Field	Value	Description
31 - 12	Reserved		Reserved
11	DATAPOL		USB PHY data polarity inversion
		0	USB PHY data polarity, no inversion
		1	USB PHY data polarity inversion
10 - 9	PHYCLKSRC		USB PHY input clock source
		0	24 MHz directly from crystal
		1h	12 MHz (after dividing 36 MHz crystal by 3)
		2h	{PLLCTRL1.SYSCLK3) backup in case 27 MHz crystal is used.
		3h	Reserved
8	PHYCLKGD		USB PHY power and clock good
		0	BAD - PHY power not ramped or PLL not locked
		1	GOOD - PHY power is good and PLL is locked
7	SESNDEN		Session end comparator enable
		0	DISABLE - Comparator disabled
		1	ENABLE - Comparator enabled
6	VBDTCTEN		VBUS comparator enabled
		0	DISABLE - Comparators (except session end) disabled
		1	ENABLE - Comparators (except session end) enabled
5	VBUSENS		OTG analog block VBUSSENSE output status
		0	ABSENT - VBUS not present (<0.5 V)
		1	PRESENT - VBUS present (>0.5 V)
4	PHYPLLON		USB PHY PLL suspend override
		0	Normal PLL operation
		1	Override PLL suspend state
3	Reserved		Reserved
2	VPSS OSCPDWN		VPSS oscillator power down control
		0	VPSS MXI2 powered on
		1	VPSS MXI2 power off
1	OTGPDWN		USB OTG analog block power down control
		0	OTG analog block powered on
		1	OTG analog block power off
0	PHYPDWN		USB PHY power down control
		0	PHY powered on
		1	PHY power off

3.1.2 Resets

The device VPBE module resets are tied to the device reset signals.

The VPBE is a subset of the VPSS module and has two module domains, the VPSS Master processing domain and the VPSS Slave register interface. Thus, resetting either of these will affect the VPFE as well.

CAUTION

Do not use the SyncReset or SwRstDisable states of the PSC for either the VPSS Master or VPSS Slave modules.

3.1.3 Power Domain and Power Management

The device VPBE module resides in the “Always On” power domain, along with the ARM core and most other peripherals. When enabled, the VPFE modules utilize auto clock gating on a clock-by-clock basis to conserve dynamic power during periods of inactivity. Active power consumption can also be managed proactively via numerous clock enable/disable controls.

3.1.3.1 Minimize Active Power

To completely disable the VPSS module and all logic gated by external clocks:

- Disable the VPSS master module in the PSC (use Disable only; not SwRstDisable). This will disable the clock to the VPSS logic and the VPSS shared DMA logic and memory buffers. Note that this also disables the VPFE logic.
- Disable the VPSS slave module in the PSC (useDisable only; not SwRstDisable). This will disable the clock to the VPSS register interface. Note that this also disables the register interface for the VPFE modules.

To disable any other clocks to the VPBE:

- Disable any external imaging device driving the VPFE pixel clock (PCLK) to avoid clocking any input logic and any of the VPBE logic via pass-through.
- Disable any external EXTCLK source to avoid clocking any output logic.
- Stop the DAC clock directly via SYSTEM.VPSS_CLK_CTRL.DACCLKEN = 0.
- Stop Gamma table, digital LCD, and analog video encoder clocks via VENC.CLKCTL.

3.1.3.2 Minimize Active Power When only VPBE is Used (VPFE is Disabled)

VPBE-only mode: Clock gate VPFE only, but keep VPBE active:

- Disable the clocks to the VPFE modules via VPSSCLK.CLKCTRL (i.e., CCDC_CLK, IPIPE_CLK, H3A_CLK).
- Disable any external imaging device driving the VPFE pixel clock (PCLK) to avoid clocking any input logic and any of the VPBE logic via pass-through.

VPBE digital-only mode: Clock gate video DAC:

- Stop the DAC clock directly via SYSTEM.VPSS_CLK_CTRL.DACCLKEN = 0.
- Stop analog video encoder clock via VENC.CLKCTL.
- Stop gamma table clock via VENC.CLKCTL, if not used.

Note: When PCLK is used for VPBE (CLK_VENC), the DAC clock is automatically disabled: SYSTEM.VPSS_CLK_CTRL.VPSS_MUXSEL = 3.

3.1.3.3 Minimize Active Power When Only VPFE is Used (VPBE is Disabled)

VPFE-only mode: Clock gate VPBE only, but keep VPFE active:

- Gate CLK_VENC by stopping it at the source (at the clock input pin or via SYSTEM.VPSS_CLK_CTRL.VENCCLKEN = 0).
- Gate CLK_DAC by stopping it at the source (at the clock input pin or via SYSTEM.VPSS_CLK_CTRL.DACCLKEN = 0).

VPFE-only mode: Other options:

- Gate all VPBE clocks off via VPSSCLK.CLKCTRL.VPBE_CLK = 0.
- Disable the video encoder (VENC) operation via VENC.VMOD.VENC = 0.

3.2 Hardware Requests

3.2.1 Interrupt Requests

The device OSD and VENC can generate interrupts to the ARM as shown in Table 17. This indicates an end-of-frame event, i.e., processing has completed for a frame.

Table 17. ARM Interrupts - VPBE

INT Number	Acronym	Source	VPBE Options
0 - 8	VPSSINT0 - 8	VPSS, configurable via the VPSSBL.INTSEL register	OSDINT, VENCINT

3.2.2 EDMA Requests

The OSD and VENC interrupt events can also be used to trigger EDMA as shown in Table 18. This indicates an end-of-frame event, i.e., processing has completed for a frame.

Table 18. EDMA Interrupts

EVT Number	Acronym	Source	VPBE Options
4 - 7	VPSSEVT1 - 4	VPSS, configurable via register: VPSSBL.EVTSEL	OSDINT, VENCINT

3.3 Video DAC Configuration

The Video DACs are recommended to be configured per the following table settings via the VDAC_CONFIG register in the System module. Capacitive coupling is not supported.

- TRESB4R4 = 0x3
- TRESB4R2 = 0x8
- TRESB4R1 = 0x8
- TRIMBITS = 0x34
- PWD_BGZ = 1 (power-up VREF)
- SPEED = 1 (faster)
- PWD_VBUFZ = 1 (power-up video buffer)
- ACCUP_EN = 0 (default 1)
- DINV = 1 (invert)

3.3.1 Video DAC Configuration Register (VDAC CONFIG)

The video DAC configuration register (VDAC CONFIG) is shown in Figure 18 and described in Table 19. The address for this register is 0x01C4:002C.

Figure 18. Video DAC Configuration Register (VDAC CONFIG)

31	30	29	26	25
Reserved		TRESB4R4		TRESB4R2
R - 0		R/W - 0xC		R/W - 0x8

22	21	20	19	18	17
TRESB4R2			TRESB4R1		TRIMBITS
R/W - 0x8			R/W - 0xC		R/W - 0x37

				11	10	9	8
TRIMBITS					PWD_BGZ	SPEED	TVINT
R/W - 0x37					R/W - 0	R/W - 1	R - 0

7	6	4	3	2	1	0
PWD_VBUFZ	VREFSET		ACCUP_EN	DINV	POWER_OK	DAC_DMEN
R/W - 0	R/W - 3		R/W - 1	R/W - 1	R/W - 1	R - 0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 19. Video DAC Configuration Register (VDAC CONFIG) Field Descriptions

Bit	Field	Value	Description
31 - 30	Reserved		Reserved
29 - 26	TRESB4R4		TRESB4R4
25 - 22	TRESB4R2		TRESB4R4
21 - 17	TRESB4R1		TRESB4R4
17 - 11	TRIMBITS		TRIMBITS
10	PWD_BGZ		Power Down of VREF_ active low
		0	DISABLE - power down
		1	ENABLE - power up
9	SPEED		Faster operation of VREF transfer
		0	DISABLE - normal
		1	ENABLE - faster
8	TVINT		TV cable connect status from DAC
		0	Cable connected
		1	Cable disconnected
7	PWD_VBUFZ		Video buffer power down
		0	DISABLE - power down
		1	ENABLE - power up
6 - 4	VREFSET		Video buffer VREF setting
3	ACCUP_EN		Video buffer AC capacitor external coupling
		0	Disable the coupling
		1	Enable the coupling
2	DINV		VENC data inversion (inside the DAC)
		0	No inversion - use only when VDAC is used without VREF and buffer
		1	Inversion - when VDAC is used with VREF and buffer
1	POWER_OK		Reserved for test purposes; reserved from application perspective
0	DAC_DMEN		DAC DMEN eFuse

3.4 VPBE Top-Level Register Mapping Summary

The VPSS module memory map is described in Table 20.

Table 20. VSPP Module Register Map

Address	Peripheral	Description
0x01C7:0000	VPSSCLK	VPSS clock control
0x01C7:0080	H3A	VPFE - Hardware 3A
0x01C7:0100	IPIPEIF	VPFE - Image pipe IF
0x01C7:0200	OSD	VPBE - On screen display
0x01C7:1000	IPIPE	VPFE - Image pipe

4 VPBE Functional Description

4.1 Block Diagram

The VPSS block diagram is shown in Figure 19. Additional detailed block diagrams are shown in the Interface and Image Processing subsections.

Figure 19. Video Processing Subsystem Block Diagram

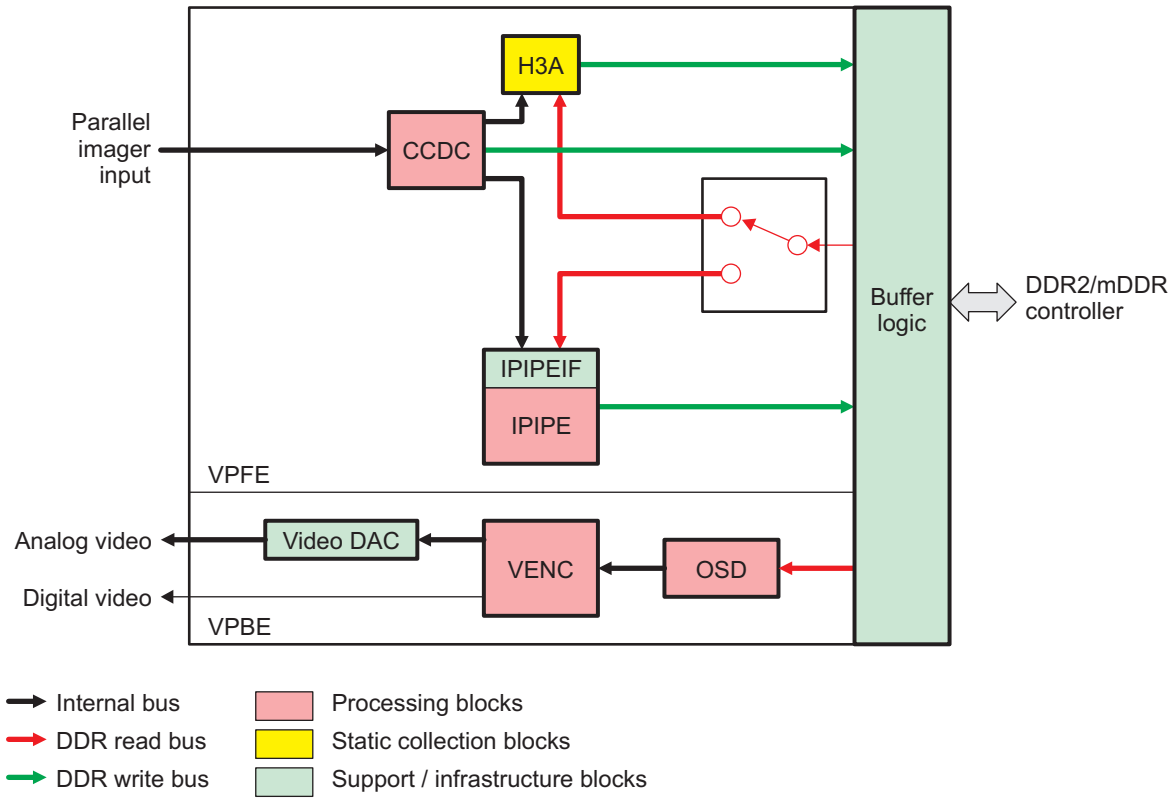
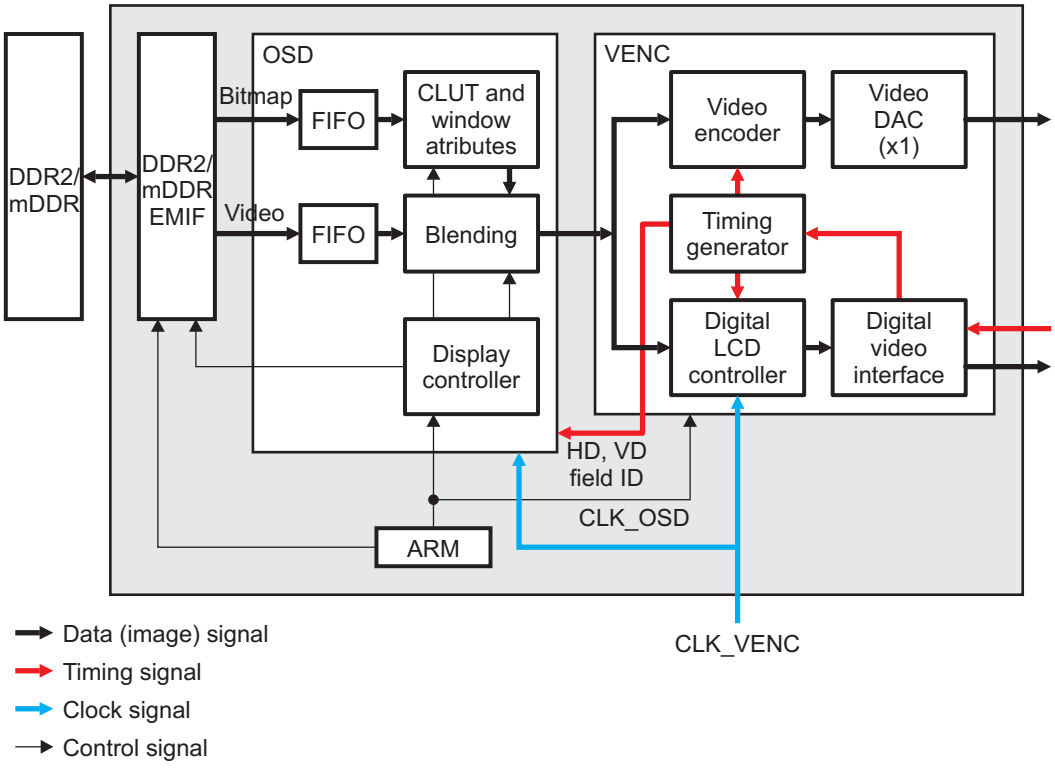


Figure 20. Video Processing Back End Block Diagram



4.2 Interfacing with Displays

The VENC/digital LCD controller supports several display/output interfaces described in the following sections. For further details on configuring the VENC for operation in the various modes, see Section 5.

4.2.1 Analog Display Interface

The analog display interface uses these DAC signals as described below.

Table 21. Analog Display Interface Signals

Name	I/O	Function
IOUT	O	Video DAC - pre video buffer DAC output • (1000 Ω to VFB)
VFB	O	VFB • (1070 Ω to TVOUT)
TVOUT	O	Video buffer output to display

4.2.2 YCC16 Digital Display Interface

The YCC16 interface includes the signals described in Table 22.

Table 22. YCC16 Digital Display Interface Signals

Name	I/O	Function
YOUT[7:0] COUT[7:0]	O	Image Data – mode set by VMOD.VDMD • Busses can be swapped via VIDCTL.YCSWAP • Cb, Cr order controlled by YCCCTL.YCP
VSYNC	I/O	VSYNC-vertical sync signal • This signal can be configured as an input or an output (VMOD.SLAVE) • When configured as an output, the OSD/VENC supplies the VD signal • When configured as an input, the Display supplies the VD signal
HSYNC	I/O	HSYNC – horizontal sync signal • This signal can be configured as an input or an output (SLAVE bit in VMOD) • When configured as an output, the OSD/VENC supplies the HD signal • When configured as an input, the Display supplies the HD signal
LCD_OE	O	LCD output enable signal • This signal indicates when the VENC/DLCD outputs valid data
VCLK	O	Video pixel clock • This signal is the pixel clock used to indicate valid display data
EXTCLK	I	VPBE pixel clock (SYSTEM.VPSS_CLK_CTRL.VPSS_MUXSEL) • This signal is the optional input pixel clock

4.2.3 YCC8 Digital Display Interface

The YCC8/REC656 interface includes the signals described in Table 23.

Table 23. YCC8 Digital Display Interface Signals

Name	I/O	Function
YOUT[7:0] or COUT[7:0]	O	Image Data – mode set by the VMOD.VDMD; REC656 mode set by YCCCTL.R656 • Busses can be selected via VIDCTL.YCSWAP • Y, Cb, Cr order controlled by the YCCCTL.YCP
VSYNC	I/O	VSYNC-vertical sync signal • This signal can be configured as an input or an output (VMOD.SLAVE) • When configured as an output, the OSD/VENC supplies the VD signal • When configured as an input, the Display supplies the VD signal
HSYNC	I/O	HSYNC – horizontal sync signal • This signal can be configured as an input or an output (VMOD.SLAVE) • When configured as an output, the OSD/VENC supplies the HD signal • When configured as an input, the Display supplies the HD signal
LCD_OE	O	LCD output enable signal • This signal indicates when the VENC/DLCD outputs valid data
VCLK	O	Video pixel clock • This signal is the pixel clock used to indicate valid display data
EXTCLK	I	VPBE pixel clock (SYSTEM.VPSS_CLKCTL.MUXSEL) • This signal is the optional input pixel clock

4.2.4 Parallel RGB Digital Display Interface

The parallel RGB interface includes the signals described in Table 24.

Table 24. Parallel RGB Digital Display Interface Signals

Name	I/O	Function
R[7:2], G[7: 2], B[7:2]	O	Image Data – mode set by the VMOD.VDMD • Default is RGB565 • Use system register PINMUX1.EXTCLK and PINMUX1.FIELD to set up RGB666 mode
VSYNC	I/O	VSYNC-vertical sync signal • This signal can be configured as an input or an output (VMOD.SLAVE) • When configured as an output, the OSD/VENC supplies the VD signal • When configured as an input, the Display supplies the VD signal
HSYNC	I/O	HSYNC – horizontal sync signal • This signal can be configured as an input or an output (VMOD.SLAVE) • When configured as an output, the OSD/VENC supplies the HD signal • When configured as an input, the Display supplies the HD signal
LCD_OE	O	LCD output enable signal • This signal indicates when the VENC/DLCD outputs valid data
VCLK	O	Video pixel clock • This signal is the pixel clock used to indicate valid display data
EXTCLK	I	VPBE pixel clock (SYSTEM.VPSS_CLK_CTRL.VPSS_MUXSEL) • This signal is the optional input pixel clock; cannot be used in RGB666 mode

4.2.5 Serial RGB Digital Display Interface

The serial RGB interface includes the signals described in Table 25.

Table 25. Serial RGB Digital Display Interface Signals

Name	I/O	Function
Data[7:0]	O	Image Data – mode set by the VDMD bit in VDMD.
VSYNC	I/O	VSYNC-vertical sync signal • This signal can be configured as an input or an output (VMOD.SLAVE) • When configured as an output, the OSD/VENC supplies the VD signal • When configured as an input, the Display supplies the VD signal
HSYNC	I/O	HSYNC – horizontal sync signal • This signal can be configured as an input or an output (VMOD.SLAVE) • When configured as an output, the OSD/VENC supplies the HD signal • When configured as an input, the Display supplies the HD signal
LCD_OE	O	LCD output enable signal • This signal indicates when the VENC/DLCD outputs valid data
VCLK	O	Video pixel clock • This signal is the pixel clock used to indicate valid display data
EXTCLK	I	VPBE pixel clock (SYSTEM.VPSS_CLK_CTRL.VPSS_MUXSEL) • This signal is the optional input pixel clock
LCD_AC	I	LCD_AC signal
BRIGHT	I	BRIGHT signal
PWM	I	PWM signal
CSYNC	I	CSYNC signal

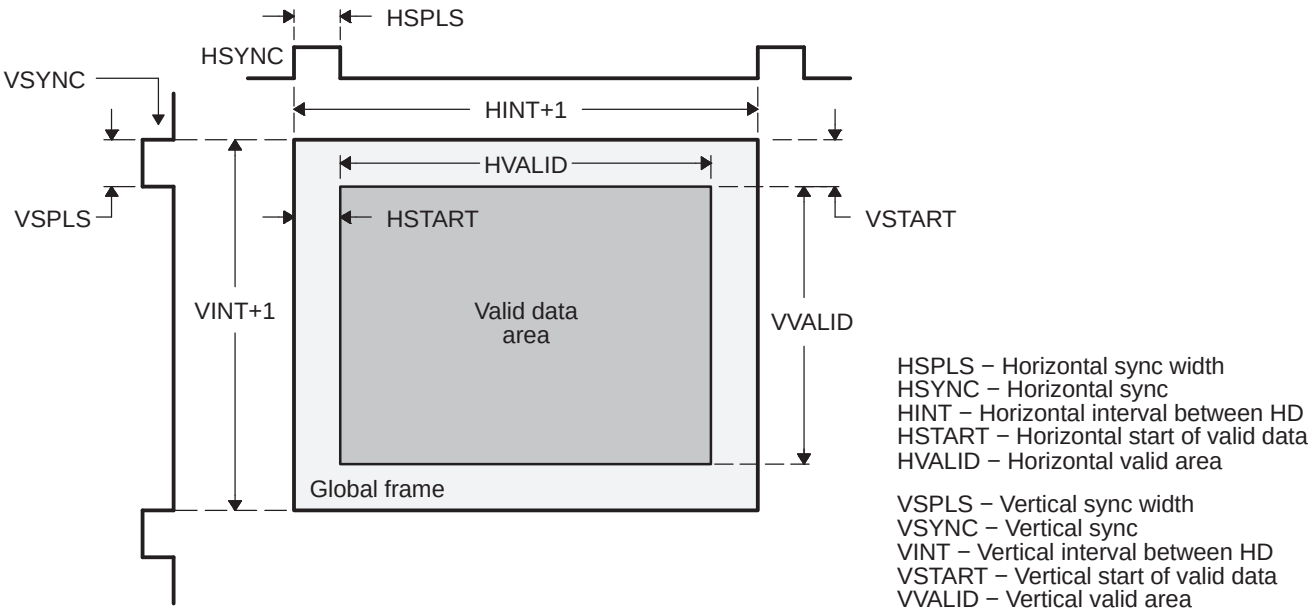
4.3 Master/Slave Mode Interface

The device can be separately configured to either source or sink the VSYNC/HSYNC signals. If master mode is set via VMOD.SLAVE=0, the VIDCTL.SYDIR=0 must be set to output the sync signals. In addition, the registers listed in Table 26 must be set to define the output frame (Figure 21).

Table 26. Master Mode Configuration Registers

Acronym	Register
HSPLS	Horizontal sync pulse width
VSPLS	Vertical sync pulse width
HINT	Horizontal interval
HSTART	Horizontal valid data start position
HVALID	Horizontal data valid range
VINT	Vertical interval
VSTART	Vertical valid data start position
VVALID	Vertical data valid range
HSDLY	Horizontal sync delay
VSDLY	Vertical sync delay

Figure 21. Video Encoder Display Frame and Control Signal Definitions



NOTE: HINT + 1 must be even when OSD clock is 1/2 VENC clock.

4.4 On-Screen Display (OSD) Module

The on-screen display (OSD) module reads data in various window formats from DDR2/mDDR and converts them into YUV display data, blends the various windows using the fixed display priority and any optional blending and transparency rules and sends the combined display image to the VENC for conditioning and output. The OSD windows (Table 27 and Figure 22) show the display priority, window type, and data types supported by each window.

Table 27. OSD Windows

Window	Priority	Type	Data Types	Control Register	Description
CURSOR	1	Rectangular outline w/transparent center	NA	RECTCUR	Controls the size and on/off control of rectangular cursor window
OSD1	2	Bitmap (or Attribute)	Bitmap, RGB565, RGB888+blend YUV422 or Attribute (blend+blink)	OSDWIN1MD	Controls the display, zoom blending, and on/off control of OSD window 1
OSD0	3	Bitmap	Bitmap, RGB565, RGB888+blend YUV422	OSDATRMD	Controls the blinking, display, zoom, on/off control of Attribute window
VID1	4	Video	YUV422	OSDWIN0MD	Controls the display, zoom blending, and on/off control of OSD window 0
VID0	5	Video	YUV422	VIDWINMD	Controls the display, zoom and on/off control of Video windows

Figure 22. OSD Window Display Priorities

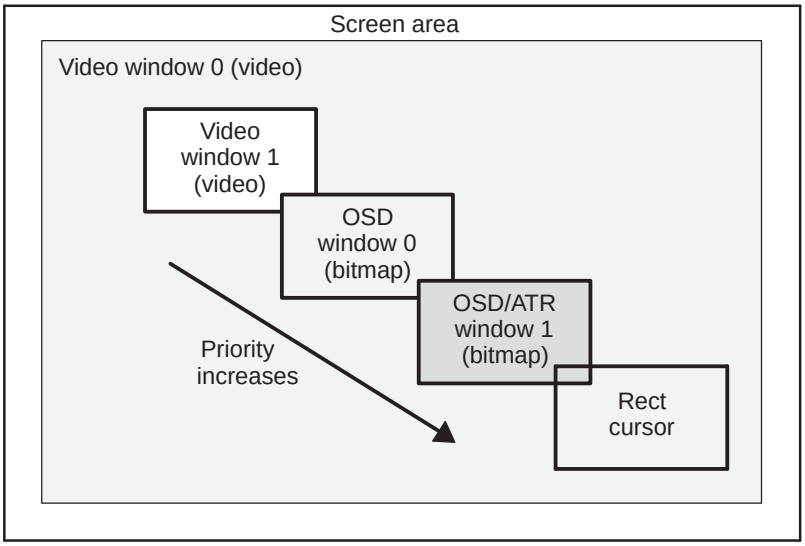


Table 28. Functional Description of the OSD Windows

Function	Video0	Video1	Bitmap0	Bitmap1	H/W Cursor
Blend with 8 steps	√ (Higher one of video windows)		√ (Higher one of bitmap windows)		x (paste only)
Independent display	√	√	√	√	√
Duplicational display	x	x	x	√	√
Color look-up table ROM and RAM	x	x	√	√	√
Blinking with programmable interval	x	x	√ (with attribute mode of bitmap window 1)		x
Pixel level blending factor	x	x	√ (with attribute mode of bitmap window 1)		x
RGB565 and RGB888 mode support	x	x	√	√	x
1/2/4/8-bit/pixel bitmap support	x	x	√	√	8-bit supported
Rescaling on horizontal x2/x4	√	√	√	√	x
Rescaling on vertical x2/x4	√	√	√	√	x
Rescaling on horizontal x1. 125/1.5	√ (Higher one of video windows)		√ (Higher one of bitmap windows)		x
Rescaling on vertical x1.2	√ (Higher one of video windows)		√ (Higher one of bitmap windows)		x

4.4.1 Video Window Constraints

The following constraints are for each window type in support of HD resolution video:

- Video window 0: Use video window 0 for HD display.
- Video window 1: Do not use video window 1 (turn off video window 1 when doing HD display).

4.4.2 OSD Configuration and Control

Many of the OSD registers contain bits that are latched by the VD signal, which is the vertical sync pulse generated by the device's Video Encoder module. Data written to a latched bit does not take affect until the VD pulse is received. This allows registers that control the OSD, such as the SDRAM data address, display window size, display zoom configuration, etc., to be changed between successive VD pulses without corrupting the current display. In the OSD register descriptions, bit fields marked with (*) are latched by the VD signal.

4.4.2.1 DDR Addresses

The location of data stored in DDR is defined by several memory-mapped registers. The DDR addresses are specified as an offset for the start of DDR in units of 32-byte burst.

Table 29. OSD SDRAM Address Registers

SDRAM Address Register	Window
VIDWIN0ADL	Video window 0 address (low 16 bits)
VIDWIN1ADL	Video window 1 address (low 16 bits)
VIDWINADH	Video window addresses (upper bits)
OSDWIN0ADL	OSD bitmap window 0 address (low 16 bits)
OSDWIN1ADL	OSD bitmap window 1/attribute window address (low 16 bits)
OSDWINADH	OSD bitmap window addresses (upper bits)

4.4.2.2 DDR Offsets

The offset registers specify the address offset between each horizontal line of display data. Since this is independent of the window display size, this allows a subset of an image to be displayed. The offset is in units of 32 bytes. Thus, the width of each line of data stored in DDR must be a multiple of 32 bytes. If the width of data is not a multiple of 32 bytes, then it must be padded when stored in DDR.

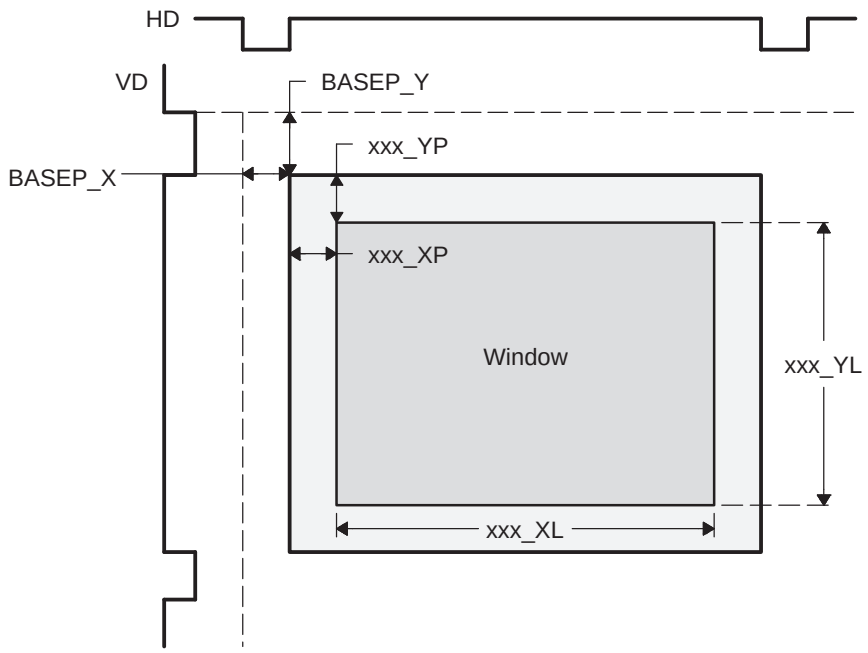
Table 30. OSD SDRAM Offset Registers

SDRAM Address Register	Window
VIDWIN0OFST	Video Window 0 SDRAM offset register
VIDWIN1OFST	Video Window 1 SDRAM offset register
OSDWIN0OFST	OSD Bitmap Window 0 SDRAM offset register
OSDWIN1OFST	OSD Bitmap Window 1/Attribute Window SDRAM offset register

4.4.2.3 Window Positioning

All windows use a common reference pixel (base pixel). The position of this pixel is determined from the beginning of the video encoder HD and the beginning of the video encoder VD signal. For each window (video, bitmap, and cursor), the location of the upper left corner is specified, along with the horizontal and vertical display sizes. The relationship of the display positions of each window is shown in Figure 23.

Figure 23. OSD Window Positioning



Window start position is specified with respect to the BASEP_X and BASEP_Y position. Window start position in X-direction and window width is specified in units of pixels. Window start position in Y-direction and window height is specified in units of lines. When the VENC is in interlaced mode, window vertical position and height (*YP and *YL registers) are defined in terms of display lines in each field. When the VENC is in progressive mode, window vertical position and height (*YP and *YL) registers are defined in terms of display lines in the progressive frame. Table 31 shows the register used for window position and size.

Table 31. OSD Window Positioning Registers

Window Positioning Registers	Window
VIDWIN0XP VIDWIN0YP VIDWIN0XL VIDWIN0YL	Video Window 0 start position and size registers
VIDWIN1XP VIDWIN1YP VIDWIN1XL VIDWIN1YL	Video Window 1 start position and size registers
OSDWIN0XP OSDWIN0YP OSDWIN0XL OSDWIN0YL	OSD Bitmap Window 0 start position and size registers
OSDWIN1XP OSDWIN1YP OSDWIN1XL OSDWIN1YL	OSD Bitmap Window 1/Attribute Window start position and size registers
CURXP CURYP CURXL CURYL	Hardware cursor start position and size registers

4.4.2.4 Window Mode – Field/Frame

Each video and bitmap window has two display modes: field mode and frame mode (VIDWINMD.VFF*n*, OSDWINnMD.OFF*n*). Table 32 shows the registers used for the window modes. The field/frame mode setting describes how the display data is organized in and read from DRAM, as shown in Table 33.

Table 32. OSD Field/Frame Mode Registers

Register.Field	Description
VIDWINMD.VFF0	Video Window 0 Field/Frame specification
VIDWINMD.VFF1	Video Window 1 Field/Frame specification
OSDWIN0MD.OFF0	OSD Bitmap Window 0 Field/Frame specification
OSDWIN1MD.OFF1	OSD Bitmap Window 1 Field/Frame specification
OSDATRMD.OFFA	OSD Attribute Window Field/Frame specification (same address/offset as for OSD Bitmap Window 1)

Table 33. Window Mode Description

Window Mode	Display Field	Initial Data	Line Increment	VENC Mode	Window Height Register	Display Usage
Frame	Top	Start Address	2 × Offset	Interlaced	Field Height (1/2 display height)	Progressive data to interlaced display device
	Bottom	Start Address + Offset	2 × Offset			
Field		Start Address	Offset	Interlaced	Field Height (1/2 display height)	Field data is line doubled
Field		Start Address	Offset	Interlaced	Field Height (full display height)	Progressive frame to progressive display

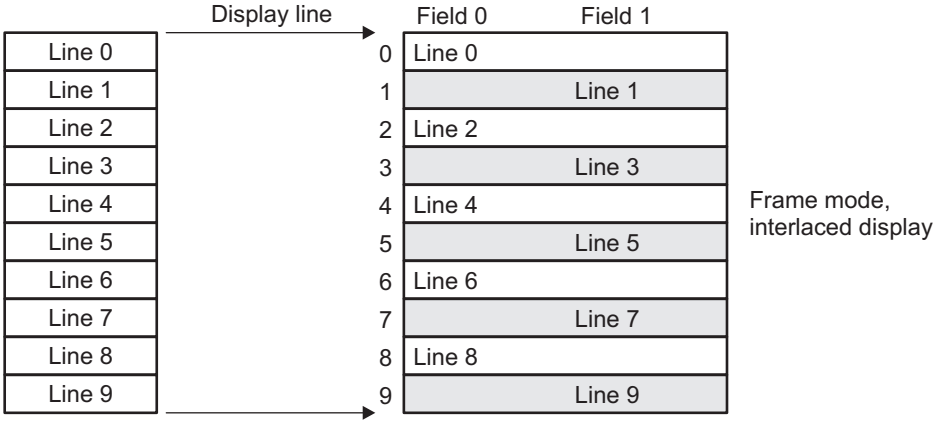
4.4.2.4.1 Frame Mode

Frame mode (Figure 24) allows a progressive frame of data (full vertical resolution) stored in DRAM and data is read sequentially, beginning from the start address and skipping every other line by incrementing by 2× the offset each line.

The readout for the second field is started at an offset of 1 line from the start address.

If the VENC is in interlaced mode (standard TV out mode), different data is read for each field and the full progressive frame is output on each even/odd field pair. In this case, the window height registers are programmed to the number of lines in each field; that is, the number of lines the VENC reads for each VSYNC (field) = 1/2 the display height.

Figure 24. OSD Window Frame Mode



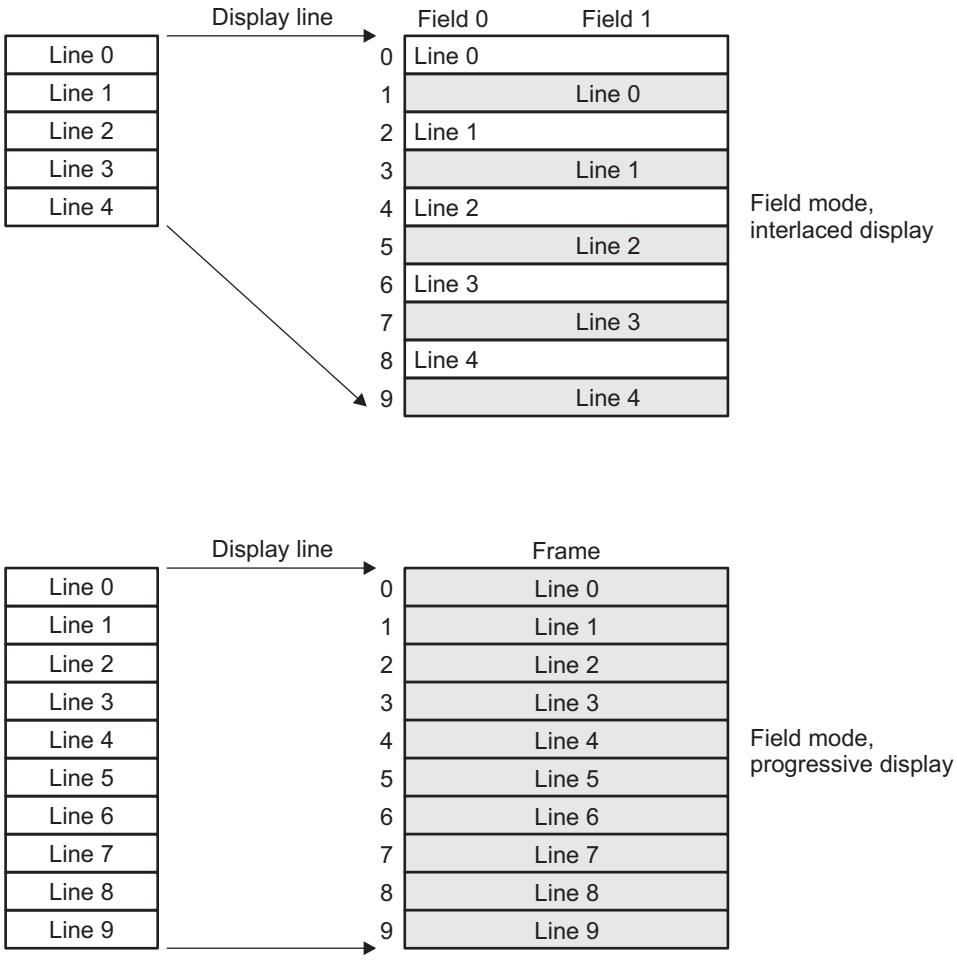
4.4.2.4.2 Field Mode

Field mode (Figure 25) assumes a single display field is stored in DRAM and data lines are read sequentially, beginning from the start address, and incrementing by the offset each line, and repeating for each field (or frame).

If the VENC is in interlaced mode (standard TV out mode), the same data is read twice for each field. This results in each line being displayed twice, once for each field (line-doubled). In this case, the window height registers are programmed to the number of lines in each field (i.e., the number of lines the VENC reads for each VSYNC (field) = 1/2 the display height). Alternately, if interlaced video frames are to be displayed, for instance from a video decode operation, the start address can be altered at each VSYNC to ping-pong between the two actual video fields and output the interlaced data to the interlaced display output.

If the VENC is in progressive mode, then field mode should be used so that all data is read from DRAM progressively so that each line is displayed once per progressive frame. In this case, window height registers are programmed to the number of lines in each progressive frame (i.e., the number of lines the VENC reads for each VSYNC (frame) = full display height).

Figure 25. OSD Window Field Mode



4.4.2.5 Window Scaling

The OSD has two rescaling methods. Window zooming is based on pure pixel/line copy for x2 and x4 rescaling. Zooming can be applied to each window independently. The other scaling method is based on linear interpolation between pixels for x9/8 and x3/2 in horizontal direction and x6/5 in vertical direction.

Horizontal x9/8 rescaling is provided for up-sampling of VGA (640) sized windows to 720 pixels for NTSC/PAL analog displays, which shrink the effective display by 8/9 when displayed on a TV. The horizontal rescaling function of x3/2 is provided for specific LCD panels displaying 960 pixels horizontal.

Vertical x6/5 rescaling is provided for up-sampling of VGA/NTSC-sized windows (480 lines) to 576 lines for usage of PAL-based TV displaying. Notice that these scaling functions are applied to a window type (i.e., both video or both bitmap windows) and the user cannot configure different rescaling ratios for each window of the same type (video and bitmap window rescaling can be configured to be different from each other). Also, a combination of rescaling and zoom methods (x9/8, x3/2 horizontal rescaling / x6/5 vertical rescaling / x2 and x4 horizontal and vertical zoom) is possible.

The combined usage of the scaling / zoom function is described by taking actual usage that can be expected with common sense. The usage matrix of scaling and zoom function is shown in Table 34. The relationship between the source picture size and displayed picture size has some limitations as mentioned here.

Table 34. Functional Matrix of Scaling and Zoom

Output Source	960(h) x 480(v)	960(h) x 576(v)	720(h) x 480(v)	720(h) x 576(v)
VGA (640(h) x 480(v))	√ (x1.5(h))	√ (x1.5(h)x1.2(v))	√ (x1.125(h))	√ (x1.125(h)x1.2(v))
NTSC D1(720(h) x 480(v))	x	x	√	√ (x1.2(v)
PAL D1(720(h) x 480(v))	x	x	x	√
3/4 VGA (480(h) x 480(v))	√ (x2(h))	√ (x2(h)x1.2(v))	√ (x1.5(h))	√ (x1.5(h)x1.2(v))
1/2 VGA (320(h) x 480(v))	√ (x2(h)x1.5(h))	√ (x2(h)x1.5(h)x1.2(v))	√ (x2(h)x1.125(h))	√ (x2(h)x1.125(h)x1.2(v))
1/4 VGA (320(h) x 240(v))	√ (x2(h)x1.5(h)x2(v)x2(v))	√ (x2(h)x1.5(h)x2(v)x1.2(v))	√ (x2(h)x1.125(h)x2(v))	√ (x2(h)x1.125(h)x2(v)x1.2(v))
1/2 QVGA (160(h) x 240(v))	√ (x4(h)x1.5(h)x2(v))	√ (x4(h)x1.5(h)x2(v)x1.2(v))	√ (x4(h)x1.125(h)x2(v))	√ (x4(h)x1.125(h)x2(v)x1.2(v))
1/4 QVGA (160(h) x 120(v))	√ (x4(h)x1.5(h)x4(v))	√ (x4(h)x1.5(h)x4(v)x1.2(v))	√ (x4(h)x1.125(h)x4(v))	√ (x4(h)x1.125(h)x4(v)x1.2(v))
3/4 D1 (544(h) x 480(v))	x	x	x	x
1/2 D1 (352(h) x 480(v))	x	x	x	x
1/4 D1 (352(h) x 240(v))	x	x	x	x

4.4.2.5.1 Window Zooming

The video windows and OSD bitmap windows can be zoomed along their horizontal and vertical directions by a factor of 2 or 4. Figure 26 shows the zoom process and the parameters that must be set up to execute a zoom. All of the registers used in the zoom process (Table 35) are latched by the VD signal so they can be safely updated any time.

- Set the starting DDR address of the area desired to be magnified, offset, zoom factor and the display window size. The OSD will take data, starting from the start address, to generate a magnified image that fits into the display window.
- Set the display position to the desired position of the window. Set the display height and display width to the desired magnified height and width.
- When zoom is enabled (VIDWINMD.VVZ*n*, VIDWINMD.VHZ*n*, OSDWIN*n*MD.OVZ*n*, OSDWIN*n*MD.OHZ*n*), data starting from the DDR start position will be magnified to fit into the display area specified by the display height and display width. For example, if the horizontal and vertical directions are set to 2× zoom and the display width and height are set to 640 × 480, then a 320 × 240 block of data starting from the DDR start position will be magnified to 640 × 480 in the display window.

Figure 26. OSD Window Zoom Process

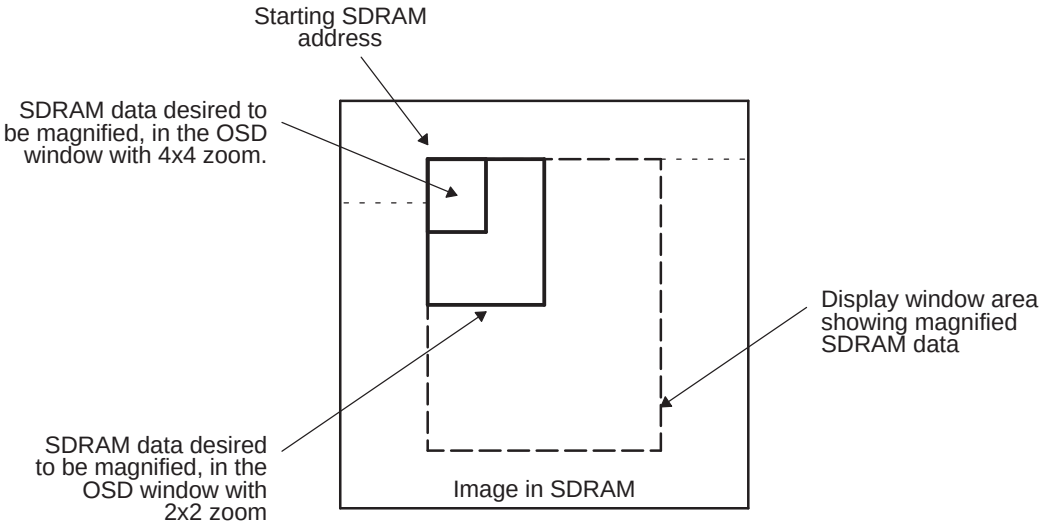


Table 35. OSD Window Zoom Registers

Register.Field	Description
VIDWINMD.VHZ0	Video Window 0 Horizontal Zoom
VIDWINMD.VVZ0	Video Window 0 Vertical Zoom
VIDWINMD.VHZ1	Video Window 1 Horizontal Zoom
VIDWINMD.VVZ1	Video Window 1 Vertical Zoom
OSDWIN0MD.OHZ0	Bitmap Window 0 Horizontal Zoom
OSDWIN0MD.OVZ0	Bitmap Window 0 Vertical Zoom
OSDWIN1MD.OHZ1	Bitmap Window 1 Horizontal Zoom
OSDWIN1MD.OVZ1	Bitmap Window 1 Vertical Zoom

4.4.2.5.2 Window Scaling – Square Pixels for NTSC/PAL Analog Output or Display Matching

The analog NTSC/PAL output video signals are spatially compressed. As a result, the OSD has an option to horizontally and vertically expand the video and bitmaps windows to counteract the spatial compression in the video signal. In addition, there are options to smooth the expanded video window data. Table 36 shows the registers used for window expansion.

- NTSC analog output is compressed 8/9 horizontally
  - 720 × 480 input appears as 640 × 480 (6:4 aspect ratio source data appears as 4:3)
  - Solution (example)-Use 640 × 480 source material with 9/8 horizontal expansion (MODE.VHRSZ and MODE.OHRSZ) and window display size set to 720 × 480, which will appear as 640 × 480.
  - If EXTMODE.EXPMDSEL = 1, then use EXTMODE.SCRNHEXP (applies to all windows).
- PAL analog output is compressed 8/9 horizontally and 5/6 vertically
  - 720 × 576 input appears as 640 × 480
  - Solution (example)-Use 640 × 480 source material with 9/8 horizontal expansion (MODE.VHRSZ and/or MODE.OHRSZ) and 6/5 vertical expansion (MODE.VVRSZ and/or MODE.OVRSZ) and window display size set to 720 × 576, which will appear as 640 × 480.
  - If EXTMODE.EXPMDSEL = 1, then use EXTMODE.SCRNVEXP (applies to all windows).
- Display scaling to 960 wide LCD
  - Must set: MODE.VHRSZ and/or MODE.OHRSZ to 0
  - Must set: EXTMODE.EXPMDSEL = 0
  - Then enable with EXTMODE.VIDHRSZ and EXTMODE.OSDHRSZ

Table 36. Normal OSD Window Expansion Registers

Register.Field	Description
MODE.VHRSZ	Video Window Horizontal 9/8 Expansion
MODE.VVRSZ	Video Window Vertical 6/5 Expansion
MODE.V0EFC	Video Window 0 smoothing filter enable (with MODE.EF)
MODE.V1EFC	Video Window 1 smoothing filter enable (with MODE.EF)
MODE.EF	Video Window smoothing filter (maximum line width is 720)
MODE.OHRSZ	Video Window Horizontal 9/8 Expansion
MODE.OVRSZ	Video Window Vertical 6/5 Expansion

Table 37. Extended OSD Window Expansion Registers

Register.Field	Description
EXTMODE.EXPMDSEL	Sets filtering mode before expansion
EXTMODE.SCRNHEXP	Global H expansion on all windows
EXTMODE.SCRNVEXP	Global V expansion for all windows
EXTMODE.OSDHRSZ15	Bitmap window 1.5x expansion if normal filtering done
EXTMODE.VIDHRAZ15	Video window 1.5x expansion if normal filtering done

4.4.2.5.3 Zoom and Expansion Filter Usage

Table 38 shows the usage of the zoom and expansion filters. Note that the vertical expansion filter has a higher priority than the vertical zoom filter. If you configure both the zoom and expansion filters to be active, the OSD module can perform only the expansion filter for the vertical direction due to limitations in the design.

Additionally, if you configure EXTMODE.EXTMDSEL = 1 (post=blend mode), you can perform only the expansion filter (no zoom filter). This fact means that only screen-level filtering is valid in post-blend mode. Window-level filtering is impossible in post-blend mode.

Table 38. Zoom and Expansion Filter Usage

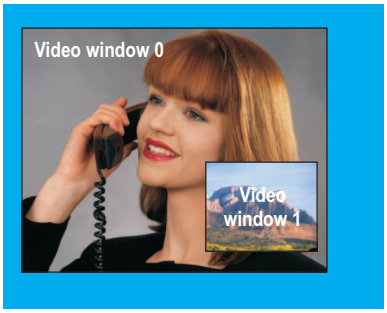
Performance Expand Filter (MODE.EF)	Description of Detailed Performance			
ON (MODE.EF = 1)	All interpolation filters perform in both horizontal and vertical direction. (Also both of zoom (x2/x4) and expansion (x9/8h, x3/2h, x6/5v). Additionally; H(On, On) and V(On, On)) In combined performance of vertical zoom and vertical expansion, filter is active for expansion only.			
OFF (MODE.EF = 0)	Filter SW (H) (EXTMODE.EXPFILVEN)	ON	zoom_SW(h) ON EXTMODE.ZMFILV1HEN EXTMODE.ZMFILV0HEN	Interpolation filter is active in zoom function. Also, expansion filter is active (source is result of zoom function).
			zoom_SW(h) OFF EXTMODE.ZMFILV1HEN EXTMODE.ZMFILV0HEN	No interpolation (only pixel copy) is executed in zoom function. Expansion filter is active (source is result of zoom function).
		OFF	zoom_SW(h) ON EXTMODE.ZMFILV1HEN EXTMODE.ZMFILV0HEN	Interpolation filter is active in zoom function. Expansion filter is inactive; just pixel copy is executed (source is result of zoom function).
			zoom_SW(h) OFF EXTMODE.ZMFILV1HEN EXTMODE.ZMFILV0HEN	No interpolation (only pixel copy) is executed in zoom function. Expansion filter is inactive, just pixel copy is executed (source is result of zoom function).
	FILTER SW (V) (EXTMODE.EXPFILHEN)	ON	zoom_SW(v) ON EXTMODE.ZMFILV1VEN EXTMODE.ZMFILV0VEN	No interpolation (only pixel copy) is executed in zoom function. Expansion filter is active (source is result of zoom function).
			zoom_SW(v) OFF EXTMODE.ZMFILV1VEN EXTMODE.ZMFILV0VEN	
		OFF	zoom_SW(V) ON EXTMODE.ZMFILV1VEN EXTMODE.ZMFILV0VEN	Interpolation filter is active in zoom function. Expansion filter is inactive, just pixel copy is executed. (source is result of zoom function)
			zoom_SW(v) OFF EXTMODE.ZMFILV1VEN EXTMODE.ZMFILV0VEN	No interpolation filter (only pixel copy) is executed in zoom function. Expansion filter is inactive, just pixel copy is executed. (source is result of zoom function).

4.4.2.5.4 Window Positioning Limits for When Using Horizontal Expansion

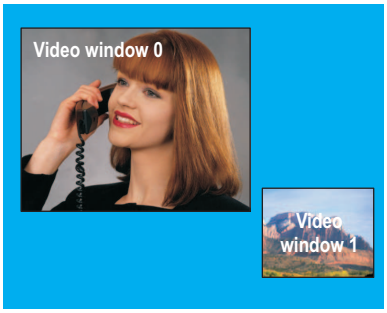
When using horizontal expansion (x9/8 or x3/2), there are some limitations on window positioning and layout. Section 4.4.2.5.5 describes the limitation on the location and layout of each window when horizontal expansion is used. These limitations apply only between windows of the same type (Video Window 0 and Video Window 1, or Bitmap Window 0 and Bitmap Window 1).

Windows of the same type can be located independently if there is no overlap / duplication or if Window 1 is fully contained within Window 0. Window 1 can overlap on the right side of Window 0. However, Window 1 cannot overlap the left side of Window 0. This limitation is only present when horizontal expansion (x9/8 and x3/2) is used.

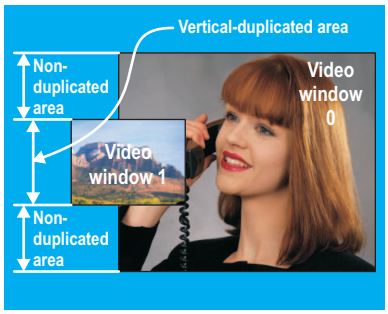
[Case 1] OK
(horizontal duplication on right only)



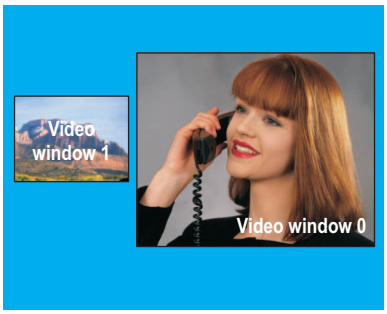
[Case 2] OK



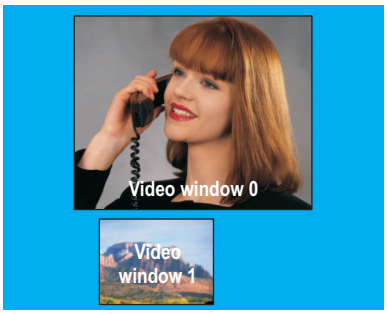
[Case 3] OK
(no horizontal duplication)



[Case 4] Prohibited
(horizontal duplication from left)



[Case 5] OK
(no horizontal duplication)



[Case 6] OK
(no vertical duplication)

4.4.2.5.6 Vertical Boundary Processing

When using vertical expansion (x6/5) with filtering, filtering is not applied at the lower boundary line of Window 1 in cases 1, 2, and 4 in Table 39. This is because the expansion method used in each window is different (start line is different) and the line is repetitively read from different positions and, as a result, the lower boundary between the windows will appear improper. In this case, the user can prevent or control filtering on the edge of the window.

Table 39. Vertical Boundary Filtering Control Registers

Register Field	Description
VBNDRY. VBNDRYPRCSEN	Enables video boundary processing
VBNDRY. VFILINCMD	Turn ON to have vertical filtering increment past the end of the vertical display area. In this case, additional data to be processed for vertical filtering should be stored in SDRAM, immediately following the display data. Turn OFF to have vertical filtering stop incrementing when it reaches the last display line. This is the DM320 equivalent mode.

4.4.2.6 OSD Background Color

The background color can be specified in terms of the color lookup tables. This color is displayed in regions of the combined OSD display area that do not have an overlapping window. Table 40 shows the registers used for OSD background color.

Table 40. OSD Background Color Registers

Register.Field	Description
MODE.BCLUT	Selects the color lookup table to be used (ROM or RAM). Note that there are two ROM tables and the selection for the other windows also applies here (MISCCTL.RSEL).

Table 40. OSD Background Color Registers (continued)

Register.Field	Description
MODE.CABG	Background color. 8-bit offset into color lookup table.

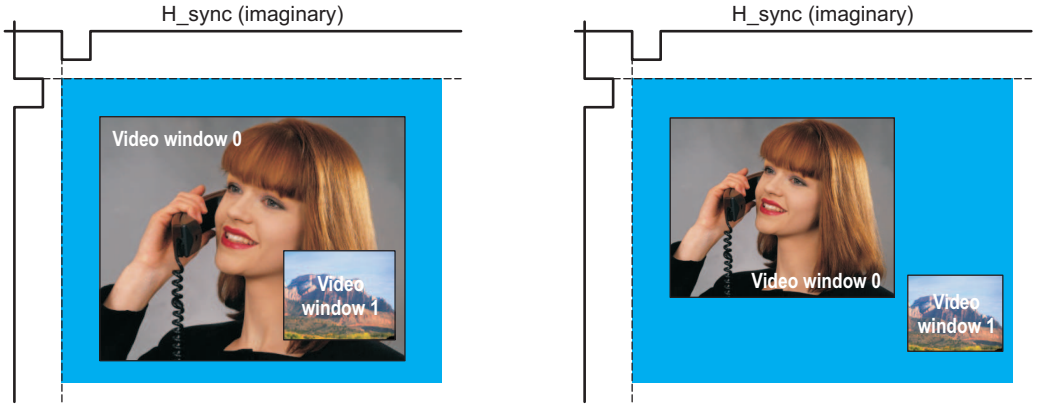
4.4.3 Video Windows

The device supports two video windows (VIDWIN0 and VIDWIN1) that can be displayed simultaneously. Data referenced by each Video window is read from external memory and displayed within the two windows.

Note that both picture-in-picture (PIP) and independent displays are supported.

Note also that blending on video window 1 (VIDWIN1) and video window 0 (VIDWIN0) is not supported.

Figure 27. Video Window Display Options



The only data format accepted by the video windows is YUV 4:2:2 interleaved data as described below. This is the data format output by the VPFE IPIPE and Resizer modules.

OSD window data is always packed into 32-bit words and left-justified. Starting from the upper left corner of the OSD window, all data will be packed into adjacent 32-bit words. Figure 28 shows data format window data in SDRAM.

Figure 28. Pixel Arrangement in the Display

Left, Top

P0	P1	P2	P3	P4	P5	P6	P7 ...

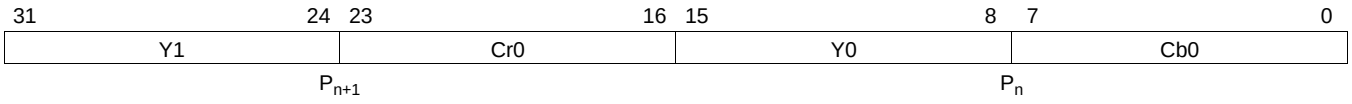
4.4.3.1 Video Window Data – YUV422 Format

OSD video window data is in YCbCr 4:2:2 format. Other formats, for example, 4:2:0 and 4:4:4 interleaved data formats are not supported. Note that the order of the Cb and Cr data is dependent on MODE.CS (chroma swap). Figure 29 describes the default case of Cb/Cr order.

Since each horizontal line of window data must be a multiple of 32 bytes, video window data must contain a multiple of 32 bytes/2 bytes/pixel = 16 pixels per horizontal line.

Figure 29. Video Data Format – YUV422

(a) 16-bits per pixel, 32-bit pixel pair with combined Chroma



(b) SDRAM format

Address	31	16	15	0
N	P1		P0	
N + 1	P3		P2	
N + 2	P5		P4	
...	...		...	

4.4.3.2 Expansion and Anti-Flicker Filter for Video Window

The OSD module has a two-tap linear filter for the video window. This is useful when using horizontal and vertical expansion for reduction of flicker noise due to display rate conversion such as 60i display from 30 Hz frame data that are field-based. This section also describes configuration options of this filtering function.

Table 41. Expansion and Anti-Flicker Filter for Video Window

Register.Field	Description
MODE.EF	Expansion filter enable. Only use when EXTMODE.EXPMDSEL = 0
WIDWINMD.VFINV	Inverts application of the two sets of expansion filter coefficients between field 0 and field 1.
WIDWINMD.VnEFC	Enables different anti-flicker coefficients for each field
EXTMODE.EXPMDSEL	Extended mode expansion filtering mode select
EXTMODE.ZMFILVnVEN	Extended mode - video window n vertical zoom filter type (x6/5)
EXTMODE.ZMFILVnHEN	Extended mode - video window n horizontal zoom filter type
EXTMODE.EXPFILHEN	Extended mode - video window horizontal expansion filter enable (x9/8, x1/5)
EXTMODE.EXPFILVEN	Extended mode - video window vertical expansion filter enable (x6/5)

4.4.3.2.1 Video Window Filtering - Horizontal Direction

In the horizontal direction, this filter operates only if x2/x4 zoom-up function or x1.5/x9/8 rescaling functions are enabled. Configuration and processing details are described in this section.

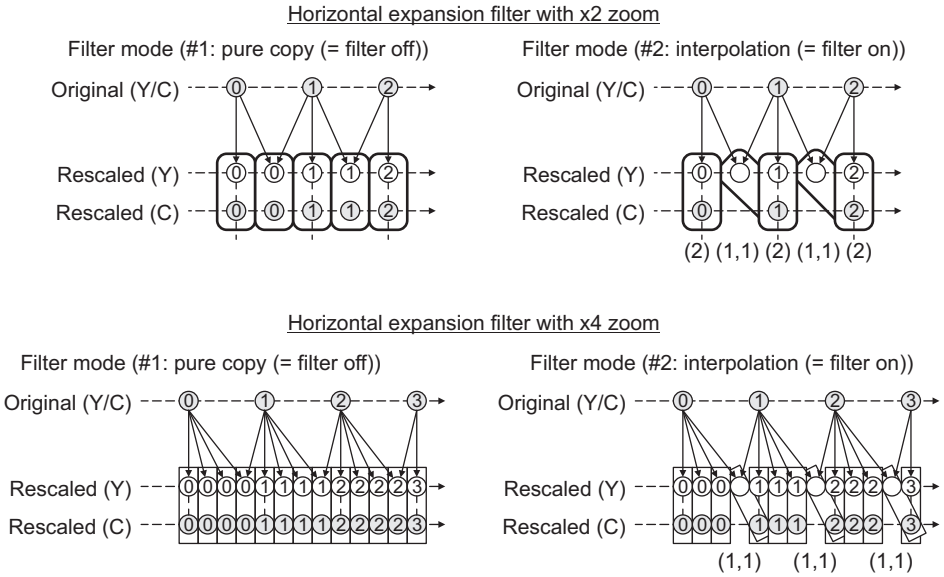
4.4.3.2.1.1 Horizontal x2/x4 Zoom-Up Filter

In this case, the filtering function is only interpolating a pixel value for the new pixel at the boundary of the resized pixels. All other pixels are duplicated.

Table 42. Filtering Configuration for Horizontal x2/x4 Zoom

Filter Mode #1		Filter Mode #2	
Normal			
Register. Field	**Value**	**Register. Field**	**Value**
MODE.EF	0	MODE.EF	1
Extended			
Register. Field	**Value**	**Register. Field**	**Value**
MODE.EF	0	MODE.EF	0
EXTMODE.ZMFILVnHEN	0	EXTMODE.ZMFILVnHEN	1

Figure 30. Filtering Method for Horizontal x2/x4 Zoom



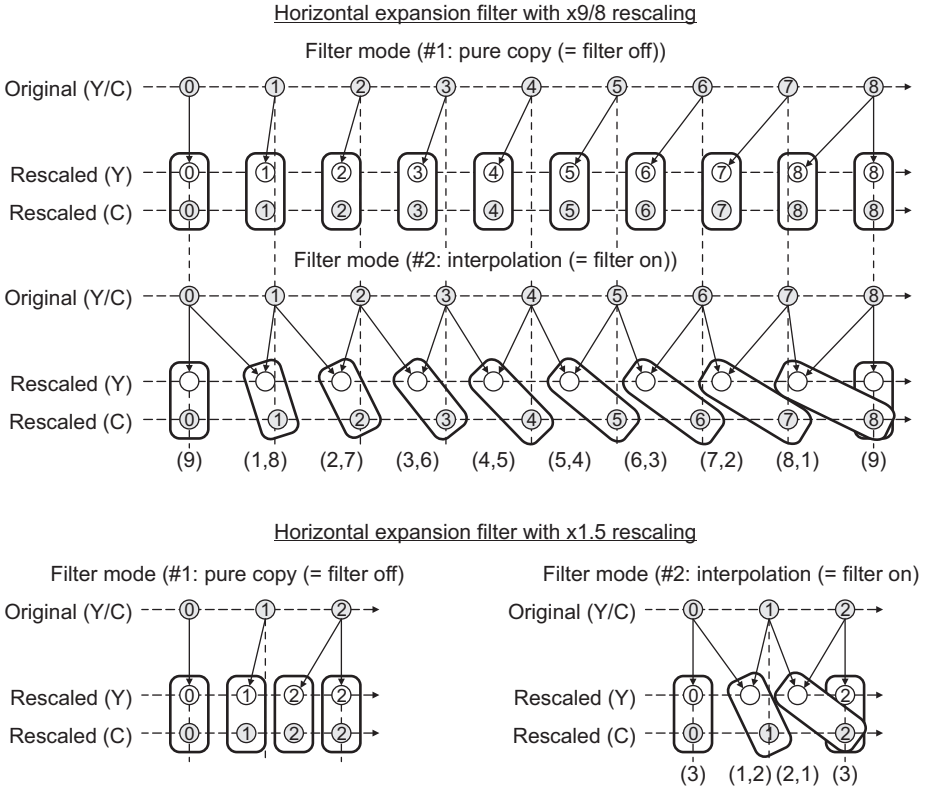
4.4.3.2.1.2 Horizontal x1.5 (3/2)/x1.125 (9/8) Rescaling Filter

In this case, the filtering function is a linear interpolation.

Table 43. Filtering Configuration for Horizontal x1.5/x1.125 Expansion

Filter Mode #1		Filter Mode #2	
Normal			
Register. Field	**Value**	**Register. Field**	**Value**
MODE.EF	0	MODE.EF	1
Extended			
Register. Field	**Value**	**Register. Field**	**Value**
MODE.EF	0	MODE.EF	0
EXTMODE.ZMFILVnHEN	0	EXTMODE.ZMFILVnHEN	1

Figure 31. Filtering Method for Horizontal x1.5/x1.125 Zoom



4.4.3.2.2 Video Window Filtering - Vertical Direction

In the vertical direction, this filter operates only when x1/x2/x4 zoom or x1.5(x6/5) scaling is active (x1 zoom-up is only for field rate conversion).

4.4.3.2.2.1 Vertical x1 Anti-Flicker (Expansion) Filter (Field Rate Conversion)

This case applies when a field-based image is displayed as 60i image (i.e., data for each 60i field is the same). In this case, the filtering function is effective to reduce flicker noise.

Table 44. Table 37. Vertical x1 Anti-Flicker Filter Control Registers

Register Field	Value			
WIDWINMD.FSINV or WIDWINMD.VFINV	1			
WIDWINMD.VnEFC	0 or 1			

Figure 32. Filtering Method for Vertical x1 Expansion (Same Data Each Field)

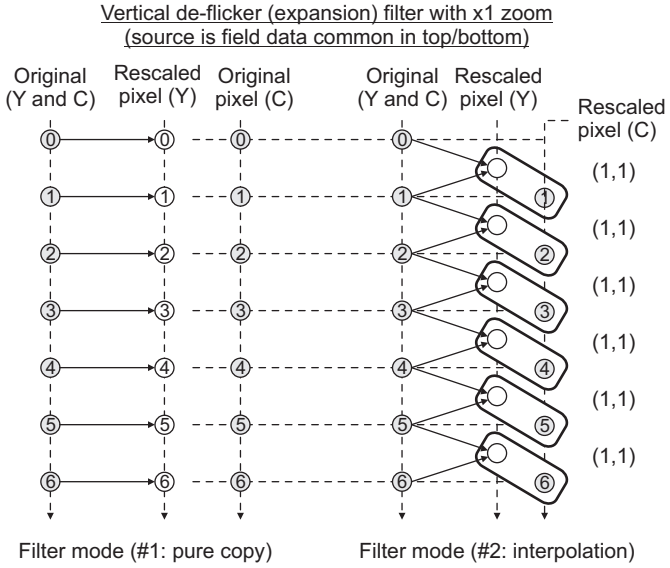


Table 45. Operation of Vertical x1 Anti-Flicker Filter Control Registers

Invert bit (VIDWINMD.VFINF or MODE.FSINV) Expand Filter (V)	0		1	
Coefficient bit (VIDWINMD.VnEFC)	Different (due to same field source)			
ON	FID = 0	1	FID = 0	2
	FID = 1	2	FID = 1	1
OFF	FID = 0	1	FID = 0	1
	FID = 1	1	FID = 1	1

4.4.3.2.2.2 Vertical x1 Anti-Flicker (Expansion) Filter (Without Field Rate Conversion)

This case applies when source image top and bottom are stored in SDRAM and displayed as a 60i image (i.e., data for each 60i field is unique). In this case, the filtering function is not applied.

Table 46. Operation of Vertical x1 Anti-Flicker Filter Control Registers

Invert bit (VIDWINMD.VFINF or MODE.FSINV) Expand Filter (V)	0		1	
Coefficient Bit (VIDWINMD.VnEFC)	Same (due to different field source)			
ON	FID = 0	1	FID = 0	1
	FID = 1	1	FID = 1	1
OFF	FID = 0	1	FID = 0	1
	FID = 1	1	FID = 1	1

4.4.3.2.2.3 Vertical x1 Anti-Flicker (Expansion) Filter (Frame Source Data Case)

This case applies when any frame-based image is displayed. In this case, the filtering function is not applied

Figure 33. Filtering Method for Vertical x1 Expansion (Frame Data)

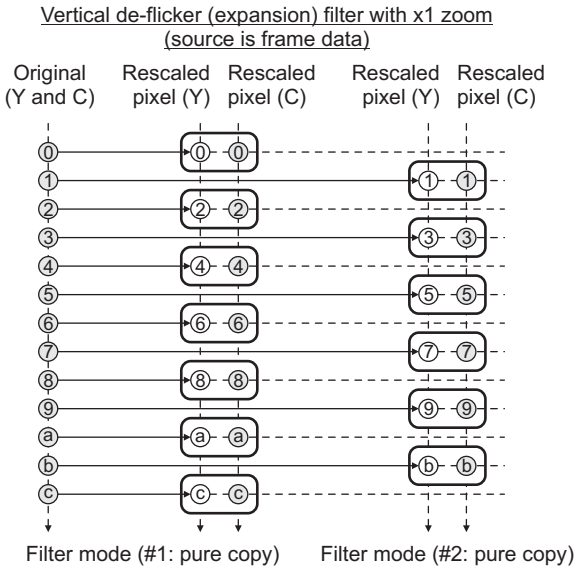


Table 47. Operation of Vertical x1 Anti-Flicker Filter for Frame Mode

Invert bit (VIDWINMD.VFINF or MODE.FSINV) Expand Filter (V)	0		1	
Coefficient bit (VIDWINMD.VnEFC)	Different (due to same field source)			
ON	FID = 0	1	FID = 0	2
	FID = 1	2	FID = 1	1
OFF	FID = 0	1	FID = 0	2
	FID = 1	2	FID = 1	1

4.4.3.2.2.4 Vertical x2 Zoom-Up Filter (Including Field Rate Conversion)

This case applies when a field-based image is displayed as 60i image (i.e., data for each 60i field is the same) with x2 vertical zoom. In this case, the filtering function is effective to reduce flicker noise.

Figure 34. Filtering Method for Vertical x2 Expansion (Same Data Each Field)

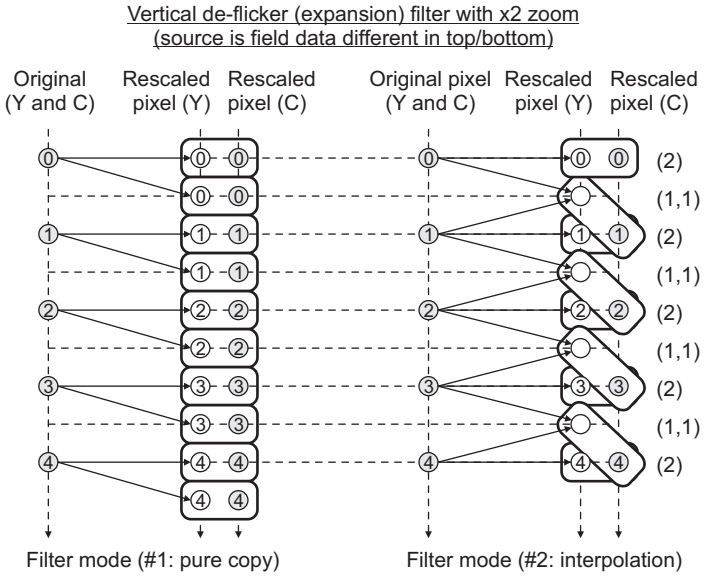


Table 48. Operation of Vertical x2 Anti-Flicker Filter for Field Mode

Invert bit (VIDWINMD.VFINF or MODE.FSINV) Expand Filter (V)	0		1	
Coefficient Bit (VIDWINMD.VnEFC)	Different (due to same field source)			
ON	FID = 0	1	FID = 0	2
	FID = 1	2	FID = 1	1
OFF	FID = 0	1	FID = 0	1
	FID = 1	1	FID = 1	1

4.4.3.2.2.5 Vertical x2 Zoom-Up Filter (Without Field Rate Conversion)

This case applies when source image top and bottom are stored in SDRAM and displayed as a 60i image (i.e., data for each 60i field is unique) and x2 zoom is applied. In this case, the filtering function is not applied.

Figure 35. Filtering Method for Vertical x2 Expansion (No Field Rate Conversion)

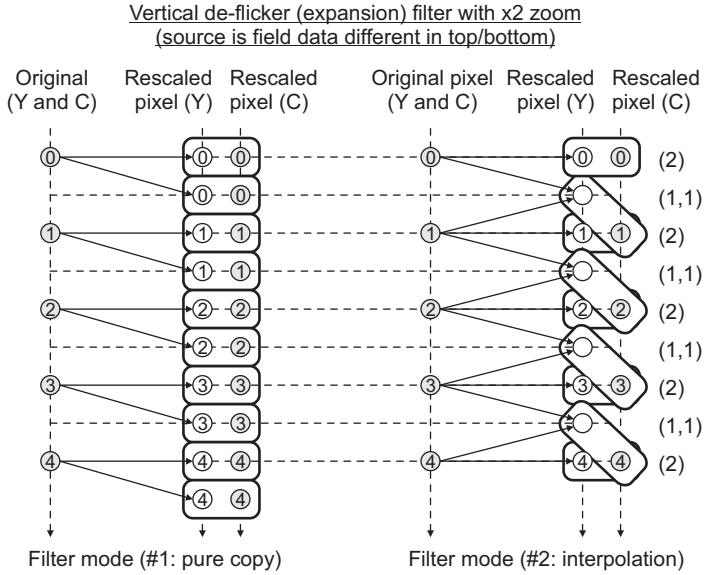


Table 49. Operation of Vertical x2 Anti-Flicker Filter (No Field Rate Conversion)

Invert bit (VIDWINMD.VFINF or MODE.FSINV) Expand Filter (V)	0		1	
Coefficient bit (VIDWINMD.VnEFC)	Same (due to different field source)			
ON	FID = 0	2	FID = 0	2
	FID = 1	2	FID = 1	2
OFF	FID = 0	1	FID = 0	1
	FID = 1	1	FID = 1	1

4.4.3.2.2.6 Vertical x2 Zoom-Up Filter (Frame Source Data Case)

This case applies when any frame-based image is displayed with x2 zoom. In this case, the filtering function is not applied. The interpolated value for filter mode #2 is derived from the average value between two pixels that surround the interpolated pixel data.

Figure 36. Filtering Method for Vertical x2 Expansion (Frame Data)

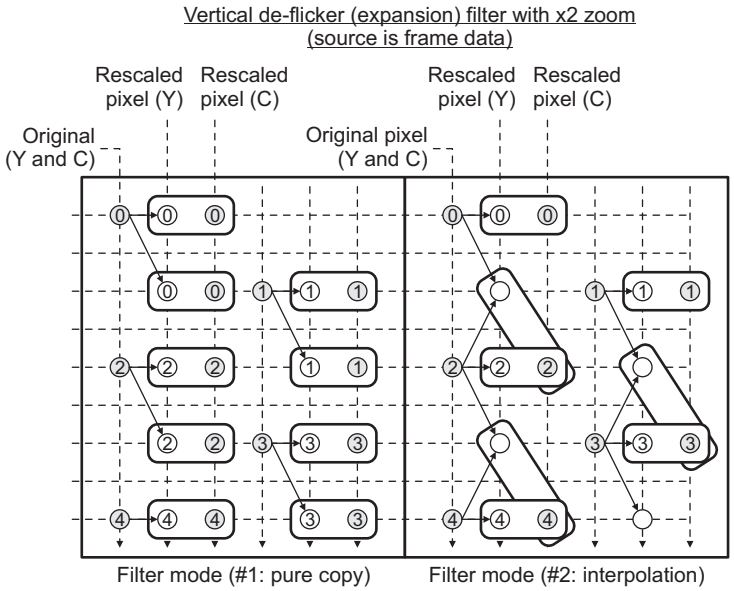


Table 50. Operation of Vertical x2 Anti-Flicker Filter for Frame Mode

Invert bit (VIDWINMD.VFINF or MODE.FSINV) Expand Filter (V)	0		1	
Coefficient bit (VIDWINMD.VnEFC)	Same (due to frame source)			
ON	FID = 0	1	FID = 0	2
	FID = 1	2	FID = 1	1
OFF	FID = 0	1	FID = 0	1
	FID = 1	1	FID = 1	1

4.4.3.2.2.7 Vertical x4 Zoom-Up Filter (Including Field Rate Conversion)

This case applies when a field based image is displayed as 60i image (i.e., data for each 60i field is the same) with x4 vertical zoom. In this case, the filtering function is effective to reduce flicker noise. Filter processing and configuration is described in this section.

Figure 37. Filtering Method for Vertical x4 Expansion (Same Data Each Field)

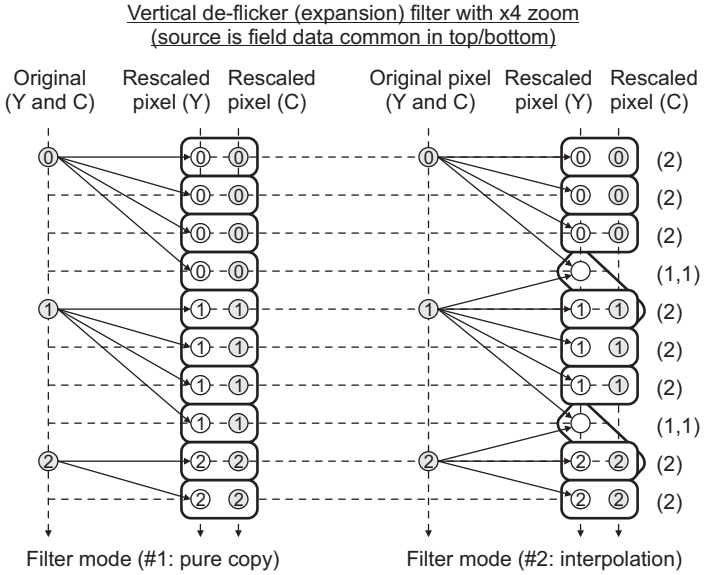


Table 51. Operation of Vertical x4 Anti-Flicker Filter for Field Mode

Invert bit (VIDWINMD.VFINF or MODE.FSINV) Expand Filter (V)	0		1	
Coefficient bit (VIDWINMD.VnEFC)	Different (due to same field source)			
ON	FID = 0	1	FID = 0	2
	FID = 1	2	FID = 1	1
OFF	FID = 0	1	FID = 0	1
	FID = 1	1	FID = 1	1

4.4.3.2.2.8 Vertical x4 Zoom-Up Filter (Without Field Rate Conversion)

This case applies when source image top and bottom are stored in SDRAM and displayed as a 60i image (i.e., data for each 60i field is unique) and x4 zoom is applied. In this case, the filtering function is not applied.

Figure 38. Filtering Method for Vertical x4 Expansion (No Field Rate Conversion)

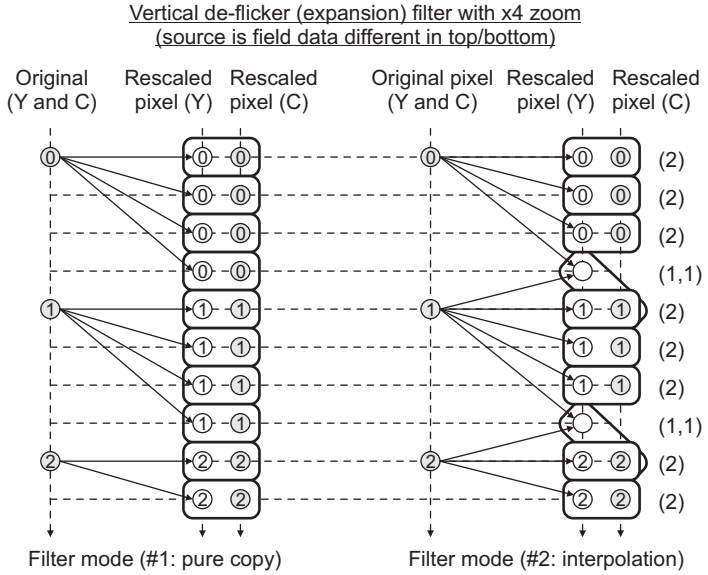


Table 52. Operation of Vertical x4 Anti-Flicker Filter (No Field Rate Conversion)

Invert bit (VIDWINMD.VFINF or MODE.FSINV) Expand Filter (V)	0		1	
Coefficient bit (VIDWINMD.VnEFC)	Same (due to different field source)			
ON	FID = 0	2	FID = 0	2
	FID = 1	2	FID = 1	2
OFF	FID = 0	1	FID = 0	1
	FID = 1	1	FID = 1	1

4.4.3.2.2.9 Vertical x4 Zoom-Up Filter (Frame Source Data Case)

This case applies when any frame based image is displayed with x4 zoom. In this case, the filtering function is not applied. The interpolated value for filter mode #2 is derived from the average value between two pixels that surround the interpolated pixel data.

Figure 39. Filtering Method for Vertical x4 Expansion (Frame Data)

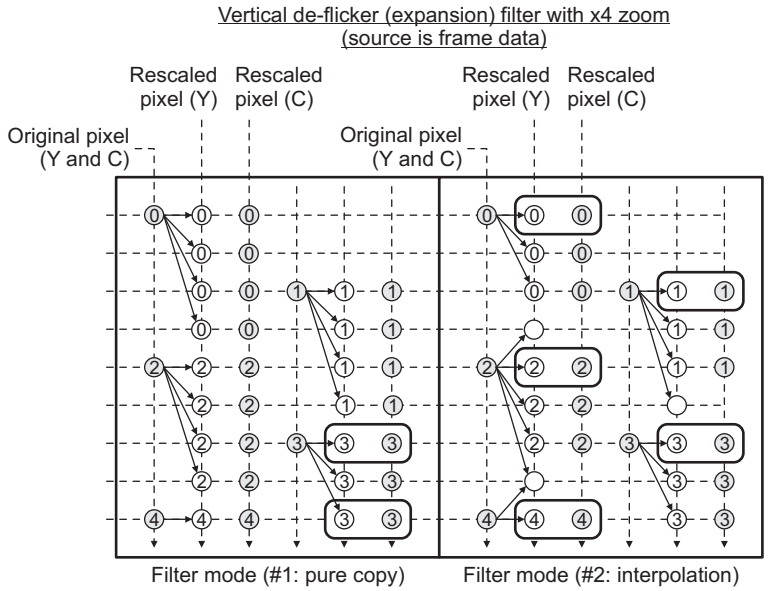


Table 53. Vertical x4 Anti-Flicker Filter for Frame Mode

Invert bit (VIDWINMD.VFINF or MODE.FSINV) Expand Filter (V)	0		1	
Coefficient bit (VIDWINMD.VnEFC)	Same (due to frame source)			
ON	FID = 0	2	FID = 0	2
	FID = 1	2	FID = 1	2
OFF	FID = 0	1	FID = 0	1
	FID = 1	1	FID = 1	1

4.4.3.2.2.10 Vertical x6/5 Anti-Flicker (Expansion) Filter

If the user configures vertical x1.2 expansion, this case is available. The user can select filter type with the configuration of the register based on the type of source data stored in SDRAM. The recommended type for each stored type of source data is:

- If source data is a field-based image and the source image of each field is the same, select only “different coefficient mode” so that the filter coefficients of top field processing are different from those used for bottom field processing.
- If source data is a field-based image and the source image of each field is stored in SDRAM, user can select either “same coefficient mode” or “different coefficient mode.” Because source data for top field is different from bottom field, the same filter coefficient can provide sufficient quality.
- If source data is a frame-based image, user can select either “same coefficient mode” and “different coefficient mode”. Because source data for top field is different from bottom field, the same filter coefficient can provide sufficient quality.

Figure 40. Filtering Method for Vertical x1.2 Expansion with No Zoom

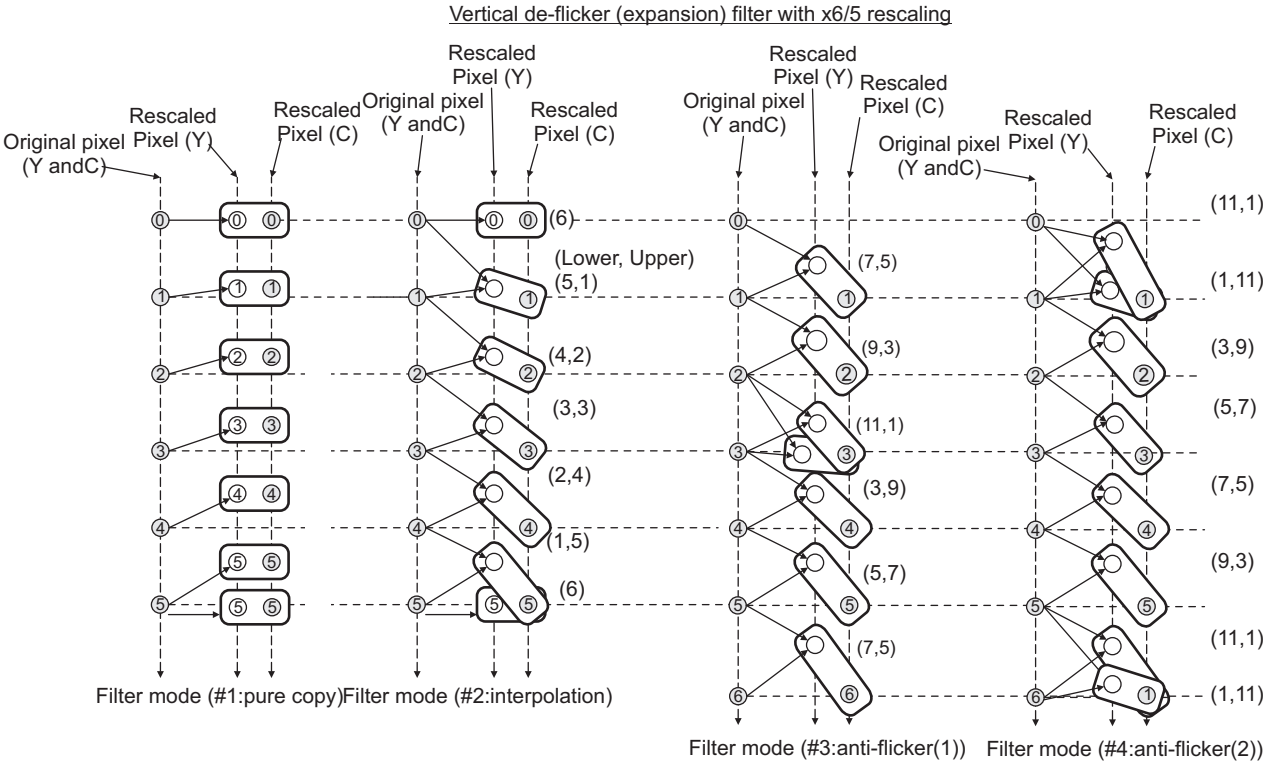


Table 54. Filtering Method for Vertical x1.2 Expansion with No Zoom

Invert bit Expand Filter (V)	0				1				0				1			
SDRAM Stored Mode	Field								Frame							
Coefficient Bit	Same		Different		Same		Different		Same		Different		Same		Different	
ON	FID = 0	2	FID = 0	2	FID = 0	2	FID = 0	3	FID = 0	2	FID = 0	2	FID = 0	2	FID = 0	4
	FID = 1	2	FID = 1	3	FID = 1	2	FID = 1	2	FID = 1	2	FID = 1	4	FID = 1	2	FID = 1	2
OFF	FID = 0	1	FID = 0	1	FID = 0	1	FID = 0	1	FID = 0	1	FID = 0	1	FID = 0	1	FID = 0	1
	FID = 1	1	FID = 1	1	FID = 1	1	FID = 1	1	FID = 1	1	FID = 1	1	FID = 1	1	FID = 1	1

The 1.2x vertical rescaling function can be also used with combination of x2/x4 zoom functions. Notice that the register configuration is the same as for x1.2 rescaling, only without zoom.

Figure 41. Filtering Method for Vertical x1.2 Expansion with 2x Zoom

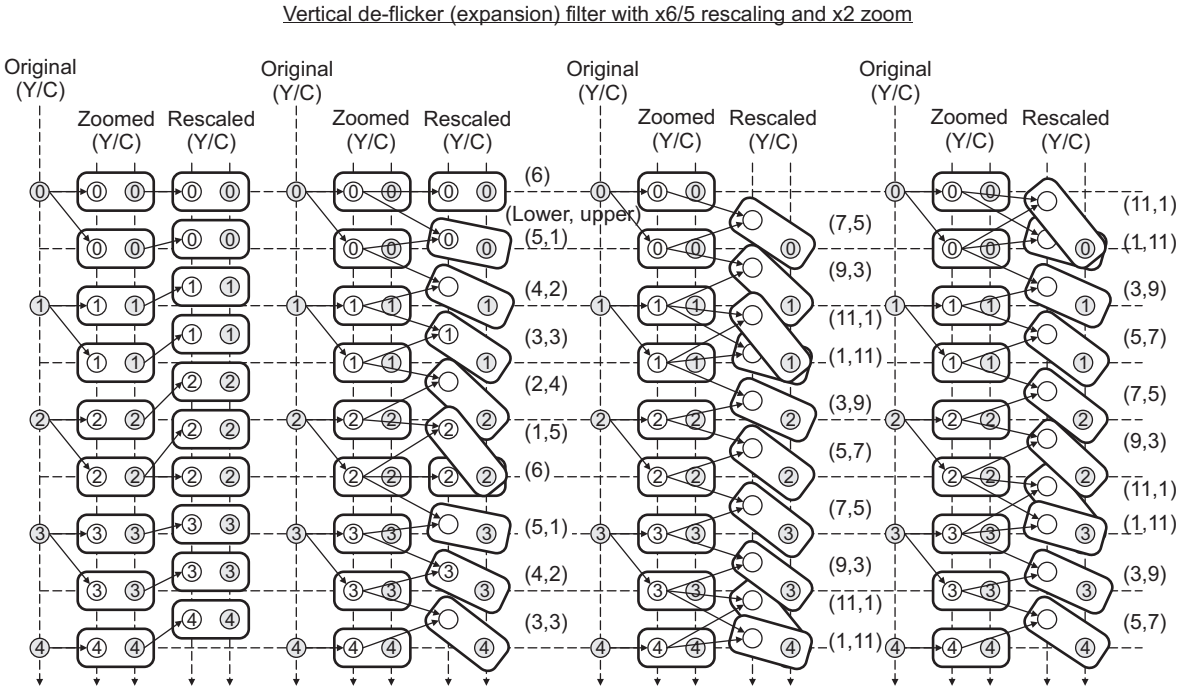
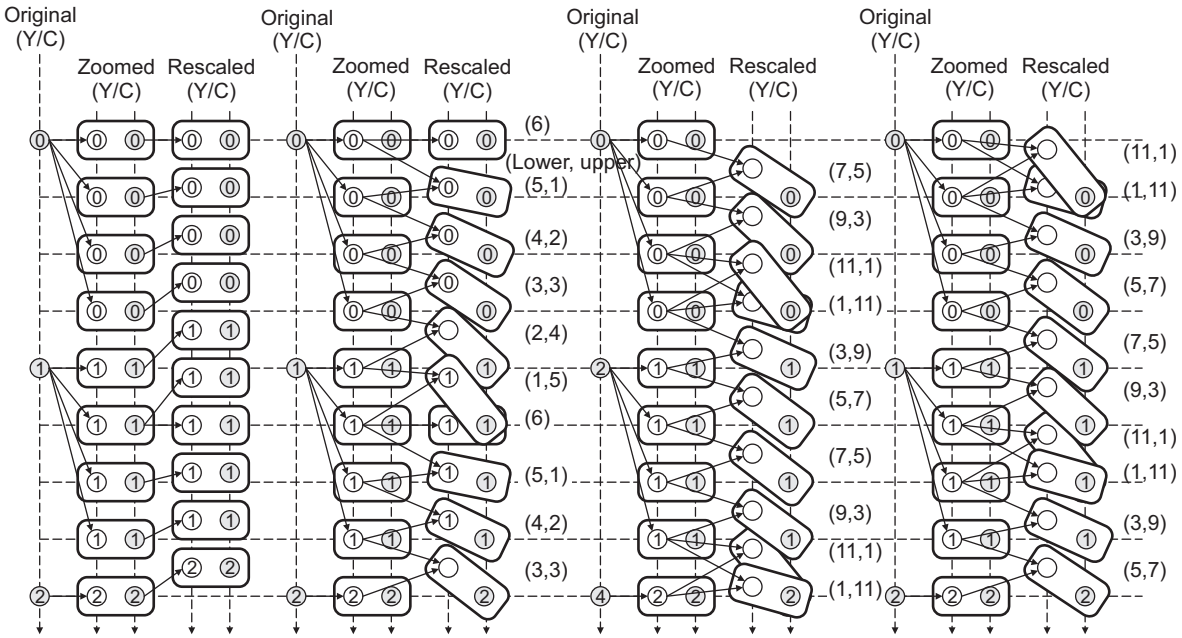


Figure 42. Filtering Method for Vertical x1.2 Expansion with 4x Zoom

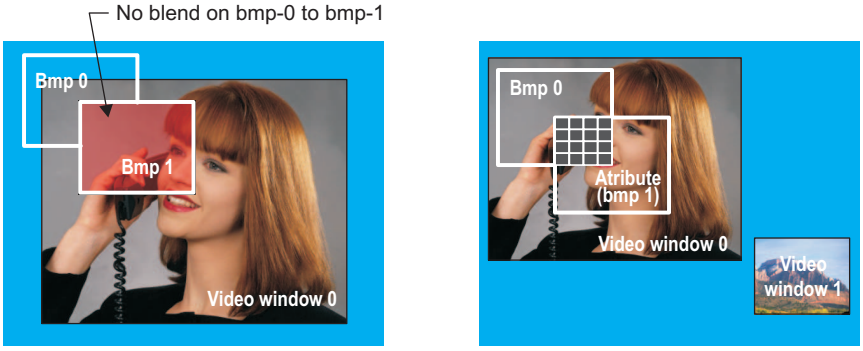


4.4.4 Bitmap Windows

The device supports two bitmap windows (OSDWIN0 and OSDWIN1) that can be displayed simultaneously. Data referenced by each bitmap window is read from external memory and displayed within the two windows.

Bitmap windows allow the user to display graphics and icons on the display unit. In typical usage, the source data is an index into a color lookup table (CLUT), either in ROM or RAM, to determine the actual display color for a given bitmap pixel value. A total of 256 CLUT entries, in 24-bit YUV color space, are available. The maximum width of a bitmap pixel is thus 8-bits. However, 1, 2, and 4-bit bitmap color depths are also supported.

Figure 43. Bitmap + Video Window Display Examples



Bitmap window 1 can be defined as an attribute window, whose data pixels modify the display attributes of the underlying Bitmap window 0.

In addition to displaying bitmap data, the OSD bitmap windows support displaying RGB data in either 16-bit RGB565 format; i.e., each R and B pixel is 5 bits and the G pixel is 6 bits or 24-bit format. The RGB data from external memory is converted into YCbCr data within the OSD module using the following equations to calculate YCrCb.

$Y = (0.2990 \times R) + (0.5870 \times G) + (0.1140 \times B)$

$Cb = (-0.1687 \times R) - (0.3313 \times G) + (0.5000 \times B) + 128$

$Cr = (0.5000 \times R) - (0.4187 \times G) - (0.0813 \times B) + 128$

The OSD bitmap windows can also display YUV422 data used by the video windows.

4.4.4.1 Color LookUp Tables

There are three possible color look-up tables (CLUTs). Two of these are fixed-ROM CLUTs and one is a user-configurable RAM CLUT. Each of the windows uses either the RAM or ROM CLUT and you must select which of the two ROM CLUTs to use for all OSD options that use the ROM CLUT (MISCCTL.RSEL). Table 55 shows the registers used for the color look-up tables.

In addition to the bitmap windows, the overall OSD background color (the color displayed in areas where no windows are displayed) is set to a specific CLUT entry and the cursor color is selected from one of the CLUT tables/values.

The RAM CLUT must be initialized before it can be used. To set up the OSD RAM CLUT, the following steps are required:

1. Wait for the CPBSY bit of the MISCCTL register to be cleared to 0.
2. Write the luma and chroma Cb values into the CLUTRAMYCB register.
3. Write the chroma Cr value and the CLUT address into the CLUTRAMCR register. The address is the offset address into the CLUT RAM table for the Y, Cb and Cr values.
4. Repeat the previous steps until the RAM table is loaded completely.

Table 55. OSD Color Look-Up Table Registers

	Register.Field	Description
ROM color look-up table selection	MISCCTL.RSEL	Selects the ROM color look-p table to use for all options that select the ROM table (0=DM270, 1=DM320)
Background color selection	MODE.BCLUT	Background CLUT selection (ROM or RAM)
	MODE.CABG	Background CLUT selection (offset into 256-bit table)
Cursor CLUT selection	RECTCUR.CLUTSR	Cursor CLUT selection (ROM or RAM)
	RECTCUR.RCAD	Rectangular Cursor color address within CLUT (offset into 256-bit table)
Bitmap window CLUT selections	OSDWIN0MD.CLUTS0	Window 0 CLUT selection (ROM or RAM)
	OSDWIN1MD.CLUTS1	Window 1 CLUT selection (ROM or RAM)
RAM CLUT Setup/Write	CLUTRAMYCB.Y	CLUTRAM Y (luma) value
	CLUTRAMYCB.CB	CLUTRAM CB (chroma) value
	CLUTRAMCR.CR	CLUTRAM CR (chroma) value
	CLUTRAMCR.CADDR	CLUTRAM address offset (writes all values)
	MISCCTL.CPBUSY	Indicates if busy when writing to CLUT RAM

The RGB equivalent CLUT values are shown in Section 4.4.4.1.1 as converted with the inverse of the OSD's RGB-to-YUV conversion matrix for RGB888 and RGB565 window data shown below.

$R = (1.00000 \times Y) + (0.00000 \times (Cb - 128)) + (1.40200 \times (Cr - 128))$

$G = (1.00000 \times Y) - (0.34414 \times (Cb - 128)) - (0.71444 \times (Cr - 128))$

$B = (1.00000 \times Y) + (1.72200 \times (Cb - 128)) + (0.00000 \times (Cr - 128))$

Note: The default YUV-to-RGB conversion matrix values in the VENC module shown below are different and thus the output colors may not exactly match those shown here.

$R = (1.00000 \times Y) + (0.00000 \times (Cb - 128)) + (1.37110 \times (Cr - 128))$

$G = (1.00000 \times Y) - (0.33690 \times (Cb - 128)) - (0.69820 \times (Cr - 128))$

$B = (1.00000 \times Y) + (1.73240 \times (Cb - 128)) + (0.00000 \times (Cr - 128))$

The YUV output of each bitmap window can be attenuated to reduce the dynamic range of the YUV signals (see Table 56). Luma values are attenuated to a range between 16-235 and chroma values are attenuated to a range between 16-240.

Table 56. OSD Bitmap Window YUV Output Attenuation Registers

Register.Field	Description
EXTMODE.ATNOSD0EN	Enable YUV attenuation for Bitmap Window 0
EXTMODE.ATNOSD1EN	Enable YUV attenuation for Bitmap Window 1

4.4.4.1.1 ROM0 Color LookUp Tables

Table 57. ROM0 Color Look-Up Table (YUV Values)

ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value
0	00 80 80	32	59 71 A2	64	72 1E F5	96	D2 08 95	128	63 46 46	160	3F 93 72	192	52 D3 4F	224	54 A7 76
1	26 5A DA	33	6E 6C AE	65	5B 6F 88	97	92 1F 93	129	17 71 71	161	26 93 72	193	8A 9B 71	225	AE 87 7F
2	4B 35 35	34	66 6C AE	66	18 68 89	98	B7 00 9F	130	4D 4B 4B	162	51 E4 37	194	48 9B 71	226	9D 88 7F
3	71 0F 8F	35	60 6A B4	67	49 4F 91	99	BD 00 A1	131	1B 6D 6D	163	58 EE 30	195	43 D1 55	227	6C 87 7F
4	0F F1 71	36	68 62 C5	68	41 4F 91	100	B5 00 A1	132	3B 55 55	164	EE 89 79	196	4A EB 46	228	64 87 7F
5	35 CB CB	37	40 40 FF	69	30 60 89	101	C4 00 A3	133	29 6F 67	165	DB 94 73	197	4A EB 46	229	53 87 7F
6	5A A6 26	38	53 5E C1	70	6E 1A 9E	102	D2 00 A5	134	8A 82 7A	166	D1 9E 6C	198	3B E1 4D	230	5B 88 7F
7	C0 80 80	39	2D 5B C6	71	50 59 8A	103	CA 10 94	135	48 82 7A	167	B9 9D 6C	199	BB 9B 72	231	4B 87 7F
8	D0 70 70	40	48 40 F5	72	48 59 8A	104	A8 32 64	136	2F 82 7A	168	A8 9E 6C	200	58 9B 72	232	43 87 7F
9	C4 AC 62	41	65 65 AF	73	77 32 95	105	AD 3E 67	137	27 82 7A	169	28 89 79	201	50 9B 72	233	6D 8E 7E
10	FB 80 80	42	4C 65 AF	74	6E 2A 96	106	A5 2D 5F	138	1E 83 7A	170	96 A7 65	202	37 9B 72	234	65 8E 7E
11	08 80 80	43	51 47 E4	75	5E 32 95	107	A6 34 5E	139	5F 8C 73	171	6E 9E 6C	203	47 AC 6A	235	22 87 7F
12	10 80 80	44	23 65 AF	76	27 59 8A	108	9A 30 59	140	8E C0 3C	172	86 A7 65	204	5E C7 5B	236	4D 96 7D
13	18 80 80	45	3B 4D D9	77	46 3A 94	109	8F 33 54	141	9B CC 2F	173	A5 B1 5F	205	E6 91 78	237	19 88 7F
14	21 80 80	46	43 45 EA	78	BE 04 A0	110	8C 2D 4E	142	BC A2 60	174	95 B1 5E	206	83 91 78	238	11 87 7F
15	29 80 80	47	1D 63 B5	79	35 4B 8D	111	84 2D 4E	143	81 DD 28	175	8C B1 5F	207	58 AC 6A	239	45 85 85
16	31 80 80	48	8B 68 AA	80	76 43 8E	112	88 29 4A	144	A8 B6 53	176	65 A7 65	208	59 A2 71	240	1C 85 85
17	4A 80 80	49	5A 4F D3	81	BE 1C 98	113	7D 24 45	145	98 B6 53	177	74 B1 5E	209	59 A2 71	241	74 87 90
18	5A 80 80	50	5D 3B F1	82	55 43 8E	114	72 50 60	146	78 D6 39	178	9A C4 51	210	51 A2 71	242	50 82 8A
19	73 80 80	51	18 68 AA	83	9C 0D 99	115	22 66 6E	147	74 E2 2D	179	62 EC 36	211	49 A2 70	243	58 82 8B
20	7B 80 80	52	45 53 C7	84	7C 1C 98	116	72 26 3F	148	62 EC 26	180	69 CC 50	212	41 A2 70	244	73 80 91
21	94 80 80	53	53 2D FF	85	B2 00 A4	117	6A 26 3F	149	C7 A0 66	181	7F AE 64	213	1F B3 69	245	00 80 80
22	A5 80 80	54	7F 5B B6	86	8A 06 9B	118	5E 5B 64	150	9C AA 5F	182	85 B8 5E	214	1F C4 61	246	FB 75 84
23	BD 80 80	55	2D 5B B6	87	AA 00 A4	119	9C 57 5F	151	5C EA 2C	183	74 B9 5E	215	B5 91 78	247	A0 84 80
24	44 7E 86	56	33 5D B0	88	B0 00 A6	120	73 2E 3E	152	AD A9 5F	184	5E AE 64	216	94 91 78	248	80 80 80
25	70 7B 8B	57	7B 4F C2	89	C4 06 9A	121	63 35 3E	153	AB B3 59	185	61 DC 48	217	7B 91 78	249	4C 34 FF
26	68 7B 8B	58	71 40 D5	90	B2 00 9C	122	2E 7B 7B	154	9B B3 58	186	B1 A5 6B	218	39 91 78	250	96 00 00
27	57 7B 8C	59	65 23 F9	91	BA 00 9C	123	31 67 67	155	A1 BD 52	187	A1 A5 6B	219	31 91 78	251	E2 00 9D
28	85 76 97	60	5F 21 FF	92	C1 00 9D	124	54 55 55	156	65 F1 2B	188	90 A5 6B	220	28 BB 68	252	1D FF 63
29	6D 76 97	61	2E 62 A4	93	B0 00 9E	125	78 41 41	157	C3 93 72	189	80 A5 6B	221	18 AA 70	253	69 FF FF
30	64 76 97	62	25 63 A5	94	98 00 9D	126	70 41 41	158	A2 93 72	190	46 A5 6B	222	63 98 77	254	B3 CC 00
31	5E 74 9D	63	6B 25 F3	95	3D 43 8D	127	4C 55 55	159	60 93 72	191	4C C0 5D	223	52 99 78	255	FF 80 80

Figure 44. ROM0 Color Look-Up Table (Equivalent RGB)

ndx	color	ndx	color	ndx	color	ndx	color	ndx	color	ndx	Color	ndx	color	ndx	color
0		224		64		96		128		160		192		224	
1		225		65		97		129		161		193		225	
2		226		66		98		130		162		194		226	
3		227		67		99		131		163		195		227	
4		228		68		100		132		164		196		228	
5		229		69		101		133		165		197		229	
6		230		70		102		134		166		198		230	
7		231		71		103		135		167		199		231	
8		232		72		104		136		168		200		232	
9		233		73		105		137		169		201		233	
10		234		74		106		138		170		202		234	
11		235		75		107		139		171		203		235	
12		236		76		108		140		172		204		236	
13		237		77		109		141		173		205		237	
14		238		78		110		142		174		206		238	
15		239		79		111		143		175		207		239	
16		240		80		112		144		176		208		240	
17		241		81		113		145		177		209		241	
18		242		82		114		146		178		210		242	
19		243		83		115		147		179		211		243	
20		244		84		116		148		180		212		244	
21		245		85		117		149		181		213		245	
22		246		86		118		150		182		214		246	
23		247		87		119		151		183		215		247	
24		248		88		120		152		184		216		248	
25		249		89		121		153		185		217		249	
26		250		90		122		154		186		218		250	
27		251		91		123		155		187		219		251	
28		252		92		124		156		188		220		252	
29		253		93		125		157		189		221		253	
30		254		94		126		158		190		222		254	
31		255		95		127		159		191		223		255	

4.4.4.1.2 ROM1 Color Look-Up Tables

Table 58. ROM1 Color Look-Up Table (YUV Values)

ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value
0	FF 80 80	32	5E A1 F3	64	61 66 CC	96	69 D5 A2	128	6C 9A 7C	160	6F 5E 55	192	77 CD 2B	224	05 7D 88
1	F9 66 84	33	58 88 F7	65	5B 4D D1	97	63 BB A7	129	66 80 80	161	69 45 59	193	71 B3 2F	225	8C 31 1C
2	F3 4D 88	34	52 6E FB	66	5A DD D1	98	5D A2 AB	130	60 66 84	162	68 D5 5A	194	6B 9A 34	226	82 37 23
3	EE 34 8C	35	4C 55 FF	67	54 C4 D5	99	57 88 AF	131	5A 4D 88	163	62 BC 5E	195	65 80 38	227	6E 42 32
4	E8 1A 91	36	F0 89 66	68	4E AA DA	100	51 6F B3	132	5A DD 89	164	5D A2 62	196	60 67 3C	228	64 48 39
5	E2 00 95	37	EA 6F 6B	69	49 91 DE	101	4C 55 B7	133	54 C4 8D	165	57 89 66	197	5A 4D 40	229	50 53 47
6	E1 91 95	38	E4 56 6F	70	43 77 E2	102	4B E6 B8	134	4E AA 91	166	51 6F 6B	198	59 DE 41	230	46 59 4E
7	DB 77 9A	39	DE 3C 73	71	3D 5E E6	103	45 CC BC	135	48 91 95	167	4B 56 6F	199	53 C4 45	231	32 64 5C
8	D5 5E 9E	40	D8 23 77	72	E1 91 4D	104	3F B3 C0	136	42 77 9A	168	4A E6 6F	200	4D AB 49	232	28 69 64
9	D0 44 A2	41	D3 09 7B	73	DB 78 51	105	39 99 C4	137	3C 5E 9E	169	44 CC 74	201	48 91 4D	233	14 75 72
10	CA 2B A6	42	D2 9A 7C	74	D5 5E 55	106	34 80 C8	138	3C EE 9E	170	3F B3 78	202	42 78 51	234	0A 7A 79
11	C4 11 AA	43	CC 80 80	75	CF 45 59	107	34 80 C8	139	36 D5 A2	171	39 9A 7C	203	3C 5E 55	235	1B F7 6D
12	C3 A2 AB	44	C6 66 84	76	C9 2B 5E	108	D1 9A 34	140	30 BB A7	172	33 80 80	204	3B EF 56	236	19 EE 6E
13	BD 88 AF	45	C0 4D 88	77	C3 12 62	109	CB 80 38	141	2A A2 AB	173	2D 66 84	205	35 D5 5A	237	15 DE 71
14	B7 6F B3	46	BB 34 8C	78	C3 A2 62	110	C6 67 3C	142	24 88 AF	174	2C F7 85	206	2F BC 5E	238	13 D5 72
15	B2 55 B7	47	B5 1A 91	79	BD 89 66	111	C0 4D 40	143	1E 6F B3	175	27 DD 89	207	2A A2 62	239	10 C4 75
16	AC 3C BB	48	B4 AA 91	80	B7 6F 6B	112	BA 34 44	144	C2 A2 1A	176	21 C4 8D	208	24 89 66	240	0E BC 76
17	A6 22 BF	49	AE 91 95	81	B1 56 6F	113	B4 1A 48	145	BC 89 1E	177	1B AA 91	209	1E 6F 6B	241	0A AA 79
18	A5 B3 C0	50	A8 77 9A	82	AB 3C 73	114	B3 AB 49	146	B6 6F 22	178	15 91 95	210	1D FF 6B	242	08 A2 7A
19	9F 99 C4	51	A2 5E 9E	83	A5 23 77	115	AE 91 4D	147	B1 56 26	179	0F 77 9A	211	17 E6 6F	243	04 91 7D
20	9A 80 C8	52	9D 44 A2	84	A5 B3 78	116	A8 78 51	148	AB 3C 2B	180	B3 AB 00	212	11 CC 74	244	02 88 7F
21	94 66 CC	53	97 2B A6	85	9F 9A 7C	117	A2 5E 55	149	A5 23 2F	181	AD 92 05	213	0C B3 78	245	EE 80 80
22	8E 4D D1	54	96 BB A7	86	99 80 80	118	9C 45 59	150	A4 B3 2F	182	A7 78 09	214	06 9A 7C	246	DD 80 80
23	88 33 D5	55	90 A2 AB	87	93 66 84	119	96 2B 5E	151	9E 9A 34	183	A1 5F 0D	215	47 58 F7	247	BB 80 80
24	87 C4 D5	56	8A 88 AF	88	8D 4D 88	120	95 BC 5E	152	98 80 38	184	9B 45 11	216	42 5B EE	248	AA 80 80
25	81 AA DA	57	84 6F B3	89	88 34 8C	121	90 A2 62	153	93 67 3C	185	96 2C 15	217	38 60 DE	249	88 80 80
26	7C 91 DE	58	7F 55 B7	90	87 C4 8D	122	8A 89 66	154	8D 4D 40	186	95 BC 16	218	33 63 D5	250	77 80 80
27	76 77 E2	59	79 3C BB	91	81 AA 91	123	84 6F 6B	155	87 34 44	187	8F A2 1A	219	29 69 C4	251	55 80 80
28	70 5E E6	60	78 CC BC	92	7B 91 95	124	7E 56 6F	156	87 34 44	188	89 89 1E	220	24 6C BC	252	44 80 80
29	6A 44 EA	61	72 B3 C0	93	75 77 9A	125	78 3C 73	157	80 AB 49	189	83 6F 22	221	19 72 AA	253	22 80 80
30	69 D4 EB	62	6C 99 C4	94	6F 5E 9E	126	77 CC 74	158	7B 91 4D	190	7E 56 26	222	14 75 A2	254	11 80 80
31	64 BB EF	63	67 80 C8	95	6F 5E 9E	127	72 B3 78	159	75 78 51	191	78 3C 2B	223	0A 7A 91	255	00 80 80

Table 59. ROM1 Color Look-Up Table (Equivalent RGB Values)

ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value
0	FF FF FF	32	FF 00 98	64	CB 33 32	96	98 33 FF	128	66 65 9A	160	32 99 32	192	00 99 FF	224	10 00 00
1	FE FF CA	33	FE 00 66	65	CC 32 00	97	99 32 CB	129	66 66 66	161	32 99 00	193	00 99 CB	225	00 EE 00
2	FE FE 98	34	FE 00 32	66	CB 00 FE	98	99 32 99	130	65 66 31	162	32 65 FE	194	00 98 99	226	00 DD 00
3	FE FF 67	35	FE 00 00	67	CB 00 CC	99	98 32 65	131	65 65 00	163	32 65 CC	195	00 98 65	227	00 BB 00
4	FF FE 33	36	CB FF FF	68	CC 00 98	100	98 32 32	132	66 33 FE	164	32 66 99	196	00 99 33	228	00 A9 00
5	FF FF 00	37	CC FE CB	69	CC 00 67	101	99 33 00	133	66 33 CC	165	32 66 66	197	00 99 00	229	00 88 00
6	FE CC FF	38	CC FE 99	70	CC 00 33	102	99 00 FF	134	65 33 98	166	33 65 32	198	00 65 FF	230	00 77 00
7	FF CB CB	39	CB FE 65	71	CC 00 00	103	99 00 CB	135	65 33 66	167	33 65 00	199	00 65 CB	231	00 55 00
8	FF CB 98	40	CB FE 33	72	99 FF FF	104	98 00 99	136	66 32 32	168	32 33 FE	200	00 65 99	232	00 43 00
9	FF CC 65	41	CB FF 00	73	99 FF CC	105	98 00 65	137	66 32 00	169	33 32 CA	201	00 66 66	233	00 21 00
10	FF CC 33	42	CC CB FF	74	98 FF 98	106	98 00 34	138	66 00 FE	170	33 33 99	202	00 66 33	234	00 11 00
11	FE CC 00	43	CC CC CC	75	98 FF 66	107	98 00 00	139	65 00 CC	171	33 32 67	203	00 66 00	235	00 00 ED
12	FF 98 FF	44	CB CC 97	76	99 FE 32	108	66 FE FF	140	66 00 98	172	33 33 33	204	00 32 FF	236	00 00 DB
13	FE 98 CB	45	CB CB 65	77	98 FE 00	109	66 FE CB	141	66 00 66	173	32 33 00	205	00 32 CB	237	00 00 BB
14	FE 98 98	46	CB CC 34	78	98 CC FF	110	66 FF 99	142	65 00 32	174	33 00 FE	206	00 32 99	238	00 00 A9
15	FF 99 65	47	CC CB 00	79	98 CC CC	111	66 FF 65	143	65 00 00	175	33 00 CB	207	00 33 66	239	00 00 88
16	FE 99 33	48	CB 99 FE	80	99 CB 98	112	65 FF 33	144	32 FF FE	176	33 00 99	208	00 33 33	240	00 00 78
17	FE 99 00	49	CB 99 CC	81	99 CB 66	113	65 FF 00	145	32 FE CB	177	32 00 65	209	00 32 00	241	00 00 54
18	FE 65 FF	50	CC 98 98	82	98 CB 32	114	65 CB FF	146	32 FE 97	178	32 00 33	210	00 00 FE	242	00 00 44
19	FE 65 CB	51	CC 98 65	83	98 CB 00	115	66 CC CC	147	32 FF 66	179	33 00 00	211	00 00 CB	243	00 00 22
20	FE 66 9A	52	CC 99 32	84	99 99 FF	116	66 CC 99	148	33 FF 32	180	00 FF FF	212	00 00 97	244	00 00 10
21	FE 66 65	53	CC 99 00	85	99 98 CD	117	65 CC 65	149	33 FE 00	181	00 FE CC	213	00 00 66	245	EE EE EE
22	FF 65 33	54	CC 65 FE	86	99 99 99	118	65 CC 33	150	32 CC FE	182	00 FE 98	214	00 00 34	246	DD DD DD
23	FF 65 00	55	CC 65 CC	87	98 99 64	119	66 CB 00	151	33 CB CC	183	00 FE 66	215	ED 00 00	247	BB BB BB
24	FE 32 FF	56	CB 65 98	88	98 98 32	120	65 98 FF	152	33 CB 98	184	00 FE 32	216	DC 00 00	248	AA AA AA
25	FF 32 CB	57	CB 65 65	89	98 99 01	121	65 99 CC	153	33 CC 66	185	00 FF 01	217	BB 00 00	249	88 88 88
26	FF 33 9A	58	CC 66 32	90	99 66 FF	122	65 99 99	154	33 CC 32	186	00 CC FF	218	AA 00 00	250	77 77 77
27	FF 33 66	59	CB 66 00	91	98 66 CB	123	66 98 65	155	32 CC 00	187	00 CC CB	219	88 00 00	251	55 55 55
28	FF 32 33	60	CC 32 FE	92	98 66 99	124	66 98 33	156	33 98 FE	188	00 CB 98	220	78 00 00	252	44 44 44
29	FE 32 00	61	CB 32 CC	93	99 65 65	125	65 98 00	157	32 98 CC	189	00 CB 64	221	53 00 00	253	22 22 22
30	FF 00 FD	62	CB 32 98	94	99 65 32	126	66 65 FD	158	33 99 99	190	00 CC 33	222	43 00 00	254	11 11 11
31	FF 00 CC	63	CB 33 67	95	99 66 00	127	66 66 CC	159	33 99 66	191	00 CC 00	223	21 00 00	255	00 00 00

Figure 45. ROM1 Color Look-Up Table (Equivalent RGB)

ndx	Color	ndx	color	ndx	color	ndx	color	ndx	color	ndx	color	ndx	color	ndx	color
0		32		64		96		128		160		192		224	
1		33		65		97		129		161		193		225	
2		34		66		98		130		162		194		226	
3		35		67		99		131		163		195		227	
4		36		68		100		132		164		196		228	
5		37		69		101		133		165		197		229	
6		38		70		102		134		166		198		230	
7		39		71		103		135		167		199		231	
8		40		72		104		136		168		200		232	
9		41		73		105		137		169		201		233	
10		42		74		106		138		170		202		234	
11		43		75		107		139		171		203		235	
12		44		76		108		140		172		204		236	
13		45		77		109		141		173		205		237	
14		46		78		110		142		174		206		238	
15		47		79		111		143		175		207		239	
16		48		80		112		144		176		208		240	
17		49		81		113		145		177		209		241	
18		50		82		114		146		178		210		242	
19		51		83		115		147		179		211		243	
20		52		84		116		148		180		212		244	
21		53		85		117		149		181		213		245	
22		54		86		118		150		182		214		246	
23		55		87		119		151		183		215		247	
24		56		88		120		152		184		216		248	
25		57		89		121		153		185		217		249	
26		58		90		122		154		186		218		250	
27		59		91		123		155		187		219		251	
28		60		92		124		156		188		220		252	
29		61		93		125		157		189		221		253	
30		62		94		126		158		190		222		254	
31		63		95		127		159		191		223		255	

4.4.4.2 Bitmap Indexing Into Color LookUp Tables

When the bitmap color depth is 8 bits (OSDWIN0MD.BMW0, OSDWIN1MD.BMW1), each 8-bit pixel value in SDRAM is a direct index into the color lookup table (CLUT). However, when the bitmap color depth is 1, 2, or 4 bits, the W*n*BMP01-W*n*BMPEF registers must be used to map the pixel values into the CLUT. Any of the 256 colors in the table can be used. For example, given 1-bit bitmap data, any of the 256 colors in the CLUT can be mapped to bit value 0 and any of the 256 colors can be mapped to bit value 1. This mapping is specified separately for each OSD bitmap window. Table 60 shows the registers which can be used to select the color for a bitmap value.

Table 60. CLUT Mapping for 1-Bit, 2-Bit, or 4-Bit Bitmaps

Register.Field (n = 0 or 1 for OSD Bitmap Window 0 or 1, respectively)	Color Corresponding to Bitmap Value		
	4-Bit Bitmap	2-Bit Bitmap	1-Bit Bitmap
WnBMP01.PAL00	0	0	0
WnBMP01.PAL01	1	-	-
WnBMP23.PAL02	2	-	-
WnBMP23.PAL03	3	-	-
WnBMP45.PAL04	4	-	-
WnBMP45.PAL05	5	1	-
WnBMP67.PAL06	6	-	-
WnBMP67.PAL07	7	-	-
WnBMP89.PAL08	8	-	-
WnBMP89.PAL09	9	-	-
WnBMPAB.PAL10	10	2	-
WnBMPAB.PAL11	11	-	-
WnBMPCD.PAL12	12	-	-
WnBMPCD.PAL13	13	-	-
WnBMPEF.PAL14	14	-	-
WnBMPEF.PAL15	15	3	1

4.4.4.3 Bitmap Window Blending and Transparency

The OSD also supports pixel blending for the bitmap windows only. If blending is enabled, the amount of blending (relative amount of video data versus bitmap data) at each pixel is determined by the blending factor.

The OSD also supports transparency blending mode. If transparency is enabled, any pixel on the bitmap display that has a value equal to that of the transparent value for that window as defined in TRANSPBMPIDX.BMPn will be transparent (only partially transparent) and allow the underlying video pixel to be displayed based on the blending factor.

Blending factor and transparency are configured using OSDWIN0MD and OSDWIN1MD registers for OSD bitmap window 0 and 1 respectively.

Table 61. Bitmap Transparency and Blending Settings

Transparency OSDWINnMD.TEn	Blending Factor OSDWINnMD.BLNDn	OSD Window Contribution	Video Contribution
OFF	0	0	1
	1	1/8	7/8
	2	2/8	6/8
	3	3/8	5/8
	4	4/8	4/8
	5	5/8	3/8
	6	6/8	2/8
	7	1	0
ON		If pixel value is equal to 0:	
	0	0	1
	1	1/8	7/8
	2	2/8	6/8
	3	3/8	5/8
	4	4/8	4/8
	5	5/8	3/8
	6	6/8	2/8
	7	1	0
		If pixel value is not equal to 0:	
	X	1	0

4.4.4.4 Attenuation in Bitmap Window (RGB Mode Only)

The OSD module has an attenuation function for use when displaying RGB data in a bitmap window. Because RGB data is displayed by converting to YC format, the converted result values may not fall into appropriate ranges for digital video. This function is useful if the video output module does not have any attenuation function (this is regulated by CCIR Rec.601 and Rec.656).

Luminance data is scaled down to 16~235 and chrominance data is scaled down to 16~240 using linear interpolation. This function is performed after conversion from RGB to YC format.

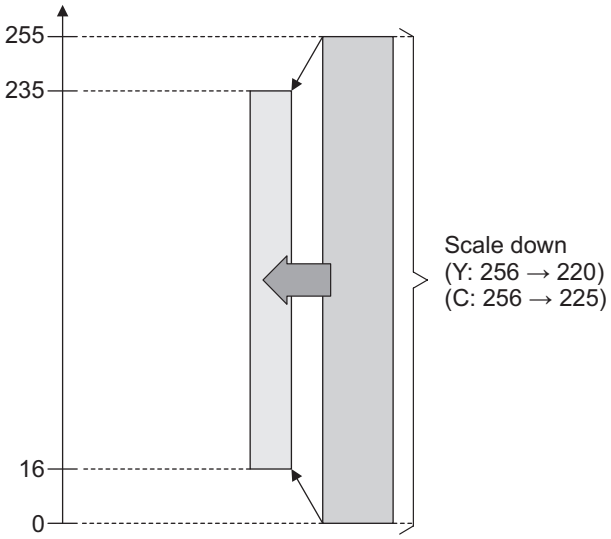
Table 62. Expansion and Anti-Flicker Filters for Video Window Registers

Register.Field	Description
EXTMODE.ATENOSD0EN	Bitmap Window 0 RGB attenuation enable
EXTMODE.ATENOSD1EN	Bitmap Window 1 RGB attenuation enable

This conversion is not performed unless the data source is RGB, even if it is enabled.

Note: For Digital RGB output, the matrix values converting from YC to RGB in the video encoder are set for the Rec.601 attenuation at the default setting.

Figure 46. Concept of Attenuation for RGB Bitmap Data



4.4.4.5 Bitmap Window Data Formats

The bitmap data formats are shown in Figure 47. Bitmap data is interpreted in bytes, with the pixels read in order from the most significant portion of the byte. Note that since each horizontal line of window data must be a multiple of 32-bytes:

- 8-bit bitmap windows must contain a multiple of 32 bytes/1 bytes/pixel = 32 pixels per horizontal line.
- 4-bit bitmap windows must contain a multiple of 32 bytes/1/2 bytes/pixel = 64 pixels per horizontal line.
- 2-bit bitmap windows must contain a multiple of 32 bytes/1/4 bytes/pixel = 128 pixels per horizontal line.
- 1-bit bitmap windows must contain a multiple of 32 bytes/1/8 bytes/pixel = 256 pixels per horizontal line.

Figure 47. Bitmap Data Formats

8−bits per pixel within 32−bit word

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
P3		P2		P1		P0	

8−bits per pixel SDRAM format

Addr	31 24	23 16	15 8	7 0
N	P3	P2	P1	P0
N+1	P7	P6	P5	P4
N+2	P11	P10	P9	P8

4−bits per pixel within 32−bit word

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
P6	P7	P4	P5	P2	P3	P0	P1

4−bits per pixel SDRAM format

Addr	31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
N	P6	P7	P4	P5	P2	P3	P0	P1
N+1	P14	P15	P12	P13	P10	P11	P8	P9
N+2	P22	P23	P20	P21	P18	P19	P16	P17

2−bits per pixel within 32−bit word

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
P12	P13	P14	P15	P8	P9	P10	P11	P4	P5	P6	P7	P0	P1	P2	P3

2−bits per pixel SDRAM format

Addr	31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
N	P12	P13	P14	P15	P8	P9	P10	P11	P4	P5	P6	P7	P0	P1	P2	P3
N+1	P28	P29	P30	P31	P24	P25	P26	P27	P20	P21	P22	P23	P16	P17	P18	P19
N+2	P44	P45	P46	P47	P40	P41	P42	P43	P36	P37	P38	P39	P32	P33	P34	P35

1−bit per pixel within 32−bit word

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P24	P25	P26	P27	P28	P29	P30	P31	P16	P17	P18	P19	P20	P21	P22	P23	P8	P9	P10	P11	P12	P13	P14	P15	P0	P1	P2	P3	P4	P5	P6	P7

1−bit per pixel SDRAM format

Addr	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
N	P24	P25	P26	P27	P28	P29	P30	P31	P16	P17	P18	P19	P20	P21	P22	P23	P8	P9	P10	P11	P12	P13	P14	P15	P0	P1	P2	P3	P4	P5	P6	P7
N+1	P56	P57	P58	P59	P60	P61	P62	P63	P48	P49	P50	P51	P52	P53	P54	P55	P40	P41	P42	P43	P44	P45	P46	P47	P32	P33	P34	P35	P36	P37	P38	P39
N+2	P88	P89	P90	P91	P92	P93	P94	P95	P80	P81	P82	P83	P84	P85	P86	P87	P72	P73	P74	P75	P76	P77	P78	P79	P64	P65	P66	P67	P68	P69	P70	P71

4.4.4.6 Bitmap Window Data — RGB Formats

OSD bitmap windows also support the display of 16-bit and 24-bit RGB source data. This data in internally converted to YUV422 prior to entering the OSD module for blending. The RGB data from external memory is converted into YCbCr data within the OSD module using the following equations to calculate YCrCb.

Y = 0.2990*R + 0.5870*G + 0.1140*B

Cb = -0.1687*R - 0.3313*G + 0.5000*B + 128

Cr = 0.5000*R - 0.4187*G – 0.0813*B + 128

While there is no restriction on bitmap data formats (both bitmap windows can be RGB16 or RGB25 or one of each), only one transparency color key setting is provided.

Table 63. RGB Control Registers

Control Register	Window
OSDWIN0MD.BMP0MD	Defines data source format for Bitmap Window 0
OSDWIN1MD.BMP1MD	Defines data source format for Bitmap Window 1
TRANSPVALL.RGBL	Transparency value (RGB565) for RGB565 data, or lower 16-bit of transparency value (GB) for RGB888.
TRANSPVALU.RGBU	Transparency value upper byte (R) for RGB888.

The 16-bit RGB565 data is stored in DDR2/mDDR in 16-bit words. Within each 16-bit element, the red value is least significant, followed by the green, then blue, as shown in Figure 49.

The DDR format for RGB565 data is shown below.

Figure 48. Data Format – RGB565

(a) RGB565 pixels within 32-bit word

31 27	26 21	20 16	15 11	10 5	4 0
R1	G1	B1	R0	G0	B0

(b) RGB565 SDRAM format

Address	31 27	26 21	20 16	15 11	10 5	4 0
N	R1	G1	B1	R0	G0	B0
N + 1	R3	G3	B3	R2	G2	B2
N + 2	R5	G5	B5	R4	G4	B4
...	...					

Note that since each horizontal line of window data must be a multiple of 32-bytes, the RGB565 windows must contain a multiple of 32-bytes / 2 byte/pixel = 16 pixels per horizontal line.

The 24-bit RGB888 data is stored in DDR2/mDDR in 32-bit words. Within each 24-bit element, the red value in the least significant byte, followed by the green, then the blue byte, as shown in Figure 49. The three lower bits of the MSByte are interpreted as pixel-level blending bits.

Figure 49. Bitmap Data Format – RGB888

(a) RGB565 pixels within 32-bit word

31 27	26 24	23 16	15 8	7 0
n/a	Blend0	RO	G0	R0

(b) SDRAM format

Address	31 27	26 24	23 16	15 8	7 0
N	n/a	Blend0	R0	G0	B0
N + 1	n/a	Blend1	R1	G1	B1
N + 2	n/a	Blend2	R2	G2	B2

4.4.4.7 OSD Bitmap Window —YUV422 Format

The OSD windows can also display YUV422 data. See the Video Window descriptions for the data formats.

4.4.4.8 OSD Attribute Window

OSD bitmap window 1 can be configured as an attribute window (OSDWIN1MD.OASW and OSDATRMD.OASW) instead of a bitmap window, see Figure 50. In this mode, the attribute window allows blending and blinking on a pixel-by-pixel basis in bitmap window 0. In particular, the attribute window provides a means to:

- Set the blending level (3 bits, 8 levels) of individual pixels in OSD window 0
- Set individual pixels in OSD window 0 to blink, if blinking is enabled

Table 64. OSD Attribute Pixel Format

Bit 3	Bit 2	Bit 1	Bit 0
Blink Enable 0: No blink 1: Blink	Blend factor		

Figure 50. OSD Attribute Window

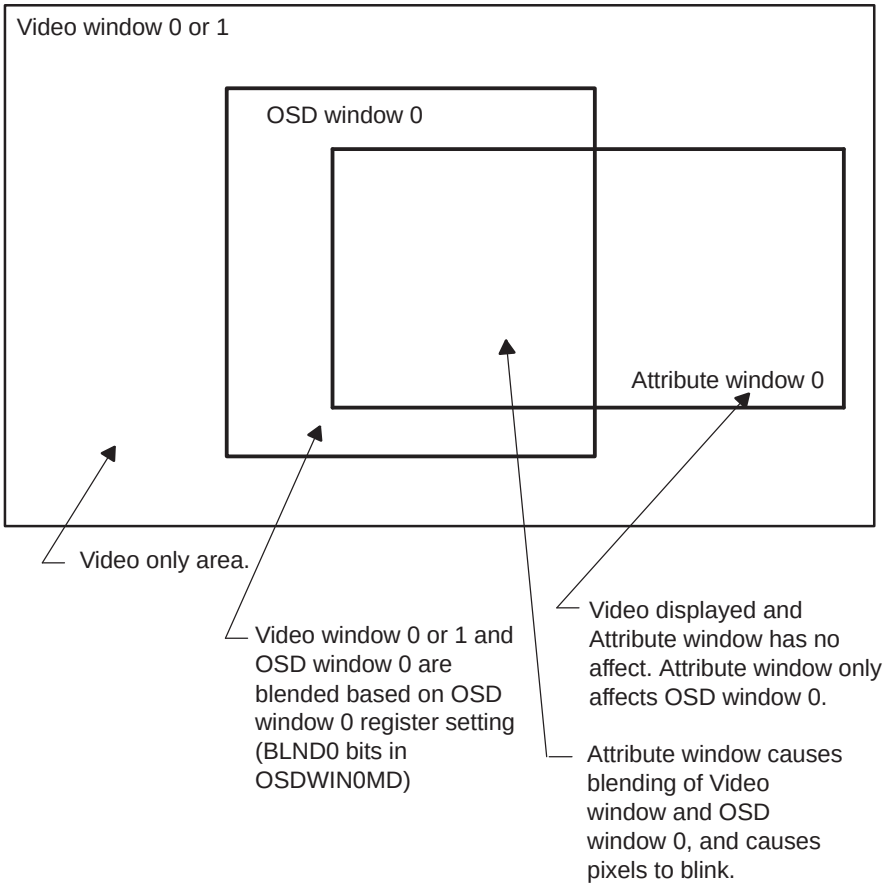


Table 65. OSD Blink Attribute Control Registers

Control Register.Field	Description
OSDATRMD.BLNK	Enable blinking defined by attribute window
OSDATRMD.BLNKINT	Set the blink interval

The SDRAM data format follows that for 4-bit bitmap windows (see Figure 47). Note that since each horizontal line of window data must be a multiple of 32 bytes, the attribute windows must contain a multiple of 32 bytes/ 1/2 byte/pixel = 64 pixels per horizontal line.

4.4.5 OSD – Cursor Window

The rectangular hardware cursor always appears on top of all other OSD windows. The cursor size, color, horizontal and vertical thickness can be specified (see Table 66). This cursor can also be configured to use the ROM or RAM CLUT.

Figure 51 shows an example usage of the rectangle cursor. The outline shows the rectangle cursor and the ICON 1-4 windows are displayed by using OSD window 0 or 1.

Table 66. OSD Cursor Window Control Registers

Control Register	Description
RECTCUR.RCAD	Cursor color address (offset into CLUT)
RECTCUR.CLUTSR	Cursor CLUT selection (RAM or ROM)
RECTCUR.RCHW	Rectangular Cursor Horizontal Width
RECTCUR.RCVW	Rectangular Cursor Vertical Width

Figure 51. Cursor Window Example

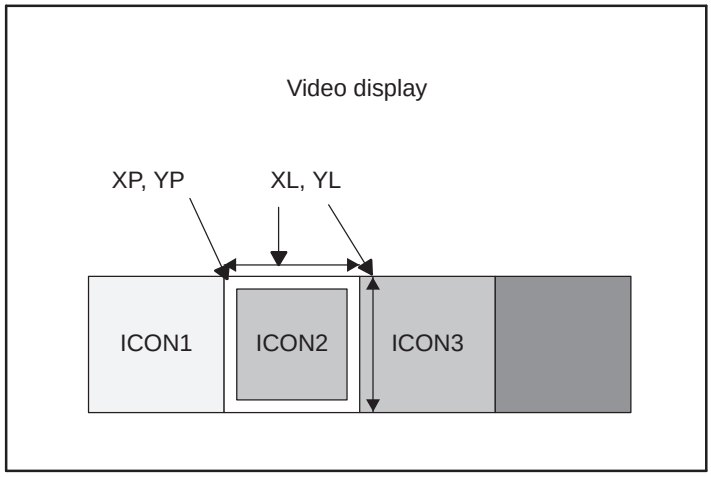
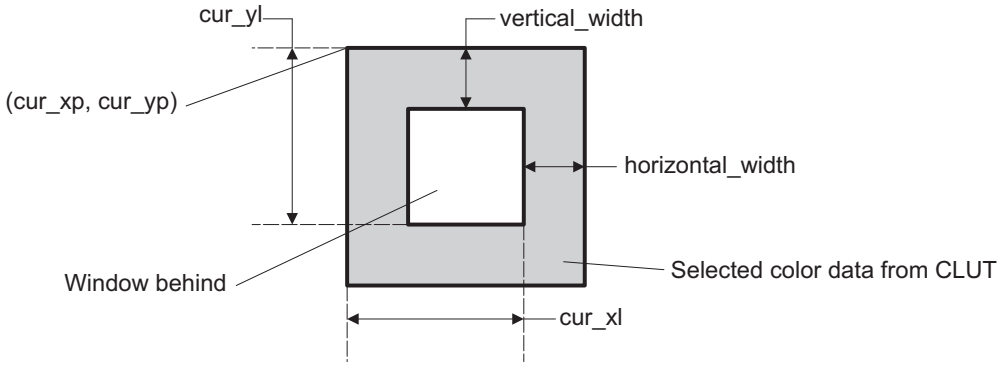


Figure 52. Cursor Window Configuration



4.5 Video Encoder Module

The video encoder (VENC) module consists of two main submodules, and an analog NTSC/PAL video encoder with integrated 1-channel, 27-MHZ video DAC with buffer and a digital LCD/video controller.

4.5.1 Video Timing Mode

The VENC module supports two timing modes: standard NTSC/PAL and non-standard (user-defined).

4.5.1.1 Standard Mode

In this mode, the timing generator operates in the standard format. The support formats are 525/60 Hz (NTSC-M) or 625/50 Hz (PAL-B/D/G/H/I) for SDTV. The digital output from the LCD interface is also available simultaneously. Note, however, this is limited to LCDs that support NTSC/PAL timing and the output will mirror the analog output display.

4.5.1.2 Nonstandard Mode

This mode is provided to configure the user-defined generic timing. The VENC module operates at any given timing defined by the module's register settings. In this mode, the VENC block is automatically disabled. To select non-standard mode, set VMOD.VMD to 1.

4.5.2 Synchronous Mode

The VENC module supports two synchronous modes: master and slave. Each mode can be used in either of the two video timing modes (standard NTSC/PAL and non-standard).

4.5.2.1 Master Mode

This mode operates in synchronization with horizontal/vertical sync signals generated by the timing generator in the VENC module.

4.5.2.2 Slave Mode

This mode operates in synchronization with sync signals input from an external source. To configure the video encoder as a slave device, set VMOD.SLAVE to 1.

1. When SYNCCTL.EXSYNC is cleared to 0, the external inputs from the HSYNC/VSYNC/FIELD pins are used as the external sync signals. It is also required to set VIDCTL.SYDIR to 1 to configure the HSYNC/VSYNC/FIELD pins as input.
2. When SYNCCTL.EXSYNC is set to 1, the sync signals from the CCD controller (see the device VPFE Programmer's Guide) are used as external sync signals. This provides synchronization between the CCD timing and video timing. It is possible to invert the timing signals by setting the EXHIV, EXVIV, and EXFIV fields in the SYNCCTL register.

4.5.3 Analog NTSC/PAL Video Encoder

The NTSC/PAL encoder (Figure 53) takes video data from the OSD module and generates the necessary signaling and formatting to display the video/image data onto an NTSC/PAL display. The RVTYP field of the VMOD register (see Table 67) specifies the video formats.

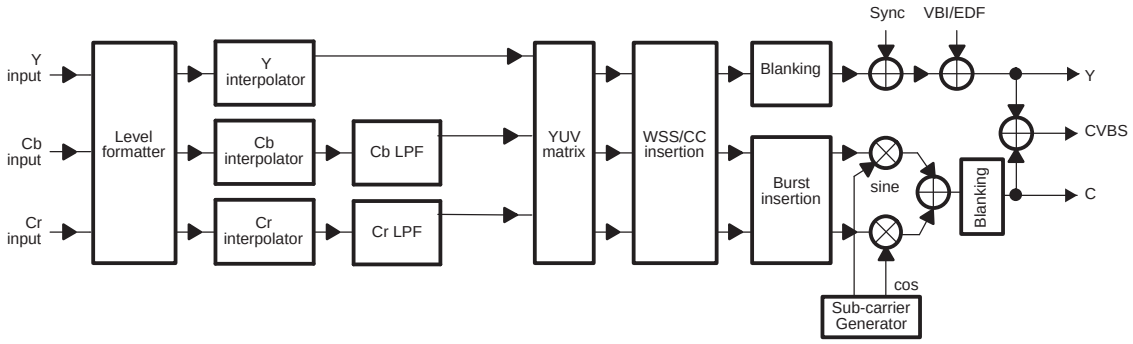
Table 67. Supported TV Formats

VMD	TVTYP	ITLC	ITLCL	NSIT	Video Format
0	0	0	-	-	NTSC
0	0	1	0	-	Non-interlace 262 line/field
0	0	1	1	-	Non-interlace 263 line/field
0	1	0	-	-	PAL
0	1	1	0	-	Non-interlace 312 line/field
0	1	1	1	-	Non-interlace 313 line/field
1	-	-	-	0	Progressive
1	-	0	-	1	Interlace
1	-	1	-	1	Interlace (FIELD low fix)

Other composite DAC/timing settings are made via fields in the CVBS and ETMG0/1 registers.

The BLNK field in the VMOD register is the blanking enable. When this field is set to 1, the CVBS and/or component output is blanked without regard to the input video signals.

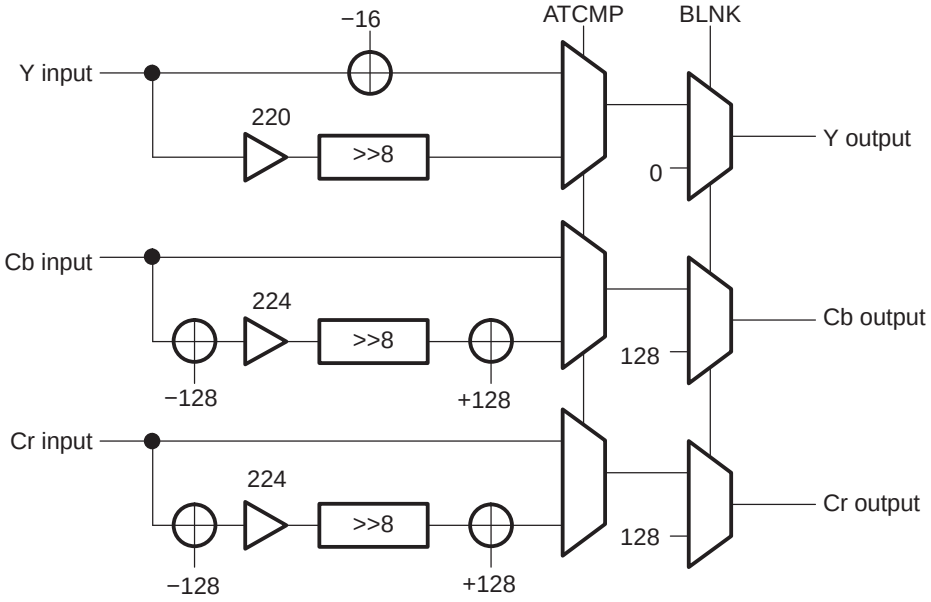
Figure 53. NTSC/PAL Video Encoder Block Diagram



4.5.3.1 Level Formatter

The front-end of the video encoder receives the YCbCr pixel data from the OSD module and converts it into the digital YCbCr, YUV, and RGB representations. The level formatter has the role to compress the signal level with 0-255 into the ITU-R BT.601 specified level (Y:16-235, C:16-240). The user can choose whether or not to apply the attenuation independently for each data path using the ATCOM, ATYCC, and the ATRGB fields in the VDPRO register. Figure 54 shows the block diagram for the level formatter.

Figure 54. Level Formatter Block Diagram



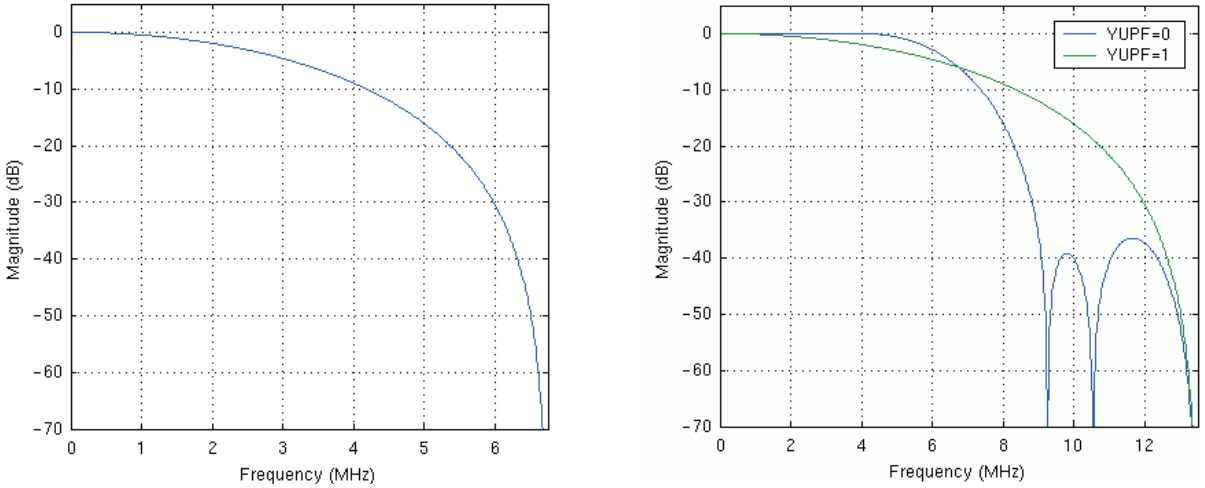
4.5.3.2 Luma Signal Processing

The luma signal from the level formatter can be processed by a 2× interpolation with a filter. The interpolation filter has 11 taps with a transfer function of:

$[3 - 10_{(z-2)} + 39_{(z-4)} + 64_{(z-5)} + 39_{(z-6)} - 10_{(z-8)} + 3_{(z-10)}]/64$

The interpolation is disabled by default and can be enabled by setting VDPRO.YUPS = 1. When in progressive mode, the interpolation should be disabled since the pixel rate is already 27 MHZ. The frequency response of the luma interpolation filter is shown in Figure 55. A low-pass filter follows the interpolation filter. The LPF is provided only for compatibility with previous devices for test purposes. It is disabled by default and is not supported.

Figure 55. Luma LPF (left) and Luma Interpolation Filter (right)



4.5.3.3 Chroma Signal Processing

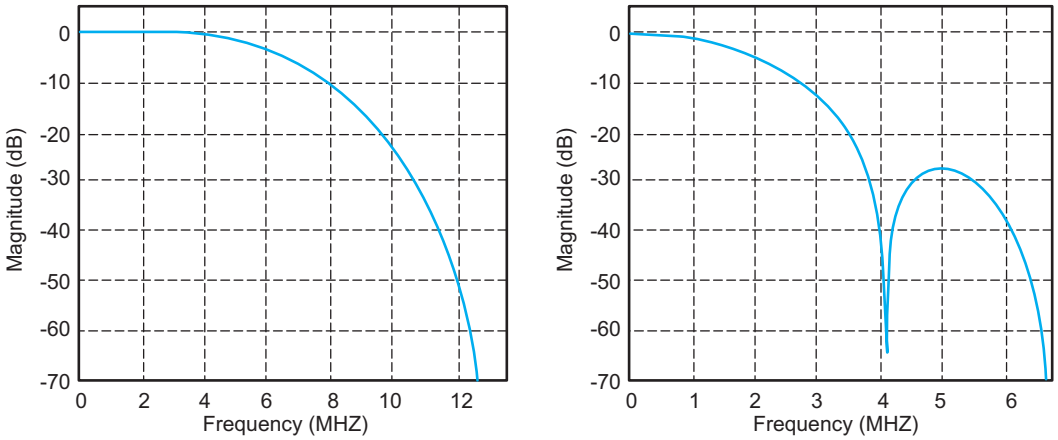
The chroma signal from the level formatter can also be processed by a 2× interpolation with a filter. Two cut-off frequencies, 1.5 MHz or 3.0 MHz can be selected by CVBS.CRCUT. The transfer functions are:

[3 + 8(z-1)+ 10(z-2) + 8(z-3)+ 3(z-4)]/32 for CRCUT=0 and

(-1+8z-1+18z-2+8z-3-1z-4)/32 for CRCUT=1

The interpolation is disabled by default and can be enabled by setting VDPRO.CUPS = 1. The sampling rate of the LPF is 1/2 VENC clock (13.5 MHz). There are two outputs of this LPF block, composite and component. Low-pass filtering is only processed for composite output. No filtering is applied to the component output. The frequency response of the chroma interpolation filter is shown in Figure 56.

Figure 56. Chroma Interpolation Filter (left) and Chroma LPF (right)



4.5.3.4 CVBS Output

4.5.3.4.1 YUV Conversion

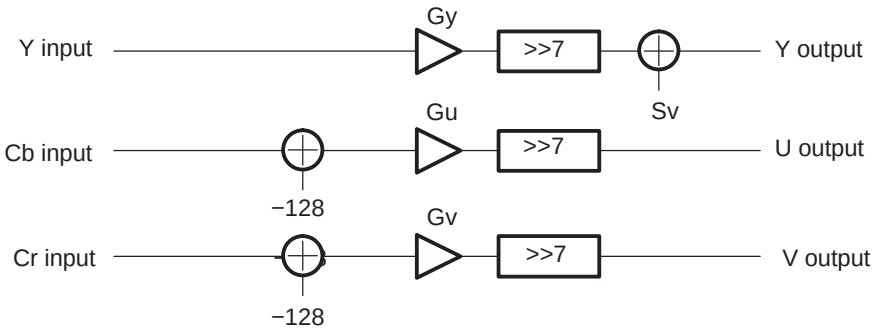
The interpolated and low pass filter YCbCr data are applied the proper gain and are then converted to YUV signals for CVBS generation. Table 68 shows the gain applied for each mode.

Table 68. Gains Used in YUV Conversion

CVBS.CVLVL	CVBS.CSTUP	Gy	Gu	Gv	Sv
0	0	305	315	444	0
	1	282	291	411	39
1	0	299	309	435	0
	1	277	285	403	38

The processing is done by subtracting 128 for the chroma (not for the luminance), then multiplying the gain and shifting right by 7. Figure 57 shows the block diagram for YCbCr to YUV conversion. When the CVBS.CSTUP = 1, then 7.5% setup is added for the output. The setting CSTUP is effective for both NTSC or PAL. However, note that for PAL mode, setting CSTUP = 1 causes an illegal output level.

Figure 57. YUV Conversion Block Diagram



4.5.3.4.2 CVBS Output Generation

The scaled luma then has the WSS and closed caption signals inserted and then is applied to the video edge controller. The video edge controller clips the video level of a few pixels around the horizontal blanking edge so that the output video has the proper blanking transition. This feature is enabled by default and can be disabled by CVBS.CBLS. Please refer to Section 2.1.3.2 for details of blanking edge shaping. Horizontal blanking start/end position can be adjusted by the CFPW and CLBI fields in the ETMG1 register. Following the edge shaping, the sync pulse (and optionally Macrovision pulses) are inserted. The horizontal sync pulse duration can be adjusted by the CEPW and CFSW fields in the ETMG0 register.

The scaled chroma signals (U and V) are modulated onto the sub-carrier following color burst insertion. The SC-H (sub-carrier to horizontal) phase can be controlled by the user. The SCSD field in the SCPROG register automatically updates the sub-carrier phases. The update occurs at line 9 in the color field 1 for both NTSC and PAL. By default, the values shown in Table 69 are applied. These values are chosen so that the SC-H phase is close to 0.

Table 69. Sub-Carrier Initial Phase Default Value

Mode	Preset Value
NTSC	378
PAL	356

Color burst insertion horizontal position can be controlled by the CBST and CBSE fields in the ETMG1 register. The modulated chroma signal is also applied to blanking edge shaping. Chroma blanking shaping can also be disabled by CBLS and blanking horizontal position is also adjusted by CFPW and CLBI.

The resulting Y and C are mixed together to get composite video output. Separated Y and C are also available for S-Video output. The offset 512 is added to the separated C to have the blanking level at the center of the DAC range. You can also control the blanking build-up time (Table 70) and the sync build-up time (Table 71).

Table 70. CVBS Blanking Build-Up Time

CVBS.CBBLD	Time
0	140 ns
1	300 ns

Table 71. CVBS Sync Build-Up Time

CVBS.CSBLD	Time
0	140 ns
1	200 ns

4.5.3.5 DAC Output

4.5.3.5.1 DAC Output Level

The video encoder has a 10-bit digital output to the DAC input. It is designed so that the full digital output (7FFh = 1023) is expected to be converted to 1400 mV. In consideration of this, the user needs to take care of the DAC termination.

4.5.3.5.2 DAC Output Disable/Power Down

Setting VMOD.VIE to '0' will force the output of the DAC to a low voltage level regardless of the video signal. The DAC can also be powered down by setting the DAPD0 field in the DACTST registers. By default this registers are set to '1' so the user must set them to 0 to enable before using the analog output.

4.5.3.5.3 DAC DC Output Mode

The DACs support outputting a DC output instead of an analog output from the DAC pins. Setting the DADC bit in DACTST to 1 switches DAC digital input from normal video signal to the digital signal level, as specified in DACTST.DALVL.

4.5.3.5.4 Y/C Delay

The Y signal delay can be adjusted and different delays can be applied to CVBS and component. The CVBS.CYDLY adjusts the Y delay for CVBS output.

4.5.3.5.5 Video Attribute Insertion

The video encoder has the capability to insert video information into the vertical blanking period. For example, the video encoder can insert a video attribute which indicates the proper aspect ratio to the video receiver. For NTSC mode, the video encoder can insert 14-bit video information on line 20 and line 283 to conform to the EIAJ CPR-1024 Video Aspect Ratio ID specification. Attribute information should be set using the ATR1 and ATR0 registers. The ATR2 register should be set with the 6-bit CRC data that is calculated by the following equation:

$G(x) = x^6 + x + 1$, where x^6 and x are preset to 1.

Bit 7 of ATR2 enables attribute insertion.

For PAL mode, the video encoder can insert 14-bit video information (WSS) on line 23 of every frame to conform to the ITU-R BT.1119-2 (ETSI EN 300 294) Wide Screen Signaling specification. Attribute information should be set in ATR1 register and ATR2 bits 5-0. Bit 7 of ATR2 enables attribute insertion.

In NTSC and PAL encoding modes, data in the ATR1 and ATR0 registers are transferred to internal circuitry when ATR2 is set. For this reason, ATR2 should be set last.

The video encoder also supports video ID insertion for progressive. EIAJ CPR-1204-1 for 525p and IEC 62375 for 625p. Usage of ATR0-ATR2 registers is same as in SDTV (NTSC for 525p, PAL for 625p).

4.5.3.5.6 Closed-Captioning

The video encoder supports closed-caption encoding. Closed-caption data is transmitted on line 21 of the odd field and line 284 of the even field in NTSC. It is possible to specify the fields on which closed-captioning is enabled by CAPCTL.CAPF.

The data should be written to the CAPDO or CAPDE registers for odd or even fields, respectively. It is required to load the data at least 1 line early. When data is written to CAPDO/CAPDE, VSTAT.CAOST/VSTAT.CAEST) is changed to 1. This bit is automatically cleared to 0 when caption data transmission is completed on line 21 in the odd field or line 284 in the even field.

When the caption data register (CAPDO or CAPDE) is not updated before the caption data transmission timing for the corresponding field, the ASCII code specified by CAPCTL.CADF is automatically transmitted for closed caption data.

The width of every data register is 7 bits and the parity bit is automatically calculated by hardware.

4.5.3.5.7 Sub-Carrier Generation

The video encoder generates the sub-carrier by internal direct digital synthesizer (DDS). The phase resolution of DDS is (1/1024) × 360°.

Sub-carrier to Horizontal (SC-H) phase can be controlled by the user. Writing SCPROG.SCSD automatically updates the sub-carrier phase as the specified value. Update occurs at line 9 in color field 1 for both NTSC and PAL. By default, preset values shown in Table 72 are applied. These values are chosen so that SC-H phase close to 0°.

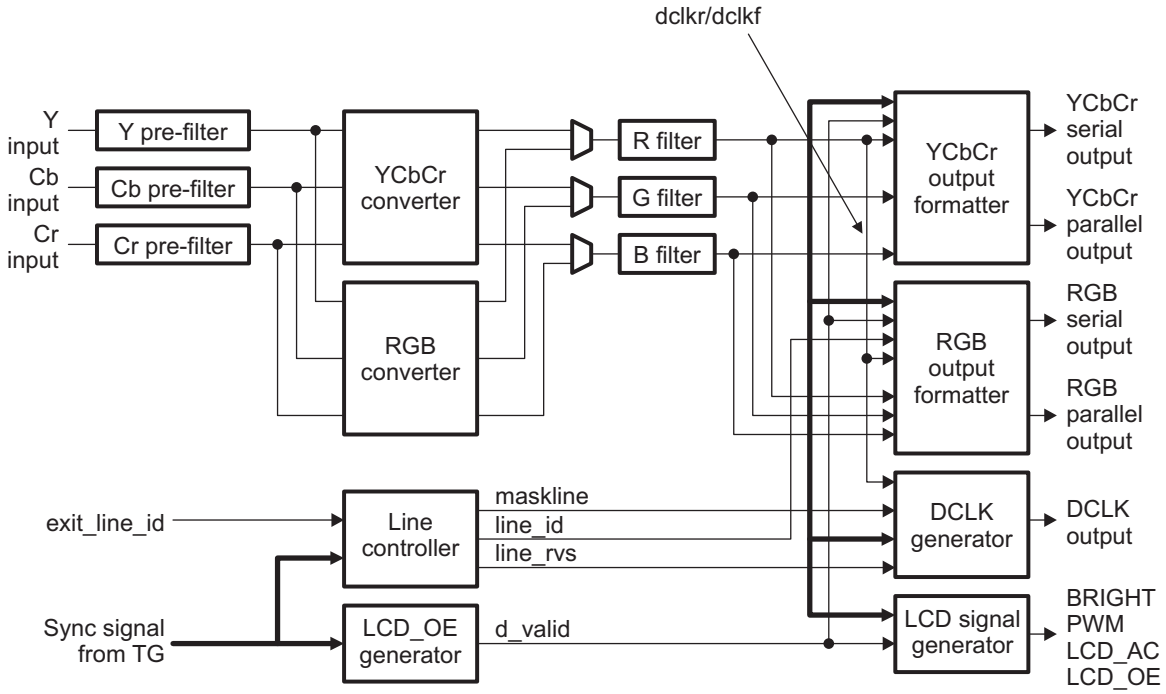
Table 72. Sub-Carrier Initial Phase Default Values

Mode	Preset Value
NTSC	378
PAL	356

4.5.4 Digital LCD Controller

The digital LCD controller is shown in Figure 58.

Figure 58. Digital LCD Controller Block Diagram



4.5.4.1 Digital Video Output Mode

The digital LCD controller supports eight digital output modes. The mode can be selected by VMOD.VDMD and are shown in Table 73.

Table 73. Digital Video Output Modes

VDMD	Mode	Description
0	YCC16	16-bit YCbCr output mode. Y and C are output separately on 16-bit bus.
1	YCC8	8-bit YCbCr output mode. 422 YCbCr is time-multiplexed on the 8-bit bus. Optionally supports ITU-R BT.656 output.
2	PRGB	Parallel RGB mode to output RGB separately.
3	SRGB	Serial RGB mode to output RGB sequentially

4.5.4.2 Timings

The timing parameter control registers are shown in Table 74. Figure 59 to Figure 61 show the timing charts for HSYNC, VSYNC, FIELD and LCD_OE. For interlaced operation when VMOD.NSIT is 1, the vertical interval and pulse width is counted by half line (0.5H).

Table 74. Timing Control Registers

Register	Description	Unit[(1)]
HSPLS	HSYNC pulse width	CLK
VSPLS	VSYNC pulse width	H (0.5H)
HINT	HSYNC interval (HINT + 1). Must be even when OSD clock is 1/2 VENC clock (standard timing)	CLK
HSTART	Horizontal data valid start position	CLK
HVALID	Horizontal data valid duration	CLK
VINT	VSYNC interval (VINT + 1)	H (0.5H)
VSTART	Vertical data valid start position	H
VSTARTA	Vertical data valid start position (optionally available only for even field).	H
VVALID	Vertical data valid duration	H
HSDLY	HSYNC delay	CLK
VSDLY	VSYNC delay	CLK

(1) Value in brackets apply to interlace (NSIT = 1)

Figure 59. Horizontal Timing

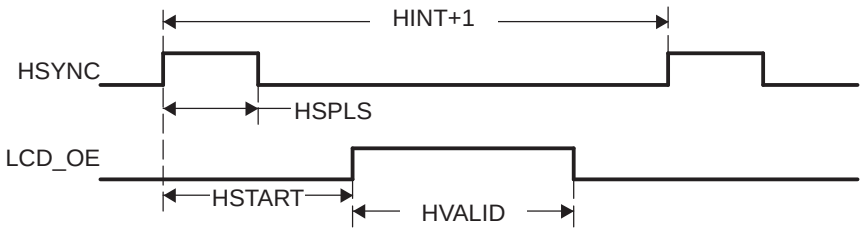
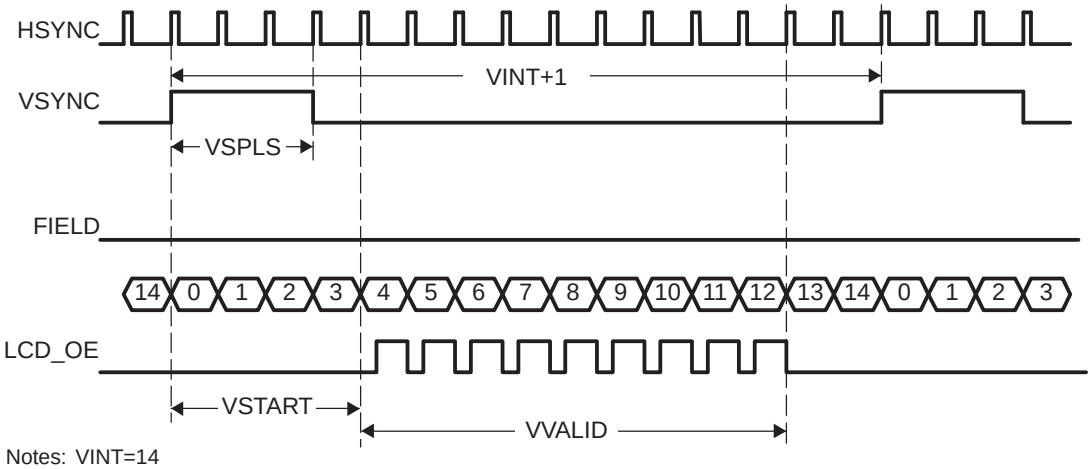
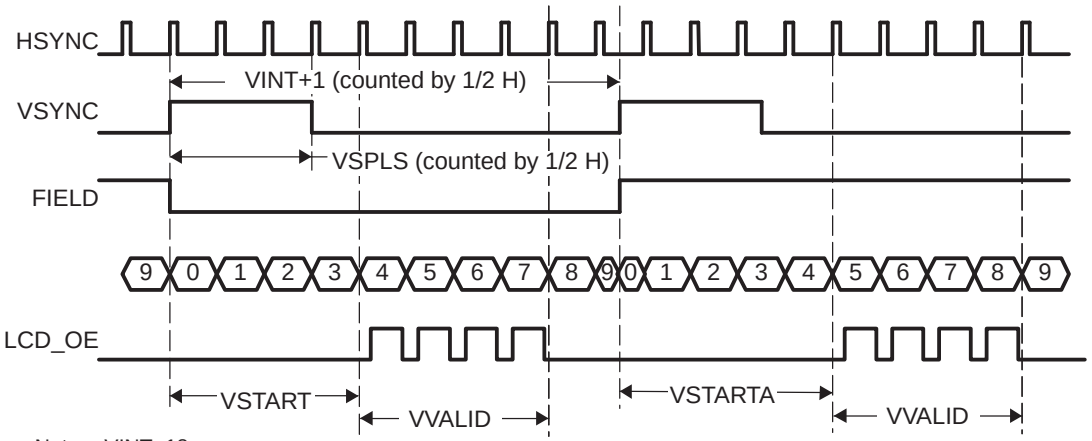


Figure 60. Vertical Timing (Progressive)



Notes: VINT=14
VSTART=4
VSPLS=3
VVALID=9

Figure 61. Vertical Timing (Interlaced)



Notes: VINT=18
VSTART=4
VSPLS=6
VVALID=4
VSTARTA=5

When in interlaced mode (VMOD.NSIT = 1 or NTSC/PAL), different VSTART positions can be specified for odd and even fields. VSTART is for odd fields and VSTARTA is for even fields.

The HSYNC and VSYNC outputs can be delayed via HSDLY and VSDLY registers, respectively, without affecting the timing of the internal sync signals. The FIELD output is also delayed by VSDLY. The delays unit is CLK.

In standard mode operation (VMOD.VMD = 0), horizontal and vertical pulse width and interval timings are fixed by hardware to conform to the video standard regardless of the HSPLS, VSPLS, HINT, and VINT registers. Regarding pulse width, the optional sync pulse width processing mode is provided to program standard mode sync pulse width by the HSPLS and VSPLS registers. This mode is enabled when SYNCTL.SYSW is 1. When interlaced (VMOD.HDMD = 0), VSYNC pulse width is counted in 0.5H (half lines). The parameters are shown in Table 75.

Table 75. Standard Video Timing

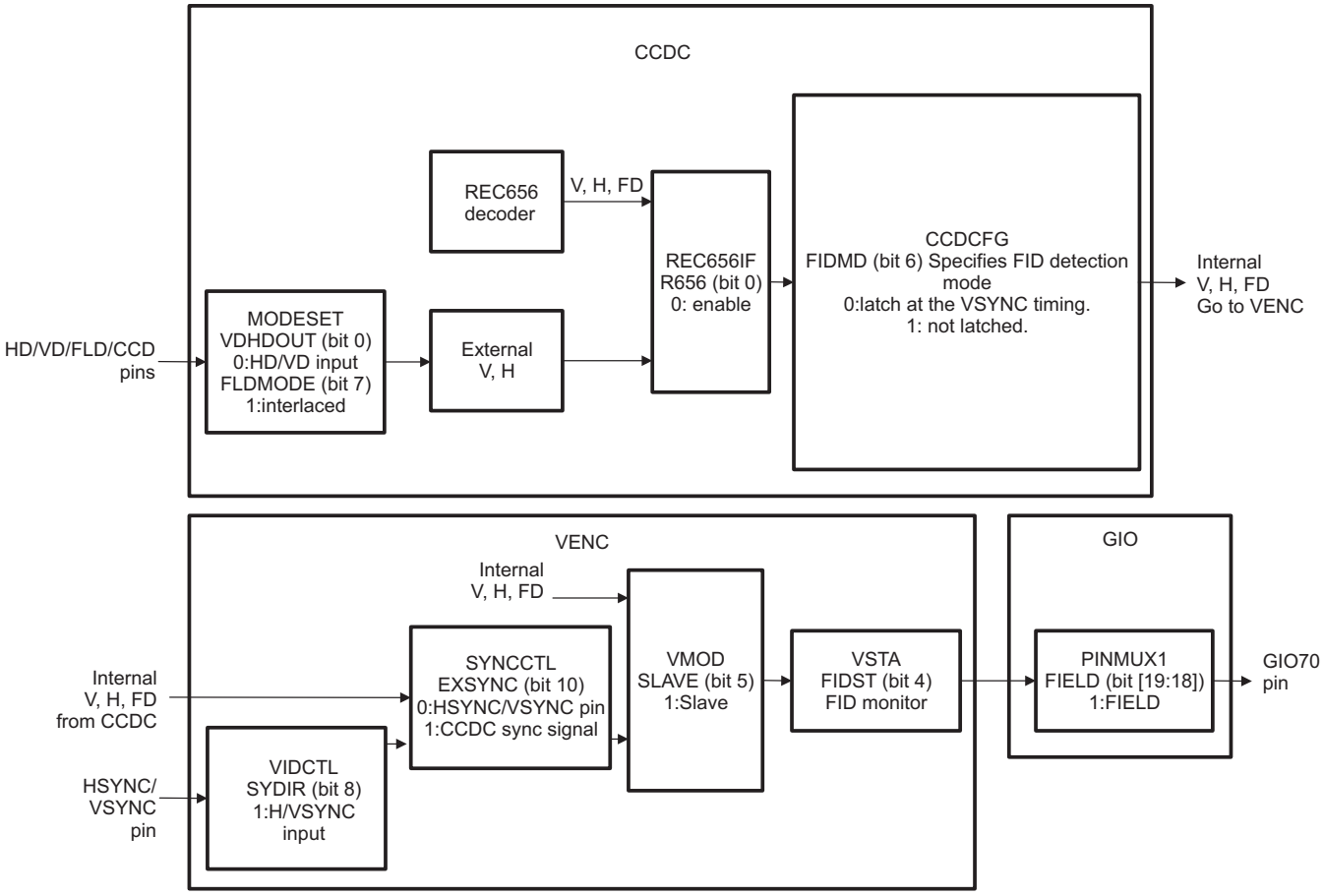
Parameter	SDTV (HDMD = 0)		Unit
	NTSC (TVTYP = 0)	PAL (TVTYP = 1)	
HSYNC pulse width	127	127	CLK
VSYNC pulse width	6	5	H
Horizontal interval	1716	1724	CLK
Vertical interval	262.5	312.5	H

4.5.4.3 Slave Mode Timings

4.5.4.3.1 Slave Mode Sync Path Using VPFE

Figure 62 illustrates how to set the VENC slave mode.

Figure 62. Slave Mode Sync Path

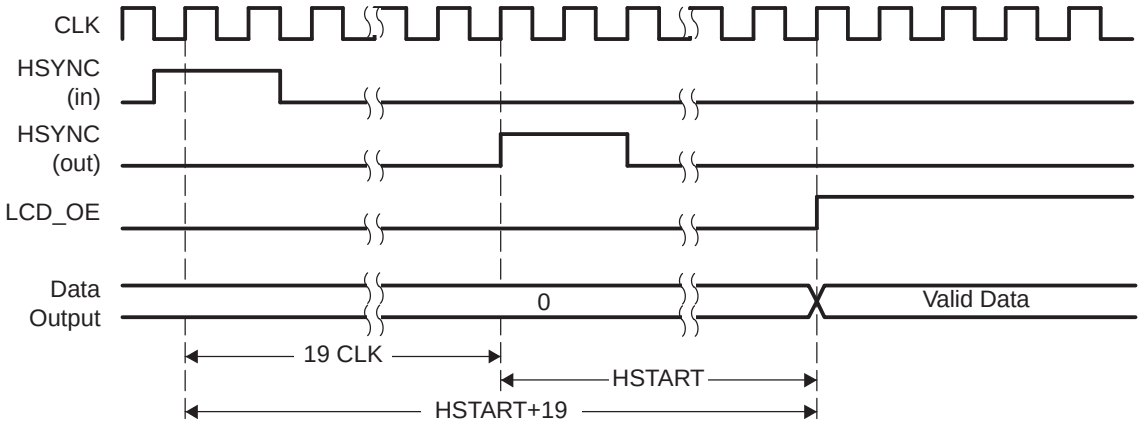


4.5.4.3.2 Horizontal Timing

Figure 63 shows the slave mode horizontal timing chart. It takes 19 CLKs for HSYNC output to be asserted after the external HSYNC input is latched. The data start position from HSYNC output is not different from master mode. However, HSYNC output cannot be seen from the outside chip because HSYNC pin is shared with input for slave and output for master. The HSYNC output timing in Figure 63 is for reference.

This horizontal timing is always applied, regardless of video timing mode (VMOD.VMD).

Figure 63. Horizontal Timing Chart



4.5.4.3.3 Vertical Timings

Figure 65 shows the vertical timing chart of NTSC slave mode. Vertical timing is reset when VSYNC rise transition is detected at HSYNC rising edge or the center of line (0.5H). Figure 66 indicates the PAL slave mode. Please note that the field is oppositely detected in PAL. In vertical timing chart of slave mode, output timings of HSYNC, VSYNC and VSYNC pins are denoted but these cannot be seen from outside the chip because they are used as input in slave mode.

If VSYNC is behind HSYNC assertion, vertical reset is suspended until the next HSYNC rise edge. Figure 64 shows various VSYNC detection timings.

Figure 64. VSYNC Input Latch Timing

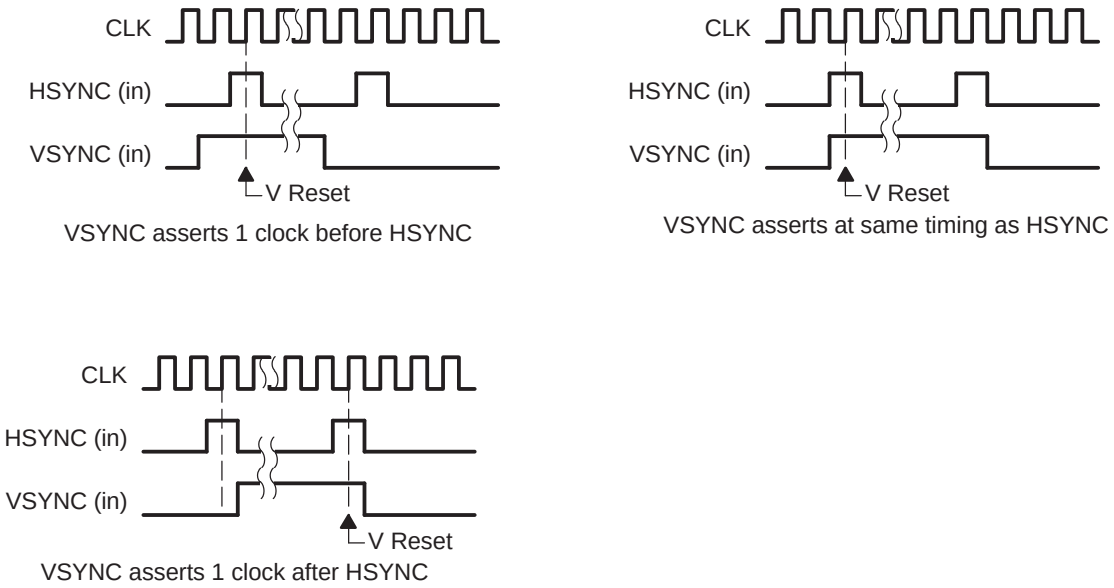


Figure 65. Vertical Timing Chart (NTSC)

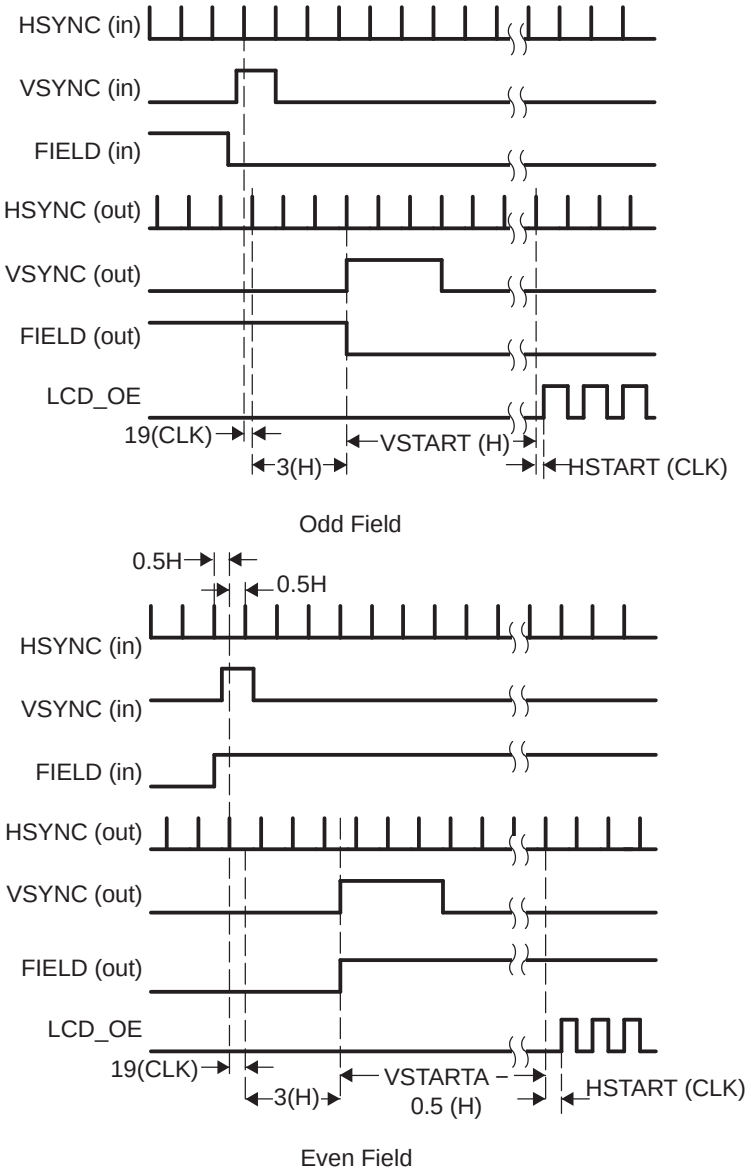


Figure 66. Vertical Timing Chart (PAL)

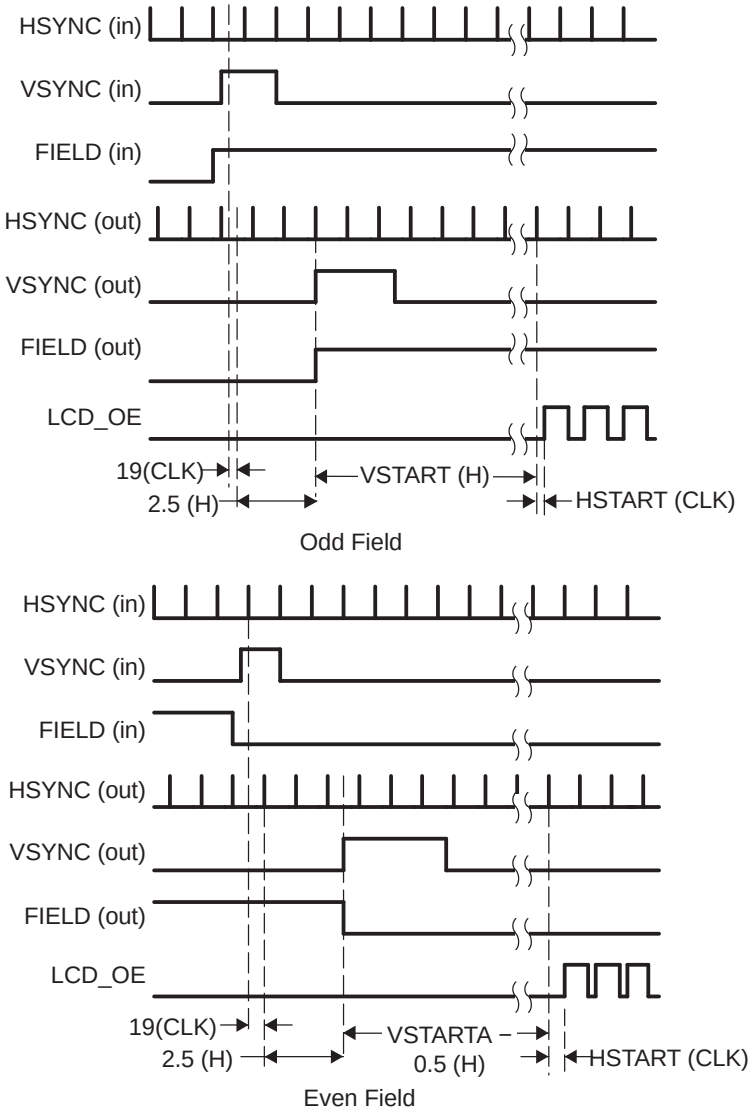


Figure 67 shows the vertical timing char of slave non-standard progressive mode (VMD=1, NSIT=0). Figure 68 indicates the nonstandard interlace timing (VMD=1, NSIT=1). Vertical timing is reset when VSYNC rise transition is detected at HSYNC rising edge. Please note that interlace mode vertical timing is reset only when VSYNC rise transition is detected at HSYNC rising edge (not at the center of line (0.5H) as in NTSC/PAL).

Figure 67. Vertical Timing Chart (Nonstandard/Progressive)

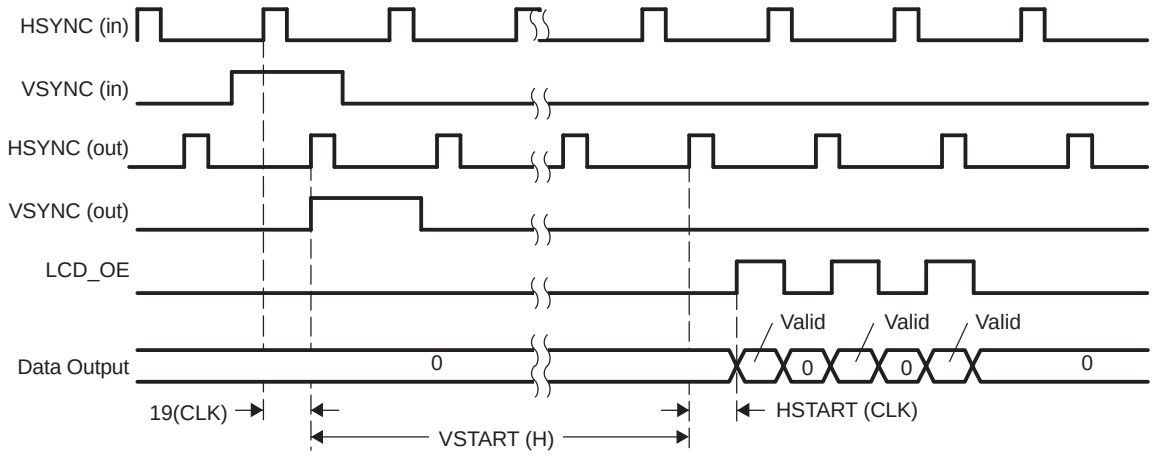
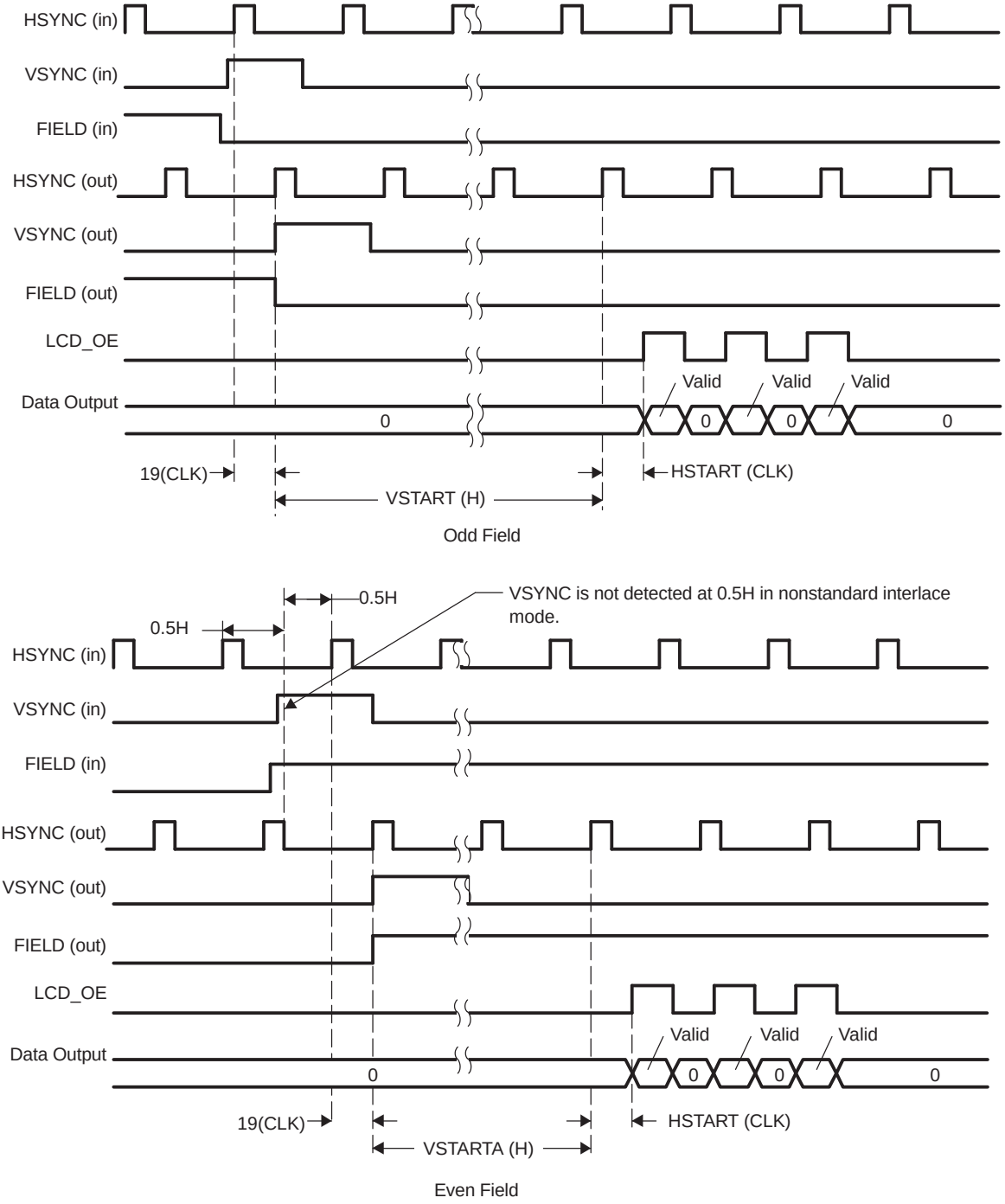


Figure 68. Vertical Timing Chart (Nonstandard/Interlace)



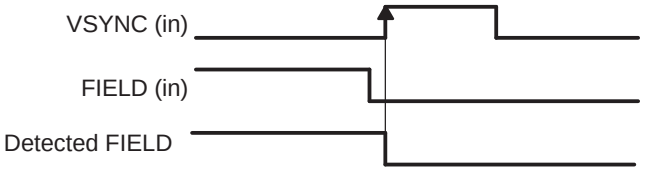
4.5.4.3.4 Slave Mode Field Detection

For slave interlace mode, namely when NTSC/PAL (VMD = 0 and HDMD = 0) or non-standard interlace (VMD = 1 and NSIT = 1), external field ID is detected. There are four field detection modes:

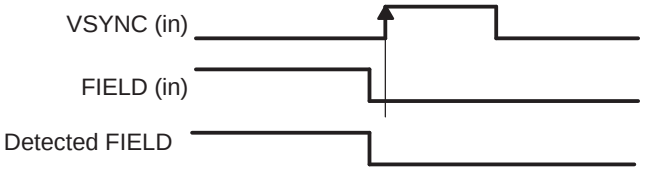
- Latch FIELD input at VSYNC rise edge
- Use raw FIELD input
- Use VSYNC input as FIELD
- Detect VSYNC phase

These four modes can be selected by SYNCCTL.EXFMD. Figure 69 shows the timing of each mode.

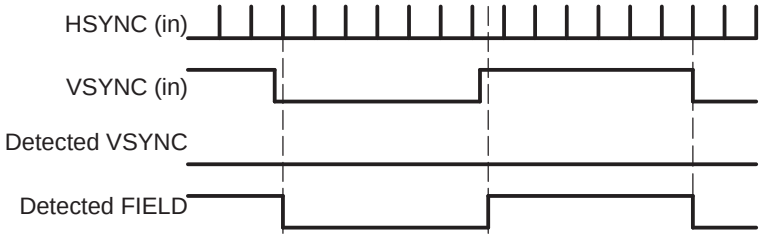
Figure 69. Field Detection Mode



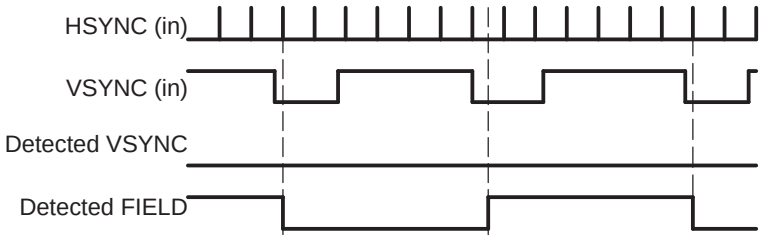
(1) Latch FIELD input at VSYNC rise edge



(2) Use raw FIELD input



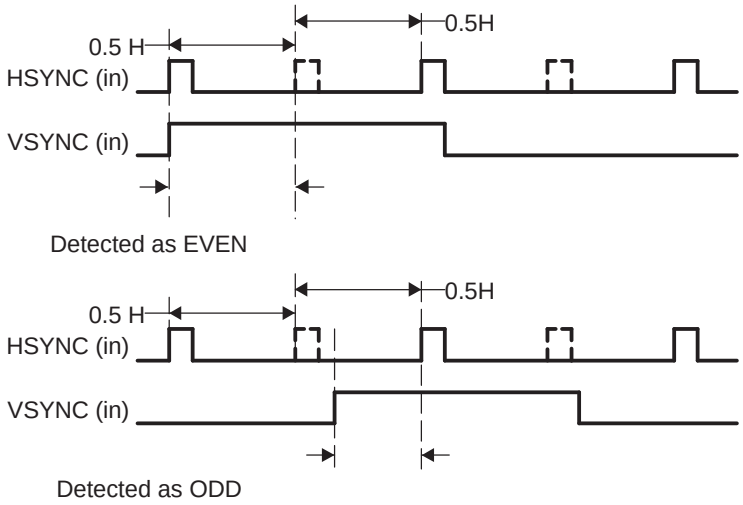
(3) Use VSYNC input as FIELD



(4) Detect VSYNC phase

In the option 4 (Detect VSYNC phase), the timing generator detects VSYNC assertion position in a line. When VSYNC is in the first half of a line, the field is detected as even. When VSYNC is the second half of a line, the field is detected as odd. Figure 70 shows this detection scheme. This mode is only available for NTSC/PAL. When in non-standard mode, Field_id is always detected as odd in option 4.

Figure 70. Field Detection by VSYNC Phase



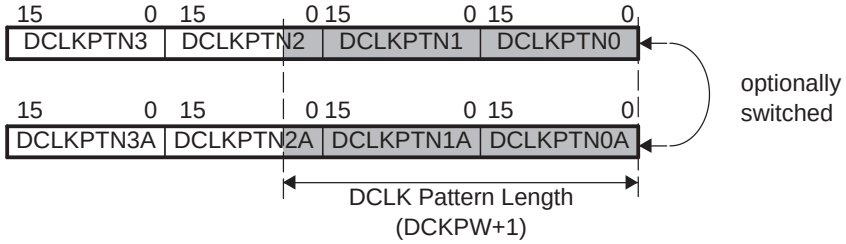
4.5.4.4 DCLK Generator

The LCD controller can generate a dot clock, called DCLK, that is fed to LCD panels. The generated DCLK is output from the VCLK pin. Frequency, waveform, and valid duration of the DCLK is programmed by register settings with various options. The digital data is output synchronized to the rising edge of DCLK.

4.5.4.4.1 Pattern Register

The DCLKPTN register is provided for DCLK waveform configuration. The user can configure various waveforms for DCLK within and up to a 64-cycle period. The register is 64 bits in length, mapped onto four 16-bit registers (DCLKPTN0-3). The effective pattern length can be specified in DCLKCTL.DCKPW. Moreover, another set of pattern registers with same structure (DCLKPTN0-3A) is optionally provided. This enables the user to switch the waveform on certain lines. Figure 71 shows the DCLK pattern register configuration scheme.

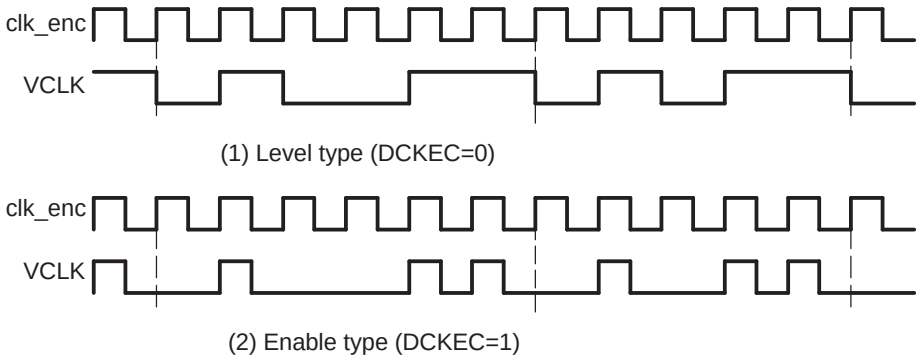
Figure 71. Pattern Register Configuration



There are two types of clock waveform configurations. They can be selected by DCLKCTL.DCKEC. For an example, see Figure 72.

- When DCKEC = 0, the pattern register becomes the clock level pattern of DCLK itself (Level mode).
- When DCKEC = 1, the pattern register works as the clock enable of the ENC clock (Enable mode).

Figure 72. DCLK Pattern Mode



Notes: DCKPW=5
DCLKPTN0=0013h

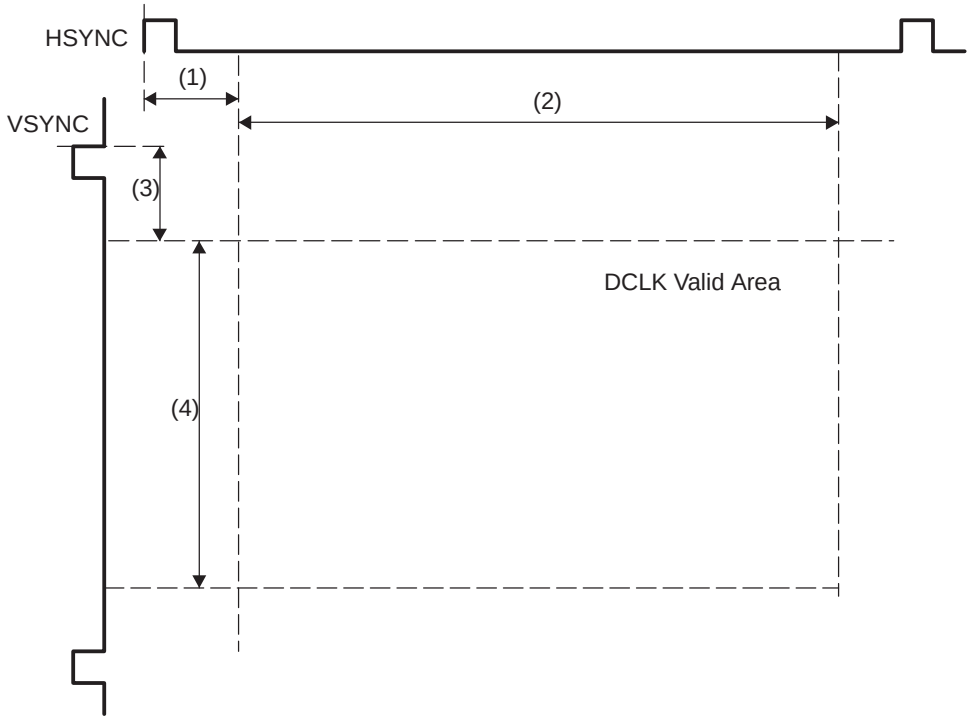
4.5.4.4.2 Masking

It is possible to mask the DCLK signal in horizontal and vertical directions. The registers listed in Table 76 allow you to set when DCLK is valid in the horizontal and vertical start positions of LCD display data. As shown in Figure 73, the valid start position in the horizontal direction is set relative to HSYNC, and the length of valid data in the horizontal position is set relative to the horizontal start position of valid data. The horizontal resolution is in ENC clocks. Figure 73 shows that valid data in the vertical direction is configured similar to valid data in the horizontal direction. DCLKCTL.DCKME can activate DCLK masking. Regarding horizontal start position, two sets of registers are provided as well as a pattern register.

Table 76. DCLK Masking Registers

Mark	Register	Description	Unit
1	DCLKHS.DCHS DCLKHSA.DCHS	Horizontal DCLK mask start position.	CLK
2	DCLKHR.DCHR	Horizontal DCLK mask range.	CLK
3	DCLKVS.DCVS	Vertical DCLK mask start position.	H
4	DCLKVR.DCVR	Vertical DCLK mask range.	H

Figure 73. DCLK Masking



4.5.4.4.3 Half-Rate Mode

It is possible to divide the DCLK by two. The dividing can be applied to the internal DCLK or the output DCLK. When DCLKCTL.DCKOH is 1, only the DCLK output is divided by two. Since the internal DCLK is not divided, the RGB data rate is not changed. Therefore, this mode can be used to connect to the LCD that captures the data using both edges of DCLK. On the other hand, when DCLKCTL.DCKIH is 1, the internal DCLK is divided by two. When output dividing is not enabled, two clocks can be output per one data sample. Therefore, this mode can be used to connect to the LCD that requires data at a rate of double the clock frequency.

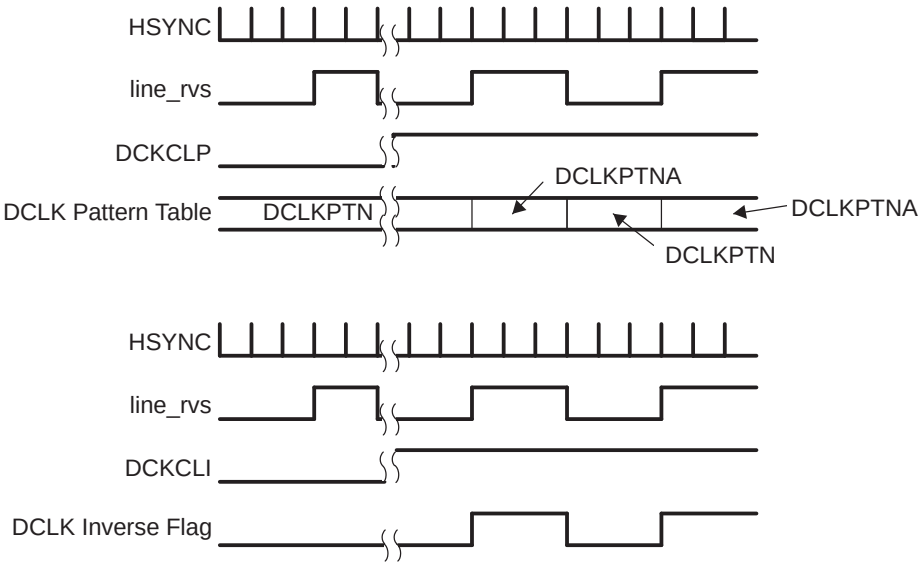
4.5.4.4.4 Line Control

The DCLK controller provides two kinds of DCLK waveform alteration by line. The culling line ID that controls RGB data output sequence also affects DCLK waveform alteration. Figure 74 shows this functionality.

- DCLK Pattern Switching. When LINECTL.DCKCLP = 1, DCLK pattern can be switched according to the culling line ID. The DCLK pattern on each line is specified by the DCLKPTN and DCLKPTNA registers.
- DCLK Polarity Inversion. When LINECTL.DCKCLI = 1, DCLK polarity is inverted on the line whose line ID is the culling line ID set by the CULLLINE register.

Both DCKCLP and DCKCLI can be set to 1, simultaneously.

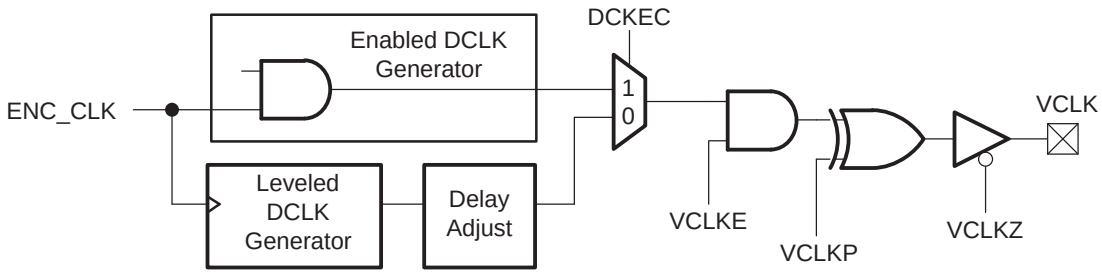
Figure 74. DCLK Pattern Switch/Inversion by Line



4.5.4.4.5 DCLK Output

VCLK output attributes, such as output enable, polarity and clock output on/off, can be controlled by registers in VIDCTL. Moreover, the level type DCLK output can have the offset of-0.5, 0.5 or 1.0 ENC CLK as set by DCLKCTL.DOFST. Figure 75 shows the DCLK output block diagram.

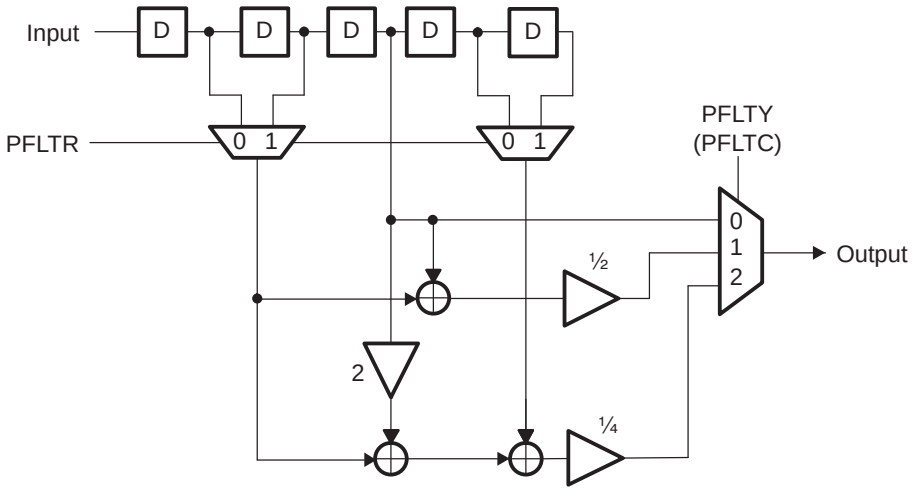
Figure 75. DCLK Output



4.5.4.5 YCbCr Pre-Filter

The video encoder inputs data from the OSD module in YCbCr format. A YCbCr filter (Figure 76) resides in the beginning of the data path. Each component (Y, Cb and Cr) has its own filter. The filter length can be programmed to 2 or 3 taps by PFLTY/PFLTC for Y/C, respectively, in the VDPRO register. The pre-filter sampling rate can be chosen to be either VENC clock or 1/2 VENC clock by VDPRO.PFLTR.

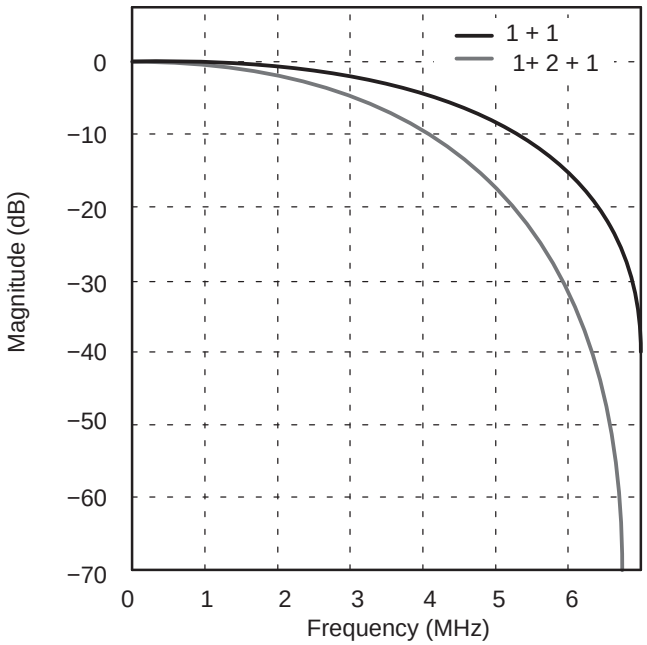
Figure 76. YCbCr Pre-Filter



The pre-filter frequency response with the sampling rate of 13.5 MHZ is shown in Figure 77.

The group delay of the filter is 1 when PFLTY/PFLTC = 0 or 2, and 0.5 for PFLTY/PFLTC = 1. Do not set PFLTY and PFLTC to different values or Y and C will not be aligned.

Figure 77. Frequency Response of the Pre-Filter



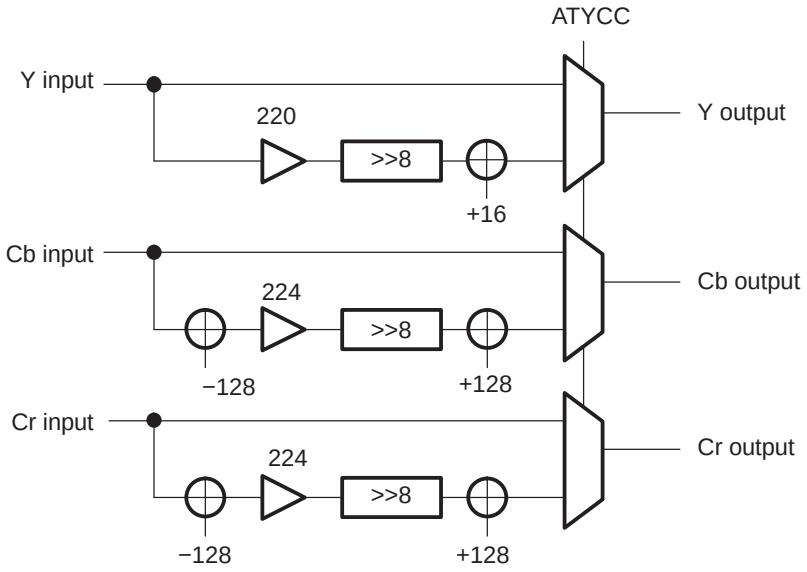
4.5.4.6 YCbCr Output Formatter

The YCbCr Output Formatter manages YCbCr data output in YUV16 and YUV8 modes.

4.5.4.6.1 YCbCr Conversion

YCbCr data processed by the pre-filter is then input to the YCbCr converter (Figure 78). This converter can attenuate the data with full range (0-255) levels to ITU-R BT.601 compliant levels (Y:16-235, C:16-240). The attenuation is enabled by setting VDPRO.ATYCC to 1.

Figure 78. YCbCr Conversion Block Diagram



4.5.4.6.2 16-Bit YCbCr Output Mode (YCC16)

In YCC16 mode, the Y (luma) signal is output to YOUT[7:0] at every VCLK rising edge, while Cb and Cr (chroma) are alternately multiplexed onto COUT[7:0]. For details of this output mode and the optional controls, see Section 2.2.1.

4.5.4.6.3 8-Bit YCbCr Output Mode (YCC8)

In YCC8 mode, each component of the OSD YCbCr signal is alternately output from YOUT[7:0]. For details of this output mode and the optional controls, see Section 2.2.2.

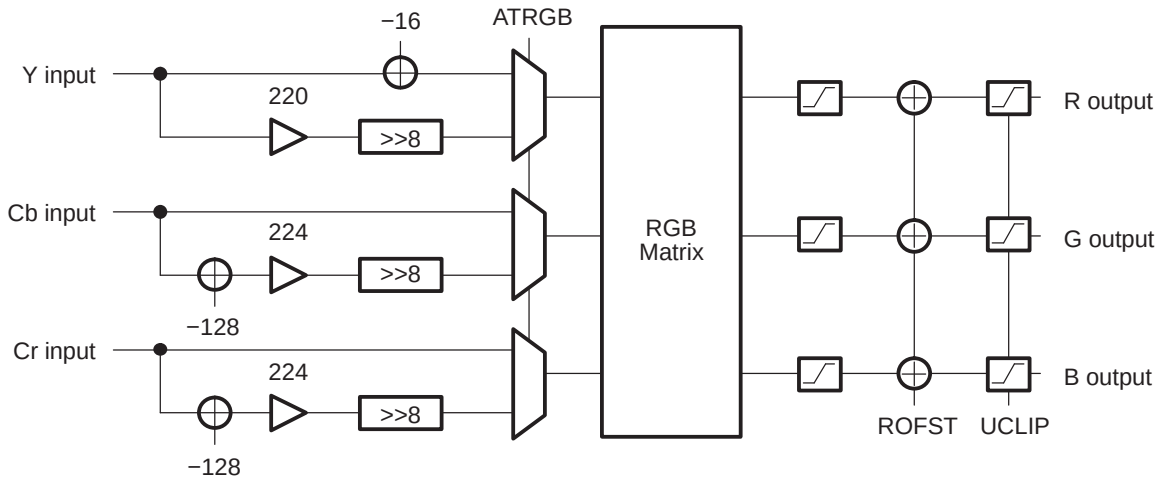
4.5.4.7 RGB Output Formatter

The RGB output formatter manages RGB data output in RGB parallel and serial modes.

4.5.4.7.1 RGB Conversion

Figure 79 shows the block diagram of the YCbCr to RGB converter. At the first stage, YCbCr input ranging from 0-255 can be attenuated to ITU-R BT601 levels (Y:0-219, C:-128-128). This is enabled by setting VDPRO.ATRGB = 1.

Figure 79. RGB Conversion Block Diagram



The formatted YCbCr data is then converted to RGB according to the following equation:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \frac{1}{1024} \begin{bmatrix} GY & 0 & RV \\ GY & -GU & -GV \\ GY & BU & 0 \end{bmatrix} \begin{bmatrix} Y-16 \\ Cb-128 \\ Cr-128 \end{bmatrix}$$

The coefficients of the matrix can be programmed by setting the DRGBX0-DRGBX4 registers with the appropriate coefficients. By default, these values are set to the ITU-R BT601 RGB conversion matrix. RGB ranging from 0 to 219 is possible from the REC.601 formatted signal (Y:16-235, C:16-240). Since the converted RGB may become negative due to finite precision arithmetic, zero level clipping is applied.

Then the offset specified by RGBCLP.OFST is added followed by upper level clipping. The clip level is set by RGBCLP.UCLIP. The output RGB samples are limited to 8-bit resolution.

4.5.4.7.2 RGB Filter

A low-pass filter can then be applied to the converted RGB data. There is a separate LPF module for each color component, each with 8-bit inputs and outputs. For each component, either a 3-tap or a 7-tap LPF can be selected via RGBCTL.DFLTS. The sampling clock can also be chosen from the VENC clock or its divided clock by RGBCTL.DFLTR. Even though there are separate filters that operate in parallel, the user does not have individual control so these settings apply to all components.

Note: When YCbCr output is selected VMOD.VDMD = 0 or 1, (YCC16 or YCC8 modes), the RGB filters should be disabled (DFLTS = 0).

4.5.4.7.3 Parallel RGB Mode (PRGB)

In parallel RGB mode, up to 18-bit resolution data (6-bits each for RGB) can be output. By default, RGB565 can be output using the dedicated YOUT[7:0]/COUT[7:0] signals. For additional details, see Section 2.2.3. RGB666 and RGB656 output modes can also be supported by assigning additional GPIO pins to the display interface. This assignment, done via the pin multiplexing, is controlled from the System module, described in Section 2.3.

4.5.4.7.4 Serial RGB Mode (SRGB)

For Serial RGB modes, the RGB data samples are output serially, multiplexed onto the YOUT bus. Output data is sub-sampled at DCLK rising edge when data valid signal (LCD_OE) is asserted, and output signals are held low when LCD_OE is deasserted. See Section 2.2.4 for additional details and options, including the IronMan interface protocol.

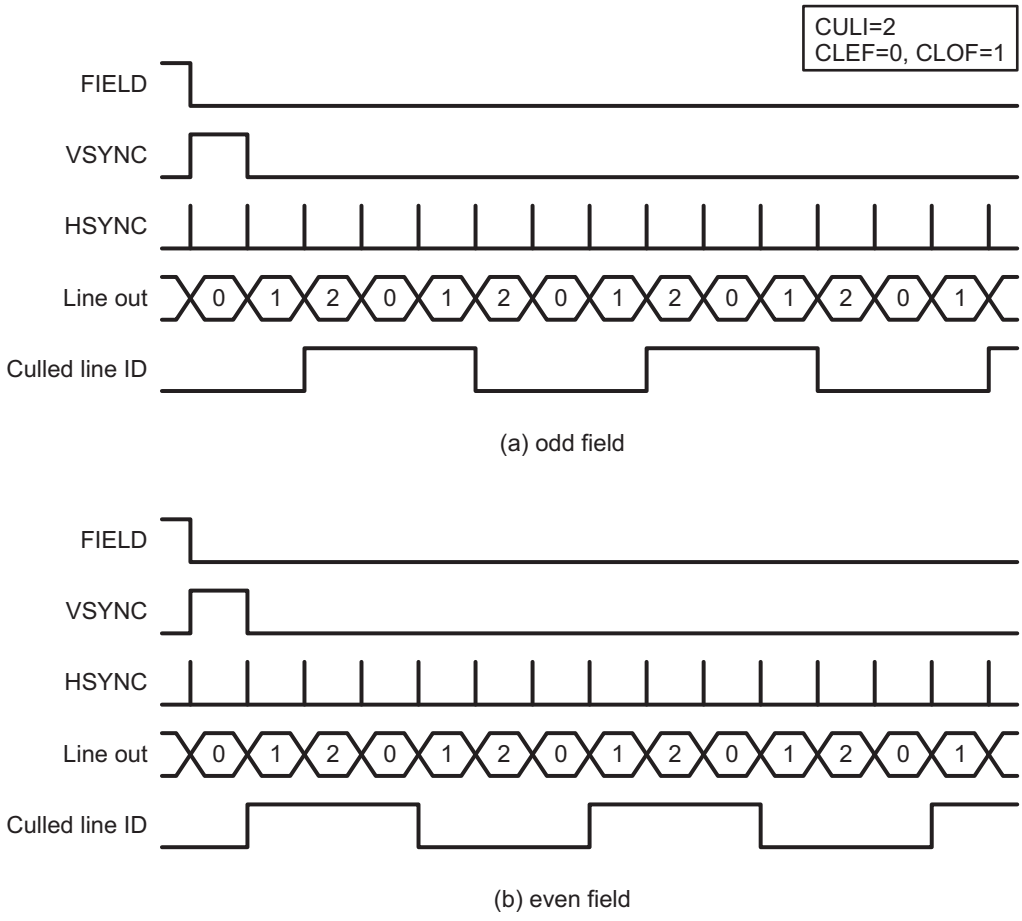
4.5.4.8 Line ID Control

Line ID is the line identification flag altered at HSYNC and reset by VSYNC. This flag is used for the RGB rotation order selector or DCLK waveform alteration. Normally, line ID is toggled at every HSYNC. In addition to this normal behavior, the LCD controller provides a culling line ID feature. This feature enables the use of the line ID toggled by a specified line interval. You can also set the line ID toggle position within the interval for even and odd field, respectively.

The generated culled line ID in Figure 80 affects the RGB rotation order when LINECTL.RGBCL = 1. In this mode, the XORed signal of the actual line ID and the culled line ID operates as the ID for the RGB rotation order.

In addition to RGB order, the DCLK waveform can be controlled by the culled line ID. When LINECTL.DCKCLP = 1, the effective DCLK pattern register (DCLKPTN) is switched by the culled line ID. The DCLKPTN is selected for culled line ID = 0 and DCLKPTNA for 1. As well as pattern switching, a DCLK inversion feature is also provided when LINECTL.DCKCLI = 1. In this mode, the created DCLK waveform is inverted for the culled line ID = 1.

Figure 80. Culled Line ID

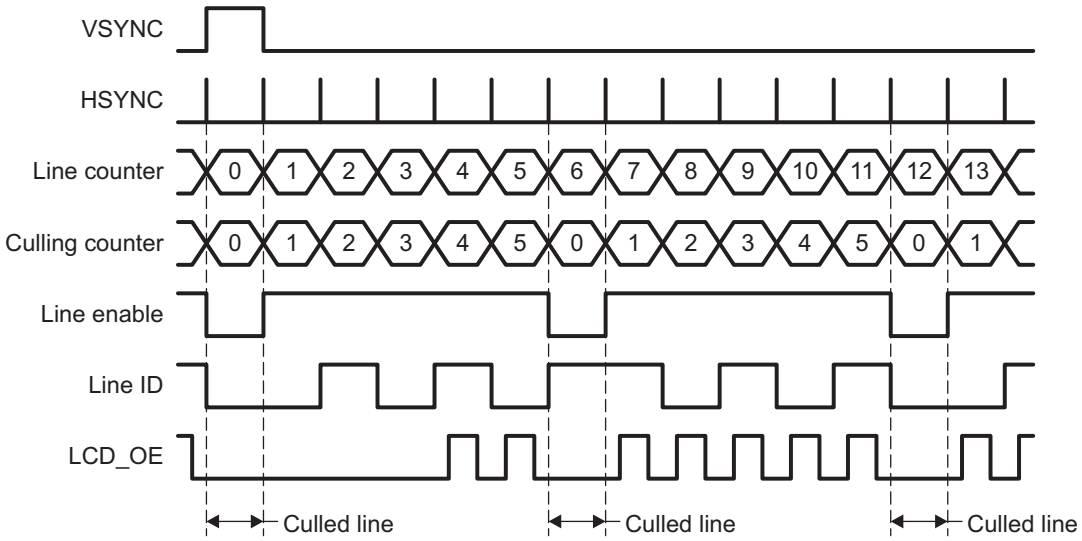


For PAL, the field is identified as odd when FIELD = 1.

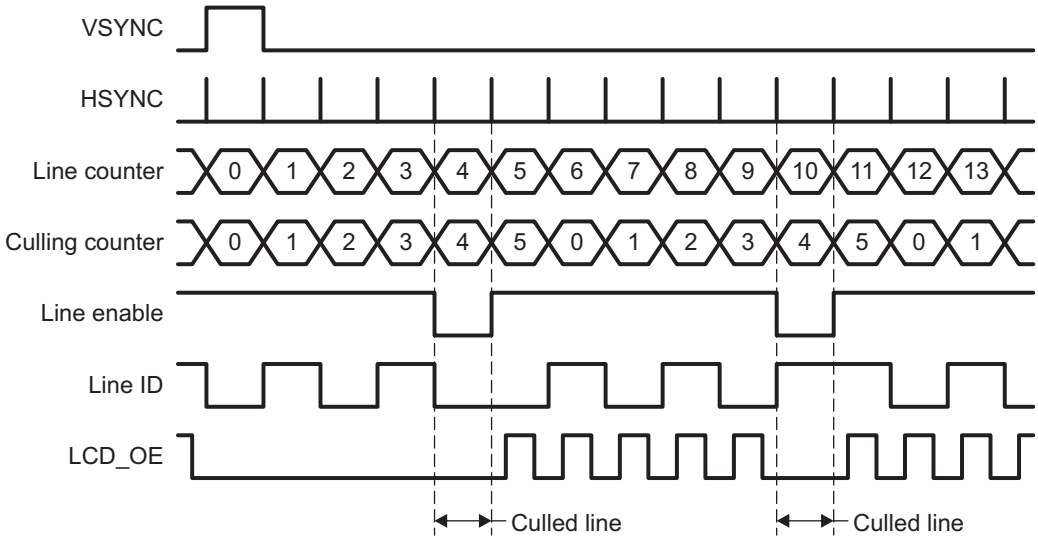
4.5.4.9 5/6 Line Culling

The digital video output can be vertically culled of 5/6. Setting LINECTL.VCL56 to 1 activates the culling. When in this mode, one line of video output is discarded every six lines. The VENC asserts the sync for the OSD and reads data from the OSD, but ignores it for output for the culled line. HSYNC output and LCD_OE assertion are also disabled in the culled line. The line position to be culled can be controlled by the VCLRD and VCLID bits in LINECTL. See Figure 81 and Figure 82 for details of the operation. Culling is enabled on the line where the internal culling counter (remove_counter) value is equal to the VCLID bit value. The internal culling counter is incremented at hsync and reset at vsync. The reset value can be 0 or a pseudo-random value that can be selected by the VCLRD bit.

Figure 81. 5/6 Line Culling Mode

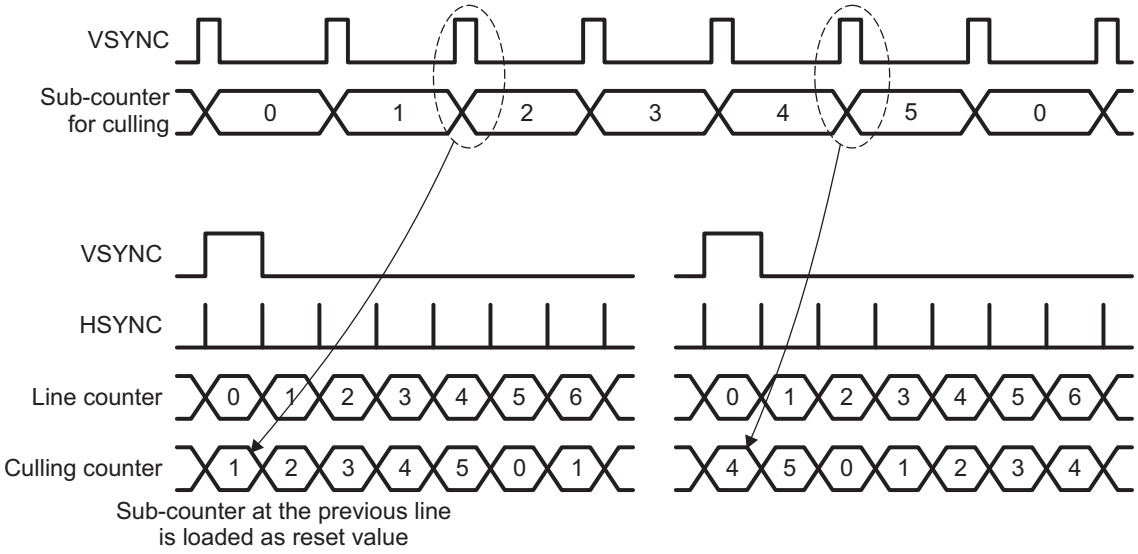


(1) VCLRD=0, VCLID=0, V_VALID=4



(2) VCLRD=0, VCLID=4, V_VALID=4

Figure 82. Random Reset of Vertical Culling Counter



4.5.4.10 Output Hold

The LCD controller provides a video output hold function. The controller can stop the operation of the timing generator when the current line or field transmission is completed. During the hold mode, reading data from the OSD is suspended and the output of the sync signals and video data is also suspended. The hold function is available only for digital video output in non-standard mode.

Setting the LINECTL.HLDL to 1 brings the controller into the line hold mode (Figure 83). Once HLDL is set, the controller automatically turns into the hold mode when the current line transmission is completed. Similarly, setting LINECTL.HLDF to 1 activates the field hold mode (Figure 84). After HLDF is set, the timing generator is suspended when the current field transmission is completed. Clearing these bits to 0 restarts the timing generator.

Figure 83. Output Line Hold Mode

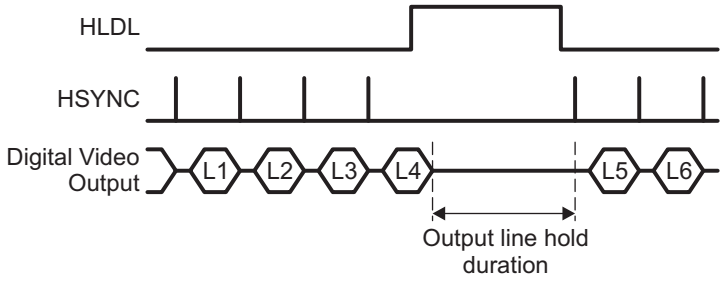
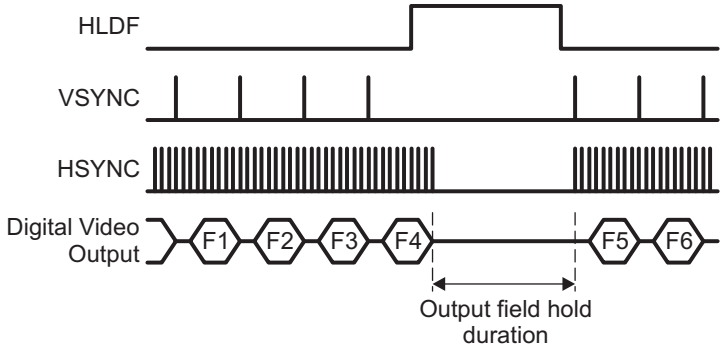


Figure 84. Output Field Hold Mode



4.5.4.11 LCD_OE Horizontal Culling

LCD_OE can be horizontally culled when HVLDCL0.HCM is 1. When in this mode, you can specify the culling period and valid pattern by HVLDCL0.HCPW and HVLDCL1.HCPT, respectively. Figure 85 shows the register usage for LCD_OE culling. Figure 86 shows an example of LCD_OE horizontal culling timing. In Figure 86, DCLK is set to be the same as CLK. Every third data is thrown away. Zero is transmitted during LCD_OE = 0.

Figure 85. LCD_OE Horizontal Culling Register

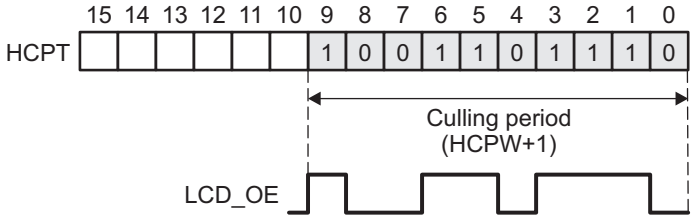
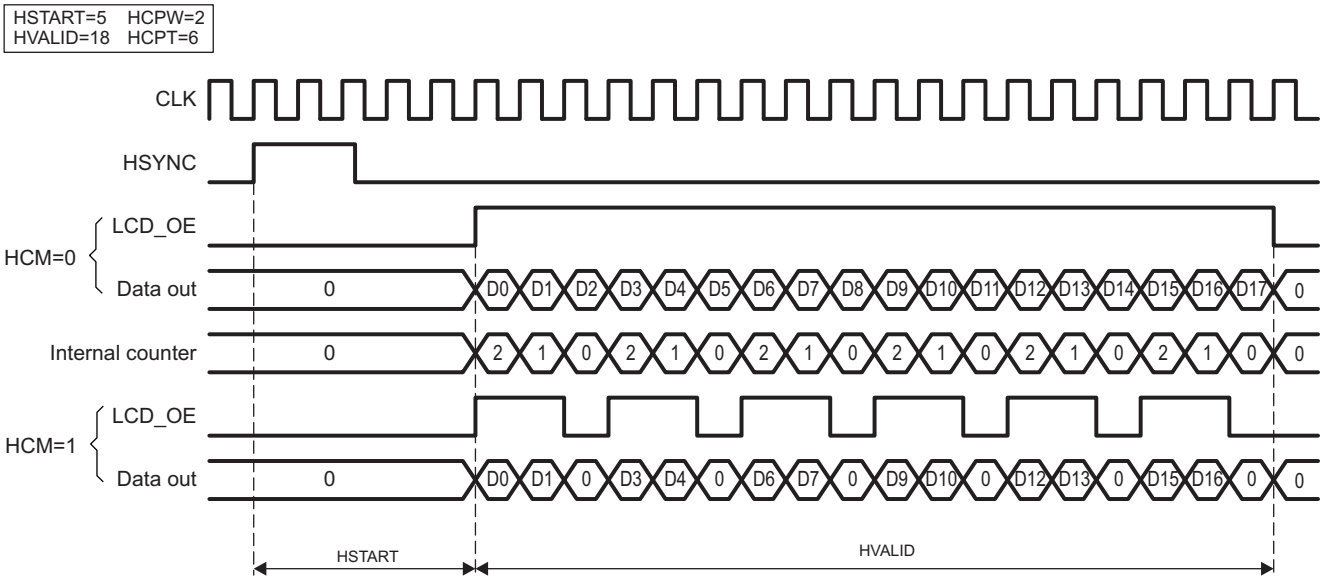


Figure 86. LCD_OE Horizontal Culling Timing Chart



4.5.5 Other Video Encoder Features

4.5.5.1 Internal Color Bar

The VENC can internally generate the color bar by itself. Setting VDPRO.CBAE = 1 enables the internal color bar generator. VDPRO.CBTY switches the saturation of the color bar (0 = 75%, 1 = 100%).

Table 77. Digital Output Value of Color Bar Generator

	100% (VDPRO.CBTYP = 1)			75% (VDPRO.CBTYP = 0)		
Color	**Y**	**Cb**	**Cr**	**Y**	**Cb**	**Cr**
Black	16	128	128	16	128	128

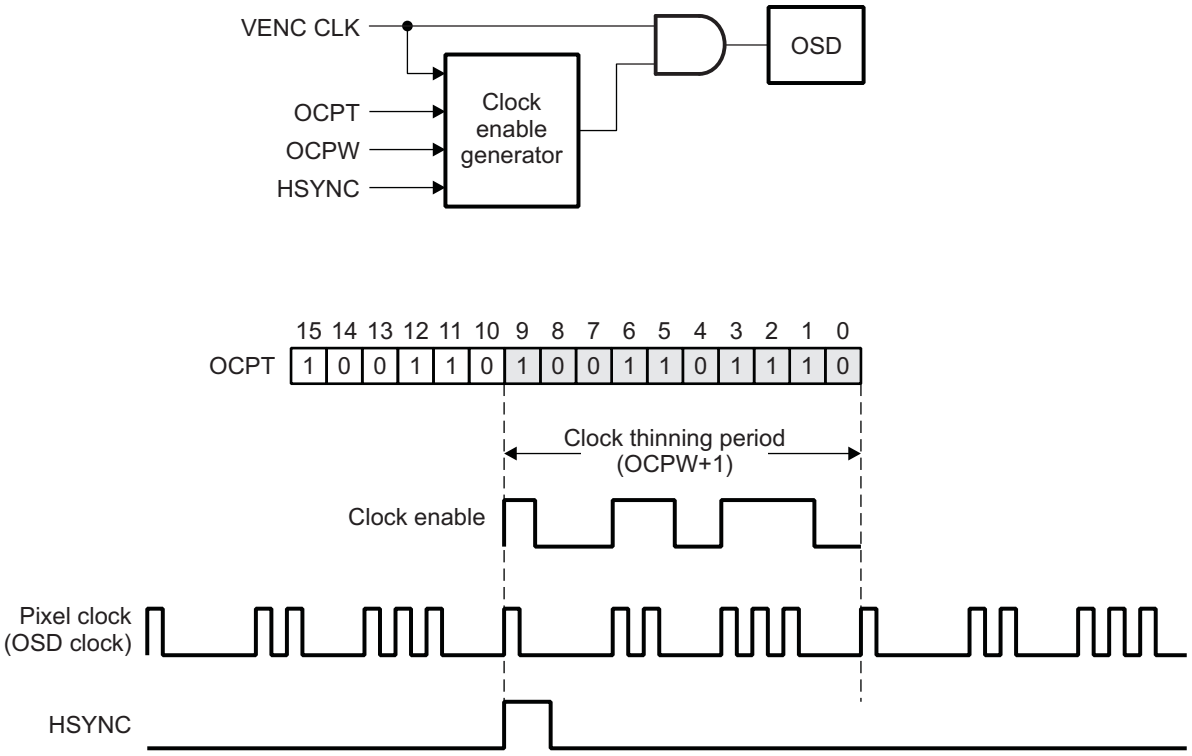
Table 77. Digital Output Value of Color Bar Generator (continued)

	100% (VDPRO.CBTYP = 1)			75% (VDPRO.CBTYP = 0)		
Color	**Y**	**Cb**	**Cr**	**Y**	**Cb**	**Cr**
Blue	41	240	110	35	212	114
Red	81	90	240	65	100	212
Magenta	106	202	222	84	184	198
Green	145	54	34	112	72	58
Cyan	170	166	16	131	156	44
Yellow	210	16	146	162	44	142
White	235	128	128	180	128	128

4.5.5.2 Pixel Clock Programming

You can arbitrarily thin out the pixel clock, which is the main clock used in the OSD module. Thinning out is processed periodically in the horizontal direction. During this period, you can freely program the active clock position. The period is specified by the OCPW bit in the OSD clock control 0 register (OSDCLK0) and the clock enable pattern is specified by the OCPT bit in the OSD clock control 1 register (OSDCLK1). The period of the clock gating pattern is started at HSYNC. Figure 87 shows the pixel clock thin out processing scheme.

Figure 87. Thinning Out Pixel Clock



After a reset, the OCPW bit is set to 1 and the OCPT bit is set to 2h so that the resulting pixel clock becomes half of VENC CLK (when VENC CLK is 27 MHz, the pixel clock becomes 13.5 MHz). For NTSC/PAL use, there is no change of these registers from the default value. It is required to clear the OCPW bit to 0 and set the OCPT bit to 1 for progressive scan output.

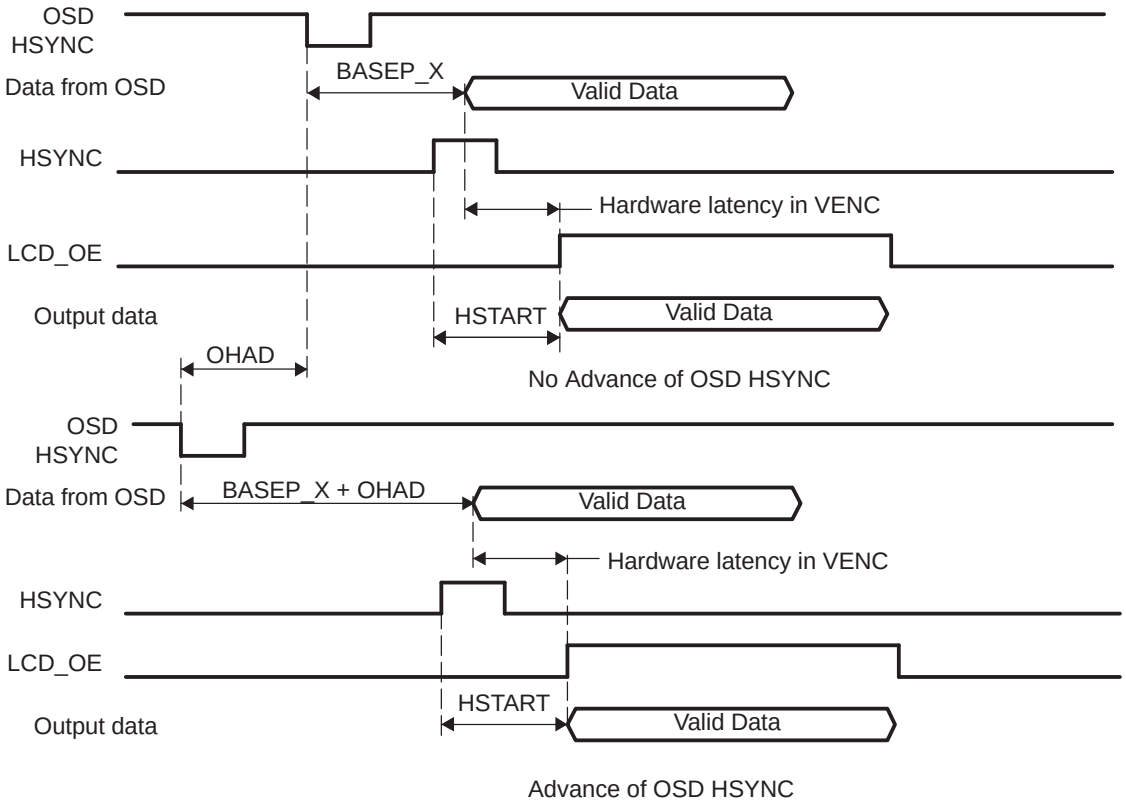
4.5.5.3 OSD Sync Control

4.5.5.3.1 Advanced Horizontal Sync

The VENC provides the sync signals to the OSD module. The horizontal sync timing is controlled by the VENC hardware so that the horizontal data start position is aligned between VENC and OSD when HSTART and BASEP_X (OSD register) have the same value (when OSD CLK is set to VENC CLK itself without gating). This horizontal sync timing can be advanced by OSDHADV.OHAD. The assertion timing can be 0 to 127 VENC CLK ahead of the original timing. This feature is useful when OSD does not have enough margin to prepare the first data in specified BASEP_X value due to SDRAM bandwidth limitation. In such a case, if the user advances the OSD horizontal sync, it will relax the latency for OSD to prepare the first data. Figure 88 shows the OSD horizontal sync advanced feature.

Note that OSD sync signals are low active.

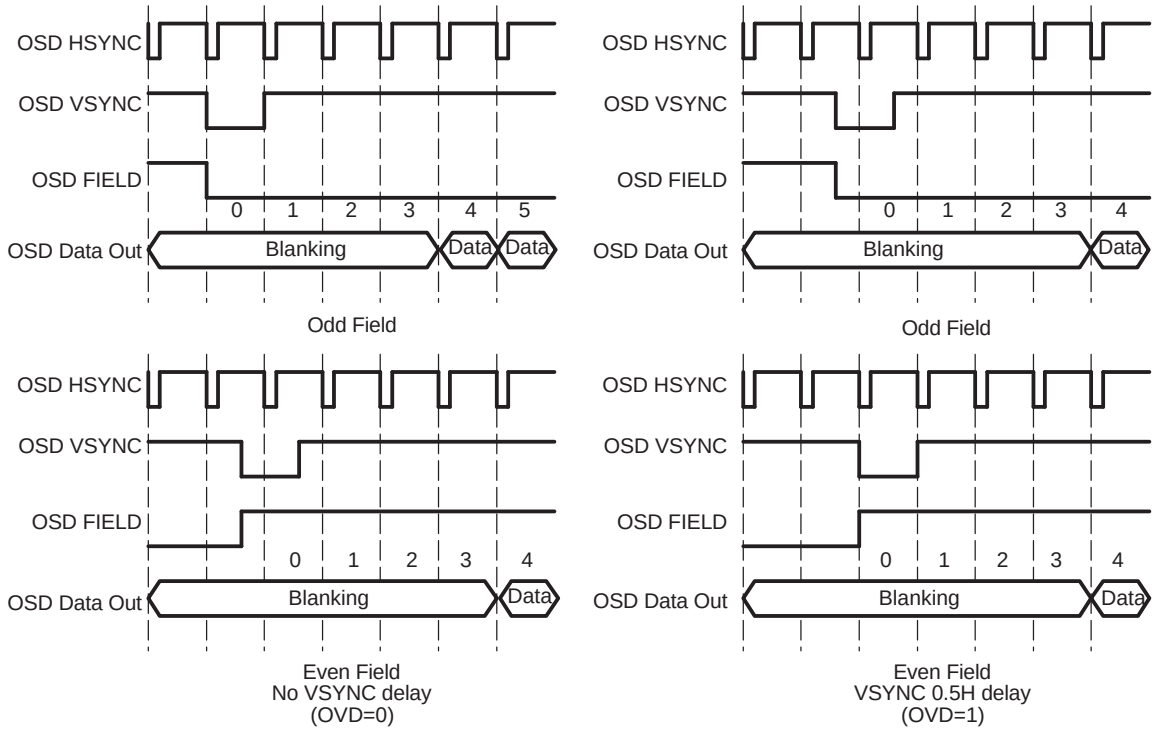
Figure 88. Advanced OSD HSYNC



4.5.5.3.2 0.5H Delay Vertical Sync

The vertical sync assertion for OSD can be delayed 0.5H by setting SYNCCTL.OVD to 1. This can modify the OSD data start line in odd field. The difference is shown in Figure 89. For PAL, OVD is automatically set to 1.

Figure 89. OSD VSYNC 0.5H Delay



4.5.5.4 Field ID Monitor

The current field ID status can be read from VSTAT.FIDST. The field status that can be seen from this bit is the field ID provided to the OSD module.

4.5.5.5 Interrupt

VENC asserts an interrupt at every VSYNC assertion. When the OSD module receives a vertical sync pulse from VENC, it updates its internal configuration registers. The interrupt assertion immediately follows this register update.

4.5.5.6 I/O Control

When VIDCTL.YCDC is 1, the specified level in YLVL, CLVL in the register, YCOLVL can be directly output onto YOUT and COUT pins. It is necessary to set the direction of YOUT and COUT to output by setting VIDCTL.YCDIR. YCDIR affects YOUT and COUT.

The direction of sync signals is controlled by SYNCCTL.SYDIR. This bit affects HSYNC, VSYNC and FIELD (if GIOx is configured as FIELD).

4.5.5.7 Gamma Correction

The video encoder includes 8-bit programable gamma correction located between the R/G/B Filter and output formatter. The gamma table consists of 256 x 8-bit values. The table address can be set by using the RAMADR register and the value can be set via the RAMPORT register. For example, if the RAMADR register is set to 0x0 and then 0x1234 is written to the RAMPORT register, the first table entry is set to 0x34 (LSB) and the second table entry is set to 0x12. The RAMPORT register is automatically incremented every time it is accessed.

When in parallel RGB or serial RGB mode, the gamma table is applied to each R,G,B color element. When in YCC16 or YCC8 mode, the gamma table is only applied to the Y signal.

Gamma correction can be enabled/disabled via the GAMCTL register. When gamma correction is enabled, the lookup value in the gamma table addressed by the signal level is output.

4.5.5.8 Clock Control

Individual clock enable/disable is provided for the gamma table, digital LCD controller, and analog video encoder in the CLKCTL register.

5 Programming Model

5.1 Setup for Typical Configuration

A typical configuration of the VPBE would be standard mode timing in master mode, which would support analog NTSC/PAL SDTV output via the integrated video DACs and also could support digital LCD display devices if they, in turn, supported standard mode timing.

5.2 Resetting the VPBE Subsystem

The entire VPSS subsystem (VPFE and VPBE) can be reset via the Power and Sleep Controller (PSC).

CAUTION

Do not reset the entire VPSS Master or VPSS Slave subsystem (VPFE and VPBE), via the Power Sleep Controller.

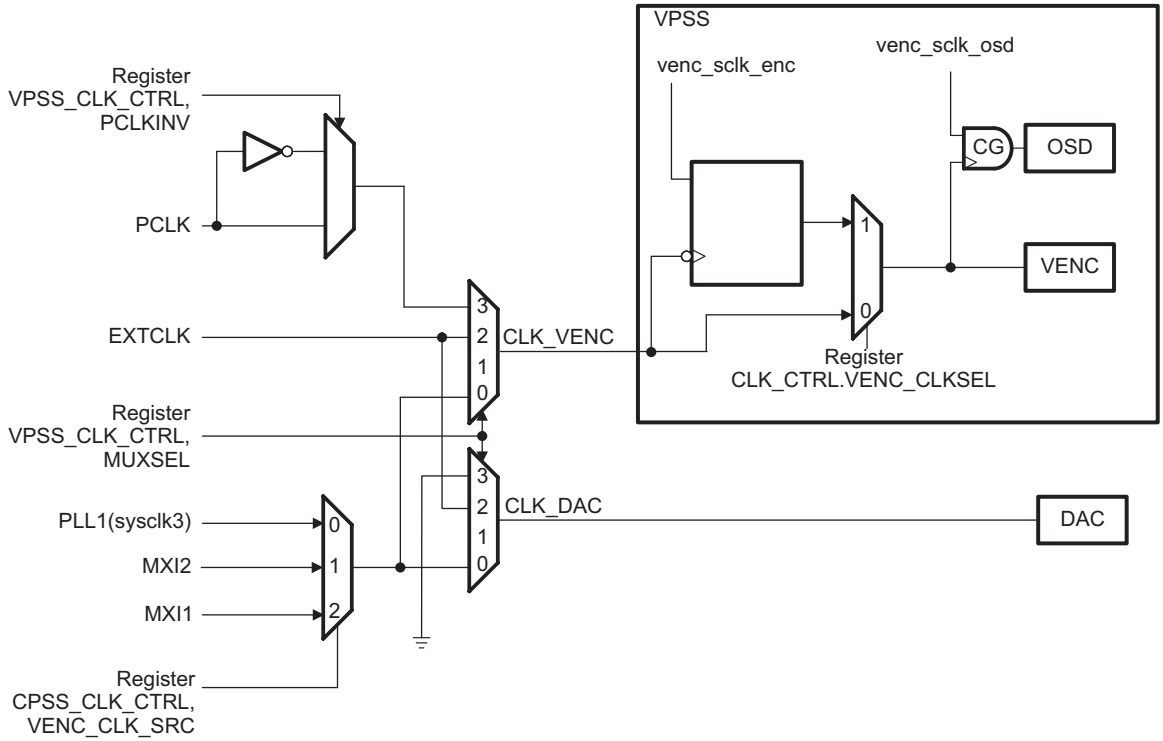
5.3 Configuring the Clocks and Control Signals

The VPBE/VENC clock must be configured for proper operation of the desired display mode. For more information, see Section 3.1.1. Also note that an external clock (VPBECLK) is required to support HDTV (720p/1080i) output rates of digital data suitable for driving a high-definition video encoder.

5.3.1 VPBE Clock Source Selection

The VBPE clock can be selected from five different sources. Note that MXI2 is powered off by default. Clear SYSTEM.USB_PHY_CTL.VPSS_OSCPDWN to power it on.

Figure 90. VPBE Clock Mux Block Diagram



5.4 Programming the On-Screen Display (OSD)

This section discusses issues related to the software control of the on-screen display (OSD) module. It lists registers that are required to be programmed in different modes and how to enable and disable OSD window displays. Additionally, it discusses the different register access types, and enumerates several programming constraints.

5.4.1 Hardware Setup/Initialization

This section discusses how the OSD must be configured before the module can be used. Also, note that the VENC module must also be configured before any display output is produced by the device.

5.4.1.1 Reset Behavior

Upon hardware reset of the VPSS, all of the registers in the OSD are initialized to their reset values. However, since the OSD RAM CLUT is stored in internal RAM, its content does not have reset values. After reset, the contents of these tables are unknown.

5.4.1.2 Hardware Setup

Prior to enabling the OSD, the hardware must be properly configured via register writes. Table 78 identifies the register parameters that must be programmed before enabling the OSD. Note that the default settings may be appropriate values so explicit register write may not be needed to all indicated registers/fields.

Table 78. OSD Hardware Setup

Function	Configuration Required	Description
Global Configuration	MODE.CS	CB/CY order
	MODE.FSINV	Field signal inverse
	MODE.VVRSZ	Video window vertical 9/8 resize
	MODE.VHRSZ	Video window horizontal 6/5 resize
	MODE.OVRSZ	Bitmap window vertical 9/8 resize
	MODE.OHRSZ	Bitmap window horizontal 6/5 resize
Background color	MODE.BCLUT	Background CLUT (ROM/RAM)
	MODE.CABG	Background color
OSD display frame	BASEPX	Base pixel X
	BASEPY	Base pixel Y
ROM CLUT	MISCCTL.RSEL	ROM CLUT selection
Transparency	TRANSPVALL.RGBL	RGB Transparency value (Low 16)
	TRANSPVALU.RGBU	RGB Transparency value (High 8)
	TRANSPVALU.Y	Luma Transparency
	TRANSPBMPIDX.BMP0	Bitmap Transparency (Window 0)
	TRANSPBMPIDX.BMP1	Bitmap Transparency (Window 1)

5.4.2 Color LookUp Table Setup

The user-defined RAM Color Look-Up Table (CLUT) must be programmed before it can be used. For additional details, see Section 4.4.4.1.

5.4.2.1 Window Setup

Before an individual window can be displayed, appropriate data must be made available in DDR2/mDDR, along with the appropriate window settings. The data formats are described above and the window configuration settings are described in Table 79.

Table 79. OSD Window Configuration

Function	Configuration Options
All Windows	Position offset relative to BASEPX/Y
	Window display size
	DDR2/mDDR data pointer
	DDR2/mDDR Offset (size in 32-byte increments of each data line)
	Field/Frame settings
	Horizontal/vertical Zoom factor
Video Windows	Expansion filter coefficient settings
Bitmap Windows	YUV attenuation enable
	RGB565 display mode (one window only)
	CLUT selection (ROM/RAM)
	Bitmap data width (1, 2, 4, or 8)
	CLUT mapping if bit depth < 8-bits
	Blend factor
	Transparency enable
	Transparent color value (global for RGB and YUV)
Attribute Window	Blinking (ON/OFF)
	Blink Rate

Table 79. OSD Window Configuration (continued)

Function	Configuration Options
Cursor Window	Size
	Thickness
	Color

5.4.3 Enable/Disable Hardware

The OSD has no separate hardware enable/disable but each window has a separate display enable/disable (see Table 80).

Table 80. OSD Window Enable/Disable

Window	Display Enable
Video Window 0	VIDWINMD.ACT0
Video Window 0	VIDWINMD.ACT1
Bitmap Window 0	OSDWIN0MD.OACT0
Bitmap Window 1	OSDWIN1MD.OACT1
Attribute Window	None – always active when in attribute mode
Cursor Window	RECTCUR.RCACT

5.4.4 Events and Status Checking

The VPBE generates a frame sync interrupt. This can be used as a trigger to update any frame-dependent registers. The OSD generates no events or status other than the indicator that a CLUT write is pending.

5.4.5 Register Accessibility During Frame Display

Some registers/fields are shadowed during the frame display time and any writes to these locations are not applied until the next frame field. These are highlighted in Table 81.

Table 81. OSD Window Registers/Field Shadowing

Register.Field	Description
MODE.CS	Cb/Cr or Cr/Cb Format
MODE.OVRSZ	OSD Window Vertical Expansion Enable
MODE.OHRSZ	OSD Window Horizontal Expansion Enable
MODE.EF(1)	Expansion Filter Enable
MODE.VVRSZ(1)	Video Window Vertical Expansion Enable
MODE.VHRSZ(1)	Video Window Horizontal Expansion Enable
MODE.FSINV(1)	Field Signal Inversion
MODE.BCLUT(1)	Background CLUT Selection
MODE.CABG	Background Color CLUT
VIDWINMD.VFINV	Video Window 0/1 Expansion Filter Coefficient Inverse
VIDWINMD.V1EFC	Video Window 1 Expansion Filter Coefficient
VIDWINMD.VHZ1(1)	Video Window 1 Horizontal Direction Zoom
VIDWINMD.VVZ1(1)	Video Window 1 Vertical Direction Zoom
VIDWINMD.VFF1(1)	Video Window 1 Display Mode
VIDWINMD.ACT1(1)	Sets Image Display On/Off Video Window 1
VIDWINMD.V0EFC	Video Window 0 Expansion Filter Coefficient
VIDWINMD.VHZ0(1)	Video Window 0 Horizontal Direction Zoom
VIDWINMD.VVZ0(1)	Video Window 0 Vertical Direction Zoom
VIDWINMD.VFF0(1)	Video Window 0 Display Mode
VIDWINMD.ACT0(1)	Sets Image Display On/Off Video Window 0
OSDWINOMD.BMPOMD	Bitmap Input Mode
OSDWIN0MD.CLUTS0(1)	CLUT Select for OSD Window 0
OSDWIN0MD.OHZ0(1)	OSD Window 0 Horizontal Zoom
OSDWIN0MD.OVZ0(1)	OSD Window 0 Vertical Zoom
OSDWIN0MD.BMW0(1)	Bitmap Bit Width for OSD Window 0
OSDWIN0MD.BLND0(1)	Blending Ratio for OSD Window 0
OSDWIN0MD.TE0(1)	Transparency Enable for OSD Window 0
OSDWIN0MD.OFF0(1)	OSD Window 0 Display Mode
OSDWIN0MD.OACT0(1)	OSD Window 0 Active (displayed)
OSDWIN1MD.OASW(1)	OSD Window 1 Attribute Mode Enable
OSDWIN1MD.BMP1MD	Bitmap Input Mode
OSDWIN1MD.CLUTS1	CLUT Select for OSD Window 1
OSDWIN1MD.OHZ1(1)	OSD Window 1 Horizontal Zoom
OSDWIN1MD.OVZ1(1)	OSD Window 1 Vertical Zoom
OSDWIN1MD.BMW1(1)	Bitmap Bit Width for OSD Window 1
OSDWIN1MD.BLND1(1)	Blending Ratio for OSD Window 1
OSDWIN1MD.TE1(1)	Transparency Enable for OSD Window 1
OSDWIN1MD.OFF1(1)	OSD Window 1 Display Mode
OSDWIN1MD.OACT1(1)	OSD Window 1 Active (displayed)
OSDATRMD.OASW(1)	OSD Window 1 Attribute Mode Enable
OSDATRMD.OHZA(1)	OSD Attribute Window Horizontal Zoom

(1) This register/field is shadowed during the frame display time and any writes to this location is not applied until the next frame field.

Table 81. OSD Window Registers/Field Shadowing (continued)

Register.Field	Description
OSDATRMD.OVZA(1)	OSD Attribute Window Vertical Zoom
OSDATRMD.BLNKINT(1)	Blinking Interval
OSDATRMD.OFFA(1)	OSD Attribute Window Display Mode
OSDATRMD.BLNK(1)	OSD Attribute Window Blink Enable
RECTCUR.RCAD	Rectangular Cursor Color Palette Address
RECTCUR.CLUTSR(1)	CLUT Select
RECTCUR.RCHW(1)	Rectangular Cursor Horizontal Line Width
RECTCUR.RCVW(1)	Rectangular Cursor Vertical Line Width
RECTCUR.RCACT(1)	Rectangular Cursor Active (displayed)
VIDWIN0OFST.V0LO(1)	Video Window 0 Line Offset
VIDWIN1OFST.V1LO(1)	Video Window 1 Line Offset
OSDWIN0OFST.O0LO(1)	OSD Window 0 Line Offset
OSDWIN1OFST.O1LO(1)	OSD Window 1 Line Offset
VIDWINADH.V1AH(1)	Video Window 1 SDRAM Source Address (High)
VIDWINADH.V0AH(1)	Video Window 0 SDRAM Source Address (High)
VIDWIN0ADL.VIDWIN0ADL(1)	Video Window 0 SDRAM Source Address (Low)
VIDWIN1ADL.VIDWIN1ADL(1)	Video Window 1 SDRAM Source Address (Low)
OSDWINADH.O1AH(1)	OSD Window 0 SDRAM Source Address (High)
OSDWINADH.O0AH(1)	OSD Window 1 SDRAM Source Address (High)
OSDWIN0ADL.OSDWIN0ADL(1)	OSD Window 0 SDRAM Source Address (Low)
OSDWIN1ADL.OSDWIN1ADL(1)	OSD Window 1 SDRAM Source Address (Low)
BASEPX.BPX(1)	Base Pixel in X
BASEPY.BPY(1)	Base Pixel(Line) in Y
VIDWIN0XP.V0X(1)	Video Window 0 X-Position
VIDWIN0YP.V0Y(1)	Video Window 0 Y-Position
VIDWIN0XL.V0W(1)	Video Window 0 X-Width
VIDWIN0YL.V0H(1)	Video Window 0 Y-Height
VIDWIN1XP.V1X(1)	Video Window 1 X-Position
VIDWIN1YP.V1Y(1)	Video Window 1 Y-Position
VIDWIN1XL.V1W(1)	Video Window 1 X-Width
VIDWIN1YL.V1H(1)	Video Window 1 Y-Height
OSDWIN0XP.W0X(1)	OSD Window 0 X-Position
OSDWIN0YP.W0Y(1)	OSD Window 0 Y-Position
OSDWIN0XL.W0W(1)	OSD Window 0 X-Width
OSDWIN0YL.W0H(1)	OSD Window 0 Y-Height
OSDWIN1XP.W1X(1)	OSD Window 1 X-Position
OSDWIN1YP.W1Y(1)	OSD Window 1 Y-Position
OSDWIN1XL.W1W(1)	OSD Window 1 X-Width
OSDWIN1YL.W1H(1)	OSD Window 1 Y-Height
CURXP.RCSX(1)	Rectangular Cursor Window X-Position
CURYP.RCSY(1)	Rectangular Cursor Window Y-Position
CURXL.RCSW(1)	Rectangular Cursor Window X-Width
CURYL.RCSH(1)	Rectangular Cursor Window Y-Height
W0BMP01.PAL01	Palette Address for Bitmap Value [1,x,x]-OSD Window 0
W0BMP01.PAL00	Palette Address for Bitmap Value [0,0,0]-OSD Window 0
W0BMP23.PAL03	Palette Address for Bitmap Value [3,x,x]-OSD Window 0

Table 81. OSD Window Registers/Field Shadowing (continued)

Register.Field	Description
W0BMP23.PAL02	Palette Address for Bitmap Value [2,x,x]-OSD Window 0
W0BMP45.PAL05	Palette Address for Bitmap Value [5,1,x]-OSD Window 0
W0BMP45.PAL04	Palette Address for Bitmap Value [4,x,x]-OSD Window 0
W0BMP67.PAL07	Palette Address for Bitmap Value [7,x,x]-OSD Window 0
W0BMP67.PAL06	Palette Address for Bitmap Value [6,x,x]-OSD Window 0
W0BMP89.PAL09	Palette Address for Bitmap Value [9,x,x]-OSD Window 0
W0BMP89.PAL08	Palette Address for Bitmap Value [8,x,x]-OSD Window 0
W0BMPAB.PAL11	Palette Address for Bitmap Value [B,x,x]-OSD Window 0
W0BMPAB.PAL10	Palette Address for Bitmap Value [A,2,x]-OSD Window 0
W0BMPCD.PAL13	Palette Address for Bitmap Value [D,x,x]-OSD Window 0
W0BMPCD.PAL12	Palette Address for Bitmap Value [C,x,x]-OSD Window 0
W0BMPEF.PAL15	Palette Address for Bitmap Value [F,3,1]-OSD Window 0
W0BMPEF.PAL14	Palette Address for Bitmap Value [E,x,x]-OSD Window 0
W1BMP01.PAL01	Palette Address for Bitmap Value [1,x,x]-OSD Window 1
W1BMP01.PAL00	Palette Address for Bitmap Value [0,0,0]-OSD Window 1
W1BMP23.PAL03	Palette Address for Bitmap Value [3,x,x]-OSD Window 1
W1BMP23.PAL02	Palette Address for Bitmap Value [2,x,x]-OSD Window 1
W1BMP45.PAL05	Palette Address for Bitmap Value [5,1,x]-OSD Window 1
W1BMP45.PAL04	Palette Address for Bitmap Value [4,x,x]-OSD Window 1
W1BMP67.PAL07	Palette Address for Bitmap Value [7,x,x]-OSD Window 1
W1BMP67.PAL06	Palette Address for Bitmap Value [6,x,x]-OSD Window 1
W1BMP89.PAL09	Palette Address for Bitmap Value [9,x,x]-OSD Window 1
W1BMP89.PAL08	Palette Address for Bitmap Value [8,x,x]-OSD Window 1
W1BMPAB.PAL11	Palette Address for Bitmap Value [B,x,x]-OSD Window 1
W1BMPAB.PAL10	Palette Address for Bitmap Value [A,2,x]-OSD Window 1
W1BMPCD.PAL13	Palette Address for Bitmap Value [D,x,x]-OSD Window 1
W1BMPCD.PAL12	Palette Address for Bitmap Value [C,x,x]-OSD Window 1
W1BMPEF.PAL15	Palette Address for Bitmap Value [F,3,1]-OSD Window 1
W1BMPEF.PAL14	Palette Address for Bitmap Value [E,x,x]-OSD Window 1
VBNDRY.VFILINCMD	Vertical Filter Increment Mode
VBNDRY.VDNDRYPRCSEN	Video Boundary Processing Enable
EXTMODE.EXPMDSEL	Expansion Filtering Mode Select
EXTMODE.SCRNHEXP	Horizontal Expansion Mode
EXTMODE.SCRNVEXP	Vertical Expansion Mode
EXTMODE.OSD1BLDCHR	OSD Bitmap1 Blend Characteristics
EXTMODE.OSD0BLDCHR	OSD Bitmap0 Blend Characteristics
EXTMODE.ATNOSD1EN	Attenuation Enable for REC601 for OSD Bitmap 1
EXTMODE.ATNOSD0EN	Attenuation Enable for REC601 for OSD Bitmap 0
EXTMODE.OSDHRSZ15	OSD Bitmap Window Horizontal 1.5x Expansion
EXTMODE.VIDHRSZ15	OSD Video Window Horizontal 1.5x Expansion
EXTMODE.ZMFILV1HEN	Video Window 1 Horizontal Zoom Filter
EXTMODE.ZMFILV1VEN	Video Window 1 Vertical Zoom Filter
EXTMODE.ZMFILV0HEN	Video Window 0 Horizontal Zoom Filter
EXTMODE.ZMFILV0VEN	Video Window 0 Vertical Zoom Filter
EXTMODE.EXPFILHEN	Horizontal Expansion Filter Enable
EXTMODE.EXPFILVEN	Vertical Expansion Filter Enable

Table 81. OSD Window Registers/Field Shadowing (continued)

Register.Field	Description
MISCCTL.FIELD_ID	Indicates field being processed
MISCCTL.DMANG	DMA Status
MISCCTL.RSEL	CLUT ROM Selection
MISCCTL.CPBSY	CLUT Write Busy
RSV5.RSV5	Reserved
CLUTRAMYCB.Y	Write Data (Y) Into Built-In CLUT RAM
CLUTRAMYCB.CB	Write Data (Cb) Into Built-In CLUT RAM
CLUTRAMCR.CR	Write Data (Cr) Into Built-In CLUT RAM
CLUTRAMCR.CADDR	CLUT Write Pallette Address
TRANSPVALL.RGBL	RGB Transparency Value (Low)
TRANSPVALU.Y	Luma Transparency Value
TRANSPVALU.RGBH	RGB Transparency Value (High)
TRANSPBMPIDX.BMP1	OSD Bitmap Window 1 Transparent Value
TRANSPBMPIDX.BMP0	OSD Bitmap Window 0 Transparent Value

5.4.6 Summary of Constraints

The following restrictions exist in the OSD module.

- If the vertical resize filter is enabled for either of the video windows, the maximum horizontal window dimension cannot be greater than 720 currently. This is due to the limitation in the size of the line memory.
- It is not possible to use both of the CLUT ROMs at the same time. However, a window can use RAM while another chooses ROM.

5.5 Programming the VENC

This section discusses issues related to the software control of the Video Encoder/Digital LCD Controller module (VENC). It lists registers that are required to be programmed in different modes and how to enable and disable the VENC. It also discusses the different register access types and enumerates several programming constraints.

5.5.1 Hardware Setup/Initialization

This section discusses the configuration of the VENC required before the module can be used. Also, the OSD module must be configured before any display output is produced by the device.

5.5.1.1 Reset Behavior

Upon hardware reset of the VPSS, all of the registers in the VENC are returned to their reset values. However, since the gamma table is stored in internal RAM, its content does not have reset values. If the reset is a chip-level power-on reset (reset after power is applied), then the contents of this table is unknown. If the reset is a VPSS module reset (when power remains active) then the contents of the Gamma RAM Table remains the same as before the reset

5.5.1.2 Hardware Setup

Prior to enabling the VENC, the hardware must be properly configured via register writes. Essentially all of the VENC programming is related to hardware setup and little to no interaction is required once the desired display operating condition is set. Table 82 shows which register/field affects the available display modes.

The analog output is only available in standard (NTSC/PAL) timing mode, but the digital outputs are available in either mode. Therefore, if the digital display device supports standard mode timing, the analog and digital outputs can be available simultaneously, if desired.

Table 82. VPBE Global Registers for Hardware Setup[1]

Register.Field	Description	Analog SDTV	YCC16	YCC8	Parallel RGB	Serial RGB
VMOD.VDMD	Digital Video Output Mode	Sets mode				
VMOD.ITLCL	Non-Interlace Line Number Select	O	O	O	O	O
VMOD.ITLC	Interlaced Scan Mode Enable	O	O	O	O	O
VMOD.NSIT	Nonstandard Interlace Mode		O	O	O	O
VMOD.TVTYP	TV Format Type Select	Sets mode				
VMOD.SLAVE	Master-Slave Select					
VMOD.VMD	Video Timing	Standard	Standard or Non-Standard			
VMOD.BLNK	Blanking Enable	O				
VMOD.VIE	Composite Analog Output Enable	O				
VMOD.VENC	Video Encoder Enable	R				
VIDCTL.VCLKP	VCLK Output Polarity		O	O	O	O
VIDCTL.VCLKE	VCLK Output Enable		R	R	R	R
VIDCTL.VCLKZ	VCLK Pin Output Enable		R	R	R	R
VIDCTL.SYDIR	Horizontal/Vertical Sync Pin I/O Control		Enable in Master mode			
VIDCTL.DOMD	Digital Data Output Mode		R	R	R	R
VIDCTL.YCSWAP	Swaps YOUT/COUT Pins		O	O		
VIDCTL.YCOL	YOUT/COUT Pin Output Level		O	O		
VIDCTL.YCOMD	YOUT/COUT Pin Output Mode (N/A)		N/A	N/A		
VIDCTL.YCDIR	YOUT/COUT Pin Direction (N/Z)		N/A	N/A		
VDPRO.PFLTC	C Prefilter Select		O	O		
VDPRO.PFLTY	Y Prefilter Select		O	O		
VDPRO.PFLTR	Prefilter Sampling Frequency		O	O		
VDPRO.CBTYP	Color Bar Type	O				
VDPRO.CBMD	Color Bar Mode	O				
VDPRO.ATRGB	Input Video Attenuation Control for RGB				O	O
VDPRO.ATYCC	Input Video Attenuation Control for YCbCr		O	O		
VDPRO.ATCOM	Input Video Attenuation Control for Composite	O				
VDPRO.CUPS	C Signal Up-Sampling Enable	O				
VDPRO.YUPS	Y Signal Up-Sampling Enable	O				
SYNCCTL.OVD	OSD Vsync Delay	O				
SYNCCTL.EXFMD	External Field Detection Mode		SL	SL	SL	SL
SYNCCTL.EXFIV	External Field Input Inversion		SL	SL	SL	SL
SYNCCTL.EXSYNC	External Sync Select		SL	SL	SL	SL
SYNCCTL.EXVIV	External Vertical Sync Input Polarity		SL	SL	SL	SL
SYNCCTL.EXHIV	External Horizontal Sync Input Polarity		SL	SL	SL	SL
SYNCCTL.CSP	Composite Signal Output Polarity		SL	SL	SL	SL
SYNCCTL.CSE	Composite Signal Output Enable		SL	SL	SL	SL
SYNCCTL.SYSW	Output Sync Select		SL	SL	SL	SL
SYNCCTL.VSYNCS	Vertical Sync Output Signal		SL	SL	SL	SL
SYNCCTL.VPL	Vertical Sync Output Polarity		SL	SL	SL	SL
SYNCCTL.HPL	Horizontal Sync Output Polarity		SL	SL	SL	SL
SYNCCTL.SYEV	Vertical Sync Output Enable		SL	SL	SL	SL
SYNCCTL.SYEH	Horizontal Sync Output Enable		SL	SL	SL	SL
HSPLS.HSPLS	Horizontal Sync Pulse Width (number of ENC clocks)	M	M	M	M	M

(1) R = Required, O = Optional, M = Master Mode, SL = Slave Mode, r = Read-Only Status

Table 82. VPBE Global Registers for Hardware Setup (continued)

Register.Field	Description	Analog SDTV	YCC16	YCC8	Parallel RGB	Serial RGB
VSPLS.VSPLS	Vertical Sync Pulse Width (number of ENC clocks)	M	M	M	M	M
HINT.HINT	Horizontal Interval (number of ENC clocks)	M	M	M	M	M
HSTART.HSTART	Horizontal Valid Data Start Position	M	M	M	M	M
HVALID.HVALID	Horizontal Data Valid Range	M	M	M	M	M
VINT.VINT	Vertical Interval (number of lines)	M	M	M	M	M
VSTART.VSTART	Vertical Valid Data Start Position	M	M	M	M	M
VVALID.VVALID	Vertical Data Valid Range	M	M	M	M	M
HSDLY.HSDLY	Output Delay of Horizontal Sync Signal	M	M	M	M	M
VSDLY.VSDLY	Output Delay of Vertical Sync Signal	M	M	M	M	M
YCCCTL.CHM	Chroma Output Mode		O	O		
YCCCTL.YCP	YC Output Order		O	O		
YCCCTL.R656	REC656 Mode (Standard Mode timing only)			O		
RGBCTL.RGBLAT	RGB Latch Setting				O	O
RGBCTL.IRSWP	Swap Order of data output in IronMan mode					O
RGBCTL.IR9	IronMan 9-bit mode					O
RGBCTL.IRONM	IronMan Type RGB output					O
RGBCTL.DFLTR	RGB LPF Sampling Frequency				O	O
RGBCTL.DFLTS	RGB LPF Select				O	O
RGBCTL.RGBEF	RGB Output Order (Line id=1)					O
RGBCTL.RGBOF	RGB Output Order (Line id=0)					O
RGBCLP.UCLIP	Upper Clip Level for RGB Output				O	O
RGBCLP.OFST	Offset Level for RGB Output				O	O
LINECTL.VSTF	Vertical Data Valid Start Position Field Mode					
LINECTL.VCLID	Vertical Culling Line Position					
LINECTL.VCLRD	Vertical Culling Counter Reset Mode					
LINECTL.VCL56	Digital Output Vertical Culling					
LINECTL.HLDF	Digital Output Field Hold					
LINECTL.HLDL	Digital Output Line Hold					
LINECTL.LINID	Start Line ID Control in Even Field					
LINECTL.DCKCLP	DCLK Pattern Switching by Culling Line ID					
LINECTL.DCKCLI	DCLK Polarity Inversion by Culling Line ID					
LINECTL.RGBCL	RGB Output Order Switching by Culling Line ID					
CULLLINE.CLOF	Culling Line ID Toggle Position (Odd field)					
CULLLINE.CLEF	Culling Line ID Toggle Position (Even field)					
CULLLINE.CULI	Culling Line ID Inversion Interval					
LCDOUT.OES	Output Enable Signal Selection				O	O
LCDOUT.FIDP	Field ID Output Polarity				O	O
LCDOUT.PWMP	PWM Output Pulse Polarity				O	O
LCDOUT.PWME	PWM Output Control				O	O
LCDOUT.ACE	LCD_AC Output Control				O	O
LCDOUT.BRP	BRIGHT Output Polarity				O	O
LCDOUT.BRE	BRIGHT Output Control				O	O
LCDOUT.OEP	LCD_OE Output Polarity		O	O	O	O

Table 82. VPBE Global Registers for Hardware Setup (continued)

Register.Field	Description	Analog SDTV	YCC16	YCC8	Parallel RGB	Serial RGB
LCDOUT.OEE	LCD_OE Output Control		O	O	O	O
BRTS.BRTS	BRIGHT Pulse Start Position				O	O
BRTW.BRTW	BRIGHT Pulse Width				O	O
ACCTL.ACTF	LCD_AC Toggle Interval				O	O
ACCTL.ACTH	LCD_AC Toggle Horizontal Position				O	O
PWMP.PWMP	PWM Output Period				O	O
PWMW.PWMW	PWM Output Pulse Width				O	O
DCLKCTL.DCKIM	DCLK Internal Mode					
DCLKCTL.DOFST	DCLK Output Offset					
DCLKCTL.DCKEC	DCLK Pattern Mode				R	R
DCLKCTL.DCKME	DCLK Mask Control					
DCLKCTL.DCKOH	DCLK Output Divide					
DCLKCTL.DCKIH	Internal DCLK Output Divide					
DCLKCTL.DCKPW	DCLK Pattern Valid Bit Width				R	R
DCLKPTN0.DCPTN0	DCLK Pattern				R	R
DCLKPTN1.DCPTN1	DCLK Pattern				R	R
DCLKPTN2.DCPTN2	DCLK Pattern				R	R
DCLKPTN3.DCPTN3	DCLK Pattern				R	R
DCLKPTN0A.DCPTN0A	DCLK Pattern (auxiliary)					
DCLKPTN1A.DCPTN1A	DCLK Pattern (auxiliary)					
DCLKPTN2A.DCPTN2A	DCLK Pattern (auxiliary)					
DCLKPTN3A.DCPTN3A	DCLK Pattern (auxiliary)					
DCLKHS.DCHS	Horizontal DCLK Mask Start Position					
DCLKHSA.DCHS	Horizontal DCLK (auxiliary) Mask Start Position					
DCLKHR.DCHR	Horizontal DCLK Mask Range					
DCLKVS.DCVS	DCLK Vertical Mask Start Position					
DCLKVR.DCVR	DCLK Vertical Mask Range					
CAPCTL.CADF	Closed Caption Default Data Register	O				
CAPCTL.CAPF	Closed Caption Field Select	O				
CAPDO.CADO0	Closed Caption Default Data0 (odd field)	O				
CAPDO.CADO1	Closed Caption Default Data1 (odd field)	O				
CAPDE.CADE0	Closed Caption Default Data0 (even field)	O				
CAPDE.CADE1	Closed Caption Default Data1 (even field)	O				
ATR0.ATR0	Video Attribute Data Register 0	O				
ATR1.ATR1	Video Attribute Data Register 1	O				
ATR2.ATR2	Video Attribute Data Register 2	O				
VSTAT.CAEST	Closed Caption Status (even field)	r				
VSTAT.CAOST	Closed Caption Status (odd field)	r				
VSTAT.FIDST	Field ID Monitor	r	r	r	r	r
RAMADR.RAMADR	Gamma Correction Table RAM address					
RAMPORT.RAMPORT	RAM Data Port					
DACTST.DAPD0	DAC0 Power-Down	O				
DACTST.DACDC	DC Output mode	O				
DACTST.DALVL	DC DC Level control	O				
YCOLVL.YLVL	YOUT DC Level		O	O		

Table 82. VPBE Global Registers for Hardware Setup (continued)

Register.Field	Description	Analog SDTV	YCC16	YCC8	Parallel RGB	Serial RGB
YCOLVL.CLVL	COUT DC Level		O	O		
SCPROG.SCSD	Sub-Carrier Initial Phase Value	O				
CVBS.YCDLY	Delay Adjustment of Y Signal in Composite Signal	O				
CVBS.CVLVL	Composite Video Level (sync/white)	O				
CVBS.CSTUP	Setup Level at NTSC Output	O				
CVBS.CBLS	Blanking Shape Disable	O				
CVBS.CBBLD	Blanking Build-Up Time for Composite Output	O				
CVBS.CSBLD	Sync Build-Up Time for Composite Output	O				
ETMG0.CEPW	Equalizing Pulse Width Offset for Composite	O				
ETMG0.CFSW	Field Sync Pulse Width Offset for Composite	O				
ETMG0.CLSW	Line Sync Pulse Width Offset for Composite	O				
ETMG1.CBSE	Burst End Position Offset for Composite	O				
ETMG1.CBST	Burst Start Position Offset for Composite	O				
ETMG1.CFPW	Front Porch Position Offset for Composite	O				
ETMG1.CLBI	Line Blanking End Pos. offset for composite	O				
DRGBX0.DGY	YCbCr→RGB Coefficient GY for Digital RGB				R	R
DRGBX1.DRV	YCbCr→RGB Coefficient RV for Digital RGB				R	R
DRGBX2.DGU	YCbCr→RGB Coefficient GU for Digital RGB				R	R
DRGBX3.DGV	YCbCr→RGB Coefficient GV for Digital RGB				R	R
DRGBX4.DBU	YCbCr→RGB Coefficient BU for Digital RGB				R	R
VSTARTA.VSTARTA	Vertical Data Valid Start Position for Even Field					
OSDCLK0.OCPW	OSD Clock Pattern Bit Width					
OSDCLK1.OCPT	OSD Clock Pattern					
HVLDCL0.HCM	Horizontal Valid Culling Mode					
HVLDCL0.HCPW	Horizontal Valid Culling Pattern Bit Width					
HVLDCL1.HCPT	Horizontal Culling Pattern					
OSDHADV.OHAD	OSD Horizontal Sync Advance					
CLKCTL.CLKGAM	Clock Enable for Gamma Correction Table					
CLKCTL.CLKDIG	Clock Enable for Digital LCD Controller					
CLKCTL.CLKENC	Clock Enable for Video Encoder					
CLKCTL.GAMON	Enable Gamma Correction					

5.5.1.3 Gamma Table Setup

The user-defined Gamma RAM table must be programmed before it can be used.

5.5.2 Enable/Disable Hardware

The VENC has several module enables as described in Table 83.

Table 83. OSD Window Enable/Disable

Module	Display Enable
VPBE	VPBE.CLK_OFF
VENC	VMOD.VIE
Composite Analog Out	VMOD.VIE, CLKCTL.CLKENC
Digital Output	VIDCTL.DOMD, CLKCTL.CLKDIG

5.5.3 Events and Status Checking

The VENC frame sync generates an interrupt. This is useful primarily for OSD operation.

6 VPBE Registers

There are four sub-modules associated with the VPBE subsystem. The VPSS Clock (VPSSCLK) and Buffer Logic (VPSSBL) modules include common controls for VPBE as well as VPFE. The modules are described below.

Table 84. VPBE Module Register Map

Address	Register	Description
0x01C7:0000	VPSSCLK	VPSS Clock Control
0x01C7:0080	H3A	VPFE – Hardware 3A
0x01C7:0100	IPIPEIF	VPFE – Image Pipe IF
0x01C7:0200	OSD	VPBE – On Screen Display
0x01C7:0400	VENC	VPBE – Video Encoder / Digital LCD controller
0x01C7:0600	CCDC	VPFE – CCD Controller
0x01C7:0800	VPSSBL	VPSS Buffer Logic
0x01C7:1000	IPIPE	VPFE – Image Pipe

6.1 VPSSCLK - VPSS Clock Controller

The VPSS clock controller provides registers to set the VPSS clock options.

Table 85. VPSS Clock Controller Register Map

Address	Register	Description	Section
0x01C7:0000	PID	Peripheral Revision and Class Information	Section 6.1.1
0x01C7:0004	CLKCTRL	VPBE Clock Control Register	Section 6.1.2

6.1.1 Peripheral Revision and Class Information (PID)

The peripheral revision and class information register (PID) is shown in Figure 91 and described in Table 86.

Figure 91. Peripheral Revision and Class Information Register (PID)

31	24	23	16
Reserved		TID	
R-0		R-0	

15	8	7	0
CID		PREV	
R-251		R-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 86. Peripheral Revision and Class Information Register (PID) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Reserved
23-16	TID	0-FFh	Peripheral identification
		0	VPSS module

Table 86. Peripheral Revision and Class Information Register (PID) Field Descriptions (continued)

Bit	Field	Value	Description
15-8	CID	0-FFh	Class identification
		251	VPSS module
7-0	PREV	0-FFh	Peripheral revision number
		0	Initial revision

6.1.2 VPSS Clock Control Register (CLKCTRL)

The VPSS clock control register (CLKCTRL) is shown in Figure 92 and described in Table 87.

Figure 92. VPSS Clock Control Register (CLKCTRL)

31	16
Reserved	
R-0	

15	7	6	5	4	3	2	1	0
Reserved		CCDC_CLK	IPIPE_CLK	H3A_CLK	Rsvd	VENC_CLKSEL	Reserved	VPBE_CLK
R-0		R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 87. VPSS Clock Control Register (CLKCTRL) Field Descriptions

Bit	Field	Value	Description
31- 7	Reserved	0	Reserved
6	CCDC_CLK		CCDC clock enable
		0	Clock off
		1	Clock on
5	IPIPE_CLK		IPIPE clock enable
		0	Clock off
		1	Clock on
4	H3A_CLK		H3A clock enable
		0	Clock off
		1	Clock on
3	Reserved	0	Reserved
2	VENC_CLKSEL		Select clock for VENC
		0	Clock off
		1	Clock on
1	Reserved		Reserved
0	VPBE_CLK		VPBE clock enable
		0	Clock off
		1	Clock on

6.2 VPSSBL - VPSS Buffer Logic

The VPSS Buffer Logic module provides registers to view and set VPSS Buffer Logic status.

Table 88. VPSS Buffer Logic Register Map

Offset	Acronym	Register Description	Section
2780h	PID	Peripheral Revision and Class Information Register	Section 6.2.1
2784h	PCR	Peripheral Control Register	Section 6.2.2
2788h	INTSTAT	Interrupt Status Register	Section 6.2.3
278Ch	INTSEL	Interrupt Selection Register	Section 6.2.4
2790h	EVTSEL	Event Selection Register	Section 6.2.5
2794h	MEMCTRL	Shared Memory Master Select Register	Section 6.2.6

6.2.1 Peripheral Revision and Class Information (PID)

The peripheral revision and class information register (PID) is shown in Figure 93 and described in Table 89.

Figure 93. Peripheral Revision and Class Information Register (PID)

31	24	23	16
Reserved		TID	
R-0		R-1	

15	8	7	0
CID		PREV	
R-255		R-1	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

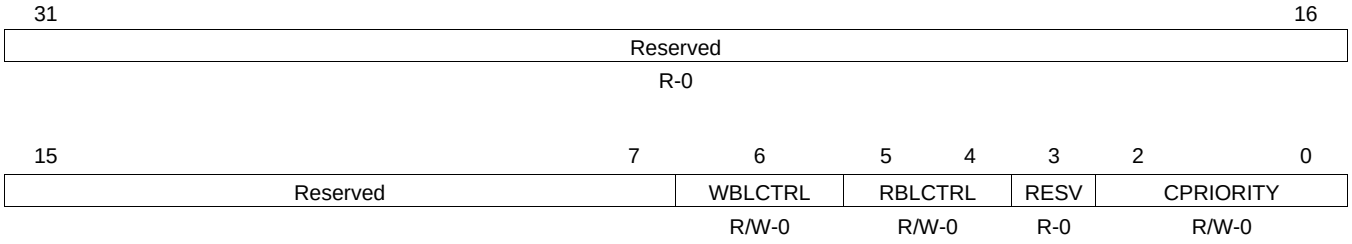
Table 89. Peripheral Revision and Class Information Register (PID) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Reserved
23-16	TID	0-FFh	Peripheral identification
		0	VPSS module
15-8	CID	0-FFh	Class identification
		255	VPSS module
7-0	PREV	0-FFh	Peripheral revision number
		0	Initial revision

6.2.2 Peripheral Control Register (PCR)

The peripheral control register (PCR) is shown in Figure 94 and described in Table 90.

Figure 94. Peripheral Control Register (PCR)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 90. Peripheral Control Register (PCR) Field Descriptions

Bit	Field	Value	Description
31-7	Reserved		Reserved
6	WBLCTRL		Select DDR2/mDDR write transfer
		0	IPIPE
		1	Reserved
5-4	RBLCTRL		Select DDR2/mDDR read master
		0	IPIPEIF
		1	Reserved
		2	H3A
3	Reserved		Reserved
2-0	CPRIORITY		Sets priority of VPSS
		0	Set to highest priority for best performance
		1	

6.2.3 Interrupt Status Register (INTSTAT)

The interrupt status register (INTSTAT) is shown in Figure 95 and described in Table 91.

Figure 95. Interrupt Status Register (INTSTAT)

31	30	29	28	27	26	25	24
Reserved							
R-0							

23	22	21	20	19	18	17	16
Reserved							
R-0							

15	14	13	12	11	10	9	8
Reserved			IPIPE_INT5	IPIPE_INT4	IPIPE_INT3	IPIPE_INT2	IPIPE_INT1
R-0			R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
IPIPE_INT0	IPIPEIFINT	OSDINT	VENCINT	H3AINT	CCDC_VDINT2	CCDC_VINT1	CCDC_VINT0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 91. Interrupt Status Register (INTSTAT) Field Descriptions

Bit	Field	Value	Description
31- 13	Reserved	0	Reserved
12	IPIPE_INT5		IPIPE_INT5 interrupt bit.
		0	Set when HSSIINT is triggered.
		1	Clear
11	IPIPE_INT4		IPIPE_INT4 interrupt bit.
		0	Set when IPIPE_INT4 is triggered.
		1	Clear
10	IPIPE_INT3		IPIPE_INT3 interrupt bit.
		0	Set when HSSIINT is triggered.
		1	Clear
9	IPIPE_INT2		IPIPE_INT2 interrupt bit.
		0	Set when IPIPE_INT2 is triggered.
		1	Clear
8	IPIPE_INT1		IPIPE_INT1 interrupt bit.
		0	Set when IPIPE_INT1 is triggered.
		1	Clear
7	IPIPE_INT0		IPIPE_INT0 interrupt bit.
		0	Set when IPIPE_INT4 is triggered.
		1	Clear
6	IPIPEIFINT		IPIPEIFIN interrupt bit.
		0	Set when IPIPEIFINT is triggered.
		1	Clear
5	OSDINT		OSDINT interrupt bit.

Table 91. Interrupt Status Register (INTSTAT) Field Descriptions (continued)

Bit	Field	Value	Description
		0	Set when OSDINT is triggered.
		1	Clear
4	VENCINT		VENCINT interrupt bit.
		0	Set when VENCINT is triggered.
		1	Clear
3	H3AINT		H3AINT interrupt bit.
		0	Set when H3AINT is triggered.
		1	Clear
2	CCDC_VDINT2		CCDC_VDINT2 interrupt bit.
		0	Set when CCDC_VDINT2 is triggered.
		1	Clear
1	CCDC_VDINT1		CCDC_VDINT1 interrupt bit.
		0	Set when CCDC_VDINT1 is triggered.
		1	Clear
0	CCDC_VDINT0		CCDC_VDINT0 interrupt bit.
		0	Set when CCDC_VDINT0 is triggered.
		1	Clear

6.2.4 Interrupt Selection Register (INTSEL)

The interrupt selection register (INTSEL) is shown in Figure 96 and described in Table 92.

Figure 96. Interrupt Selection Register (INTSEL)

31 28	27 24	23 20	19 16
INTSEL7	INTSEL6	INTSEL5	INTSEL4
R/W - 7	R/W - 6	R/W - 5	R/W - 4

15 12	11 8	7 4	3 0
INTSEL3	INTSEL2	INTSEL1	INTSEL0
R/W - 3	R/W - 2	R/W - 1	R/W - 0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 92. Interrupt Selection Register (INTSEL) Field Descriptions

Bit	Field	Value	Description
31- 28	INTSEL7	0-Fh	Selects the interrupt for vpss-int[7]
		0	CCDC VDINT0
		1	CCDC VDINT1
		2h	CCDC VDINT2
		3h	H3AINT
		4h	VENCINT
		5h	OSDINT
		6h	IPIPEIFINT
		7h	IPIPE_INT0_HST
		8h	IPIPE_INT1_SDR
		9h	IPIPE_INT2_RZA
		10h	IPIPE_INT3_RZB
		11h	IPIPE_INT4_BSC
		12h	IPIPE_INT5_MMR
27 - 24	INTSEL6	0-Fh	Selects the interrupt for vpss-int[6]
23 - 20	INTSEL5	0-Fh	Selects the interrupt for vpss-int[5]
19 - 16	INTSEL4	0-Fh	Selects the interrupt for vpss-int[4]
15 - 12	INTSEL3	0-Fh	Selects the interrupt for vpss-int[3]
11 - 8	INTSEL2	0-Fh	Selects the interrupt for vpss-int[2]
7 - 4	INTSEL1	0-Fh	Selects the interrupt for vpss-int[1]
3 - 0	INTSEL0	0-Fh	Selects the interrupt for vpss-int[0]

6.2.5 Event Selection Register (EVTSEL)

The event selection register (EVTSEL) is shown in Figure 97 and described in Table 93.

Figure 97. Event Selection Register (EVTSEL)

31 28	27 24	23 20	19 16
EVTSEL3	EVTSEL2	EVTSEL1	EVTSEL0
R/W - 13	R/W - 11	R/W - 8	R/W - 3

15 4	3 0
Reserved	EVTSEL8
R - 0	R/W - 8

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

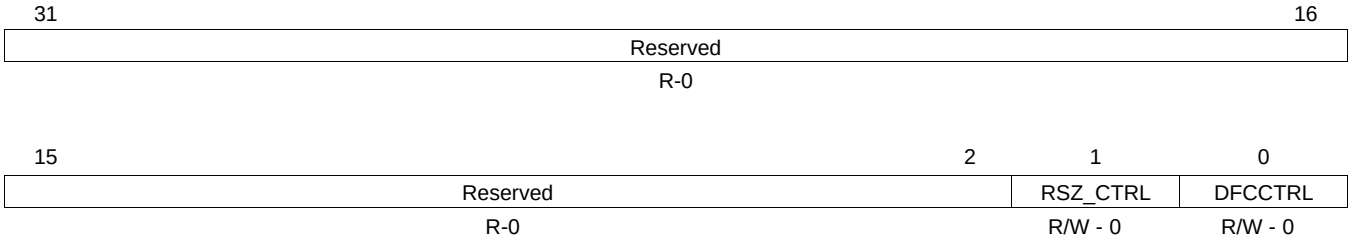
Table 93. Event Selection Register (EVTSEL) Field Descriptions

Bit	Field	Value	Description
31- 28	EVTSEL3	0-Fh	Selects the interrupt for vpss-int[3]
		0	CCDC VDINT0
		1	CCDC VDINT1
		2h	CCDC VDINT2
		3h	H3AINT
		4h	VENCINT
		5h	OSDINT
		6h	IPIPEIFINT
		7h	IPIPE_INT0_HST
		8h	IPIPE_INT1_SDR
		9h	IPIPE_INT2_RZA
		10h	IPIPE_INT3_RZB
		11h	IPIPE_INT4_BSC
		12h	IPIPE_INT5_MMR
27 - 24	EVTSEL2	0-Fh	Selects the interrupt for vpss-int[2]
23 - 20	EVTSEL1	0-Fh	Selects the interrupt for vpss-int[1]
19 - 16	EVTSEL0	0-Fh	Selects the interrupt for vpss-int[0]
15 - 4	Reserved		Reserved
3 - 0	EVTSEL8	0-Fh	Selects the interrupt for vpss-int[8]

6.2.6 Shared Memory Master Select Register (MEMCTRL)

The shared memory master select register (MEMCTRL) is shown in Figure 98 and described in Table 94.

Figure 98. Shared Memory Master Select Register (MEMCTRL)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 94. Shared Memory Master Select Register (MEMCTRL) Field Descriptions

Bit	Field	Value	Description
31- 2	Reserved	0	Reserved
1	RSZ_CTRL		Resizer memory select
		0	IPIPE
		1	
0	DFCCTRL		Defect correction memory select
		0	IPIPE
		1	CCDC

6.3 On-Screen Display (OSD) Registers

Table 95 lists the registers for the OSD module. See the device-specific data manual for the memory address of these registers. All other register offset addresses not listed in Table 95 should be considered as reserved locations and the register contents should not be modified.

Some registers/fields are shadowed during the frame display time and any writes to these locations are not applied until the next frame period. These are noted in Table 81.

Note: The upper 16 bits of these registers are not shown; they are reserved.

Table 95. On-Screen Display (OSD) Registers

Offset	Register	Description	Section
200h	MODE	OSD Mode Register	Section 6.3.1
204h	VIDWINMD	Video Window Mode Setup Register	Section 6.3.2
208h	OSDWIN0MD	OSD Window Mode Setup Register	Section 6.3.3
20Ch	OSDWIN1MD	OSD Window 1 Mode Setup Register (when used as a second OSD window)	Section 6.3.4
20Ch	OSDATRMD	OSD Attribute Window Mode Setup (when used as an attribute window)	Section 6.3.5
210h	RECTCUR	Rectangular Cursor Setup Register	Section 6.3.6
214h	Reserved	Reserved	
218h	VIDWIN0OFST	Video Window 0 Offset Register	Section 6.3.7
21Ch	VIDWIN1OFST	Video Window 1 Offset Register	Section 6.3.8
220h	OSDWIN0OFST	OSD Window 0 Offset Register	Section 6.3.9
224h	OSDWIN1OFST	OSD Window 1 Offset Register	Section 6.3.10
228h	VIDWIN0ADH	Video Window 0/1 Address - High Register	Section 6.3.11
22Ch	VIDWIN0ADL	Video Window 0 Address - Low Register	Section 6.3.12
230h	VIDWIN1ADL	Video Window 1 Address - Low Register	Section 6.3.13
234h	OSDWINADH	OSD Window 0/1 Address - High Register	Section 6.3.14
238h	OSDWIN0ADL	OSD Window 0 Address - Low Register	Section 6.3.15
23Ch	OSDWIN1ADL	Bitmap Window 1 / Attribute Window 0 Address - Low Register	Section 6.3.16
240h	BASEPX	Base Pixel X Register	Section 6.3.17
244h	BASEPY	Base Pixel Y Register	Section 6.3.18
248h	VIDWIN0XP	Video Window 0 X-Position Register	Section 6.3.19
24Ch	VIDWIN0YP	Video Window 0 Y-Position Register	Section 6.3.20
250h	VIDWIN0XL	Video Window 0 X-Size Register	Section 6.3.21
254h	VIDWIN0YL	Video Window 0 Y-Size Register	Section 6.3.22
258h	VIDWIN1XP	Video Window 1 X-Position Register	Section 6.3.23
25Ch	VIDWIN1YP	Video Window 1 Y-Position Register	Section 6.3.24
260h	VIDWIN1XL	Video Window 1 X-Size Register	Section 6.3.25
264h	VIDWIN1YL	Video Window 1 Y-Size Register	Section 6.3.26
268h	OSDWIN0XP	OSD Bitmap Window 0 X-Position Register	Section 6.3.27
26Ch	OSDWIN0YP	OSD Bitmap Window 0 Y-Position Register	Section 6.3.28
270h	OSDWIN0XL	OSD Bitmap Window 0 X-Size Register	Section 6.3.29
274h	OSDWIN0YL	OSD Bitmap Window 0 Y-Size Register	Section 6.3.30
278h	OSDWIN1XP	OSD Bitmap Window 1 X-Position Register	Section 6.3.31
27Ch	OSDWIN1YP	OSD Bitmap Window 1 Y-Position Register	Section 6.3.32
280h	OSDWIN1XL	OSD Bitmap Window 1 X-Size Register	Section 6.3.33
284h	OSDWIN1YL	OSD Bitmap Window 1 Y-Size Register	Section 6.3.34
288h	CURXP	Rectangular Cursor Window X-Position Register	Section 6.3.35

Table 95. On-Screen Display (OSD) Registers (continued)

Offset	Register	Description	Section
28Ch	CURYP	Rectangular Cursor Window Y-Position Register	Section 6.3.36
290h	CURXL	Rectangular Cursor Window X-Size Register	Section 6.3.37
294h	CURYL	Rectangular Cursor Window Y-Size Register	Section 6.3.38
298h	Reserved	Reserved	
29Ch	Reserved	Reserved	
2A0h	W0BMP01	Window 0 Bitmap Value to Palette Map 0/1 Register	Section 6.3.39
2A4h	W0BMP23	Window 0 Bitmap Value to Palette Map 2/3 Register	Section 6.3.40
2A8h	W0BMP45	Window 0 Bitmap Value to Palette Map 4/5 Register	Section 6.3.41
2ACh	W0BMP67	Window 0 Bitmap Value to Palette Map 6/7 Register	Section 6.3.42
2B0h	W0BMP89	Window 0 Bitmap Value to Palette Map 8/9 Register	Section 6.3.43
2B4h	W0BMPAB	Window 0 Bitmap Value to Palette Map A/B Register	Section 6.3.44
2B8h	W0BMPCD	Window 0 Bitmap Value to Palette Map C/D Register	Section 6.3.45
2BCh	W0BMPEF	Window 0 Bitmap Value to Palette Map E/F Register	Section 6.3.46
2C0h	W1BMP01	Window 1 Bitmap Value to Palette Map 0/1 Register	Section 6.3.47
2C4h	W1BMP23	Window 1 Bitmap Value to Palette Map 2/3 Register	Section 6.3.48
2C8h	W1BMP45	Window 1 Bitmap Value to Palette Map 4/5 Register	Section 6.3.49
2CCh	W1BMP67	Window 1 Bitmap Value to Palette Map 6/7 Register	Section 6.3.50
2D0h	W1BMP89	Window 1 Bitmap Value to Palette Map 8/9 Register	Section 6.3.51
2D4h	W1BMPAB	Window 1 Bitmap Value to Palette Map A/B Register	Section 6.3.52
2D8h	W1BMPCD	Window 1 Bitmap Value to Palette Map C/D Register	Section 6.3.53
2DCh	W1BMPEF	Window 1 Bitmap Value to Palette Map E/F Register	Section 6.3.54
2E0h	VBINDRY	Test Mode	Section 6.3.55
2E4h	EXTMODE	Extended Mode	Section 6.3.56
2E8h	MISCCTL	Miscellaneous Control Register	Section 6.3.57
2ECh	CLUTRAMYCB	CLUT RAMYCB Setup Register	Section 6.3.58
2F0h	CLUTRAMCR	CLUT RAM Setup Register	Section 6.3.59
2F4h	TRANSPVALL	Transparency Color Code - Lower Register	Section 6.3.60
2F8h	TRANSPVALU	Transparency Color Code - Upper Register	Section 6.3.61
2FCh	TRANSPBMPIDX	Transparent index Code for Bitmaps	Section 6.3.62

6.3.1 OSD Mode Register (MODE)

The OSD mode register (MODE) is shown in Figure 99 and described in Table 96.

Figure 99. OSD Mode Register (MODE)

31	16
Reserved	
R-0	

15	14	13	12	11	10	9	8	7	0
CS	OVRSZ	OHRSZ	EF	VVRSZ	VHRSZ	FSINV	BCLUT	CABG	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 96. OSD Mode Register (MODE) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15	CS		Cb/Cr or Cr/Cb format. This bit selects the order of the input data relative to the placement of the Cb and Cr components.
		0	Cb/Cr
		1	Cr/Cb
14	OVRSZ		OSD window vertical expansion enable. When enabled, the bitmap window images are stretched by a factor of 6/5 in the vertical direction. Results in proper vertical sizing to display a normal VGA (640 × 480) image on a PAL television (720 × 576); that is, 480 × 6/5 = 576.(1)(2)
		0	× 1
		1	× 6/5
13	OHRSZ		OSD window horizontal expansion enable. When enabled, the bitmap window images are stretched by a factor of 9/8 in the horizontal direction. Results in proper horizontal sizing to display a normal VGA (640 × 480) image on a PAL / NTSC television (720); i.e., 640x9/9=720.(3)(2)
		0	× 1
		1	× 9/8
12	EF		Expansion filter enable. Valid when either VVRSZ or VHRSZ is on, or video window zoom is set. When either VVRSZ (x6/5 vertical expansion) or VHRSZ (9/8 horizontal expansion) are enabled, this will enable different filter coefficients in place of the normal bilinear expansion coefficients to reduce flicker between fields. Otherwise, an anti-flicker filter is applied regardless of the vertical and horizontal zoom settings in VIDWINMD.VHZn and VIDWINMD.VHZn (i.e., even at x1 zoom) VD latches this bit.(4)
		0	Off
		1	On
11	VVRSZ		Video window vertical expansion enable. When enabled, the video window images are stretched by a factor of 6/5 in the vertical direction. Results in proper vertical sizing to display a normal VGA (640 × 480) image on a PAL television (720 × 576); that is, 480 × 6/5 = 576. (2)(5) VD latches this bit.
		0	× 1
		1	× 6/5
10	VHRSZ		Video window horizontal expansion enable. When enabled, the video window images are stretched by a factor of 9/8 in the horizontal direction. Results in proper horizontal sizing to display a normal VGA (640 × 480) image on an NTSC/PAL television (720 × n); that is, 640 × 9/8 = 720. (2)(5) VD latches this bit.
		0	× 1
		1	× 9/8

(1) This expansion only duplicates one line out of every five lines.
(2) This setting is effective when EXTMODE.EXPMDSEL = 0.
(3) This expansion only duplicates one pixel of every eight pixels.
(4) If EXTMODE.EXPMDSEL = 1, then this bit must = 0 (disabled).
(5) Simple bilinear interpolation of luma is performed if MODE.EF = 1

Table 96. OSD Mode Register (MODE) Field Descriptions (continued)

Bit	Field	Value	Description
9	FSINV		Field signal inversion. Controls polarity of the FIELD ID signal from the video encoder. VD latches this bit.
		0	Non-inverted
		1	Inverted
8	BCLUT		Background CLUT selection. Selects lookcolor up table for background color display. VD latches this bit.
		0	ROM
		1	RAM
7-0	CABG	0-FFh	Background color CLUT. Specifies the image display background color by CLUT address. This color is displayed in any part of the display region where a window is not displayed.

6.3.2 Video Window Mode Setup Register (VIDWINMD)

The video window mode setup register (VIDWINMD) is shown in Figure 100 and described in Table 97.

Figure 100. Video Window Mode Setup Register (VIDWINMD)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFINV	V1EFC	VHZ1		VVZ1		VFF1	ACT1	Rsvd	V0EFC	VHZ0		VVZ0		VFF0	ACT0
R/W-0	R/W-0	R/W-0		R/W-0		R/W-0	R/W-0	R-0	R/W-0	R/W-0		R/W-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 97. Video Window Mode Setup Register (VIDWINMD) Field Descriptions

Bit	Field	Value	Description
15	VFINV		Video window 0/1 expansion filter coefficient inverse. When V1EFC or VnEFC is set, this bit is valid.
		0	Inversed
		1	Normal
14	V1EFC		Video window 1 expansion filter coefficient. Enables different anti-flicker coefficients for each field. Valid when MODE.EF=1
		0	Same coefficients for field-0 and field-1.
		1	Different coefficients for field-0 and field-1.
13-12	VHZ1	0-3h	Video Window 1 horizontal direction zoom. VD latches this bit.
		0	× 1
		1h	× 2
		2h	× 4
		3h	Reserved (same as 0)
11-10	VVZ1	0-3h	Video window 1 vertical direction zoom. VD latches this bit.
		0	× 1
		1h	× 2
		2h	× 4
		3h	Reserved (same as 0)
9	VFF1		Video window 1 display mode. VD latches this bit.
		0	Off
		1	On
8	ACT1		Sets image display on/off video window 1. VD latches this bit.
		0	Off
		1	On
7	Reserved	0	Reserved

Table 97. Video Window Mode Setup Register (VIDWINMD) Field Descriptions (continued)

Bit	Field	Value	Description
6	V0EFC		Video window 0 expansion filter coefficient. Valid wen MODE.EF=1.
		0	Same coefficients for field-0 and field-1.
		1	Different coefficients for field-0 and field-1.
5-4	VHZ0		Video window 0 horizontal direction zoom. VD latches this bit.
		0	× 1
		1h	× 2
		2h	× 4
		3h	Reserved (same as 0)
3-2	VVZ0		Video window 0 vertical direction zoom. VD latches this bit.
		0	× 1
		1h	× 2
		2h	× 4
		3h	Reserved (same as 0)
1	VFF0		Video window 0 display mode. VD latches this bit.
		0	Field mode
		1	Frame mode
0	ACT0		Sets image display on/off video window 0. VD latches this bit.
		0	Off
		1	On

6.3.3 Bitmap Window 0 Mode Setup Register (OSDWIN0MD)

The bitmap window 0 mode setup register (OSDWIN0MD) is shown in Figure 101 and described in Table 98.

Figure 101. Bitmap Window 0 Mode Setup Register (OSDWIN0MD)

15	14 13	12	11 10	9 8	7 6	5 3	2	1	0
Reserved	BMPOMD	CLUTS0	OHZ0	OVZ0	BMW0	BLND0	TE0	OFF0	OACT0
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 98. OSD Window 0 Mode Setup Register (OSDWIN0MD) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved
14-13	BMP0MD		Bitmap input mode YCbCr is calculated from the following equation when RGB data is input: Y = 0.2990*R + 0.5870*G + 0.1140*B Cb =-0.1687*R-0.3313*G + 0.5000*B + Offset(128) Cr = 0.5000*R-0.4187*G-0.0813*B + Offset(128)
		0h	(BITMAP) Bitmap data input mode
		1h	(RGB16) RGB data-16 bit/pixel, RGB565 input mode
		2h	(RGB24) RGB data-24 bit/pixel, RGB888 + 8bpp extension data input mode
		3h	(YC) YC data-YCbYCr, Video Window data input mode
12	CLUTS0		CLUT select for OSD window 0. Selects look-up table that is used for OSD window 0. VD latches this bit.
		0	ROM-look-up table
		1	RAM-look-up table
11-10	OHZ0	0-3h	OSD window 0 horizontal zoom. VD latches this bit.
		0	× 1
		1h	× 2
		2h	× 4
		3h	Reserved (same as 0)
9-8	OVZ0	0-3h	OSD window 0 vertical zoom. VD latches this bit.
		0	× 1
		1h	× 2
		2h	× 4
		3h	Reserved (same as 0)
7-6	BMW0	0-3h	Bitmap bit width for OSD window 0. VD latches this bit. This is valid only for bitmap input mode.
		0	1 bit
		1h	2 bits
		2h	4 bits
		3h	8 bits
5-3	BLND0	0-7h	Blending ratio between OSD window 0 and Video Window 0. TE0 controls which pixels are blended. VD latches this bit.
		0	W0-0 V0-1
		1h	W0-1/8 V0-7/8
		2h	W0-2/8 V0-6/8
		3h	W0-3/8 V0-5/8
		4h	W0-4/8 V0-4/8
		5h	W0-5/8 V0-3/8
		6h	W0-6/8 V0-2/8
		7h	W0-1 V0-0

Table 98. OSD Window 0 Mode Setup Register (OSDWIN0MD) Field Descriptions (continued)

Bit	Field	Value	Description
2	TE0		Transparency enable for OSD window 0. VD latches this bit.
		0	Disable transparency. The entire bitmap window is blended with the video windows according to BLND0.
		1	Enable transparency: When enabled, blending is only performed for pixels whose value matches the transparency value specified below: • (BMP0MD = 00): TRANSPBMPIDX.BMP0 • (BMP0MD = 01): TRANSPVALL.RGBL • (BMP0MD = 10): TRANSPVALL.RGBL & TRANSPVALU.RGBU • (BMP0MD = 11): TRANSPVALL.Y (only luma value examined) The blending is done as per the BLND0 register configuration.
1	OFF0		OSD window 0 display mode. VD latches this bit.
		0	Field mode
		1	Frame mode
0	OACT0		OSD window 0 active (displayed). VD latches this bit.
		0	Off
		1	On

6.3.4 Bitmap Window 1 Mode Setup Register (OSDWIN1MD)

The bitmap window 1 mode setup register (OSDWIN1MD) is shown in Figure 102 and described in Table 99.

Figure 102. Bitmap Window 1 Mode Setup Register (OSDWIN1MD)

15	14 13	12	11 10	9 8	7 6	5 3	2	1	0
OASW	BMP1MD	CLUTS1	OHZ1	OVZ1	BMW1	BLND1	TE1	OFF1	OACT1
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 99. OSD Window 1 Mode Setup Register (OSDWIN1MD) Field Descriptions

Bit	Field	Value	Description
15	OASW		OSD window 1 attribute mode enable. This bit enables attribute mode for OSD window 0. This bit is latched by VD.
		0	OSD window 1
		1	Attribute window
14-13	BMP1MD		Bitmap input mode YCbCr is calculated from the following equation when RGB data is input: Y = 0.2990*R + 0.5870*G + 0.1140*B Cb =-0.1687*R-0.3313*G + 0.5000*B + Offset(128) Cr = 0.5000*R-0.4187*G-0.0813*B + Offset(128)
		0	(Bitmap) Bitmap data input mode
		1h	(RGB16) RGB data-16 bit/pixel, RGB565 input mode
		2h	(RGB24) RGB data-24 bit/pixel, RGB888 + 8bpp extension data input mode
		3h	(YC) YC data-YCbYCr, Video Window data input mode
			(BITMAP) Bitmap data input mode (ATTENUATED_Y_16_235_CR_16_240_CB_16_240_) Attenuated (Y: 16-235, Cr: 16-240, Cb: 16-240)
12	CLUTS1		CLUT select for OSD window 1 (when OASW = 0). Selects look-up table that is used for OSD window 1.
		0	ROM-look-up table
		1	RAM-look-up table
11-10	OHZ1	0-3h	OSD window 1 horizontal zoom (when OASW = 0). VD latches this bit.
		0	× 1
		1h	× 2
		2h	× 4
		3h	Reserved (same as 0)
9-8	OVZ1	0-3h	OSD window 1 vertical zoom (when OASW = 0). VD latches this bit.
		0	× 1
		1h	× 2
		2h	× 4
		3h	Reserved (same as 0)
7-6	BMW1	0-3h	Bitmap bit width for OSD window 1 (when OASW = 0). VD latches this bit.
		0	1 bit
		1h	2 bits
		2h	4 bits
		3h	8 bits

Table 99. OSD Window 1 Mode Setup Register (OSDWIN1MD) Field Descriptions (continued)

Bit	Field	Value	Description
5-3	BLND1	0-7h	Blending ratio for OSD window 1 (when OASW = 0). Sets blending ratio of OSD window 1 and Video Window 0. VD latches this bit.
		0	W0-0 V0-1
		1h	W0-1/8 V0-7/8
		2h	W0-2/8 V0-6/8
		3h	W0-3/8 V0-5/8
		4h	W0-4/8 V0-4/8
		5h	W0-5/8 V0-3/8
		6h	W0-6/8 V0-2/8
		7h	W0-1 V0-0
2	TE1		Transparency enable for OSD window 1 (when OASW = 0). VD latches this bit.
		0	Disable transparency. The entire bitmap window is blended with the video windows according to BLND1.
		1	Enable transparency: When enabled, blending is only performed for pixels whose value matches the transparency value specified below: • (BMP1MD = 00): TRANSPBMPIDX.BMP0 • (BMP1MD = 01): TRANSPVALL.RGBL • (BMP1MD = 10): TRANSPVALL.RGBL & TRANSPVALU.RGBU • (BMP1MD = 11): TRANSPVALL.Y (only luma value examined) The blending is done as per the BLND0 register configuration.
1	OFF1		OSD window 1 display mode (when OASW = 0). VD latches this bit.
		0	Field mode
		1	Frame mode
0	OACT1		OSD window 1 active (displayed) (when OASW = 0). VD latches this bit.
		0	Off
		1	On

6.3.5 OSD Attribute Window Mode Setup Register (OSDATRMD)

The OSD attribute window mode setup register (OSDATRMD) is shown in Figure 103 and described in Table 100.

Figure 103. OSD Attribute Window Mode Setup Register (OSDATRMD)

15	14 12	11 10	9 8	7 6	5 2	1	0
OASW	Reserved	OHZA	OVZA	BLNKINT	Reserved	OFFA	BLNK
R/W-0	R-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 100. OSD Attribute Window Mode Setup Register (OSDATRMD) Field Descriptions

Bit	Field	Value	Description
15	OASW		OSD window 1 attribute mode enable. This bit enables attribute mode for OSD window 0. VD latches this bit.
		0	OSD window 0
		1	Attribute window
14-12	Reserved	0	Reserved
11-10	OHZA	0-3h	OSD attribute window horizontal zoom (when OASW = 1). VD latches this bit.
		0	× 1
		1h	× 2
		2h	× 4
		3h	Reserved (same as 0)
9-8	OVZA	0-3h	OSD attribute window vertical zoom (when OASW = 1). VD latches this bit.
		0	× 1
		1h	× 2
		2h	× 4
		3h	Reserved (same as 0)
7-6	BLNKINT	0-3h	Blinking interval (when OASW = 1). Specifies the blinking interval of the attribute window in units of 8 VD pulses. VD latches this bit.
		0	1 unit
		1h	2 units
		2h	3 units
		3h	4 units
5-2	Reserved	0	Reserved
1	OFFA		OSD attribute window display mode VD latches this bit.
		0	Field mode
		1	Frame mode
0	BLNK		OSD attribute window blink enable (when OASW = 1). VD latches this bit.
		0	Disable
		1	Enable

6.3.6 Rectangular Cursor Setup Register (RECTCUR)

The rectangular cursor setup register (RECTCUR) is shown in Figure 104 and described in Table 101.

Figure 104. Rectangular Cursor Setup Register (RECTCUR)

15 8	7	6 4	3 1	0
RCAD	CLUTSR	RCHW	RCVW	RCACT
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 101. Rectangular Cursor Setup Register (RECTCUR) Field Descriptions

Bit	Field	Value	Description
15-8	RCAD	0-FFh	Rectangular cursor color palette address.
7	CLUTSR		CLUT select. This bit is latched by VD.
		0	ROM-look-up table
		1	RAM-look-up table
6-4	RCHW	0-7h	Rectangular cursor horizontal line width. Width is 4 pixels × RCHW. VD latches this bit.
		0	1 pixel
		1h	4 pixels
		2h	8 pixels
		3h	12 pixels
		4h	16 pixels
		5h	20 pixels
		6h	24 pixels
		7h	28 pixels
3-1	RCVW	0-7h	Rectangular cursor vertical line width. Width is 2 lines × RCVW. VD latches this bit.
		0	1 line
		1h	2 lines
		2h	4 lines
		3h	6 lines
		4h	8 lines
		5h	10 lines
		6h	12 lines
		7h	14 lines
0	RCACT		Rectangular cursor active (displayed). VD latches this bit.
		0	Off
		1	On

6.3.7 Video Window 0 Offset Register (VIDWIN0OFST)

The video window 0 offset register (VIDWIN0OFST) is shown in Figure 105 and described in Table 102.

Figure 105. Video Window 0 Offset Register (VIDWIN0OFST)16-bit, 1 Row

15	9	8	0
Reserved		V0LO	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 102. Video Window 0 Offset Register (VIDWIN0OFST) Field Descriptions

Bit	Field	Value	Description
15-9	Reserved	0	Reserved
8-0	V0LO	0-1FFh	Video window 0 line offset. Number of burst transfers (32-bytes) in a horizontal line. Video data format is YCbYCr, or 32-bits per 2 pixels, which gives 16-pixels/burst: Line width in pixels/16; for example, 720/16 = 45 (2Dh). VD latches this bit.(1)

(1) If line width setting for the window results in a non-integer value, round the value up to the next larger integer and organize the data in SDRAM so that each line begins on a burst boundary.

6.3.8 Video Window 1 Offset Register (VIDWIN1OFST)

The video window 1 offset register (VIDWIN1OFST) is shown in Figure 106 and described in Table 103.

Figure 106. Video Window 1 Offset Register (VIDWIN1OFST)

15	9	8	0
Reserved		V1LO	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 103. Video Window 1 Offset Register (VIDWIN1OFST) Field Descriptions

Bit	Field	Value	Description
15-9	Reserved	0	Reserved
8-0	V1LO	0-1FFh	Video window 1 line offset. Number of burst transfers (32-bytes) in a horizontal line. Video data format is YCbYCr, or 32-bits per 2 pixels, which gives 16-pixels/burst. Line width in pixels/16; for example, 720/16 = 45 (2Dh). If line width setting for the window result in a non-integer value, round the value up to the next larger integer and organize the data in SDRAM so that each line begins on a burst boundary. VD latches this bit.(1)

(1) If line width setting for the window results in a non-integer value, round the value up to the next larger integer and organize the data in SDRAM so that each line begins on a burst boundary.

6.3.9 OSD Window 0 Offset Register (OSDWIN0OFST)

The OSD window 0 offset register (OSDWIN0OFST) is shown in Figure 107 and described in Table 104.

Figure 107. OSD Window 0 Offset Register (OSDWIN0OFST)

15	9	8	0
Reserved		O0LO	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 104. OSD Window 0 Offset Register (OSDWIN0OFST) Field Descriptions

Bit	Field	Value	Description
15-9	Reserved	0	Reserved
8-0	O0LO	0-1FFh	OSD window 0 line offset. Number of burst transfers (32-bytes) in a horizontal line. This depends on OSD window bit depth: Line width in (pixels × bit depth)/256-bits/burst; for example, (64 × 8)/256 = 2. Note: If line width and bit depth settings for the window result in a non-integer value, round the value up to the next larger integer and organize the data in SDRAM so that each line begins on a burst boundary. VD latches this bit. Examples: Offsets for 256 pixels horizontal: 1-bit mode: (256 × 1)/256 = 1(0001h); 2-bit mode: (256 × 2)/256 = 2(0002h); 4-bit mode: (256 × 4)/256 = 4(0004h); 8-bit mode: (256 × 8)/256 = 8(0008h); RGB565 mode: (256 × 16)/256 = 16(0010h) RGB5888mode: (256 × 32)/256 = 32(0020h)(1)

(1) If line width and bit depth settings for the window results in a non-integer value, round the value up to the next larger integer and organize the data in SDRAM so that each line begins on a burst boundary.

6.3.10 OSD Window 1 Offset Register (OSDWIN1OFST)

The OSD window 1 offset register (OSDWIN1OFST) is shown in Figure 108 and described in Table 105.

Figure 108. OSD Window 1 Offset Register (OSDWIN1OFST)

15	9	8	0
Reserved		O1LO	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 105. OSD Window 1 Offset Register (OSDWIN1OFST) Field Descriptions

Bit	Field	Value	Description
15-9	Reserved	0	Reserved

Table 105. OSD Window 1 Offset Register (OSDWIN1OFST) Field Descriptions (continued)

Bit	Field	Value	Description
8-0	O1LO	0-1FFh	OSD window 1 line offset. Number of burst transfers (32-bytes) in a horizontal line. This depends on OSD window bit depth: Line width in (pixels × bit depth)/256-bits/burst; for example, (64 × 8)/256 = 2. Note: If line width and bit depth settings for the window result in a non-integer value, round the value up to the next larger integer and organize the data in SDRAM so that each line begins on a burst boundary. VD latches this bit. Examples: Offsets for 256 pixels horizontal: 1-bit mode: (256 × 1)/256 = 1(0001h); 2-bit mode: (256 × 2)/256 = 2(0002h); 4-bit mode: (256 × 4)/256 = 4(0004h); 8-bit mode: (256 × 8)/256 = 8(0008h); RGB565 mode: (256 × 16)/256 = 16(0010h). RGB5888mode: (256 × 32)/256 = 32(0020h)(1)

(1) If line width and bit depth settings for the window results in a non-integer value, round the value up to the next larger integer and organize the data in SDRAM so that each line begins on a burst boundary.

6.3.11 Video Window 0/1 Address Register-High (VIDWINADH)

The video window 0 address register-high (VIDWINADH) is shown in Figure 109 and described in Table 106.

Figure 109. Video Window 0/1 Address Register-High (VIDWINADH)

15	14	8
Reserved	V1AH	
R-0	R/W-0	

7	6	0
Reserved	V0AH	
R-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 106. Video Window 0/1 Address Register-High (VIDWINADH) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved
14-8	V1AH	0-7Fh	Video Window 1 SDRAM Source Address-High 7 MSBs of SDRAM source address The SDRAM source address is specified as an offset from the SDRAM base address, in units of 32 bytes. VD latches this bit.
7	Reserved	0	Reserved
6-0	V0AH	0-7Fh	Video Window 0 SDRAM Source Address-High 7 MSBs of SDRAM source address The SDRAM source address is specified as an offset from the SDRAM base address, in units of 32 bytes. VD latches this bit.

6.3.12 Video Window 0 Address Register-Low (VIDWIN0ADL)

The video window 0 address register (VIDWIN0ADR) is shown in Figure 110 and described in Table 107.

Figure 110. Video Window 0 Address Register-Low (VIDWIN0ADL)

15	0
VIDWIN0ADL	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 107. Video Window 0 Address Register-Low (VIDWIN0ADL) Field Descriptions

Bit	Field	Value	Description
15-0	VIDWIN0ADL	0-FFFFh	Video Window 0 SDRAM Source Address-Low 16 LSBs of SDRAM source address The SDRAM source address is specified as an offset from the SDRAM base address, in units of 32 bytes. VD latches this bit.

6.3.13 Video Window1 Address Register-Low (VIDWIN1ADL)

The video window 1 address register-low (VIDWIN1ADL) is shown in Figure 111 and described in Figure 111.

Figure 111. Video Window 1 Address Register-High (VIDWIN1ADL

15	14	8
Reserved	V1AH	
R-0	R/W-0	

7	6	0
Reserved	V0AH	
R-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 108. Video Window 1 Address Register-Low (OSDWIN1ADL) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved
14-8	V1AH	0-7Fh	Video Window 1 SDRAM Source Address-High 7 MSBs of SDRAM source address The SDRAM source address is specified as an offset from the SDRAM base address, in units of 32 bytes. VD latches this bit.
7	Reserved	0	Reserved
6-0	V0AH	0-7Fh	Video Window 0 SDRAM Source Address-High 7 MSBs of SDRAM source address The SDRAM source address is specified as an offset from the SDRAM base address, in units of 32 bytes. VD latches this bit.

6.3.14 Bitmap Window 0/1 Address Register-High (OSDWINADH)

The bitmap window 0 address register-high (VIDWIN0ADH) is shown in Figure 112 and described in Table 109.

Figure 112. Bitmap Window 0/1 Address Register-High (OSDWINADH)

15	14	8
Reserved	V1AH	
R-0	R/W-0	

7	6	0
Reserved	V0AH	
R-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 109. Bitmap Window 0/1 Address Register-High (OSDWINADH) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved
14-8	V1AH	0-7Fh	Video Window 1 SDRAM Source Address-High 7 MSBs of SDRAM source address The SDRAM source address is specified as an offset from the SDRAM base address, in units of 32 bytes. VD latches this bit.
7	Reserved	0	Reserved
6-0	V0AH	0-7Fh	Video Window 0 SDRAM Source Address-High 7 MSBs of SDRAM source address The SDRAM source address is specified as an offset from the SDRAM base address, in units of 32 bytes. VD latches this bit.

6.3.15 Bitmap Window 0 Address Register-Low (OSDWIN0ADL)

The bitmap window 0address register (OSDWIN1ADL) is shown in Figure 113 and described in Table 110.

Figure 113. Bitmap Window 0 Address Register-Low (OSDWIN0ADL)

15	0
BMPWIN0ADL	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 110. Bitmap Window 0 Address Register-Low (OSDWIN0ADL) Field Descriptions

Bit	Field	Value	Description
15-0	BMPWIN0ADL	0-FFFFh	Bitmap Window 0 SDRAM Source Address-Low 16 LSBs of SDRAM source address The SDRAM source address is specified as an offset from the SDRAM base address, in units of 32 bytes. VD latches this bit.

6.3.16 Bitmap Window 1 / Attribute Window 1 Address Register-Low (OSDWIN1ADL

The bitmap window 0 address register (OSDWIN0ADL) is shown in Figure 114 and described in Table 111.

Figure 114. Bitmap Window 1 / Attribute Window 0 Address Register-Low (OSDWIN1ADL)

15	0
BMPWIN0ADL	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 111. Bitmap Window 1 / Attribute Address Register-Low (OSDWIN1ADL) Field Descriptions

Bit	Field	Value	Description
15-0	BMPWIN0ADL	0-FFFFh	Bitmap Window 1 / Attribute SDRAM Source Address-Low 16 LSBs of SDRAM source address The SDRAM source address is specified as an offset from the SDRAM base address, in units of 32 bytes. VD latches this bit.

6.3.17 Base Pixel X Register (BASEPX)

The base pixel X register (BASEPX) is shown Figure 115 and described in Table 112.

Figure 115. Base Pixel X Register (BASEPX)

15	10	9	0
Reserved		BPX	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 112. Base Pixel X Register (BASEPX) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved
9-0	BPX	0-3FFh	Base pixel in X. VD latches this bit. Horizontal base display reference position for all windows. Specified as number of pixels from HD. Value is 24-512. Value uses if the max of the register value or these minimums: • Minimum value is 20 if EXTMODE.EXPMDSEL = 0 (pre blend filtering) • Minimum value is 22 if EXTMODE.EXPMDSEL = 1 (post blend filtering)

6.3.18 Base Pixel Y Register (BASEPY)

The base pixel Y register (BASEPY) is shown in Figure 116 and described in Table 113.

Figure 116. Base Pixel Y Register (BASEPY)

15	9	8	0
Reserved		BPY	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 113. Base Pixel Y Register (BASEPY) Field Descriptions

Bit	Field	Value	Description
15-9	Reserved	0	Reserved
8-0	BPY	0-1FFh	Base pixel (Line) in Y. VD latches this bit. Vertical base display reference position for all windows. Specified as number of pixels (lines) from VD. Value used is MAX(BPY,1); i.e., minimum value is 1.

6.3.19 Video Window 0 X-Position Register (VIDWIN0XP)

The video window 0 X-position register (VIDWIN0XP) is shown in Figure 117 and described in Table 114.

Figure 117. Video Window 0 X-Position Register (VIDWIN0XP)

15	11	10	0
Reserved		V0X	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 114. Video Window 0 X-Position Register (VIDWIN0XP) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved
10-0	V0X	0-3FFh	Video window 0 X-position. Horizontal display start position. Number of pixels from display reference position (BASEPX). VD latches this bit.

6.3.20 Video Window 0 Y-Position Register (VIDWIN0YP)

The video window 0 Y-position register (VIDWIN0YP) is shown in Figure 118 and described in Table 115.

Figure 118. Video Window 0 Y-Position Register (VIDWIN0YP)

15	9	8	0
Reserved		V0Y	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 115. Video Window 0 Y-Position Register (VIDWIN0YP) Field Descriptions

Bit	Field	Value	Description
15-9	Reserved	0	Reserved
8-0	V0Y	0-1FFh	Video window 0 Y-position. Vertical display start position. Number of pixels/lines from display reference position (BASEPY). This bit is latched by VD.

6.3.21 Video Window 0 X-Size Register (VIDWIN0XL)

The video window 0 X-size register (VIDWIN0XL) is shown in Figure 119 and described in Table 116.

Figure 119. Video Window 0 X-Size Register (VIDWIN0XL)

15	11	10	0
Reserved		V0W	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 116. Video Window 0 X-Size Register (VIDWIN0XL) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved
10-0	V0W	0-7FFh	Video window 0 X-width. Horizontal display width in pixels. VD latches this bit.

6.3.22 Video Window 0 Y-Size Register (VIDWIN0YL)

The video window 0 Y-size register (VIDWIN0YL) is shown in Figure 120 and described in Table 117.

Figure 120. Video Window 0 Y-Size Register (VIDWIN0YL)

15	10	9	0
Reserved		V0H	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

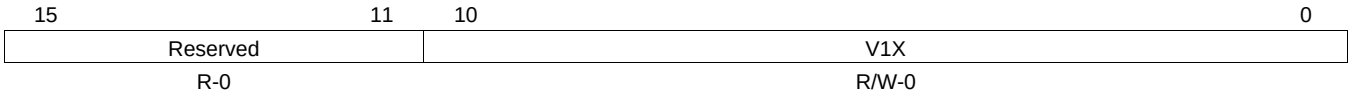
Table 117. Video Window 0 Y-Size Register (VIDWIN0YL) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved
9-0	V0H	0-3FFh	Video window 0 Y-height. Vertical display height in pixels/lines. In frame mode, specify in terms of lines/field. VD latches this bit.

6.3.23 Video Window 1 X-Position Register (VIDWIN1XP)

The video window 1 X-position register (VIDWIN1XP) is shown in Figure 121 and described in Table 118.

Figure 121. Video Window 1 X-Position Register (VIDWIN1XP)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

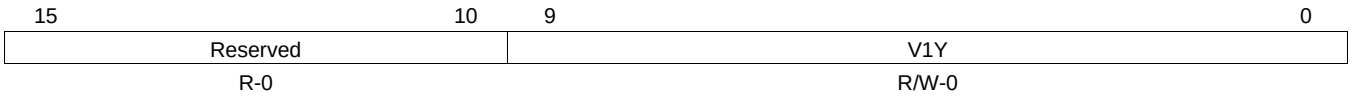
Table 118. Video Window 1 X-Position Register (VIDWIN1XP) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved
10-0	V1X	0-3FFh	Video window 1 X-position. Horizontal display start position. Number of pixels from display reference position (BASEPX). VD latches this bit.

6.3.24 Video Window 1 Y-Position Register (VIDWIN1YP)

The video window 1 Y-position register (VIDWIN1YP) is shown in Figure 122 and described in Table 119.

Figure 122. Video Window 1 Y-Position Register (VIDWIN1YP)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

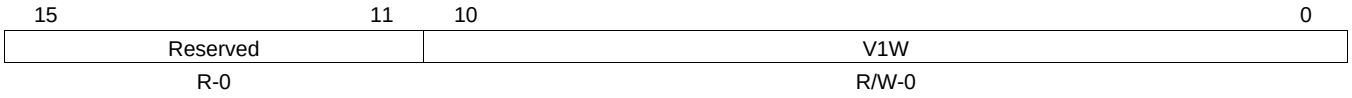
Table 119. Video Window 1 Y-Position Register (VIDWIN1YP) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved
9-0	V1Y	0-1FFh	Video window 1 Y-position. Vertical display start position. Number of pixels/lines from display reference position (BASEPY). VD latches this bit.

6.3.25 Video Window 1 X-Size Register (VIDWIN1XL)

The video window 1 X-size register (VIDWIN1XL) is shown in Figure 123 and described in Table 120.

Figure 123. Video Window 1 X-Size Register (VIDWIN1XL)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

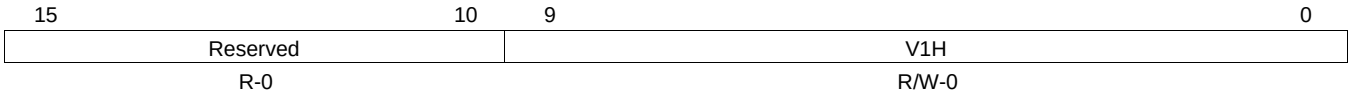
Table 120. Video Window 1 X-Size Register (VIDWIN1XL) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved
10-0	V1W	0-FFFh	Video window 1 X-width. Horizontal display width in pixels. VD latches this bit.

6.3.26 Video Window 1 Y-Size Register (VIDWIN1YL)

The video window 1 Y-size register (VIDWIN1YL) is shown in Figure 124 and described in Table 121.

Figure 124. Video Window 1 Y-Size Register (VIDWIN1YL)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 121. Video Window 1 Y-Size Register (VIDWIN1YL) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved
9-0	V1H	0-7FFh	Video window 1 Y-height. VD latches this bit. Vertical display height in pixels/lines. In frame mode, specify in terms of lines/field.

6.3.27 OSD Bitmap Window 0 X-Position Register (OSDWIN0XP)

The OSD bitmap window 0 X-position register (OSDWIN0XP) is shown in Figure 125 and described in Table 122.

Figure 125. OSD Bitmap Window 0 X-Position Register (OSDWIN0XP)

15	11	10	0
Reserved		W0X	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 122. OSD Bitmap Window 0 X-Position Register (OSDWIN0XP) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved
10-0	W0X	0-3FFh	OSD window 0 X-position. VD latches this bit. Horizontal display start position. Number of pixels from display reference position (BASEPX).

6.3.28 OSD Bitmap Window 0 Y-Position Register (OSDWIN0YP)

The OSD bitmap window 0 Y-position register (OSDWIN0YP) is shown in Figure 126 and described in Table 123.

Figure 126. OSD Bitmap Window 0 Y-Position Register (OSDWIN0YP)

15	10	9	0
Reserved		W0Y	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 123. OSD Bitmap Window 0 Y-Position Register (OSDWIN0YP) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved
9-0	W0Y	0-1FFh	OSD window 0 Y-position. Vertical display start position. Number of pixels/lines from display reference position (BASEPY). VD latches this bit.

6.3.29 OSD Bitmap Window 0 X-Size Register (OSDWIN0XL)

The OSD bitmap window 0 X-size register (OSDWIN0XL) is shown in Figure 127 and described in Table 124.

Figure 127. OSD Bitmap Window 0 X-Size Register (OSDWIN0XL)

15	11	10	0
Reserved		W0W	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 124. OSD Bitmap Window 0 X-Size Register (OSDWIN0XL) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved
10-0	W0W	0-FFFh	OSD window 0 X-width. Horizontal display width in pixels. VD latches this bit.

6.3.30 OSD Bitmap Window 0 Y-Size Register (OSDWIN0YL)

The OSD Bitmap Window 0 Y-Size Register (OSDWIN0YL) is shown in Figure 128 and described in Table 125.

Figure 128. OSD Bitmap Window 0 Y-Size Register (OSDWIN0YL)

15	10	9	0
Reserved		W0H	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 125. OSD Bitmap Window 0 Y-Size Register (OSDWIN0YL) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved
9-0	W0H	0-7FFh	OSD window 0 Y-height. This bit is latched by VD. Vertical display height in pixels/lines. In frame mode, specify in terms of lines/field.

6.3.31 OSD Bitmap Window 1 X-Position Register (OSDWIN1XP)

The OSD bitmap window 1 X-position register (OSDWIN1XP) is shown in Figure 129 and described in Table 126.

Figure 129. OSD Bitmap Window 1 X-Position Register (OSDWIN1XP)

15	11	10	0
Reserved		W1X	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 126. OSD Bitmap Window 1 X-Position Register (OSDWIN1XP) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved
10-0	W1X	0-FF	OSD window 1 X-position. VD latches this bit. Horizontal display start position. Number of pixels from display reference position (BASEPX).

6.3.32 OSD Bitmap Window 1 Y-Position Register (OSDWIN1YP)

The OSD bitmap window 1 Y-position register (OSDWIN1YP) is shown in Figure 130 and described in Table 127.

Figure 130. OSD Bitmap Window 1 Y-Position Register (OSDWIN1YP)

15	10	9	0
Reserved		W1Y	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

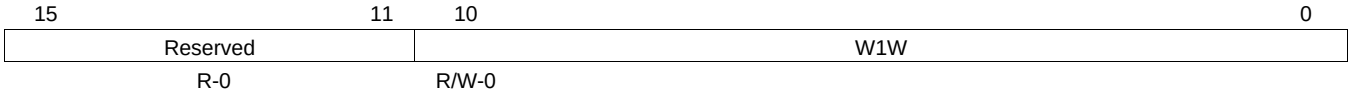
Table 127. OSD Bitmap Window 1 Y-Position Register (OSDWIN1YP) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved
9-0	W1Y	0-1FFh	OSD window 1 Y-position. This bit is latched by VD. Vertical display start position. Number of pixels/lines from display reference position (BASEPY).

6.3.33 OSD Bitmap Window 1 X-Size Register (OSDWIN1XL)

The OSD bitmap window 1 X-size register (OSDWIN1XL) is shown in Figure 131 and described in Table 128.

Figure 131. OSD Bitmap Window 1 X-Size Register (OSDWIN1XL)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

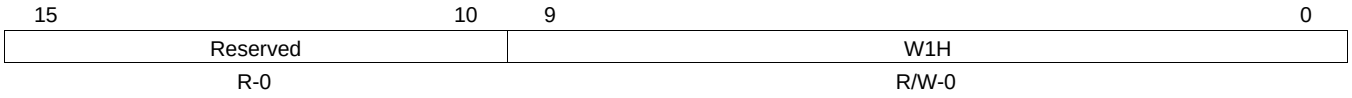
Table 128. OSD Bitmap Window 1 X-Size Register (OSDWIN1XL) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved
10-0	W1W	0-FFFh	OSD window 1 X-width. This bit is latched by VD. Horizontal display width in pixels.

6.3.34 OSD Bitmap Window 1 Y-Size Register (OSDWIN1YL)

The OSD bitmap window 1 Y-size register (OSDWIN1YL) is shown in Figure 132 and described in Table 129.

Figure 132. OSD Bitmap Window 1 Y-Size Register (OSDWIN1YL)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

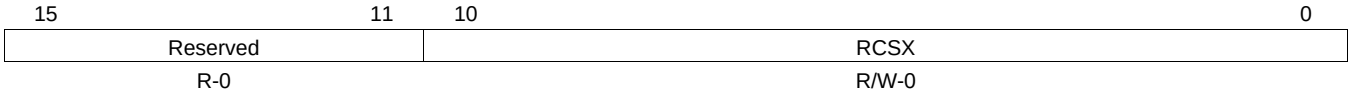
Table 129. OSD Bitmap Window 1 Y-Size Register (OSDWIN1YL) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved
9-0	W1H	0-7FFh	OSD window 1 Y-height. VD latches this bit. Vertical display height in pixels/lines. In frame mode, specify in terms of lines/field.

6.3.35 Rectangular Cursor Window X-Position Register (CURXP)

The rectangular cursor window X-position register (CURXP) is shown in Figure 133 and described in Table 130.

Figure 133. Rectangular Cursor Window X-Position Register (CURXP)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

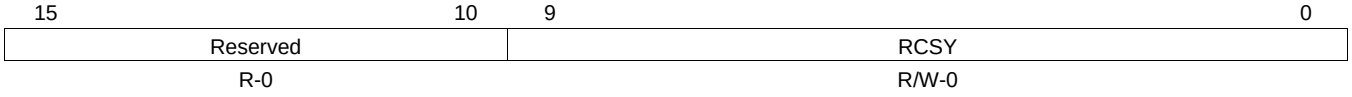
Table 130. Rectangular Cursor Window X-Position Register (CURXP) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved
10-0	RCSX	0-3FFh	Rectangular cursor window X-position. This bit is latched by VD. Horizontal display start position. Number of pixels from display reference position (BASEPX).

6.3.36 Rectangular Cursor Window Y-Position Register (CURYP)

The rectangular cursor window Y-position register (CURYP) is shown in Figure 134 and described in Table 131.

Figure 134. Rectangular Cursor Window Y-Position Register (CURYP)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

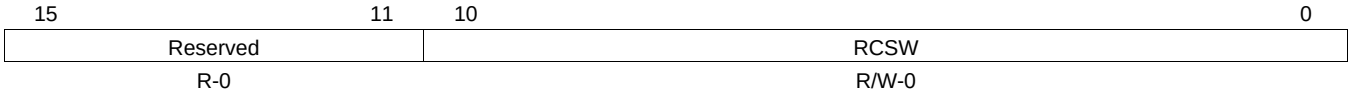
Table 131. Rectangular Cursor Window Y-Position Register (CURYP) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved
9-0	RCSY	0-1FFh	Rectangular cursor window Y-position. This bit is latched by VD. Vertical display start position. Number of pixels from display reference position (BASEPY).

6.3.37 Rectangular Cursor Window X-Size Register (CURXL)

The rectangular cursor window X-size register (CURXL) is shown in Figure 135 and described in Table 132.

Figure 135. Rectangular Cursor Window X-Size Register (CURXL)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

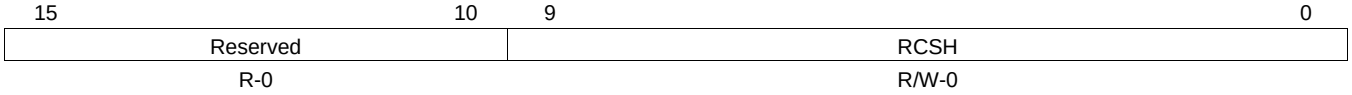
Table 132. Rectangular Cursor Window X-Size Register (CURXL) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved
10-0	RCSW	0-FFFh	Rectangular cursor window X-width. VD latches this bit. Horizontal display width in pixels.

6.3.38 Rectangular Cursor Window Y-Size Register (CURYL)

The rectangular cursor window Y-size register (CURYL) is shown in Figure 136 and described in Table 133.

Figure 136. Rectangular Cursor Window Y-Size Register (CURYL)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 133. Rectangular Cursor Window Y-Size Register (CURYL) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved
9-0	RCSH	0-7FFh	Rectangular cursor window Y-height. VD latches this bit. Vertical display height in pixels/lines. In frame mode, specify in terms of lines/field.

6.3.39 Window 0 Bitmap Value to Palette Map 0/1 Register (W0BMP01)

The window 0 bitmap value to palette map 0/1 register (W0BMP01) is shown in Figure 137 and described in Table 134.

Figure 137. Window 0 Bitmap Value to Palette Map 0/1 Register (W0BMP01)

15	8	7	0
PAL01		PAL00	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 134. Window 0 Bitmap Value to Palette Map 0/1 Register (W0BMP01) Field Descriptions

Bit	Field	Value	Description
15-8	PAL01	0-FFh	Palette address for bitmap value [1]-OSD window 0 [4-bit]
7-0	PAL00	0-FFh	Palette address for bitmap value [0]-OSD window 0 [4-bit, 2-bit, 1-bit]

6.3.40 Window 0 Bitmap Value to Palette Map 2/3 Register (W0BMP23)

The window 0 bitmap value to palette map 2/3 register (W0BMP23) is shown in Figure 138 and described in Table 135.

Figure 138. Window 0 Bitmap Value to Palette Map 2/3 Register (W0BMP23)

15	8	7	0
PAL03		PAL02	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

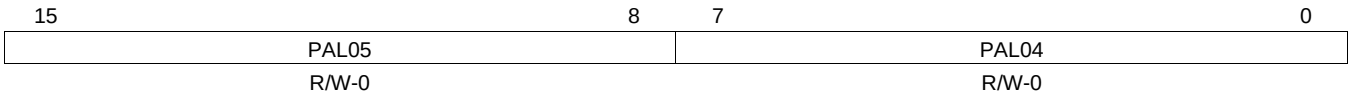
Table 135. Window 0 Bitmap Value to Palette Map 2/3 Register (W0BMP23) Field Descriptions

Bit	Field	Value	Description
15-8	PAL03	0-FFh	Palette address for bitmap value [3]-OSD window 0 [4-bit]
7-0	PAL02	0-FFh	Palette address for bitmap value [2]-OSD window 0 [4-bit]

6.3.41 Window 0 Bitmap Value to Palette Map 4/5 Register (W0BMP45)

The window 0 bitmap value to palette map 4/5 register (W0BMP45) is shown in Figure 139 and described in Table 136.

Figure 139. Window 0 Bitmap Value to Palette Map 4/5 Register (W0BMP45)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

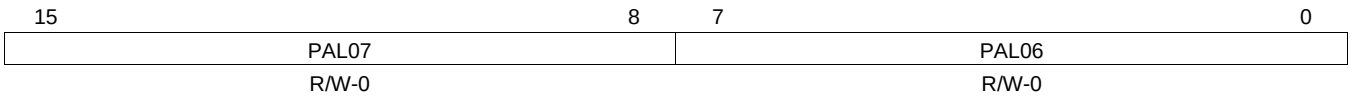
Table 136. Window 0 Bitmap Value to Palette Map 4/5 Register (W0BMP45) Field Descriptions

Bit	Field	Value	Description
15-8	PAL05	0-FFh	Palette address for bitmap value [5]-OSD window 0 [4-bit, 2-bit]
7-0	PAL04	0-FFh	Palette address for bitmap value [4]-OSD window 0 [4-bit]

6.3.42 Window 0 Bitmap Value to Palette Map 6/7 Register (W0BMP67)

The window 0 bitmap value to palette map 6/7 register (W0BMP67) is shown in Figure 140 and described in Table 137.

Figure 140. Window 0 Bitmap Value to Palette Map 6/7 Register (W0BMP67)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 137. Window 0 Bitmap Value to Palette Map 6/7 Register (W0BMP67) Field Descriptions

Bit	Field	Value	Description
15-8	PAL07	0-FFh	Palette address for bitmap value [7]-OSD window 0 [4-bit]
7-0	PAL06	0-FFh	Palette address for bitmap value [6]-OSD window 0 [4-bit]

6.3.43 Window 0 Bitmap Value to Palette Map 8/9 Register (W0BMP89)

The window 0 bitmap value to palette map 8/9 register (W0BMP89) is shown in Figure 141 and described in Table 138.

Figure 141. Window 0 Bitmap Value to Palette Map 8/9 Register (W0BMP89)

15	8	7	0
PAL09		PAL08	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 138. Window 0 Bitmap Value to Palette Map 8/9 Register (W0BMP89) Field Descriptions

Bit	Field	Value	Description
15-8	PAL09	0-FFh	Palette address for bitmap value [9]-OSD window 0 [4-bit]
7-0	PAL08	0-FFh	Palette address for bitmap value [8]-OSD window 0 [4-bit]

6.3.44 Window 0 Bitmap Value to Palette Map A/B Register (W0BMPAB)

The window 0 bitmap value to palette map A/B register (W0BMPAB) is shown in Figure 142 and described in Table 139.

Figure 142. Window 0 Bitmap Value to Palette Map A/B Register (W0BMPAB)

15	8	7	0
PAL11		PAL10	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 139. Window 0 Bitmap Value to Palette Map A/B Register (W0BMPAB) Field Descriptions

Bit	Field	Value	Description
15-8	PAL11	0-FFh	Palette address for bitmap value [B]-OSD window 0 [4-bit]
7-0	PAL10	0-FFh	Palette address for bitmap value [A]-OSD window 0 [4-bit, 2-bit]

6.3.45 Window 0 Bitmap Value to Palette Map C/D Register (W0BMPCD)

The window 0 bitmap value to palette map C/D register (W0BMPCD) is shown in Figure 143 and described in Table 140.

Figure 143. Window 0 Bitmap Value to Palette Map C/D Register (W0BMPCD)

15	8	7	0
PAL13		PAL12	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 140. Window 0 Bitmap Value to Palette Map C/D Register (W0BMPCD) Field Descriptions

Bit	Field	Value	Description
15-8	PAL13	0-FFh	Palette address for bitmap value [D]-OSD window 0 [4-bit]
7-0	PAL12	0-FFh	Palette address for bitmap value [Cx]-OSD window 0 [4-bit]

6.3.46 Window 0 Bitmap Value to Palette Map E/F Register (W0BMPEF)

The window 0 bitmap value to palette map E/F register (W0BMPEF) is shown in Figure 144 and described in Table 141.

Figure 144. Window 0 Bitmap Value to Palette Map E/F Register (W0BMPEF)

15	8	7	0
PAL15		PAL14	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

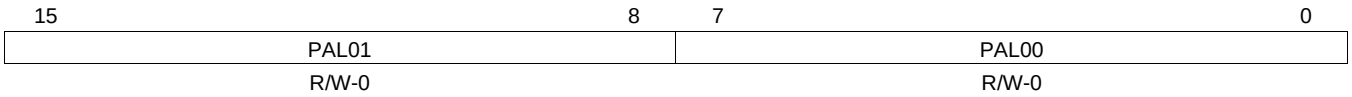
Table 141. Window 0 Bitmap Value to Palette Map E/F Register (W0BMPEF) Field Descriptions

Bit	Field	Value	Description
15-8	PAL15	0-FFh	Palette address for bitmap value [F1]-OSD window 0 [4-bit, 2-bit, 1-bit]
7-0	PAL14	0-FFh	Palette address for bitmap value [E]-OSD window 0 [4-bit]

6.3.47 Window 1 Bitmap Value to Palette Map 0/1 Register (W1BMP01)

The window 1 bitmap value to palette map 0/1 register (W1BMP01) is shown in Figure 145 and described in Table 142.

Figure 145. Window 1 Bitmap Value to Palette Map 0/1 Register (W1BMP01)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

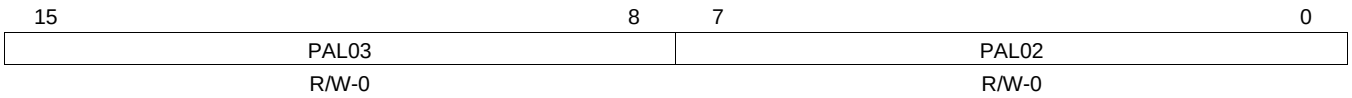
Table 142. Window 1 Bitmap Value to Palette Map 0/1 Register (W1BMP01) Field Descriptions

Bit	Field	Value	Description
15-8	PAL01	0-FFh	Palette address for bitmap value [1]-OSD window 1 [4-bit]
7-0	PAL00	0-FFh	Palette address for bitmap value [0]-OSD window 1 [4-bit, 2-bit, 1-bit]

6.3.48 Window 1 Bitmap Value to Palette Map 2/3 Register (W1BMP23)

The window 1 bitmap value to palette map 2/3 register (W1BMP23) is shown in Figure 146 and described in Table 143.

Figure 146. Window 1 Bitmap Value to Palette Map 2/3 Register (W1BMP23)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 143. Window 1 Bitmap Value to Palette Map 2/3 Register (W1BMP23) Field Descriptions

Bit	Field	Value	Description
15-8	PAL03	0-FFh	Palette address for bitmap value [3]-OSD window 1 [4-bit]
7-0	PAL02	0-FFh	Palette address for bitmap value [2]-OSD window 1 [4-bit]

6.3.49 Window 1 Bitmap Value to Palette Map 4/5 Register (W1BMP45)

The window 1 bitmap value to palette map 4/5 register (W1BMP45) is shown in Figure 147 and described in Table 144.

Figure 147. Window 1 Bitmap Value to Palette Map 4/5 Register (W1BMP45)

15	8	7	0
PAL05		PAL04	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 144. Window 1 Bitmap Value to Palette Map 4/5 Register (W1BMP45) Field Descriptions

Bit	Field	Value	Description
15-8	PAL05	0-FFh	Palette address for bitmap value [5]-OSD window 1 [4-bit, 2-bitt]
7-0	PAL04	0-FFh	Palette address for bitmap value [4]-OSD window 1 [4-bit]

6.3.50 Window 1 Bitmap Value to Palette Map 6/7 Register (W1BMP67)

The window 1 bitmap value to palette map 6/7 register (W1BMP67) is shown in Figure 148 and described in Table 145.

Figure 148. Window 1 Bitmap Value to Palette Map 6/7 Register (W1BMP67)

15	8	7	0
PAL07		PAL06	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

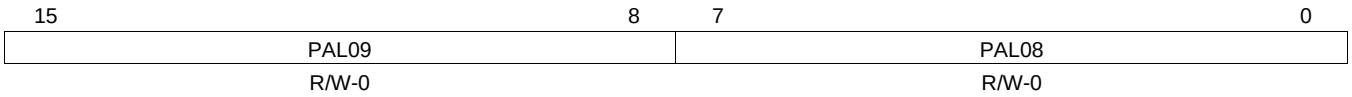
Table 145. Window 1 Bitmap Value to Palette Map 6/7 Register (W1BMP67) Field Descriptions

Bit	Field	Value	Description
15-8	PAL07	0-FFh	Palette address for bitmap value [7]-OSD window 1 [4-bit]
7-0	PAL06	0-FFh	Palette address for bitmap value [6]-OSD window 1 [4-bit]

6.3.51 Window 1 Bitmap Value to Palette Map 8/9 Register (W1BMP89)

The window 1 bitmap value to palette map 8/9 register (W1BMP89) is shown in Figure 149 and described in Table 146.

Figure 149. Window 1 Bitmap Value to Palette Map 8/9 Register (W1BMP89)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

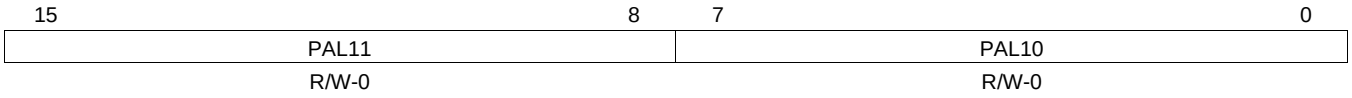
Table 146. Window 1 Bitmap Value to Palette Map 8/9 Register (W1BMP89) Field Descriptions

Bit	Field	Value	Description
15-8	PAL09	0-FFh	Palette address for bitmap value [9]-OSD window 1 [4-bit]
7-0	PAL08	0-FFh	Palette address for bitmap value [8]-OSD window 1 [4-bit]

6.3.52 Window 1 Bitmap Value to Palette Map A/B Register (W1BMPAB)

The window 1 bitmap value to palette map A/B register (W1BMPAB) is shown in Figure 150 and described in Table 147.

Figure 150. Window 1 Bitmap Value to Palette Map A/B Register (W1BMPAB)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 147. Window 1 Bitmap Value to Palette Map A/B Register (W1BMPAB) Field Descriptions

Bit	Field	Value	Description
15-8	PAL11	0-FFh	Palette address for bitmap value [B]-OSD window 1 [4-bit]
7-0	PAL10	0-FFh	Palette address for bitmap value [A]-OSD window 1 [4-bit, 2-bit]

6.3.53 Window 1 Bitmap Value to Palette Map C/D Register (W1BMPCD)

The window 1 bitmap value to palette map C/D register (W1BMPCD) is shown in Figure 151 and described in Table 148.

Figure 151. Window 1 Bitmap Value to Palette Map C/D Register (W1BMPCD)

15	8	7	0
PAL13		PAL12	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 148. Window 1 Bitmap Value to Palette Map C/D Register (W1BMPCD) Field Descriptions

Bit	Field	Value	Description
15-8	PAL13	0-FFh	Palette address for bitmap value [D]-OSD window 1 [4-bit]
7-0	PAL12	0-FFh	Palette address for bitmap value [C]-OSD window 1 [4-bit]

6.3.54 Window 1 Bitmap Value to Palette Map E/F Register (W1BMPEF)

The window 1 bitmap value to palette map E/F register (W1BMPEF) is shown in Figure 152 and described in Table 149.

Figure 152. Window 1 Bitmap Value to Palette Map E/F Register (W1BMPEF)

15	8	7	0
PAL15		PAL14	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 149. Window 1 Bitmap Value to Palette Map E/F Register (W1BMPEF) Field Descriptions

Bit	Field	Value	Description
15-8	PAL15	0-FFh	Palette address for bitmap value [F]-OSD window 1 [4-bit, 2-bit, 1-bit]
7-0	PAL14	0-FFh	Palette address for bitmap value [E]-OSD window 1 [4-bit]

6.3.55 Test Mode Register (VBNDRY)

The test mode register (VBNDRY) is shown in Figure 153 and described in Table 150.

Figure 153. Test Mode Register (VBNDRY)

15	8	7	4	3	2	1	0
TSTPATNCHROMA		Reserved		VFILINCMD	VBNDRY PRCSEN	TEST1	TEST0
R/W - 0		R-0		R/W-0	R/W - 0	R/W-0	R/W - 0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 150. Test Mode Register (VBNDRY) Field Descriptions

Bit	Field	Value	Description
15-8	TSTPATNCHROMA	0-FFh	Chrominance data input register for test mode.

Table 150. Test Mode Register (VBNDRY) Field Descriptions (continued)

Bit	Field	Value	Description
7 - 4	Reserved	0	Reserved
3	VFILINCMD		Vertical Filter Increment Mode Increment mode of address counter in vertical expansion of video or bitmap windows. Turn ON to have vertical filtering increment past the end of the vertical display area. In this case, additional data to be processed for vertical filtering should be stored in SDRAM, immediately following the display data. Turn OFF to have vertical filtering stop incrementing when it reaches the last display line. This is the DM320 equivalent mode
		0	Increment off (DM340-specific mode)
		1	Increment on (DM320 mode)
2	VBNDRYPRCSEN		Video boundary processing active Enables video boundary processing. In x9/8 or x6/5 expansion mode, with dual video windows displayed, specific boundary processing can be used.
		0	OFF (same as DM320; no specific processing)
		1	ON (with specific processing; DM340 custom mode)
1	TEST1		TI Test #1
		0	NORMAL - Normal mode
		1	RESET_ALL_REGS - All registers are loaded with default values
0	TEST0		TI Test #0
		0	NORMAL - Normal mode
		1	TEST_MODE - TI test mode

6.3.56 Extended Mode Register (EXTMODE)

The extended mode register (EXTMODE) is shown in Figure 154 and described in Table 151.

Figure 154. Extended Mode Register (EXTMODE)

15	14	13	12	11	10	9	8
EXPMDSEL	SCRNHEXP		SCRNVEXP	OSD1BLDCHR	OSDOBLDCHR	ATNOSD1EN	ATNOSD0EN
R/W-0	R/W-0		R/W-0	R/W-0	R/W-0	R/W-0	

7	6	5	4	3	2	1	0
OSDHRSZ15	VIDHRSZ15	ZMFILV1HEN	ZMFILV1VEN	ZMFILV0HEN	ZMFILV0VEN	EXPFILHEN	EXPFILVEN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 151. Extended Mode Register (EXTMODE) Field Descriptions

Bit	Field	Value	Description
15	EXPMDSEL		Expansion Filtering Mode Select Affects both horizontal or vertical directions. When enabled (filter after blending), SCRNHEXP and SCRNVEXP are used. If this bit is enabled, MODE.EF must be 0
		0	FILTER_BEFORE - filter before blend (DM320 mode)
		1	FILTER_AFTER - filter after blend (DM340 mode)

Table 151. Extended Mode Register (EXTMODE) Field Descriptions (continued)

Bit	Field	Value	Description
14 - 13	SCRNHEXP		Horizontal Expansion Mode This is only used if EXPMDSEL = 1 Note: Make sure that window start position and displayed size is same as configured value of each window if either expansion ration is enabled
		00	(X1) no expansion
		01	(X9_8) NTSC x9/8 horizontal expansion (VGA->D1)
		10	(X3_2) horizontal expansion (VGA->960 pixel LCD)
		11	RESERVED) same as 00
12	SCRNVEXP		Vertical Expansion Mode This is only used if EXPMDSEL = 1 Note: Make sure that window start position and displayed size is same as configured value of each window if either expansion ration is enabled
		0	(X1) no expansion
		1	(X6_5) NTSC->PAL x6/5 vertical expansion
11	OSD1BLDCHR		OSD Bitmap1 Blend Characteristics Enables pixel level blending between OSD Bitmap 1 and Video Windows using RGB888 mode 8_bits of extended data with blend factor (3-bit). Note: Enabling this mode has no effect unless: • OSDWIN1MD.OASW = 0 (not attribute) and • OSDWIN1MD.BMP1MD = 10 (RGB24) and • OSDWIN1MD.OACT1 = 1 (window is displayed) In all other cases, this configuration value here is ignored
		0	(GLOBAL_BLEND) global blend
		1	(PIXEL_BLEND) pixel level blend
10	OSD0BLDCHR		OSD Bitmap0 Blend Characteristics Enables pixel level blending between OSD Bitmap 0 and Video Windows using RGB888 mode 8-bits of extended data with blend factor (3-bit). Note: Enabling this mode has no effect unless: • OSDWIN0MD.BMP0MD = 10 (RGB24) and • OSDWIN0MD.OACT0 = 1 (window is displayed) In all other cases, this configuration value here is ignored
		0	(GLOBAL_BLEND) global blend
		1	(PIXEL_BLEND) pixel level blend
9	ATNOSD1EN		Attenuation Enable for REC601 for OSD Bitmap 1 Controls attenuation of data in bitmap window 1 based on REC601 limits. Note: This is only applied when RGB16 or RGB24 data is input (OSDWIN1MD.BMP1MD = 01 or 10)
		0	(NORMAL) Normal levels (Y 0-255, Cr 0-255, Cb 0-255)
		1	(ATTENUATED) Attenuated levels (Y 16-235, Cr 16-240, Cb 16-240)
8	ATNOSD0EN		Attenuation Enable for REC601 for OSD Bitmap 0 Controls attenuation of data in bitmap window 0 based on REC601 limits. Note: This is only applied when RGB16 or RGB24 data is input (OSDWIN0MD.BMP0MD = 01 or 10)
		0	(NORMAL) Normal levels (Y 0-255, Cr 0-255, Cb 0-255)
		1	(ATTENUATED) Attenuated levels (Y 16-235, Cr 16-240, Cb 16-240)
7	OSDHRSZ15		OSD Bitmap Window Horizontal 1.5x Expansion This function is to enable a 640 pixel width image to be displayed as a 960 pixel wide image; i.e., VGA to specific LCD conversion. This expansion has no filtering; it just executes a pixel copy once per 3 pixels. Notice that target window of this register has to be higher priority if window 0 and window 1 are configured to be duplicated. Note: This setting only takes effect if: • MODE.OHRSZ = 0 (no other horizontal expansion) and • EXTMODE.EXPMDSEL = 0 (filter before blend)
		0	(HRSZ_NORMAL) Normal mode, depends on MODE.OHRSZ
		1	(HRSZ_1P5) horizontal x1.5 expansion

Table 151. Extended Mode Register (EXTMODE) Field Descriptions (continued)

Bit	Field	Value	Description
6	VIDHRSZ15		OSD Video Window Horizontal 1.5x Expansion This function is to enable a 640 pixel width image to be displayed as a 960 pixel wide image; i.e., VGA to specific LCD conversion. User can perform 2-tap filtering with user defined coefficients if MODE.EF = 1. Notice that target window of this register has to be higher priority if window 0 and window 1 are configured to be duplicated. Note: This setting only takes effect if: • MODE.VHRSZ = 0 (no other horizontal expansion) and • EXTMODE.EXPMDSEL = 0 (filter before blend)
		0	(HRSZ_NORMAL) Normal mode, depends on MODE.VHRSZ
		1	(HRSZ_1P5) horizontal x1.5 expansion.
5	ZMFILV1HEN		Video Window 1 Horizontal Zoom Filter If this zoom filter is active, interpolation based on 2-tap filter with 1:1 coefficient is carried out. Note: this control is available only if: - MODE.EF = 0 (no other expansion filtering) - VIDWINMD.ACT1 = 1 (VidWin1 is displayed)
		0	(OFF) No filter
		1	(ON) Filter active for horizontal direction
4	ZMFILV1VEN		Video Window 1 Vertical Zoom Filter If this zoom filter is active, interpolation based on 2-tap filter with 1:1 coefficient is carried out. Note: this control is available only if: • MODE.EF = 0 (no other expansion filtering) • EXTMODE.EXPFILVEN = 0 (x6/5 vertical filter disabled) • VIDWINMD.ACT1 = 1 (VidWin1 is displayed)
		0	(OFF) No filter
		1	ON) Filter active for vertical direction
3	ZMFILV0HEN		Video Window 0 Horizontal Zoom Filter If this zoom filter is active, interpolation based on 2-tap filter with 1:1 coefficient is carried out. Note: this control is available only if: • MODE.EF = 0 (no other expansion filtering) • VIDWINMD.ACT0 = 0 (VidWin0 is displayed)
		0	(OFF) No filter
		1	(ON) Filter active for horizontal direction
2	ZMFILV0VEN		Video Window 0 Vertical Zoom Filter If this zoom filter is active, interpolation based on 2-tap filter with 1:1 coefficient is carried out. Note: this control is available only if: • MODE.EF = 0 (no other expansion filtering) • EXTMODE.EXPFILVEN = 0 (x6/5 vertical filter disabled) • VIDWINMD.ACT0 = 0 (VidWin0 is displayed)
		0	(OFF) No filter
		1	(ON) Filter active for vertical direction
1	EXPFILHEN		Horizontal Expansion Filter Enable This setting is only active if video window 0 or video window 1 is active. If the expansion filter is active, interpolation based on a 2-tap filter with coefficients in HW is carried out. If inactive, no filtering is carried out (just pixel copy is available). This function is available only for video window, and targeted video window has to be higher priority if window 0 and window 1 are to be duplicated. This control register configures only horizontal filtering, so this configured value is available only when MODE.EF = 0 (no expansion filtering). Additionally, the configuration of this register bit is available only case that any expansion (x9/8(h) and x3/2(h)) works.
		0	(OFF) Expansion Filter Off
		1	(ON) Expansion Filter On

Table 151. Extended Mode Register (EXTMODE) Field Descriptions (continued)

Bit	Field	Value	Description
0	EXPFILVEN		Vertical Expansion Filter Enable This setting is only active if video window 0 or video window 1 is active. If the expansion filter is active, interpolation based on a 2-tap filter with coefficients in HW is carried out. If inactive, no filtering is carried out (just pixel copy is available). This function is available only for video window, and targeted video window has to be higher priority if window 0 and window 1 are to be duplicated. This control register configures only vertical filtering, so this configured value is available only when MODE.EF = 0 (no expansion filtering). Additionally, the configuration of this register bit is available only case that any expansion (x6/5(v)) works. 0:(OFF) Expansion Filter Off 1:(ON) Expansion Filter On
		0	(OFF) Expansion Filter Off
		1	(ON) Expansion Filter On

6.3.57 Miscellaneous Control Register (MISCCTL)

The miscellaneous control register (MISCCTL) is shown in Figure 155 and described in Table 152.

Figure 155. Miscellaneous Control Register (MISCCTL)

15 8	7	6	5	4	3	2 1 0
Reserved	FIELD_ID	DMANG	Reserved	RSEL	CPBSY	Reserved
R-0	R/W-0	R/W-0	R-0	R/W-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 152. Miscellaneous Control Register (MISCCTL) Field Descriptions

Bit	Field	Value	Description
15-8	Reserved	0	Reserved
7	FIELD_ID		Video window RGB mode enable.
		0	Top field (ID=0)
		1	Bottom field (ID=1)
6	DMANG		OSD DMA Status. Write 1 to this field after an error
		0	No error
		1	Error, OSD bandwidth limitation
5	Reserved	0	Reserved
4	RSEL		CLUT ROM selection.
		0	CLUT0
		1	CLUT1
3	CPBSY		CLUT Write Busy. Used when writing CLUT data to RAM.
		0	Not busy, okay to write
		1	Busy, do not write
2-0	Reserved	0	Reserved

6.3.58 CLUT RAMYCB Setup Register (CLUTRAMYCB)

The CLUT RAMYCB setup register (CLUTRAMYCB) is shown in Figure 156 and described in Table 153.

Figure 156. CLUT RAMYCB Setup Register (CLUTRAMYCB)

15	8	7	0
Y		CB	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 153. CLUT RAMYCB Setup Register (CLUTRAMYCB) Field Descriptions

Bit	Field	Value	Description
15-8	Y	0-FFh	Write data (Y) into built-in CLUT RAM. Note: It is necessary to write into CLUTRAMYCB before CLUTRAMCR
7-0	CB	0-FFh	Write data (Cb) into built-in CLUT RAM. Note: It is necessary to write into CLUTRAMYCB before CLUTRAMCR

6.3.59 CLUT RAMCR Setup Register (CLUTRAMCR)

The CLUT RAMCR setup register (CLUTRAMCR) is shown in Figure 157 and described in Table 154.

Figure 157. CLUT RAMCR Setup Register (CLUTRAMCR)

15	8	7	0
CR		CADDR	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

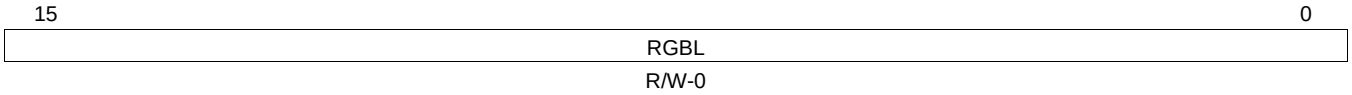
Table 154. CLUT RAMCR Setup Register (CLUTRAMCR) Field Descriptions

Bit	Field	Value	Description
15-8	CR	0-FFh	Write data (Cr) into built-in CLUT RAM. Note: It is necessary to write into CLUTRAMYCB before CLUTRAMCR
7-0	CADDR	0-FFh	CLUT write pallette address. When updating CLUT_RAM: • verify CPBSY=0 in MISCCTL and • write CLUTRAMYCB before CLUTRAMCR

6.3.60 Transparency Color Code - Lower Register (TRANSPVALL)

The transparency color code - lower register (TRANSPVALL) is shown in Figure 158 and described in Table 155.

Figure 158. Transparency Color Code - Lower Register (TRANSPVALL)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

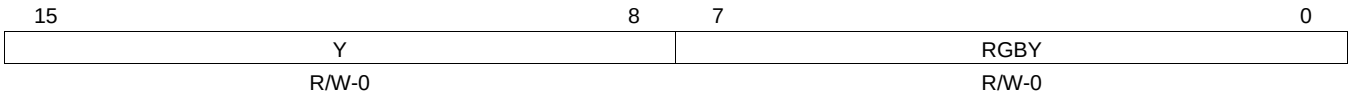
Table 155. Transparency Color Code - Lower Register (TRANSPVALL) Field Descriptions

Bit	Field	Value	Description
15-0	RGBL	0-FFFFh	RGB Transparency Value (lower 16) Transparent color code when RGB565 or RGB888 modes used in a bitmap window. • If RGB565 mode, user configures RGB565 transparent color code • If RGB888 mode, user configures lower 16-bits of RGB888 transparent color code

6.3.61 Transparency Color Code - Upper Register (TRANSPVALU)

The transparency color code - upper register (TRANSPVALU) is shown in Figure 159 and described in Table 156.

Figure 159. Transparency Color Code - Upper Register (TRANSPVALU)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

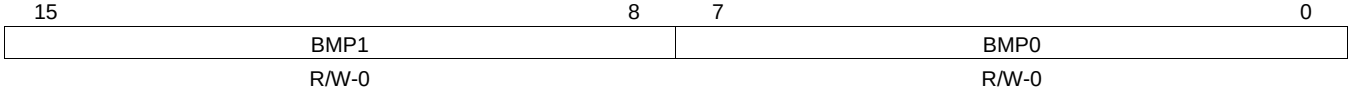
Table 156. Transparency Color Code - Upper Register (TRANSPVALU) Field Descriptions

Bit	Field	Value	Description
15 - 8	Y	0-FFh	Luma Transparency Value Transparent Luma color code when YC mode used in a bitmap window.
7 - 0	RGBU	0-FFh	RGB Transparency Value (upper 8) Transparent color code when RGB888 mode used in a bitmap window. • If RGB888 mode, user configures upper 8-bits of RGB888 transparent color code

6.3.62 Transparent Index Code for Bitmaps Register (TRANSPBMPIDX)

The ping-pong video window 0 address register (PPVWIN0ADR) is shown in Figure 160 and described in Table 157.

Figure 160. Transparent Index Code for Bitmaps Register (TRANSPBMPIDX)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 157. Transparent Index Code for Bitmaps Register (TRANSPBMPIDX) Field Descriptions

Bit	Field	Value	Description
15 - 8	BMP1	0-FFh	OSD Bitmap 1 Transparent Value Bitmap value for transparent color for 1/2/4/8-bit modes of bitmap window 1. Any pixel matching the value configured here is treated as transparent. , the pixel is blended to the window in back plane with blend factor configured as global value of bitmap window 1. The bit width specified here must match the bit depth configured for the window (example): • 1-bit bitmap mode, bit[0] is evaluated • 2-bit bitmap mode, bits[1:0] are evaluated • 4-bit bitmap mode, bits[3:0] are evaluated
7 - 0	BMP0	0-FFh	OSD Bitmap 0 Transparent Value Bitmap value for transparent color for 1/2/4/8-bit modes of bitmap window 0. Any pixel matching the value configured here is treated as transparent. , the pixel is blended to the window in back plane with blend factor configured as global value of bitmap window 0. The bit width specified here must match the bit depth configured for the window (example): • 1-bit bitmap mode, bit[0] is evaluated • 2-bit bitmap mode, bits[1:0] are evaluated • 4-bit bitmap mode, bits[3:0] are evaluated

6.4 Video Encoder/Digital LCD Subsystem (VENC) Registers

Table 158 lists the memory-mapped registers for the video encoder/digital LCD (VENC). See the device-specific data manual for the memory address of these registers. All other register offset addresses not listed in Table 158 should be considered as reserved locations and the register contents should not be modified.

Table 158. Video Encoder/Digital LCD (VENC) Registers

Offset	Acronym	Register Description	Section
0400h	VMOD	Video Mode Register	Section 6.4.1
0404h	VIDCTL	Video Interface I/O Control Register	Section 6.4.2
0408h	VDPRO	Video Data Processing Register	Section 6.4.3
040Ch	SYNCCTL	Sync Control Register	Section 6.4.4
0410h	HSPLS	Horizontal Sync Pulse Width Register	Section 6.4.5
0414h	VSPLS	Vertical Sync Pulse Width Register	Section 6.4.6
0418h	HINT	Horizontal Interval Register	Section 6.4.7
041Ch	HSTART	Horizontal Valid Data Start Position Register	Section 6.4.8
0420h	HVALID	Horizontal Data Valid Range Register	Section 6.4.9
0424h	VINT	Vertical Interval Register	Section 6.4.10
0428h	VSTART	Vertical Valid Data Start Position Register	Section 6.4.11
042Ch	VVALID	Vertical Data Valid Range Register	Section 6.4.12
0430h	HSDLY	Horizontal Sync Delay Register	Section 6.4.13
0434h	VSDLY	Vertical Sync Delay Register	Section 6.4.14
0438h	YCCTL	YCbCr Control Register	Section 6.4.15
043Ch	RGBCTL	RGB Control Register	Section 6.4.16
0440h	RGBCLP	RGB Level Clipping Register	Section 6.4.17
0444h	LINECTL	Line Identification Control Register	Section 6.4.18
0448h	CULLLINE	Culling Line Control Register	Section 6.4.19
044Ch	LCDOUT	LCD Output Signal Control Register	Section 6.4.20
0450h	BRTS	Brightness Start Position Signal Control Register	Section 6.4.21
0454h	BRTW	Brightness Width Signal Control Register	Section 6.4.22
0458h	ACCTL	LCD_AC Signal Control Register	Section 6.4.23
045Ch	PWMP	PWM Start Position Signal Control Register	Section 6.4.24
0460h	PWMW	PWM Width Signal Control Register	Section 6.4.25
0464h	DCLKCTL	DCLK Control Register	Section 6.4.26
0468h	DCLKPTN0	DCLK Pattern 0 Register	Section 6.4.27
046Ch	DCLKPTN1	DCLK Pattern 1 Register	Section 6.4.27
0470h	DCLKPTN2	DCLK Pattern 2 Register	Section 6.4.27
0474h	DCLKPTN3	DCLK Pattern 3 Register	Section 6.4.27
0478h	DCLKPTN0A	DCLK Auxiliary Pattern 0 Register	Section 6.4.28
047Ch	DCLKPTN1A	DCLK Auxiliary Pattern 1 Register	Section 6.4.28
0480h	DCLKPTN2A	DCLK Auxiliary Pattern 2 Register	Section 6.4.28
0484h	DCLKPTN3A	DCLK Auxiliary Pattern 3 Register	Section 6.4.28
0488h	DCLKHS	Horizontal DCLK Mask Start Register	Section 6.4.29
048Ch	DCLKHSA	Horizontal Auxiliary DCLK Mask Start Register	Section 6.4.30
0490h	DCLKHR	Horizontal DCLK Mask Range Register	Section 6.4.31
0494h	DCLKVS	Vertical DCLK Mask Start Register	Section 6.4.32
0498h	DCLKVR	Vertical DCLK Mask Range Register	Section 6.4.33
049Ch	CAPCTL	Caption Control Register	Section 6.4.34

Table 158. Video Encoder/Digital LCD (VENC) Registers (continued)

Offset	Acronym	Register Description	Section
04A0h	CAPDO	Caption Data Odd Field Register	Section 6.4.35
04A4h	CAPDE	Caption Data Even Field Register	Section 6.4.36
04A8h	ATR0	Video Attribute Data 0 Register	Section 6.4.37
04ACh	ATR1	Video Attribute Data 1 Register	Section 6.4.38
04B0h	ATR2	Video Attribute Data 2 Register	Section 6.4.39
04B4h	RSV0	Reserved	
04B8h	VSTAT	Video Status Register	Section 6.4.40
04BCh	RAMADR	GCP/FRC Table RAM Address	
04C0	RAMPORT	GCP/FRC Table RAM Data Port	
04C4h	DACTST	DAC Test Register	Section 6.4.43
04C8h	YCOLVL	YOUT and COUT Levels Register	Section 6.4.44
04CCh	SCPROG	Sub-Carrier Programming Register	Section 6.4.45
04D0h	RSV1	Reserved	
04D4h	RSV2	Reserved	
04D8h	RSV3	Reserved	
04DCh	CVBS	Composite Mode Register	Section 6.4.46
04E0h	RSV4	Reserved	
04E4h	ETMG0	CVBS Timing Control 0 Register	Section 6.4.47
04E8h	ETMG1	CVBS Timing Control 1 Register	Section 6.4.48
04ECh	RSV5	Reserved	
04F0h	RSV6	Reserved	
04F4h	RSV7	Reserved	
04F8h	RSV8	Reserved	
04FCh	RSV9	Reserved	
0500h	RSV10	Reserved	
0504h	RSV11	Reserved	
0508h	RSV12	Reserved	
050Ch	RSV13	Reserved	
0510h	RSV14	Reserved	
0514h	DRGBX0	Digital RGB Matrix 0 Register	Section 6.4.49
0518h	DRGBX1	Digital RGB Matrix 1 Register	Section 6.4.50
051Ch	DRGBX2	Digital RGB Matrix 2 Register	Section 6.4.51
0520h	DRGBX3	Digital RGB Matrix 3 Register	Section 6.4.52
0524h	DRGBX4	Digital RGB Matrix 4 Register	Section 6.4.53
0528h	VSTARTA	Vertical Data Valid Start Position Register (for Even Field)	Section 6.4.54
052Ch	OSDCLK0	OSD Clock Control 0 Register	Section 6.4.55
0530h	OSDCLK1	OSD Clock Control 1 Register	Section 6.4.56
0534h	HVLDCL0	Horizontal Valid Culling Control 0 Register	Section 6.4.57
0538h	HVLDCL1	Horizontal Valid Culling Control 1 Register	Section 6.4.58
053Ch	OSDHADV	OSD Horizontal Sync Advance Register	Section 6.4.59
0540h	CLKCTL	Clock Control	Section 6.4.60
0544h	GAMCTL	Enable Gamma Correction	Section 6.4.61

Note: The upper 16 bits of these registers are not shown; they are reserved.

6.4.1 Video Mode Register (VMOD)

The video mode register (VMOD) is shown in Figure 161 and described in Table 159.

Figure 161. Video Mode Register (VMOD)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD		VDMD		ITLCL	ITLC	NSIT	Rsvd	TVTYP		SLAVE	VMD	BLNK	Rsvd	VIE	VENC
R/W-0				R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 159. Video Mode Register (VMOD) Field Descriptions

Bit	Field	Value	Description
15-14	Reserved	0	Reserved
13-12	VDMD	0-Fh	Digital video output mode.
		0	YCbCr parallel 16 bit
		1h	YCbCr serial 8 bit
		2h	RGB666 parallel 18 bit
		3h	RGB8 serial 8 bit
11	ITLCL		Non-interlace line number select. Effective in standard SDTV non-interlace mode (VMD = 0, HDMD = 0, and ITLC = 1).
		0	262 line (NTSC) or 312 line (PAL)
		1	263 line (NTSC) or 313 line (PAL)
10	ITLC		Interlaced Scan Mode Enable. Effective in standard SDTV mode (VMD = 0 and HDMD = 0).
		0	Interlace
		1	Non-interlace
9	NSIT		Nonstandard interlace mode. Effective in non-standard mode (VMD = 1).
		0	Progressive
		1	Interlace
8	Reserved	0	Reserved
7-6	TVTYP	0-3h	TV Format Type Select. Effective in standard mode (VMD = 0).
			In SDTV mode (HDMD = 0):
		0	NTSC
		1h	PAL
		2h-3h	Reserved
			In HDTV mode (HDMD = 1):
		0	525P
		1h	625P
		2h-3h	Reserved
5	SLAVE		Master-slave select.
		0	Master mode
		1	Slave mode
4	VMD		Video timing.
		0	NTSC/PAL timing
		1	Not NTSC/PAL timing
3	BLNK		Blanking enable. Sync signal and color burst are still output.
		0	Normal
		1	Force blanking
2	Reserved	0	Reserved

Table 159. Video Mode Register (VMOD) Field Descriptions (continued)

Bit	Field	Value	Description
1	VIE		Composite Analog Output Enable.
		0	Fixed low-level output
		1	Normal composite output
0	VENC		Video Encoder Enable.
		0	Disable
		1	Enable

6.4.2 Video Interface I/O Control Register (VIDCTL)

The video interface I/O control register (VIDCTL) is shown in Figure 162 and described in Table 160.

Figure 162. Video Interface I/O Control Register (VIDCTL)

15	14	13	12	11 9	8	7 6	5 4	3	2	1	0
Rsvd	VCLKP	VCLKE	VCLKZ	Reserved	SYDIR	Reserved	DOMD	YCSWAP	YCOL	YCOMD	YCDIR
R-0	R/W-0	R/W-0	R/W-1	R-0	R/W-1	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 160. Video Interface I/O Control Register (VIDCTL) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved
14	VCLKP		VCLK output polarity.
		0	Non-inverse
		1	Inverse
13	VCLKE		VCLK output enable. Setting to 1 outputs DCLK from VCLK pin. When 0 VCLKP (polarity control) is still available.
		0	Off
		1	On
12	VCLKZ		VCLK pin output enable.
		0	Output
		1	High impedance
11-9	Reserved	0	Reserved
8	SYDIR		Horizontal/Vertical Sync pin I/O control. Set to 1 when external syncs are input.
		0	Output
		1	Input
7-6	Reserved	0	Reserved
5-4	DOMD	0-3h	Digital data output mode.
		0	Normal output
		1h	Inverse output
		2h	Low-level output
		3h	High-level output
3	YCSWAP		Swaps YOUT/COUT pins. Interchanges the output data of YOUT and COUT.
		0	Normal output
		1	Interchange YOUT and COUT
2	YCOL		YOUT/COUT pin output level. Setting DC out option will output the value in the YCOLVL register on YOUT/COUT pins. Effective only when YOUT/COUT pin is set as output.
		0	Normal output
		1	DC level output
1	YCOMD		YC Output Mode (Input Through Mode) Allows direct output of the data from the YIN/CIN pins on the YOUT/COUT pins
		0	Digital video output
		1	YIN / CIN input through
0	YCDIR		YOUT / COUT I/O Direction Allows use of YOUT/COUT pins as data input pin for CCDC
		0	Output
		1	Input

6.4.3 Video Data Processing Register (VDPRO)

The video data processing register (VDPRO) is shown in Figure 163 and described in Table 161.

Figure 163. Video Data Processing Register (VDPRO)

15 14	13 12	11	10	9	8	7	6	5	4	3 2	1	0
PFLTC	PFLTY	PFLTR	Reserved	CBTYP	CBMD	Reserved	ATRGB	ATYCC	ATCOM	Reserved	CUPS	YUPS
R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 161. Video Data Processing Register (VDPRO) Field Descriptions

Bit	Field	Value	Description
15-14	PFLTC	0-3h	C prefilter select Note: when PFLTR and PFLTC are 1, use PFLTY to 1 to adjust the delay between Y and C.
		0	No filter
		1h	1+1
		2h	1+2+1
		3h	Reserved
13-12	PFLTY		Y prefilter select
		0	No filter
		1h	1+1
		2h	1+2+1
		3h	Reserved
11	PFLTR		Prefilter sampling frequency
		0	ENC clock / 2
		1	ENC clock
10	Reserved	0	Reserved
9	CBTYP		Color bar type
		0	75%
		1	100%
8	CBMD		Color bar mode
		0	Normal output
		1	Color bar output
7	Reserved	0	Reserved
6	ATRGB		Input video: attenuation control for RGB
		0	No Attenuation
		1	0-255 => REC601 specified level
5	ATYCC		Input video. attenuation control for YCbCr
		0	No Attenuation
		1	0-255 => REC601 specified level
4	ATCOM		Input video: attenuation control for composite
		0	No Attenuation
		1	0-255 => REC601 specified level
3-2	Reserved		Reserved
1	CUPS		Chroma signal up-sampling enable
		0	Off
		1	On

Table 161. Video Data Processing Register (VDPRO) Field Descriptions (continued)

Bit	Field	Value	Description
0	YUPS		Y signal up-sampling enable
		0	Off
		1	On

6.4.4 Sync Control Register (SYNCCTL)

The sync control register (SYNCCTL) is shown in Figure 164 and described in Table 162.

Figure 164. Sync Control Register (SYNCCTL)

15	14	13 12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	OVD	EXFMD	EXFIV	EXSYNC	EXVIV	EXHIV	CSP	CSE	SYSW	VSYNCS	VPL	HPL	SYEV	SYEH
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 162. Sync Control Register (SYNCCTL) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved
14	OVD		OSD vsync delay
		0	No delay
		1	Delay 0.5H
13-12	EXFMD	0-3h	External field detection mode: effective in slave operation (SLAVE=1).
		0	Latch external field at external VD rising edge
		1h	Use raw external field
		2h	Use external vsync as field ID
		3h	Detect external vsync phase
11	EXFIV		External field input inversion. Effective in slave operation.
		0	Non-inverse
		1	Inverse
10	EXSYNC		External sync select
		0	HSYNC/VSYNC pin
		1	CCD sync signal
9	EXVIV		External vertical sync input polarity
		0	Active H
		1	Active L
8	EXHIV		External horizontal sync input polarity
		0	Active H
		1	Active L
7	CSP		Composite signal output polarity: specifies composite signal output polarity from COUT3 pin in YCC8 or RGB8 mode.
		0	Active H
		1	Active L
6	CSE		Composite signal output enable. Specifies composite signal output polarity from COUT3 pin in YCC8 or RGB8 mode.
		0	Off
		1	On
5	SYSW		Output sync select. Applicable to standard mode only. Setting the SYSW to 1 in standard mode outputs the pulse width that the SYNCPLS register processes as an output sync signal.
		0	Normal
		1	Sync pulse width processing mode
4	VSYNCS		Vertical sync output signal
		0	Vertical sync signal
		1	Composite sync signal

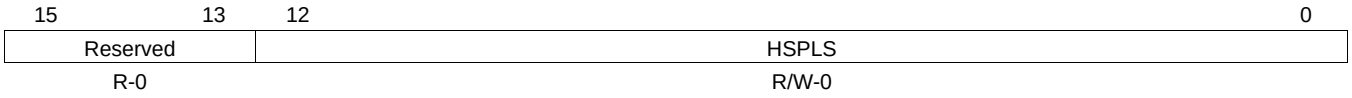
Table 162. Sync Control Register (SYNCCTL) Field Descriptions (continued)

Bit	Field	Value	Description
3	VPL		Vertical sync output polarity
		0	Active H
		1	Active L
2	HPL		Horizontal sync output polarity.
		0	Active H
		1	Active L
1	SYEV		Vertical sync output enable: The output turns ON when the SYEV is set to 1, and the signal that the VSSW selects is output from the VSYNC pin. Setting to 0 outputs an inactive level that VPL determines.
		0	Off
		1	On
0	SYEH		Horizontal sync output enable: The output turns ON when SYEH is set to 1, and the signal that the VSSW selects is output from HSYNC pin. Setting to 0 outputs inactive level that HPL determines.
		0	Off
		1	On

6.4.5 Horizontal Sync Pulse Width Register (HSPLS)

The horizontal sync pulse width register (HSPLS) is shown in Figure 165 and described in Table 163.

Figure 165. Horizontal Sync Pulse Width Register (HSPLS)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

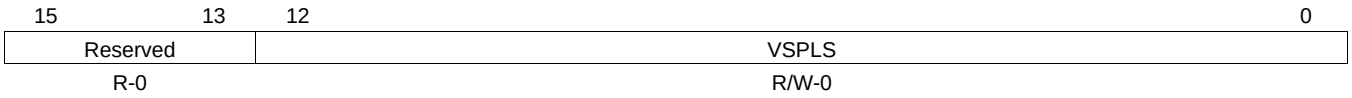
Table 163. Horizontal Sync Pulse Width Register (HSPLS) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12-0	HSPLS	0-1FFFh	Horizontal sync pulse width. Sets the pulse width of horizontal sync output from HSYNC pin in ENC clock. Effective in non-standard mode or sync processing mode (SYSW = 1).

6.4.6 Vertical Sync Pulse Width Register (VSPLS)

The vertical sync pulse width register (VSPLS) is shown in Figure 166 and described in Table 164.

Figure 166. Vertical Sync Pulse Width Register (VSPLS)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 164. Vertical Sync Pulse Width Register (VSPLS) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12-0	VSPLS	0-1FFFh	Vertical sync pulse width. Sets the pulse width of vertical sync output from VSYNC pin in lines. -Effective in non-standard mode or sync processing mode (SYSW = 1).

6.4.7 Horizontal Interval Register (HINT)

The horizontal interval register (HINT) is shown in Figure 167 and described in Table 165.

Figure 167. Horizontal Interval Register (HINT)

15 13	12 0
Reserved	HINT
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 165. Horizontal Interval Register (HINT) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12-0	HINT	0-1FFFh	Horizontal interval Effective in non-standard mode. Specify the number of ENC clocks. If ENC clock / 2 is used as OSD clock, ensure that even value is specified. The interval is HINT + 1.

6.4.8 Horizontal Valid Data Start Position Register (HSTART)

The horizontal valid data start position register (HSTART) is shown in Figure 168 and described in Table 166.

Figure 168. Horizontal Valid Data Start Position Register (HSTART)

15 13	12 0
Reserved	HSTART
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 166. Horizontal Valid Data Start Position Register (HSTART) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12-0	HSTART	0-1FFFh	Horizontal valid data start position Specify the number of ENC clocks from the start of the horizontal sync. LCD_OE is asserted at the position specified here and the data output starts.

6.4.9 Horizontal Data Valid Range Register (HVALID)

The horizontal data valid range register (HVALID) is shown in Figure 169 and described in Table 167.

Figure 169. Horizontal Data Valid Range Register (HVALID)

15 13	12 0
Reserved	HVALID
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 167. Horizontal Data Valid Range Register (HVALID) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12-0	HVALID	0-1FFFh	Horizontal data valid range Specify the number of ENC clocks. The LCD_OE is asserted during the period specified here and valid data is output. The data outside of the valid range is output in L.

6.4.10 Vertical Interval Register (VINT)

The vertical interval register (VINT) is shown in Figure 170 and described in Table 168.

Figure 170. Vertical Interval Register (VINT)

15 13	12 0
Reserved	VINT
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

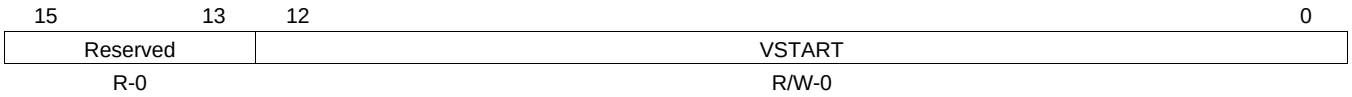
Table 168. Vertical Interval Register (VINT) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12-0	VINT	0-1FFFh	Vertical interval (number of lines): effective in non-standard mode. The interval is represented by VINT + 1.

6.4.11 Vertical Valid Data Start Position Register (VSTART)

The vertical valid data start position register (VSTART) is shown in Figure 171 and described in Table 169.

Figure 171. Vertical Valid Data Start Position Register (VSTART)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

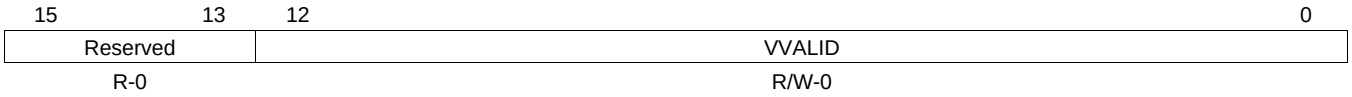
Table 169. Vertical Valid Data Start Position Register (VSTART) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12-0	VSTART	0-1FFFh	Vertical valid data start position: specify the number of lines.

6.4.12 Vertical Data Valid Range Register (VVALID)

The vertical data valid range register (VVALID) is shown in Figure 172 and described in Table 170.

Figure 172. Vertical Data Valid Range Register (VVALID)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 170. Vertical Data Valid Range Register (VVALID) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12-0	VVALID	0-1FFFh	Vertical data valid range: specify the number of lines.

6.4.13 Horizontal Sync Delay Register (HSDLY)

The horizontal sync delay register (HSDLY) is shown in Figure 173 and described in Table 171.

Figure 173. Horizontal Sync Delay Register (HSDLY)

15 13	12 0
Reserved	HSDLY
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 171. Horizontal Sync Delay Register (HSDLY) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12-0	HSDLY	0-1FFFh	Output delay of the horizontal sync signal. This delays the HSYNC signal by the ENC clock.

6.4.14 Vertical Sync Delay Register (VSDLY)

The vertical sync delay register (VSDLY) is shown in Figure 174 and described in Table 172.

Figure 174. Vertical Sync Delay Register (VSDLY)

15 13	12 0
Reserved	VSDLY
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 172. Vertical Sync Delay Register (VSDLY) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12-0	VSDLY	0-1FFFh	Output delay of vertical sync signal. This delays the VSYNC signal by ENC clock.

6.4.15 YCbCr Control Register (YCCTL)

The YCbCr control register (YCCTL) is shown in Figure 175 and described in Table 173.

Figure 175. YCbCr Control Register (YCCTL)

15	5	4	3	2	1	0
Reserved		CHM	YCP		Rsvd	R656
R-0		R/W-0	R/W-0		R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 173. YCbCr Control Register (YCCTL) Field Descriptions

Bit	Field	Value	Description
15-5	Reserved	0	Reserved
4	CHM		Chroma output mode. Effective in YCC16/YCC8 mode.
		0	Immediate sampling
		1	Latch chroma at first pixel
3-2	YCP	0-3h	YC output order. Operation based on YCC mode.
		0	YCC16 mode-CbCr
		1h	YCC16 mode-CrCb
		2h-3h	Reserved
		0	YCC8 mode-Cb-Y-Cr-Y
		1h	YCC8 mode-Y-Cr-Y-Cb
		2h	YCC8 mode-Cr-Y-Cb-Y
		3h	YCC8 mode-Y-Cb-Y-Cr
1	Reserved	0	Reserved
0	R656		REC656 mode: This is in ITU-R BT.656 format and is effective when the OSD clock runs at ENC clock/2.
		0	Normal
		1	REC656 mode

6.4.16 RGB Control Register (RGBCTL)

The RGB control register (RGBCTL) is shown in Figure 176 and described in Table 174.

Figure 176. RGB Control Register (RGBCTL)

15	14	13	12	11	10	9 8	7	6 4	3	2 0
RGBLAT	Rsrvd	IRSWP	IR9	IRONM	DFLTR	DFLTS	Rsvd	RGBEF	Rsvd	RGBOF
R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 174. RGB Control Register (RGBCTL) Field Descriptions

Bit	Field	Value	Description
15	RGBLAT		RGB latch setting Set 1 to latch and output the data input in serial RGB output. This is set when data with the same pixel are output serially.
		0	Normal output
		1	Latch mode
14	Reserved	0	Reserved
13	IRSWP		Swap order of data output in IronMan mode Effective only IRONM=1
		0	Normal
		1	Data swap
12	IR9		IronMan 9-bit mode Effective only IRONM=1. When 1, 24-bit RGB data (upper 6-bits of each color) is serially output on 9-bit data bus. The output format is the first is R[7:2] & G[7:5] and the second is G[4:2] & B[7:2]. This order can be swapped by IRSWP register.
		0	8-bit
		1	9-bit
11	IRONM		Iron-man type RGB output Effective in SRGB mode
		0	Normal
		1	Iron-man type
10	DFLTR		RGB LPF sampling frequency. Effective in all digital modes with RGB output.
		0	ENC clock / 2
		1	ENC clock
9-8	DFLTS	0-3h	RGB LPF select. Effective in all digital modes with RGB output.
		0	No filter
		1h	3 tap: 1+2+1
		2h	7 tap: 1+2+4+2+1
		3h	Reserved
7	Reserved	0	Reserved
6 - 4	RGBEF		RGB Output Order for Even Fields (Line Id = 1) Note: Effective in Serial RGB mode. The line ID at RGBCL=1 represents the culling line ID set in the CULLLINE register. At RGBCL=0, it represents normal line ID.
		0	R0-G1-B2
		1	R0-B1-G2
		2	G0-R1-B2
		3	G0-B1-R2
		4	B0-R1-G2
		5	B0-G1-R2
3	Reserved	0	Reserved

Table 174. RGB Control Register (RGBCTL) Field Descriptions (continued)

Bit	Field	Value	Description
2 - 0	RGBOF		RGB Output Order for Odd Fields (Line Id = 0) Note: Effective in Serial RGB mode. The line ID at RGBCL=1 represents the culling line ID set in the CULLLINE register. At RGBCL=0, it represents normal line ID.
		0	R0-G1-B2
		1	R0-B1-G2
		2	G0-R1-B2
		3	G0-B1-R2
		4	B0-R1-G2
		5	B0-G1-R2

6.4.17 RGB Level Clipping Register (RGBCLP)

The RGB level clipping register (RGBCLP) is shown in Figure 177 and described in Table 175.

Figure 177. RGB Level Clipping Register (RGBCLP)

15	8	7	0
UCLIP		OFST	
R/W-FFh		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 175. RGB Level Clipping Register (RGBCLP) Field Descriptions

Bit	Field	Value	Description
15-8	UCLIP	0-FFh	Upper clip level for RGB output. Effective in all digital output modes with RGB output. Clipping is performed following offset addition.
7-0	OFST	0-FFh	Offset level for RGB output. Effective in all digital output modes with the RGB output. You can add the offset specified here to RGB (converted from YCbCr).

6.4.18 Line Identification Control Register (LINECTL)

The line identification control register (LINECTL) is shown in Figure 178 and described in Table 176.

Figure 178. Line Identification Control Register (LINECTL)

15	12	11	10	8
Reserved		VSTF	VCLID	
R/W-0	R-0	R/W-0	R/W-0	

7	6	5	4	3	2	1	0
VCLRD	VCL56	HLDF	HLDL	LINID	DCKCLP	DCKCLI	RGBCL
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 176. Line Identification Control Register (LINECTL) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved

Table 176. Line Identification Control Register (LINECTL) Field Descriptions (continued)

Bit	Field	Value	Description
11	VSTF		Vertical data valid start position field mode.
		0	Normal mode
		1	Field mode.
10-8	VCLID	0-7h	Vertical culling line position. Specifies which line will be culled of every six lines. No culling will be applied when VCLID is greater than 5. Effective when VCL56 = 1.
7	VCLRD		Vertical culling counter reset mode. Effective when VCL56 = 1. Specifies which line will be culled every six lines. No culling will be applied when VCLID is greater than 5.
		0	Reset to zero
		1	Reset to a random value
6	VCL56		Digital output vertical culling. Enabling discards one line of video output every six lines. This can be used to output NTSC valid lines with PAL timing.
		0	No culling
		1	5/6 culling
5	HLDF		Digital output field hold. Effective in non-standard mode. Enabling suspends the video output when current field output is completed. Reading the data from OSD is suspended during this period and the output of the sync signal and video data are also suspended. Setting to 0 restarts output.
		0	Normal
		1	Output hold
4	HLDL		Digital output line hold. Effective in non-standard mode. Enabling suspends the video output when current line output is completed. Reading the data from OSD is suspended during this period and the output of the sync signal and video data are also suspended. Setting to 0 restarts output.
		0	Normal
		1	Output hold
3	LINID		Start line ID control in even field.
		0	Line ID = 0
		1	Line ID = 1
2	DCKCLP		DCLK pattern switching by culling line ID. When this is enabled, the DCLK pattern can be switched according to the culling line ID set by the CULLLINE register. The DCLK pattern on each line is specified by the DCLKPTN and DCLKPTNA registers.
		0	Off
		1	On
1	DCKCLI		DCLK polarity inversion by culling line ID. When this is disabled, the DCLK polarity is fixed anytime as specified by the VCLKP register. Enabling inverts this polarity according to the culling line ID set by the CULLLINE register.
		0	Off
		1	On
0	RGBCL		RGB output order switching by culling line ID. Disabling switches RGB output order every line. Enabling switches this order according to the XORed signal of the line ID and the culling line ID set by the CULLLINE register. The output order is specified by RGBOF and RGBEF in the RGBCTL register.
		0	Off
		1	On

6.4.19 Culling Line Control Register (CULLLINE)

The culling line control register (CULLLINE) is shown in Figure 179 and described in Table 177.

Figure 179. Culling Line Control Register (CULLLINE)

15 12	11 8	7 4	3 0
CLOF	CLEF	Reserved	CULI
R/W-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 177. Culling Line Control Register (CULLLINE) Field Descriptions

Bit	Field	Value	Description
15-12	CLOF	0-Fh	Culling line ID toggle position (odd field).
11-8	CLEF	0-Fh	Culling line ID toggle position (even field).
7-4	Reserved	0	Reserved
3-0	CULI	0-Fh	Culling line ID inversion interval. This is set by line. Interval is represented by CULI+1.

6.4.20 LCD Output Signal Control Register (LCDOUT)

The LCD output signal control register (LCDOUT) is shown in Figure 180 and described in Table 178.

Figure 180. LCD Output Signal Control Register (LCDOUT)

15 9	8	7	6	5	4	3	2	1	0
Reserved	OES	FIDP	PWMP	PWME	ACE	BRP	BRE	OEP	OEE
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 178. LCD Output Signal Control Register (LCDOUT) Field Descriptions

Bit	Field	Value	Description
15-9	Reserved	0	Reserved
8	OES		Output Enable Signal Selection Maps LCD_OE or BRIGHT to an alternate output (GIO71)
		0	LCD output enable signal
		1	BRIGHT signal
7	FIDP		Field ID output polarity.
		0	Non-inverse
		1	Inverse
6	PWMP		PWM output pulse polarity.
		0	Active high
		1	Active low
5	PWME		PWM output control enable. Effective when digital output mode with PWM output is selected. PWM is output on COUT4 signal (use only in serial RGB or YCC8 modes).
		0	Off
		1	On
4	ACE		LCD_AC output control enable. LCD_AC is output on COUT7 signal (use only in serial RGB or YCC8 modes).
		0	Off
		1	On
3	BRP		BRIGHT output polarity.
		0	Active high
		1	Active low
2	BRE		BRIGHT output control enable. BRIGHT is output on COUT5 signal (use only in serial RGB or YCC8 modes).
		0	Off
		1	On
1	OEP		LCD_OE output polarity.
		0	Active high
		1	Active low
0	OEE		LCD_OE output control enable. LCD_OE is output on COUT6 signal (use only in serial RGV or YCC8 modes.
		0	Off
		1	On

6.4.21 Brightness Start Position Signal Control Register (BRTS)

The brightness start position signal control register (BRTS) is shown in Figure 181 and described in Table 179.

Figure 181. Brightness Start Position Signal Control Register (BRTS)

15 13	12 0
Reserved	BRTS
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 179. Brightness Start Position Signal Control Register (BRTS) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12-0	BRTS	0-1FFFh	BRIGHT pulse start position: specify the number of ENC cycles from the HSYNC signal.

6.4.22 Brightness Width Signal Control Register (BRTW)

The brightness width signal control register (BRTW) is shown in Figure 182 and described in Table 180.

Figure 182. Brightness Width Signal Control Register (BRTW)

15 13	12 0
Reserved	BRTW
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 180. Brightness Width Signal Control Register (BRTW) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12-0	BRTW	0-1FFFh	BRIGHT pulse width: specify the number of ENC cycles.

6.4.23 LCD_AC Signal Control Register (ACCTL)

The LCD_AC signal control register (ACCTL) is shown in Figure 183 and described in Table 181.

Figure 183. LCD_AC Signal Control Register (ACCTL)

15 13	12 0
ACTF	ACTH
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

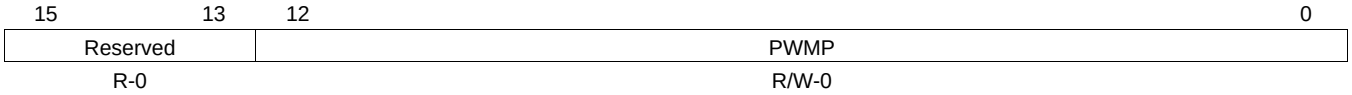
Table 181. LCD_AC Signal Control Register (ACCTL) Field Descriptions

Bit	Field	Value	Description
15-13	ACTF	0-7h	LCD_AC toggle interval. LCD_AC is toggled every field specified here.
12-0	ACTH	0-1FFFh	LCD_AC toggle horizontal position. LCD_AC is toggled by the number of ENC clocks from the rising edge of horizontal sync signal.

6.4.24 PWM Start Position Signal Control Register (PWMP)

The PWM start position signal control register (PWMP) is shown in Figure 184 and described in Table 182.

Figure 184. PWM Start Position Signal Control Register (PWMP)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

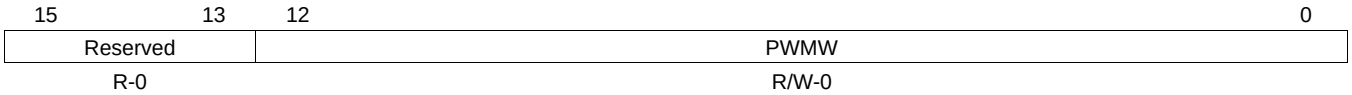
Table 182. PWM Start Position Signal Control Register (PWMP) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12-0	PWMP	0-1FFFh	PWM output period. Specify the number of ENC clocks. Period is PWMP + 1.

6.4.25 PWM Width Signal Control Register (PWMW)

The PWM width signal control register (PWMW) is shown in Figure 185 and described in Table 183.

Figure 185. PWM Width Signal Control Register (PWMW)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 183. PWM Width Signal Control Register (PWMW) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12-0	PWMW	0-1FFFh	PWM output pulse width. Specify the H pulse width by ENC clock. Setting to 0 makes PWM output L level always. Setting bigger value than PWMP sets to H level always.

6.4.26 DCLK Control Register (DCLKCTL)

The DCLK control register (DCLKCTL) is shown in Figure 186 and described in Table 184.

Figure 186. DCLK Control Register (DCLKCTL)

15	14	13 12	11	10	9	8
DCKIM	Reserved	DOFST	DCKEC	DCKME	DCKOH	DCKIH
R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5 0
Reserved		DCKPW
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

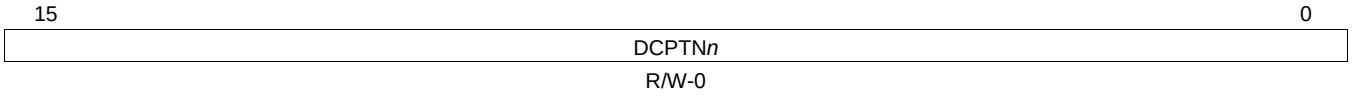
Table 184. DCLK Control Register (DCLKCTL) Field Descriptions

Bit	Field	Value	Description
15	DCKIM		DCLK internal mode. When enabled, a different pattern can be specified for the internal DCLK from the output DCLK. In this mode, DCLKPTN0A-PCLKPTN3A and DCLKHSTTA are used to specify the internal DCLK pattern and its pattern valid bit width, respectively. The DCLK pattern switching by culling line ID (LINECTL.DCKCLP = 1) is no longer available in this mode.
		0	Off
		1	On
14	Reserved	0	Reserved
13-12	DOFST	0-3h	DCLK output offset. Adjust the DCLK delay output from the VCLK pin by the ENC clock. When the DCLK output is configured as ENC clock gating with DCKEC = 1 and DCKOH = 0, these bits have no meaning.
		0	0
		1h	-0.5
		2h	0.5
		3h	1
11	DCKEC		DCLK pattern mode. When 0, the specified value in DCLKPTN (or DCLKPTNA) becomes the clock level of DCLK. When 1, DCLKPTN works as the clock enable for ENC clock.
		0	Level
		1	Enable
10	DCKME		DCLK mask control. Masks are specified by the DCLKHSTT, DCLKHVLD, DCLKVSTT, and DCLKVVLD registers.
		0	Mask is OFF and outputs DCLK directly.
		1	Mask is ON and outputs the clock in specified valid area.
9	DCKOH		DCLK output divide control Enabling divides the clock by two and outputs it from the VCLK pin. RGB data is output by the rising of internal DCLK and only divided clock output is output. Thus, this can be used to connect to the LCD that captures the data using both edges of DCLK.
		0	Divide by 1
		1	Divide by 2
8	DCKIH		Internal DCLK output divide control. Enabling divides the internal DCLK clock by 2. When the clock output is divided by 1 (DCKOH = 0), two clocks can be output per one data. Thus, this can be used to connect to the LCD that requires double clock frequency of data rate.
		0	Divide by 1
		1	Divide by 2
7-6	Reserved	0	Reserved
5-0	DCKPW	0-3Fh	DCLK pattern valid bit width. Set the width of valid bits among the 64 bits in the DCLKPTN0-DCLKPTN3- registers.

6.4.27 DCLK Pattern *n* Registers (DCLKPTN0-DCLKPTN3)

The DCLK pattern *n* register (DCLKPTN*n*) is shown in Figure 187 and described in Table 185.

Figure 187. DCLK Pattern *n* Register (DCLKPTN*n*)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

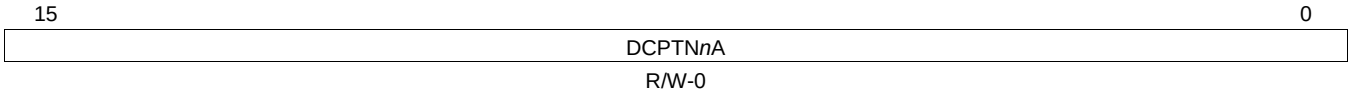
Table 185. DLCK Pattern *n* Register (DCLKPTN*n*) Field Descriptions

Bit	Field	Value	Description
15-0	DCPTN*n*	0-FFFFh	DCLK pattern. The specified bit pattern is output in resolution of ENC clock units. When DCKCLP=1, it works only for the line with the culling line ID 0.

6.4.28 DCLK Auxiliary Pattern *n* Registers (DCLKPTN0A-DCLKPTN3A)

The DCLK auxiliary pattern *n* register (DCLKPTN*n*A) is shown in Figure 188 and described in Table 186.

Figure 188. DCLK Auxiliary Pattern *n* Register (DCLKPTN*n*A)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

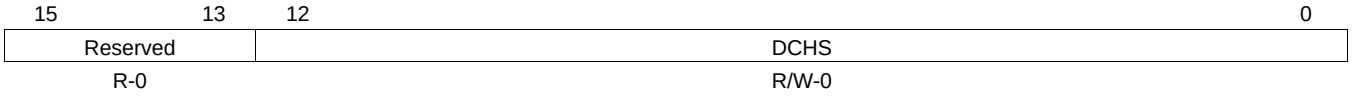
Table 186. DLCK Auxiliary Pattern *n* Register (DCLKPTN*n*A) Field Descriptions

Bit	Field	Value	Description
15-0	DCPTN*n*A	0-FFFFh	DCLK auxiliary pattern. The specified bit pattern is output in resolution of ENC clock units. Specifies the DCLK pattern for the culling line ID 1 in DCLK pattern switching mode.

6.4.29 Horizontal DCLK Mask Start Register (DCLKHS)

The horizontal DCLK mask start register (DCLKHS) is shown in Figure 189 and described in Table 187.

Figure 189. Horizontal DCLK Mask Start Register (DCLKHS)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

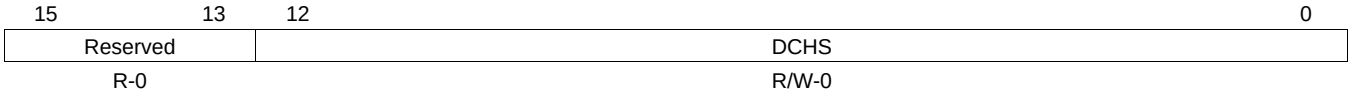
Table 187. Horizontal DCLK Mask Start Register (DCLKHS) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12-0	DCHS	0-1FFFh	Horizontal DCLK mask start position. This is specified in number of ENC clocks from start of the horizontal sync signal.

6.4.30 Horizontal Auxiliary DCLK Mask Start Register (DCLKHSA)

The horizontal auxiliary DCLK mask start register (DCLKHSA) is shown in Figure 190 and described in Table 188.

Figure 190. Horizontal Auxiliary DCLK Mask Start Register (DCLKHSA)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 188. Horizontal Auxiliary DCLK Mask Start Register (DCLKHSA) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12-0	DCHS	0-1FFFh	Horizontal auxiliary DCLK mask start position. This is specified in number of ENC clocks from start of the horizontal sync signal.

6.4.31 Horizontal DCLK Mask Range Register (DCLKHR)

The horizontal DCLK mask range register (DCLKHR) is shown in Figure 191 and described in Table 189.

Figure 191. Horizontal DCLK Mask Range Register (DCLKHR)

15 13	12 0
Reserved	DCHR
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 189. Horizontal DCLK Mask Range Register (DCLKHR) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12-0	DCHR	0-1FFFh	Horizontal DCLK mask range. This is specified in number of ENC clocks.

6.4.32 Vertical DCLK Mask Start Register (DCLKVS)

The vertical DCLK mask start register (DCLKVS) is shown in Figure 192 and described in Table 190.

Figure 192. Vertical DCLK Mask Start Register (DCLKVS)

15 13	12 0
Reserved	DCVS
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 190. Vertical DCLK Mask Start Register (DCLKVS) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12-0	DCVS	0-1FFFh	Vertical DCLK mask start position. This is specified in lines from vertical sync signal.

6.4.33 Vertical DCLK Mask Range Register (DCLKVR)

The vertical DCLK mask range register (DCLKVR) is shown in Figure 193 and described in Table 191.

Figure 193. Vertical DCLK Mask Range Register (DCLKVR)

15 13	12 0
Reserved	DCVR
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 191. Vertical DCLK Mask Range Register (DCLKVR) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12-0	DCVR	0-1FFFh	Vertical DCLK mask range. This is specified in number of lines.

6.4.34 Caption Control Register (CAPCTL)

The caption control register (CAPTCTL) is shown in Figure 194 and described in Table 192.

Figure 194. Caption Control Register (CAPCTL)

15	14 8	7 2	1 0
Reserved	CADF	Reserved	CAPF
R-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 192. Caption Control Register (CAPCTL) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved
14-8	CADF	0-7Fh	Closed caption default data register. When the caption data register (CAPDO or CAPDE) is not updated before the caption data transmission timing for the corresponding field, the ASCII code specified by this register is automatically transmitted for closed caption data.
7-2	Reserved	0	Reserved
1-0	CAPF	0-3h	Closed caption field select.
		0	No data output
		1h	(ODD) Even field
		2h	(EVEN) Odd field
		3h	(DUAL) Both odd and even fields

6.4.35 Caption Data Odd Field Register (CAPDO)

The caption data odd field register (CAPDO) is shown in Figure 195 and described in Table 193.

Figure 195. Caption Data Odd Field Register (CAPDO)

15	14 8	7	6 0
Reserved	CADO0	Reserved	CADO1
R-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 193. Caption Data Odd Field Register (CAPDO) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved
14-8	CADO0	0-7Fh	Closed caption default data0 (odd field). Specify the ASCII code of the 1st byte to be transmitted in closed captioning for odd field. Parity bit is automatically calculated.
7	Reserved	0	Reserved
6-0	CADO1	0-7Fh	Closed caption default data1 (odd field). Specify the ASCII code of the 2nd byte to be transmitted in closed captioning for odd field. Parity bit is automatically calculated.

6.4.36 Caption Data Even Field Register (CAPDE)

The caption data even field register (CAPDE) is shown in Figure 196 and described in Table 194.

Figure 196. Caption Data Even Field Register (CAPDE)

15	14 8	7	6 0
Reserved	CADE0	Reserved	CADE1
R-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 194. Caption Data Even Field Register (CAPDE) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved
14-8	CADE0	0-7Fh	Closed caption default data0 (even field). Specify the ASCII code of the 1st byte to be transmitted in closed captioning for odd field. Parity bit is automatically calculated.
7	Reserved	0	Reserved
6-0	CADE1	0-7Fh	Closed caption default data1 (even field). Specify the ASCII code of the 2nd byte to be transmitted in closed captioning for odd field. Parity bit is automatically calculated.

6.4.37 Video Attribute Data #0 Register (ATR0)

The video attribute data #0 register (ATR0) is shown in Figure 197 and described in Table 195.

Figure 197. Video Attribute Data #0 Register (ATR0)

15	8	7	0
Reserved		ATR0	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 195. Video Attribute Data #0 Register (ATR0) Field Descriptions

Bit	Field	Value	Description
15-8	Reserved	0	Reserved
7-0	ATR0	0-FFh	Video attribute data register 0. NTSC-Set the WORD0 data. • Bit7-6 is unused, • Bit5-3 is WORD0-B, • Bit2-0 is WORD0-A PAL-not used.

6.4.38 Video Attribute Data #1 Register (ATR1)

The video attribute data #1 register (ATR1) is shown in Figure 198 and described in Table 196.

Figure 198. Video Attribute Data #1 Register (ATR1)

15	8	7	0
Reserved		ATR1	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 196. Video Attribute Data #1 Register (ATR1) Field Descriptions

Bit	Field	Value	Description
15-8	Reserved	0	Reserved
7-0	ATR1	0-FFh	Video attribute data register 1. NTSC-Set the WORD1 and WORD2 data • Bit7-4 is WORD2 • Bit3-0 is WORD1 PAL-Set the GROUP1 and GROUP2 data. • Bit7-4 is GROUP2 • Bit3-0 is GROUP1

6.4.39 Video Attribute Data #2 Register (ATR2)

The video attribute data #2 register (ATR2) is shown in Figure 199 and described in Table 197.

Figure 199. Video Attribute Data #2 Register (ATR2)

15	8	7	0
Reserved		ATR2	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 197. Video Attribute Data #2 Register (ATR2) Field Descriptions

Bit	Field	Value	Description
15-8	Reserved	0	Reserved
7-0	ATR2	0-FFh	Video attribute data register 2. NTSC-Set CRC data and enable attribute insertion. • Bit7 is ATR_EN • Bit6 is unused • Bit5-0 is CRC PAL-Set GROUP3 and GROU4 data and enable attribute insertion. • Bit7 is ATR_EN • Bit6 is unused • Bit5-3 is GROUP4 and • Bit2-0 is GROUP3 ATR_EN: Attribute data insertion enable
		0	No insertion
		1	Insertion.

6.4.40 Video Status Register (VSTAT)

The video status register (VSTAT) is shown in Figure 200 and described in Table 198.

Figure 200. Video Status Register (VSTAT)

15	10	9	8	7	5	4	3	0
Reserved		CAEST	CAOST	Reserved		FIDST	Reserved	
R-0		R-0	R-0	R-0		R/W-0	R-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 198. Video Status Register (VSTAT) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved
9	CAEST		Closed caption status (even field). Bit automatically becomes 0 when transmission is done.
		0	Ready
		1	Data is being input
8	CAOST		Closed caption status (odd field). Bit automatically becomes 0 when transmission is done.
		0	Ready
		1	Data is being input
7-5	Reserved	0	Reserved

Table 198. Video Status Register (VSTAT) Field Descriptions (continued)

Bit	Field	Value	Description
4	FIDST		Field ID monitor
3-0	Reserved	0	Reserved

6.4.41 GCP/FRC Table RAM Address (RAMADR)

The GCP/FRC table RAM address (RAMADR) is shown in Figure 201 and described in Table 199.

Figure 201. GCP/FRC Table RAM Address (RAMADR)

15	6	5	0
Reserved		RAMADR	
R - 0		R/W - 0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 199. GCP/FRC Table RAM Address (RAMADR) Field Descriptions

Bit	Field	Value	Description
15- 6	Reserved	0	Reserved
7- 0	RAMADR		Gamma Correction Table RAM address Auto-increment is done after every access to RAMPORT register, When RAMADDR = 0x7F, auto-increment does not happen

6.4.42 GCP/FRC Table RAM Data Port (RAMPORT)

The GCP/FRC table RAM data port (RAMPORT) is shown in Figure 202 and described in Table 200.

Figure 202. GCP/FRC Table RAM Data Port (RAMPORT)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMPORT															
R/W - 0															

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

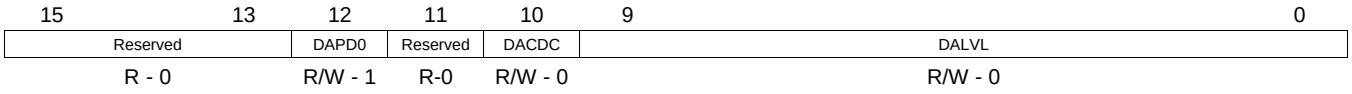
Table 200. GCP/FRC Table RAM Data Port (RAMPORT) Field Descriptions

Bit	Field	Value	Description
15 - 0	RAMPORT		RAM data port While reading, the data in the address specified in the RAMADR register can be read. While writing, the data is written to the address specified in the RAMADR register. The RAMADR is automatically incremented every access to the RAMPORT register in both write and read cases.

6.4.43 DAC Test Register (DACTST)

The DAC test register (DACTST) is shown in Figure 203 and described in Table 201.

Figure 203. DAC Test Register (DACTST)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 201. DAC Test Register (DACTST) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12	DAPD0		DAC0 power-down
		0	Normal mode
		1	Power-down mode
11	Reserved	0	Reserved
10	DAPDC		DAC DC output mode. Setting to 1 converts the value written in the DALVL register to DAC and directly outputs from DAOUT
		0	Normal mode
		1	DC output mode
9 - 0	DALVL	0-3FFh	DC level control

6.4.44 YOUT and COUT Levels Register (YCOLVL)

The YOUT and COUT levels register (YCOLVL) is shown in Figure 204 and described in Table 202.

Figure 204. YOUT and COUT Levels Register (YCOLVL)

15	8	7	0
YLVL		CLVL	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 202. YOUT and COUT Levels Register (YCOLVL) Field Descriptions

Bit	Field	Value	Description
15-8	YLVL	0-FFh	YOUT DC level. Specify the DC output level from YOUT pins when YOUT/COUT pin DC output mode (YCDC=1).
7-0	CLVL	0-FFh	COUT DC level. Specify the DC output level from COUT pins when YOUT/COUT pin DC output mode (YCDC=1).

6.4.45 Sub-Carrier Programming Register (SCPROG)

The sub-carrier programming register (SCPROG) is shown in Figure 205 and described in Table 203.

Figure 205. Sub-Carrier Programming Register (SCPROG)

15	10	9	0
Reserved		SCSD	
R-0		R/W-17Ah	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 203. Sub-Carrier Programming Register (SCPROG) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved
9-0	SCSD	0-3FFh	Sub-carrier initial phase value. Phase in degrees specified by SCSD/1024 × 360.

6.4.46 Composite Mode Register (CVBS)

The composite mode register (CVBS) is shown in Figure 206 and described in Table 204

Figure 206. Composite Mode Register (CVBS)

15	14 12	11 6	5	4	3	2	1	0
Reserved	YCDLY	Reserved	CVLVL	CSTUP	CBLS	CRCUT	CBBLD	CSBLD
R-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 204. Composite Mode Register (CVBS) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved
14-12	YCDLY	0-7h	Delay adjustment of the Y signal in the composite signal. The value represented is 2's complement.
		0	0
		1h	1
		2h	2
		3h	3
		4h	-4
		5h	-3
		6h	-2
		7h	-1
11-6	Reserved	0	Reserved
5	CVLVL		Composite video level (sync/white)
		0	286mV/714mV
		1	300mV/700mV
4	CSTUP		Setup for composite
		0	0%
		1	7.5%
3	CBLS		Blanking shape disable
		0	Enable
		1	Disable
2	CRCUT		Chroma signal low-pass filter select
		0	1.5 MHz cut-off
		1	3 MHz cut-off
1	CBBLD		Blanking build-up time for composite output
		0	140 µs
		1	300 µs
0	CSBLD		Sync build-up time for composite output
		0	140 µs
		1	200 µs

6.4.47 CVBS Timing Control 0 Register (ETMG0)

The CVBS timing control 0 register (ETMG0) is shown in Figure 207 and described in Table 205.

Figure 207. CVBS Timing Control 0 Register (ETMG0)

15 12	11 8	7 4	3 0
Reserved	CEPW	CFSW	CLSW
R-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 205. CVBS Timing Control 0 Register (ETMG0) Field Descriptions

Bit	Field	Value	Description
15-12	Reserved	0	Reserved
11-8	CEPW	0-Fh	Equalizing pulse width offset for composite output .This is set by ENC clock. This register is represented as signed-integer (2's complement).
7-4	CFSW	0-Fh	Field sync pulse width offset for composite output. This is set by ENC clock. This register is represented as signed-integer (2's complement).
3-0	CLSW	0-Fh	Line sync pulse width offset for composite output. This is set by ENC clock. This register is represented as signed-integer (2's complement).

6.4.48 CVBS Timing Control 1 Register (ETMG1)

The CVBS timing control 1 register (ETMG1) is shown in Figure 208 and described in Table 206.

Figure 208. CVBS Timing Control 1 Register (ETMG1)

15 12	11 8	7 4	3 0
CBSE	CBST	CFPW	CLBI
R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

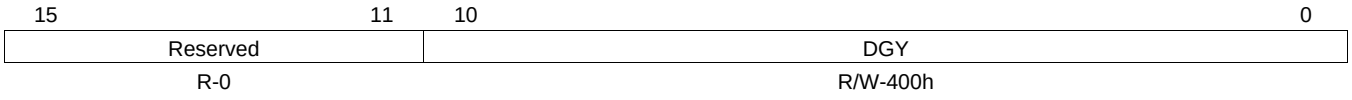
Table 206. CVBS Timing Control 1 Register (ETMG1) Field Descriptions

Bit	Field	Value	Description
15-12	CBSE	0-Fh	Burst end position offset for composite output. This is set by ENC clock. This register is represented as signed-integer (2's complement).
11-8	CBST	0-Fh	Burst start position offset for composite output. This is set by ENC clock. This register is represented as signed-integer (2's complement).
7-4	CFPW	0-Fh	Front porch position offset for composite output. This is set by ENC clock. This register is represented as signed-integer (2's complement).
3-0	CLBI	0-Fh	Line blanking end position offset for composite output. This is set by ENC clock. This register is represented as signed-integer (2's complement).

6.4.49 Digital RGB Matrix 0 Register (DRGBX0)

The digital RGB matrix 0 register (DRGBX0) is shown in Figure 209 and described in Table 207.

Figure 209. Digital RGB Matrix 0 Register (DRGBX0)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

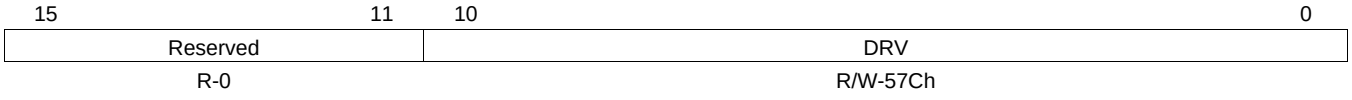
Table 207. Digital RGB Matrix 0 Register (DRGBX0) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved
10-0	DGY	0-7FFh	YCbCr->RGB matrix coefficient GY for digital RGB out. Equation | R | | GY 0 RV | | Y-16 | | G | = 1/1024 | GY -GU -GV | | Cb-128 | | B | | GY BU 0 | | Cr-128 | Default: | R | | 1024 0 1404 | | Y-16 | | G | = 1/1024 | 1024 -345 -715 | | Cb-128 | | B | | 1024 1774 0 | | Cr-128 |

6.4.50 Digital RGB Matrix 1 Register (DRGBX1)

The digital RGB matrix 1 register (DRGBX1) is shown in Figure 210 and described in Table 208.

Figure 210. Digital RGB Matrix 1 Register (DRGBX1)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 208. Digital RGB Matrix 1 Register (DRGBX1) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved
10-0	DRV	0-7FFh	YCbCr->RGB matrix coefficient RV for digital RGB out. Default is 1404(0x57C)

6.4.51 Digital RGB Matrix 2 Register (DRGBX2)

The digital RGB matrix 2 register (DRGBX2) is shown in Figure 211 and described in Table 209.

Figure 211. Digital RGB Matrix 2 Register (DRGBX2)

15	11	10	0
Reserved		DGU	
R-0		R/W-159h	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

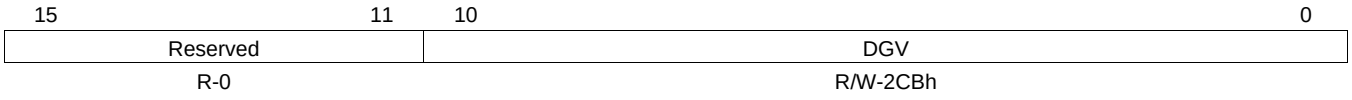
Table 209. Digital RGB Matrix 2 Register (DRGBX2) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved
10-0	DGU	0-7FFh	YCbCr->RGB matrix coefficient GU for digital RGB out. Default is 345 (0x159).

6.4.52 Digital RGB Matrix 3 Register (DRGBX3)

The digital RGB matrix 3 register (DRGBX3) is shown in Figure 212 and described in Table 210.

Figure 212. Digital RGB Matrix 3 Register (DRGBX3)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

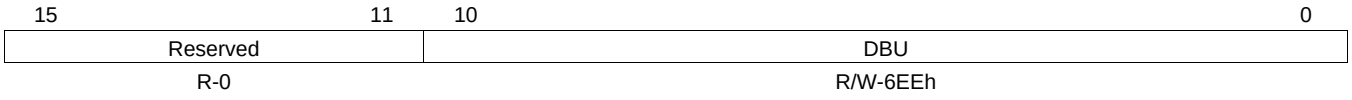
Table 210. Digital RGB Matrix 3 Register (DRGBX3) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved
10-0	DGV	0-7FFh	YCbCr->RGB matrix coefficient GV for digital RGB out. Default is 715 (0x2CB).

6.4.53 Digital RGB Matrix 4 Register (DRGBX4)

The digital RGB matrix 4 register (DRGBX4) is shown in Figure 213 and described in Table 211.

Figure 213. Digital RGB Matrix 4 Register (DRGBX4)



LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 211. Digital RGB Matrix 4 Register (DRGBX4) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved	0	Reserved
10-0	DBU	0-7FFh	YCbCr->RGB matrix coefficient BU for digital RGB out. Default is 1774 (0x6EE).

6.4.54 Vertical Data Valid Start Position for Even Field Register (VSTARTA)

The vertical data valid start position for even field register (VSTARTA) is shown in Figure 214 and described in Table 212.

Figure 214. Vertical Data Valid Start Position for Even Field Register (VSTARTA)

15 13	12 0
Reserved	VSTARTA
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 212. Vertical Data Valid Start Position for Even Field Register (VSTARTA) Field Descriptions

Bit	Field	Value	Description
15-13	Reserved	0	Reserved
12-0	VSTARTA	0-1FFFh	Vertical data valid start position for even field. Specify the number of lines.

6.4.55 OSD Clock Control 0 Register (OSDCLK0)

The OSD clock control 0 register (OSDCLK0) is shown in Figure 215 and described in Table 213.

Figure 215. OSD Clock Control 0 Register (OSDCLK0)

15 4	3 0
Reserved	OCPW
R-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 213. OSD Clock Control 0 Register (OSDCLK0) Field Descriptions

Bit	Field	Value	Description
15-4	Reserved	0	Reserved
3-0	OCPW	0-Fh	OSD clock pattern bit width. Sets the width of valid bit among all 16 bits in the OSDCLK1 register. The number of the valid bits is counted from LSB side to MSB side of the OSDCLK1.

6.4.56 OSD Clock Control 1 Register (OSDCLK1)

The OSD clock control 1 register (OSDCLK1) is shown in Figure 216 and described in Table 214.

Figure 216. OSD Clock Control 1 Register (OSDCLK1)

15	0
OCPT	
R/W-2h	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 214. OSD Clock Control 1 Register (OSDCLK1) Field Descriptions

Bit	Field	Value	Description
15-0	OCPT	0-FFFFh	OSD clock pattern.

6.4.57 Horizontal Valid Culling Control 0 Register (HVLDCL0)

The horizontal valid culling control 0 register (HVLDCL0) is shown in Figure 217 and described in Table 215.

Figure 217. Horizontal Valid Culling Control 0 Register (HVLDCL0)

15	5	4	3	0
Reserved		HCM	HCPW	
R-0		R/W-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 215. Horizontal Valid Culling Control 0 Register (HVLDCL0) Field Descriptions

Bit	Field	Value	Description
15-5	Reserved	0	Reserved
4	HCM		Horizontal valid culling mode When enabled, the LCD_OE signal is gated by the pattern specified by HCPT register.
		0	Normal mode
		1	Horizontal valid culling mode
3-0	HCPW	0-Fh	Horizontal valid culling pattern bit width Set the width of valid bit among all 16 bits in the HVLDCL1 register. The number of the valid bits is counted from LSB side to MSB side of the HVLDCL1.

6.4.58 Horizontal Valid Culling Control 1 Register (HVLDCL1)

The horizontal valid culling control 1 register (HVLDCL1) is shown in Figure 218 and described in Table 216.

Figure 218. Horizontal Valid Culling Control 1 Register (HVLDCL1)

15	0
HCPT	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 216. Horizontal Valid Culling Control 1 Register (HVLDCL1) Field Descriptions

Bit	Field	Value	Description
15-16	Reserved	0	Reserved
15-0	HCPT	0-FFFFh	Horizontal valid culling pattern.

6.4.59 OSD Horizontal Sync Advance Register (OSDHADV)

The OSD horizontal sync advance register (OSDHADV) is shown in Figure 219 and described in Table 217.

Figure 219. OSD Horizontal Sync Advance Register (OSDHADV)

15	8	7	0
Reserved		OHAD	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 217. OSD Horizontal Sync Advance Register (OSDHADV) Field Descriptions

Bit	Field	Value	Description
15-8	Reserved	0	Reserved
7-0	OHAD	0-FFh	OSD horizontal sync advance. OSD horizontal sync assertion timing can be advanced by this register. By default, the timing is adjusted so that OSD timing-related registers and VENC timing-related registers are aligned. Specify the number of ENC clocks.

6.4.60 Clock Control Register (CLKCTL)

The clock control register (CLKCTL) is shown in Figure 220 and described in Table 218.

Figure 220. Clock Control Register (CLKCTL)

15 9	8	7 5	4	3 1	0
Reserved	CKGAM	Reserved	CLKDIG	Reserved	CLKENC
R-0	R/W - 0	R-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 218. Clock Control Register (CLKCTL) Field Descriptions

Bit	Field	Value	Description
15-9	Reserved	0	Reserved
8	CKGAM		Clock Enable for Gamma Correction Table Turn on this bit when you want to change the gamma correction table. Gamma correction circuit is controlled by CLKDIG.
		0	Off
		1	On
7 - 5	Reserved	0	Reserved
4	CLKDIG		Clock Enable for Digital LCD Controller
		0	Off
		1	On
3 - 1	Reserved	0	Reserved
0	CLKENC		Clock Enable for Video Encoder
		0	Off
		1	On

6.4.61 Enable Gamma Correction Register (GAMCTL)

The enable gamma correction register (GAMCTL) is shown in Figure 221 and described in Table 219.

Figure 221. Enable Gamma Correction Register (GAMCTL)

15 1	0
Reserved	GAMON
R-0	R/W - 0

LEGEND: R/W = Read/Write; R = Read only;-*n* = value after reset

Table 219. Enable Gamma Correction Register (GAMCTL) Field Descriptions

Bit	Field	Value	Description
15 - 1	Reserved	0	Reserved
0	GAMON		Gamma Correction Enable
		0	Off
		1	On

Appendix A Revision History

This document has been revised from SPRUF72B to SPRUF72C because of the following technical change(s).

Table A-1. Changes Made in This Revision

Location	Additions, Deletions, Changes
Table 116	Changed Value column in V0W field.
Table 117	Changed Value column in V0H field.

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