

TMS320DM646x DMSoC Peripherals Overview

Reference Guide



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Read This First

About This Manual

This document provides an overview and briefly describes the peripherals available on the TMS320DM646x Digital Media System-on-Chip (DMSoC).

Related Documentation From Texas Instruments

The following documents describe the TMS320DM646x Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the DM646x DMSoC, related peripherals, and other technical collateral, is available in the C6000 DSP product folder at: www.ti.com/c6000.

[SPRUEP8](#) — ***TMS320DM646x DMSoC DSP Subsystem Reference Guide***. Describes the digital signal processor (DSP) subsystem in the TMS320DM646x Digital Media System-on-Chip (DMSoC).

[SPRUEP9](#) — ***TMS320DM646x DMSoC ARM Subsystem Reference Guide***. Describes the ARM subsystem in the TMS320DM646x Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the DSP subsystem and a majority of the peripherals and external memories.

[SPRAA84](#) — ***TMS320C64x to TMS320C64x+ CPU Migration Guide***. Describes migrating from the Texas Instruments TMS320C64x digital signal processor (DSP) to the TMS320C64x+ DSP. The objective of this document is to indicate differences between the two cores. Functionality in the devices that is identical is not included.

[SPRU732](#) — ***TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide***. Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C64x and TMS320C64x+ digital signal processors (DSPs) of the TMS320C6000 DSP family. The C64x/C64x+ DSP generation comprises fixed-point devices in the C6000 DSP platform. The C64x+ DSP is an enhancement of the C64x DSP with added functionality and an expanded instruction set.

[SPRU871](#) — ***TMS320C64x+ DSP Megamodule Reference Guide***. Describes the TMS320C64x+ digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

TMS320DM646x DMSoC Peripherals Overview

1 Overview

The TMS320DM646x Digital Media System-on-Chip (DMSoC) leverages TI's DaVinci™ technology to meet the networked media encode and decode application processing needs of next-generation embedded devices. The dual-core architecture of the DM646x DMSoC provides benefits of both a digital signal processor (DSP) and reduced instruction set computer (RISC) technologies, incorporating a high-performance TMS320C64x+™ DSP core and an ARM926EJ-S core.

The user-accessible peripherals available on the DM646x DMSoC are configured using a set of memory-mapped control registers. The peripheral bus controller performs the arbitration for accesses of on-chip peripherals. Peripherals available on the DM646x DMSoC and their associated literature number are listed in [Table 1](#).

Table 1. TMS320DM646x DMSoC Peripherals Documentation

Peripheral/Module	Acronym	Lit #
Asynchronous External Memory Interface	EMIF	SPRUEQ7
ATA Controller	ATA	SPRUEQ3
Clock Reference Generator	CRGEN	SPRUEQ1
DDR2 Memory Controller	DDR2	SPRUEQ4
Enhanced Direct Memory Access Controller	EDMA	SPRUEQ5
Ethernet Media Access Controller/Management Data Input/Output Module	EMAC/MDIO	SPRUEQ6
General-Purpose Input/Output	GPIO	SPRUEQ8
Host Port Interface	HPI	SPRUES1
Inter-Integrated Circuit Peripheral	I2C	SPRUER0
Internal Direct Memory Access Controller	IDMA	SPRU871
Interrupt Controller	INTC	SPRUEP9
Multichannel Audio Serial Port	McASP	SPRUER1
Peripheral Component Interconnect	PCI	SPRUER2
Phase-Locked Loop Controller	PLL	SPRUEP9
Power-Down Controller	PDC	SPRU871
Power and Sleep Controller	PSC	SPRUEP9
Pulse-Width Modulator	PWM	SPRUER3
Serial Peripheral Interface	SPI	SPRUER4
64-Bit Timer	Timer	SPRUER5
Transport Stream Interface	TSIF	SPRUEQ2
Universal Asynchronous Receiver/Transmitter	UART	SPRUER6
Universal Serial Bus Controller	USB	SPRUER7
Video Data Conversion Engine	VDCE	SPRUEQ9
Video Port Interface	VPIF	SPRUER9
VLYNQ Port	VLYNQ	SPRUER8

2 Asynchronous External Memory Interface (EMIF)

The asynchronous external memory interface (EMIF) provides a means to connect to a variety of external devices including:

- NAND Flash
- Asynchronous devices including Flash and SRAM
- Host processor interfaces such as the host port interface (HPI) on a Texas Instruments DSP

The most common use for the EMIF is to interface with both Flash devices and SRAM devices. The EMIF includes many features to enhance the ease and flexibility of connecting to external asynchronous devices. The EMIF features includes support for:

- 4 addressable chip select spaces of up to 32MB each
- 8-bit and 16-bit data bus widths
- Programmable cycle timings such as setup, strobe, and hold times as well as turnaround time
- Select strobe mode
- Extended Wait mode
- NAND Flash ECC generation
- Connecting as a host to a TI DSP HPI interface
- Data Bus Parking

3 ATA Controller

The AT attachment/ATA packet interface (ATA/ATAPI) is an interface that is most commonly used by portable computers (PCs) and portable devices to interface a host processor with data storage or audio devices. The ATA interface debuted in the mid 1980s as an interface between a hard-disk drive and a PC by way of a ribbon cable. Ever since then, other devices, mostly storage, including compact disks have widely adopted the ATA/ATAPI interface, leveraging from its proven capability as the means for connecting to a host processor. These allowed device manufacturers to avoid building and supporting a proprietary interface that would significantly limit the use of their devices. The ATA/ATAPI interface is popular due to its simplicity, low cost, reliability, compatibility, as well as its wide acceptance and long history of use within the PC industry market.

The TMS320DM646x DMSoC supports an onboard ATA/ATAPI host controller module (IDE controller) allowing it to exploit access to a vast majority of available data storage and audio devices. The onboard IDE host controller performs PIO, multiword, and ultra-DMA transactions with ATA and ATAPI compliant devices. Hard-disk drive, compact disk (CD), and DVD are some ATA/ATAPI-compliant devices that the IDE host controller is destined to interface with. This allows applications like streaming media and digital still cameras the means for easy access to commonly used external storage devices.

The IDE host controller logic supports PIO, multiword DMA and ultra-DMA (ultra-ATA) modes. The ATA controller has the following features:

- Single channel capable for connecting up to two ATA/ATAPI devices
- Supports PIO modes 0, 1, 2, 3, and 4
- Supports multiword DMA modes 0, 1, and 2
- Supports ultra-DMA modes 0, 1, 2, 3, 4, and 5
- Full scatter gather DMA capability
- Programmable timing parameters provide support of any multiple ATA timing options mode at any processor clock frequency

4 Clock Reference Generator (CRGEN)

The clock reference generator (CRGEN) module aims to recover the 27-MHz system clock from the program clock reference (PCR) value that is detected by the transport stream interface (TSIF) module, and also develops a system time clock (STC) counter value in both streaming (clock recovery with PCR) and video input cases.

The CRGEN consists of the following features:

- Subtractor
- Loop filter (LPF)
- Sigma-Delta digital-to-analog converter (DAC)
- System time clock (STC) counter

5 DDR2 Memory Controller

The DDR2 memory controller is used to interface with JESD79D-2A standard compliant DDR2 SDRAM devices. Memory types such as DDR1 SDRAM, SDR SDRAM, SDRAM, and asynchronous memories are not supported. The DDR2 memory controller is the major memory location for program and data storage.

The DDR2 memory controller supports the following features:

- JESD79D-2A standard compliant DDR2 SDRAM
- 1 Gbyte memory space
- Data bus width of 32 or 16 bits
- CAS latencies: 2, 3, 4, and 5
- Internal banks: 1, 2, 4, and 8
- Burst length: 8
- Burst type: sequential
- 1 CS signal
- Page sizes: 256, 512, 1024, and 2048
- SDRAM autoinitialization
- Self-refresh mode
- Prioritized refresh
- Programmable refresh rate and backlog counter
- Programmable timing parameters
- Little-endian mode

6 Enhanced Direct Memory Access (EDMA) Controller

The enhanced direct memory access (EDMA3) controller's primary purpose is to service user-programmed data transfers between two memory-mapped slave endpoints on the device. Typical usage includes, but is not limited to:

- Servicing software driven paging transfers (for example, from external memory such as SDRAM to internal device memory such as DSP L2 SRAM)
- Servicing event driven peripherals, such as a serial port
- Performing sorting or subframe extraction of various data structures
- Offloading data transfers from the main device CPU(s) or DSP(s) (See the device data manual for specific peripherals that are accessible via EDMA3.)

The EDMA3 on the TMS320DM646x DMSoC has a different architecture from the previous EDMA2 controller on the TMS320C621x/C671x DSPs and TMS320C64x DSPs.

The EDMA3 controller consists of two principal blocks:

- EDMA3 channel controller (EDMA3CC)
- EDMA3 transfer controller(s) (EDMA3TC)

The EDMA3 channel controller serves as the user interface for the EDMA3 controller. The EDMA3CC includes parameter RAM (PaRAM), channel control registers, and interrupt control registers. The EDMA3CC serves to prioritize incoming software requests or events from peripherals, and submits transfer requests (TR) to the transfer controller. The EDMA3 channel controller has the following features:

- Fully orthogonal transfer description
- Flexible transfer definition
- Interrupt generation
- Debug visibility
- 64 DMA channels
- 8 QDMA channels
- 512 PaRAM sets
- 4 transfer controllers/event queues. The system-level priority of these queues is user programmable.
- 16 event entries per event queue

The EDMA3 transfer controllers are slaves to the EDMA3 channel controller and are responsible for data movement. The transfer controller issues read/write commands to the source and destination addresses programmed for a given transfer. The EDMA3 transfer controller has the following features:

- 4 transfer controllers
- 64-bit wide read and write ports per channel
- Up to 4 in-flight transfer requests (TR)
- Programmable priority level
- Supports 2 dimensional transfers with independent indexes on source and destination (EDMA3CC manages the 3rd dimension)
- Support for increment or constant addressing mode transfers
- Interrupt and error support

7 Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO) Module

The ethernet media access controller (EMAC) and physical layer (PHY) device management data input/output (MDIO) module is used to move data between the TMS320DM646x DMSoC and another host connected to the same network, in compliance with the Ethernet protocol. The EMAC is controlled by the ARM CPU of the device; control by the DSP CPU is not supported. The EMAC controls the flow of packet data from the system to the PHY and the MDIO module controls PHY configuration and status monitoring.

Both the EMAC and the MDIO modules interface to the system core through a custom interface that allows efficient data transmission and reception. This custom interface is referred to as the EMAC control module and is considered integral to the EMAC/MDIO peripheral.

The EMAC/MDIO has the following features:

- Synchronous 10/100/1000 Mbps operation.
- G/MII interface to the physical layer device (PHY).
- Full-duplex gigabit operation (half-duplex not supported).
- EMAC acts as DMA master to either internal or external device memory space.
- Hardware error handling including CRC.
- Eight receive channels with VLAN tag discrimination for receive quality-of-service (QOS) support.
- Eight transmit channels with round-robin or fixed priority for transmit quality-of-service (QOS) support.
- Ether-Stats and 802.3-Stats RMON statistics gathering.
- Transmit CRC generation selectable on a per channel basis.
- Broadcast frames selection for reception on a single channel.
- Multicast frames selection for reception on a single channel.
- Promiscuous receive mode frames selection for reception on a single channel (all frames, all good frames, short frames, error frames).
- Hardware flow control.
- 8K-byte local EMAC descriptor memory that allows the peripheral to operate on descriptors without affecting the CPU. The descriptor memory holds enough information to transfer up to 512 Ethernet packets without CPU intervention.
- Programmable interrupt logic permits the software driver to restrict the generation of back-to-back interrupts, which allows more work to be performed in a single call to the interrupt service routine.
- TI Adaptive Performance Optimization for improved half duplex performance.
- Configurable receive address matching/filtering, receive FIFO depth, and transmit FIFO depth.
- No-chain mode truncates frame to first buffer for network analysis applications.
- Emulation support.
- Loopback mode.

8 General-Purpose Input/Output (GPIO)

The general-purpose input/output (GPIO) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, you can write to an internal register to control the state driven on the output pin. When configured as an input, you can detect the state of the input by reading the state of an internal register. The GPIO peripheral is accessible via the ARM926 CPU as well as the C64x+ CPU.

The GPIO peripheral consists of the following features.

- Supports up to 33 general-purpose pins
- Output set/clear functionality through separate data set and clear registers allows multiple software processes to control GPIO signals without critical section protection.
- Set/clear functionality through writing to a single output data register is also supported.
- Separate input/output registers
 - Output register can be read to reflect output drive status.
 - Input register can be read to reflect pin status.
- All GPIO signals can be used as interrupt sources with configurable edge detection.
- All GPIO signals can be used to generate events to the EDMA.

9 Host Port Interface (HPI)

The host port interface (HPI) provides a parallel port interface through which an external host processor can directly access the TMS320DM646x DMSoC processor's resources (configuration and program/data memories). The external host device is asynchronous to the CPU clock and functions as a master to the HPI interface. The HPI enables a host device and the DM646x DMSoC processor to exchange information via internal or external memory. Dedicated address (HPIA) and data (HPID) registers within the HPI provide the data path between the external host interface and the processor resources. An HPI control register (HPIC) is available to the host and the CPU for various configuration and interrupt functions.

The HPI supports the following features:

- Multiplexed address/data
- Dual 16-bit halfword cycle access (internal data word is 32-bits wide)
- 16-bit-wide host data bus interface
- Internal data bursting using 8-word read and write first-in, first-out (FIFO) buffers
- HPI control register (HPIC) accessible by both the ARM CPU and the external host
- HPI address register (HPIA) accessible by both the ARM CPU and the external host
- Separate HPI address registers for read (HPIAR) and write (HPIAW) with configurable option for operating as a single HPI address register
- HPI data register (HPID)/FIFOs providing data-path between external host interface and CPU resources
- Multiple strobes and control signals to allow flexible host connection
- Asynchronous HRDY output to allow the HPI to insert wait states to the host
- Software control of data prefetching to the HPID/FIFOs
- Processor-to-Host interrupt output signal controlled by HPIC accesses
- Host-to-Processor interrupt controlled by HPIC accesses
- Register controlled HPIA and HPIC ownership and FIFO timeout
- Memory-mapped peripheral identification register (PID)
- Bus holders on host data and address buses (these are actually external to HPI module)
- 32-bit word cycle access (internal data word is 32-bits wide)
- 32-bit-wide host data bus interface

10 Inter-Integrated Circuit (I2C) Peripheral

The inter-integrated circuit (I2C) peripheral provides an interface between the TMS320DM646x DMSoC and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus. External components attached to this 2-wire serial bus can transmit and receive data that is 2-bits to 8-bits wide to and from the DM646x DMSoC through the I2C peripheral.

The I2C peripheral has the following features:

- Compliance with the Philips Semiconductors I2C-bus specification (version 2.1):
 - Support for byte format transfer
 - 7-bit and 10-bit addressing modes
 - General call
 - START byte mode
 - Support for multiple master-transmitters and slave-receivers mode
 - Support for multiple slave-transmitters and master-receivers mode
 - Combined master transmit/receive and receive/transmit mode
 - I2C data transfer rate of from 10 kbps up to 400 kbps (Philips I2C rate)
- 2 to 7 bit format transfer (in addition to the byte format transfer)
- Free data format mode
- One read DMA event and one write DMA event that the DMA can use
- Seven interrupts that the CPU can use
- Peripheral enable/disable capability

11 Internal Direct Memory Access (IDMA) Controller

The internal direct memory access (IDMA) controller in the TMS320C64x+ megamodule allows rapid data transfers between all local memories. It provides a fast way to page code and data sections into any memory-mapped RAM local to the C64x+ megamodule. The key advantage of the IDMA controller is that it allows for transfers between slower (level 2: L2) and faster (level 1: L1D, L1P) memory. The IDMA controller can provide lower latency than the cache controller since the transfers take place in the background of CPU operation, thereby removing stalls due to cache.

In addition, the IDMA controller facilitates rapid programming of peripheral configuration registers accessed through the external configuration space (CFG) port of the C64x+ megamodule. The IDMA controller view of the external configuration space that has a 32-word granularity and allows any register within a 32-word block to be individually accessed.

In summary, the IDMA controller is:

- Optimized for burst transfers of memory blocks (contiguous data).
- Allows access to and from any local memory (L1P, L1D, L2 (pages 0 and 1), and external CFG (but, source and destination cannot both be in CFG). CFG is accessible to channel 0 only. No CFG-to-CFG transfers.
- Supports the full data rate to and from the L2 memory controllers (256-bit data every extended memory controller (EMC) clock cycle):
 - Maximum throughput only achieved when source and destination are two different memories (L1P, L1D, and L2).
 - 50% throughput when source and destination are the same memory.
- Indicates transfer completion through programmable interrupts to the CPU.

The internal direct memory access (IDMA) controller is described in the *TMS320C64x+ DSP Megamodule Reference Guide* ([SPRU871](#)).

12 Interrupt Controller (AINTC)

The TMS320DM646x DMSoC ARM interrupt controller (AINTC) has the following features:

- Supports up to 64 interrupt channels (16 external channels)
- Interrupt mask for each channel
- Each interrupt channel is mappable to a Fast Interrupt Request (FIQ) or to an Interrupt Request (IRQ) type of interrupt.
- Hardware prioritization of simultaneous interrupts
- Configurable interrupt priority (2 levels of FIQ and 6 levels of IRQ)
- Configurable interrupt entry table (FIQ and IRQ priority table entry) to reduce interrupt processing time

The ARM core supports two interrupt types: FIQ and IRQ. See the ARM926EJ Technical Reference Manual for detailed information about the ARM's FIQ and IRQ interrupts. Each interrupt channel is mappable to an FIQ or to an IRQ type of interrupt, and each channel can be enabled or disabled. The AINTC supports user-configurable interrupt-priority and interrupt entry addresses. Entry addresses minimize the time spent jumping to interrupt service routines (ISRs). When an interrupt occurs, the corresponding highest priority ISRs address is stored in the AINTC's ENTRY register. The IRQ or FIQ interrupt routine can read the ENTRY register and jump to the corresponding ISR directly. Thus, the ARM does not require a software dispatcher to determine the asserted interrupt.

The ARM interrupt controller (AINTC) is described in the *TMS320DM646x DMSoC ARM Subsystem Reference Guide* ([SPRUEP9](#)).

13 Multichannel Audio Serial Port (McASP)

The multichannel audio serial port (McASP) functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP is useful for time-division multiplexed (TDM) stream, Inter-Integrated Sound (I2S) protocols, and intercomponent digital audio interface transmission (DIT). The McASP consists of transmit and receive sections that may operate synchronized, or completely independently with separate master clocks, bit clocks, and frame syncs, and using different transmit modes with different bit-stream formats. The general-purpose input/output (GPIO) functionality internal to the McASP is not supported.

Features of the McASP include (all the features pertain to McASP0; features related to receiving or transmitting in burst or TDM mode do not pertain to McASP1):

- Two independent clock generator modules provide clocking flexibility that allows the McASP to receive and transmit at different rates. For example, the McASP can receive data at 48 kHz but output up-sampled data at 96 kHz or 192 kHz.
- Independent transmit and receive modules
- Individually assignable serial data pins (up to 4 pins for McASP0 and 1 pin for McASP1)
- Glueless connection to audio analog-to-digital converters (ADC), digital-to-analog converters (DAC), codec, digital audio interface receiver (DIR), and S/PDIF transmit physical layer components
- Wide variety of I2S and similar bit-stream format
- Integrated digital audio interface transmitter (DIT) supports:
 - S/PDIF, IEC60958-1, AES-3 formats
 - Up to 4 transmit pins
 - Enhanced channel status/user data RAM
- 384-slot TDM with external digital audio interface receiver (DIR) device
- Extensive error checking and recovery

14 Peripheral Component Interconnect (PCI)

The TMS320DM646x PCI module allows communication with devices compliant to the *PCI Local Bus Specification* (revision 2.3) via a 32-bit address/data bus operating at speeds up to 33 MHz and up to 66 MHz (for DM6467T devices only).

The PCI module supports the following features:

- PCI Local Bus Specification (revision 2.3) compliant
- Single function PCI interface provided
- 32-bit address/data bus width
- Operation up to 33 MHz and up to 66 MHz (for DM6467T devices only).
- Optimized burst behavior supported for system cache line sizes of 16, 32, 64 and 128 bytes
- PCI is only accessible from the ARM

The PCI operates as a PCI slave device for configuration cycles and memory cycles. It also acts as a PCI master device for configuration cycles, IO cycles, and memory accesses to other devices.

15 Phase-Locked Loop Controller (PLL)

The TMS320DM646x DMSoC has two PLL controllers that provide clocks to different parts of the system. PLL1 provides clocks (though various dividers) to most of the components of the DM646x DMSoC. PLL2 is dedicated to the DDR2 memory controller. See the device-specific data manual for the supported input clocks.

The PLL controller provides the following:

- Glitch-Free Transitions (on changing clock settings)
- Domain Clocks Alignment
- Clock Gating
- PLL power down

The various clock outputs given by the controller are as follows:

- Domain Clocks: SYSCLK[1:n]
- Auxiliary Clock from reference clock source: AUXCLK
- Bypass Domain clock: SYSCLKBP

Various dividers that can be used are as follows:

- SYSCLK Divider: D1, ... Dn
- SYSCLKBP Divider: BPDIV

Various other controls supported are as follows:

- PLL Multiplier Control: PLLM
- Software-programmable PLL Bypass: PLEN

The PLL controller (PLL) is described in the *TMS320DM646x DMSoC ARM Subsystem Reference Guide* ([SPRUEP9](#)).

16 Power-Down Controller (PDC)

The TMS320C64x+ megamodule supports the ability to power-down various parts of the C64x+ megamodule. Using the power-down controller (PDC) in the C64x+ megamodule, the entire C64x+ megamodule can be powered-down. These power-down features can be used to design systems for lower overall system power requirements.

The power-down controller (PDC) is described in the *TMS320C64x+ DSP Megamodule Reference Guide* ([SPRU871](#)).

17 Power and Sleep Controller (PSC)

The power and sleep controller (PSC) provides a standard method for controlling device power by gating clocks to individual modules. The PSC is described in the *TMS320DM646x DMSoC ARM Subsystem Reference Guide* ([SPRUEP9](#)).

18 Pulse-Width Modulator (PWM)

The pulse-width modulator (PWM) peripheral is very common in embedded systems. It provides a way to generate a pulse periodic waveform for motor control or can act as a digital-to-analog converter with some external components. This PWM peripheral is basically a timer with a period counter and a first-phase duration comparator, where bit width of the period and first-phase duration are both programmable.

The PWM peripheral has the following features:

- 32-bit period counter
- 32-bit first-phase duration counter
- 32-bit repeat counter for one-shot operation. One-shot operation will produce $N + 1$ periods of the waveform, where N is the repeat counter value.
- Configurable to operate in either one-shot or continuous mode.
- One-shot operation can be triggered by VPIF or GPIO
- Configurable PWM output pin inactive state.
- Interrupt and EDMA synchronization events.
- Emulation support for stop or free-run operation.

19 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (2 to 16 bits) to be shifted into and out of the TMS320DM646x DMSoC at a programmed bit-transfer rate. The SPI is normally used for communication between the DM646x DMSoC and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EPROMs and analog-to-digital converters.

The SPI allows serial communication with other SPI devices through a 3-pin, 4-pin, or 5-pin mode interface. The DM646x DMSoC implementation supports multichip-select operation for up to two SPI slave devices. The SPI can operate as both a master device and a slave device.

The SPI has the following features:

- 16-bit shift register
- Receive buffer register
- 8-bit clock prescaler
- Serial clock I/O pin
- Programmable SPI clock frequency range
- Programmable character length (2 to 16 bits)
- Programmable clock phase (delay or no delay)
- Programmable clock polarity (high or low)
- Two chip select signals provide the ability to control two slave devices
- One slave in, master out pin and one slave out, master in pin
- One enable signal (input to SPI) controlled by the slave device indicating that the slave device is ready to receive

20 64-Bit Timer

The TMS320DM646x DMSoC processor contains three software-programmable 64-bit timers (Timer0, Timer1, and Timer2) that can be operated by either the ARM or the DSP. Timer0 and Timer1 are used as general-purpose timers and can be programmed in 64-bit mode, dual 32-bit unchained mode, or dual 32-bit chained mode; Timer2 is used only as a watchdog timer. The watchdog timer mode is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

The 64-bit timer has the following features:

- 64-bit count-up counter
- Timer modes:
 - 64-bit general-purpose timer mode
 - Dual 32-bit general-purpose timer mode (chained or unchained)
 - Watchdog timer mode
- 2 possible clock sources:
 - Internal clock
 - External clock input via timer input pin
- 2 possible operation modes:
 - One-time operation (timer runs for one period then stops)
 - Continuous operation (timer automatically resets after each period)
- Generates interrupts to both the DSP and the ARM CPUs
- Generates sync event to EDMA

21 Transport Stream Interface (TSIF)

The transport stream interface (TSIF) module is used to parser stream including TS (Time Stamp) header, adaptation field, payload and PID table, and to input and output stream with a parallel and serial interface.

The TSIF has the following features:

- Simple I/O section that consists of a serial and parallel interface with both synchronous and asynchronous modes.
- Stream Parser and PID filter.
- Absolute time stamp (ATS) generator and checker for time management by CPU and video codec.
- Ring buffer controller prepared for SDRAM access.
- Input and output ping-pong buffer (one buffer has 256 byte (64 bit × 32 word)).
- Serial and parallel I/F with both synchronous and asynchronous modes.
- Data bus width is 1 bit on serial interface (using MSB of parallel interface) and 8 bits on parallel interface.
- Stream input/output (I/O) speed rate is configurable by I/O clock speed.
- Input data is stored into SDRAM in 32-bit little-endian mode only with 192 byte/unit format or 256 byte/unit format.
- ATS detection, correction, and addition mode are implemented.
- Automatically detect program association table (PAT) and program map table (PMT) and reflect to PID table assignment in itself (partial TS only; stream type and PID should be one-to-one mapping).
- PID filter with 7 PID filter tables and stream type assignments.
- Bypass mode is implemented so that not only TS data but also any other data can be received or transmitted by this module.
- Ring buffer control for both write (8 channels) and read (1 channel) control for SDRAM.
- Specific packet support which is prepared for indicating boundary of plural program on TS.
- Full-TS can be supported in one mode (semiautomatic A mode) with communication to the CPU. Mainly, TS-related functions are available only in partial TS (semiautomatic B mode and full automatic mode can support only partial TS whose stream type and PID is one-to-one mapping).

22 Universal Asynchronous Receiver/Transmitter (UART)

This universal asynchronous receiver/transmitter (UART) peripheral performs serial-to-parallel conversion on data received from a peripheral device and parallel-to-serial conversion on data received from the TMS320DM646x DMSoC processor CPU. The CPU can read the UART status at any time. The UART includes control capability and a processor interrupt system that can be tailored to minimize software management of the communications link.

The UART module is also capable of performing standard infrared communication in slow infrared mode (SIR) and medium infrared mode (MIR) defined by the Infrared Data Association (IrDA).

Moreover, the UART module also supports consumer infrared (CIR) communications. The CIR mode uses a variable pulse-width modulation technique to encompass the various formats of infrared encoding for remote control applications. The CIR logic is to transmit and receive data packets according to the user-definable frame structure and packet content.

The UART module consists of the following main features:

- Selectable UART/IrDA/CIR modes.
- Dual 64 entry FIFOs for received and transmitted data payload.
- Programmable and selectable transmit and receive FIFO trigger levels for DMA and interrupt generation.
- Frequency prescaler values from 0 to 16383 to generate the appropriate baud rates.
- Two DMA requests, 1 interrupt request to the system.

The UART/Modem includes the following functions:

- Baud-rate up to 1.8432 Mbits/s.
- Software/Hardware flow control.
- Programmable serial interface characteristics.
- False start bit detection.
- Line break generation and detection.
- Fully prioritized interrupt system controls.
- Internal test and loopback capabilities.
- Modem control functions.

IR-IrDA functions include:

- Slow infrared (SIR, baud-rate up to 57.6 Kbits/s) and medium infrared (MIR, baud-rate up to 0.576 Mbits/s) operations.
- Framing error, cyclic redundancy check (CRC) error, abort pattern (SIR, MIR) detection.
- 8-entry status FIFO (with selectable trigger levels) available to monitor frame length and frame errors.

IR-CIR functions include:

- Consumer Infrared remote control mode with programmable data encoding.

23 Universal Serial Bus (USB)

The universal serial bus (USB) controller in the TMS320DM646x DMSoC can be used as either a host or a peripheral. As a host, it supports all three speeds (low, full, and high) in point-to-point data transfers with another peripheral or device or multiple peripherals/devices via a HUB in a multipoint set-up. As a peripheral, it supports high-speed and full-speed operations. The USB controller is operated by the ARM through the memory-mapped registers. The USB controller provides a low-cost connectivity solution for consumer portable devices by providing a mechanism for data transfer between USB devices up to 480 Mbps.

The USB has the following features:

- Operating as a host, it complies with the USB 2.0 standard for high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations with a peripheral
- Operating as a peripheral, it complies with the USB 2.0 standard for high-speed (480 Mbps) and full-speed (12 Mbps) operation with a host.
- Supports 4 simultaneous receive and transmit endpoints, in addition to control endpoint, more devices can be supported by dynamically switching endpoints states
- Each endpoint (other than endpoint 0) can support all transfer types (control, bulk, interrupt, and isochronous)
- Includes a 4K endpoint FIFO RAM, and supports programmable FIFO sizes
- External 5V power supply for VBUS, when operating as host, enabled directly by the USB controller through a dedicated signal
- Includes a DMA controller that supports 4 transmit and 4 receive DMA channels
- Includes RNDIS mode of DMA for accelerating RNDIS type protocols using short packet termination over USB

24 Video Data Conversion Engine (VDCE)

The video data conversion engine (VDCE) is used for video data processing in the TMS320DM646x DMSoC. The VDCE has several capabilities of not only pure video data processing but also functions that are required from the video codec module.

The VDCE supports the following functions:

- Resize function on horizontal (HRSZ) and vertical (VRSZ) with ratio defined by $256/N$ (N is natural number that ranges from 256 to 2048) with 4 taps interpolation. Magnification ratio of horizontal resize and vertical resize can be configured separately (different value can be configured).
- Anti-alias filter (combination of two kinds of low-pass filter) with horizontal 7 taps, and vertical direction (if this filter is activated for vertical direction, no interpolation on the vertical direction will be the result of the function).
- Chrominance signal format conversion (CCV) on both directions, one is from 4:2:2 to 4:2:0 and one is from 4:2:0 to 4:2:2. This function also uses 4 taps interpolation. MPEG-1 specific format (half-pixel phased from even pixel position of luminance) is also supported.
- Edge padding for preparation of MC with unrestricted motion vector (required by MPEG-4, H.264, VC-1). All modes (progressive, interlace frame, and interlace field) are supported (macro-block level control that is required in H.264 is not supported).
- VC-1 range mapping in advanced profile (in case of displaying decoded reference image or trans-coding from VC-1 to any other format of video codec).
- 2-bit hardware menu overlay function used for multiplexing video image data and sub-title data that has to be supported in digital TV broadcasting in Japan.

25 Video Port Interface (VPIF)

The video port interface (VPIF) in the in the TMS320DM646x DMSoC is a receiver and transmitter of video data, which has two input channels (channel 0 and 1) and two output channels (channel 2 and 3). Channels 0 and 1 have the same architecture, and channels 2 and 3 have the same architecture.

The functional features of the VPIF are:

- Three speed grades (99 MHz, 108 MHz, and 150 MHz) available for the VPIF. See device-specific data manual for the part number associated with each speed grade.
- ITU-BT.656 format is supported.
- ITU-BT.1120, such as 1080I60, 1080P30, and 1080P60 (150 MHz VPIF devices only), and SMTPE 296 formats are supported.
- Raw data capturing function (receiver only; 8/10/12-bit format) is supported.
- VBI data storage is supported on BT.656 (SDTV) mode.
- Data clipping function for output (silicon revision 3.0 and later revisions only).

26 VLYNQ Port

The VLYNQ™ communications interface port is a serial interface with a low pin count, high-speed point-to-point serial interface in the TMS320DM646x DMSoC for connecting to host processors and other VLYNQ-compatible devices. The VLYNQ port is a full-duplex serial bus where transmit and receive operations occur separately and simultaneously without interference.

The VLYNQ enables the extension of an internal bus segment to one or more external physical devices. The external devices are mapped to local physical address space and appear as if they are on the internal bus of the DM646x DMSoC. The external devices must also have a VLYNQ interface.

The general features of the VLYNQ port are:

- Low pin count (10 pin interface, scalable to as low as 3 pins)
- No tri-state signals
 - All signals are dedicated and driven by only one device
 - Necessary to allow support for high-speed PHYs
- Scalable Performance
 - Programmable frequency and 1 to 4 bits for TX and RX data
 - Performance increases linearly as the data port width increases
- Simple packet-based transfer protocol for memory-mapped access
 - Write request/data packet
 - Read request packet
 - Read response data packet
 - Interrupt request packet
- Auto width negotiation
- Symmetric Operations
 - Transmit (TX) pins on the first device connect to the receive (RX) pins on the second device and vice-versa.
 - Data pin widths are automatically detected after reset
 - Re-request packets, response packets, and flow control information are all multiplexed and sent across the same physical pins.
 - Supports both host/peripheral and peer-to-peer communication models
- Simple block code packet formatting (8b/10b)
- Supports in-band and flow control
 - No extra pins are needed
 - Allows the receiver to momentarily throttle the transmitter back when overflow is about to occur
 - Uses the special built-in block code capability to interleave flow control information seamlessly with user data

- Automatic packet formatting optimizations
- Internal loopback modes are provided

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