TMS320DM647/DM648 DSP 64-Bit Timer

User's Guide

Literature Number: SPRUEL0B
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About This Manual

Describes the operation of the software-programmable 64-bit timer in the TMS320DM647/DM648 Digital Signal Processor (DSP). Timer 0, Timer 1, Timer2, and Timer3 are used as general-purpose (GP) timers and can be programmed in 64-bit mode, dual 32-bit unchained mode, or dual 32-bit chained mode. The GP timer modes can be used to generate periodic interrupts or enhanced direct access (EDMA) synchronization events.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Note: Acronyms 3PSW, CPSW, CPSW_3G, and 3pGSw are interchangeable and all refer to the 3 port gigabit switch.

Related Documentation From Texas Instruments

The following documents describe the TMS320DM647/DM648 Digital Signal Processor (DSP). Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

SPRU732 — ***TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide*** describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C64x and TMS320C64x+ digital signal processors (DSPs) of the TMS320C6000 DSP family. The C64x/C64x+ DSP generation comprises fixed-point devices in the C6000 DSP platform. The C64x+ DSP is an enhancement of the C64x DSP with added functionality and an expanded instruction set.

SPRUEK5 — ***TMS320DM647/DM648 DSP DDR2 Memory Controller User's Guide*** describes the DDR2 memory controller in the TMS320DM647/DM648 Digital Signal Processor (DSP). The DDR2/mDDR memory controller is used to interface with JESD79D-2A standard compliant DDR2 SDRAM devices and standard Mobile DDR SDRAM devices.

SPRUEK6 — ***TMS320DM647/DM648 DSP External Memory Interface (EMIF) User's Guide*** describes the operation of the asynchronous external memory interface (EMIF) in the TMS320DM647/DM648 Digital Signal Processor (DSP). The EMIF supports a glueless interface to a variety of external devices.

SPRUEK7 — ***TMS320DM647/DM648 DSP General-Purpose Input/Output (GPIO) User's Guide*** describes the general-purpose input/output (GPIO) peripheral in the TMS320DM647/DM648 Digital Signal Processor (DSP). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an input, you can detect the state of the input by reading the state of an internal register. When configured as an output, you can write to an internal register to control the state driven on the output pin.

SPRUEK8 — ***TMS320DM647/DM648 DSP Inter-Integrated Circuit (I2C) Module User's Guide*** describes the inter-integrated circuit (I2C) peripheral in the TMS320DM647/DM648 Digital Signal Processor (DSP). The I2C peripheral provides an interface between the DSP and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus. External components attached to this 2-wire serial bus can transmit and receive up to 8-bit wide data to and from the DSP through the I2C peripheral. This document assumes the reader is familiar with the I2C-bus specification.

SPRUEL0 — ***TMS320DM647/DM648 DSP 64-Bit Timer User's Guide*** describes the operation of the 64-bit timer in the TMS320DM647/DM648 Digital Signal Processor (DSP). The timer can be configured as a general-purpose 64-bit timer or dual general-purpose 32-bit timers.

SPRUEL1 — ***TMS320DM647/DM648 DSP Multichannel Audio Serial Port (McASP) User's Guide*** describes the multichannel audio serial port (McASP) in the TMS320DM647/DM648 Digital Signal Processor (DSP). The McASP functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP is useful for time-division multiplexed (TDM) stream, Inter-Integrated Sound (I2S) protocols, and intercomponent digital audio interface transmission (DIT).

SPRUEL2 — ***TMS320DM647/DM648 DSP Enhanced DMA (EDMA) Controller User's Guide*** describes the operation of the enhanced direct memory access (EDMA3) controller in the TMS320DM647/DM648 Digital Signal Processor (DSP). The EDMA3 controller's primary purpose is to service user-programmed data transfers between two memory-mapped slave endpoints on the DSP.

SPRUEL4 — ***TMS320DM647/DM648 DSP Peripheral Component Interconnect (PCI) User's Guide*** describes the peripheral component interconnect (PCI) port in the TMS320DM647/DM648 Digital Signal Processor (DSP). The PCI port supports connection of the C642x DSP to a PCI host via the integrated PCI master/slave bus interface. The PCI port interfaces to the DSP via the enhanced DMA (EDMA) controller. This architecture allows for both PCI master and slave transactions, while keeping the EDMA channel resources available for other applications.

SPRUEL5 — ***TMS320DM647/DM648 DSP Host Port Interface (UHPI) User's Guide*** describes the host port interface (HPI) in the TMS320DM647/DM648 Digital Signal Processor (DSP). The HPI is a parallel port through which a host processor can directly access the CPU memory space. The host device functions as a master to the interface, which increases ease of access. The host and CPU can exchange information via internal or external memory. The host also has direct access to memory-mapped peripherals. Connectivity to the CPU memory space is provided through the enhanced direct memory access (EDMA) controller.

SPRUEL8 — ***TMS320DM647/DM648 DSP Universal Asynchronous Receiver/Transmitter (UART) User's Guide*** describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320DM647/DM648 Digital Signal Processor (DSP). The UART peripheral performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data received from the CPU.

SPRUEL9 — ***TMS320DM647/DM648 DSP VLYNQ Port User's Guide*** describes the VLYNQ port in the TMS320DM647/DM648 Digital Signal Processor (DSP). The VLYNQ port is a high-speed point-to-point serial interface for connecting to host processors and other VLYNQ compatible devices. It is a full-duplex serial bus where transmit and receive operations occur separately and simultaneously without interference.

SPRUEM1 — ***TMS320DM647/DM648 DSP Video Port/VCXO Interpolated Control (VIC) Port User's Guide*** discusses the video port and VCXO interpolated control (VIC) port in the TMS320DM647/DM648 Digital Signal Processor (DSP). The video port can operate as a video capture port, video display port, or transport channel interface (TCI) capture port. The VIC port provides single-bit interpolated VCXO control with resolution from 9 bits to up to 16 bits. When the video port is used in TCI mode, the VIC port is used to control the system clock, VCXO, for MPEG transport channel.

SPRUEM2 — ***TMS320DM647/DM648 DSP Serial Port Interface (SPI) User's Guide*** discusses the Serial Port Interface (SPI) in the TMS320DM647/DM648 Digital Signal Processor (DSP). This reference guide provides the specifications for a 16-bit configurable, synchronous serial peripheral interface. The SPI is a programmable-length shift register, used for high speed communication between external peripherals or other DSPs.

SPRUEU6 — **TMS320DM647/DM648 DSP Subsystem User's Guide** describes the subsystem in the TMS320DM647/DM648 Digital Signal Processor (DSP). The subsystem is responsible for performing digital signal processing for digital media applications. The subsystem acts as the overall system controller, responsible for handling many system functions such as system-level initialization, configuration, user interface, user command execution, connectivity functions, and overall system control.

SPRUF57 — **TMS320DM647/DM648 DSP 3 Port Switch (3PSW) Ethernet Subsystem User's Guide** describes the operation of the 3 port switch (3PSW) ethernet subsystem in the TMS320DM647/DM648 Digital Signal Processor (DSP). The 3 port switch gigabit ethernet subsystem provides ethernet packet communication and can be configured as an ethernet switch (DM648 only). It provides the serial gigabit media independent interface (SGMII), the management data input output (MDIO) for physical layer device (PHY) management.

Trademarks

64-Bit Timer

1 Introduction

This document describes the operation of the software-programmable 64-bit timer in the TMS320DM647/DM648 Digital Signal Processor (DSP). The processor contains four software-programmable general purpose timer of which only Timer0 and Timer1 have external input/output. Timer 0, Timer 1, Timer2, Timer3 each of which can be configured as a general-purpose timer. When configured as a general purpose timer, each timer can be programmed in 64-bit mode, dual 32-bit unchained mode (operated independently), or dual 32-bit chained mode (operated in conjunction with each other).

1.1 Purpose of the Peripheral

The timers support four modes of operation: a 64-bit general-purpose (GP) timer, dual unchained 32-bit GP timers, or dual chained 32-bit timers. The GP timer modes can be used to generate periodic interrupts or EDMA synchronization events. The capabilities of each of the timers are summarized in Table 1.

Table 1. Supported Timer Features by Instantiation

Capability	Timer 0	Timer 1	Timer 2	Timer3
64-bit general-purpose timer	√	√	√	√
Dual 32-bit general-purpose timer (unchained)	√	√	√	√
Dual 32-bit general-purpose timer (chained)	√	√	√	√
External clock input T0INPL and T1INPL Pins	√	√	–	–
External clock output T0OUTL and T1OUTL Pins	√	√	–	–

1.2 Features

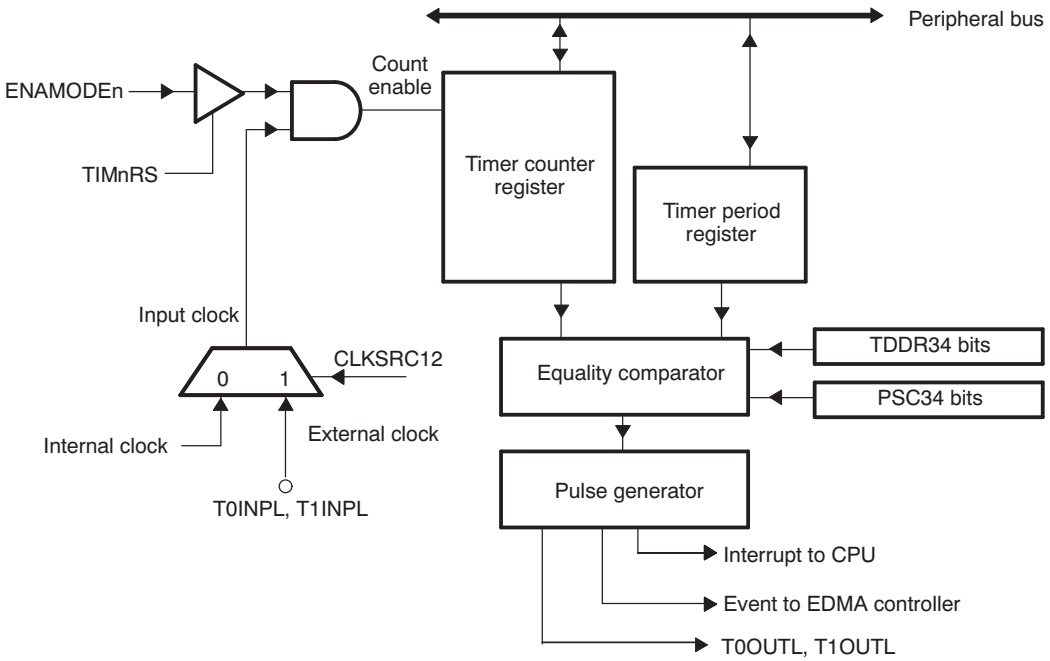
The 64-bit timer consists of the following features.

- 64-bit count-up counter
- Timer modes:
  - 64-bit general-purpose timer mode
  - Dual 32-bit general-purpose timer mode
- 2 possible clock sources:
  - Internal clock
  - External clock input via T0INPL and T1INPL Pins
- 2 possible operation modes:
  - One-time operation (timer runs for one period then stops)
  - Continuous operation (timer automatically resets after each period)
- Generates interrupt to the CPU
- Generates sync event to EDMA

1.3 Functional Block Diagram

A block diagram of the timer is shown in Figure 1. Detailed information about the architecture and operation of the timers is in Section 2.

Figure 1. Timer Block Diagram



1.4 Industry Standard Compatibility Statement

This peripheral is not intended to conform to any specific industry standard.

2 Architecture – General-Purpose Timer Mode

This section describes the timer in the general-purpose (GP) timer mode. The timer can be configured as a 64-bit general-purpose (GP) timer, using the TIMMODE bits in the TGCR register. At reset, the timer is in 64-bit (GP) timer mode.

2.1 Clock Control

The timer can use an internal or external clock source for the counter period. The following sections explain how to select the clock source. Table 2 shows which clock sources are supported on each timer.

Table 2. Supported Timer Clock Sources

Clock Source	Timer 0	Timer 1	Timer 2	Timer 3
Internal clock source	√	√	√	√
External clock input T0INPL and T1INPL Pins	√	√	-	-

As shown in Table 3 and Figure 2, the timer clock source is selected using the clock source (CLKSRC12) bit in the timer control register (TCR). Three clock sources are available to drive the timer clock:

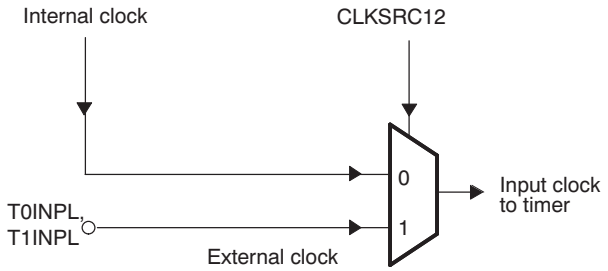
- internal clock, by setting CLKSRC12 = 0 and TIEN = 0
- external clock on timer input pin (T0INPL/T1INPL), by setting CLKSRC12 = 1. This input signal is synchronized internally.

At reset, the clock source is the internal clock. Details on each of the clock source configuration options are included in the following sections.

Table 3. Timer Clock Source Selection

CLKSRC12	TIEN	Input Clock
0	0	Internal clock (default)
1	x	External clock on timer input (T0INPL, T1INPL pin)

Figure 2. Timer Clock Source Block Diagram



2.1.1 Using the Internal Clock Source to the Timer

The internal clock source to the timer is generated by the PLL1 controller and is a divide-down verison of the CPU clock (see device-specific data manual for more information). This clock source determines the speed of the timer since the timer counts up based on each cycle of the clock source. When determining the period and prescalers settings for the timer, choose the desired period in terms of number of cycles of ths divide-down version of CPU clock. For details on the generation of the on-chip clocks, see the DSP Subsystem User's Guide.

The CLKSRC12 parameter in the timer control register (TCR) controls whether the internal or external clock is used as the clock source for the timer. If the timer is configured in 64-bit mode or 32-bit chained mode, CLKSRC12 controls the clock source for the entire timer. If the timer is configured in dual 32-bit unchained mode (TIMMODE = 01 in TGCR), CLKSRC12 controls the timer 1:2 side of the timer. The timer 3:4 side must use the internal clock.

To select the internal clock as the clock source for the timer, CLKSRC12 in TCR must be cleared to 0. If the timer being used does not support an external clock source, CLKSRC12 must always be 0.

2.1.2 Using the External Clock Source to the Timer

An external clock source can be provided to clock the timer via the T0INPL, T1INPL pin.

The CLKSRC12 parameter in the timer control register (TCR) controls whether the internal or external clock is used as the clock source for the timer. If the timer is configured in 64-bit mode or 32-bit chained mode, CLKSRC12 controls the clock source for the entire timer. If the timer is configured in dual 32-bit unchained mode (TIMMODE = 01 in TGCR), CLKSRC12 controls the timer 1:2 side of the timer. The timer 3:4 side must use the internal clock.

To select the external clock as the clock source for the timer, CLKSRC12 in TCR must be set to 1.

2.2 Signal Descriptions

The timer module provides only one input signal for the timer instantiation. The timer input T0INPL/T1INPL is connected to the input clock circuit to allow timer synchronization to audio streams. The external timer input clock frequency must be no greater than CPU/6.

2.3 Timer Modes

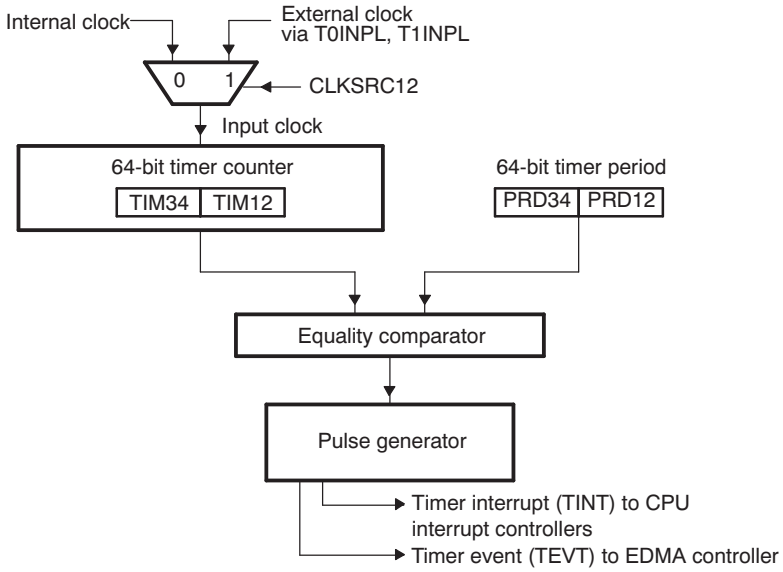
The timer can be configured as a 64-bit general-purpose(GP) timer, using the TIMMODE bits in the TGCR register. At reset, the timer is in 64-bit GP timer mode. The following section describes the general-purpose (GP) timer modes.

2.3.1 64-Bit Timer Mode

The general-purpose timers can each be configured as a 64-bit timer by clearing the TIMMODE bit in the timer global control register (TGCR) to 0. At reset, 0 is the default setting for the TIMMODE bit.

In this mode, the timer operates as a single 64-bit up-counter (Figure 3). The counter registers (TIM12 and TIM34) form a 64-bit timer counter register and the period registers (PRD12 and PRD34) form a 64-bit timer period register. When the timer is enabled, the timer counter starts incrementing by 1 at every timer input clock cycle. When the timer counter matches the timer period, a maskable timer interrupt (TINT*n*) and a timer EDMA (TEVT) are generated. When the timer is configured in continuous mode, the timer counter is reset to 0 on the cycle after the timer counter reaches the timer period. The timer can be stopped, restarted, reset, or disabled using control bits in TGCR.

Figure 3. 64-Bit Timer Mode Block Diagram



2.3.1.1 Enabling the 64-Bit Timer

The TIM12RS and TIM34RS bits in TGCR control whether the timer is in reset or capable of operating. For the timer to operate in 64-bit timer mode, the TIM12RS and TIM34RS bits must be set to 1.

The ENAMODE12 bit in the timer control register (TCR) controls whether the timer is disabled, enabled to run once, or enabled to run continuously; the ENAMODE34 bit has no effect in 64-bit timer mode. When the timer is disabled (ENAMODE12 = 0), the timer does not run and maintains its current count value. When the timer is enabled for one time operation (ENAMODE12 = 1), it counts up until the counter value equals the period value and then stops. When the timer is enabled for continuous operation (ENAMODE12 = 2h), the counter counts up until it reaches the period value, then resets itself to zero and begins counting again.

Table 4 shows the bit values in TGCR to configure the 64-bit timer.

Table 4. 64-Bit Timer Configurations

64-Bit Timer Configuration	TGCR Bit		TCR Bit
	TIM12RS	TIM34RS	ENAMODE12
To place the 64-bit timer in reset	0	0	0
To disable the 64-bit timer (out of reset)	1h	1h	0
To enable the 64-bit timer for one-time operation	1h	1h	1h
To enable the 64-bit timer for continuous operation	1h	1h	2h

Once the timer stops, if an external clock is used as the timer clock, the timer must remain disabled for at least one external clock period or the timer will not start counting again. When using the external clock, the count value is synchronized to the internal clock.

Note that when both the timer counter and timer period are cleared to 0, the timer can be enabled but the timer counter does not increment because the timer period is 0.

2.3.1.2 Reading the Counter Registers

When reading the timer count in 64-bit timer mode, the CPU must first read TIM12 followed by TIM34. When TIM12 is read, the timer copies TIM34 into a shadow register. When reading TIM34, the hardware logic forces the reads to read from the shadow register. This ensures that the values read from the registers are not affected by the fact that the timer may continue to run as the registers are read. When reading the timers in 32-bit mode, TIM12 and TIM34 may be read in either order.

2.3.1.3 64-Bit Timer Configuration Procedure

To configure the GP timer to operate as a 64-bit timer, follow the steps below:

1. Select 64-bit mode (TIMMODE in TGCR).
2. Remove the timer from reset (TIM12RS and TIM34RS in TGCR).
3. Select the desired timer period (PRD12 and PRD34).
4. Enable the timer (ENAMODE12 in TCR).

2.3.2 Dual 32-Bit Timer Modes

Each of the general-purpose timers can be configured as dual 32-bit timers by configuring the TIMMODE bit in the timer global control register (TGCR). In dual 32-bit timer mode, the two 32-bit timers can be operated independently (unchained mode) or in conjunction with each other (chained mode).

2.3.2.1 Chained Mode

The general-purpose timers can each be configured as a dual 32-bit chained timer by setting the TIMMODE bit to 3h in TGCR.

In the chained mode (Figure 4), one 32-bit timer (timer 3:4) is used as a 32-bit prescaler and the other 32-bit timer (timer 1:2) is used as a 32-bit timer. The 32-bit prescaler is used to clock the 32-bit timer. The 32-bit prescaler uses one counter register (TIM34) to form a 32-bit prescale counter register and one period register (PRD34) to form a 32-bit prescale period register.

When the timer is enabled, the prescale counter starts incrementing by 1 at every timer input clock cycle. One cycle after the prescale counter matches the prescale period, a clock signal is generated and the prescale counter register is reset to 0 (see the example in Figure 5).

The other 32-bit timer (timer 1:2) uses one counter register (TIM12) to form a 32-bit timer counter register and one period register (PRD12) to form a 32-bit timer period register. This timer is clocked by the output clock from the prescaler. The timer counter increments by 1 at every prescaler output clock cycle. When the timer counter matches the timer period, a maskable timer interrupt (TINT) and a timer EDMA event (TEVT) are generated. When the timer is configured in continuous mode, the timer counter is reset to 0 on the cycle after the timer counter reaches the timer period. The timer can be stopped, restarted, reset, or disabled using the TIM12RS and TIM34RS bits in TGCR. In the chained mode, the upper 16-bits of the timer control register (TCR) are not used.

Figure 4. Dual 32-Bit Timers Chained Mode Block Diagram

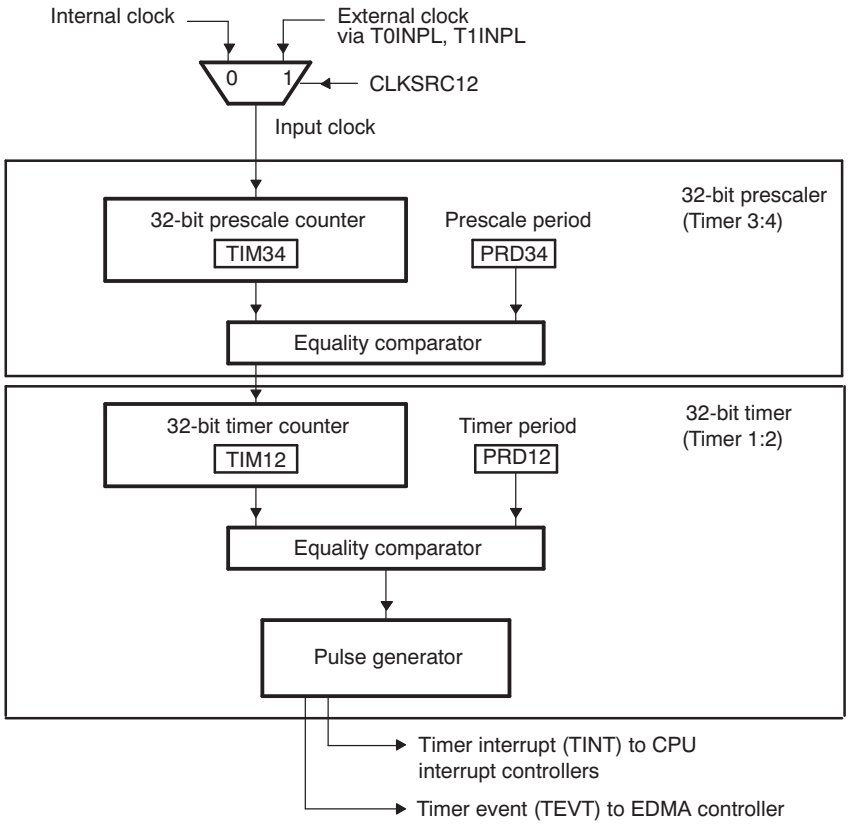
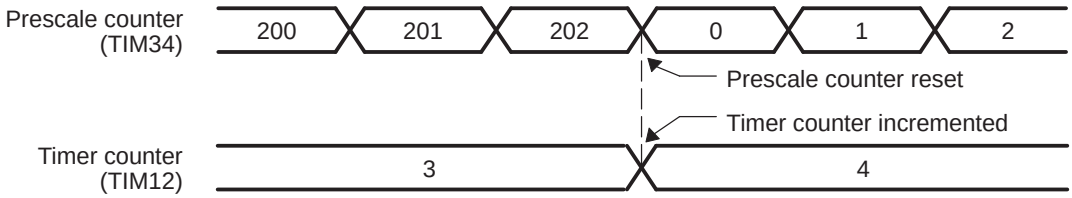


Figure 5. Dual 32-Bit Timers Chained Mode Example

32-bit prescaler settings: count = TIM34 = 200; period = PRD34 = 202
32-bit timer settings: count = TIM12 = 3; period = PRD12= 4



2.3.2.1.1 Enabling the 32-Bit Timer Chained Mode

The TIM12RS and TIM34RS bits in TGCR control whether the timer is in reset or capable of operating. The TIM12RS bit controls the reset of the timer 1:2 side of the timer and the TIM34RS bits control the reset of the timer 3:4 side of the timer. For the timer to operate, the TIM12RS and TIM34RS bits must be set to 1.

The ENAMODE12 bit in the timer control register (TCR) controls whether the timer is disabled, enabled to run once, or enabled to run continuously; the ENAMODE34 bit has no effect in 32-bit timer chained mode. When the timer is disabled (ENAMODE12 = 0), the timer does not run and maintains its current count value. When the timer is enabled for one time operation (ENAMODE12 = 1), it counts up until the counter value equals the period value and then stops. When the timer is enabled for continuous operation (ENAMODE12 = 2h), the counter counts up until it reaches the period value, then resets itself to zero and begins counting again.

Table 5 shows the bit values in TGCR to configure the 32-bit timer in chained mode.

Table 5. 32-Bit Timer Chained Mode Configurations

	TGCR Bit		TCR Bit
32-Bit Timer Configuration	**TIM12RS**	**TIM34RS**	**ENAMODE12**
To place the 32-bit timer chained mode in reset	0	0	0
To disable the 32-bit timer chained mode (out of reset)	1h	1h	0
To enable the 32-bit timer chained mode for one-time operation	1h	1h	1h
To enable the 32-bit timer chained mode for continuous operation	1h	1h	2h

Once the timer stops, if an external clock is used as the timer clock, the timer must remain disabled for at least one external clock period or the timer will not start counting again. When using the external clock, the count value is synchronized to the internal clock.

Note that when both the timer counter and timer period are cleared to 0, the timer can be enabled but the timer counter does not increment because the timer period is 0.

2.3.2.1.2 32-Bit Timer Chained Mode Configuration Procedure

To configure the GP timer to operate as a dual 32-bit chained mode timer, follow the steps below:

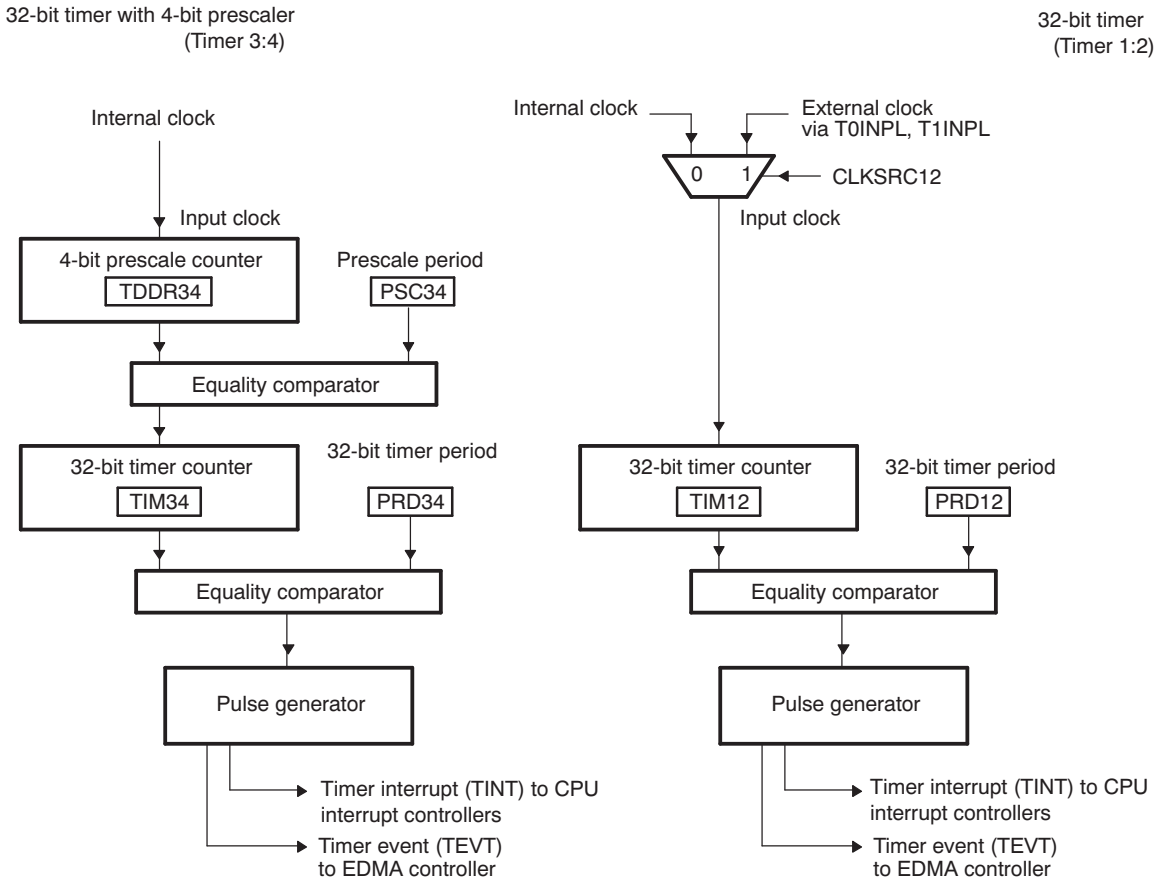
1. Select 32-bit chained mode (TIMMODE in TGCR).
2. Remove the timer from reset (TIM12RS and TIM34RS in TGCR).
3. Select the desired timer period (PRD12).
4. Select the desired timer prescaler value (PRD34).
5. Enable the timer (ENAMODE12 in TCR).

2.3.2.2 Unchained Mode

The general-purpose timers can each be configured as a dual 32-bit unchained timers by setting the TIMMODE bit to 1 in TGCR.

In the unchained mode (Figure 6), the timer operates as two independent 32-bit timers. One 32-bit timer (timer 3:4) operates as a 32-bit timer being clocked by a 4-bit prescaler. The other 32-bit timer (timer 1:2) operates as a 32-bit timer with no prescaler.

Figure 6. Dual 32-Bit Timers Unchained Mode Block Diagram

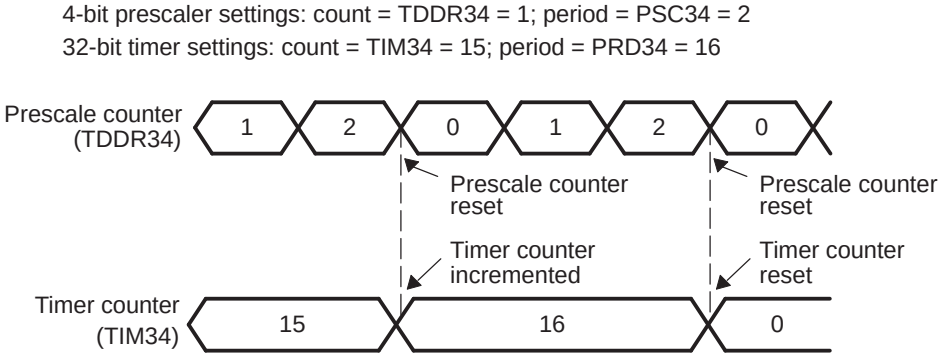


2.3.2.2.1 32-Bit Timer With a 4-Bit Prescaler

In the unchained mode, the 4-bit prescaler must be clocked by the internal clock; an external clock source cannot be used for timer 3:4. The 4-bit prescaler uses the timer divide-down ratio (TDDR34) bit in TGCR to form a 4-bit prescale counter register and the prescale counter bits (PSC34) to form a 4-bit prescale period register (see Figure 6). When the timer is enabled, the prescale counter starts incrementing by 1 at every timer input clock cycle. One cycle after the prescale counter matches the prescale period, a clock signal is generated for the 32-bit timer.

The 32-bit timer uses TIM34 as a 32-bit timer counter register and PRD34 as a 32-bit timer period register. The 32-bit timer is clocked by the output clock from the 4-bit prescaler (see the example in Figure 7). The timer counter increments by 1 at every prescaler output clock cycle. When the timer counter matches the timer period, a maskable timer interrupt (TINT*n*) and a timer EDMA event (TEVTn) are generated. The state of the timer is read in the timer status (TSTAT) bit of the timer control register. When in pulse mode (CP = 0), TSTAT stays high or low for 1,2,3, or 4 time clock cycles. The pulse width depends on the setting of the pulse width (PWID) in TCR. When in clock mode (CP = 1), the TSTAT bit changes state (high-to-low or low-to-high) every time the timer counter matches the timer period. When the timer is configured in continuous mode, the timer counter is reset to 0 on the cycle after the timer counter reaches the timer period. The timer can be stopped, restarted, reset, or disabled using the TIM34RS bit in TGCR. For timer 3:4, the lower 16 bits of the timer control register (TCR) have no control.

Figure 7. Dual 32-Bit Timers Unchained Mode Example



2.3.2.2.2 32-Bit Timer with No Prescaler

The other 32-bit timer (timer 1:2) uses TIM12 as the 32-bit counter register and PRD12 as a 32-bit timer period register (see Figure 6). When the timer is enabled, the timer counter increments by 1 at every timer input clock cycle. When the timer counter matches the timer period, a maskable timer interrupt (TINT*n*) and a timer EDMA event (TEVTn) are generated. The state of the timer is read in the timer status (TSTAT) bit of the timer control register. When in pulse mode (CP = 0), TSTAT stays high or low for 1,2,3, or 4 time clock cycles. The pulse width depends on the setting of the pulse width (PWID) in TCR. When in clock mode (CP = 1), the TSTAT bit changes state (high-to-low or low-to-high) every time the timer counter matches the timer period. When the timer is configured in continuous mode, the timer counter is reset to 0 on the cycle after the timer counter reaches the timer period. The timer can be stopped, restarted, reset, or disabled using the TIM12RS bit in TGCR. For timer 1:2, the upper 16 bit of the timer control register (TCR) have no control.

2.3.2.2.3 Enabling the 32-Bit Unchained Mode Timer

The TIM12RS and TIM34RS bits in TGCR control whether the timer is in reset or capable of operating. The TIM12RS bit controls the reset of the timer 1:2 side of the timer and the TIM34RS bit controls the reset of the timer 3:4 side of the timer. For the timer to operate, the TIM12RS and/or TIM34RS bits must be set to 1.

The ENAMODE*n* bit in the timer control register (TCR) controls whether the timer is disabled, enabled to run once or enabled to run continuously. When the timer is disabled (ENAMODE*n* = 0), the timer does not run and maintains its current count value. When the timer is enabled for one time operation (ENAMODE*n* = 1), it counts up until he counter value equals the period value and then stops. When the timer is enabled for continuous operation (ENAMODE*n* = 2h), the counter counts up until it reaches the period value, then resets itself to zero and begins counting again.

Table 6 shows the bit values in TGCR to configure the 32-bit timer in unchained mode.

Once the timer stops, if an external clock is used as the timer clock, the timer must remain disabled for at least one external clock period or the timer will not start counting again. When using the external clock, the count value is synchronized to the internal clock. External clock is only available on the timer 1:2 side in unchained mode.

Note that when both the timer counter and timer period are cleared to 0, the timer can be enabled but the timer counter does not increment because the timer period is 0.

Table 6. 32-Bit Timer Unchained Mode Configurations

	TGCR Bit		TCR Bit	
32-Bit Timer Configuration	**TIM12RS**	**TIM34RS**	**ENAMODE12**	**ENAMODE34**
To place the 32-bit timer unchained mode with 4-bit prescaler in reset	x	0	x	0
To disable the 32-bit timer unchained mode with 4-bit prescaler (out of reset)	x	1h	x	0
To enable the 32-bit timer unchained mode with 4-bit prescaler for one-time operation	x	1h	x	1h
To enable the 32-bit timer unchained mode with 4-bit prescaler for continuous operation	x	1h	x	2h
To place the 32-bit timer unchained mode with no prescaler in reset	0	x	0	x
To disable the 32-bit timer unchained mode with no prescaler (out of reset)	1h	x	0	x
To enable the 32-bit timer unchained mode with no prescaler for one-time operation	1h	x	1h	x
To enable the 32-bit timer unchained mode with no prescaler for continuous operation	1h	x	2h	x

2.3.2.2.4 32-Bit Timer Unchained Mode Configuration Procedure

To configure timer 1:2, follow the steps below:

1. Select 32-bit unchained mode (TIMMODE in TGCR).
2. Remove the timer 1:2 from reset (TIM12RS in TGCR).
3. Select the desired timer period for timer 1:2 (PRD12).
4. Select the desired clock source for timer 1:2 (CLKSRC12 in TCR).
5. Enable timer 1:2 (ENAMODE12 in TCR).

To configure timer 3:4, follow the steps below:

1. Select 32-bit unchained mode (TIMMODE in TGCR).
2. Remove the timer 3:4 from reset (TIM34RS in TGCR).
3. Select the desired timer period for timer 3:4 (PRD34).
4. Select the desired prescaler value for timer 3:4 (PSC34 in TGCR).
5. Enable timer 3:4 (ENAMODE34 in TCR).

2.3.3 Counter and Period Registers Used in GP Timer Modes

Table 7 summarizes how the counter registers (TIM*n*) and period registers (PRD*n*) are used in each GP timer mode.

Table 7. Counter and Period Registers Used in GP Timer Modes

Timer Mode	Counter Registers	Period Registers
64-bit general-purpose	TIM34:TIM12	PRD34:PRD12
Dual 32-bit chained		
Prescaler (TIM34)	TIM34	PRD34
Timer (TIM12)	TIM12	PRD12
Dual 32-bit unchained		
Timer (TIM12)	TIM12	PRD12
Timer with prescaler (TIM34)	TDDR34 bits and TIM34	PSC34 bits and PRD34

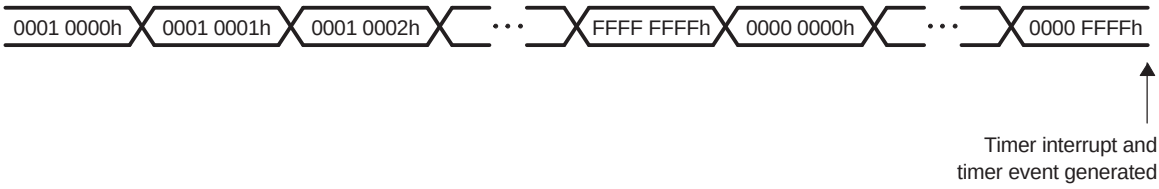
2.4 Timer Operation Boundary Conditions

The following boundary conditions affect the timer operation.

2.4.1 Timer Counter Overflow

Timer counter overflow can happen when the timer counter register is set to a value greater than the value in the timer period register. The counter reaches its maximum value (FFFF FFFFh or FFFF FFFF FFFF FFFFh), rolls over to 0, and continues counting until it reaches the timer period. An example is in Figure 8.

Figure 8. 32-Bit Timer Counter Overflow Example



2.4.2 Writing to Registers of an Active Timer

Writes to the timer registers are not allowed when the timer is active, except for stopping or resetting the timers. In the 64-bit and dual 32-bit timer modes, registers that are protected by hardware are:

- TIM12
- TIM34
- PRD12
- PRD34
- TCR (except the ENAMODE bit)
- TGCR (except the TIM12RS and TIM34RS bits)

2.5 General-Purpose Timer Power Management

The timer can be placed in reduced power modes to conserve power during periods of low activity. The power management of the peripheral is controlled by the processor Power and Sleep Controller (PSC). The PSC acts as a master controller for power management for all of the peripherals on the device. For detailed information on power management procedures using the PSC, see the DSP Subsystem User's Guide. The timer can be placed in an idle mode to conserve power when it is not being used.

3 Reset Considerations

The timer has two reset sources: hardware reset and the timer reset (TIM12RS and TIM34RS) bits in the timer global control register (TGCR).

3.1 Software Reset Considerations

When the TIM12RS bit in the timer global control register (TGCR) is cleared to 0, the TIM12 register is held with the current value, TSTAT in TCR is reset to 0.

When the TIM34RS bit in the timer global control register (TGCR) is cleared to 0, the TIM34 register is held with the current value, TSTAT in TCR is reset to 0.

3.2 Hardware Reset Considerations

When a hardware reset is asserted, all timer registers are set to their default values.

4 Interrupt Support

Each of the timers can send either one of two separate interrupt events (TINT*n*) to the CPU, depending on the operating mode of the timer. The timer interrupts are generated when the count value in the counters register reaches the value specified in the period register.

Table 8 shows the interrupts generated in each mode on each instance of the timer.

Table 8. Timer Interrupts Generated

	Timer 0	Timer 1	Timer 2	Timer 3
Timer Mode	**CPU**	**CPU**	**CPU**	**CPU**
64-bit mode	TINT0L	TINT1L	TINT2L	TINT3L
32-bit chained mode	TINT0L	TINT1L	TINT2L	TINT3L
32-bit unchained mode without prescaler (TIM12)	TINT0L	TINT1L	TINT2L	TINT3L
32-bit unchained mode with prescaler (TIM34)	TINT0H	TINT1H	TINT2H	TINT3H

5 EDMA Event Support

Each of the timers can send either one of two separate timer events (TEVT*n*) to the EDMA, depending on the operating mode of the timer. The timer events are generated when the count value in the counters register reaches the value specified in the period register.

Table 9 shows the EDMA events generated in each mode on each instance of the timer.

Table 9. Timer EDMA Events Generated

	Timer 0	Timer 1	Timer 2	Timer 3
Timer Mode	**CPU**	**CPU**	**CPU**	**CPU**
64-bit mode	TEVT0L	TEVT1L	TEVT2L	TEVT3L
32-bit chained mode	TEVT0L	TEVT1L	TEVT2L	TEVT3L
32-bit unchained mode without prescaler (timer 1:2)	TEVT0L	TEVT1L	TEVT2L	TEVT3L
32-bit unchained mode with prescaler (timer 3:4)	TEVT0H	TEVT1H	TEVT2H	TEVT3H

6 Power Management

The general purpose timers can be placed in reduced power modes to conserve power during periods of low activity. The power management of the peripheral is controlled by the processor Power and Sleep Controller (PSC). The PSC acts as a master controller for power management for all of the peripherals on the device. For detailed information on power management procedures using the PSC, see the DSP Subsystem User's Guide.

7 Emulation Considerations

Each timer has an emulation management register (EMUMGT). As shown in Table 10, the FREE and SOFT bits of EMUMGT determine how the timer responds to an emulation suspend event. An emulation suspend event corresponds to any type of emulator access to the CPU, such as a hardware or software breakpoint or a probe point.

Table 10. Timer Emulation Modes Selection

FREE	SOFT	Emulation Mode
0	0	The timer stops immediately.
0	1	The timer stops when the timer counter value increments and reaches the value in the timer period register.
1	x	The timer runs free regardless of SOFT bit status.

Note that during emulation, the timer count values will increment once every timer peripheral clock (not CPU clock). So when single-steeping though code, the timer values will not update on every CPU clock cycle.

8 Registers

Table 11 lists the memory-mapped registers for the 64-bit timer. See the device-specific data manual for the memory address of these registers. All other register offset addresses not listed in Table 11 should be considered as reserved locations and the register contents should not be modified.

Table 11. 64-Bit Timer Registers

Offset	Acronym	Register Description	Section
00h	PID12	Peripheral Identification Register 12	Section 8.1
04h	EMUMGT	Emulation Management Register	Section 8.2
10h	TIM12	Timer Counter Register 12	Section 8.3
14h	TIM34	Timer Counter Register 34	Section 8.3
18h	PRD12	Timer Period Register 12	Section 8.4
1Ch	PRD34	Timer Period Register 34	Section 8.4
20h	TCR	Timer Control Register	Section 8.5
24h	TGCR	Timer Global Control Register	Section 8.6

8.1 *Peripheral Identification Register 12 (PID12)*

The peripheral ID register 12 (PID12) contains identification data (type, class, and revision) for the peripheral. The PID12 is shown in Figure 9 and described in Table 12.

Figure 9. Peripheral Identification Register 12 (PID12)

31	23	22	16
Reserved		TYPE	
R-0		R-01h	

15	8	7	0
CLASS		REVISION	
R-07h		R-01h	

LEGEND: R = Read only; -*n* = value after reset

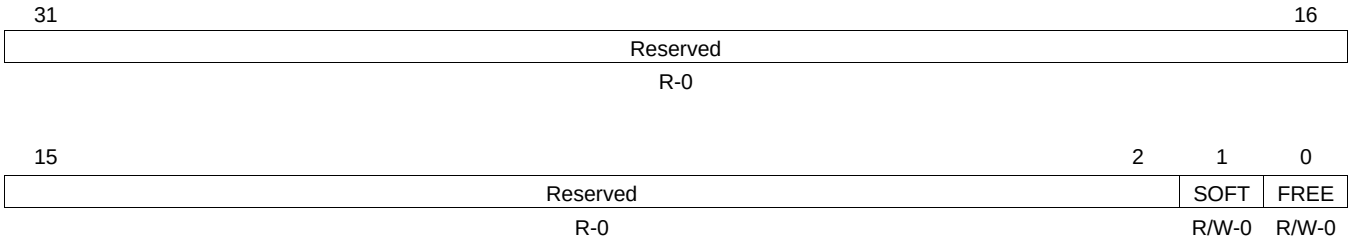
Table 12. Peripheral Identification Register 12 (PID12) Field Descriptions

Bit	Field	Value	Description
31-23	Reserved	0	Reserved
22-16	TYPE		Identifies type of peripheral
		01h	Timer
15-8	CLASS		Identifies class of peripheral
		07h	Timer
7-0	REVISION		Identifies revision of peripheral.
		01h	Current revision of peripheral.

8.2 Emulation Management Register (EMUMGT)

The emulation management register (EMUMGT) is shown in Figure 10 and described in Table 13.

Figure 10. Emulation Management Register (EMUMGT)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 13. Emulation Management Register (EMUMGT) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Reserved
1	SOFT		Determines emulation mode functionality of the timer. When the FREE bit is cleared to 0, the SOFT bit selects the timer mode.
		0	The timer stops immediately.
		1	The timer stops when the counter increments and reaches the value in the timer period register (PRD*n*).
0	FREE		Determines emulation mode functionality of the timer. When the FREE bit is cleared to 0, the SOFT bit selects the timer mode.
		0	The SOFT bit selects the timer mode.
		1	The timer runs free regardless of the SOFT bit.

8.3 Timer Counter Registers (TIM12 and TIM34)

The timer counter register is a 64-bit wide register. This 64-bit register is divided into two 32-bit registers, TIM12 and TIM34.

In the dual 32-bit timer mode, the 64-bit register is divided with TIM12 acting as one 32-bit counter and TIM34 acting as another. These two registers can be configured as chained or unchained.

8.3.1 Timer Counter Register 12 (TIM12)

The timer counter register 12 (TIM12) is shown in Figure 11 and described in Table 14

Figure 11. Timer Counter Register 12 (TIM12)

31	16
TIM12	
R/W-0	

15	0
TIM12	
R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14. Timer Counter Register 12 (TIM12) Field Descriptions

Bit	Field	Value	Description
31-0	TIM12	0-FFFF FFFFh	TIM12 count bits. This 32-bit value is the current count of the main counter.

8.3.2 Timer Counter Register 34 (TIM34)

The timer counter register 34 (TIM34) is shown in Figure 12 and described in Table 15.

Figure 12. Timer Counter Register 34 (TIM34)

31	16
TIM34	
R/W-0	

15	0
TIM34	
R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 15. Timer Counter Register 34 (TIM34) Field Descriptions

Bit	Field	Value	Description
31-0	TIM34	0-FFFF FFFFh	TIM34 count bits. This 32-bit value is the current count of the main counter.

8.4 Timer Period Registers (PRD12 and PRD34)

The timer period register is a 64-bit wide register. This 64-bit register is divided into two 32-bit registers, PRD12 and PRD34.

Similar to TIM*n* in the dual 32-bit timer mode, PRD*n* can be divided into 2 registers: for timer 1:2, PRD12 and for timer 3:4, PRD34. These two registers can be used in conjunction with the two timer counter registers TIM12 and TIM34.

8.4.1 Timer Period Register (PRD12)

The timer period register 12 (PRD12) is shown in Figure 13 and described in Table 16.

Figure 13. Timer Period Register 12 (PRD12)

31	16
PRD12	
R/W-0	

15	0
PRD12	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 16. Timer Period Register (PRD12) Field Descriptions

Bit	Field	Value	Description
31-0	PRD12	0-FFFF FFFFh	PRD12 period bits. This 32-bit value is the number of timer input clock cycles to count.

8.4.2 Timer Period Register 34 (PRD34)

The timer period register 34 (PRD34) is shown in Figure 14 and described in Table 17.

Figure 14. Timer Period Register 34 (PRD34)

31	16
PRD34	
R/W-0	

15	0
PRD34	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

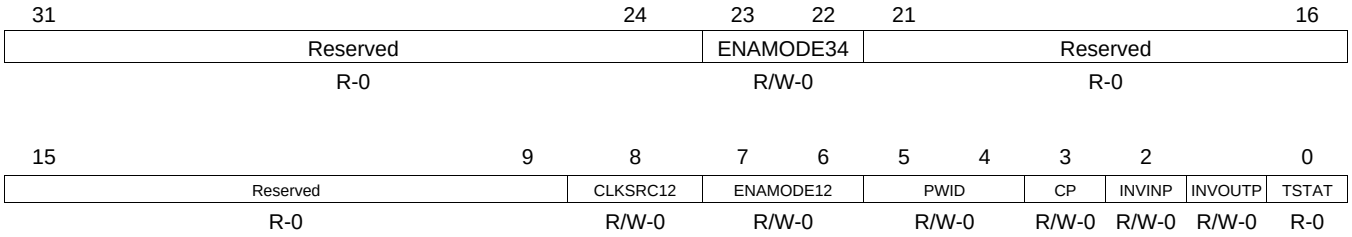
Table 17. Timer Period Register (PRD34) Field Descriptions

Bit	Field	Value	Description
31-0	PRD34	0-FFFF FFFFh	PRD34 period bits. This 16-bit value is the number of timer input clock cycles to count.

8.5 Timer Control Register (TCR)

The timer control register (TCR) is shown in Figure 15 and described in Table 18.

Figure 15. Timer Control Register (TCR)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18. Timer Control Register (TCR) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Reserved
23-22	ENAMODE34	0-3h	ENAMODE34 determines the enabling modes of the timer. Note that ENAMODE34 is applicable only when the timer is configured in dual 32-bit unchained timer mode (TIMMODE = 01 in TGCR).
		0	The timer is disabled (not counting) and maintains current value.
		1h	The timer is enabled one time. The timer stops after the counter reaches the period.
		2h	The timer is enabled continuously, TIM*n* increments until the timer counter matches the period, resets the timer counter to 0 on the cycle after matching and continues.
		3h	Reserved.
21-9	Reserved	0	Reserved
8	CLKSRC12		CLKSRC12 determines the selected clock source for the timer.
		0	Internal clock
		1	Timer input pin
7-6	ENAMODE12	0-3h	ENAMODE12 determines the enabling modes of the timer.
		0	The timer is disabled (not counting) and maintains current value.
		1h	The timer is enabled one time. The timer stops after the counter reaches the period.
		2h	The timer is enabled continuously, TIM*n* increments until the timer counter matches the period, resets the timer counter to 0 on the cycle after matching and continues.
		3h	Reserved.
5-4	PWID	0-3h	Pulse width bits. PWID is only used in pulse mode (CP = 0). PWID controls the width of the timer output signal. The polarity of the pulse is controlled by the INVOUTP bit. The timer output bit is recorded in the TSTAT bit and can be made visible on the timer output pin.
		00b	The pulse width is 1 timer clock cycle.
		01b	The pulse width is 2 timer clock cycle.
		10b	The pulse width is 3 timer clock cycle.
		11b	The pulse width is 4 timer clock cycle.
3	CP		Clock/pulse mode bit for timer output.
		0	Pulse mode. When the timer counter reaches the timer period, the timer output appears as a pulse defined by the PWID bits and the polarity defined by INVOUTP bits.
		1	Clock mode. The timer output signal has a 50% duty cycle signal. When the timer counter reaches the timer period, the level of the timer output signal is toggled.(from low to high or from high to low)
2	INVINP		Timer input inverter control bit. Only affects operation if CLKSRC = 1.
		0	A non-inverted timer input drives the timer.
		1	A inverted timer input drives the timer.

Table 18. Timer Control Register (TCR) Field Descriptions (continued)

Bit	Field	Value	Description
1	INVOUTP		Timer output inverter control bit.
		0	The timer output is inverted.
		1	The timer output is not inverted.
0	TSTAT		Timer status bit. This is a read-only bit that shows the value of the timer output. TSTAT drives the timer pin when the pin is used as a timer output pin and may be inverted by setting INVOUTP = 1.
		0	The timer output is low.
		1	The timer output is high.

8.6 Timer Global Control Register (TGCR)

The timer global control register (TGCR) is shown in Figure 16 and described in Table 19.

Figure 16. Timer Global Control Register (TGCR)

31	16
Reserved	
R-0	

15	12	11	8
TDDR34		PSC34	
R/W-0		R/W-0	

7	4	3	2	1	0
Reserved		TIMMODE		TIM34RS	TIM12RS
R-0		R/W-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 19. Timer Global Control Register (TGCR) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-12	TDDR34	0-Fh	Timer linear divide-down ratio specifies the timer divide-down ratio for timer 3:4. When the timer is enabled, TDDR34 increments every timer clock. The TIM34 counter increments on the cycle after TDDR34 matches PSC34. TDDR34 resets to 0 and continues. When TIM34 matches PRD34, timer 3:4 stops, if timer 3:4 is enabled one time; TIM34 resets to 0 on the cycle after matching PRD34 and timer 3:4 continues, if timer 3:4 is enabled continuously.
11-8	PSC34	0-Fh	TIM34 pre-scalar counter specifies the count for timer 3:4.
7-4	Reserved	0	Reserved
3-2	TIMMODE	0-3h	TIMMODE determines the timer mode.
		0	The timer is in 64-bit GP timer mode.
		1h	The timer is in dual 32-bit timer unchained mode.
		2h	Reserved
		3h	The timer is in dual 32-bit timer, chained mode.
1	TIM34RS		Timer 3:4 reset.
		0	Timer 3:4 is in reset.
		1	Timer 3:4 is not in reset. Timer 3:4 can be used as a 32-bit timer. Note that for the timer to function properly in 64-bit timer mode, both TIM34RS and TIM12RS must be set to 1.
0	TIM12RS		Timer 1:2 reset.
		0	Timer 1:2 is in reset.
		1	Timer 1:2 is not in reset. Timer 1:2 can be used as a 32-bit timer. Note that for the timer to function properly in 64-bit timer mode, both TIM34RS and TIM12RS must be set to 1.

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