TMS320DM643x DMP Peripherals Overview

Reference Guide

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Contents

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About This Manual

This document provides an overview and briefly describes the peripherals available on the TMS320DM643x Digital Media Processor (DMP).

Related Documentation From Texas Instruments

The following documents describe the TMS320DM643x Digital Media Processor (DMP). Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the DM643x DMP, related peripherals, and other technical collateral, is available in the C6000 DSP product folder at: www.ti.com/c6000.

SPRU978 — *TMS320DM643x DMP DSP Subsystem Reference Guide.* Describes the digital signal processor (DSP) subsystem in the TMS320DM643x Digital Media Processor (DMP).

SPRAA84 — *TMS320C64x to TMS320C64x+ CPU Migration Guide.* Describes migrating from the Texas Instruments TMS320C64x digital signal processor (DSP) to the TMS320C64x+ DSP. The objective of this document is to indicate differences between the two cores. Functionality in the devices that is identical is not included.

SPRU732 — *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide.* Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C64x and TMS320C64x+ digital signal processors (DSPs) of the TMS320C6000 DSP family. The C64x/C64x+ DSP generation comprises fixed-point devices in the C6000 DSP platform. The C64x+ DSP is an enhancement of the C64x DSP with added functionality and an expanded instruction set.

SPRU871 — *TMS320C64x+ DSP Megamodule Reference Guide.* Describes the TMS320C64x+ digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

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TMS320DM643x DMP Peripherals Overview

1 Overview

The TMS320DM643x Digital Media Processor (DMP) is a highly-integrated hardware and software platform, designed to meet the application processing needs of next-generation embedded devices. The DM643x DMP enables OEMs and ODMs to quickly bring to market devices featuring rich user interfaces, high-processing performance, and long battery life through the maximum flexibility of a fully-integrated mixed-processor solution.

The user-accessible peripherals available on the DM643x DMP are configured using a set of memory-mapped control registers. The peripheral bus controller performs the arbitration for accesses of on-chip peripherals. Peripherals available on the DM643x DMP and their associated literature number are listed in Table 1.

Due to the pin multiplexing scheme on the DM643x DMP, not all of the peripherals listed in Table 1 are available simultaneously. Also, there may be features differences between devices for the same peripheral. You should check the device-specific data manual for further detail.

Table 1. TMS320DM643x DMP Peripherals Documentation

Peripheral/Module	Acronym	Lit #	DM6431	DM6433	DM6435	DM6437
Asynchronous External Memory Interface	EMIF	SPRU984	√	√	√	√
DDR2 Memory Controller	DDR2	SPRU986	√	√	√	√
DSP Megamodule—Internal Direct Memory Access Controller	IDMA	SPRU871	√	√	√	√
DSP Megamodule—Interrupt Controller	INTC	SPRU871	√	√	√	√
DSP Megamodule—Power-Down Controller	PDC	SPRU871	√	√	√	√
DSP Subsystem—Phase-Locked Loop Controller	PLLC	SPRU978	√	√	√	√
DSP Subsystem—Power and Sleep Controller	PSC	SPRU978	√	√	√	√
Enhanced Direct Memory Access Controller	EDMA	SPRU987	√	√	√	√
Ethernet Media Access Controller/ Management Data Input/Output Module	EMAC/MDIO	SPRU941	√	√	√	√
General-Purpose Input/Output	GPIO	SPRU988	√	√	√	√
High-End CAN Controller	HECC	SPRU981	√		√	√
Host Port Interface	HPI	SPRU998		√	√	√
Inter-Integrated Circuit Module	I2C	SPRU991	√	√	√	√
Multichannel Audio Serial Port	McASP	SPRU980	√	√	√	√
Multichannel Buffered Serial Port	McBSP	SPRU943	√	√	√	√
Peripheral Component Interconnect	PCI	SPRU985		√		√
Pulse-Width Modulator	PWM	SPRU995	√	√	√	√
Timer, 64-bit	Timer	SPRU989	√	√	√	√
Two-Level Internal Memory	Cache	SPRU862	√	√	√	√
Universal Asynchronous Receiver/Transmitter	UART	SPRU997	√	√	√	√
VLYNQ Port	VLYNQ	SPRU938		√	√	√
Video Processing Back End	VPBE	SPRU952		√		√
Video Processing Front End	VPFE	SPRU977	√		√	√

2 Asynchronous External Memory Interface (EMIF)

The asynchronous external memory interface (EMIF) provides a means to connect to a variety of external devices including:

- NAND Flash
- Asynchronous devices including Flash and SRAM
- Host processor interfaces such as the host port interface (HPI) on a Texas Instruments DSP

The most common use for the EMIF is to interface with both Flash devices and SRAM devices. The EMIF includes many features to enhance the ease and flexibility of connecting to external asynchronous devices. The EMIF features includes support for:

- 4 addressable chip select spaces of up to 32MB each
- 8-bit data bus width
- Programmable cycle timings such as setup, strobe, and hold times as well as turnaround time
- Select strobe mode
- Extended Wait mode
- NAND Flash ECC generation
- Connecting as a host to a TI DSP HPI interface
- Data Bus Parking
- Little-endian mode

3 DDR2 Memory Controller

The DDR2 memory controller is used to interface with JESD79D-2A standard compliant DDR2 SDRAM devices. Memory types such as DDR1 SDRAM, SDR SDRAM, SBSRAM, and asynchronous memories are not supported. The DDR2 memory controller is the major memory location for program and data storage.

The DDR2 memory controller supports the following features:

- JESD79D-2A standard compliant DDR2 SDRAM
- 256M-byte memory space
- Data bus width of 32 or 16 bits
- CAS latencies: 2, 3, 4, and 5
- Internal banks: 1, 2, 4, and 8
- Burst length: 8
- Burst type: sequential
- 1 CS signal
- Page sizes: 256, 512, 1024, and 2048
- SDRAM autoinitialization
- Self-refresh mode
- Prioritized refresh
- Programmable refresh rate and backlog counter
- Programmable timing parameters
- Little-endian mode

4 DSP Megamodule Internal Direct Memory Access (IDMA) Controller

The internal direct memory access (IDMA) controller in the TMS320C64x+ megamodule allows rapid data transfers between all local memories. It provides a fast way to page code and data sections into any memory-mapped RAM local to the C64x+ megamodule. The key advantage of the IDMA controller is that it allows for transfers between slower (level 2: L2) and faster (level 1: L1D, L1P) memory. The IDMA controller can provide lower latency than the cache controller since the transfers take place in the background of CPU operation, thereby removing stalls due to cache.

In addition, the IDMA controller facilitates rapid programming of peripheral configuration registers accessed through the external configuration space (CFG) port of the C64x+ megamodule. The IDMA controller view of the external configuration space that has a 32-word granularity and allows any register within a 32-word block to be individually accessed.

In summary, the IDMA controller is:

- Optimized for burst transfers of memory blocks (contiguous data).
- Allows access to and from any local memory (L1P, L1D, L2 (pages 0 and 1), and external CFG (but, source and destination cannot both be in CFG). CFG is accessible to channel 0 only. No CFG-to-CFG transfers.
- Supports the full data rate to and from the L2 memory controllers (256-bit data every extended memory controller (EMC) clock cycle):
  - Maximum throughput only achieved when source and destination are two different memories (L1P, L1D, and L2).
  - 50% throughput when source and destination are the same memory.
- Indicates transfer completion through programmable interrupts to the CPU.

The internal direct memory access (IDMA) controller is described in the *TMS320C64x+ DSP Megamodule Reference Guide* (SPRU871).

5 DSP Megamodule Interrupt Controller (INTC)

The TMS320C64x+ megamodule provides a large assortment of system events; the interrupt controller (INTC) supports up to 128 system events. The INTC provides a way to select the necessary events and route them to the appropriate DSP CPU interrupt and exception inputs. While many of these same system events are also used to drive other peripherals, such as the EDMA, the INTC is dedicated to managing the DSP CPU.

There are 128 system events that act as inputs to the INTC. They consist of both internally-generated events (within the C64x+ megamodule) and chip-level events. In addition to these 128 events, the INTC also receives (and routes straight through to the CPU) the nonmaskable and reset events. From these event inputs, the INTC outputs the following signals to the C64x+ CPU:

- 1 maskable, hardware exception (EXCEP)
- 12 maskable, hardware interrupts (INT4–INT15)
- 1 nonmaskable signal that can be used as either an interrupt or exception (NMI)
- 1 reset signal (RESET)

To facilitate the routing of events to interrupts and exceptions, the INTC includes the following modules:

- Interrupt selector: routes any of the system events to the 12 maskable interrupts
- Event combiner: reduces the large number of system events down to 4 events
- Exception combiner: lets any of the system events be grouped together for the single hardware exception input

The interrupt controller (INTC) is described in the *TMS320C64x+ DSP Megamodule Reference Guide* (SPRU871).

6 DSP Megamodule Power-Down Controller (PDC)

The TMS320C64x+ megamodule supports the ability to power-down various parts of the C64x+ megamodule. Using the power-down controller (PDC) in the C64x+ megamodule, the entire C64x+ megamodule can be powered-down. These power-down features can be used to design systems for lower overall system power requirements.

The power-down controller (PDC) is described in the *TMS320C64x+ DSP Megamodule Reference Guide* (SPRU871).

7 Enhanced Direct Memory Access (EDMA) Controller

The enhanced direct memory access (EDMA) controller handles all user-programmed data transfers between two slave endpoints on the device. The EDMA enables movement of data to/from any addressable memory spaces (internal/external), slave peripherals. The EDMA on the TMS320DM643x DMP has a different architecture from previous EDMA controllers on the TMS320C621x/C671x and TMS320C64x devices. It includes several enhancements over the previous EDMA controller and provides enhanced debug visibility and error reporting.

The EDMA controller has two principal blocks:

- EDMA channel controller
- EDMA transfer controller(s)

The EDMA channel controller primarily serves as the user interface for the EDMA controller. It also serves as event interface for the EDMA controller and is responsible for event latch-up, event prioritization, queue management, and transfer request (TR) submission to the EDMA transfer controllers. The EDMA transfer controllers are primarily responsible for data movement. The transfer controller is responsible for issuing read/write commands to the slaves.

8 Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO) Module

The ethernet media access controller (EMAC) and physical layer (PHY) device management data input/output (MDIO) module is used to move data between the TMS320DM643x DMP and another host connected to the same network, in compliance with the Ethernet protocol. The EMAC controls the flow of packet data from the system to the PHY and the MDIO module controls PHY configuration and status monitoring.

Both the EMAC and the MDIO modules interface to the system core through a custom interface that allows efficient data transmission and reception. This custom interface is referred to as the EMAC control module and is considered integral to the EMAC/MDIO peripheral.

Supports Media Independent Interface (MII) connection to physical layer devices.

9 General-Purpose Input/Output (GPIO)

The general-purpose input/output (GPIO) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, you can write to an internal register to control the state driven on the output pin. When configured as an input, you can detect the state of the input by reading the state of an internal register.

The GPIO peripheral has the following features:

- Output set/clear functionality through separate data set and clear registers allows multiple software processes to control GPIO signals without critical section protection.
- Set/clear functionality through writing to a single output data register is also supported.
- Separate input/output registers:
  - Output register can be read to reflect output drive status.
  - Input register can be read to reflect pin status.
- Some GPIO signals can be used as interrupt sources with configurable edge detection.

10 High-End CAN Controller (HECC)

The high-end CAN controller (HECC) in the TMS320DM643x DMP supports the following features:

- Full implementation of CAN protocol, version 2.0B
- 32 message objects
- Low-power modem
- Programmable wake-up on bus activity
- Automatic reply to a remote request message
- Automatic retransmission of a frame in case of loss of arbitration or error
- 32-bit local network time counter synchronized by a specific message (communication in conjunction with mailbox 16)
- Standard CAN controller (SCC)-compatible mode
- Dual clock support to avoid CAN bit-timing jitter

11 Host Port Interface (HPI)

The host port interface (HPI) provides a parallel port interface through which an external host processor can directly access the TMS320DM643x DMP resources (configuration and program/data memories). The external host device is asynchronous to the CPU clock and functions as a master to the HPI interface. The HPI enables a host device and the DM643x DMP to exchange information via internal or external memory. Dedicated address (HPIA) and data (HPID) registers within the HPI provide the data path between the external host interface and the processor resources. An HPI control register (HPIC) is available to the host and the CPU for various configuration and interrupt functions.

12 Inter-Integrated Circuit (I2C) Module

The inter-integrated circuit (I2C) module provides an interface between the TMS320DM643x DMP and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus. External components attached to this 2-wire serial bus can transmit and receive up to 8-bit wide data to and from the DM643x DMP through the I2C module.

The I2C module has the following features:

- Compliance with the Philips Semiconductors I2C-bus specification (version 2.1):
  - Support for byte format transfer
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers mode
  - Support for multiple slave-transmitters and master-receivers mode
  - Combined master transmit/receive and receive/transmit mode
  - I2C data transfer rate of from 10 kbps up to 400 kbps (Philips I2C rate)
- 2 to 7 bit format transfer
- Free data format mode
- One read DMA event and one write DMA event that can be used by the DMA
- Seven interrupts that can be used by the CPU
- Module enable/disable capability

13 Multichannel Audio Serial Port (McASP)

The multichannel audio serial port (McASP) functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP is useful for time-division multiplexed (TDM) stream, Inter-Integrated Sound (I2S) protocols, and intercomponent digital audio interface transmission (DIT). The McASP consists of transmit and receive sections that may operate synchronized, or completely independently with separate master clocks, bit clocks, and frame syncs, and using different transmit modes with different bit-stream formats. The McASP module also includes up to 4 serializers that can be individually enabled to either transmit or receive.

The McASP provides the following features:

- Two independent clock generator modules provide clocking flexibility that allows the McASP to receive and transmit at different rates. For example, the McASP can receive data at 48 kHz but output up-sampled data at 96 kHz or 192 kHz.
- Independent transmit and receive modules, each includes:
  - Programmable clock and frame sync generator
  - TDM streams from 2 to 32, and 384 time slots
  - Support for time slot sizes of 8, 12, 16, 20, 24, 28, and 32 bits
  - Data formatter for bit manipulation
- Individually assignable serial data pins (up to 5 pins)
- Glueless connection to audio analog-to-digital converters (ADC), digital-to-analog converters (DAC), codec, digital audio interface receiver (DIR), and S/PDIF transmit physical layer components
- Wide variety of I2S and similar bit-stream format
- Integrated digital audio interface transmitter (DIT) supports:
  - S/PDIF, IEC60958-1, AES-3 formats
  - Up to 4 transmit pins
  - Enhanced channel status/user data RAM
- 384-slot TDM with external digital audio interface receiver (DIR) device
  - For DIR reception, an external DIR receiver integrated circuit should be used with I2S output format and connected to the McASP receive section.
- Extensive error checking and recovery:
  - Transmit underruns and receiver overruns due to the system not meeting real-time requirements
  - Early or late frame sync in TDM mode
  - Out-of-range high-frequency master clock for both transmit and receive
  - External error signal coming into the AMUTEIN input
  - DMA error due to incorrect programming

14 Multichannel Buffered Serial Port (McBSP)

The primary use for the multichannel buffered serial port (McBSP) is for audio interface purposes. The McBSP is a specialized version of the McBSP peripheral used on other TI DSPs. The primary audio modes that are supported by the McBSP are the AC97 and IIS modes. In addition to the primary audio modes, the McBSP can be programmed to support other serial formats but is not intended to be used as a high-speed interface. The McBSP provides these functions:

- Full-duplex communication
- Double-buffered data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit
- Direct interface to industry-standard codecs, analog interface chips (AICs), and other serially connected analog-to-digital (A/D) and digital-to-analog (D/A) devices
- External shift clock or an internal, programmable frequency shift clock for data transfer

In addition, the McBSP has the following capabilities:

- Direct interface to:
  - T1/E1 framers
  - MVIP switching compatible and ST-BUS compliant devices including:
    - MVIP framers
    - H.100 framers
    - SCSA framers
  - IOM-2 compliant devices
  - AC97 compliant devices (the necessary multiphase frame synchronization capability is provided.)
  - IIS compliant devices
  - SPI™ devices
- Multichannel transmit and receive of up to 128 channels
- A wide selection of data sizes, including 8, 12, 16, 20, 24, and 32 bits
- µ-Law and A-Law companding
- 8-bit data transfers with the option of LSB or MSB first
- Programmable polarity for both frame synchronization and data clocks
- Highly programmable internal clock and frame generation

15 Peripheral Component Interconnect (PCI)

The peripheral component interconnect (PCI) port supports connection of the TMS320DM643x DMP to a PCI host via the integrated PCI master/slave bus interface. The PCI port interfaces to the DMP independently from the enhanced DMA (EDMA) controller. This architecture allows for both PCI master and slave transactions, while keeping the EDMA channel resources available for other applications.

The PCI port is compliant to the PCI Local Bus Specification (revision 2.3). It uses a 32-bit wide data and address bus operating at 33 MHZ. The PCI operates as a PCI slave device for configuration cycles and memory cycles. It also acts as a PCI master device for configuration cycles, IO cycles, and memory accesses to other devices.

16 Power and Sleep Controller (PSC)

The Power and Sleep Controller (PSC) provides a standard method for controlling device power by gating clocks to individual modules. The PSC is described in the *TMS320DM643x DMP DSP Subsystem Reference Guide* (SPRU978).

17 Pulse-Width Modulator (PWM)

The pulse-width modulator (PWM) peripheral is very common in embedded systems. It provides a way to generate a pulse periodic waveform for motor control or can act as a digital-to-analog converter with some external components. This PWM peripheral is basically a timer with a period counter and a first-phase duration comparator, where bit width of the period and first-phase duration are both programmable.

The PWM peripheral has the following features:

- 32-bit period counter
- 32-bit first-phase duration counter
- 8-bit repeat counter for one-shot operation. One-shot operation will produce N + 1 periods of the waveform, where N is the repeat counter value.
- Configurable to operate in either one-shot or continuous mode.
- One-shot operation can be triggered by the CCD VSYNC output of the video processing subsystem to allow any of the PWM instantiations to be used as a CCD timer.
- Configurable PWM output pin inactive state.
- Interrupt and enhanced direct memory access (EDMA) synchronization events.

18 64-Bit Timer

The TMS320DM643x DMP contains three software-programmable 64-bit timers (Timer 0, Timer 1, and Timer 2). Timer 0 and Timer 1 are used as general-purpose timers and can be programmed in 64-bit mode, dual 32-bit unchained mode, or dual 32-bit chained mode; Timer 2 is used only as a watchdog timer. The watchdog timer mode is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

The 64-bit timer consists of the following features:

- 64-bit count-up counter
- Timer modes:
  - 64-bit general-purpose timer mode
  - Dual 32-bit general-purpose timer mode
  - Watchdog Timer mode
- 2 possible clock sources:
  - Internal clock
  - External clock input via timer input pins TIN0 and TIN1 (Timer 0 and Timer 1 only)
- 2 possible output modes:
  - Pulse mode (configurable pulse width)
  - Clock mode
- 2 possible operation modes:
  - One-time operation (timer runs for one period then stops)
  - Continuous operation (timer automatically resets after each period)
- Generates interrupts to DSP
- Generates sync event to EDMA

19 Universal Asynchronous Receiver/Transmitter (UART)

This universal asynchronous receiver/transmitter (UART) peripheral performs serial-to-parallel conversion on data received from a peripheral device or modem, and parallel-to-serial conversion on data received from the TMS320DM643x CPU. The CPU can read the UART status at any time. The UART includes control capability and a processor interrupt system that can be tailored to minimize software management of the communications link.

The UART peripheral has the following features:

- Programmable baud rates up to 128 kbps (frequency pre-scale values from 1 to 65 535)
- Fully programmable serial interface characteristics:
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no PARITY bit generation and detection
  - 1, 1.5, or 2 STOP bit generation
- 16-byte depth transmitter and receiver FIFOs:
  - The UART can be operated with or without the FIFOs
  - 1, 4, 8, or 14 byte selectable receiver FIFO trigger level for autoflow control and DMA
- DMA signaling capability for both received and transmitted data
- CPU interrupt capability for both received and transmitted data
- False START bit detection
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, and framing error simulation
- Programmable autoflow control using CTS and RTS signals (not supported on all UARTs. See the device-specific data manual for supported features.)
- Modem control functions using CTS and RTS signals (not supported on all UARTs. See the device-specific data manual for supported features.)

20 VLYNQ Port

The VLYNQ communications interface port is a low pin count, high-speed, point-to-point serial interface in the TMS320DM643x Digital Media Processor (DMP) used for connecting to host processors and other VLYNQ compatible devices. The VLYNQ port is a full-duplex serial bus where transmit and receive operations occur separately and simultaneously without interference. The general features of the VLYNQ port are:

- Low pin count (10 pin interface, scalable to as low as 3 pins)
- No tri-state signals
  - All signals are dedicated and driven by only one device
  - Necessary to allow support for high-speed PHYs
- Simple packet-based transfer protocol for memory-mapped access
  - Write request/data packet
  - Read request packet
  - Read response data packet
  - Interrupt request packet
- Auto width negotiation
- Symmetric Operations
  - Transmit (TX) pins on the first device connect to the receive (RX) pins on the second device and vice-versa.
  - Data pin widths are automatically detected after reset
  - Re-request packets, response packets, and flow control information are all multiplexed and sent across the same physical pins.
  - Supports both host/peripheral and peer-to-peer communication models
- Simple block code packet formatting (8b/10b)
- Supports in-band and flow control
  - No extra pins are needed
  - Allows the receiver to momentarily throttle the transmitter back when overflow is about to occur
  - Uses the special built-in block code capability to interleave flow control information seamlessly with user data
  - Automatic packet formatting optimizations
- Internal loopback modes are provided
- Connects to legacy VLYNQ devices

21 Video Processing Back End (VPBE)

The video processing back end (VPBE) in the video processing subsystem consists of the on-screen display (OSD) module, video encoder (VENC), and digital LCD controller (DLCD).

21.1 On-Screen Display (OSD) Module

The major function of the on-screen display (OSD) module is to gather and blend video data and display/bitmap data before feeding it to the video encoder (VENC) in YCbCr format. The video and display data is read from an external memory, typically DDR2. The OSD is programmed via control and parameter registers. The OSD has the following features:

- Simultaneous display of two video windows and two OSD windows.
- Support for a rectangular cursor window and a programmable background color selection.
- Support for attenuation of the YCbCr values for the REC601 standard.

21.2 Video Encoder (VENC)

The video encoder (VENC) generates analog video output. The VENC supports the following features:

- Master Clock Input - 27 MHZ (×2 Up-sampling)
- SDTV support
- HDTV support
- 10-bit over-sampling D/A converters
- Optional 7.5% pedestal
- 16-235/0-255 input amplitude selectable
- Programmable luma delay
- Master/slave operation
- Internal color bar generation (100%/75%)

21.3 Digital LCD Controller (DLCDC)

The digital LCD controller (DLCDC) generates digital RGB/YCbCr data output and timing signals. The DLCD supports the following features:

- Programmable DCLK
- Various output formats:
  - YCbCr 16 bit
  - YCbCr 8 bit
  - ITU-R BT.656
  - Parallel RGB 24 bit
- Low-pass filter for digital RGB output
- Programmable timing generator
- Master/slave operation
- Internal color bar generation (100%/75%)

22 Video Processing Front End (VPFE)

The video processing front end (VPFE) in the video processing subsystem consists of the CCD controller (CCDC), preview engine, resizer, hardware 3A (H3A) statistic generator and histogram modules. Together these modules provide a powerful and flexible front-end interface. These modules are briefly described below:

22.1 CCD Controller (CCDC)

The CCD controller (CCDC) provides an interface to image sensors and digital video sources. The CCDC receives raw image/video data from sensors (CMOS or CCD) or YUV video data in numerous formats from video decoder devices. The CCDC output requires additional image processing to transform raw input images to final processed images. This processing can be done either on-the-fly in the preview engine or in software on the DSP and image coprocessor subsystem. Simultaneously, while processing, raw data input to the CCDC can be used for computing various statistics (H3A and histogram) for use in control of image/video tuning parameters.

22.2 Preview Engine

The preview engine is an image processing module that is configurable for various sensor types, image quality, and video frame rates for digital still camera preview and video recording. The preview engine transforms raw unprocessed image/video data from a sensor (CMOS or CCD) into YCbCr 422 data. The output of the preview engine is used for both video compression and external display devices such as an NTSC/PAL analog encoder or a digital LCD.

22.3 Resizer

The resizer module resizes the input image data to the desired display or video encoding resolution, including the ability to zoom up to 10×. The resizer module can accept input image/video data from either the preview engine or DDR2. The output of the resizer module is sent to DDR2.

22.4 Hardware 3A (H3A)

The hardware 3A (H3A) module provides control loops for auto focus (AF), auto white balance (AWB) and auto exposure (AE). There are 2 main components of the H3A module:

- Auto focus (AF) engine
- Auto exposure (AE) and auto white balance (AWB) engine

The AF engine extracts and filters the red, green, and blue data from the input image/video data and provides either the accumulation or peaks of the data in a specified region. The specified region is a two-dimensional block of data and is referred to as a “paxel” for the case of AF.

The AE/AWB engine accumulates the values and checks for saturated values in a sub-sampling of the video data. In the case of the AE/AWB, the two-dimensional block of data is referred to as a “window”. Thus, other than referring to them by different names, a paxel and a window are essentially the same thing. However, the number, dimensions, and starting position of the AF paxels and the AE/AWB windows are separately programmable.

22.5 Histogram

The histogram module accepts raw image/video data (either 3 or 4 colors) and bins input color pixels, depending on the amplitude value and color, and provides statistics required to implement various hardware 3A (AF and AE/AWB) algorithms and tune the final image/video output. The value of the pixel is not stored, but each bin contains the number of pixels that are within the appropriate set range. The source of the raw data for the histogram is typically a CCD/CMOS sensor (via the CCD controller) or optionally from DDR2.

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