TMS320DM643x DMP
Video Processing Back End (VPBE)

User's Guide

Literature Number: SPRU952A
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TEXAS INSTRUMENTS

Contents

List of Figures

List of Tables

Read This First

About This Manual

This document describes the video processing back end (VPBE) in the TMS320DM643x Digital Media Processor (DMP).

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320DM643x Digital Media Processor (DMP). Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the DM643x DMP, related peripherals, and other technical collateral, is available in the C6000 DSP product folder at: www.ti.com/c6000.

SPRU978 — *TMS320DM643x DMP DSP Subsystem Reference Guide.* Describes the digital signal processor (DSP) subsystem in the TMS320DM643x Digital Media Processor (DMP).

SPRU983 — *TMS320DM643x DMP Peripherals Overview Reference Guide.* Provides an overview and briefly describes the peripherals available on the TMS320DM643x Digital Media Processor (DMP).

SPRAA84 — *TMS320C64x to TMS320C64x+ CPU Migration Guide.* Describes migrating from the Texas Instruments TMS320C64x digital signal processor (DSP) to the TMS320C64x+ DSP. The objective of this document is to indicate differences between the two cores. Functionality in the devices that is identical is not included.

SPRU732 — *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide.* Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C64x and TMS320C64x+ digital signal processors (DSPs) of the TMS320C6000 DSP family. The C64x/C64x+ DSP generation comprises fixed-point devices in the C6000 DSP platform. The C64x+ DSP is an enhancement of the C64x DSP with added functionality and an expanded instruction set.

SPRU871 — *TMS320C64x+ DSP Megamodule Reference Guide.* Describes the TMS320C64x+ digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

Video Processing Back End (VPBE)

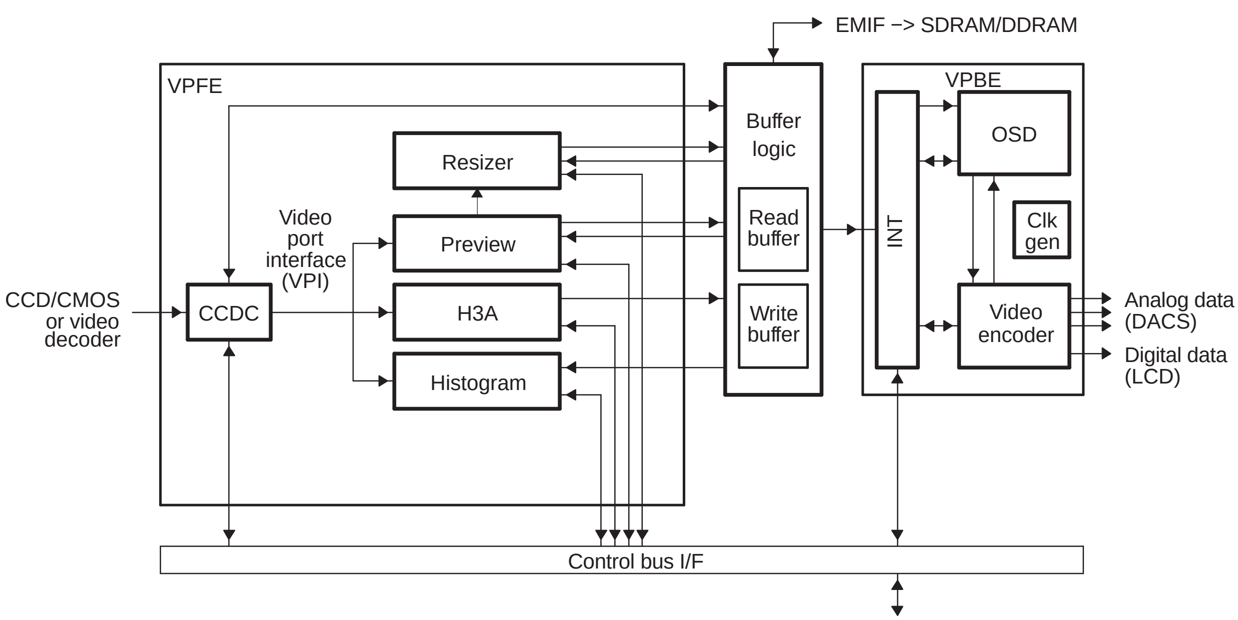
1 Introduction

1.1 Purpose of the Video Processing Back End

The video processing subsystem (VPSS), shown in Figure 1, provides an input interface (video processing front end, VPFE) for external imaging peripherals such as image sensors, video decoders, etc.; an output interface (video processing back end, VPBE) for display devices, such as analog SDTV displays, digital LCD panels, and HDTV video encoders, etc.

In addition to these peripherals, there is a set of common buffer memory and DMA controls to ensure efficient use of the DDR2 burst bandwidth. The shared buffer logic/memory is a unique block that is tailored to seamlessly integrate the VPSS into an image/video processing system. It acts as the primary source or sink to all of the VPFE and VPBE modules that are either requesting or transferring data from the or to the DDR2. In order to use the external DDR2 bandwidth efficiently, the shared buffer logic/memory interfaces with the DMA system via a high-bandwidth bus (64 bits wide). The shared buffer logic/memory also interfaces with all of the VPFE and VPBE modules via a 128-bit-wide bus. It is imperative that the VPSS uses DDR2 bandwidth efficiently due to both its large bandwidth requirements and the real-time requirements of the VPSS modules. A set of user-accessible registers is provided to monitor overflows or failures in data transfers because you can configure the VPSS modules so that you will exceed the DDR2 bandwidth.

Figure 1. Video Processing Subsystem (VPSS) Block Diagram



1.2 Features

The VPBE block is comprised of the on-screen display (OSD) and the video encoder (VENC) modules. Together, these modules provide a powerful and flexible back-end display interface.

- On-screen display (OSD) graphic accelerator: The OSD manages display data in various formats for several types of hardware display windows and it also handles blending of the display windows into a single display frame, which the video encoder (VENC) module then outputs.
- Video encoder (VENC): The VENC takes the display frame from the on-screen display (OSD) and formats it into the desired output format and output signals (including data, clocks, sync, etc.) that are required to interface to display devices.
  The VENC consists of three primary sub-blocks:
  – The analog video encoder generates the signaling to interface to NTSC/PAL television displays, including video A/D conversion.
  – The digital LCD controller supports interfaces to various digital LCD display formats as well as standard digital YUV outputs to interface to high-definition video encoders and/or DVI/HDMI interface devices.
  – Timing generator to generate the specific timing required for analog video output as well as various digital video output modes.

The following restriction exists in the enabling sequence for the OSD and VENC modules:

- The OSD windows should be enabled (VIDWINMD.ACT*n* and OSDWIN*n*MD.OACT*n*) prior to enabling the VENC (VMOD.VENC = 1).

1.2.1 On-Screen Display (OSD) Features

The primary function of the OSD module is to gather and blend video data and display/bitmap data and then pass it to the video encoder (VENC) in YCbCr format. The video and display data is read from external DDR2 memory. The OSD is programmed via control and parameter registers. The following are the primary features that are supported by the OSD:

- Support for two video windows and two OSD windows that can be displayed simultaneously (VIDWIN0/VIDWIN1 and OSDWIN0/OSDWIN1).
- Separate enable/disable control for each window.
- Programmable width, height, and base starting coordinates for each window.
- External memory address and offset registers for each window.
- Support for $\times 2$ and $\times 4$ zoom in both the horizontal and vertical direction.
- Can configure OSDWIN1 to be an attribute window for OSDWIN0.
- Ability to select either field/frame mode for the windows (interlaced/progressive).
- An eight-step blending process between the OSD and video windows.
- Transparency support for the OSD and video data (blending between bitmap and video only for pixels matching the background color).
- Ability to resize from VGA to NTSC/PAL (640×480 to 720×576) for both the OSD and video windows.
- Reads in YCbCr data in 422 format from the external memory with the ability to interchange the order of the CbCr component in the 32-bit word (this is relevant to the two video windows).
- Support for a ping-pong buffer scheme that you can use for VIDWIN0 (this allows you to access video data from two different locations in the SDRAM/DDRAM).
- The OSD window (either one, but not both at the same time) is capable of reading in RGB data (16-bit data with six bits for the green and five bits each for the red and blue colors) instead of bitmap data in YCbCr format restricted to a maximum of 8-bits.
- The OSD bitmap data width is selectable between 1 bit, 2 bits, 4 bits, or 8 bits.
- Each OSD window supports 16 entries for the bitmap (to index into a 256 entry RAM/ROM CLUT table).
- Indirect support for 24-bit RGB input data (which will be transformed into 16-bit YCbCr video window data) via the wrapper interface in the VPBE.
- A programmable background color selection.

- Programmable color palette with the ability to select between a RAM/ROM table with support for 256 colors. There are 2 ROM tables from which one can be selected for all the windows together.
- The width, height, and color of the cursor is selectable.
- The display priority is: Rectangular-Cursor > OSDWIN1 > OSDWIN0 > VIDWIN1 > VIDWIN0 > background color.
- Support for attenuation of the YCbCr values for the REC601 standard.

The following restrictions exist in the OSD module:

- Both the OSD windows and VIDWIN1 should be fully contained inside VIDWIN0. This means that both the Y and X position of either the OSD windows or VIDWIN1 should be greater (not equal) to the Y and X position of VIDWIN0. This also requires VIDWIN0 to be enabled when using either the OSD windows or VIDWIN1.
- The OSD cannot support more than 256 color entries in the CLUT RAM/ROM. Some applications require higher number of entries, and one workaround is to use VIDWIN1 as an overlay mimicking the OSD window. Another option is to use the RGB mode for one of the OSD windows, which allows for a total of 16-bits for the R, G, and B colors (64K colors).
- The OSD can only read YCbCr in 422 interleaved format for the video windows. Other formats, either color separate storage or 444/420 interleaved data is not supported.
- If the vertical resize filter is enabled for either of the video windows, the maximum horizontal window dimension cannot be greater than 720 currently. This is due to the limitation in the size of the line memory.
- It is not possible to use both of the CLUT ROMs at the same time. However, a window can use RAM while another chooses ROM.
- The 24-bit RGB input mode is only valid for one of the two video windows (programmable) and does not apply to the OSD windows.

1.2.2 Video Encoder (VENC) Features

The VENC/DLCD consists of three major blocks: the video encoder that generates analog video output, the digital LCD controller that generates digital RGB/YCbCr data output and timing signals, and the timing generator.

Note: The DACs should not be used in non-standard mode.

The analog video encoder features are:

- Master Clock Input - 27 MHz (×2 Upsampling)
- SDTV Support
  - Composite NTSC-M, PAL-B/D/G/H/I
  - S-Video (Y/C)
  - Component YPbPr (SMPTE/EBU N10, Betacam, MII)
  - RGB
  - Non-Interlace
  - CGMS/WSS
  - Line 21 Closed Caption Data Encoding
  - Chroma Low-Pass Filter 1.5 MHz/3 MHz
  - Programmable SC-H phase
- HDTV Support
  - Progressive Output (525p/625p)
  - Component YPbPr
  - RGB
  - CGMS/WSS

- 10-bit Over-Sampling D/A Converters (54 MHz)
- Optional 7.5% Pedestal
- 16-235/0-255 Input Amplitude Selectable
- Programmable Luma Delay
- Master/Slave Operation
- Internal Color Bar Generation (100%/75%)

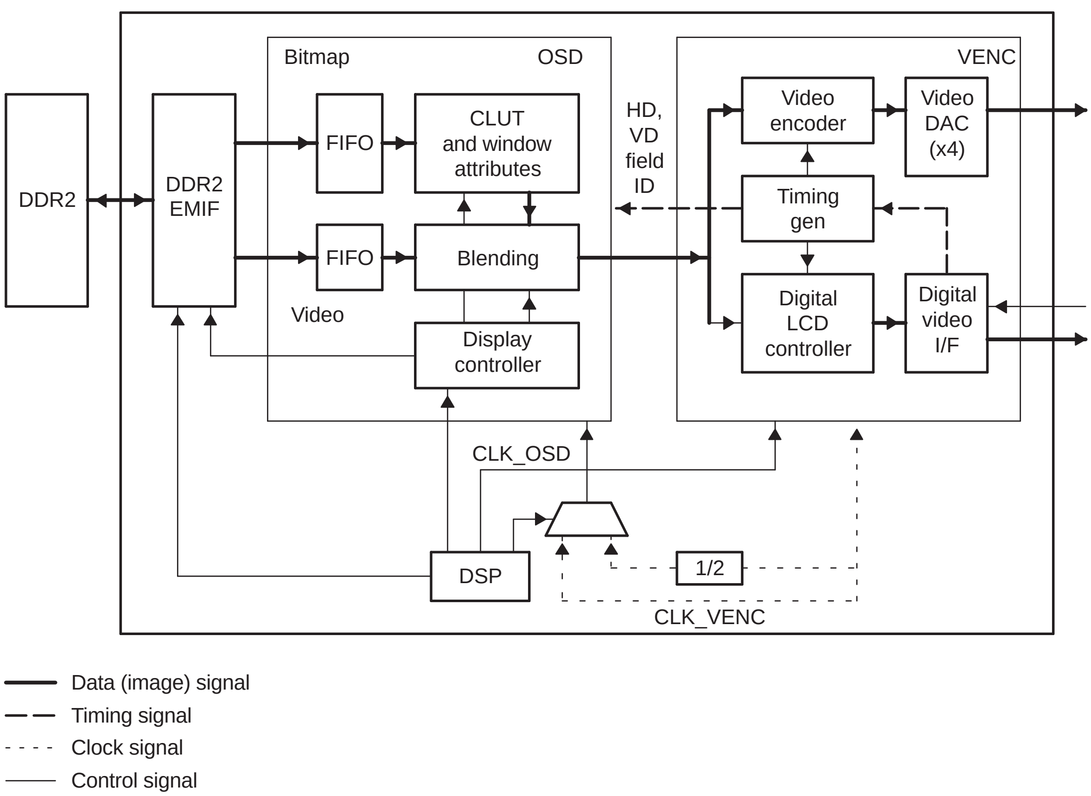
The digital LCD interface features are:

- Programmable DCLK
- Various Output Formats
  - YCbCr 16 bit
  - YCbCr 8 bit
  - ITU-R BT. 656
  - Parallel RGB 24 bit
- Low-Pass Filter for Digital RGB Output
- Programmable Timing Generator
- Master/Slave Operation
- Internal Color Bar Generation (100%/75%)

1.3 Functional Block Diagram

Figure 2 shows a high-level functional block diagram of the VPBE, along with the different data flow paths.

Figure 2. Video Processing Back End (VPBE) Block Diagram



1.4 Supported Use Case Statement

The VPBE supports image (2-D window) compositing and blending from data stored in DDR2 memory in various display formats by the OSD module and then data formatting and conversion for display to analog SDTV/EDTV displays and to digital display devices various modes/formats by the VENC module. YUV output modes have minimal data processing applied and can be passed through directly from YUV input sources to the VPBE. Digital RGB and LCD display formats are generated from the OSD's YUV422 output format as are the analog outputs. The analog DAC outputs supports up to 525p/625p EDTV with composite, S-Video (Y/C), component (YPbPr), and RGB output formats.

1.5 Industry Standard(s) Compliance Statement

Analog television standards supported:

- SDTV
  - 525-line/60 Hz (NTSC-M) or
  - 625-line/50 Hz (PAL-B/D/G/H/I)
- HDTV
  - 525p or 625p

2 Display Subsystem Environment

The VPBE signals are shown in Table 1.

Table 1. Interface Signals for Video Processing Back End

Pin Name	I/O	Description	Default	Tristate	ID Pullup/ Pulldown
		VPBE Analog Signals			
DAC_IOUT_A	Out	Video DAC A		-	-
DAC_IOUT_B	Out	Video DAC B		-	-
DAC_IOUT_C	Out	Video DAC C		-	-
DAC_IOUT_D	Out	Video DAC D		-	-
DAC_VREF	Bi	Video DAC VREF	0.5 V	-	-
DAC_RBIAS	Bi	Video DAC R Bias	0.5 V	-	-
VDDA_1P8V	Pwr	Video DAC Analog 1.8 V power	1.8 V	-	-
VSSA_1P8V	Gnd	Video DAC Analog 1.8 V ground		-	-
VDDA_1P1V	Pwr	Video DAC Analog 1.1 V power	Core	-	-
VSSA_1P1V	Gnd	Video DAC Analog 1.1 V ground		-	-
		VPBE Digital Signals			
HSYNC	Bi	H sync	Out	tri	PD
VSYNC	Bi	V sync	Out	tri	PD
VCLK	Out	Video Clock	Out	tri	
VPBECLK	In	VPBE External Clock Input (optional)	In	tri	PD
YOUT7	Out	Y OUT signal	Out	tri	
YOUT6	Out	Y OUT signal	Out	tri	
YOUT5	Out	Y OUT signal	Out	tri	
YOUT4	Bi	Y OUT signal	Out	tri	PD
YOUT3	Bi	Y OUT signal	Out	tri	PD
YOUT2	Bi	Y OUT signal	Out	tri	PD
YOUT1	Bi	Y OUT signal	Out	tri	PD
YOUT0	Bi	Y OUT signal	Out	tri	PD
COUT7	Out	C OUT signal	Out	tri	
COUT6	Out	C OUT signal	Out	tri	
COUT5	Out	C OUT signal	Out	tri	
COUT4	Bi	C OUT signal	Out	tri	
COUT3	Bi	C OUT signal	Out	tri	PD
COUT2	Bi	C OUT signal	Out	tri	PD
COUT1	Bi	C OUT signal	Out	tri	PD
COUT0	Bi	C OUT signal	Out	tri	PD
R2	Bi	RGB666 mode R2	In	tri	
B2	Bi	RGB666 mode B2	In	tri	
LCD_OE	Out	LCD Output Enable	Out	tri	
G0	Bi	RGB666 mode G0	In	tri	
B0/LCD_FIELD	Bi	RGB666 mode B0/LCD_FIELD	In	tri	
R0	Bi	RGB666 mode R0	In	tri	
G1	Bi	RGB666 mode G1	In	tri	
B1	Bi	RGB666 mode B1	In	tri	
R1	Bi	RGB666 mode R1	In	tri	

2.1 Analog Display Interface

The analog display interface is used for driving NTSC/PAL compatible television displays, video decoders, and other devices with NTSC/PAL compatible display interfaces.

2.1.1 Analog Display Signal Interface

Table 2 shows the interface connections for the analog display interface.

Table 2. Interface Signals for Analog Displays

Pin Name	Description
DAC_IOUT_A	Video DAC A
DAC_IOUT_B	Video DAC B
DAC_IOUT_C	Video DAC C
DAC_IOUT_D	Video DAC D
DAC_VREF	Video DAC VREF
DAC_RBIAS	Video DAC R Bias
VDDA_1P8V	Video DAC Analog 1.8 V power
VSSA_1P8V	Video DAC Analog 1.8 V ground
VDDA_1P1V	Video DAC Analog 1.1 V power
VSSA_1P1V	Video DAC Analog 1.1 V ground

2.1.2 Analog Display Signal Interface Description

The VPBE analog interface includes up to four video DAC signals, a DAC voltage reference, and R bias signals, and separate 1.8V and core power/ground signals. Up to four DACs are available, supporting composite (1 DAC), S-Video or Y/C (2 DACs), component YPbPr (3 DACs), analog RGB (3 DACs) and PAL component YPbPr + syncs (4 DACs). The DACs can operate at either 27 MHz or 54 MHz sampling rate to support either SDTV (interlaced, 6.5 MHz bandwidth) or EDTV (progressive, 13 MHz bandwidth) signals.

2.1.3 Analog Display Signal Interface Timing

This section describes master mode timings. For slave mode timings, see Section 4.4.4.3.

2.1.3.1 Horizontal Timing

The timings, such as location of horizontal sync pulses, color burst position, and active video position are automatically calculated by hardware. Figure 3 shows horizontal timing characteristics. Table 3 and Table 4 show the parameters of the timing chart. Each parameter is set to conformed standards but can be adjusted by user registers. Independent timing configurations can be available for CVBS and component/RGB output.

Figure 3. Horizontal Timing

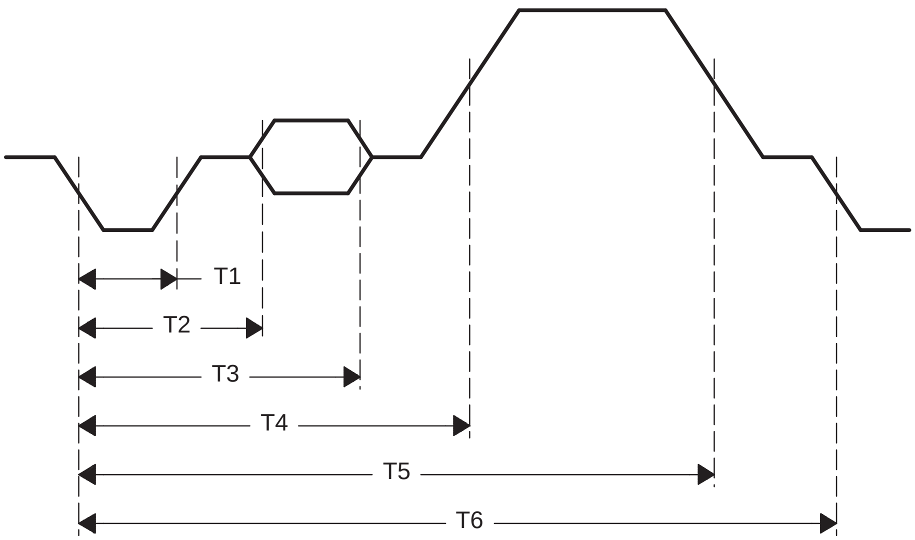


Table 3. Horizontal Timing Parameters (SDTV)

Parameter	Item	NTSC [(1)]	PAL [(1)]	CVBS Adjust	Component Adjust
T1	Horizontal Sync Pulse Width	127	127	ETMG0.CLSW	ETMG2.MLSW
T2	H Ref to Burst Start	141	151	ETMG1.CBST	N/A
T3	H Ref to Burst End	210	212	ETMG1.CBSE	N/A
T4	H Ref to H Blanking End	243	263	ETMG1.CLBI	ETMG3.CLBI
T5	H Ref to H Blanking Start	1683	1703	ETMG1.CFPW	ETMG3.CFPW
T6	1H	1716	1728	-	-

(1) Units are in ENC clocks

Table 4. Horizontal Timing Parameters (Progressive/EDTV)

Parameter	Item	525P [(1)]	625 [(1)]	CVBS Adjust	Component Adjust
T1	Horizontal Sync Pulse Width	64	64	N/A	ETMG2.MLSW
T4	H ref to H Blanking End	122	132	N/A	ETMG3.CLBI
T5	H ref to H Blanking Start	842	852	N/A	ETMG3.CFPW
T6	1H	858	864	-	-

(1) Units are in ENC clocks

2.1.3.2 Horizontal Blanking Timing

Some pixels around horizontal video blanking edge are clipped so that the output video has the proper blanking transition.

This feature is enabled by default but can be disabled by setting to 1 the parameter CBLS (for CVBS) or MBLS (for YPbPr/RGB). Figure 4 shows the waveforms when blanking edge shaping is enabled and disabled. Table 5 shows the difference of T4 and T5 (see Figure 3 for T4 and T5).

Figure 4. Horizontal Blanking Shaping

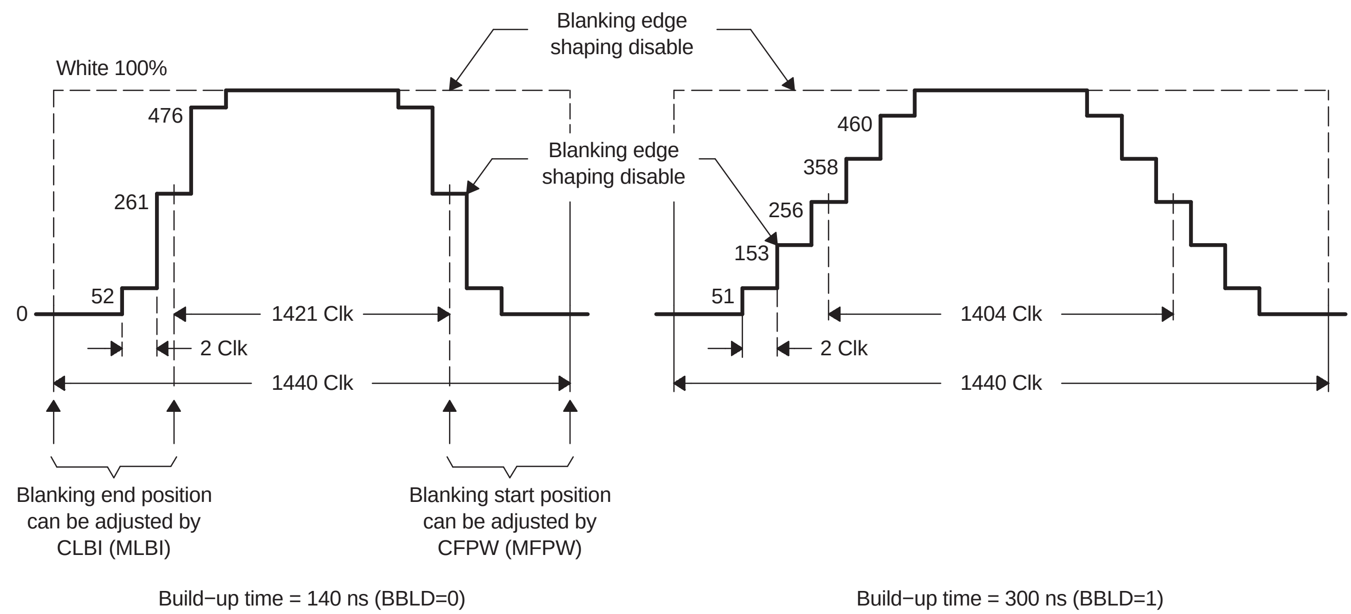


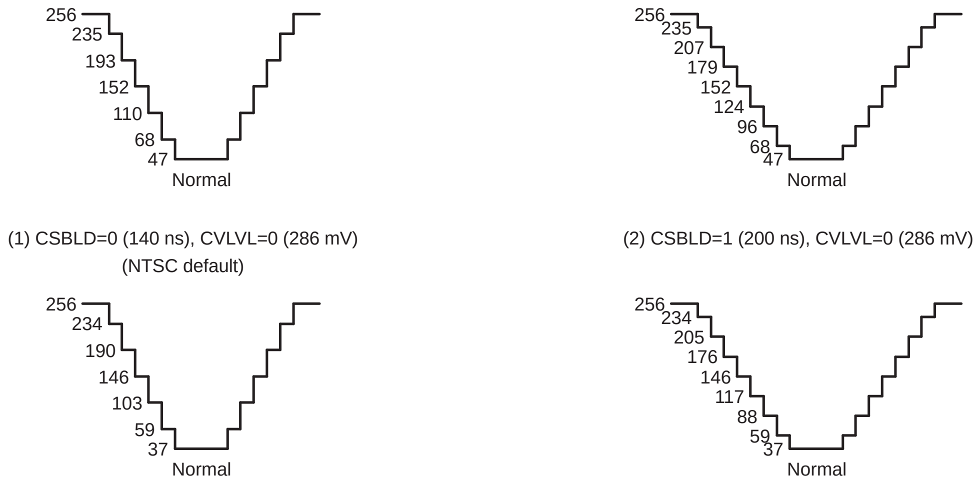
Table 5. Blanking Shaping On/Off

	NTSC		PAL	
Parameter	CVBS.CBLS = 0	CVBS.CBLS = 1	CVBS.CBLS = 0	CVBS.CBLS = 1
T4	252	243	282	263
T5	1673	1683	1686	1703

2.1.3.3 Horizontal Sync Timing

The detail waveform of horizontal sync pulse to be inserted on the luma signal is shown in Figure 5. The levels in Figure 5 are the internal digital values. The duration of each step is one ENC clock period. The register name in this figure is for CVBS output. For component/RGB output, CMPNT.MSBLD and CMPNT.MYLVL control sync build-up time and sync level, respectively.

Figure 5. Sync Signal Detail Waveform (SDTV)



(1) CSBLD=0 (140 ns), CVLVL=0 (286 mV) (NTSC default)

(2) CSBLD=1 (200 ns), CVLVL=0 (286 mV)

(3) CSBLD=0 (140 ns), CVLVL=1 (300 mV)

(4) CSBLD=1 (200 ns), CVLVL=1 (300 mV) (PAL default)

2.1.3.4 Vertical Timing

The vertical timing is also controlled by hardware automatically for each mode (NTSC or PAL). Serration and equalization pulses are generated for appropriate lines. The color burst is automatically disabled on appropriate lines. The line number in a field can be selected by VMOD.ITCLCL, as shown in Table 6.

Table 6. Number of Lines for Each Scan Mode

		Line	
VMOD.ITLC	VMOD.ITCLCL	NTSC	PAL
0	x	262.5	312.5
1	0	262	312
1	1	263	313

Figure 6 and Figure 7 show the vertical timing characteristics of NTSC and PAL, respectively.

Figure 8 and Figure 9 show the non-interlaced mode for NTSC and PAL, respectively. The non-interlaced mode is activated when VMOD.ITLC = 1.

Figure 10 and Figure 11 show the vertical timing of progressive mode. FIELD output for progressive and non-interlace mode is fixed to low.

In these figures, the color burst is denoted as |, ↑ or ↓ marks. For NTSC, | denotes the color burst position. For PAL, ↑ means +135°, while ↓ means -135° relative to U. For interlaced NTSC, the video encoder operation starts with the field I in master mode. For interlaced PAL, starts with the field II.

Figure 6. NTSC Vertical Timing

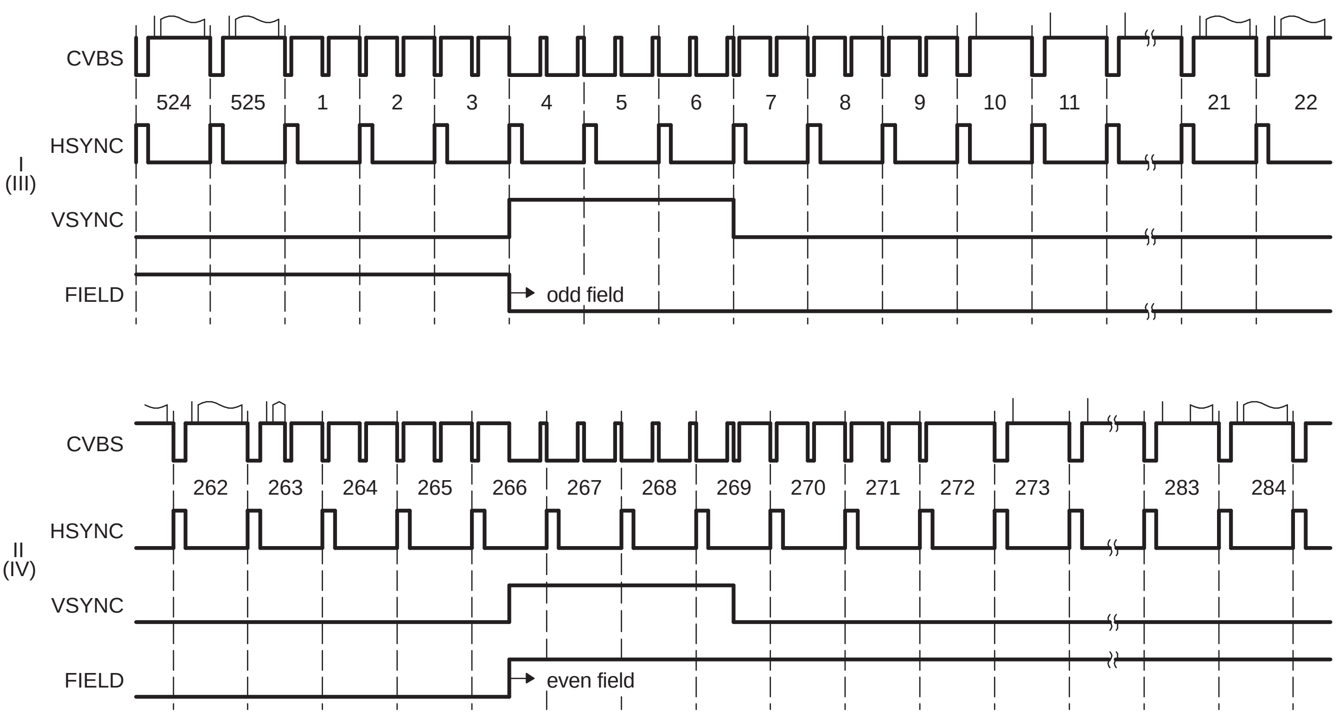


Figure 7. PAL Vertical Timing

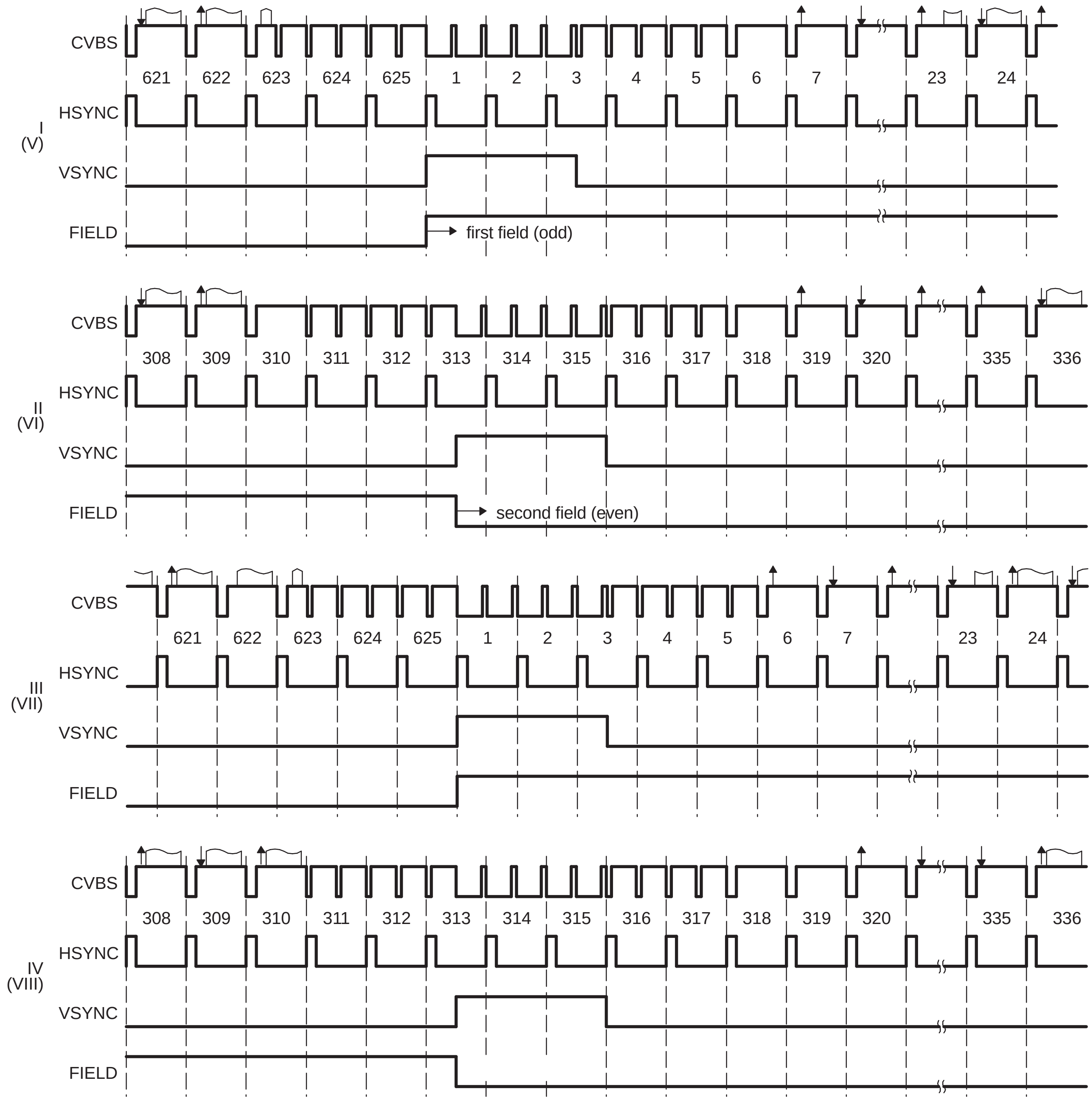


Figure 8. Non-Interlaced NTSC (ITLC = 1, ITLCL = 0) Vertical Timing

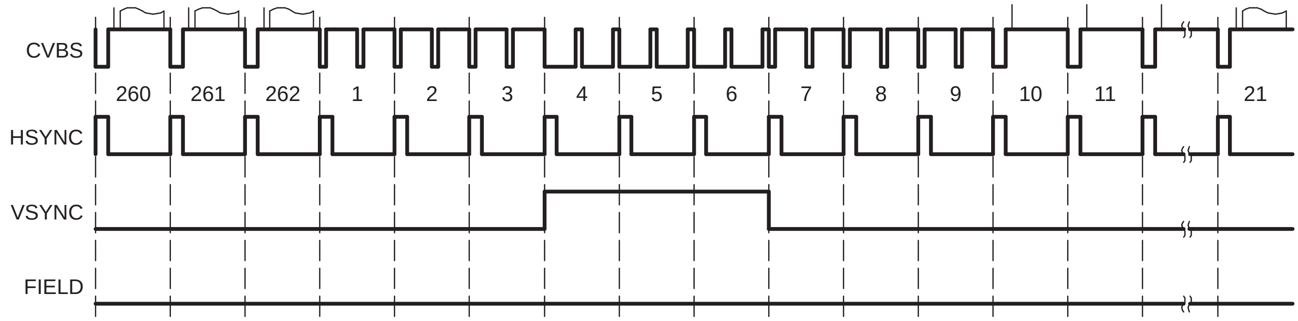


Figure 9. Non-Interlaced PAL (ITLC = 1, ITLCL = 0) Vertical Timing

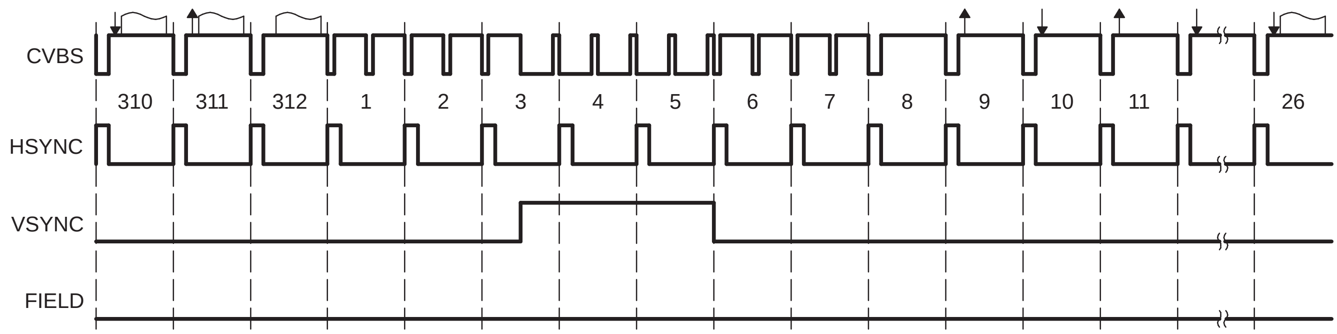


Figure 10. 525P Vertical Timing

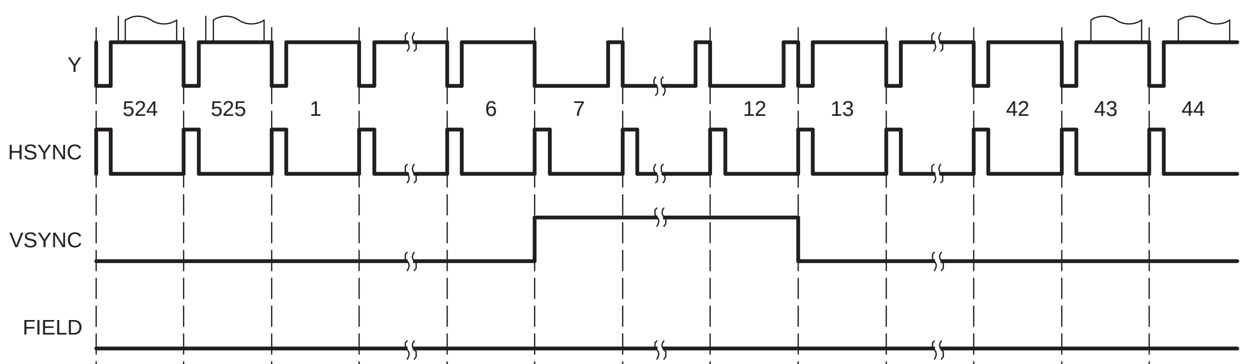
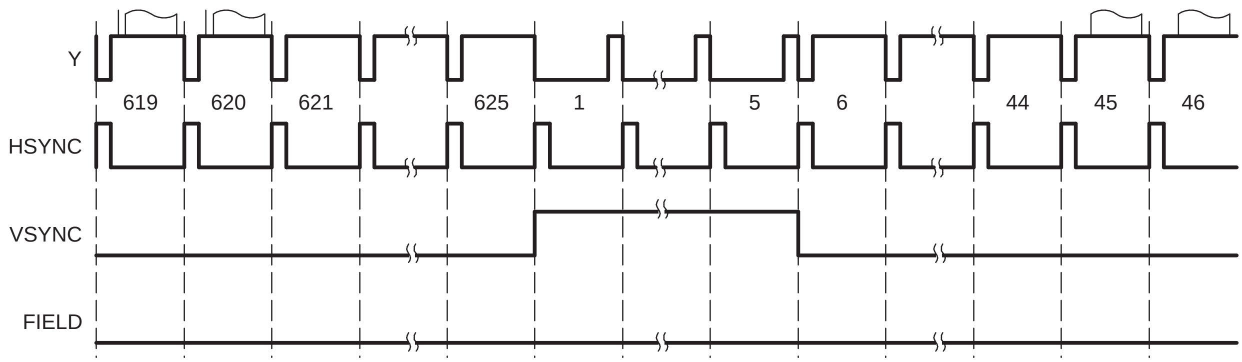


Figure 11. 625P Vertical Timing



2.1.3.5 Internal Color Bar Output Level

The NTSC/PAL encoder can internally generate color bars. Setting VDPRO.CBMD = 1 enables the internal color bar generator. The VDPRO.CBTY field switches the saturation of the color bar, 0 for 75%, 1 for 100%. Figure 12 and Figure 13 show the digital level of the video encoder when the internal color bar is enabled for each mode.

Figure 12. 100% Color Bar Output Level

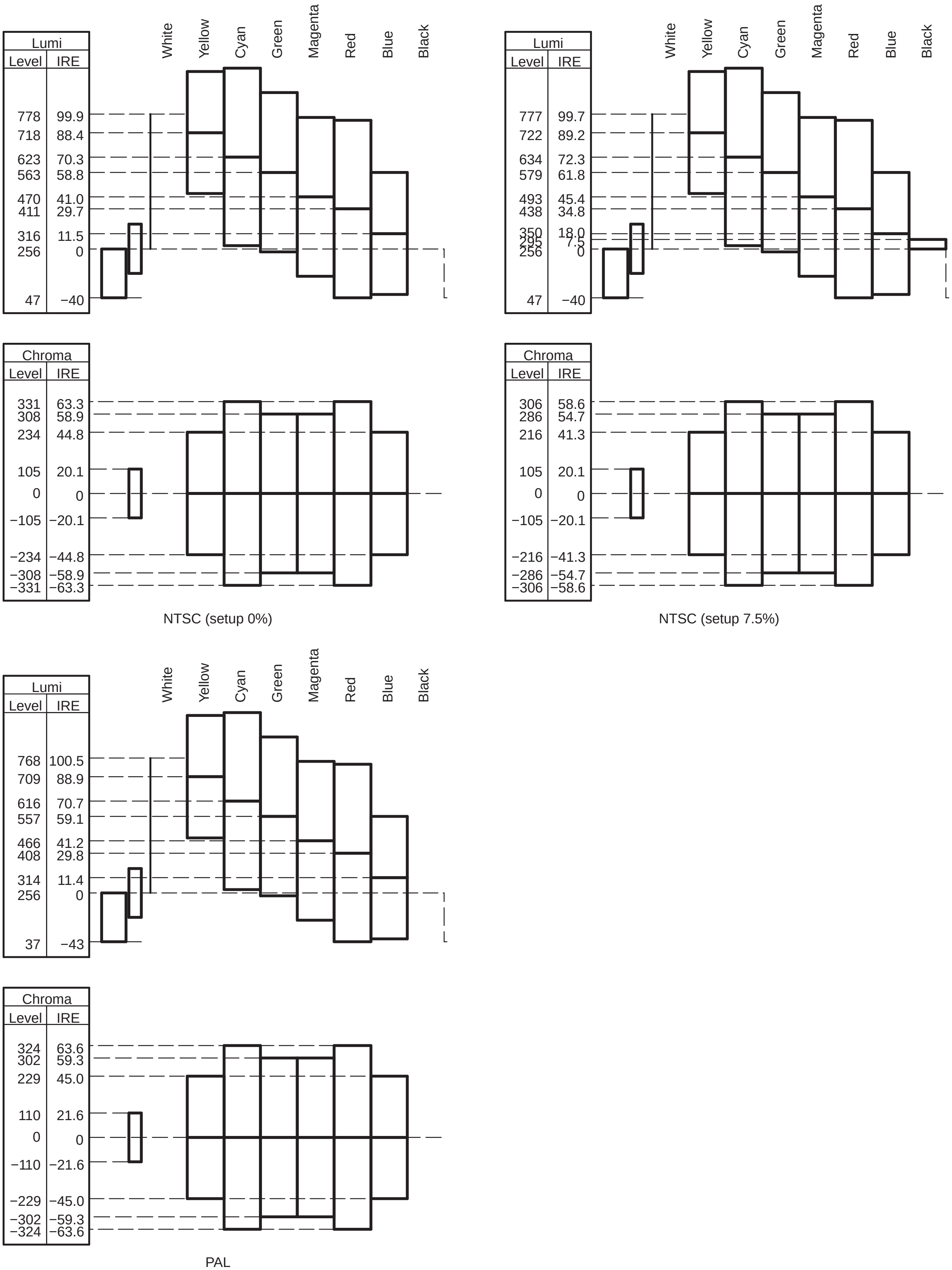
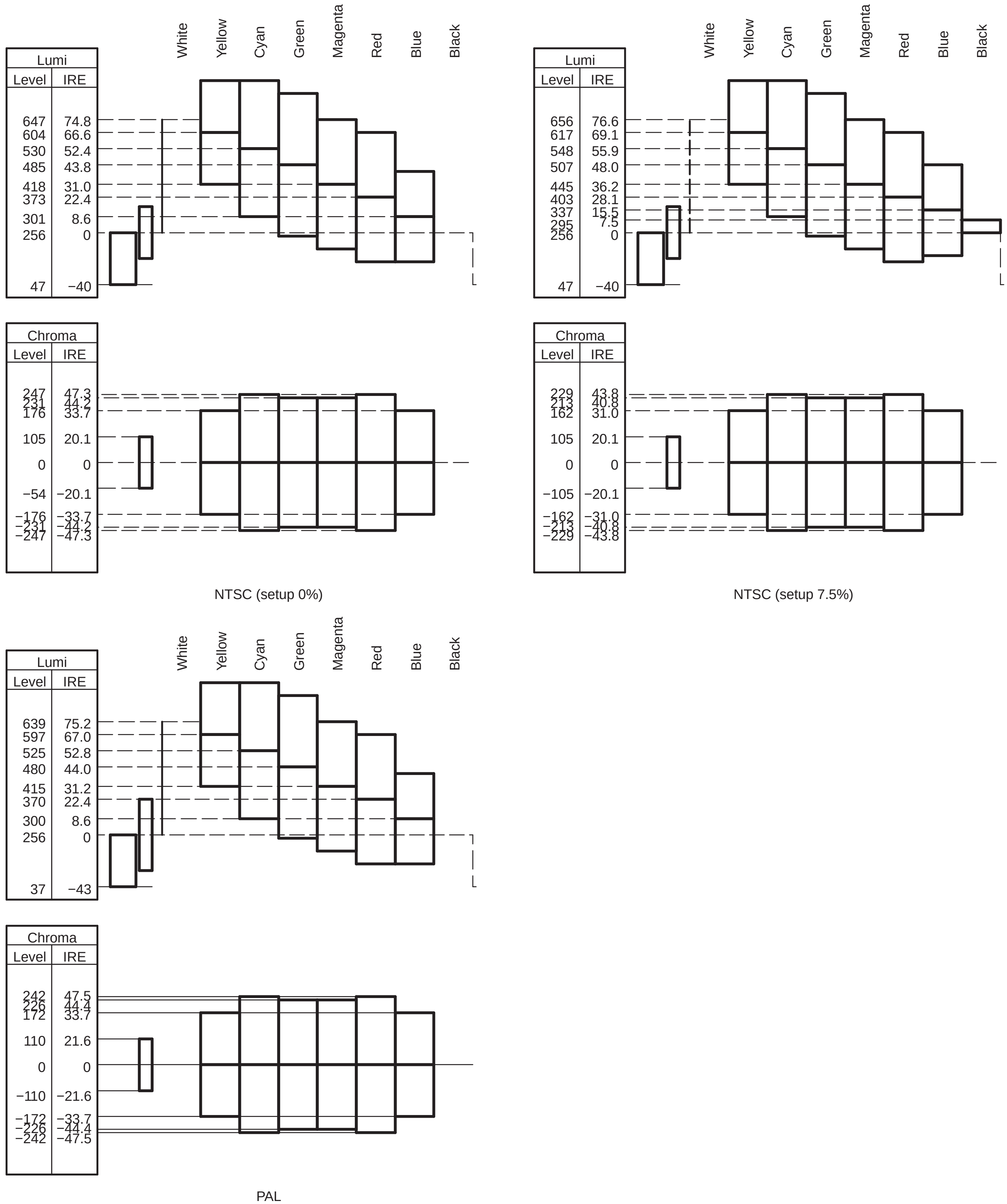


Figure 13. 75% Color Bar Output Level



2.2 Digital Display Interface

The digital display interface is used for driving various types of digital display devices. The digital display modes can be selected by VMOD.VDMD as listed in Table 7.

Table 7. Digital Display Modes

VMOD.VDMD	Mode	Description
0	YCC16	16-bit YCbCr output mode. Y and C are output separately on 16-bit bus.
1h	YCC8	8-bit YCbCr output mode. 422 YCbCr is time-multiplexed on the 8-bit bus. Optionally supports ITU-R BT.656 output.
2h	PRGB	Parallel RGB mode to output RGB separately.
3h-7h	-	Reserved

The digital image data output signals support multiple functions/interfaces, depending on the display mode selected. Table 8 describes these signals for the digital display modes. Note that parallel RGB with more than RGB565 signals requires enabling pin multiplexing to support (for RGB666 and RGB888 modes).

Table 8. Signals for VPBE Digital Display Modes

Pin Name	YCC16	YCC8/ REC656	RGB888	RGB666
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
VCLK	VCLK	VCLK	VCLK	VCLK
VPBECLK	VPBECLK	VPBECLK	VPBECLK	VPBECLK
YOUT7	Y7	Y7,Cb7,Cr7	R7	R7
YOUT6	Y6	Y6,Cb6,Cr6	R6	R6
YOUT5	Y5	Y5,Cb5,Cr5	R5	R5
YOUT4	Y4	Y4,Cb4,Cr4	R4	R4
YOUT3	Y3	Y3,Cb3,Cr3	R3	R3
YOUT2	Y2	Y2,Cb2,Cr2	G7	G7
YOUT1	Y1	Y1,Cb1,Cr1	G6	G6
YOUT0	Y0	Y0,Cb0,Cr0	G5	G5
COUT7	C7	LCD_AC	G4	G4
COUT6	C6	LCD_OE	G3	G3
COUT5	C5	BRIGHT	G2	G2
COUT4	C4	PWM	B7	B7
COUT3	C3	-	B6	B6
COUT2	C2	-	B5	B5
COUT1	C1	-	B4	B4
COUT0	C0	-	B3	B3
R2	-	-	R2	R2
B2	-	-	B2	B2
LCD_OE	LCD_OE	-	LCD_OE	LCD_OE
G0	-	-	G0	-
B0/LCD_FIELD	-	-	B0	LCD_FIELD
R0	-	-	R0	-
G1	-	-	G1	-
B1	-	-	B1	-
R1	-	-	R1	-

2.2.1 YCC16 Signal Interface

In YCC16 mode, the Y (luma) signal is output to YOUT[7:0] at every VCLK rising edge, while Cb and Cr (chroma) are alternately multiplexed onto COUT[7:0]. The order of chroma output is controlled by YCCCTL.YCP. The LCD output enable (LCD_OE) signal is asserted only when valid data is output; otherwise, the output signals are held low.Table 9 shows the interface connections for the YCC16 digital display interface.

Table 9. Interface Signals for YCC16 Digital Displays

Pin Name	Description
HSYNC	H sync
VSYNC	V sync
VCLK	Video Clock
VPBECLK	VPBE External Clock Input (optional)
YOUT7	Y OUT signal
YOUT6	Y OUT signal
YOUT5	Y OUT signal
YOUT4	Y OUT signal
YOUT3	Y OUT signal
YOUT2	Y OUT signal
YOUT1	Y OUT signal
YOUT0	Y OUT signal
COUT7	C OUT signal
COUT6	C OUT signal
COUT5	C OUT signal
COUT4	C OUT signal
COUT3	C OUT signal
COUT2	C OUT signal
COUT1	C OUT signal
COUT0	C OUT signal
LCD_OE	LCD_OE
B0/LCD_FIELD	LCD_FIELD

2.2.1.1 YCC16 Signal Interface Description

The YCC16 interface includes the 8-bit YOUT[7:0] and COUT[7:0] signals, along with the HSYNC, VSYNC, and VCLK signals. An optional VPBECLK input clock can be used if the internally generated VPBE clock is not fast enough; for example, to support HDTV display rates or any clock > 54 MHz.

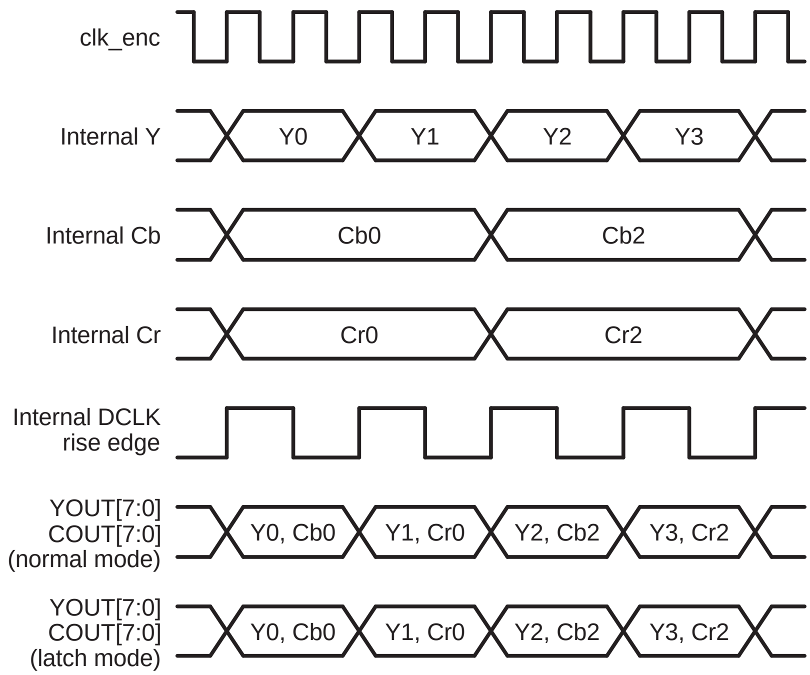
Note that the YOUT/COUT busses can be swapped via the VIDCTL.YCSWAP register setting.

Note that GP[13] must be separately assigned to function as LCD_OE and GP[11] must be separately assigned to function as LCD_FIELD in this mode.

2.2.1.2 YCC16 Protocol and Data Formats

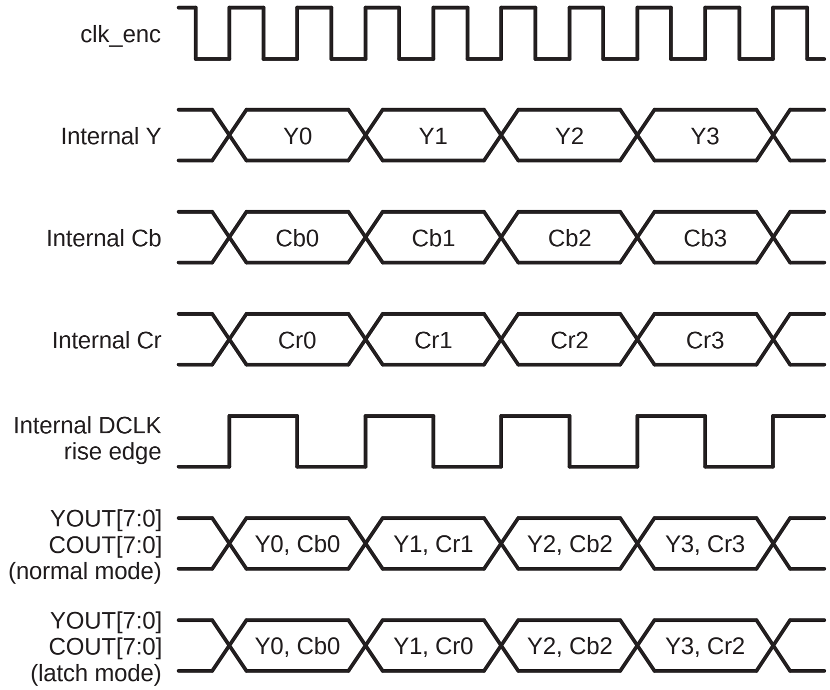
Figure 14 shows the output data sampling of the input YUV422 signal from the OSD module in normal operation. In this mode, the OSD blends the data and subsamples the chroma values to YUV422 format.

Figure 14. YCC16 Output for Normal OSD Operation



The OSD also includes support for window data in bitmap format, either 1, 2, 4, or 8-bit resolution via a YUV Color Look Up Table (CLUT) or via RGB565 bitmap format (Figure 15). Data corresponding to bitmap pixels is in full YUV444 resolution and is overlaid onto the YUV422 resolution video window pixel output. In this case, chroma blurring can occur at the edge between bitmap windows and the rest of the OSD image. In normal operation, the chroma value output from VENC is the immediate value at the sampling time. However, to alleviate this chroma blurring, a latch mode is provided where the chroma output for the second pixel in a UV pair can be the data latched at the first pixel. The latch mode is enabled by setting the CHM bit in the YCbCr control register (YCCTL) to 1.

Figure 15. YCC16 Output When OSD Window in RGB565



2.2.2 YCC8 Signal Interface, Including ITU-R BT.656

In YCC8 mode, each component of the OSD YCbCr signal is alternately output from YOUT[7:0]. The default output order is Cb-Y-Cr-Y but this can be modified by YCCCTL.YCP. Data output is enabled only when the LCD output enable (LCD_OE) signal is asserted. Table 10 shows the interface connections for the YCC8 digital display interface.

Table 10. Interface Signals for YCC8 Digital Displays

Pin Name	Description
HSYNC	H sync
VSYNC	V sync
VCLK	Video Clock
VPBECLK	VPBE External Clock Input (optional)
YOUT7	Y/C OUT signal
YOUT6	Y/C OUT signal
YOUT5	Y/C OUT signal
YOUT4	Y/C OUT signal
YOUT3	Y/C OUT signal
YOUT2	Y/C OUT signal
YOUT1	Y/C OUT signal
YOUT0	Y/C OUT signal
COUT7	Y/C OUT signal (optional, when bus is swapped)
COUT6	Y/C OUT signal (optional, when bus is swapped)
COUT5	Y/C OUT signal (optional, when bus is swapped)
COUT4	Y/C OUT signal (optional, when bus is swapped)
COUT3	Y/C OUT signal (optional, when bus is swapped)
COUT2	Y/C OUT signal (optional, when bus is swapped)
COUT1	Y/C OUT signal (optional, when bus is swapped)
COUT0	Y/C OUT signal (optional, when bus is swapped)

2.2.2.1 YCC8 Signal Interface Description

The YCC8 interface includes the 8-bit YOUT[7:0] or the 8-bit COUT[7:0] signals, along with the HSYNC, VSYNC, and VCLK signals. An optional VPBECLK input clock can be used if the internally generated VPBE clock is not fast enough; for example, to support HDTV display rates or any clock > 54 MHz.

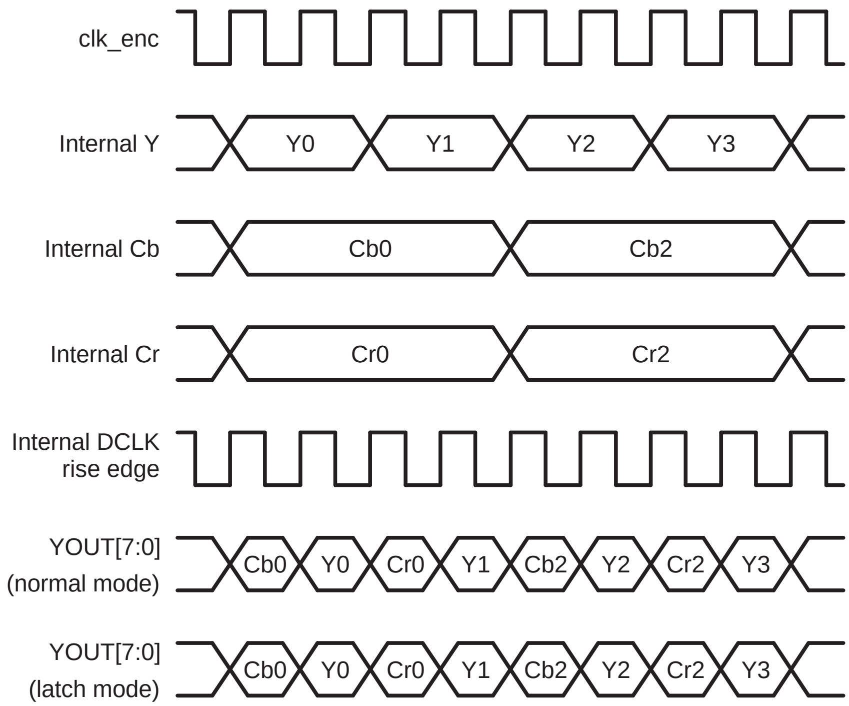
Note that in YCC8 mode, data is normally output on the YOUT bus. However, the YOUT/COUT busses can be swapped via the VIDCTL.YCSWAP register setting to output the YCC8 data on the COUT bus.

ITU-R BT.656 format output is optionally available in YCC8 mode and is enabled via YCCCTL.R656. In this mode, the YCbCr output timing and output order is fixed by hardware in order to conform to the standard and they cannot be altered by user. To use BT656 mode, the VENC must operate in the standard mode (VIDCTL.VDMD = 0). Note that this mode operates correctly only when the pixel clock frequency is half of the VENC clock. In this mode, the sync signals are embedded within the data stream and HSYNC/VSYNC are inactive.

2.2.2.2 YCC8 Protocol and Data Formats

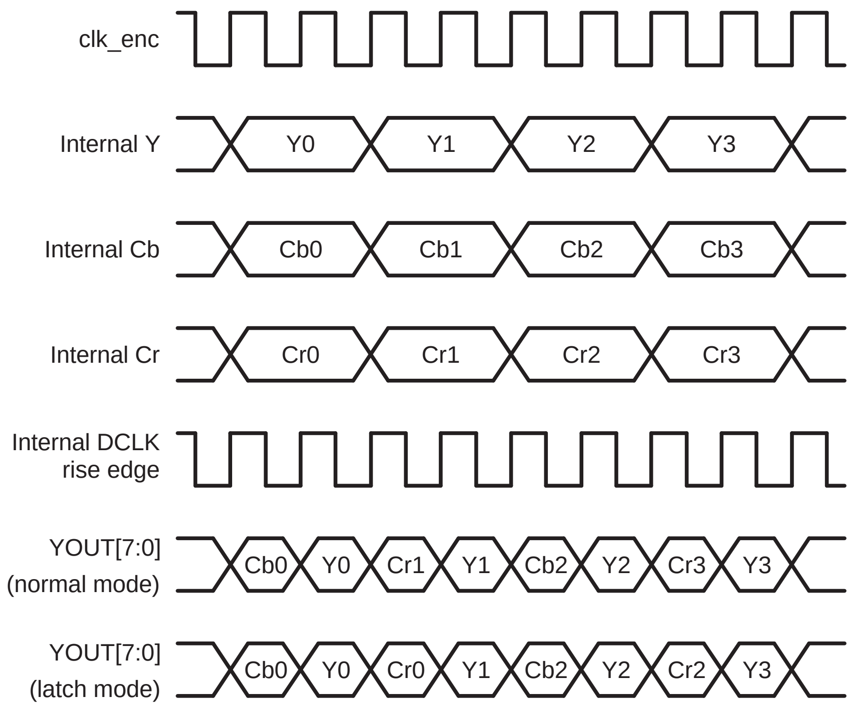
Figure 16 shows the output data sampling of the input YUV422 signal from the OSD module in normal operation. In this mode, the OSD blends the data and subsamples the chroma values to YUV422 format.

Figure 16. YCC8 Output for Normal OSD Operation



The OSD also includes support for window data in RGB565 format (Figure 17), which is converted to YUV444 format by the OSD and overlaid onto the YUV422 output. In this case, chroma blurring can occur at the edge between the RGB565 window and the rest of the OSD image. In normal operation, the chroma value output from VENC is the immediate value at the sampling time. However, to alleviate this chroma blurring, a latch mode is provided where the chroma output for the second pixel in a UV pair can be the data latched at the first pixel. The latch mode is enabled by setting YCCCTL.CHM to 1.

Figure 17. YCC8 Output When OSD Window in RGB565



2.2.3 Parallel RGB Signal Interface

For parallel RGB modes, up to 24-bit RGB display data is output in parallel. The upper bits of the RGB samples are multiplexed onto the YOUT and COUT pins. Output data is sub-sampled at DCLK rising edge when the LCD output enable (LCD_OE) signal is asserted and output signals are held low when LCD_OE is de-asserted. Table 11 shows the interface connections for the parallel RGB digital display interface.

Table 11. Interface Signals for Parallel RGB Digital Displays

Pin Name	Description
HSYNC	H sync
VSYNC	V sync
VCLK	Video Clock
VPBECLK	VPBE External Clock Input (optional)
YOUT7/R7	R7
YOUT6/R6	R6
YOUT5/R5	R5
YOUT4/R4	R4
YOUT3/R3	R3
YOUT2/G7	G7
YOUT1/G6	G6
YOUT0/G5	G5
COUT7/G4	G4
COUT6/G3	G3
COUT5/G2	G2
COUT4/B7	B7
COUT3/B6	B6
COUT2/B5	B5
COUT1/B4	B4
COUT0/B3	B3
R2	R2
B2	B2
LCD_OE	LCD_OE
G0	G0
B0/LCD_FIELD	B0
R0	R0
G1	G1
B1	B1
R1	R1

2.2.3.1 Parallel RGB Signal Interface Description

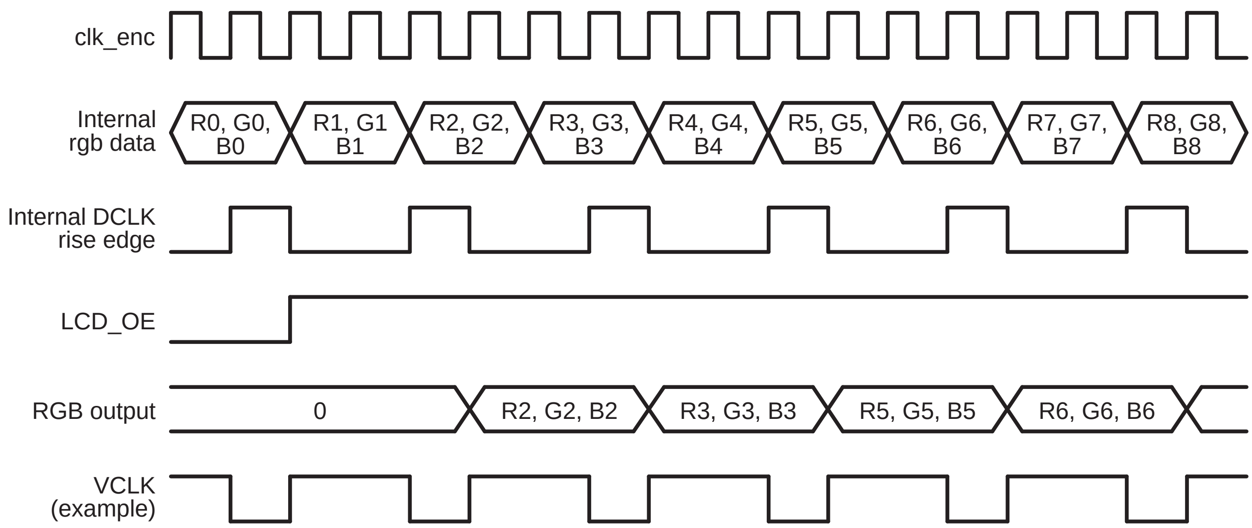
In parallel RGB mode, an RGB565 interface (5-bits red, 6-bits green, 5-bits blue) can be supported via the normal YOUT/COUT signals without requiring additional GPIO signals. In addition to this, RGB666 and RGB888 modes can be supported by assigning additional GPIO pins to the display interface. This assignment done via the pin multiplexing is controlled from the System Module. In addition to these signals, the HSYNC, VSYNC, and VCLK signals are also output. An optional VPBECLK input clock can also be used.

Note that GP[13] must be separately assigned to function as LCD_OE in this mode.

2.2.3.2 Parallel RGB Protocol and Data Formats

Figure 18 shows the output data sampling of the input YUV422 signal from the OSD module converted by the VENC to RGB888 format. In this diagram, the values R0, G0, B0, etc. refer to pixel locations.

Figure 18. RGB Output in Parallel RGB Mode



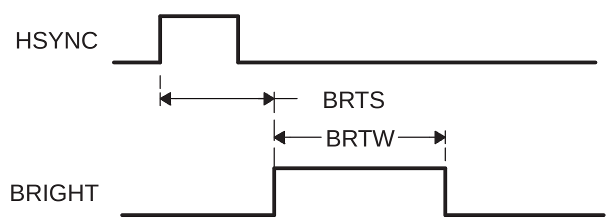
2.2.4 Other Digital LCD Interface Signals

The following LCD signals can be optionally generated. Utilize them as appropriate. For the signal availability in each mode, see Table 8.

2.2.4.1 BRIGHT Signal

- Polarity can be inverted via LCDOUT.BRP.
- When using the BRIGHT signal, set LCDOUT.BRE to 1.
- The units of BRTS and BRTW are in VCLK periods.

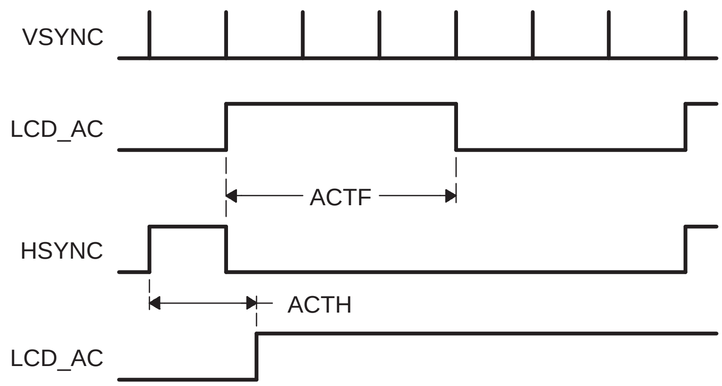
Figure 19. BRIGHT Signal Timing



2.2.4.2 LCD_AC Signal

- When using the LCD_AC signal, set LCDOUT.ACE to 1.
- The units of ACCTL.ACTH and ACCTL.ACTF are VCLK and line, respectively.

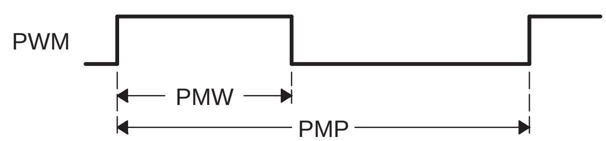
Figure 20. LCD_AC Signal Timing



2.2.4.3 PWM Signal

To use the pulse width modulation (PWM) signal, set LCDOUT.PWME to 1. Polarity can be inverted by LCDOUT.PWMP. This is a free-run signal and is not synchronized to any sync signals. The unit is VCLK. In Figure 21, PWM = PWMW register and PMP = PWMP register.

Figure 21. PWM Signal Timing



2.3 VPBE Display Subsystem Pin Multiplexing

On the DM643x DMP extensive pin multiplexing is used to accommodate the largest number of peripheral functions in the smallest possible package. Pin multiplexing is controlled using a combination of hardware configuration at device reset and software programmable register settings. Refer to the device-specific data manual to determine how pin multiplexing affects the VPBE.

2.4 VPSS Initialization

The following steps are required to configure the VPSS:

1. Perform the necessary device pin multiplexing setup (see the device-specific data manual).
2. Program the VDD3P3V_PWDN register in the System Module to power up the IO pins for the VPSS (see the device-specific data manual).

3 Integration

This section describes how the VPBE subsystem is integrated into the TMS320DM643x DMP.

3.1 Clocking, Reset, and Power Management Scheme

3.1.1 Clocks

3.1.1.1 Processing and DMA Clock

The DM643x VPBE module is a DMA master and resides in the CLKDIV3 clock domain; thus, its processing logic is clocked at 153 MHz (Normal mode) or 198 MHz (Turbo mode). This clock is the VPSSmstr module in the Power and Sleep Controller (PSC) and it is shared with the video processing front end (VPFE). Thus, this clock can be gated off to conserve power, but this also precludes use of the VPFE. The VPBE modules utilize auto clock gating on a clock-by-clock basis to conserve dynamic power during periods of inactivity. In addition, the VPBE clocks can be gated off using the CLK_OFF bit in the VPBE peripheral control register (PCR).

Note that the clock should only be disabled when the VPBE is not operational. The clocks should be enabled prior to any other operations on the VPBE (including reading/writing other registers).

3.1.1.2 Register Interface Clock

The DM643x VPBE module includes a Slave Port for the control registers that resides in the CLKDIV6 clock domain; thus, the CPU register interface is clocked at 76.5 MHz (Normal mode) or 99 MHz (Turbo mode). This clock is the VPSSslv module in the PSC and it is shared with the VPFE. Thus, this clock can be gated off to conserve power, but this also precludes use of the VPFE.

3.1.1.3 DAC and External Clock

Note: The VPFE pixel clock input (PCLK) is not available on all devices. Check your device-specific data manual for PCLK availability.

The VPBE must interface with a variety of LCDs, as well as the 4-channel DAC module. There are many different types of LCDs, which require many different specific frequencies. The range of frequencies that the pin interface needs to run is 6.25 MHz to 75 MHz.

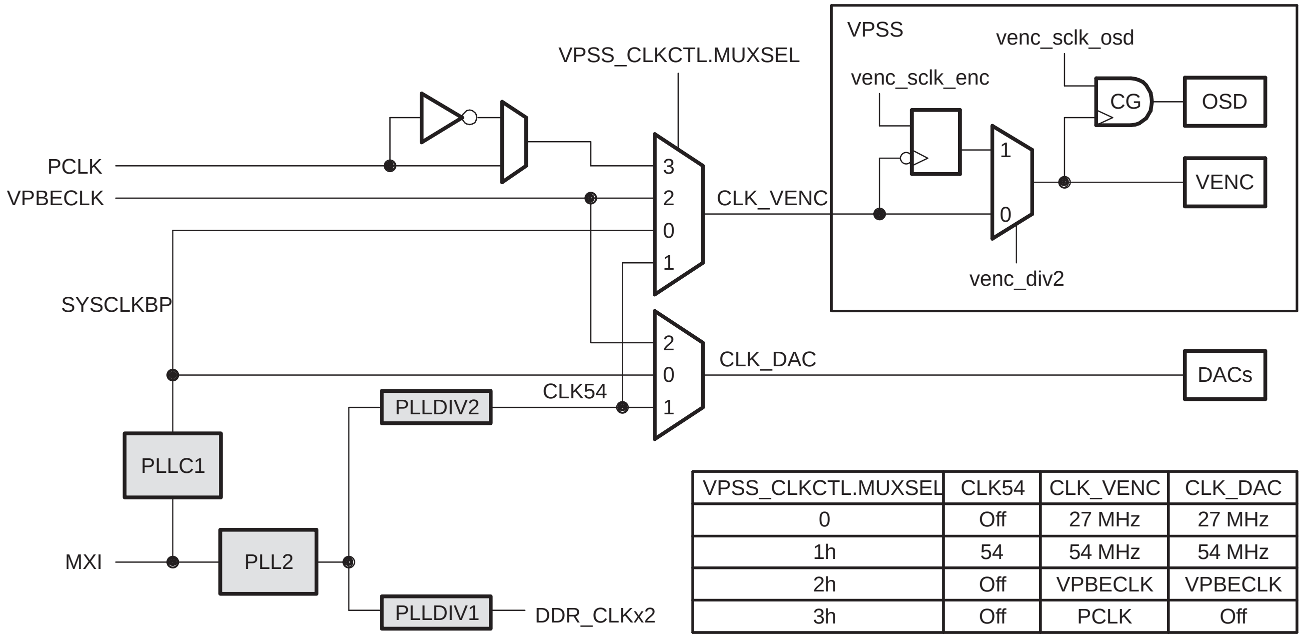
The external clock domain (6.25 MHz to 75 MHz) is asynchronous to the internal or system clock domain, which is at the PLL1/3 clock rate. The external clock domain can get its clock from 4 sources:

- The 27 MHz crystal input
- The VPBECLK input pin
- The VPFE pixel clock input (PCLK)
- The PLLDIV1 divide-down output from PLL2 (for 27/54 MHz operation)

The 4 video DACs are hooked up to the VENC module that is inside the VPBE. The data flow between the VPBE and DACs is synchronous. The various clocking modes possible are shown in Figure 22.

The DACs can also have their clocks independently gated off when the DACs are not being used.

Figure 22. VPBE/DAC Clocking Options



VPSS_CLKCTL.MUXSEL	CLK54	CLK_VENC	CLK_DAC
0	Off	27 MHz	27 MHz
1h	54	54 MHz	54 MHz
2h	Off	VPBECLK	VPBECLK
3h	Off	PCLK	Off

The VPBE clock is controlled by the MUXSEL bits in the VPSS clock mux control register (VPSS_CLKCTL), see Section 3.1.1.4, of the System Module.

- MUXSEL = 0 (MXI mode): Both the DAC and VENC get their clock from PLLC1 SYSCLKBP, which defaults to the MXI 27 MHz crystal input.
- MUXSEL = 1h (PLL2 mode): The PLL2 (divided-down) generates a 54 MHz clock. Both the DAC and the VENC receive the 54 MHz. In this mode, the VENC clock must be divided-down 27 MHz via the VENC_DIV bit in the VPBE peripheral control register (PCR). Note this mode requires the DDR2 clock setting (from PLL2) to be an even multiple of 27 MHz so that an integer divisor can be used to create the 54 MHz DAC clock. Thus, this mode limits the available DDR2 clock frequencies.
- MUXSEL = 2h (VPBECLK mode): Both the DAC and VENC receive the VPBECLK. The VENC optionally can divide this frequency by 2, for progressive scan support driving in 54 MHz on VPBECLK.
- MUXSEL = 3h (PCLK mode): The VENC receives the PCLK. The DAC receives no clock, and should be disabled. PCLK can be inverted for negative edge support, selectable by the PCLKINV bit in VPSS_CLKCTL.

In addition to the clock multiplex control, VPSS_CLKCTL also includes controls for enabling/disabling of the DAC clock (DACCLKEN) and enabling/disabling of the VPBE clock (VENCLKEN). In addition, the VPBE clock can be gated off using the CLK_OFF bit in the VPBE peripheral control register (PCR).

3.1.1.4 VPSS Clock Mux Control Register (VPSS_CLKCTL)

The VPSS clock mux control register (VPSS_CLKCTL) is shown in Figure 23 and described in Table 12.

Figure 23. VPSS Clock Mux Control Register (VPSS_CLKCTL)

31–16
Reserved
R-0

15–5	4	3	2	1–0
Reserved	DACCLKEN	VENCLKEN	PCLKINV	MUXSEL
R-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 12. VPSS Clock Mux Control Register (VPSS_CLKCTL) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Reserved
4	DACCLKEN		Video DAC clock enable.
		0	Video DAC clock is disabled.
		1	Video DAC clock is enabled.
3	VENCLKEN		VPBE/Video encoder clock enable.
		0	VPBE/Video encoder clock.is disabled.
		1	VPBE/Video encoder clock.is enabled.
2	PCLKINV		VPFE pixel clock (PCLK) invert enable.
		0	VENC clock mux and CCDC receive noninverted PCLK.
		1	VENC clock mux and CCDC receive inverted PCLK.
1-0	MUXSEL	0-3h	VPSS clock selection.
		0	MXI mode. Use 27 MHz (from MXI27) (DAC clock = 27 MHz).
		1h	PLL2 mode. Use 54 MHz (from PLLC2) (DAC clock = 54 MHz).
		2h	VPBECLK mode. Use external VPBE clock input (DAC clock = VPBECLK).
		3h	PCLK mode. Use PCLK from VPFE (DAC clock = off).

3.1.2 Resets

The DM643x VPBE module resets are tied to the device reset signals.

In addition, the VPBE modules can be reset by transitioning to the SyncReset state of the PSC. Note that the VPBE is a subset of the VPSS module and has two module domains, the VPSSmstr processing domain and the VPSSslv register interface; thus, resetting either of these also affects the video processing front end (VPFE).

3.1.3 Power Domain and Power Management

The VPBE module resides in the “Always On” power domain, along with the DSP core and other peripherals. When enabled, the VPFE modules utilize auto clock gating on a clock-by-clock basis to conserve dynamic power during periods of inactivity. Active power consumption can also be managed proactively via numerous clock enable/disable controls. The following sections describe the various clock gating methods, and the guidelines that must be met to gate the clocks.

3.1.3.1 General Power Down Guidelines

Active power consumption is minimized when clocks are disabled. The three levels of clock gating the VPSS are as follow:

- Clock gate within the VPSS by programming the VPSS registers (for example, using VPBE.PCR.CLK_OFF, VENC.VMOD.VENC, CCDC.PCR.ENABLE). This method allows you to selectively clock gate portions within the VPSS.
- Clock gate through the Local Power and Sleep Controller (LPSC0 and LPSC1). This stops the clocks at the VPSS boundary. This level of clock gating is only allowed if the entire VPSS is not used. This method cannot be used to selectively clock gate portions of the VPSS. This method not only stops the video clock sources at the VPSS boundary, it also stops the chip-level system clocks to the VPSS logic and VPSS register interface.
- Clock gate at the clock source (for example, using SYSTEM.VPSS_CLKCTL.VENCLKEN, SYSTEM.VPSS_CLKCTL.DACCLKEN). This method allows you to selectively clock gate portions of the VPSS by gating only the clock sources not needed. This method is typically used along with the first method to maximize power saving by stopping clocks at their sources.

The following sections make use of one or more of these methods to achieve power savings.

3.1.3.2 Minimize Active Power when Entire VPSS is Not Used

If the entire VPSS is not used, power saving can be achieved by stopping the clock at the VPSS boundary (using the Power and Sleep Controller (PSC)), and also at the clock source.

Use PSC to completely disable the VPSS module and all logic gated by external clocks:

- Disable the VPSSmstr module in the PSC (either Disable or SwRstDisable). This disables the clock to the VPSS logic and the VPSS shared DMA logic and memory buffers. Note that this also disables the VPFE logic.
- Disable the VPSSslv module in the PSC (either Disable or SwRstDisable). This disables the clock to the VPSS register interface. Note that this also disables the register interface for the VPFE modules.

To disable clock sources to the VPSS module:

- VPFE clock sources
  - – Disable any external imaging device driving the VPFE pixel clock (PCLK) to avoid clocking any input logic and any of the VPBE logic via passthrough.
- VPBE clock sources:
  - – Stop the clocks by programming the VPSS clock mux control register (VPSS_CLKCTL) in the System Module:
    - Stop the DAC clock directly by clearing the DACCLKEN bit in VPSS_CLKCTL to 0.
    - Stop the VENC clock directly by clearing the VENCLKEN bit in VPSS_CLKCTL to 0.
  - – For further power savings, you can disable all of the VPBE clock sources:
    - VPBECLK: Disable any external VPBECLK source to avoid clocking any output logic.
    - PCLK: Disable any external PCLK source.
    - PLLC1 SYSCLKBP: Disable PLLC1 SYSCLKBP clock source by clearing the BPDEN bit in BPDIV to 0 in PLL Controller 1.
    - PLLC2 SYSCLK2: Disable PLLC2 SYSCLK2 clock source by clearing the D2EN bit in PLLDIV2 to 0 in PLL Controller 2.

3.1.3.3 Minimize Active Power When Video DAC is Not Used

If the video DAC of the VPBE is not used, perform the following step to minimize active power:

- Stop the DAC clock directly by clearing the DACCLKEN bit in the VPSS clock mux control register (VPSS_CLKCTL) to 0.
- Note that when PCLK is used for the VPBE (CLK_VENC), the DAC clock is automatically disabled: set the MUXSEL bits in VPSS_CLKCTL to 3h.

3.1.3.4 Minimize Active Power When only VPBE is Used (VPFE is Disabled)

In VPBE only mode, where the VPFE is not used, perform the following step to minimize active power:

VPBE only mode: Clock gate VPFE only, but keep VPBE active:

- Disable the CCD controller (CCDC) in the VPFE by clearing the ENABLE bit in the CCDC peripheral control register (PCR) to 0. If only selected modules within the VPFE need to be clock gated, program the individual enable bits (within the VPFE submodules) to disable the modules (Resizer, Histogram, etc.). Note that modules are disabled by default, so coming out from a device reset makes this step not necessary. Another point, if the CCDC is disabled, other modules (primarily the Resizer) can still be used if the module has an input path from the DDR.
- For further power saving, disable any external imaging device driving the VPFE pixel clock (PCLK) to avoid clocking any input logic and any of the VPBE logic via passthrough.

If the video DAC of the VPBE is not needed, further power saving can be achieved by following Section 3.1.3.3 to clock gate the video DAC.

3.1.3.5 Minimize Active Power When only VPFE is Used (VPBE is Disabled)

In VPFE only mode, where the entire VPBE is disabled and is not used, perform the following step to minimize active power:

VPFE only mode: Clock gate VPBE only, but keep VPFE active:

- Gate all VPBE clocks off by setting the CLK_OFF bit in the VPBE peripheral control register (PCR) to 1.
- Disable the video encoder (VENC) operation by clearing the VENC bit in the VENC video mode register (VMOD) to 0.
- For further power savings, gate the clocks at the source:
  – Gate CLK_VENC by stopping it at the source (at the clock input pin or by clearing the VENCLKEN bit in the VPSS clock mux control register (VPSS_CLKCTL) to 0).
  – Gate CLK_DAC by stopping it at the source (at the clock input pin or by clearing the DACCLKEN bit in VPSS_CLKCTL to 0).

3.2 Hardware Requests

3.2.1 Interrupt Requests

The VPBE generates an interrupt (VENCINT) to the DSP. This indicates an end-of-frame event, for example, processing has completed for a frame.

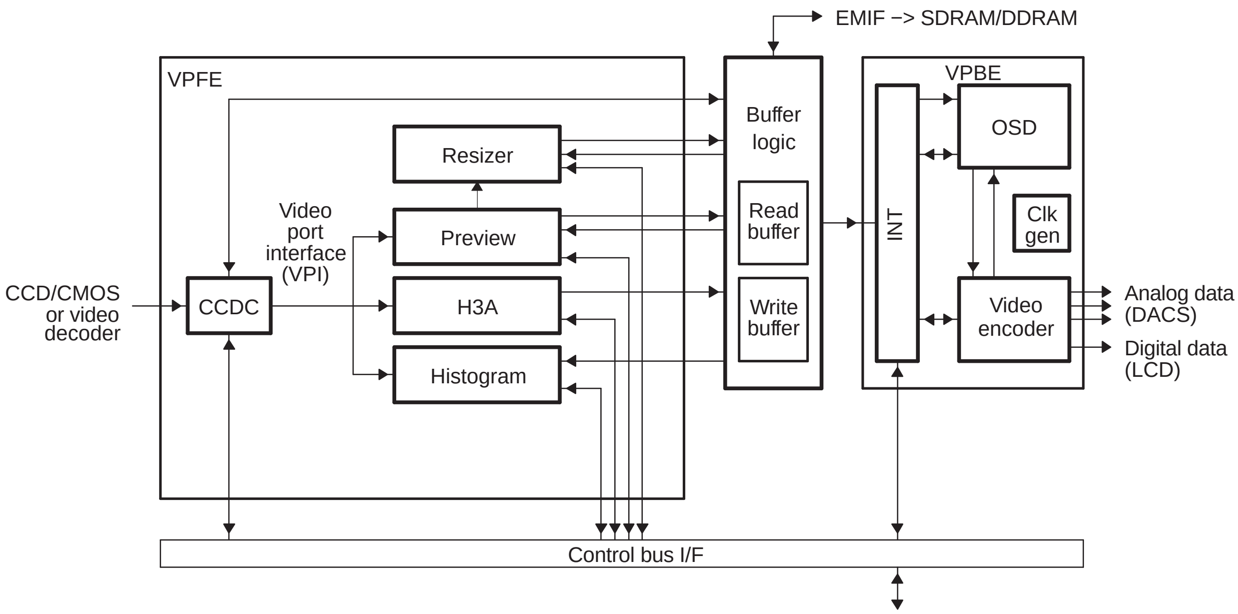
3.2.2 EDMA Requests

There are no VPBE-related EDMA events since the VPBE is a DMA master and nothing needs to be tied to display frame completion.

4 Functional Description

This section provides a functional description of the VPBE. The video processing subsystem is shown in Figure 24.

Figure 24. Video Processing Subsystem (VPSS) Block Diagram



4.1 *Interfacing with Displays*

The VENC/digital LCD controller supports several display/output interfaces described in the following sections. For further details on configuring the VENC for operation in the various modes, see Section 5.

4.1.1 Analog Display Interface

The analog display interface uses four DAC signals as described in Table 13.

Table 13. Analog Display Interface Signals

Name	I/O	Function
DAC_IOUT_A DAC_IOUT_B DAC_IOUT_C DAC_IOUT_D	O	Analog image data • Mode set by the VDMD bit in VMOD. • DAC selection is set by the DA*n*S bit in DACSEL.

4.1.2 YCC16 Digital Display Interface

The YCC16 interface includes the signals described in Table 14.

Table 14. YCC16 Digital Display Interface Signals

Name	I/O	Function
YOUT[7:0] COUT[7:0]	O	Image Data – mode set by VMOD.VDMD • Busses can be swapped via YCSWAP bit in VIDCTL. • Cb, Cr order controlled by the YCP bit in YCCCTL.
VSYNC	I/O	VSYNC - vertical sync signal • This signal can be configured as an input or an output (SLAVE bit in VMOD) • When configured as an output, the OSD/VENC supplies the VD signal • When configured as an input, the Display supplies the VD signal
HSYNC	I/O	HSYNC – horizontal sync signal • This signal can be configured as an input or an output (SLAVE bit in VMOD) • When configured as an output, the OSD/VENC supplies the HD signal • When configured as an input, the Display supplies the HD signal
LCD_OE	O	LCD output enable signal • This signal indicates when the VENC/DLCD outputs valid data
VCLK	O	Video pixel clock • This signal is the pixel clock used to indicate valid display data
VPBECLK	I	VPBE pixel clock (SYSTEM.VPSS_CLKCTL.MUXSEL) • This signal is the optional input pixel clock

4.1.3 YCC8 Digital Display Interface

The YCC8/REC656 interface includes the signals described in Table 15.

Table 15. YCC8 Digital Display Interface Signals

Name	I/O	Function
YOUT[7:0] or COUT[7:0]	O	Image Data – mode set by the VDMD bit in VMOD, REC656 mode set by the R656 bit in YCCCTL. • Busses can be swapped via YCSWAP bit in VIDCTL. • Y, Cb, Cr order controlled by the YCP bit in YCCCTL.
VSYNC	I/O	VSYNC - vertical sync signal • This signal can be configured as an input or an output (SLAVE bit in VMOD) • When configured as an output, the OSD/VENC supplies the VD signal • When configured as an input, the Display supplies the VD signal
HSYNC	I/O	HSYNC – horizontal sync signal • This signal can be configured as an input or an output (SLAVE bit in VMOD) • When configured as an output, the OSD/VENC supplies the HD signal • When configured as an input, the Display supplies the HD signal
LCD_OE	O	LCD output enable signal • This signal indicates when the VENC/DLCD outputs valid data
VCLK	O	Video pixel clock • This signal is the pixel clock used to indicate valid display data
VPBECLK	I	VPBE pixel clock (SYSTEM.VPSS_CLKCTL.MUXSEL) • This signal is the optional input pixel clock

4.1.4 Parallel RGB Digital Display Interface

The parallel RGB interface includes the signals described in Table 16.

Table 16. Parallel RGB Digital Display Interface Signals

Name	I/O	Function
R[7:0], G[7: 0], B[7:0]	O	Image Data – mode set by the VDMD bit in VMOD. • Default is RGB565 • Use system register PINMUX0.RGB888 to setup RGB888 mode • Use system register PINMUX0.RGB666 to setup RGB666 mode
VSYNC	I/O	VSYNC - vertical sync signal • This signal can be configured as an input or an output (SLAVE bit in VMOD) • When configured as an output, the OSD/VENC supplies the VD signal • When configured as an input, the Display supplies the VD signal
HSYNC	I/O	HSYNC – horizontal sync signal • This signal can be configured as an input or an output (SLAVE bit in VMOD) • When configured as an output, the OSD/VENC supplies the HD signal • When configured as an input, the Display supplies the HD signal
LCD_OE	O	LCD output enable signal • This signal indicates when the VENC/DLCD outputs valid data
VCLK	O	Video pixel clock • This signal is the pixel clock used to indicate valid display data
VPBECLK	I	VPBE pixel clock (SYSTEM.VPSS_CLKCTL.MUXSEL) • This signal is the optional input pixel clock

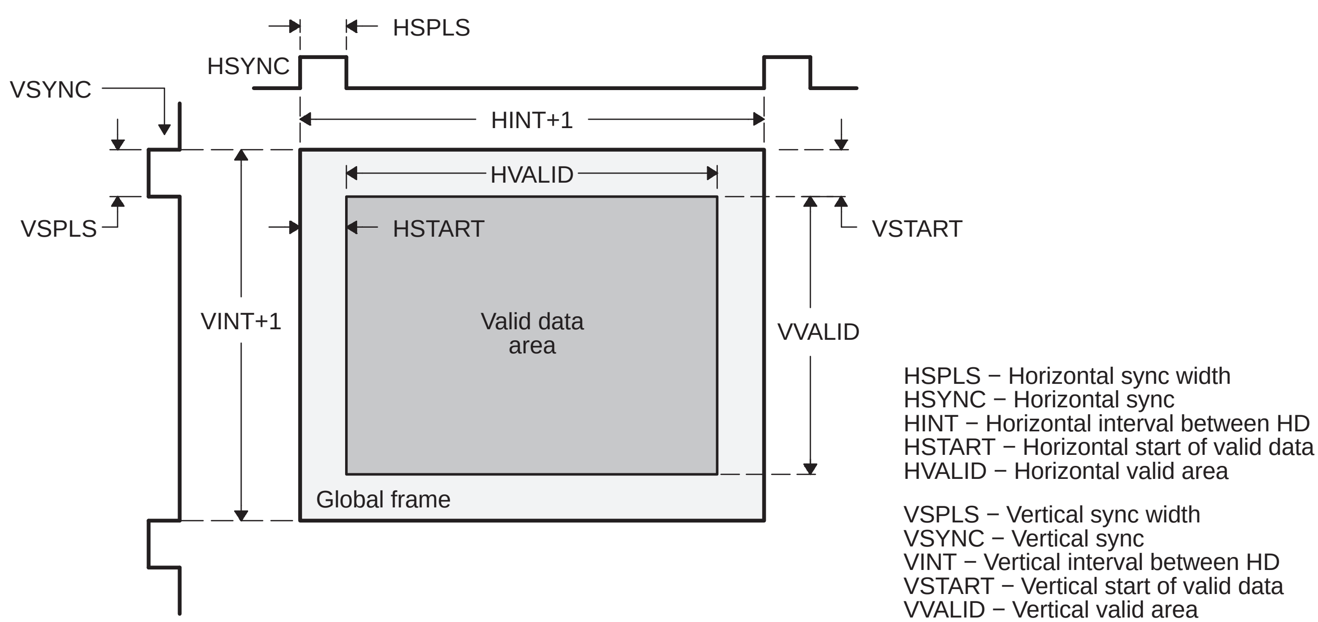
4.2 Master/Slave Mode Interface

The DM643x device can be separately configured to either source or sink the VSYNC/HSYNC signals. If master mode is set by clearing the SLAVE bit in VMOD to 0, the SYDIR bit in VIDCTL must be cleared to output the sync signals. In addition, the registers listed in Table 17 must be set to define the output frame (Figure 25).

Table 17. Master Mode Configuration Registers

Acronym	Register
HSPLS	Horizontal sync pulse width
VSPLS	Vertical sync pulse width
HINT	Horizontal interval
HSTART	Horizontal valid data start position
HVALID	Horizontal data valid range
VINT	Vertical interval
VSTART	Vertical valid data start position
VVALID	Vertical data valid range
HSDLY	Horizontal sync delay
VSDLY	Vertical sync delay

Figure 25. CCD Controller Frame and Control Signal Definitions



NOTE: HINT + 1 must be even when OSD clock is 1/2 VENC clock.

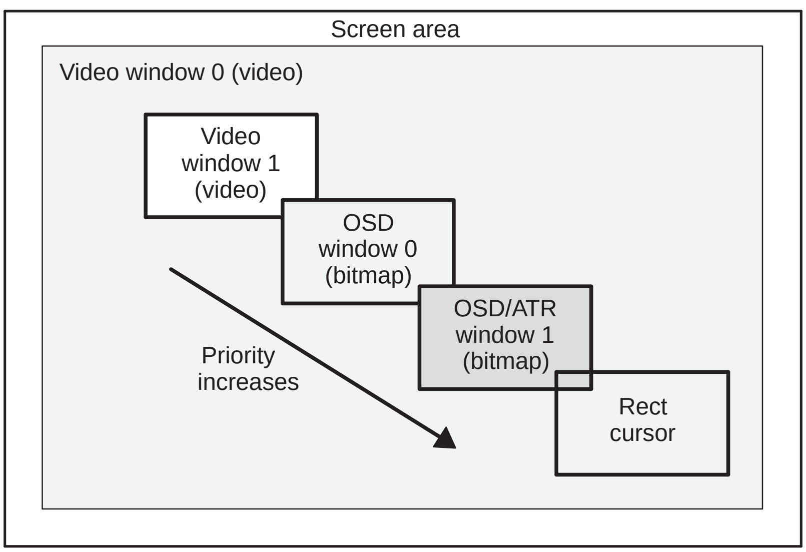
4.3 On-Screen Display (OSD) Module

The on-screen display (OSD) module reads data in various window formats from DDR2 and converts them into YUV display data, blends the various windows using the fixed display priority and any optional blending and transparency rules and sends the combined display image to the VENC for conditioning and output. The OSD windows (Table 18 and Figure 26) show the display priority, window type, and data types supported by each window. For the constraints on each window type when supporting HD resolution video, see Section 4.3.1.

Table 18. OSD Windows

Window	Priority	Type	Data Types	Control Register	Description
CURSOR	1	Rectangular outline w/transparent center	NA	RECTCUR	Controls the size and on/off control of rectangular cursor window
OSD1	2	Bitmap (or Attribute)	Bitmap, RGB565, or Attribute	OSDWIN1MD	Controls the display, zoom blending, and on/off control of OSD window 1
OSD0	3	Bitmap	Bitmap or RGB565	OSDATRMD	Controls the blinking, display, zoom, on/off control of Attribute window
VID1	4	Video	YUV422 or RGB888	OSDWIN0MD	Controls the display, zoom blending, and on/off control of OSD window 0
VID0	5	Video	YUV422 or RGB888	VIDWINMD	Controls the display, zoom and on/off control of Video windows

Figure 26. OSD Window Display Priorities



4.3.1 Video Window Constraints

The following constraints are for each window type in support of HD resolution video.

- **Video window 0:** Use video window 0 for HD display.
- **Video window 1:** Do not use video window 1 (turn off video window 1 when doing HD display).
- **OSD windows 0 and 1:** You may use the OSD windows but their combined total bandwidth must be less than 25 Mbytes/second.

  The bandwidth for the OSD windows depends on the size of the windows and also the bytes per pixel associated with the input data format. The equation is:

  $[(x0 \times y0) \times b0 + (x1 \times y1) \times b1] \times 60 < 25$ *Mbytes/second*

  Where:

  x0 = horizontal size of OSD window 0 in units of pixels

  y0 = vertical size of OSD window 0 in units of pixels

  b0 = bytes per pixel (depends on data input format selected for the OSD window)

  x1 = horizontal size of OSD window 0 in units of pixels

  y1 = vertical size of OSD window 0 in units of pixels

  b1 = bytes per pixel (depends on data input format selected for the OSD window)

  60 = frame rate for HD video

4.3.2 OSD Configuration and Control

Many of the OSD registers contain bits that are latched by the VD signal, which is the vertical sync pulse generated by the video encoder module. Data written to a latched bit does not take affect until the VD pulse is received. This allows registers that control the OSD, such as the SDRAM data address, display window size, display zoom configuration, etc. to be changed between successive VD pulses without corrupting the current display.

4.3.2.1 DDR Addresses

The location of data stored in SDRAM is defined by several memory-mapped registers (Table 19). The SDRAM addresses are specified in units of bytes with an absolute address. However, since data is transferred from SDRAM to the OSD in bursts of 32 bytes, the addresses must be 32-byte aligned, that is, the 5 LSBs of the address should be 00000.

Table 19. OSD SDRAM Address Registers

SDRAM Address Register	Window
VIDWIN0ADR	Video Window 0 address register
VIDWIN1ADR	Video Window 1 address register
OSDWIN0ADR	OSD Bitmap Window 0 address register
OSDWIN1ADR	OSD Bitmap Window 1/Attribute Window address register

4.3.2.2 DDR Offsets

The offset registers (Table 20) specify the address offset between each horizontal line of display data. Since this is independent of the window display size, this allows a subset of an image to be displayed. The offset is in units of 32 bytes. Therefore, the width of each line of data stored in SDRAM must be multiple of 32 bytes. If the width of data is not a multiple of 32 bytes, then it must be padded when stored in SDRAM.

Table 20. OSD SDRAM Offset Registers

SDRAM Address Register	Window
VIDWIN0OFST	Video Window 0 SDRAM offset register
VIDWIN1OFST	Video Window 1 SDRAM offset register
OSDWIN0OFST	OSD Bitmap Window 0 SDRAM offset register
OSDWIN1OFST	OSD Bitmap Window 1/Attribute Window SDRAM offset register

4.3.2.3 Window Positioning

All windows use a common reference pixel (base pixel). The position of this pixel is determined from the beginning of the video encoder HD and the beginning of the video encoder VD signal. For each window (video, bitmap, and cursor), the location of the upper left corner is specified, along with the horizontal and vertical display sizes. The relationship of the display positions of each window is shown in Figure 27.

Window start position is specified with respect to the BASEP_X and BASEP_Y position. Window start position in X-direction and window width is specified in units of pixels. Window start position in Y-direction and window height is specified in units of lines. When the VENC is in interlaced mode, window vertical position and height (*YP and *YL registers) are defined in terms of display lines in each field. When the VENC is in progressive mode, window vertical position and height (*YP and *YL) registers are defined in terms of display lines in the progressive frame. Table 21 shows the register used for window position and size.

Figure 27. OSD Window Positioning

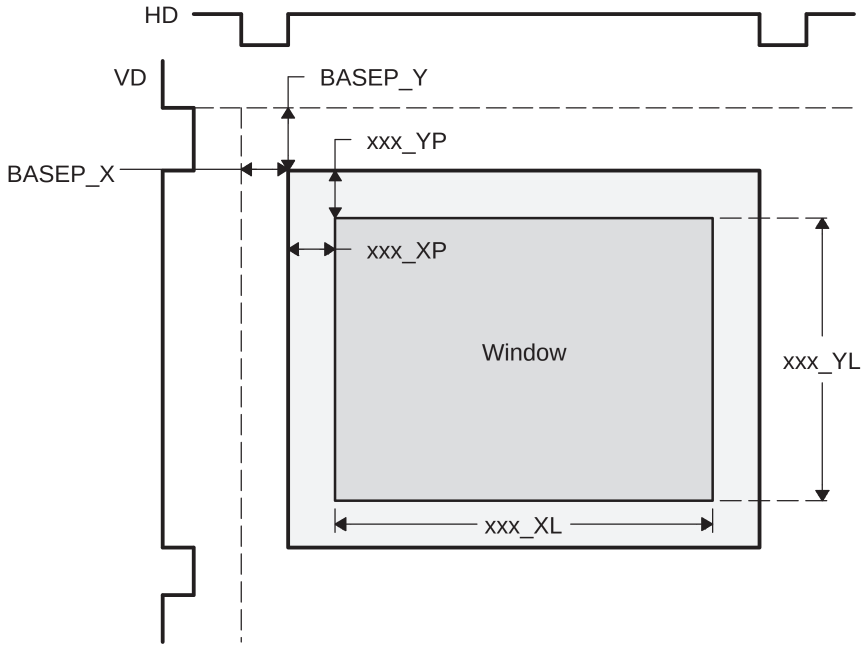


Table 21. OSD Window Positioning Registers

Window Positioning Registers	Window
VIDWIN0XP VIDWIN0YP VIDWIN0XL VIDWIN0YL	Video Window 0 start position and size registers
VIDWIN1XP VIDWIN1YP VIDWIN1XL VIDWIN1YL	Video Window 1 start position and size registers
OSDWIN0XP OSDWIN0YP OSDWIN0XL OSDWIN0XL	OSD Bitmap Window 0 start position and size registers
OSDWIN1XP OSDWIN1YP OSDWIN1XL OSDWIN1XL	OSD Bitmap Window 1/Attribute Window start position and size registers
CURXP CURYP CURYP CURYL	Hardware cursor start position and size registers

4.3.2.4 Window Mode – Field/Frame

Each video and bitmap window has two display modes: field mode and frame mode (VIDWINMD.VFF*n*, OSDWINnMD.OFF*n*). Table 22 shows the registers used for the window modes. The field/frame mode setting describes how the display data is organized in and read from DRAM, as shown in Table 23.

Table 22. OSD Field/Frame Mode Registers

Register.Field	Description
VIDWINMD.VFF0	Video Window 0 Field/Frame specification
VIDWINMD.VFF1	Video Window 1 Field/Frame specification
OSDWIN0MD.OFF0	OSD Bitmap Window 0 Field/Frame specification
OSDWIN1MD.OFF1	OSD Bitmap Window 1 Field/Frame specification
OSDATRMD.OFFA	OSD Attribute Window Field/Frame specification (same address/offset as for OSD Bitmap Window 1)

Table 23. Window Mode Description

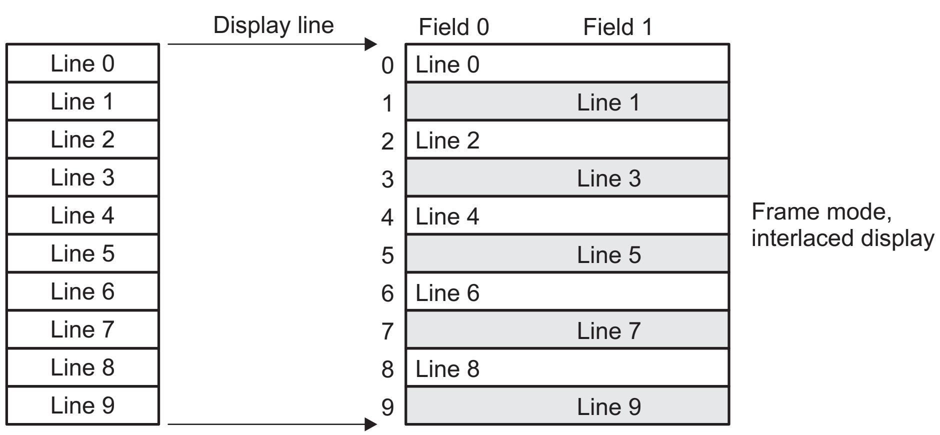
Window Mode	Display Field	Initial Data	Line Increment	VENC Mode	Window Height Register	Display Usage
Frame	Top	Start Address	2 × Offset	Interlaced	Field Height (1/2 display height)	Progressive data to interlaced display device
	Bottom	Start Address + Offset	2 × Offset			
Field		Start Address	Offset	Interlaced	Field Height (1/2 display height)	Field data is line doubled
Field		Start Address	Offset	Interlaced	Field Height (full display height)	Progressive frame to progressive display

4.3.2.4.1 Frame Mode

Frame mode (Figure 28) allows a progressive frame of data (full vertical resolution) stored in DRAM and data is read sequentially, beginning from the start address and skipping every other line by incrementing by 2× the offset each line. The readout for the second field is started at an offset of 1 line from the start address.

If the VENC is in interlaced mode (standard TV out mode), different data is read for each field and the full progressive frame is output on each even/odd field pair. In this case, the window height registers are programmed to the number of lines in each field; that is, the number of lines the VENC reads for each VSYNC (field) = 1/2 the display height.

Figure 28. OSD Window Frame Mode



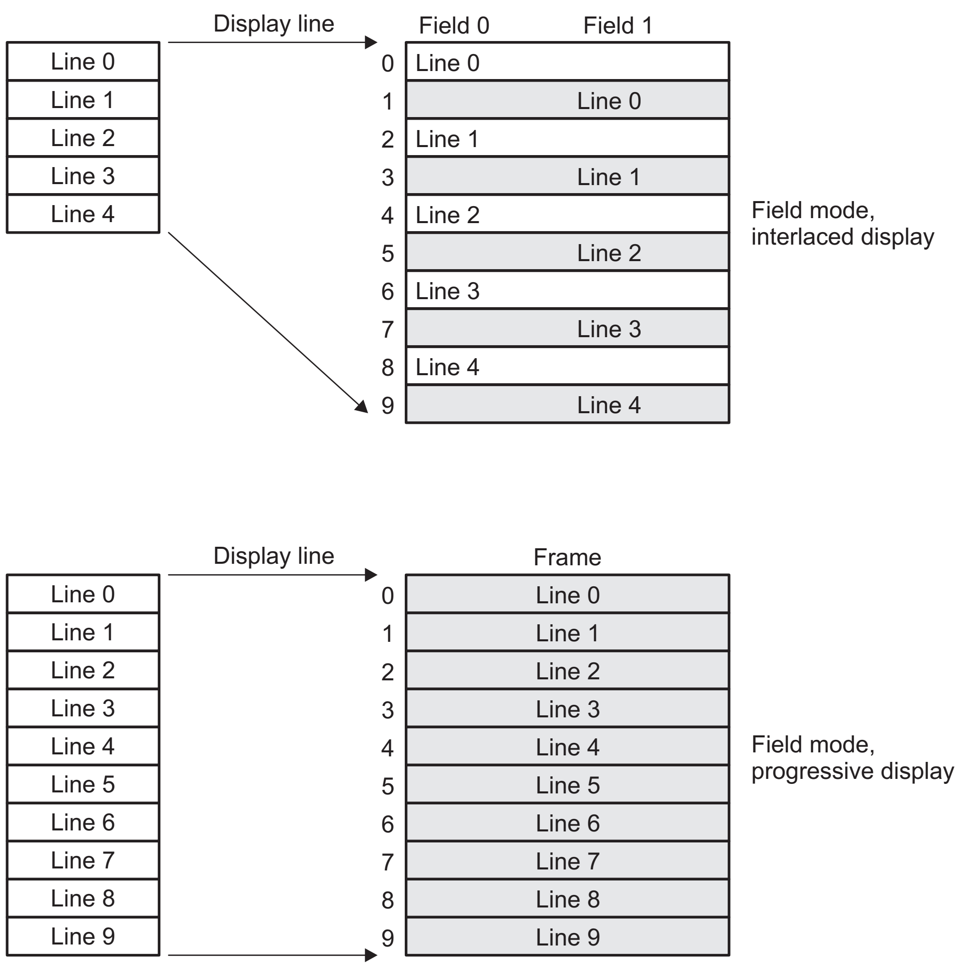
4.3.2.4.2 Field Mode

Field mode (Figure 29) assumes a single display field is stored in DRAM and data lines are read sequentially, beginning from the start address and incrementing by the offset each line and repeating for each field (or frame).

If the VENC is in interlaced mode (standard TV out mode), the same data is read twice for each field. This results in each line being displayed twice, once for each field; that is, line doubled. In this case, the window height registers are programmed to the number of lines in each field; that is, the number of lines the VENC reads for each VSYNC (field) = 1/2 the display height. Alternately, if interlaced video frames are to be displayed, from a video decode operation, the start address can be altered at each VSYNC to ping-pong between the two actual video fields and output the interlaced data to the interlaced display output.

If the VENC is in progressive mode, then field mode should be used so that all data is read from DRAM progressively so that each line is displayed once per progressive frame. In this case, window height registers are programmed to the number of lines in each progressive frame; that is, the number of lines the VENC reads for each VSYNC (frame) = full display height.

Figure 29. OSD Window Field Mode



4.3.2.5 Window Zooming

The video windows and OSD bitmap windows can be zoomed along their horizontal and vertical directions by a factor of 2 or 4. Figure 30 shows the zoom process and the parameters that must be setup to execute a zoom. All of the registers used in the zoom process (Table 24) are latched by the VD signal so they can be safely updated any time.

- Set the starting SDRAM address of the area desired to be magnified, offset, zoom factor and the display window size. The OSD will take data, starting from the start address, to generate a magnified image that fits into the display window.
- Set the display position to the desired position of the window. Set the display height and display width to the desired magnified height and width.
- When zoom is enabled (VIDWINMD.VVRSZ*n*, VIDWINMD.VHRSZ*n*, OSDWIN*n*MD.OVZ*n*, OSDWIN*n*MD.OHZ*n*), SDRAM data starting from the SDRAM start position will be magnified to fit into the display area specified by the display height and display width. For example, if the horizontal and vertical directions are set to 2× zoom and the display width and height are set to 640 × 480, then a 320 × 240 block of data starting from the SDRAM start position will be magnified to 640 × 480 in the display window.

Figure 30. OSD Window Zoom Process

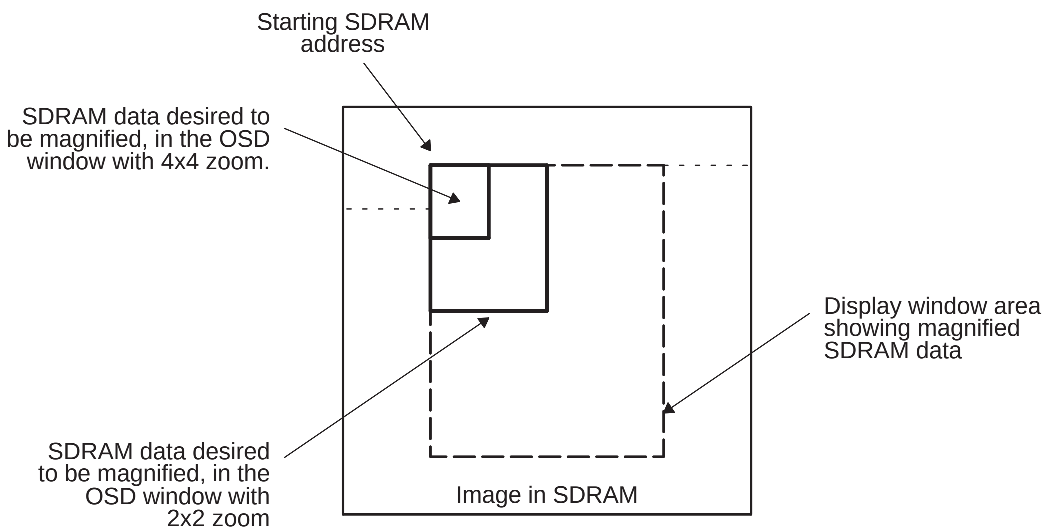


Table 24. OSD Window Zoom Registers

Register.Field	Description
VIDWINMD.VHZ0	Video Window 0 Horizontal Zoom
VIDWINMD.VVZ0	Video Window 0 Vertical Zoom
VIDWINMD.VHZ1	Video Window 1 Horizontal Zoom
VIDWINMD.VVZ1	Video Window 1 Vertical Zoom
OSDWIN0MD.OHZ0	Bitmap Window 0 Horizontal Zoom
OSDWIN0MD.OVZ0	Bitmap Window 0 Vertical Zoom
OSDWIN1MD.OHZ1	Bitmap Window 1 Horizontal Zoom
OSDWIN1MD.OVZ1	Bitmap Window 1 Vertical Zoom

4.3.2.6 Window Expansion – Square Pixels for NTSC/PAL Analog Output

The analog NTSC/PAL output video signals are spatially compressed. As a result, the OSD has an option to horizontally and vertically expand the video and bitmaps windows to counteract the spatial compression in the video signal. In addition, there are options to smooth the expanded video window data. Table 25 shows the registers used for window expansion.

- NTSC analog output is compressed 8/9 horizontally
  - 720 × 480 input appears as 640 × 480 (6:4 aspect ratio source data appears as 4:3)
  - Solution (example) - Use 640 × 480 source material with 9/8 horizontal expansion (MODE.VHRSZ and MODE.OHRSZ) and window display size set to 720 × 480, which will appear as 640 × 480.
- PAL analog output is compressed 8/9 horizontally and 5/6 vertically
  - 720 × 576 input appears as 640 × 480
  - Solution (example) - Use 640 × 480 source material with 9/8 horizontal expansion (MODE.VHRSZ and MODE.OHRSZ) and 6/5 vertical expansion (MODE.VVRSZ and MODE.OVRSZ) and window display size set to 720 × 576, which will appear as 640 × 480.

Table 25. OSD Window Expansion Registers

Register.Field	Description
MODE.VHRSZ	Video Window Horizontal 9/8 Expansion
MODE.VVRSZ	Video Window Vertical 6/5 Expansion
MODE.V0EFC	Video Window 0 smoothing filter enable (with MODE.EF)
MODE.V1EFC	Video Window 1 smoothing filter enable (with MODE.EF)
MODE.EF	Video Window smoothing filter (maximum line width is 720)
MODE.OHRSZ	Video Window Horizontal 9/8 Expansion
MODE.OVRSZ	Video Window Vertical 6/5 Expansion 4.4.1.7

4.3.2.7 OSD Background Color

The background color can be specified in terms of the color look-up tables. This color is displayed in regions of the combined OSD display area that do not have an overlapping window. Table 26 shows the registers used for OSD background color.

Table 26. OSD Background Color Registers

Register.Field	Description
MODE.BCLUT	Selects the color look-up table to be used (ROM or RAM). Note that there are two ROM tables and the selection for the other windows also applies here (MISCCTL.RSEL).
MODE.CABG	Background color. 8-bit offset into color look-up table.

4.3.3 Video Windows

The two video windows (VIDWIN0 and VIDWIN1) can be displayed simultaneously. Data referenced by each video window is read from external memory and displayed within the two windows.

Note: Video window 1 (VIDWIN1) and all OSD bitmap windows and the cursor window must be fully contained inside of video window 0 (VIDWIN0).

Video window 0 is, therefore, typically the canvas on which the GUI is built, with the other windows serving as storage for graphics/test overlays, picture-in-picture overlay via VIDWIN1, etc. The primary data format accepted by the video windows is YUV 4:2:2 interleaved data as described below. This is the data format output by the VPFE preview engine image signal processor (ISP) and resizer modules. Typically, the video/image decoders produce this output and the encoders accept this input format as well. In addition, one of the video windows can be configured to accept 24-bit RGB888 bit data, if required.

OSD window data is always packed into 32-bit words and left justified. Starting from the upper left corner of the OSD window, all data will be packed into adjacent 32-bit words. Figure 31 shows data format window data in SDRAM.

Figure 31. Pixel Arrangement in the Display

Left, Top

P0	P1	P2	P3	P4	P5	P6	P7 ...

4.3.3.1 Video Window Data – YUV422 Format

OSD video window data is in YCbCr 4:2:2 format. Other formats, for example, 4:2:0 and 4:4:4 interleaved data formats are not supported. Note that the order of the Cb and Cr data is dependent on MODE.CS (chroma swap). Figure 32 describes the default case of Cb/Cr order.

Note that since each horizontal line of window data must be a multiple of 32 bytes, video window data must contain a multiple of 32 bytes/2 bytes/pixel = 16 pixels per horizontal line.

Figure 32. Video Data Format – YUV422

(a) 16-bits per pixel, 32-bit pixel pair with combined Chroma

31 – 24	23 – 16	15 – 8	7 – 0
Y1	Cr0	Y0	Cb0

P_{n+1} (bits 31–16), P_n (bits 15–0)

(b) SDRAM format

Address	31 – 16	15 – 0
N	P1	P0
N + 1	P3	P2
N + 2	P5	P4
...	...	...

4.3.3.2 Video Window Data – RGB888 Format

OSD video windows also support display of 24-bit RGB source data or RGB888 format. This data is internally converted to YUV422 prior to entering the OSD module for blending. The RGB data from external memory is converted into YCbCr data within the OSD module using the following equations to calculate YCrCb:

$$Y = (0.2990 \times R) + (0.5870 \times G) + (0.1140 \times B)$$

$$Cb = (-0.1687 \times R) - (0.3313 \times G) + (0.5000 \times B) + 128$$

$$Cr = (0.5000 \times R) - (0.4187 \times G) - (0.0813 \times B) + 128$$

Note that only one video window at a time can be configured to accept RGB888 data, as shown by the control registers listed in Table 27.

Table 27. RGB888 Control Registers

Control Register.Field	Description
MISCCTL.RGBWIN	Defines which video window data is RGB888 format.
MISCCTL.RGBEN	Enable RGB888 → YUV422 conversion of the selected video window data.

The 24-bit RGB888 data is stored packed in DDR2, with 4 pixels stored in three 32-bit words. Within each 24-bit element, the red (R) byte value is in the least significant byte, followed by the green (G) byte, then the blue (B) byte, as shown in Figure 33.

Note that since each horizontal line of window data must be both a multiple of 32-bytes and an integer number of pixels, RGB888 windows must contain a multiple of 32-bytes/3-bytes/pixel × 3 = 32-pixels per horizontal line.

Figure 33. Video Data Format – RGB888

(a) 3 bytes per pixel at 32-bit intervals

31 – 24	23 – 16	15 – 8	7 – 0	
R1	B0	G0	R0	P_n
G2	R2	B1	G1	P_{n+1}
B3	G3	R3	B2	P_{n+2}

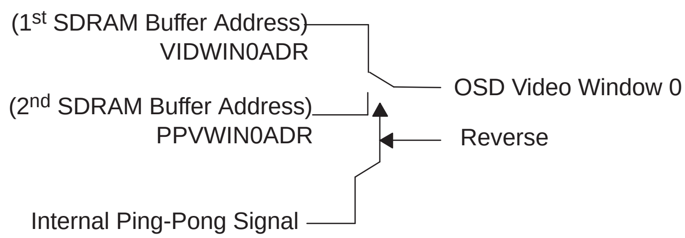
(b) SDRAM format

Address	**31**	**16**	**15**	**0**
N	P1 [R]	P0 [B:G:R]		
N + 1	P2 [G:R]		P1 [B:G]	
N + 2	P3 [B:G:R]			P2 [B]
...	...			

4.3.4 Video Window Ping-Pong Display Switching

The main video window (video window 0) supports ping-pong buffers to quickly change the SDRAM data address pointer. Initially, the SDRAM source address for video window 0 can be set to the SDRAM address specified in VIDWIN0ADR and, when the ping-pong buffer toggle bit is cleared, the SDRAM source address switches to the address specified in PPVWIN0ADR register. Ping-pong buffer switching is done by configuring MISCCTL.PPSW. The sense of the ping-pong switch (which address is selected when PPSW = 1) can be reversed by setting the ping-pong reverse option, MISCCTL.PPRV. The buffer switching is illustrated Figure 34.

Figure 34. Ping-Pong Buffers for the Main Video Window 0



4.3.5 Bitmap Windows

Two bitmap windows (OSDWIN0 and OSDWIN1) can be displayed simultaneously. Data referenced by each bitmap window is read from external memory and displayed within the two windows.

Bitmap windows allow you to display graphics and icons on the display unit. The bitmap window uses a color look-up table (CLUT), either in ROM or RAM, to determine the actual display color for a given bitmap pixel value. A total of 256 CLUT entries, in 24-bit YUV color space are available. The maximum width of a bitmap pixel is 8 bits. However, 1-bit, 2-bit, and 4-bit bitmap color depths are also supported.

Bitmap window 1 can be defined as an attribute window, whose data pixels modify the display attributes of the underlying bitmap window 0.

In addition to displaying bitmap data, the OSD bitmap windows indirectly supports displaying 16-bit RGB565 data; that is, each R and B pixel is 5 bits and the G pixel is 6 bits. The RGB data from external memory is converted into YCbCr data within the OSD module using the following equations to calculate YCrCb:

$$Y = (0.2990 \times R) + (0.5870 \times G) + (0.1140 \times B)$$

$$Cb = (-0.1687 \times R) - (0.3313 \times G) + (0.5000 \times B) + 128$$

$$Cr = (0.5000 \times R) - (0.4187 \times G) - (0.0813 \times B) + 128$$

4.3.5.1 Color Look-Up Tables

There are three possible color look-up tables (CLUTs). Two of these are fixed-ROM CLUTs and one is a user-configurable RAM CLUT. Each of the windows uses either the RAM or ROM CLUT and you must select which of the two ROM CLUTs to use for all OSD options that use the ROM CLUT (MISCCTL.RSEL). Table 28 shows the registers used for the color look-up tables.

In addition to the bitmap windows, the overall OSD background color (the color displayed in areas where no windows are displayed) is set to a specific CLUT entry and the cursor color is selected from one of the CLUT tables/values.

The RAM CLUT must be initialized before it can be used. To setup the OSD RAM CLUT, the following steps are required:

1. Wait for the CPBSY bit of the MISCCTL register to be cleared to 0.
2. Write the luma and chroma Cb values into the CLUTRAMYCB register.
3. Write the chroma Cr value and the CLUT address into the CLUTRAMCR register. The address is the offset address into the CLUT RAM table for the Y, Cb and Cr values.
4. Repeat the previous steps until the RAM table is loaded completely.

Table 28. OSD Color Look-Up Table Registers

	Register.Field	Description
ROM color look-up table selection	MISCCTL.RSEL	Selects the ROM color look-up table to use for all options that select the ROM table
Background color selection	MODE.BCLUT	Background CLUT selection (ROM or RAM)
	MODE.CABG	Background CLUT selection (offset into 256-bit table)
Cursor CLUT selection	RECTCUR.CLUTSR	Cursor CLUT selection (ROM or RAM)
	RECTCUR.RCAD	Rectangular Cursor color address within CLUT (offset into 256-bit table)
Bitmap window CLUT selections	OSDWIN0MD.CLUTS0	Window 0 CLUT selection (ROM or RAM)
	OSDWIN1MD.CLUTS1	Window 1 CLUT selection (ROM or RAM)
RAM CLUT Setup/Write	CLUTRAMYCB.Y	CLUTRAM Y (luma) value
	CLUTRAMYCB.CB	CLUTRAM CB (chroma) value
	CLUTRAMCR.CR	CLUTRAM CR (chroma) value
	CLUTRAMCR.CADDR	CLUTRAM address offset (writes all values)
	MISCCTL.CPBUSY	Indicates if busy when writing to CLUT RAM

The RGB equivalent CLUT values are shown in Table 31 as converted with the inverse of the OSD's RGB-to-YUV conversion matrix for RGB888 and RGB565 window data shown below.

$$R = (1.00000 \times Y) + (0.00000 \times (Cb - 128)) + (1.40200 \times (Cr - 128))$$

$$G = (1.00000 \times Y) - (0.34414 \times (Cb - 128)) - (0.71444 \times (Cr - 128))$$

$$B = (1.00000 \times Y) + (1.72200 \times (Cb - 128)) + (0.00000 \times (Cr - 128))$$

Note, however, that the default YUV-to-RGB conversion matrix values in the VENC module shown below are different and thus the output colors may not exactly match those shown here.

$$R = (1.00000 \times Y) + (0.00000 \times (Cb - 128)) + (1.37110 \times (Cr - 128))$$

$$G = (1.00000 \times Y) - (0.33690 \times (Cb - 128)) - (0.69820 \times (Cr - 128))$$

$$B = (1.00000 \times Y) + (1.73240 \times (Cb - 128)) + (0.00000 \times (Cr - 128))$$

The YUV output of each bitmap window can be attenuated to reduce the dynamic range of the YUV signals (see Table 29). Luma values are attenuated to a range between 16-235 and chroma values are attenuated to a range between 16-240.

Note: Attenuation is automatically disabled when OSDWIN1 is used as an attribute window.

Table 29. OSD Bitmap Window YUV Output Attenuation Registers

Register.Field	Description
OSDWIN0MD.ATN0E	Enable YUV attenuation for Bitmap Window 0
OSDWIN1MD.ATN1E	Enable YUV attenuation for Bitmap Window 1

4.3.5.1.1 ROM0 Color Look-Up Tables

Table 30. ROM0 Color Look-Up Table (YUV Values)

ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value
0	00 80 80	32	59 71 A2	64	72 1E F5	96	D2 08 95	128	63 46 46	160	3F 93 72	192	52 D3 4F	224	54 A7 76
1	26 5A DA	33	6E 6C AE	65	5B 6F 88	97	92 1F 93	129	17 71 71	161	26 93 72	193	8A 9B 71	225	AE 87 7F
2	4B 35 35	34	66 6C AE	66	18 68 89	98	B7 00 9F	130	4D 4B 4B	162	51 E4 37	194	48 9B 71	226	9D 88 7F
3	71 0F 8F	35	60 6A B4	67	49 4F 91	99	BD 00 A1	131	1B 6D 6D	163	58 EE 30	195	43 D1 55	227	6C 87 7F
4	0F F1 71	36	68 62 C5	68	41 4F 91	100	B5 00 A1	132	3B 55 55	164	EE 89 79	196	4A EB 46	228	64 87 7F
5	35 CB CB	37	40 40 FF	69	30 60 89	101	C4 00 A3	133	29 6F 67	165	DB 94 73	197	4A EB 46	229	53 87 7F
6	5A A6 26	38	53 5E C1	70	6E 1A 9E	102	D2 00 A5	134	8A 82 7A	166	D1 9E 6C	198	3B E1 4D	230	5B 88 7F
7	C0 80 80	39	2D 5B C6	71	50 59 8A	103	CA 10 94	135	48 82 7A	167	B9 9D 6C	199	BB 9B 72	231	4B 87 7F
8	D0 70 70	40	48 40 F5	72	48 59 8A	104	A8 32 64	136	2F 82 7A	168	A8 9E 6C	200	58 9B 72	232	43 87 7F
9	C4 AC 62	41	65 65 AF	73	77 32 95	105	AD 3E 67	137	27 82 7A	169	28 89 79	201	50 9B 72	233	6D 8E 7E
10	FB 80 80	42	4C 65 AF	74	6E 2A 96	106	A5 2D 5F	138	1E 83 7A	170	96 A7 65	202	37 9B 72	234	65 8E 7E
11	08 80 80	43	51 47 E4	75	5E 32 95	107	A6 34 5E	139	5F 8C 73	171	6E 9E 6C	203	47 AC 6A	235	22 87 7F
12	10 80 80	44	23 65 AF	76	27 59 8A	108	9A 30 59	140	8E C0 3C	172	86 A7 65	204	5E C7 5B	236	4D 96 7D
13	18 80 80	45	3B 4D D9	77	46 3A 94	109	8F 33 54	141	9B CC 2F	173	A5 B1 5F	205	E6 91 78	237	19 88 7F
14	21 80 80	46	43 45 EA	78	BE 04 A0	110	8C 2D 4E	142	BC A2 60	174	95 B1 5E	206	83 91 78	238	11 87 7F
15	29 80 80	47	1D 63 B5	79	35 4B 8D	111	84 2D 4E	143	81 DD 28	175	8C B1 5F	207	58 AC 6A	239	45 85 85
16	31 80 80	48	8B 68 AA	80	76 43 8E	112	88 29 4A	144	A8 B6 53	176	65 A7 65	208	59 A2 71	240	1C 85 85
17	4A 80 80	49	5A 4F D3	81	BE 1C 98	113	7D 24 45	145	98 B6 53	177	74 B1 5E	209	59 A2 71	241	74 87 90
18	5A 80 80	50	5D 3B F1	82	55 43 8E	114	72 50 60	146	78 D6 39	178	9A C4 51	210	51 A2 71	242	50 82 8A
19	73 80 80	51	18 68 AA	83	9C 0D 99	115	22 66 6E	147	74 E2 2D	179	62 EC 36	211	49 A2 70	243	58 82 8B
20	7B 80 80	52	45 53 C7	84	7C 1C 98	116	72 26 3F	148	62 EC 26	180	69 CC 50	212	41 A2 70	244	73 80 91
21	94 80 80	53	53 2D FF	85	B2 00 A4	117	6A 26 3F	149	C7 A0 66	181	7F AE 64	213	1F B3 69	245	00 80 80
22	A5 80 80	54	7F 5B B6	86	8A 06 9B	118	5E 5B 64	150	9C AA 5F	182	85 B8 5E	214	1F C4 61	246	FB 75 84
23	BD 80 80	55	2D 5B B6	87	AA 00 A4	119	9C 57 5F	151	5C EA 2C	183	74 B9 5E	215	B5 91 78	247	A0 84 80
24	44 7E 86	56	33 5D B0	88	B0 00 A6	120	73 2E 3E	152	AD A9 5F	184	5E AE 64	216	94 91 78	248	80 80 80
25	70 7B 8B	57	7B 4F C2	89	C4 06 9A	121	63 35 3E	153	AB B3 59	185	61 DC 48	217	7B 91 78	249	4C 34 FF
26	68 7B 8B	58	71 40 D5	90	B2 00 9C	122	2E 7B 7B	154	9B B3 58	186	B1 A5 6B	218	39 91 78	250	96 00 00
27	57 7B 8C	59	65 23 F9	91	BA 00 9C	123	31 67 67	155	A1 BD 52	187	A1 A5 6B	219	31 91 78	251	E2 00 9D
28	85 76 97	60	5F 21 FF	92	C1 00 9D	124	54 55 55	156	65 F1 2B	188	90 A5 6B	220	28 BB 68	252	1D FF 63
29	6D 76 97	61	2E 62 A4	93	B0 00 9E	125	78 41 41	157	C3 93 72	189	80 A5 6B	221	18 AA 70	253	69 FF FF
30	64 76 97	62	25 63 A5	94	98 00 9D	126	70 41 41	158	A2 93 72	190	46 A5 6B	222	63 98 77	254	B3 CC 00
31	5E 74 9D	63	6B 25 F3	95	3D 43 8D	127	4C 55 55	159	60 93 72	191	4C C0 5D	223	52 99 78	255	FF 80 80

Table 31. ROM0 Color Look-Up Table (Equivalent RGB Values)

ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value
0	00 00 00	32	7B 4A 4A	64	E7 4A 10	96	E7 DE 5A	128	29 8C 29	160	31 42 52	192	21 5A A5	224	4A 52 7B
1	80 00 00	33	9C 5A 5A	65	63 5A 4A	97	A5 9C 31	129	08 21 08	161	18 29 39	193	7B 8C A5	225	AD AD B5
2	00 80 00	34	94 52 52	66	21 18 00	98	D6 C6 18	130	18 73 18	162	08 63 B5	194	39 4A 63	226	9C 9C A5
3	80 80 00	35	94 4A 4A	67	5A 4A 18	99	DE CE 10	131	08 29 08	163	08 6B C6	195	18 4A 94	227	6B 6B 73
4	00 00 80	36	AD 4A 4A	68	52 42 10	100	D6 C6 08	132	10 5A 10	164	E7 EF F7	196	10 52 B5	228	63 63 6B
5	80 00 80	37	C6 08 00	69	39 31 10	101	E7 D6 08	133	10 39 18	165	CE DE EF	197	08 39 84	229	52 52 5A
6	00 80 80	38	94 39 31	70	8C 73 08	102	F7 E7 08	134	84 8C 8C	166	BD D6 EF	198	08 42 9C	230	5A 5A 63
7	C0 C0 C0	39	73 10 08	71	5A 52 29	103	DE D6 5A	135	42 4A 4A	167	A5 BD D6	199	AD BD D6	231	4A 4A 52
8	C0 DC C0	40	BD 18 08	72	52 4A 21	104	8C C6 5A	136	29 31 31	168	94 AD C6	200	4A 5A 73	232	42 42 4A
9	A6 CA F0	41	94 52 4A	73	8C 7B 29	105	94 C6 6B	137	21 29 29	169	21 29 31	201	42 52 6B	233	6B 6B 7B
10	FB FB FB	42	7B 39 31	74	84 73 18	106	84 C6 52	138	18 21 21	170	7B 9C BD	202	29 39 52	234	63 63 73
11	08 08 08	43	B5 29 18	75	73 63 10	107	84 C6 5A	139	52 63 6B	171	5A 73 8C	203	31 4A 73	235	21 21 29
12	10 10 10	44	52 10 08	76	31 29 00	108	73 BD 4A	140	4A A5 CE	172	6B 8C AD	204	39 63 A5	236	4A 4A 63
13	18 18 18	45	94 18 08	77	5A 4A 00	109	63 B5 42	141	4A B5 E7	173	84 AD D6	205	DE E7 F7	237	18 18 21
14	21 21 21	46	AD 18 08	78	DE C6 42	110	5A B5 39	142	9C C6 DE	174	73 9C C6	206	7B 84 94	238	10 10 18
15	29 29 29	47	52 08 00	79	42 39 00	111	52 AD 31	143	29 9C DE	175	6B 94 BD	207	42 5A 84	239	4A 42 4A
16	31 31 31	48	B5 7B 73	80	84 7B 39	112	52 B5 31	144	7B B5 DE	176	4A 6B 8C	208	4A 5A 7B	240	21 18 21
17	4A 4A 4A	49	AD 39 29	81	D6 C6 5A	113	42 AD 21	145	6B A5 CE	177	52 7B A5	209	21 29 39	241	84 6B 7B
18	5A 5A 5A	50	CE 31 18	82	63 5A 18	114	52 8C 42	146	31 8C CE	178	6B A5 DE	210	42 52 73	242	5A 4A 52
19	73 73 73	51	42 08 00	83	B5 A5 29	115	10 31 08	147	21 8C D6	179	18 73 CE	211	39 4A 6B	243	63 52 5A
20	7B 7B 7B	52	8C 29 18	84	94 84 18	116	31 A5 18	148	08 7B CE	180	39 73 B5	212	31 42 63	244	84 6B 73
21	94 94 94	53	D6 21 00	85	D6 BD 18	117	29 9C 10	149	AD CE E7	181	63 84 AD	213	08 21 52	245	00 00 00
22	A5 A5 A5	54	B5 6B 5A	86	A5 94 10	118	42 73 39	150	7B A5 C6	182	63 8C BD	214	00 21 63	246	FF FB F0
23	BD BD BD	55	63 18 08	87	CE B5 10	119	7B B5 73	151	08 73 C6	183	52 7B AD	215	AD B5 C6	247	A0 A0 A4
24	4A 42 42	56	63 21 10	88	D6 BD 08	120	31 A5 21	152	8C B5 D6	184	42 63 8C	216	8C 94 A5	248	80 80 80
25	7B 6B 6B	57	BD 63 4A	89	DE CE 4A	121	21 94 18	153	84 B5 DE	185	29 6B BD	217	73 7B 8C	249	FF 00 00
26	73 63 63	58	C6 52 31	90	CE BD 31	122	29 31 29	154	73 A5 CE	186	9C B5 D6	218	31 39 4A	250	00 FF 00
27	63 52 52	59	DE 39 08	91	D6 C6 31	123	18 42 18	155	73 AD DE	187	8C A5 C6	219	29 31 42	251	FF FF 00
28	9C 7B 7B	60	DE 31 00	92	DE CE 31	124	29 73 29	156	10 7B D6	188	7B 94 B5	220	10 29 63	252	00 00 FF
29	84 63 63	61	52 21 10	93	CE BD 21	125	39 A5 39	157	B5 C6 D6	189	6B 84 A5	221	08 18 42	253	FF 00 FF
30	7B 5A 5A	62	4A 18 08	94	B5 A5 08	126	31 9C 31	158	94 A5 B5	190	31 4A 6B	222	5A 63 7B	254	00 FF FF
31	7B 52 52	63	DE 42 10	95	4A 42 00	127	21 6B 21	159	52 63 73	191	29 52 8C	223	4A 52 6B	255	FF FF FF

Table 32. ROM0 Color Look-Up Table (Equivalent RGB)

ndx	color	ndx	color	ndx	color	ndx	color	ndx	color	ndx	Color	ndx	color	ndx	color
0		224		64		96		128		160		192		224	
1		225		65		97		129		161		193		225	
2		226		66		98		130		162		194		226	
3		227		67		99		131		163		195		227	
4		228		68		100		132		164		196		228	
5		229		69		101		133		165		197		229	
6		230		70		102		134		166		198		230	
7		231		71		103		135		167		199		231	
8		232		72		104		136		168		200		232	
9		233		73		105		137		169		201		233	
10		234		74		106		138		170		202		234	
11		235		75		107		139		171		203		235	
12		236		76		108		140		172		204		236	
13		237		77		109		141		173		205		237	
14		238		78		110		142		174		206		238	
15		239		79		111		143		175		207		239	
16		240		80		112		144		176		208		240	
17		241		81		113		145		177		209		241	
18		242		82		114		146		178		210		242	
19		243		83		115		147		179		211		243	
20		244		84		116		148		180		212		244	
21		245		85		117		149		181		213		245	
22		246		86		118		150		182		214		246	
23		247		87		119		151		183		215		247	
24		248		88		120		152		184		216		248	
25		249		89		121		153		185		217		249	
26		250		90		122		154		186		218		250	
27		251		91		123		155		187		219		251	
28		252		92		124		156		188		220		252	
29		253		93		125		157		189		221		253	
30		254		94		126		158		190		222		254	
31		255		95		127		159		191		223		255	

4.3.5.1.2 ROM1 Color Look-Up Tables

Table 33. ROM1 Color Look-Up Table (YUV Values)

ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value
0	FF 80 80	32	5E A1 F3	64	61 66 CC	96	69 D5 A2	128	6C 9A 7C	160	6F 5E 55	192	77 CD 2B	224	05 7D 88
1	F9 66 84	33	58 88 F7	65	5B 4D D1	97	63 BB A7	129	66 80 80	161	69 45 59	193	71 B3 2F	225	8C 31 1C
2	F3 4D 88	34	52 6E FB	66	5A DD D1	98	5D A2 AB	130	60 66 84	162	68 D5 5A	194	6B 9A 34	226	82 37 23
3	EE 34 8C	35	4C 55 FF	67	54 C4 D5	99	57 88 AF	131	5A 4D 88	163	62 BC 5E	195	65 80 38	227	6E 42 32
4	E8 1A 91	36	F0 89 66	68	4E AA DA	100	51 6F B3	132	5A DD 89	164	5D A2 62	196	60 67 3C	228	64 48 39
5	E2 00 95	37	EA 6F 6B	69	49 91 DE	101	4C 55 B7	133	54 C4 8D	165	57 89 66	197	5A 4D 40	229	50 53 47
6	E1 91 95	38	E4 56 6F	70	43 77 E2	102	4B E6 B8	134	4E AA 91	166	51 6F 6B	198	59 DE 41	230	46 59 4E
7	DB 77 9A	39	DE 3C 73	71	3D 5E E6	103	45 CC BC	135	48 91 95	167	4B 56 6F	199	53 C4 45	231	32 64 5C
8	D5 5E 9E	40	D8 23 77	72	E1 91 4D	104	3F B3 C0	136	42 77 9A	168	4A E6 6F	200	4D AB 49	232	28 69 64
9	D0 44 A2	41	D3 09 7B	73	DB 78 51	105	39 99 C4	137	3C 5E 9E	169	44 CC 74	201	48 91 4D	233	14 75 72
10	CA 2B A6	42	D2 9A 7C	74	D5 5E 55	106	34 80 C8	138	3C EE 9E	170	3F B3 78	202	42 78 51	234	0A 7A 79
11	C4 11 AA	43	CC 80 80	75	CF 45 59	107	34 80 C8	139	36 D5 A2	171	39 9A 7C	203	3C 5E 55	235	1B F7 6D
12	C3 A2 AB	44	C6 66 84	76	C9 2B 5E	108	D1 9A 34	140	30 BB A7	172	33 80 80	204	3B EF 56	236	19 EE 6E
13	BD 88 AF	45	C0 4D 88	77	C3 12 62	109	CB 80 38	141	2A A2 AB	173	2D 66 84	205	35 D5 5A	237	15 DE 71
14	B7 6F B3	46	BB 34 8C	78	C3 A2 62	110	C6 67 3C	142	24 88 AF	174	2C F7 85	206	2F BC 5E	238	13 D5 72
15	B2 55 B7	47	B5 1A 91	79	BD 89 66	111	C0 4D 40	143	1E 6F B3	175	27 DD 89	207	2A A2 62	239	10 C4 75
16	AC 3C BB	48	B4 AA 91	80	B7 6F 6B	112	BA 34 44	144	C2 A2 1A	176	21 C4 8D	208	24 89 66	240	0E BC 76
17	A6 22 BF	49	AE 91 95	81	B1 56 6F	113	B4 1A 48	145	BC 89 1E	177	1B AA 91	209	1E 6F 6B	241	0A AA 79
18	A5 B3 C0	50	A8 77 9A	82	AB 3C 73	114	B3 AB 49	146	B6 6F 22	178	15 91 95	210	1D FF 6B	242	08 A2 7A
19	9F 99 C4	51	A2 5E 9E	83	A5 23 77	115	AE 91 4D	147	B1 56 26	179	0F 77 9A	211	17 E6 6F	243	04 91 7D
20	9A 80 C8	52	9D 44 A2	84	A5 B3 78	116	A8 78 51	148	AB 3C 2B	180	B3 AB 00	212	11 CC 74	244	02 88 7F
21	94 66 CC	53	97 2B A6	85	9F 9A 7C	117	A2 5E 55	149	A5 23 2F	181	AD 92 05	213	0C B3 78	245	EE 80 80
22	8E 4D D1	54	96 BB A7	86	99 80 80	118	9C 45 59	150	A4 B3 2F	182	A7 78 09	214	06 9A 7C	246	DD 80 80
23	88 33 D5	55	90 A2 AB	87	93 66 84	119	96 2B 5E	151	9E 9A 34	183	A1 5F 0D	215	47 58 F7	247	BB 80 80
24	87 C4 D5	56	8A 88 AF	88	8D 4D 88	120	95 BC 5E	152	98 80 38	184	9B 45 11	216	42 5B EE	248	AA 80 80
25	81 AA DA	57	84 6F B3	89	88 34 8C	121	90 A2 62	153	93 67 3C	185	96 2C 15	217	38 60 DE	249	88 80 80
26	7C 91 DE	58	7F 55 B7	90	87 C4 8D	122	8A 89 66	154	8D 4D 40	186	95 BC 16	218	33 63 D5	250	77 80 80
27	76 77 E2	59	79 3C BB	91	81 AA 91	123	84 6F 6B	155	87 34 44	187	8F A2 1A	219	29 69 C4	251	55 80 80
28	70 5E E6	60	78 CC BC	92	7B 91 95	124	7E 56 6F	156	87 34 44	188	89 89 1E	220	24 6C BC	252	44 80 80
29	6A 44 EA	61	72 B3 C0	93	75 77 9A	125	78 3C 73	157	80 AB 49	189	83 6F 22	221	19 72 AA	253	22 80 80
30	69 D4 EB	62	6C 99 C4	94	6F 5E 9E	126	77 CC 74	158	7B 91 4D	190	7E 56 26	222	14 75 A2	254	11 80 80
31	64 BB EF	63	67 80 C8	95	6F 5E 9E	127	72 B3 78	159	75 78 51	191	78 3C 2B	223	0A 7A 91	255	00 80 80

Table 34. ROM1 Color Look-Up Table (Equivalent RGB Values)

ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value	ndx	value
0	FF FF FF	32	FF 00 98	64	CB 33 32	96	98 33 FF	128	66 65 9A	160	32 99 32	192	00 99 FF	224	10 00 00
1	FE FF CA	33	FE 00 66	65	CC 32 00	97	99 32 CB	129	66 66 66	161	32 99 00	193	00 99 CB	225	00 EE 00
2	FE FE 98	34	FE 00 32	66	CB 00 FE	98	99 32 99	130	65 66 31	162	32 65 FE	194	00 98 99	226	00 DD 00
3	FE FF 67	35	FE 00 00	67	CB 00 CC	99	98 32 65	131	65 65 00	163	32 65 CC	195	00 98 65	227	00 BB 00
4	FF FE 33	36	CB FF FF	68	CC 00 98	100	98 32 32	132	66 33 FE	164	32 66 99	196	00 99 33	228	00 A9 00
5	FF FF 00	37	CC FE CB	69	CC 00 67	101	99 33 00	133	66 33 CC	165	32 66 66	197	00 99 00	229	00 88 00
6	FE CC FF	38	CC FE 99	70	CC 00 33	102	99 00 FF	134	65 33 98	166	33 65 32	198	00 65 FF	230	00 77 00
7	FF CB CB	39	CB FE 65	71	CC 00 00	103	99 00 CB	135	65 33 66	167	33 65 00	199	00 65 CB	231	00 55 00
8	FF CB 98	40	CB FE 33	72	99 FF FF	104	98 00 99	136	66 32 32	168	32 33 FE	200	00 65 99	232	00 43 00
9	FF CC 65	41	CB FF 00	73	99 FF CC	105	98 00 65	137	66 32 00	169	33 32 CA	201	00 66 66	233	00 21 00
10	FF CC 33	42	CC CB FF	74	98 FF 98	106	98 00 34	138	66 00 FE	170	33 33 99	202	00 66 33	234	00 11 00
11	FE CC 00	43	CC CC CC	75	98 FF 66	107	98 00 00	139	65 00 CC	171	33 32 67	203	00 66 00	235	00 00 ED
12	FF 98 FF	44	CB CC 97	76	99 FE 32	108	66 FE FF	140	66 00 98	172	33 33 33	204	00 32 FF	236	00 00 DB
13	FE 98 CB	45	CB CB 65	77	98 FE 00	109	66 FE CB	141	66 00 66	173	32 33 00	205	00 32 CB	237	00 00 BB
14	FE 98 98	46	CB CC 34	78	98 CC FF	110	66 FF 99	142	65 00 32	174	33 00 FE	206	00 32 99	238	00 00 A9
15	FF 99 65	47	CC CB 00	79	98 CC CC	111	66 FF 65	143	65 00 00	175	33 00 CB	207	00 33 66	239	00 00 88
16	FE 99 33	48	CB 99 FE	80	99 CB 98	112	65 FF 33	144	32 FF FE	176	33 00 99	208	00 33 33	240	00 00 78
17	FE 99 00	49	CB 99 CC	81	99 CB 66	113	65 FF 00	145	32 FE CB	177	32 00 65	209	00 32 00	241	00 00 54
18	FE 65 FF	50	CC 98 98	82	98 CB 32	114	65 CB FF	146	32 FE 97	178	32 00 33	210	00 00 FE	242	00 00 44
19	FE 65 CB	51	CC 98 65	83	98 CB 00	115	66 CC CC	147	32 FF 66	179	33 00 00	211	00 00 CB	243	00 00 22
20	FE 66 9A	52	CC 99 32	84	99 99 FF	116	66 CC 99	148	33 FF 32	180	00 FF FF	212	00 00 97	244	00 00 10
21	FE 66 65	53	CC 99 00	85	99 98 CD	117	65 CC 65	149	33 FE 00	181	00 FE CC	213	00 00 66	245	EE EE EE
22	FF 65 33	54	CC 65 FE	86	99 99 99	118	65 CC 33	150	32 CC FE	182	00 FE 98	214	00 00 34	246	DD DD DD
23	FF 65 00	55	CC 65 CC	87	98 99 64	119	66 CB 00	151	33 CB CC	183	00 FE 66	215	ED 00 00	247	BB BB BB
24	FE 32 FF	56	CB 65 98	88	98 98 32	120	65 98 FF	152	33 CB 98	184	00 FE 32	216	DC 00 00	248	AA AA AA
25	FF 32 CB	57	CB 65 65	89	98 99 01	121	65 99 CC	153	33 CC 66	185	00 FF 01	217	BB 00 00	249	88 88 88
26	FF 33 9A	58	CC 66 32	90	99 66 FF	122	65 99 99	154	33 CC 32	186	00 CC FF	218	AA 00 00	250	77 77 77
27	FF 33 66	59	CB 66 00	91	98 66 CB	123	66 98 65	155	32 CC 00	187	00 CC CB	219	88 00 00	251	55 55 55
28	FF 32 33	60	CC 32 FE	92	98 66 99	124	66 98 33	156	33 98 FE	188	00 CB 98	220	78 00 00	252	44 44 44
29	FE 32 00	61	CB 32 CC	93	99 65 65	125	65 98 00	157	32 98 CC	189	00 CB 64	221	53 00 00	253	22 22 22
30	FF 00 FD	62	CB 32 98	94	99 65 32	126	66 65 FD	158	33 99 99	190	00 CC 33	222	43 00 00	254	11 11 11
31	FF 00 CC	63	CB 33 67	95	99 66 00	127	66 66 CC	159	33 99 66	191	00 CC 00	223	21 00 00	255	00 00 00

Table 35. ROM1 Color Look-Up Table (Equivalent RGB)

ndx	Color	ndx	color	ndx	color	ndx	color	ndx	color	ndx	color	ndx	color	ndx	color
0		32		64		96		128		160		192		224	
1		33		65		97		129		161		193		225	
2		34		66		98		130		162		194		226	
3		35		67		99		131		163		195		227	
4		36		68		100		132		164		196		228	
5		37		69		101		133		165		197		229	
6		38		70		102		134		166		198		230	
7		39		71		103		135		167		199		231	
8		40		72		104		136		168		200		232	
9		41		73		105		137		169		201		233	
10		42		74		106		138		170		202		234	
11		43		75		107		139		171		203		235	
12		44		76		108		140		172		204		236	
13		45		77		109		141		173		205		237	
14		46		78		110		142		174		206		238	
15		47		79		111		143		175		207		239	
16		48		80		112		144		176		208		240	
17		49		81		113		145		177		209		241	
18		50		82		114		146		178		210		242	
19		51		83		115		147		179		211		243	
20		52		84		116		148		180		212		244	
21		53		85		117		149		181		213		245	
22		54		86		118		150		182		214		246	
23		55		87		119		151		183		215		247	
24		56		88		120		152		184		216		248	
25		57		89		121		153		185		217		249	
26		58		90		122		154		186		218		250	
27		59		91		123		155		187		219		251	
28		60		92		124		156		188		220		252	
29		61		93		125		157		189		221		253	
30		62		94		126		158		190		222		254	
31		63		95		127		159		191		223		255	

4.3.5.2 Bitmap Indexing Into Color Look-Up Tables

When the bitmap color depth is 8 bits (OSDWIN0MD.BMW0, OSDWIN1MD.BMW1), each 8-bit pixel value in SDRAM is a direct index into the color look-up table (CLUT). However, when the bitmap color depth is 1, 2, or 4 bits, the W*n*BMP01-W*n*BMPEF registers must be used to map the pixel values into the color look-up table. Any of the 256 colors in the table can be used. For example, given 1-bit bitmap data, any of the 256 colors in the CLUT can be mapped to bit value 0 and any of the 256 colors can be mapped to bit value 1. This mapping is specified separately for each OSD bitmap window. Table 36 shows the register, which can be used to select the color for a bitmap value.

Table 36. CLUT Mapping for 1-Bit, 2-Bit, or 4-Bit Bitmaps

Register.Field (n = 0 or 1 for OSD Bitmap Window 0 or 1, respectively)	Color Corresponding to Bitmap Value		
	4-Bit Bitmap	2-Bit Bitmap	1-Bit Bitmap
WnBMP01.PAL00	0	0	0
WnBMP01.PAL01	1	-	-
WnBMP23.PAL02	2	-	-
WnBMP23.PAL03	3	-	-
WnBMP45.PAL04	4	-	-
WnBMP45.PAL05	5	1	-
WnBMP67.PAL06	6	-	-
WnBMP67.PAL07	7	-	-
WnBMP89.PAL08	8	-	-
WnBMP89.PAL09	9	-	-
WnBMPAB.PAL10	10	2	-
WnBMPAB.PAL11	11	-	-
WnBMPCD.PAL12	12	-	-
WnBMPCD.PAL13	13	-	-
WnBMPEF.PAL14	14	-	-
WnBMPEF.PAL15	15	3	1

4.3.5.3 Bitmap Window Blending and Transparency

The OSD also supports pixel blending for the bitmap windows only. If blending is enabled, the amount of blending (relative amount of video data versus bitmap data) at each pixel is determined by the blending factor.

The OSD also supports transparency blending mode. When transparency is enabled, only bitmap pixels with a value of 0 (the background color) or RGB16 bitmap pixels whose value matches that of the RGB16 transparent value register will be transparent (or partially transparent) and allow the underlying video pixel to be displayed based on the blending factor. When transparency is enabled, blending only applies to pixels with a value of zero; otherwise, blending is applied to all pixels.

Blending factor and transparency is configured using OSDWIN0MD and OSDWIN1MD registers for OSD bitmap window 0 and 1 respectively. The RGB16 transparent color is configured in the TRANSPVAL register.

Table 37. CLUT Mapping for 1-Bit, 2-Bit ,or 4-Bit Bitmaps

Transparency OSDWINnMD.TEn	Blending Factor OSDWINnMD.BLNDn	OSD Window Contribution	Video Contribution
OFF	0	0	1
	1	1/8	7/8
	2	2/8	6/8
	3	3/8	5/8
	4	4/8	4/8
	5	5/8	3/8
	6	6/8	2/8
	7	1	0
ON		If pixel value is equal to 0:	
	0	0	1
	1	1/8	7/8
	2	2/8	6/8
	3	3/8	5/8
	4	4/8	4/8
	5	5/8	3/8
	6	6/8	2/8
	7	1	0
		If pixel value is not equal to 0:	
	X	1	0

4.3.5.4 Bitmap Window Data Formats

The bitmap data formats are shown in Figure 35. Bitmap data is interpreted in bytes, with the pixels read in order from the most significant portion of the byte. Note that since each horizontal line of window data must be a multiple of 32-bytes:

- 8-bit bitmap windows must contain a multiple of 32 bytes/1 byte/pixel = 32 pixels per horizontal line.
- 4-bit bitmap windows must contain a multiple of 32 bytes/1/2 bytes/pixel = 64 pixels per horizontal line.
- 2-bit bitmap windows must contain a multiple of 32 bytes/1/4 bytes/pixel = 128 pixels per horizontal line.
- 1-bit bitmap windows must contain a multiple of 32 bytes/1/8 bytes/pixel = 256 pixels per horizontal line.

Figure 35. Bitmap Data Formats

8−bits per pixel within 32−bit word

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
P3		P2		P1		P0	

8−bits per pixel SDRAM format

Addr	31 24	23 16	15 8	7 0
N	P3	P2	P1	P0
N+1	P7	P6	P5	P4
N+2	P11	P10	P9	P8

4−bits per pixel within 32−bit word

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
P6	P7	P4	P5	P2	P3	P0	P1

4−bits per pixel SDRAM format

Addr	31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
N	P6	P7	P4	P5	P2	P3	P0	P1
N+1	P14	P15	P12	P13	P10	P11	P8	P9
N+2	P22	P23	P20	P21	P18	P19	P16	P17

2−bits per pixel within 32−bit word

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
P12	P13	P14	P15	P8	P9	P10	P11	P4	P5	P6	P7	P0	P1	P2	P3

2−bits per pixel SDRAM format

Addr	31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
N	P12	P13	P14	P15	P8	P9	P10	P11	P4	P5	P6	P7	P0	P1	P2	P3
N+1	P28	P29	P30	P31	P24	P25	P26	P27	P20	P21	P22	P23	P16	P17	P18	P19
N+2	P44	P45	P46	P47	P40	P41	P42	P43	P36	P37	P38	P39	P32	P33	P34	P35

1−bit per pixel within 32−bit word

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P24	P25	P26	P27	P28	P29	P30	P31	P16	P17	P18	P19	P20	P21	P22	P23	P8	P9	P10	P11	P12	P13	P14	P15	P0	P1	P2	P3	P4	P5	P6	P7

1−bit per pixel SDRAM format

Addr	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
N	P24	P25	P26	P27	P28	P29	P30	P31	P16	P17	P18	P19	P20	P21	P22	P23	P8	P9	P10	P11	P12	P13	P14	P15	P0	P1	P2	P3	P4	P5	P6	P7
N+1	P56	P57	P58	P59	P60	P61	P62	P63	P48	P49	P50	P51	P52	P53	P54	P55	P40	P41	P42	P43	P44	P45	P46	P47	P32	P33	P34	P35	P36	P37	P38	P39
N+2	P88	P89	P90	P91	P92	P93	P94	P95	P80	P81	P82	P83	P84	P85	P86	P87	P72	P73	P74	P75	P76	P77	P78	P79	P64	P65	P66	P67	P68	P69	P70	P71

4.3.5.5 OSD Attribute Window

OSD bitmap window 1 can be configured as an attribute window (OSDWIN1MD.OASW and OSDATRMD.OASW) instead of a bitmap window, see Figure 36. In this mode, the attribute window allows blending and blinking on a pixel-by-pixel basis in bitmap window 0. In particular, the attribute window provides a means to:

- Set the blending level (3 bits, 8 levels) of individual pixels in OSD window 0
- Set individual pixels in OSD window 0 to blink, if blinking is enabled

Table 38. OSD Attribute Pixel Format

Bit 3	Bit 2	Bit 1	Bit 0
Blink Enable 0: No blink 1: Blink	Blending level		

Figure 36. OSD Attribute Window

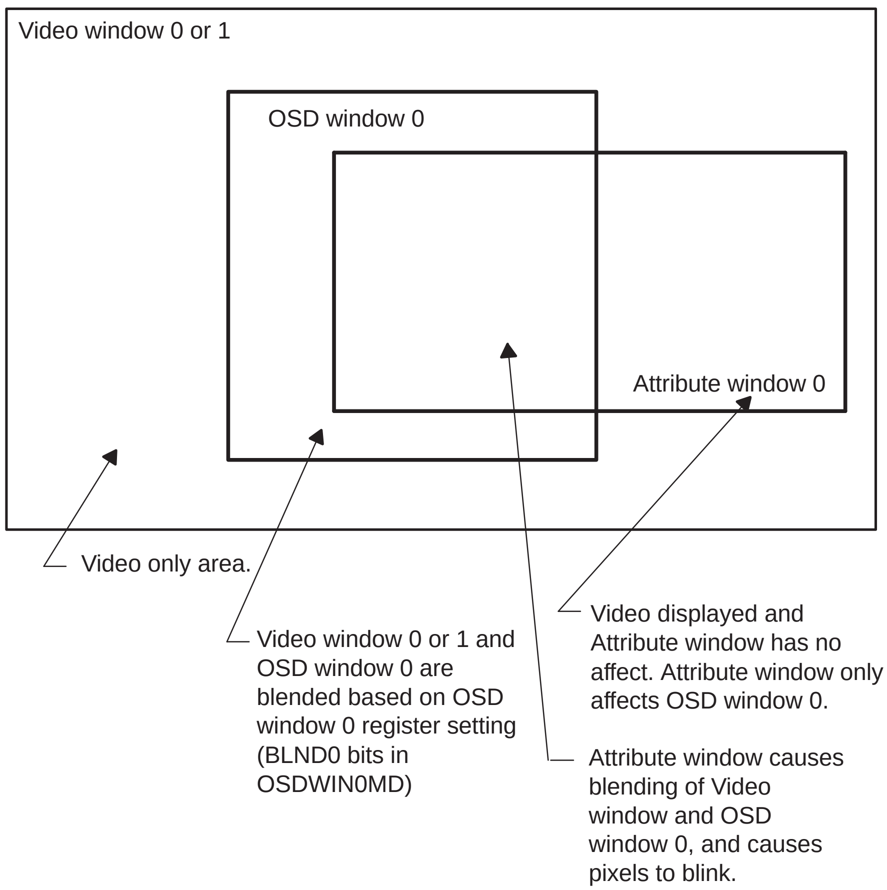


Table 39. OSD Blink Attribute Control Registers

Control Register.Field	Description
OSDATRMD.BLNK	Enable blinking defined by attribute window
OSDATRMD.BLNKINT	Set the blink interval

The SDRAM data format follows that for 4-bit bitmap windows (see Figure 35). Note that since each horizontal line of window data must be a multiple of 32 bytes, the attribute windows must contain a multiple of 32 bytes/1/2 bytes/pixel = 64 pixels per horizontal line.

4.3.5.6 OSD RGB565 Window

Either of the OSD bitmap windows can be configured to accept 16-bit RGB565 data instead of bitmap data. The RGB data from external memory is converted into YCbCr data within the OSD module using the following equations to calculate YCrCb:

$$Y = (0.2990 \times R) + (0.5870 \times G) + (0.1140 \times B)$$

$$Cb = (-0.1687 \times R) - (0.3313 \times G) + (0.5000 \times B) + 128$$

$$Cr = (0.5000 \times R) - (0.4187 \times G) - (0.0813 \times B) + 128$$

The transparency value for RGB565 windows can also be explicitly set rather than being forced to use a zero value, which would correspond to black.

Table 40. OSD RGB565 Control Registers

Control Register.Field	Description
OSDWIN0MD.RGB0E	Enable RGB565 mode for Window 0
OSDWIN1MD.RGB1E	Enable RGB565 mode for Window 1
TRANSPVAL.RGBTRANS	Transparency value for RGB565 window

The SDRAM format for RGB565 data is shown in Figure 37. Note that since each horizontal line of window data must be a multiple of 32 bytes, the RGB565 windows must contain a multiple of 32 bytes/2 bytes/pixel = 16 pixels per horizontal line.

Figure 37. Data Format – RGB565

(a) RGB565 pixels within 32-bit word

31 27	26 21	20 16	15 11	10 5	4 0
R1	G1	B1	R0	G0	B0

(b) RGB565 SDRAM format

Address	31 27	26 21	20 16	15 11	10 5	4 0
N	R1	G1	B1	R0	G0	B0
N + 1	R3	G3	B3	R2	G2	B2
N + 2	R5	G5	B5	R4	G4	B4
...	...					

4.3.6 OSD – Cursor Window

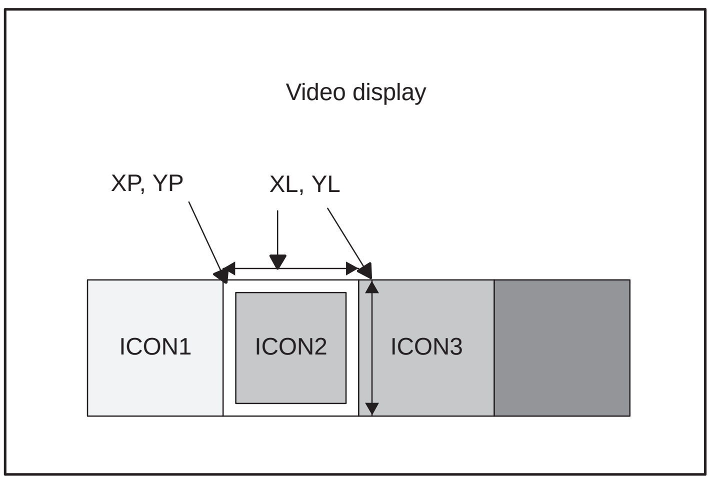
The rectangular hardware cursor always appears on top of all other OSD windows. The cursor size, color, horizontal and vertical thickness can be specified (see Table 41). This cursor can also be configured to use the ROM or RAM CLUT.

Figure 38 shows an example usage of the rectangle cursor. The outline shows the rectangle cursor and the ICON 1-4 windows are displayed by using OSD window 0 or 1.

Table 41. OSD Cursor Window Control Registers

Control Register.Field	Description
RECTCUR.RCAD	Cursor color address (offset into CLUT)
RECTCUR.CLUTSR	Cursor CLUT selection (RAM or ROM)
RECTCUR.RCHW	Rectangular Cursor Horizontal Width
RECTCUR.RCVW	Rectangular Cursor Vertical Width

Figure 38. Cursor Window Example



4.4 Video Encoder Module

The video encoder (VENC) module consists of two main submodules, and an analog NTSC/PAL video encoder with integrated 4-channel, 54-MHz video DACs and a digital LCD/video controller.

4.4.1 Video Timing Mode

The VENC module supports two timing modes: standard and non-standard.

4.4.1.1 Standard Mode

In this mode, the timing generator operates in the standard format. The support formats are 525/60 Hz (NTSC-M) or 625/50 Hz (PAL-B/D/G/H/I) for SDTV and 525p or 625p for HDTV. The digital output from the LCD interface is also available simultaneously. Note, however, this is limited to LCDs, DACs, and encoders that support NTSC/PAL timing and the output will mirror the analog output display.

4.4.1.2 Non-standard Mode

Note: The DACs should not be used in non-standard mode.

This mode is provided to configure the user-defined generic timing. The VENC module operates at any given timing defined by the module's register settings. In this mode, the DACs are automatically disabled. To select non-standard mode, set the VMD bit in VMOD to 1.

4.4.2 Synchronous Mode

The VENC module supports two synchronous modes: master and slave. Each mode can be used in either of the two video timing modes (standard NTSC/PAL and non-standard).

4.4.2.1 Master Mode

This mode operates in synchronization with horizontal/vertical sync signals generated by the timing generator in the VENC module.

4.4.2.2 Slave Mode

This mode operates in synchronization with sync signals input from an external source. To configure the video encoder as a slave device, set the SLAVE bit in VMOD to 1.

1. When the EXSYNC bit in SYNCCTL is cleared to 0, the external inputs from the HSYNC/VSYNC/FIELD pins are used as the external sync signals. It is also required to set the SYDIR bit in VIDCTL to 1 to configure the HSYNC/VSYNC/FIELD pins as input.
2. When EXSYNC bit in SYNCCTL is set to 1, the sync signals from the CCD controller are used as external sync signals. This provides synchronization between the CCD timing and video timing. It is possible to invert the timing signals by setting the EXHIV, EXVIV, and EXFIV fields in SYNCCTL.

4.4.3 Analog NTSC/PAL Video Encoder

The NTSC/PAL encoder (Figure 39) takes video data from the OSD module and generates the necessary signaling and formatting to display the video/image data on to an NTSC/PAL display. Table 42 specifies the video formats.

Table 42. Supported TV Formats

VMOD.HDMD	VMOD.TVTYP	Video Format
0	0	NTSC
	1	PAL
1	0	525p
	1	625p

Each of the 4 DACs can be assigned to any desired signal via the DACSEL register. The combination of 4 DAC outputs are described in Section 4.4.3.7.

For SDTV (NTSC/PAL), the following output configurations are supported:

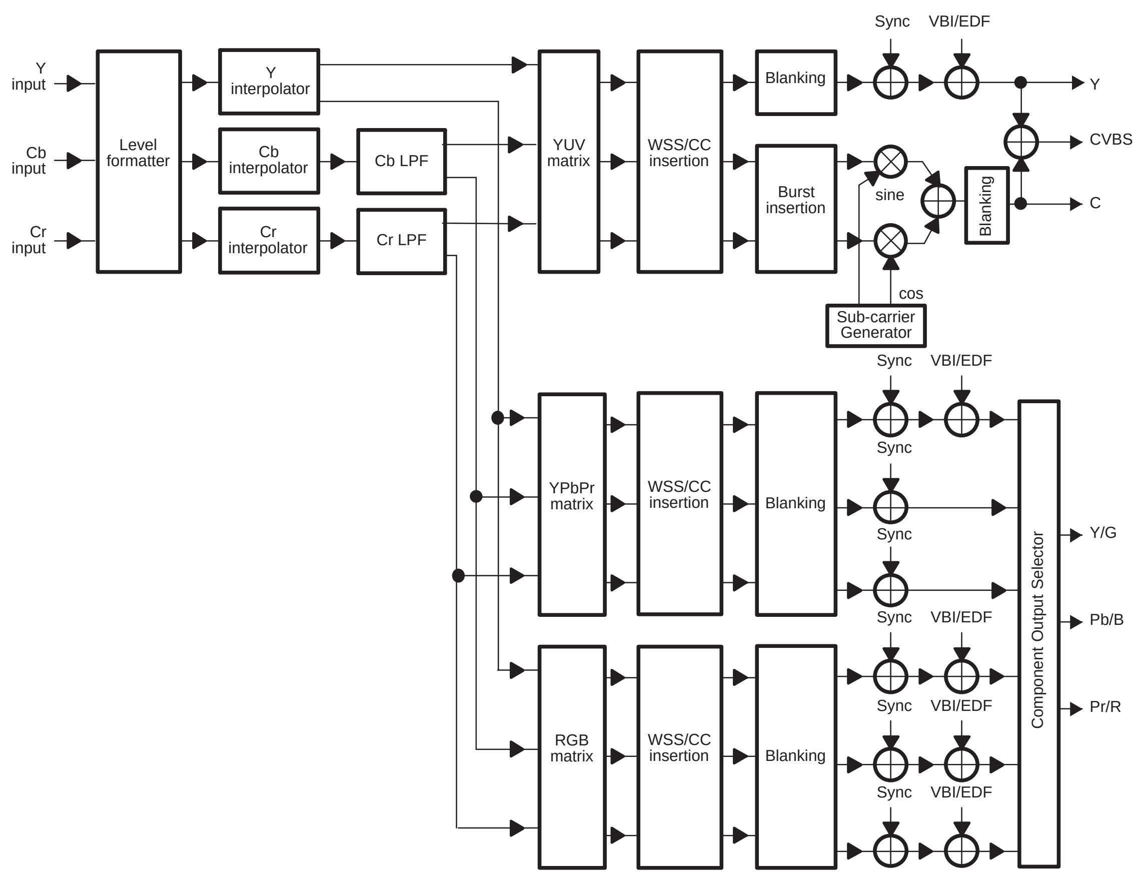
- Composite video (CVBS),
- S-video,
- Component (YPbPr), and
- RGB

Other composite DAC/timing settings are made via fields in the CVBS and ETMG0/1 registers.

For HDTV/EDTV (525p/625p), only component (YPbPr) or RGB output modes are valid. Other component DAC/timing settings are made via fields in the CMPNT and ETMG2/3 registers.

The BLNK field in the VMOD register is the blanking enable. When this field is set to 1, the CVBS and/or component output is blanked without regard to the input video signals.

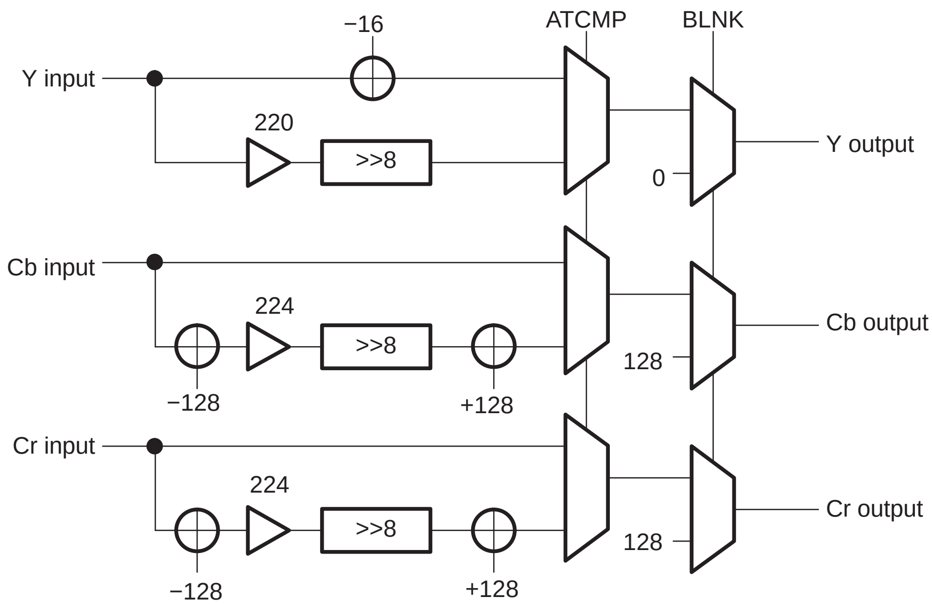
Figure 39. NTSC/PAL Video Encoder Block Diagram



4.4.3.1 Level Formatter

The front-end of the video encoder receives the YCbCr pixel data from the OSD module and converts it into the digital YPbPr, YUV, and RGB representations. The level formatter has the role to compress the signal level with 0-255 into the ITU-R BT.601 specified level (Y:16-235, C: 16-240). The user can choose whether or not to apply the attenuation independently for each data path using the ATCOM, ATYCC, and the ATRGB fields in the VDPRO register. Figure 40 shows the block diagram for the level formatter.

Figure 40. Level Formatter Block Diagram



4.4.3.2 Luma Signal Processing

The luma signal from the level formatter can be processed by a 2× interpolation with a filter. The filter is selected using VMISC.YUPF = 1. There are two filters available to perform the interpolation, from which only one is supported:

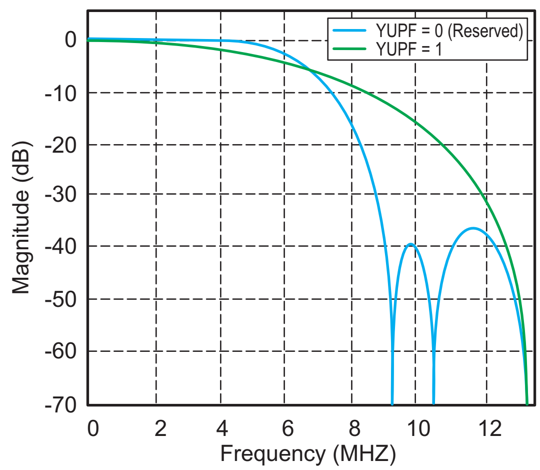
YUPF = 0: $[3 - 10_{(z-2)} + 39_{(z-4)} + 64_{(z-5)} + 39_{(z-6)} - 10_{(z-8)} + 3_{(z-10)}]/64$ (default, not supported)

YUPF = 1: $[1 + 2_{(z-1)} + 1_{(z-2)}$ (must be selected)

The interpolation is disabled by default and can be enabled by setting VDPRO.YUPS = 1. Note that when interpolation is enabled, VMISC.YUPF must be set to 1. When in progressive mode, the interpolation should be disabled since the pixel rate is already 27 MHZ. The frequency response of the luma interpolation filter is shown in Figure 41.

Note: When interpolation is enabled (VDPRO.YUPS = 1), VMISC.YUPF must be set to 1.

Figure 41. Luma Interpolation Filter



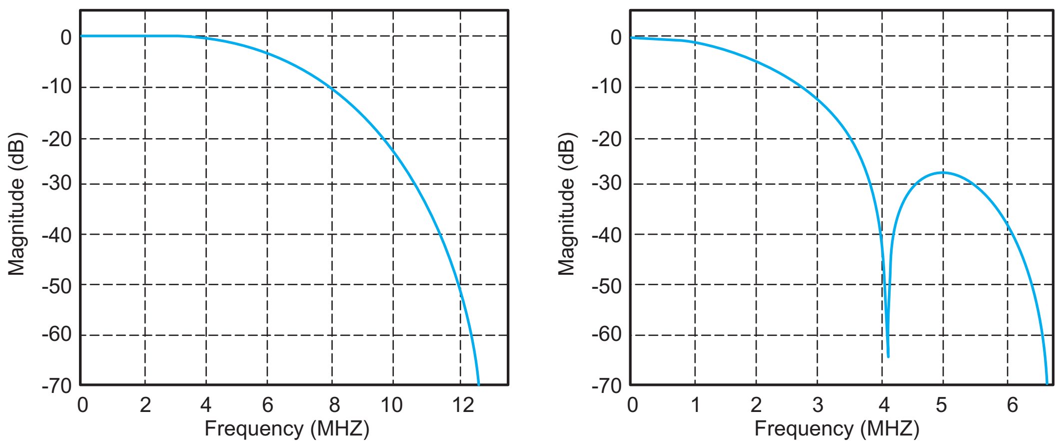
4.4.3.3 Chroma Signal Processing

The chroma signal from the level formatter can also be processed by a 2× interpolation with a filter. The cut-off frequency is 1.5 MHz with a transfer function of:

$[3 + 8_{(z-1)} + 10_{(z-2)} + 8_{(z-3)} + 3_{(z-4)}]/32$

The interpolation is disabled by default and can be enabled by setting VDPRO.CUPS = 1. The sampling rate of the LPF is 1/2 VENC clock (13.5 MHz). There are two outputs of this LPF block, composite and component. Low-pass filtering is only processed for composite output. No filtering is applied to the component output. The frequency response of the chroma interpolation filter is shown in Figure 42.

Figure 42. Chroma Interpolation Filter (left) and Chroma LPF (right)



4.4.3.4 CVBS Output

4.4.3.4.1 YUV Conversion

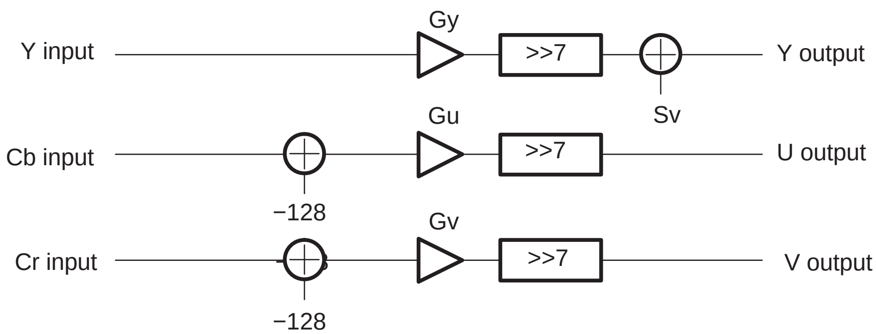
The interpolated and low pass filter YCbCr data are applied the proper gain and are then converted to YUV signals for CVBS generation. Table 43 shows the gain applied for each mode.

Table 43. Gains Used in YUV Conversion

CVBS.CVLVL	CVBS.CSTUP	Gy	Gu	Gv	Sv
0	0	305	315	444	0
	1	282	291	411	39
1	0	299	309	435	0
	1	277	285	403	38

The processing is done by subtracting 128 for the chroma (not for the luminance), then multiplying the gain and shifting right by 7. Figure 43 shows the block diagram for YCbCr to YUV conversion. When the CVBS.CSTUP = 1, then 7.5% setup is added for the output. The setting CSTUP is effective for both NTSC or PAL. However, note that for PAL mode, setting CSTUP = 1 causes an illegal output level.

Figure 43. YUV Conversion Block Diagram



4.4.3.4.2 CVBS Output Generation

The scaled luma then has the WSS and closed caption signals inserted and then is applied to the video edge controller. The video edge controller clips the video level of a few pixels around the horizontal blanking edge so that the output video has the proper blanking transition. This feature is enabled by default and can be disabled by CVBS.CBLS. For details of blanking edge shaping, see Section 2.1.3.2. Horizontal blanking start/end position can be adjusted by the CFPW and CLBI fields in the ETMG1 register. Following the edge shaping, the sync pulse are inserted. The horizontal sync pulse duration can be adjusted by the CEPW and CFSW fields in the ETMG0 register.

Table 44. Sub-Carrier Initial Phase Default Value

Mode	Preset Value
NTSC	378
PAL	356

Color burst insertion horizontal position can be controlled by the CBST and CBSE fields in the ETMG1 register. The modulated chroma signal is also applied to blanking edge shaping. Chroma blanking shaping can also be disabled by CBLS and blanking horizontal position is also adjusted by CFPW and CLBI.

The resulted Y and C are mixed together to get composite video output. Separated Y and C are also available for S-Video output. The offset 512 is added to the separated C to have the blanking level at the center of the DAC range. You can also control the blanking build-up time (Table 45) and the sync build-up time (Table 46).

Table 45. CVBS Blanking Build-Up Time

CVBS.CBBLD	Time
0	140 ns
1	300 ns

Table 46. CVBS Sync Build-Up Time

CVBS.CSBLD	Time
0	140 ns
1	200 ns

4.4.3.5 Analog Component Output

4.4.3.5.1 YPbPr Matrix

The interpolated and low-pass filtered YCbCr data has a gain applied and then is converted into YPbPr component. The processing is done by subtracting 128 for chroma (not for luma) then multiplying by the appropriate gain followed by right shifting by 7-bits. Figure 44 shows the block diagram for YCbCr to YPbPr conversion. MYLVL and MCLVL in the CMPNT register specify the luma and chroma level, respectively. When the CMPNT.MSTUP is 1, a 7.5% setup offset is added to the luma output. Table 47 and Table 48 show the gain for each mode.

Figure 44. YUV Conversion Block Diagram

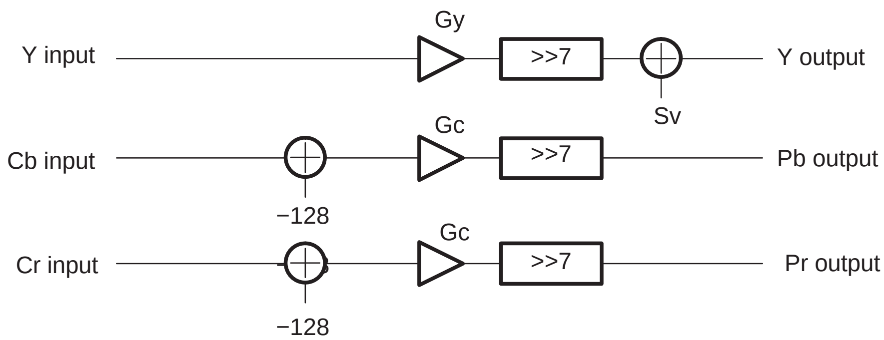


Table 47. Gain for YPbPr Conversion (Luma Level)

CMPNT.MYLVL	CMPNT.MSTUP	Gy	Sv	Mode
0	0	305	0	100% 714 mV, Sync:286 mV, no setup
	1	282		100%:714 mV, Sync:286 mV, with setup
1	0	299		100%:700 mV, Sync:300 mV, no setup
	1	277		100% 700 mV, Sync:300 mV, with setup

Table 48. Gain for YPbPr Conversion (Chroma Level)

CMPNT.MCLVL	Gc	Mode
0	292	SMPTE/N10
1	390	Betacam
2	270	MII
3	-	-

4.4.3.5.2 Component Output Generation

The scaled YPbPr has the WSS and closed caption signals inserted and is then applied to the video edge controller. The same features as are used for composite mode are available for component mode. The chroma signals, Pb and Pr, can also be applied to this shaper. This feature is enabled by default and can be disabled by setting the MBLS bit in CMPNT to 1. The horizontal blanking position can be adjusted by the CFPW and CLBI fields in ETMG3.

Following edge shaping, the sync pulse is inserted. Sync insertion on/off can be controlled by the MSYG, MSYB, and MSYR fields in CMPNT. Sync on the luminance component is on by default. Horizontal sync insertion timing can be adjusted by the MLSW field in ETMG2. The duration of the equalizing pulse and the vertical serration pulse can be adjusted by the MEPW and MFSW fields in ETMG2. Different sync timing can be applied for composite and component even when both signals are output from different DACs simultaneously.

For progressive, the processing is the same as above. Sync build-up times and blanking edge build-up time are different from SDTV. Table 49 and Table 50 show these timings.

Table 49. Component Blanking Build-Up Time

VMOD.HDMD	CMPNT.MBBLD	Time
0	0	140 ns
	1	300 ns
1	0	70 ns
	1	150 ns

Table 50. Component Sync Build-Up Time

VMOD.HDMD	CMPNT.MSBLD	Time
0	0	140 ns
	1	200 ns
1	0	70 ns
	1	100 ns

4.4.3.6 Analog RGB Output

4.4.3.6.1 RGB Matrix

The interpolated and low-pass filtered YCbCr data comes into the RGB converted to get an analog RGB output (Figure 45). The RGB matrix is implemented based on the following equation:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \frac{1}{1024} \begin{bmatrix} GY & 0 & RV \\ GY & -GU & -GV \\ GY & BU & 0 \end{bmatrix} \begin{bmatrix} Y \\ Cb - 128 \\ Cr - 128 \end{bmatrix}$$

The coefficients of this matrix are fully programmable. The ARGBX0—ARGBX4 registers are used to program the conversion coefficients. The ITU-R BT601 RGB conversion matrix is used as the default. RGB ranging from 0 to 219 can be obtained from the REC.601YCbCr signal (Y:0-219, C:16-240). Note, that the subtraction of 16 for Y is already done. A 7.5% setup offset is also added to the RGB output when the MSTUP bit in CMPNT is 1. MSTUP is effective with regards to MYLVL. Table 51 shows the gain for each mode.

Figure 45. RGB Converter Block Diagram

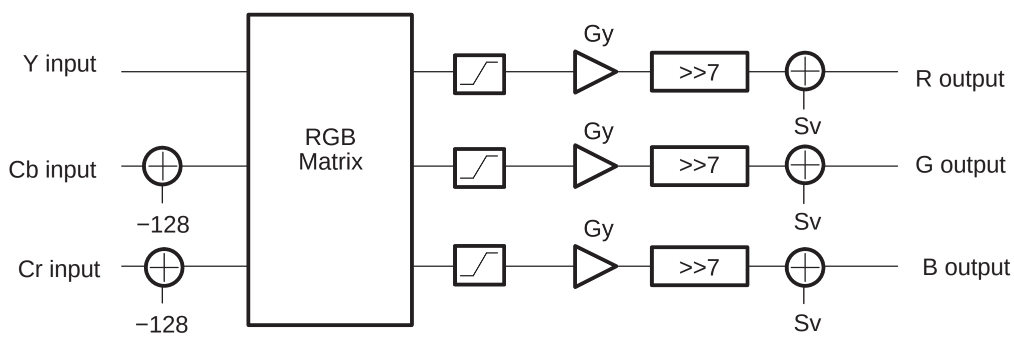


Table 51. RGB Gain for Component Conversion

CMPNT.MYLVL	CMPNT.MSTUP	Gy	Sv	Mode
0	0	305	0	100% 714 mV, Sync:286 mV, no setup
	1	282	39	100%:714 mV, Sync:286 mV, with setup
1	0	299	0	100%:700 mV, Sync:300 mV, no setup
	1	277	35	100% 700 mV, Sync:300 mV, with setup

4.4.3.6.2 RGB Output Generation

The converted RGB output has the WSS and closed-caption signals inserted. These signals are inserted to all 3 components simultaneously. Then they are applied to the video edge controller, similar to the case for CVBS or YPbPr. Following edge shaping, the sync pulse pulses are inserted. You can specify which RGB component to have the sync pulse inserted.

The following registers for RGB are shared with component video:

- Sync insertion enable (MSYG, MSYB, MSYR)
- Blanking edge enable (MBLS)
- Blanking build-up time (MBBLD)
- Sync build-up time (MSBLD)
- Horizontal timing control (ETMG2, ETMG3)

Either YPbPr or RGB can be output from the DACs. The device does not support parallel use. This can be controlled by the MRGB bit in CMPNT.

4.4.3.7 DAC Output

4.4.3.7.1 DAC Output Level

The video encoder has a 10-bit digital output to the DAC input. It is designed so that the full digital output (7FFh = 1023) is expected to be converted to 1400 mV. You need to take care of the DAC termination in considering this.

4.4.3.7.2 DAC Output Configuration

Output video signal assignments to 4 DACs can be configurable by corresponding DA0S-DA3S fields in DACSEL. For component output, the MRGB bit in CMPNT controls whether the YPbPr component or RGB is output. Table 52 shows the configuration of DAC output selection.

Table 52. DAC Output Select

DACSEL.DA*n*S	CMPNT.MRGB	DAC Output
0	-	CVBS
1	-	S-Video Y
2	-	S-Video C
3	0	Y
	1	G
4	0	Pb
	1	B
5	0	Pr
	1	R
6-15	-	Reserved

4.4.3.7.3 DAC Oversampling

When the DAC is clocked at 54 MHz and the video encoder (VENC) is operating in 27 MHz, the video output from the video encoder can have 2× oversampling applied for anti-aliasing (enabled by setting the DAUPS bit in the video data processing register (VDPRO to 1). The structure and coefficients of the interpolation filter is the same as used in luma upsampling (see Section 4.4.3.2).

If the DAC frequency is configured to 27 MHz, the DAC oversampling should not be activated (DAUPS = 0 in VDPRO). Note that the DAC frequency is configured in the System Module.

Table 53 shows the possible clock options for OSD, VENC, and DACs. For NTSC/PAL (SDTV), the OSD must be operated at half the clock rate of the VENC. The DAC can be clocked at either 27 MHz or 54 MHz. For HDTV/EDTV (525p, 625p), the video data rate is doubled; therefore, the OSD module needs to be clocked at 27 MHz. To remove aliasing, the DAC needs to be clocked at 54 MHz.

Note that the DAC operating frequency must be set according to the clock rate set in the Clock Controller/System Modules using the DAFRQ bit setting in VDPRO.

Table 53. OSD, VENC, DAC Clocking Options

Format	OSD	VENC	DAC	DAFRQ	DAUPS	Oversampling
NTSC/PAL	13.5 MHz	27 MHz	27 MHz	0	0	Off
NTSC/PAL	13.5 MHz	27 MHz	54 MHz	1	0	Off
NTSC/PAL	13.5 MHz	27 MHz	54 MHz	1	1	On
525p/625p	27 MHz	27 MHz	54 MHz	1	0	On
525p/625p	27 MHz	27 MHz	54 MHz	1	1	On

4.4.3.7.4 DAC Output Disable/Power Down

Clearing the VIE bit in VMOD to 0 forces the output of the 4 DACs to a low-voltage level regardless of the video signal. The DAC can also power down itself by setting the DAPD0-3 fields in DACTST. The 4 DACs can be powered down independently. Note, that by default, these registers are set to 1, so you must clear them to 0 before using the analog output.

4.4.3.7.5 DAC DC Output Mode

The DACs support outputting a DC output instead of an analog output from the DAC pins. Setting the DADC bit in DACTST to 1 switches DAC digital input from normal video signal to the digital signal level, as specified by the DALVL bit in DACTST. In this mode, all 4 DACs have the same DC output.

4.4.3.7.6 Y/C Delay

The Y signal delay can be adjusted and different delays can be applied to CVBS and component. The CYDLY bit in CVBS adjusts the Y delay for CVBS output; the MYDLY bit in CMPNT adjusts the Y delay for component video.

4.4.3.7.7 Video Attribute Insertion

The video encoder has capability to insert video information into the vertical blanking period. For example, the video encoder can insert a video attribute which indicates the proper aspect ratio to the video receiver. For NTSC mode, the video encoder can insert 14-bit video information on line 20 and line 283 to conform to the EIAJ CPR-1024 Video Aspect Ratio ID specification. Attribute information should be set using the ATR1 and ATR0 registers. The ATR2 register should be set with the 6-bit CRC data that is calculated by the following equation:

$G(x) = x^6 + x + 1$, where x^6 and x are preset to 1.

Bit 7 of ATR2 enables attribute insertion.

For PAL mode, the video encoder can insert 14-bit video information (WSS) on line 23 of every frame to conform to the ITU-R BT.1119-2 (ETSI EN 300 294) Wide Screen Signaling specification. Attribute information should be set in ATR1 and ATR2 bits 5-0. Bit 7 of ATR2 enables attribute insertion.

In NTSC and PAL encoding modes, data in the ATR1 and ATR0 registers are transferred to internal circuitry when ATR2 is set. For this reason, ATR2 should be set last.

The video encoder also supports video ID insertion for progressive. EIAJ CPR-1204-1 for 525p and IEC 62375 for 625p. Usage of ATR0-ATR2 registers is same as in SDTV (NTSC for 525p, PAL for 625p).

4.4.3.7.8 Closed-Captioning

The video encoder supports closed-caption encoding. Closed-caption data is transmitted on line 21 of the odd field and line 284 of the even field in NTSC. It is possible to specify the fields on which closed-captioning is enabled by CAPCTL.CAPF.

The data should be written to the CAPDO or CAPDE registers for odd or even fields, respectively. It is required to load the data at least 1 line early. When data is written to CAPDO/CAPDE, VSTAT.CAOST/VSTAT.CAEST) is changed to 1. This bit is automatically cleared to 0 when caption data transmission is completed on line 21 in the odd field or line 284 in the even field.

When the caption data register (CAPDO or CAPDE) is not updated before the caption data transmission timing for the corresponding field, the ASCII code specified by CAPCTL.CADF is automatically transmitted for closed caption data.

The width of every data register is 7-bits and the parity bit is automatically calculated by hardware.

4.4.3.7.9 Sub-Carrier Generation

The video encoder generates the sub-carrier by internal DDS (Direct Digital Synthesizer). The phase resolution of DDS is (1/1024) × 360°.

SC-H (Sub-carrier to Horizontal) phase can be controlled by user. Writing the SCSD bit in SCPROG automatically updates the sub-carrier phase as the specified value. Update occurs at line 9 in color field 1 for both NTSC and PAL. By default, preset values shown in Table 54 are applied. These values are chosen so that SC-H phase close to 0°.

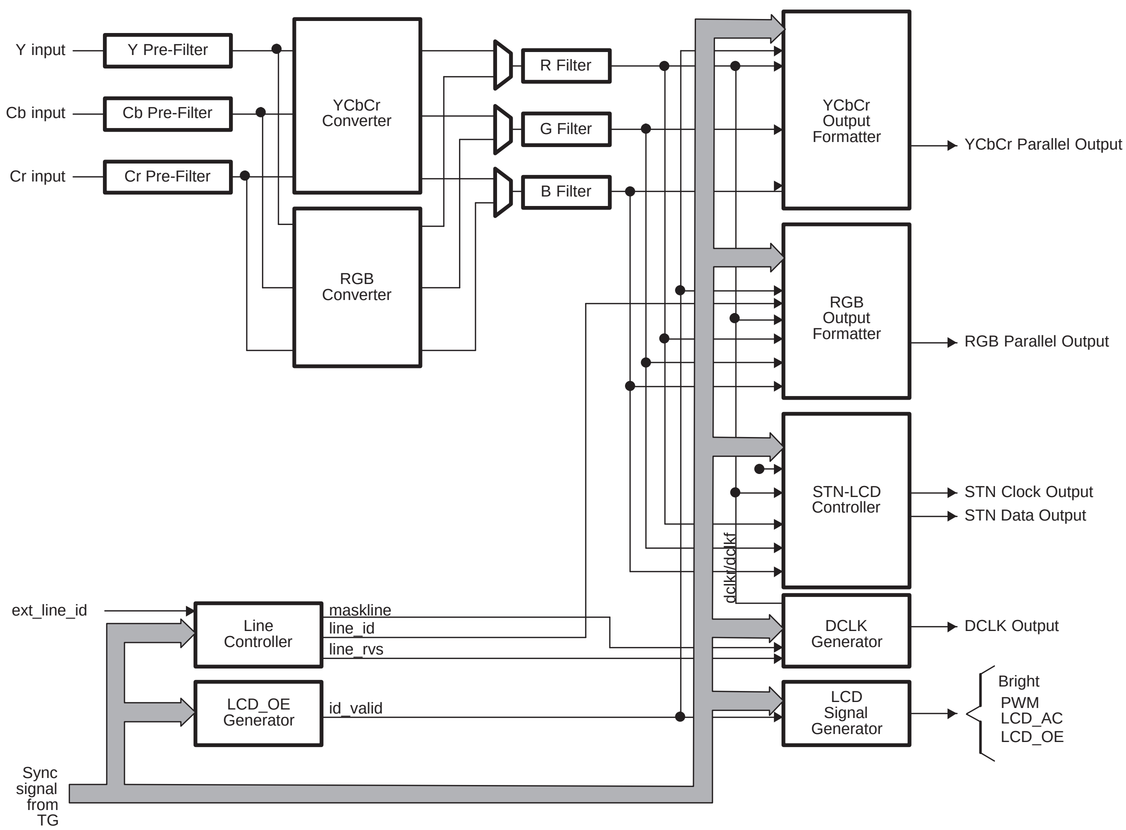
Table 54. OSD, VENC, DAC Clocking Options

Mode	Preset Value
NTSC	378
PAL	356

4.4.4 Digital LCD Controller

The digital LCD controller is shown in Figure 46.

Figure 46. Digital LCD Controller Block Diagram



4.4.4.1 Digital Video Output Mode

The digital LCD controller supports up to 8 digital output modes. The mode can be selected by VMOD.VDMD and are shown in Table 55.

Table 55. Digital Video Output Modes

VMOD.VDMD	Mode	Description
0	YCC16	16-bit YCbCr output mode. Y and C are output separately on 16-bit bus.
1h	YCC8	8-bit YCbCr output mode. 422 YCbCr is time-multiplexed on the 8-bit bus. Optionally supports ITU-R BT.656 output.
2h	PRGB	Parallel RGB mode to output RGB separately.
3h-7h	-	Reserved

4.4.4.2 Timings

The timing parameter control registers are shown in Table 56. Figure 47 to Figure 49 show the timing charts for HSYNC, VSYNC, FIELD and LCD_OE. For interlaced operation when VMOD.NSIT is 1, the vertical interval and pulse width is counted by half line (0.5H).

Table 56. Timing Control Registers

Register	Offset	Description	Unit
HSPLS	04h	HSYNC pulse width	CLK
VSPLS	05h	VSYNC pulse width	H (0.5H)
HINT	06h	HSYNC interval (HINT + 1). Must be even when OSD clock is 1/2 VENC clock	CLK
HSTART	07h	Horizontal data valid start position	CLK
HVALID	08h	Horizontal data valid duration	CLK
VINT	09h	VSYNC interval (VINT + 1)	H (0.5H)
VSTART	0Ah	Vertical data valid start position	H
VSTARTA	4Ah	Vertical data valid start position (optionally available only for even field).	H
VVALID	0Bh	Vertical data valid duration	H
HSDLY	0Ch	HSYNC delay	CLK
VSDLY	0Dh	VSYNC delay	CLK

Figure 47. Horizontal Timing

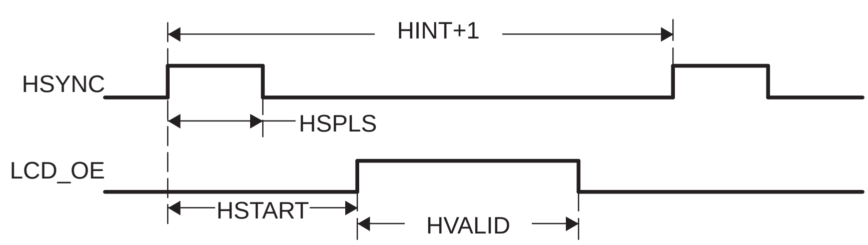
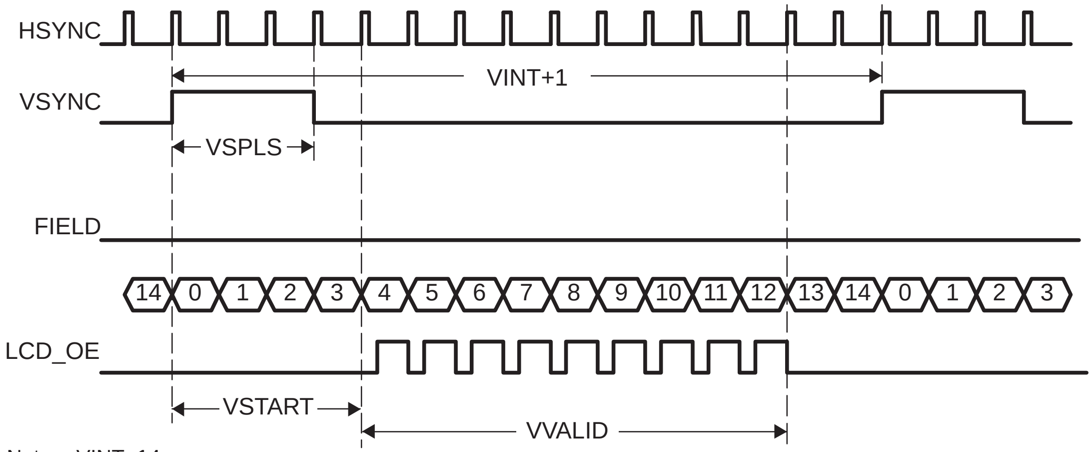
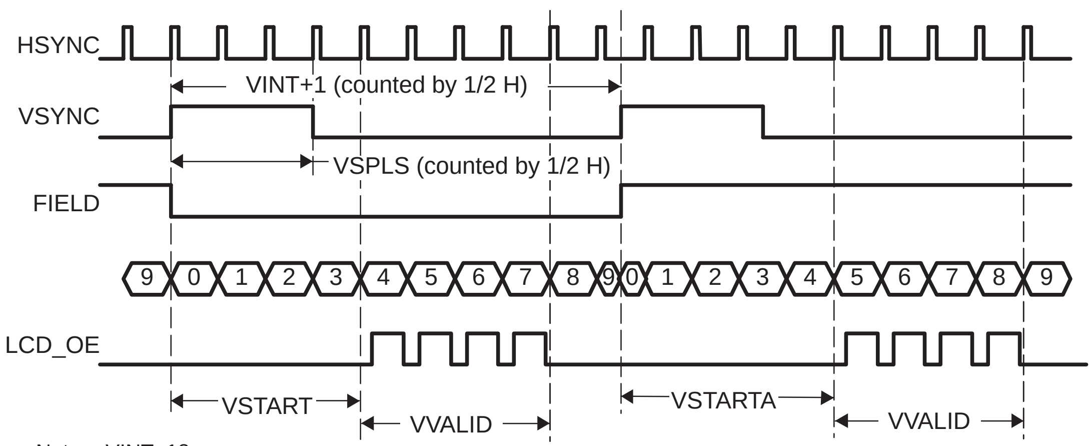


Figure 48. Vertical Timing (Progressive)



Notes: VINT=14
VSTART=4
VSPLS=3
VVALID=9

Figure 49. Vertical Timing (Interlaced)



Notes: VINT=18
VSTART=4
VSPLS=6
VVALID=4
VSTARTA=5

When in interlaced mode (VMOD.NSIT = 1 or NTSC/PAL), different VSTART positions can be specified for odd and even fields. VSTART is for odd fields and VSTARTA is for even fields.

The HSYNC and VSYNC outputs can be delayed via HSDLY and VSDLY registers, respectively, without affecting the timing of the internal sync signals. The FIELD output is also delayed by VSDLY.

In standard mode operation (VMOD.VMD = 0), horizontal and vertical pulse width and interval timings are fixed by hardware to conform to the video standard regardless of the HSPLS, VSPLS, HINT and VINT registers. Regarding pulse width, the optional sync pulse width processing mode is provided to program standard mode sync pulse width by the HSPLS and VSPLS registers. This mode is enabled when SYNCTL.SYSW is 1. When interlaced (VMOD.HDMD = 0), VSYNC pulse width is counted in 0.5H (half lines). The parameters are shown in Table 57.

Table 57. Standard Video Timing

	SDTV (HDMD = 0)		HDTV (HDMD = 1)		
Parameter	**NTSC (TVTYP = 0)**	**PAL (TVTYP = 1)**	**525p (TVTYP = 0)**	**625p (TVTYP = 1)**	**Unit**
HSYNC pulse width	127	127	63	63	CLK
VSYNC pulse width	6	5	6	5	H
Horizontal interval	1716	1724	858	864	CLK
Vertical interval	262.5	312.5	525	625	H

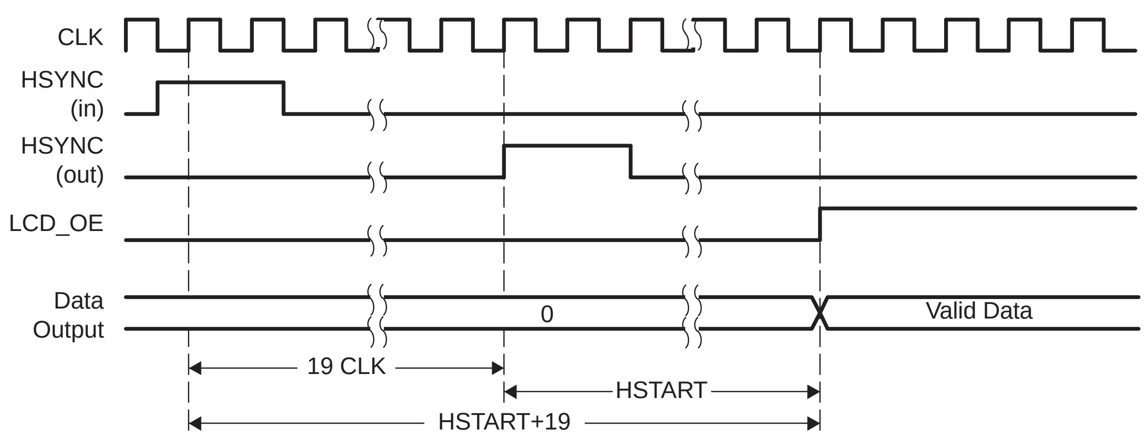
4.4.4.3 Slave Mode Timings

4.4.4.3.1 Horizontal Timing

Figure 50 shows the slave mode horizontal timing chart. It takes 19 CLK's for HSYNC output to be asserted after the external HSYNC input is latched. The data start position from HSYNC output is not different from master mode. However, HSYNC output cannot be seen from outside chip because HSYNC pin is shared with input for slave and output for master. The HSYNC output timing in Figure 50 is for reference.

This horizontal timing is always applied regardless video timing mode (VMOD.VMD).

Figure 50. Horizontal Timing Chart

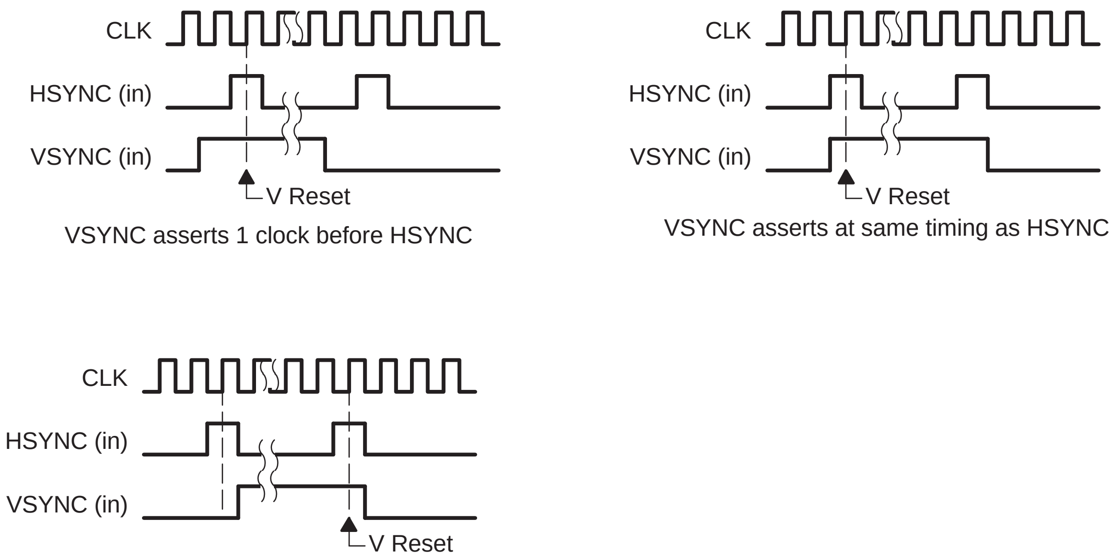


4.4.4.3.2 Vertical Timings

If VSYNC is behind HSYNC assertion, vertical reset is suspended until the next HSYNC rise edge. Figure 51 shows various VSYNC detection timings.

Figure 52 shows the vertical timing chart of NTSC slave mode. Vertical timing is reset when VSYNC rise transition is detected at HSYNC rising edge or the center of line (0.5H). Figure 53 indicates the PAL slave mode. Please note that the field is oppositely detected in PAL. In vertical timing chart of slave mode, output timings of HSYNC, VSYNC and VSYNC pins are denoted but these cannot be seen from outside chip because they are used as input in slave mode.

Figure 51. VSYNC Input Latch Timing



VSYNC asserts 1 clock before HSYNC

VSYNC asserts at same timing as HSYNC

VSYNC asserts 1 clock after HSYNC

Figure 52. Vertical Timing Chart (NTSC)

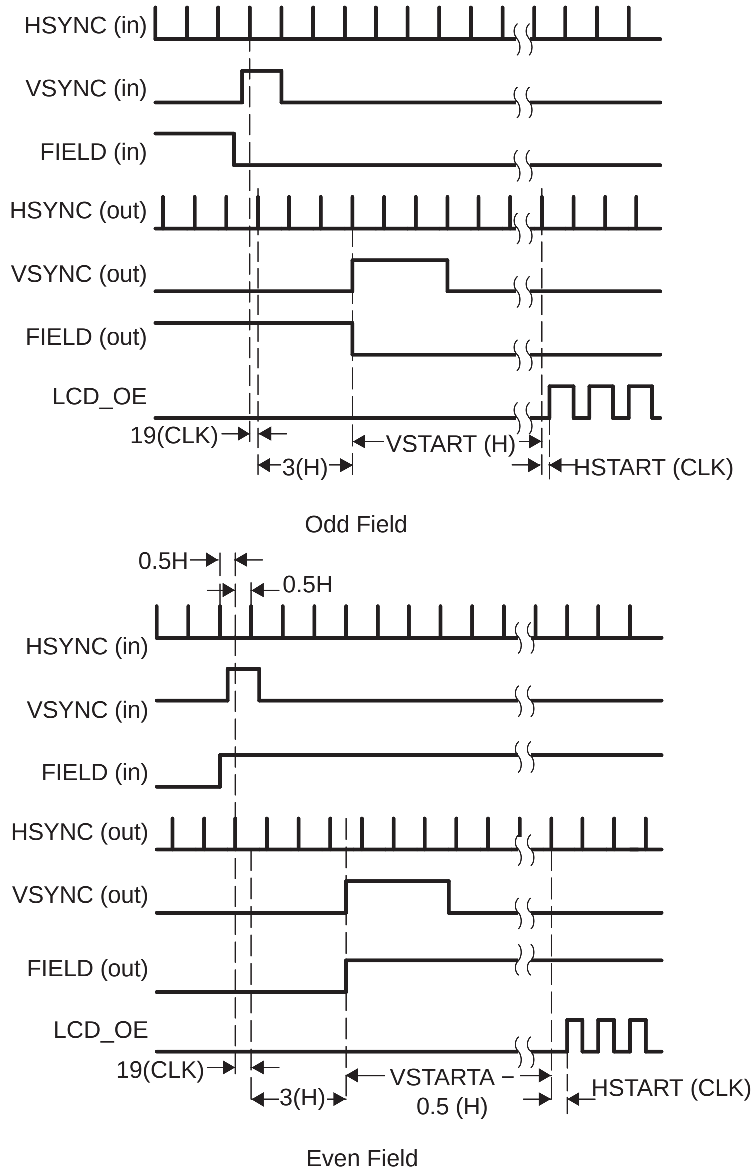


Figure 53. Vertical Timing Chart (PAL)

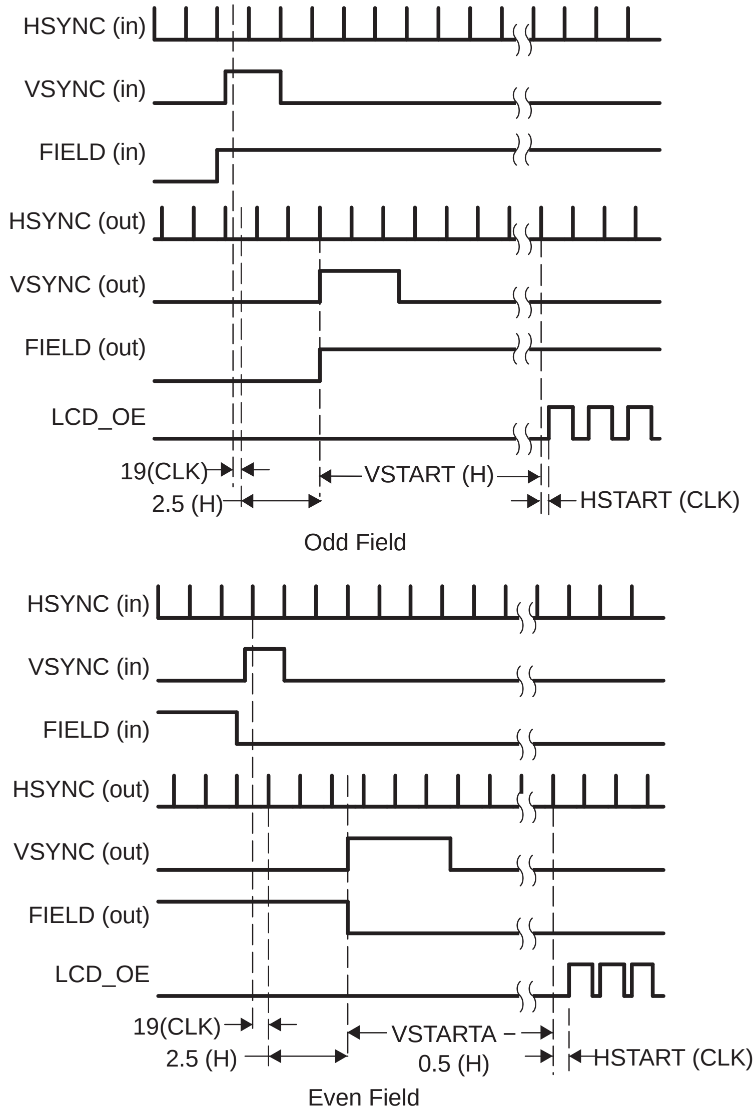


Figure 54 shows the vertical timing char of slave non-standard progressive mode (VMD=1, NSIT=0). Figure 55 indicates the Non-standard interlace timing (VMD=1, NSIT=1). Vertical timing is reset when VSYNC rise transition is detected at HSYNC rising edge. Please note that interlace mode vertical timing is reset only when VSYNC rise transition is detected at HSYNC rising edge (not at the center of line (0.5H) as in NTSC/PAL).

Figure 54. Vertical Timing Chart (Non-standard/Progressive)

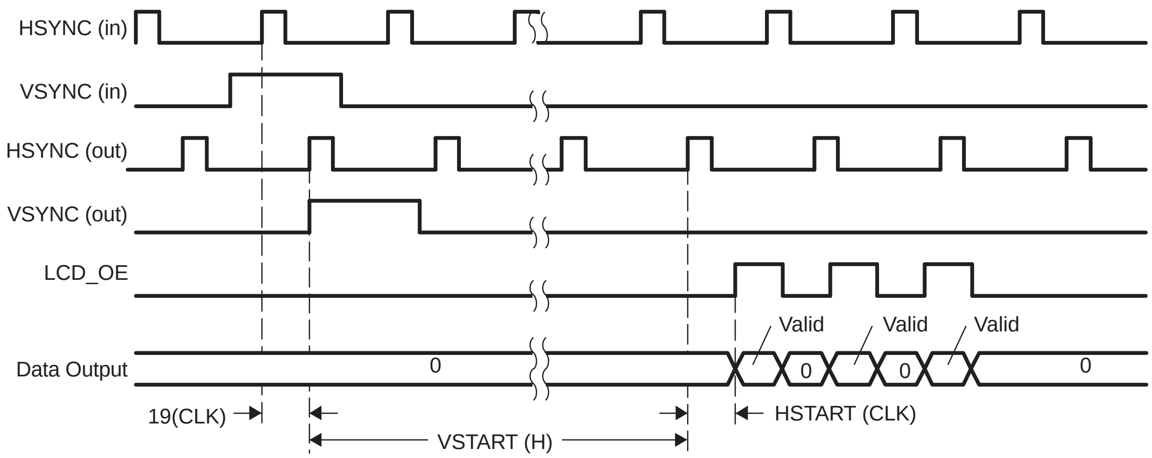
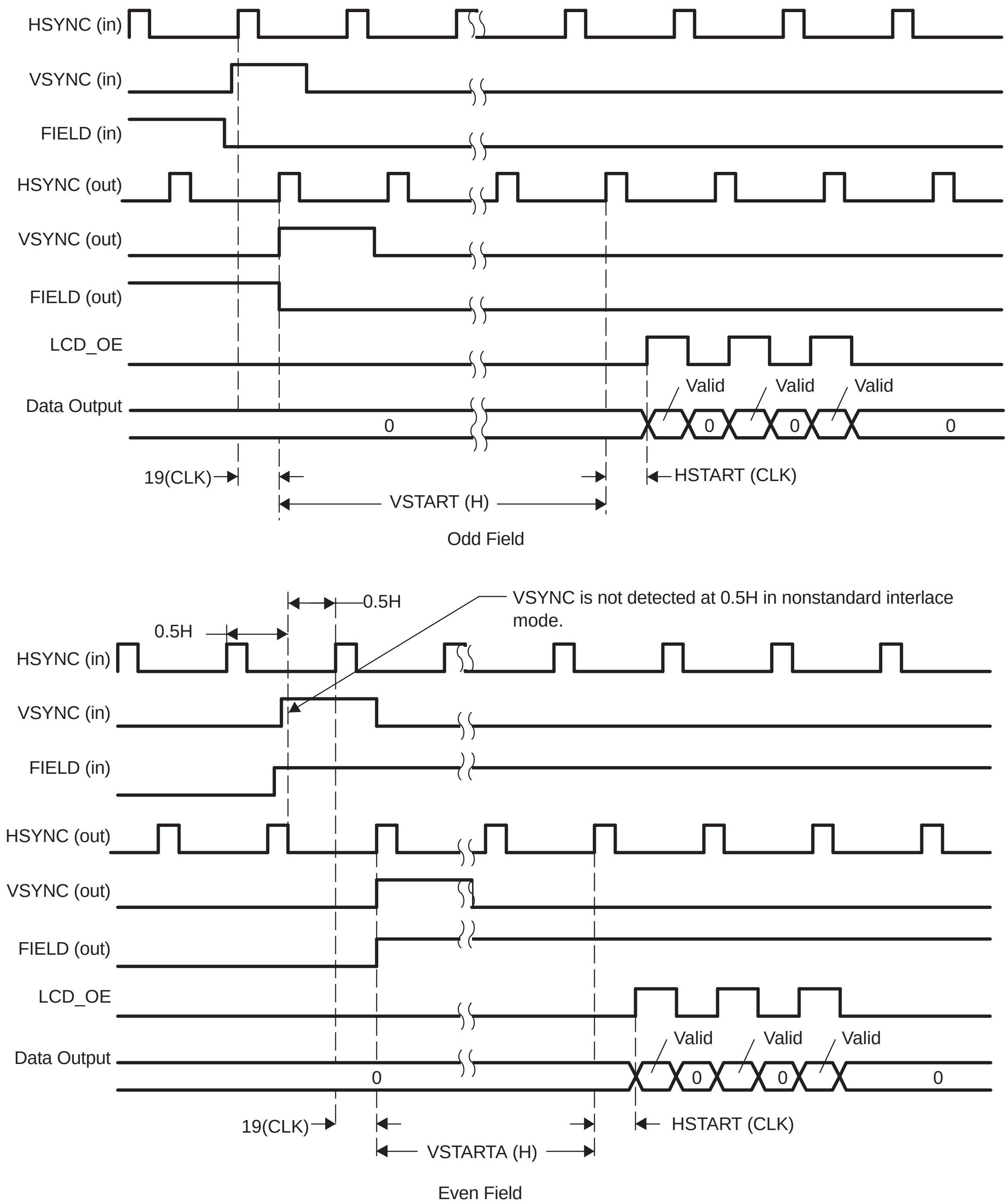


Figure 55. Vertical Timing Chart (Non-standard/Interlace)



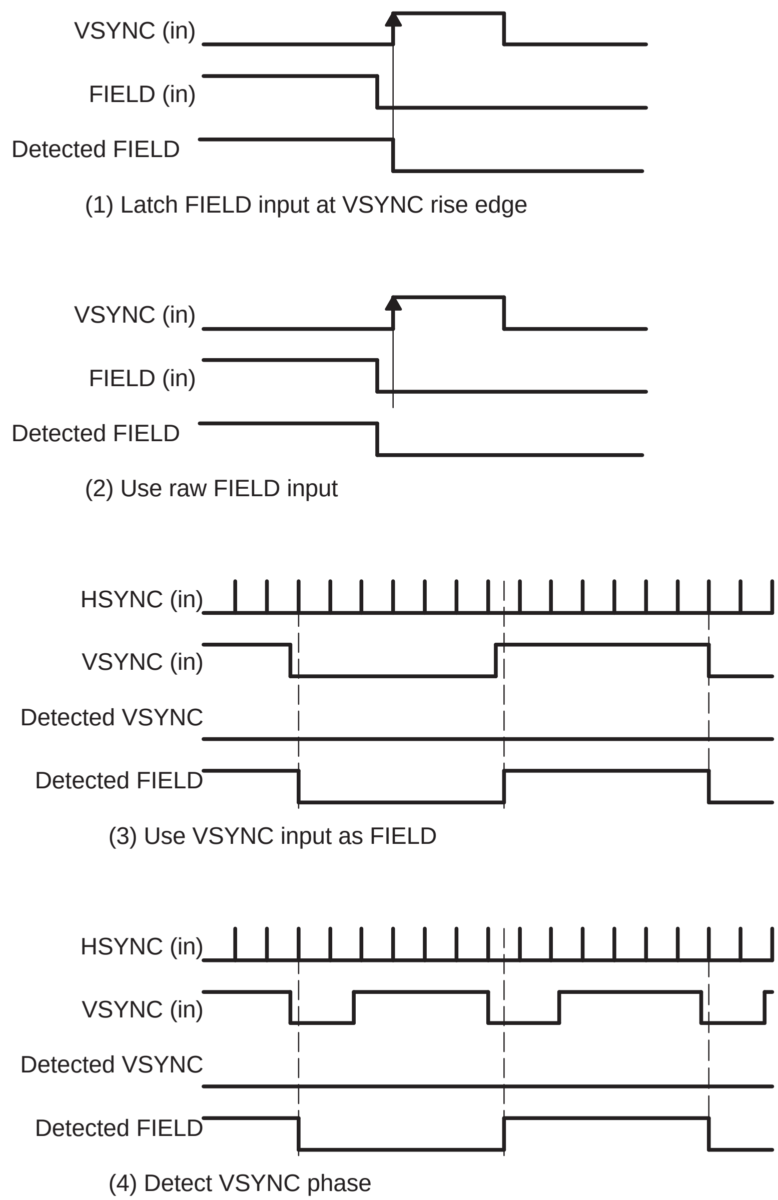
4.4.4.3.3 Slave Mode Field Detection

For slave interlace mode, namely when NTSC/PAL (VMD = 0 and HDMD = 0) or non-standard interlace (VMD = 1 and NSIT = 1), external field ID is detected. There are 4 field detection modes:

- Latch FIELD input at VSYNC rise edge
- Use raw FIELD input
- Use VSYNC input as FIELD
- Detect VSYNC phase

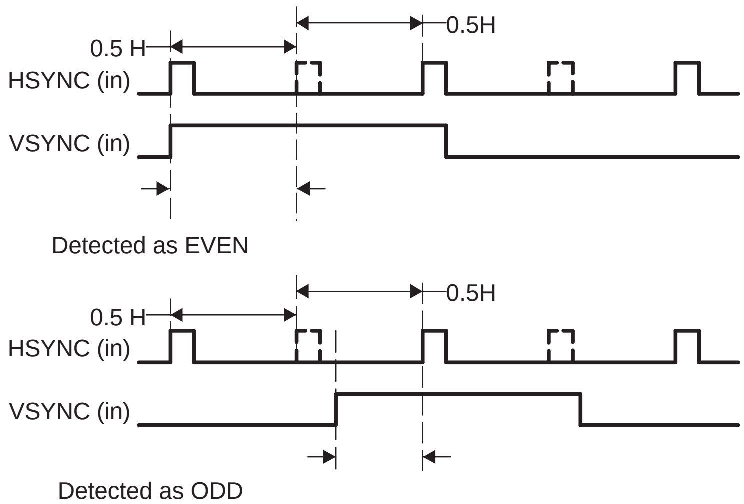
These 4 modes can be selected by SYNCCTL.EXFMD. Figure 56 shows the timing of each mode.

Figure 56. Field Detection Mode



In the option 4 (Detect VSYNC phase), the timing generator detects VSYNC assertion position in a line. When VSYNC is in the first half of a line, the field is detected as even. When VSYNC is the second half of a line, the field is detected as odd. Figure 57 show this detection scheme. This mode is only available for NTSC/PAL. When in non-standard mode, Field_id is always detected as odd in option 4.

Figure 57. Field Detection by VSYNC Phase



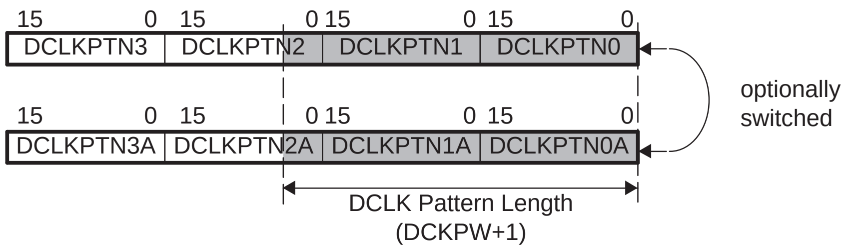
4.4.4.4 DCLK Generation

The LCD controller can generate a dot clock, called DCLK, that is fed to LCD panels. The generated DCLK is output from the VCLK pin. Frequency, waveform, and valid duration of the DCLK is programmed by register settings with various options. The digital data is output synchronized to the rising edge of DCLK.

4.4.4.4.1 Pattern Register

The DCLKPTN register is provided for DCLK waveform configuration. The user can configure various waveforms for DCLK within up to a 64 cycle period. The register is 64-bits in length, mapped onto four 16-bit registers (DCLKPTN0-3). The effective pattern length can be specified in DCLKCTL.DCKPW. Moreover, another set of pattern registers with same structure (DCLKPTN0- 3A) is optionally provided. This enables user to switch the waveform on certain lines. Figure 58 shows the DCLK pattern register configuration scheme.

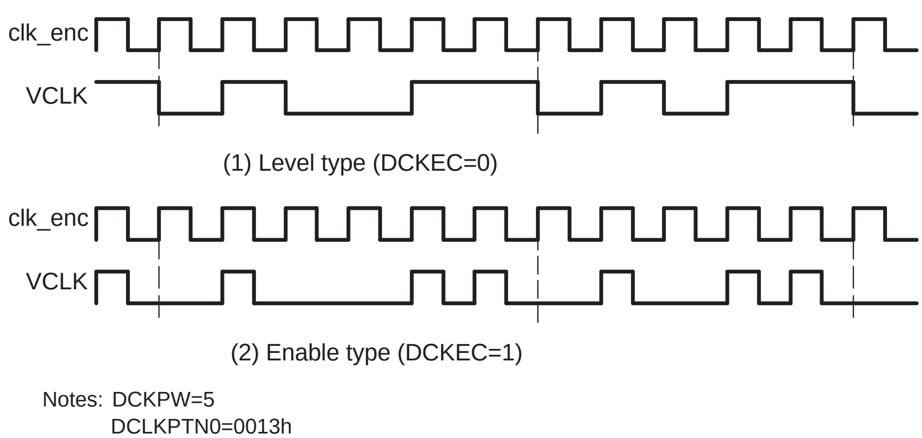
Figure 58. Pattern Register Configuration



There are two types of clock waveform configurations. They can be selected by DCLKCTL.DCKEC. For an example, see Figure 59.

- When DCKEC = 0, the pattern register becomes the clock level pattern of DCLK itself (Level mode).
- When DCKEC = 1, the pattern register works as the clock enable of the ENC clock (Enable mode).

Figure 59. DCLK Pattern Mode



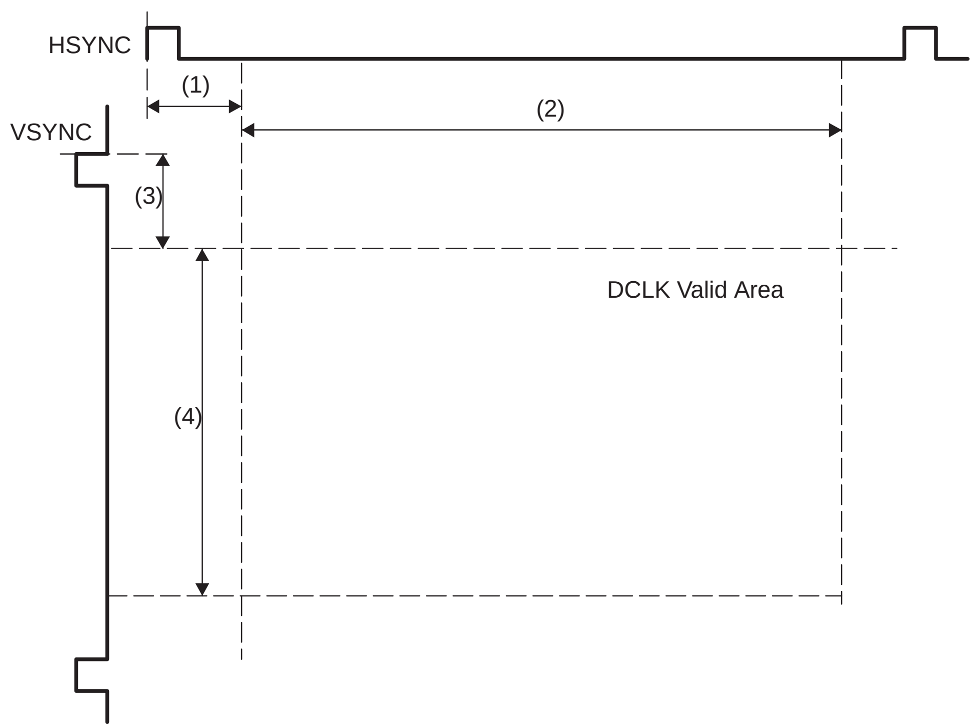
4.4.4.4.2 Masking

It is possible to mask the DCLK signal in horizontal and vertical. The registers listed in Table 58 allow you to set when DCLK is valid in the horizontal and vertical start positions of LCD display data. As shown in Figure 60, the valid start position in the horizontal direction is set relative to HSYNC, and the length of valid data in the horizontal position is set relative to the horizontal start position of valid data. The horizontal resolution is in ENC clocks. Figure 60 shows that valid data in the vertical direction is configured similar to valid data in the horizontal direction. DCLKCTL.DCKME can activate DCLK masking. Regarding horizontal start position, two sets of registers are provided as well as a pattern register.

Table 58. DCLK Masking Registers

Mark	Register	Description	Unit
1	DCLKHS.DCHS DCLKHSA.DCHS	Horizontal DCLK mask start position.	CLK
2	DCLKHR.DCHR	Horizontal DCLK mask range.	CLK
3	DCLKVS.DCVS	Vertical DCLK mask start position.	H
4	DCLKVR.DCVR	Vertical DCLK mask range.	H

Figure 60. DCLK Masking



4.4.4.4.3 Half-Rate Mode

It is possible to divide the DCLK by two. The dividing can be applied to the internal DCLK or the output DCLK. When DCLKCTL.DCKOH is 1, only the DCLK output is divided by two. Since the internal DCLK is not divided, the RGB data rate is not still changed. Therefore, this mode can be used to connect to the LCD that captures the data using both edges of DCLK. On the other hand, when DCLKCTL.DCKIH is 1, the internal DCLK is divided by two. When output dividing is not enabled, two clocks can be output per one data sample. Therefore, this mode can be used to connect to the LCD that requires data at a rate of double the clock frequency.

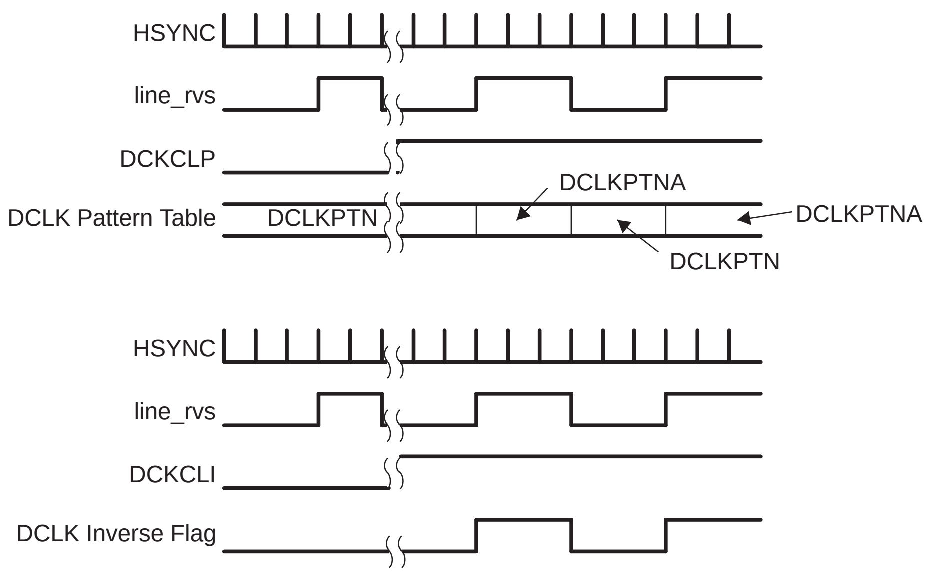
4.4.4.4.4 Line Control

The DCLK controller provides two kinds of DCLK waveform alteration by line. The culling line ID that controls RGB data output sequence also affects DCLK waveform alteration. Figure 61 shows this functionality.

- DCLK Pattern Switching. When LINECTL.DCKCLP = 1, DCLK pattern can be switched according to the culling line ID. The DCLK pattern on each line is specified by the DCLKPTN and DCLKPTNA registers.
- DCLK Polarity Inversion. When LINECTL.DCKCLI = 1, DCLK polarity is inverted on the line whose line ID is the culling line ID set by the CULLLINE register.

Both DCKCLP and DCKCLI can be set to 1, simultaneously

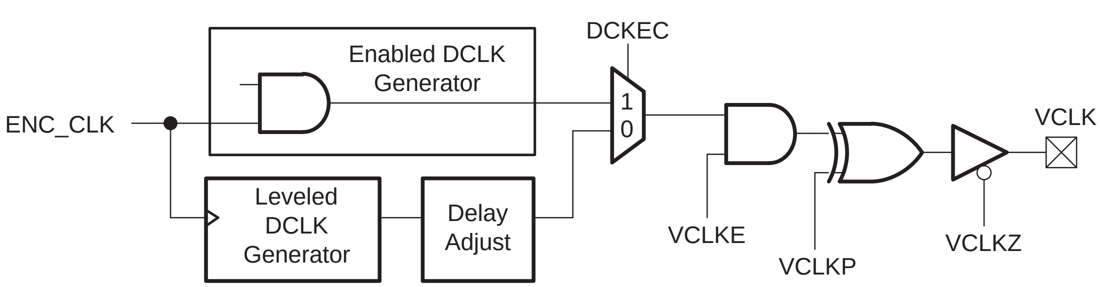
Figure 61. DCLK Pattern Switch/Inversion by Line



4.4.4.4.5 DCLK Output

VCLK output attributes, such as output enable, polarity and clock output on/off, can be controlled by registers in VIDCTL. Moreover, the level type DCLK output can have the offset of -0.5, 0.5 or 1.0 ENC CLK as set by DCLKCTL.DOFST. Figure 62 shows the DCLK output block

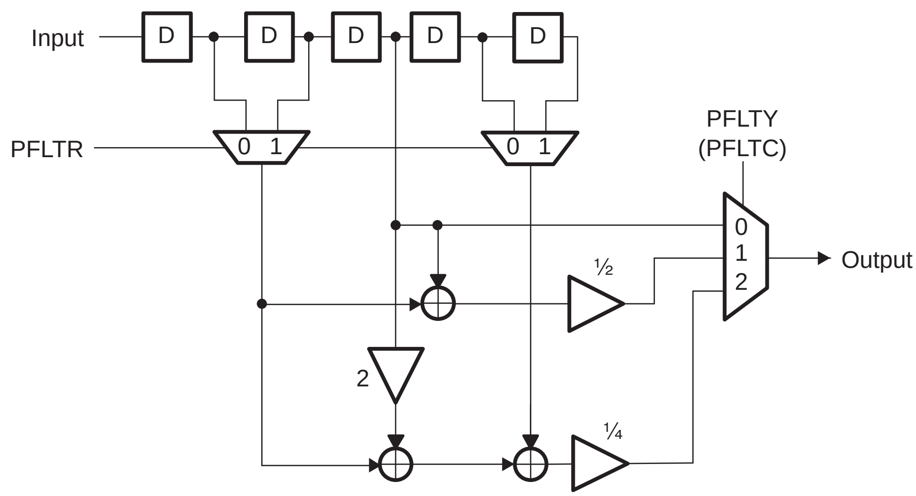
Figure 62. DCLK Output



4.4.4.5 YCbCr Pre-Filter

The Video Encoder inputs data from the OSD module in YCbCr format. A YCbCr filter (Figure 63) resides in the beginning of the data path. Each component (Y, Cb and Cr) has its own filter. The filter length can be programmed to 2 or 3 taps by PFLTY/PFLTC for Y/C, respectively, in the VDPRO register. The pre-filter sampling rate can be chosen to be either VENC clock or 1/2 VENC clock by VDPRO.PFLTR.

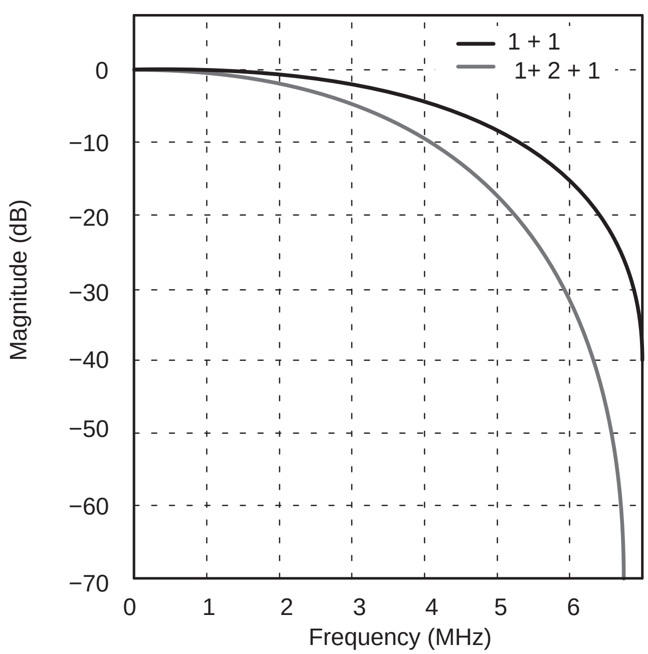
Figure 63. YCbCr Pre-Filter



The pre-filter frequency response with the sampling rate of 13.5 MHz is shown in Figure 64.

The group delay of the filter is 1 when PFLTY/PFLTC = 0 or 2, and 0.5 for PFLTY/PFLTC = 1. Do not set PFLTY and PFLTC to different values or Y and C will not be aligned.

Figure 64. Frequency Response of the Pre-Filter



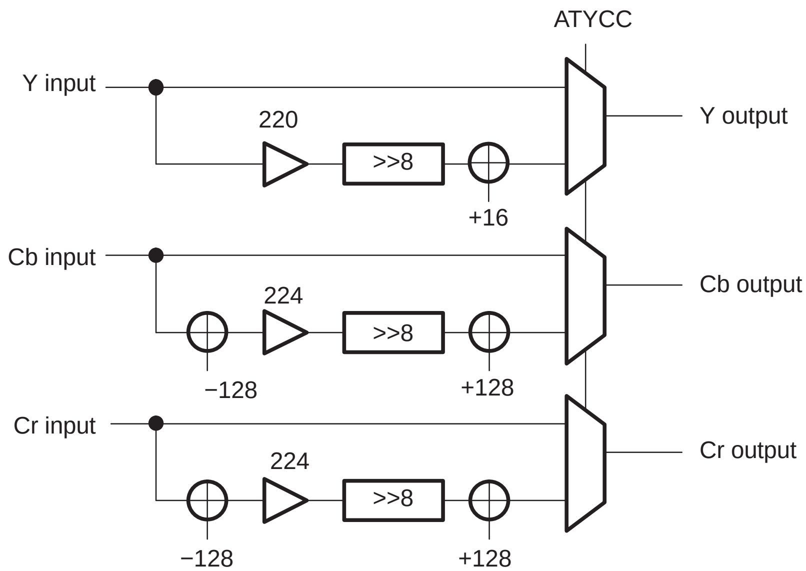
4.4.4.6 YCbCr Output Formatter

The YCbCr Output Formatter manages YCbCr data output in YUV16 and YUV8 modes.

4.4.4.6.1 YCbCr Conversion

YCbCr data processed by the pre-filter is then input to the YCbCr converter (Figure 65). This converter can attenuate the data with full range (0-255) levels to ITU-R BT.601 compliant levels (Y:16-235, C:16-240). The attenuation is enabled by setting VDPRO.ATYCC to 1.

Figure 65. YCbCr Conversion Block Diagram



4.4.4.6.2 16-Bit YCbCr Output Mode (YCC16)

In YCC16 mode, the Y (luma) signal is output to YOUT[7:0] at every VCLK rising edge, while Cb and Cr (chroma) are alternately multiplexed onto COUT[7:0]. For details of this output mode and the optional controls, see Section 2.2.1.

4.4.4.6.3 8-Bit YCbCr Output Mode (YCC8)

In YCC8 mode, each component of the OSD YCbCr signal is alternately output from YOUT[7:0]. For details of this output mode and the optional controls, see Section 2.2.2.

4.4.4.7 RGB Output Formatter

The RGB output formatter manages RGB data output in RGB parallel mode.

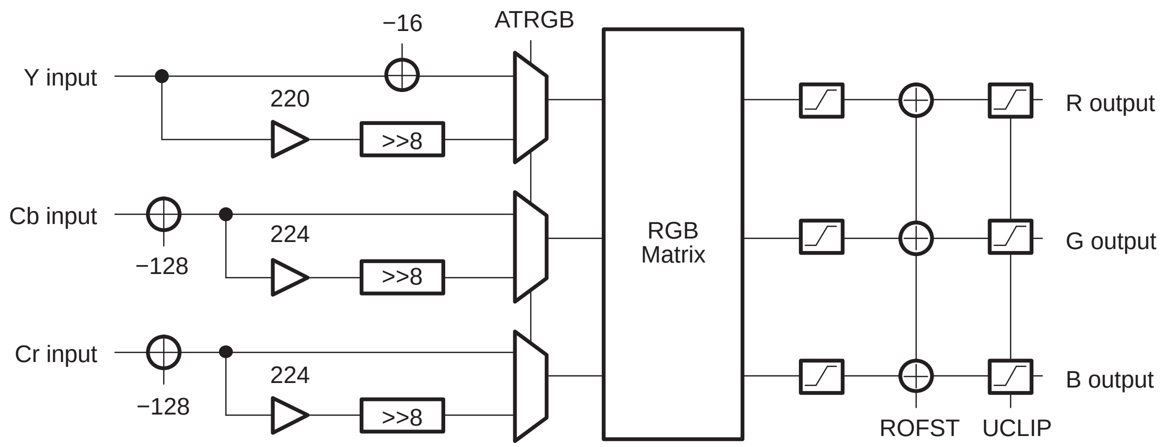
4.4.4.7.1 RGB Conversion

Figure 66 shows the block diagram of the YCbCr to RGB converter. At the first stage, YCbCr input ranging from 0-255 can be attenuated to ITU-R BT601 levels (Y:0-219, C:-128-128). This is enabled by setting VDPRO.ATRGB = 1.

The formatted YCbCr data is then converted to RGB according to the following equation:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \frac{1}{1024} \begin{bmatrix} GY & 0 & RV \\ GY & -GU & -GV \\ GY & BU & 0 \end{bmatrix} \begin{bmatrix} Y-16 \\ Cb-128 \\ Cr-128 \end{bmatrix}$$

Figure 66. RGB Conversion Block Diagram



The coefficients of the matrix can be programmed by setting the DRGBX0-DRGBX4 registers with the appropriate coefficients. By default, these values are set to the ITU-R BT601 RGB conversion matrix. RGB ranging from 0 to 219 is possible from the REC.601 formatted signal (Y:16-235, C:16-240). Since the converted RGB may become negative due to finite precision arithmetic, zero level clipping is applied.

Then the offset specified by RGBCLP.OFST is added followed by upper level clipping. The clip level is set by RGBCLP.UCLIP. The output RGB samples are limited to 8-bit resolution.

4.4.4.7.2 RGB Filter

A low-pass filter can then be applied to the converted RGB data. There is a separate LPF module for each color component, each with 8-bit inputs and outputs. For each component, either a 3-tap or a 7-tap LPF can be selected via RGBCTL.DFLTS. The sampling clock can also be chosen from the VENC clock or its divided clock by RGBCTL.DFLTR. Even though there are separate filters that operate in parallel, the user does not have individual control so these setting apply to all components.

Note: When YCbCr output is selected VMOD.VDMD = 0 or 1, (YCC16 or YCC8 modes), the RGB filters should be disabled (DFLTS = 0).

4.4.4.7.3 Parallel RGB Mode (PRGB)

In parallel RGB mode, up to 24-bit resolution data (8-bits each for RGB) can be output. By default, RGB565 can be output using the dedicated YOUT[7:0]/COUT[7:0] signals. For additional details, see Section 2.2.3. RGB666 and RGB888 output modes can also supported by assigning additional GPIO pins to the display interface. This assignment, done via the pin multiplexing, is controlled from the System Module, described in Section 2.3.

4.4.4.8 Line ID Control

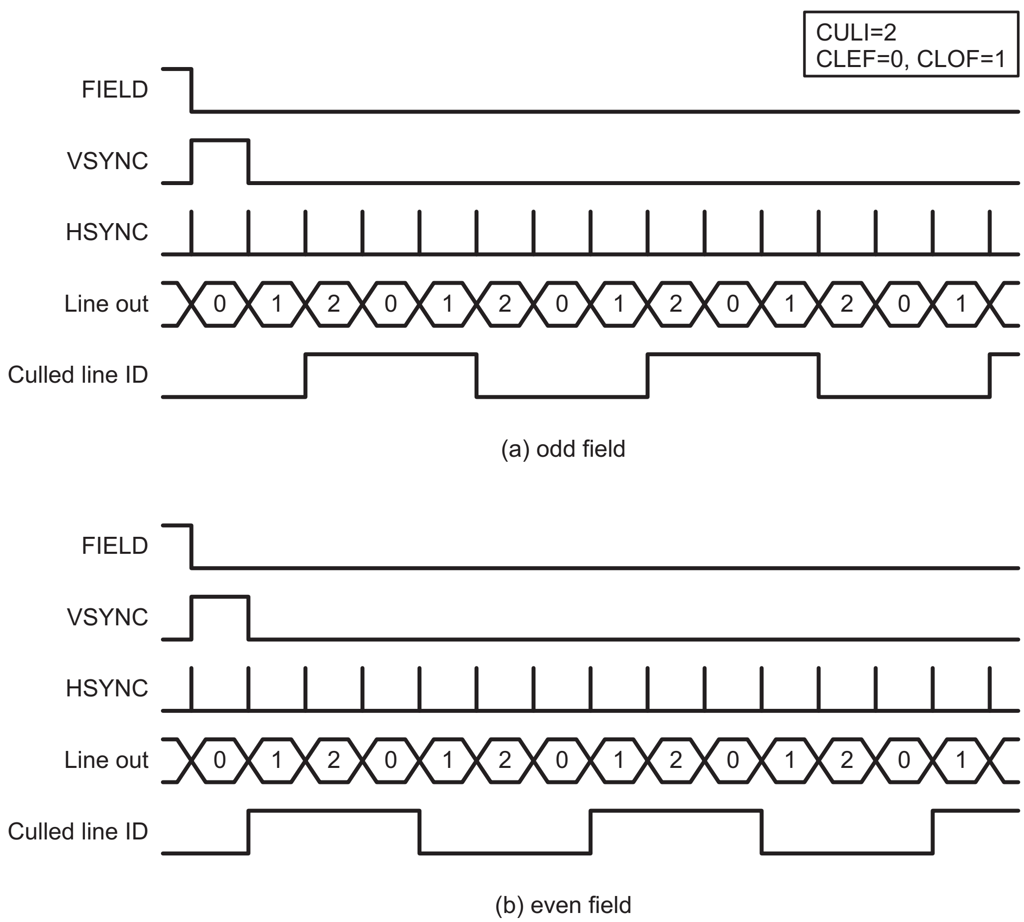
Line ID is the line identification flag altered at HSYNC and reset by VSYNC. This flag is used for the RGB rotation order selector or DCLK waveform alteration. Normally, line ID is toggled at every HSYNC. In addition to this normal behavior, the LCD controller provides a culling line ID feature. This feature enables the use of the line ID toggled by a specified line interval. You can also set the line ID toggle position within the interval for even and odd field, respectively.

The generated culled line ID in Figure 67 affects the RGB rotation order when LINECTL.RGBCL = 1. In this mode, the XORed signal of the actual line ID and the culled line ID operates as the ID for the RGB rotation order.

In addition to RGB order, the DCLK waveform can be controlled by the culled line ID. When LINECTL.DCKCLP = 1, the effective DCLK pattern register (DCLKPTN) is switched by the culled line ID. The DCLKPTN is selected for culled line ID = 0 and DCLKPTNA for 1. As well as pattern switching, a DCLK inversion feature is also provided when LINECTL.DCKCLI = 1. In this mode, the created DCLK waveform is inverted for the culled line ID = 1.

The LINECTL.LINID field can specify the start line ID in even field.

Figure 67. Culled Line ID



For PAL, the field is identified as odd when FIELD = 1.

4.4.4.9 5/6 Line Culling

The digital video output can be vertically culled of 5/6. Setting LINECTL.VCL56 to 1 activates the culling. When in this mode, one line of video output is discarded every six lines. The VENC asserts the sync for the OSD and reads data from the OSD, but ignores it for output for the culled line. HSYNC output and LCD_OE assertion are also disabled in the culled line. The line position to be culled can be controlled by the VCLRD and VCLID bits in LINECTL. See Figure 68 and Figure 69 for details of the operation. Culling is enabled on the line where the internal culling counter (remove_counter) value is equal to the VCLID bit value. The internal culling counter is incremented at hsync and reset at vsync. The reset value can be 0 or a pseudo-random value that can be selected by the VCLRD bit.

Figure 68. 5/6 Line Culling Mode

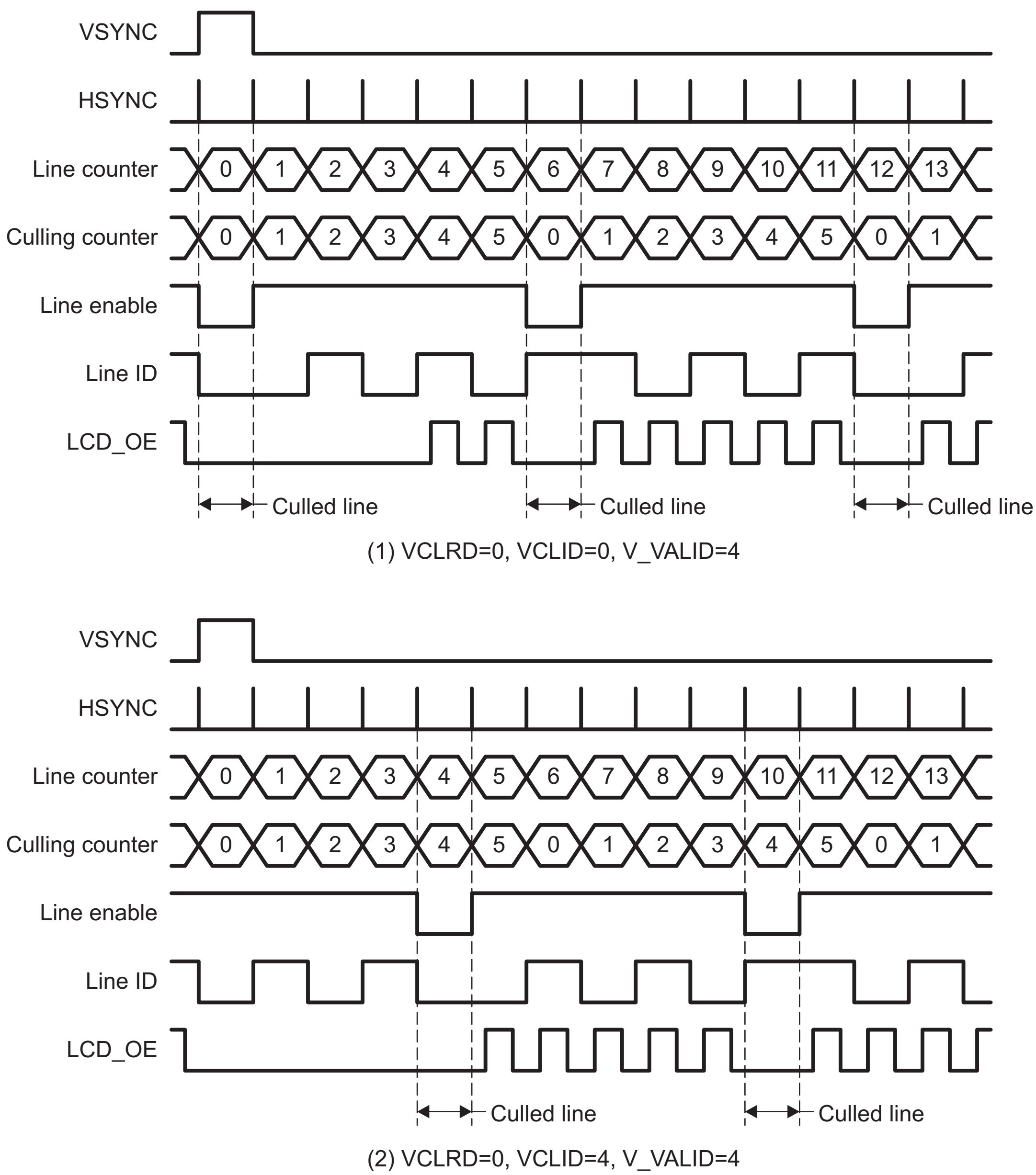
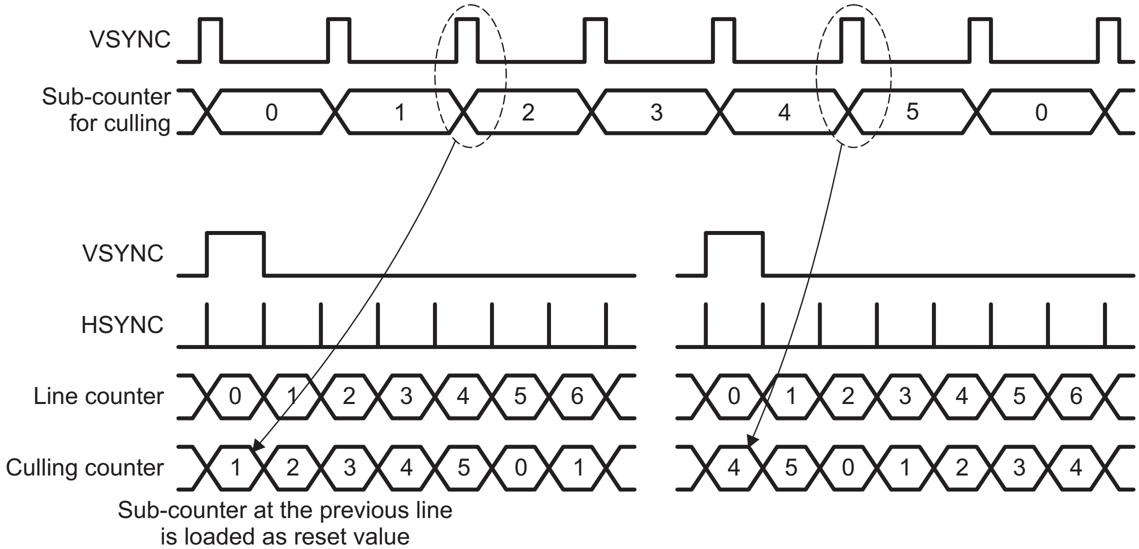


Figure 69. Random Reset of Vertical Culling Counter



4.4.4.10 Output Hold

The LCD controller provides a video output hold function. The controller can stop the operation of the timing generator when the current line or field transmission is completed. During the hold mode, reading data from the OSD is suspended and the output of the sync signals and video data is also suspended. The hold function is available only for digital video output in non-standard mode.

Setting the LINECTL.HLDL to 1 brings the controller into the line hold mode (Figure 70). Once HLDL is set, the controller automatically turns into the hold mode when the current line transmission is completed. Similarly, setting LINECTL.HLDF to 1 activates the field hold mode (Figure 71). After HLDF is set, the timing generator is suspended when the current field transmission is completed. Clearing these bits to 0 restarts the timing generator.

Figure 70. Output Line Hold Mode

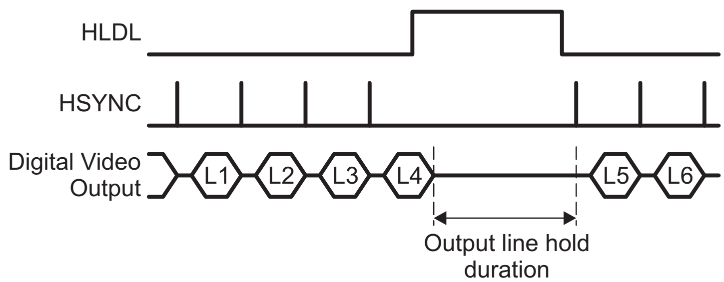
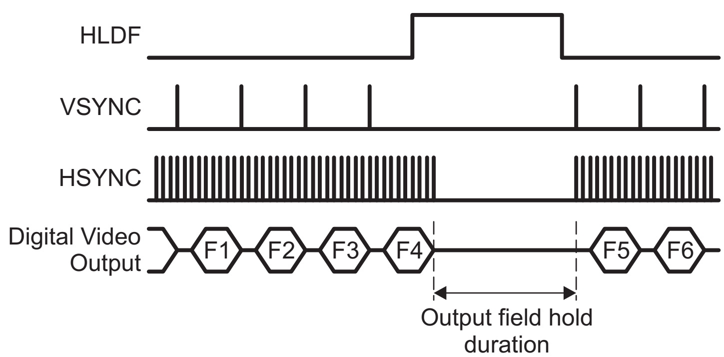


Figure 71. Output Field Hold Mode



4.4.4.11 LCD_OE Horizontal Culling

LCD_OE can be horizontally culled when HVLDCL0.HCM is 1. When in this mode, you can specify the culling period and valid pattern by HVLDCL0.HCPW and HVLDCL1.HCPT, respectively. Figure 72 shows the register usage for LCD_OE culling. Figure 73 shows an example of LCD_OE horizontal culling timing. In Figure 73, DCLK is set to be the same as CLK. Every third data is thrown away. Zero is transmitted during LCD_OE = 0.

Figure 72. LCD_OE Horizontal Culling Register

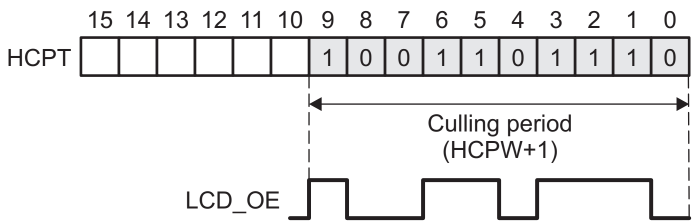
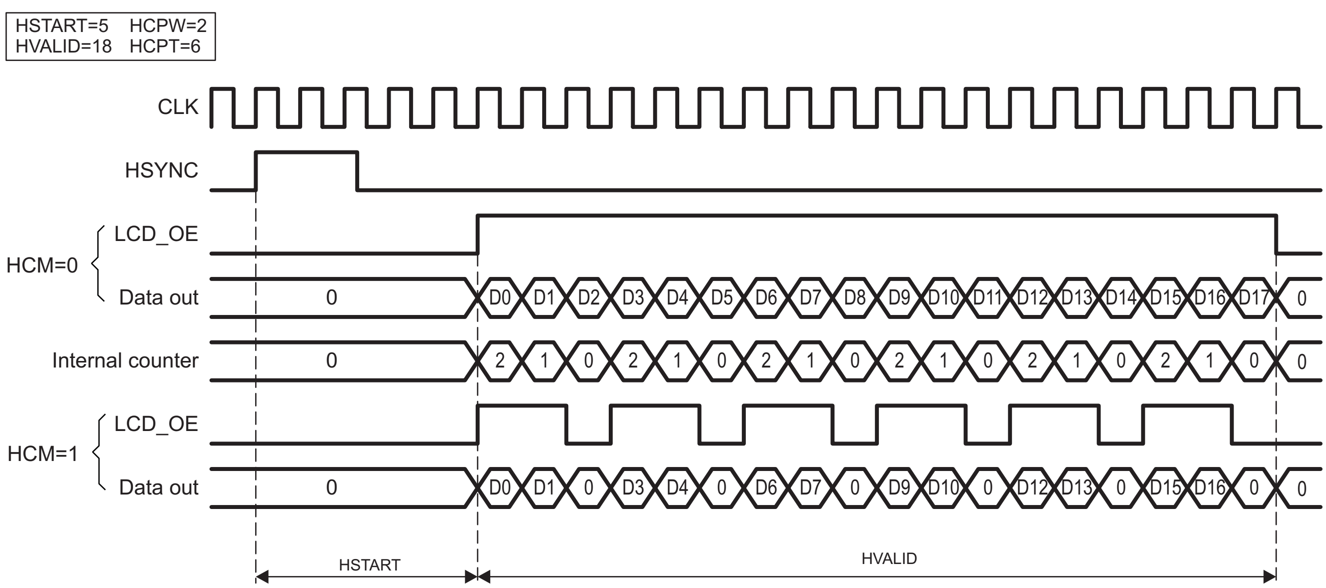


Figure 73. LCD_OE Horizontal Culling Timing Chart



4.5 Other Features

4.5.1 Internal Color Bar

The VENC can internally generate color bar by itself. Setting VDPRO.CBMD = 1 enables internal color bar generator. VDPRO.CBTYP switches the saturation of the color bar (0 = 75%, 1 = 100%).

Table 59. Digital Output Value of Color Bar Generator

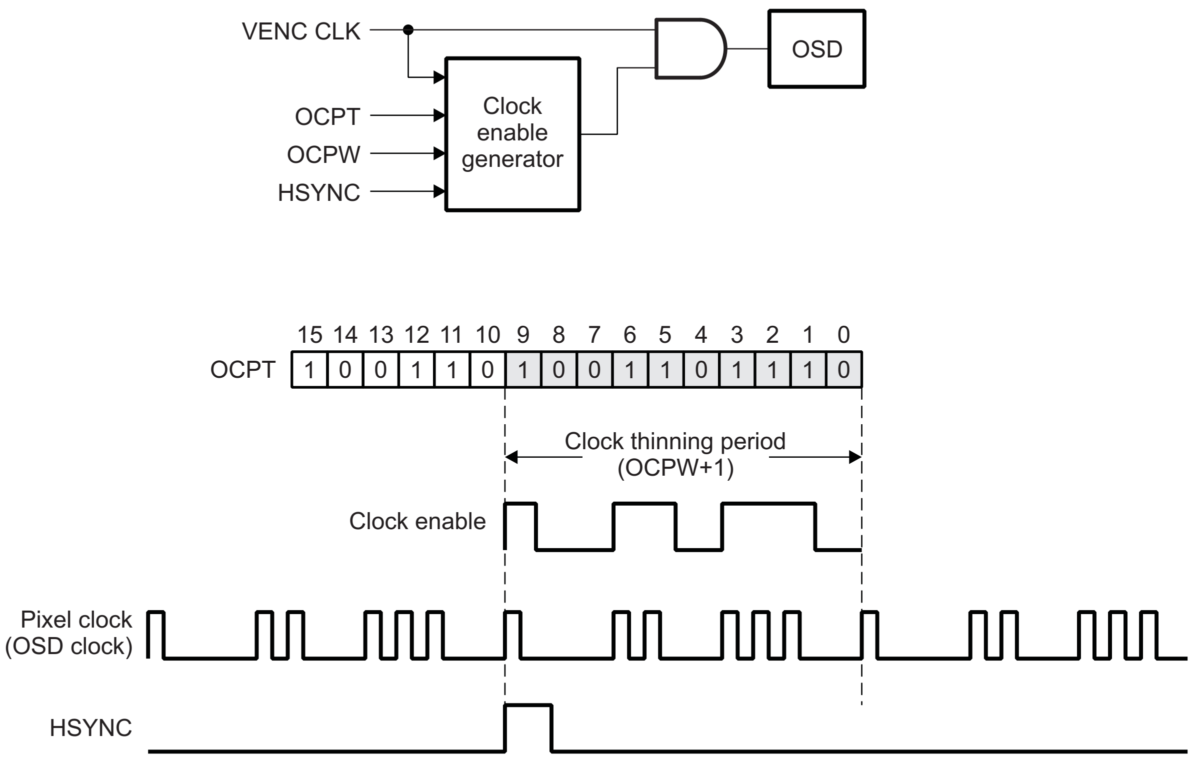
	100% (VDPRO.CBTYP = 1)			75% (VDPRO.CBTYP = 0)		
Color	**Y**	**Cb**	**Cr**	**Y**	**Cb**	**Cr**
Black	16	128	128	16	128	128
Blue	41	240	110	35	212	114
Red	81	90	240	65	100	212
Magenta	106	202	222	84	184	198
Green	145	54	34	112	72	58
Cyan	170	166	16	131	156	44
Yellow	210	16	146	162	44	142
White	235	128	128	180	128	128

4.5.2 Pixel Clock Programming

You can arbitrarily thin out the pixel clock that is the main clock used in the OSD module. Thinning out is processed periodically in the horizontal. In this period, you can freely program the active clock position. The period is specified by the OCPW bit in the OSD clock control 0 register (OSDCLK0) and the clock enable pattern is specified by the OCPT bit in the OSD clock control 1 register (OSDCLK1). The period of the clock gating pattern is started at HSYNC. Figure 74 shows the pixel clock thin out processing scheme.

After a reset, the OCPW bit is set to 1 and the OCPT bit is set to 2h so that the resulted pixel clock becomes half of VENC CLK (when VENC CLK is 27 MHz, the pixel clock becomes 13.5 MHz). For NTSC/PAL use, there is no change of these registers from the default value. It is required to clear the OCPW bit to 0 and set the OCPT bit to 1 for progressive scan output.

Figure 74. Thinning Out Pixel Clock



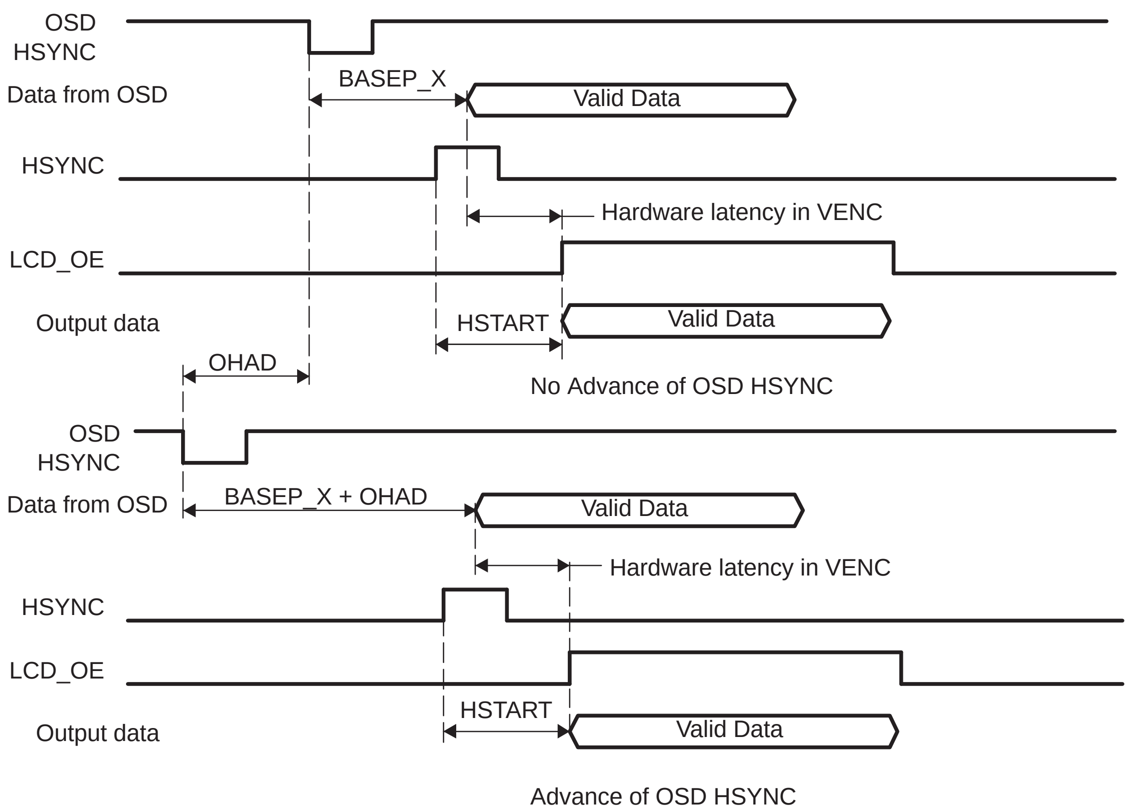
4.5.3 OSD Sync Control

4.5.3.1 Advanced Horizontal Sync

The VENC provides the sync signals to the OSD module. The horizontal sync timing is controlled by the VENC hardware so that horizontal data start position is aligned between VENC and OSD when HSTART and BASEP_X (OSD register) have same value (when OSD CLK is set to VENC CLK itself without gating). This horizontal sync timing can be advanced by OSDHADV. OHAD. The assertion timing can be 0 to 127 VENC CLK ahead of the original timing. This feature is useful when OSD does not have enough margin to prepare the first data in specified BASEP_X value due to SDRAM bandwidth limitation. In such a case, if user advances the OSD horizontal sync, it will relax the latency for OSD to prepare the first data. Figure 75 shows the OSD horizontal sync advanced feature.

Note that OSD sync signals are low active.

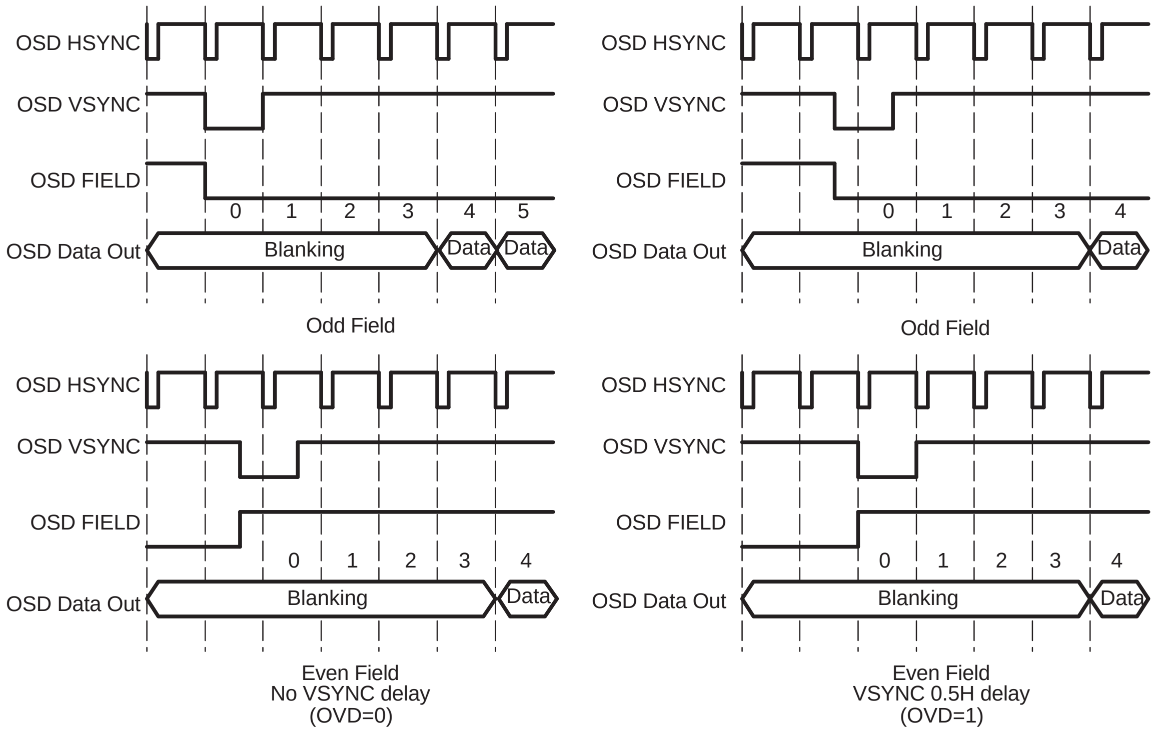
Figure 75. Advanced OSD HSYNC



4.5.3.2 0.5H Delay Vertical Sync

The vertical sync assertion for OSD can be delayed 0.5H by setting SYNCCTL.OVD to 1. This can modify the OSD data start line in odd field. The difference is shown in Figure 76. For PAL, OVD is automatically set to 1.

Figure 76. OSD VSYNC 0.5H Delay



4.5.4 Field ID Monitor

User can read the current field ID status from VSTAT.FIDST. The field status that can be seen from this bit is the field ID provided to the OSD module.

4.5.5 Interrupt

VENC asserts an interrupt at every VSYNC assertion. When the OSD module receives a vertical sync pulse from VENC, it updates its internal configuration registers. The interrupt assertion immediately follows this register update.

5 Programming Model

5.1 Setup for Typical Configuration

A typical configuration of the VPBE would be standard mode timing in master mode which would support analog NTSC/PAL SDTV output via the integrated Video DACs and also could support digital LCD display devices if they, in turn, supported standard mode timing.

5.2 Resetting the VPBE Subsystem

The entire VPSS subsystem (VPFE and VPBE) can be reset via the Power and Sleep Controller (PSC).

5.3 Configuring the Clocks and the Control Signals

The VPBE/VENC clock must be configured for proper operation of the desired display mode. For more information, see Section 3.1.1. Also note that an external clock (VPBECLK) is required to support HDTV (720p/1080i) output rates of digital data suitable for driving a High-Definition Video Encoder.

Prior to programming or enabling the VENC, the hardware must be properly configured via register writes. Table 60 shows the VPBE global registers. You must use care to address the requirement listed here before programming the OSD/VENC modules.

Table 60. VPBE Global Registers for Hardware Setup

Register.Field	Description	Notes
PID.TID	Peripheral Identification	Read only
PID.CID	Class Identification	Read only
PID.PREV	Peripheral Revision Number	Read only
PCR.VENC_DIV	Video Encoder Clock Divisor	Enable clock divisor for VENC if 54 MHz DAC mode is used
PCR.CLK_OFF	Gate VPBE Clocks for Power Savings	Enable clocks before accessing any other OSD or VENC registers

5.4 Programming the On-Screen Display (OSD)

This section discusses issues related to the software control of the on-screen display (OSD) module. It lists registers that are required to be programmed in different modes, how to enable and disable OSD window displays, discusses the different register access types, and enumerates several programming constraints.

5.4.1 Hardware Setup/Initialization

This section discusses the configuration of the OSD required before the module can be used. Note that in addition to this initialization, the OSD module must also be configured and enabled prior to enabling the VENC module before any display output is produced by the DM643x DMP.

5.4.1.1 Reset Behavior

Upon hardware reset of the VPSS, all of the registers in the OSD are initialized to their reset values. However, since the OSD RAM Color Look-Up Table is stored in internal RAM, its content does not have reset values. If the reset is a chip-level power-on reset (reset after power is applied), then the contents of these tables are unknown. If the reset is a VPSS module reset (when power remains active) then the contents of the RAM CLUT remains the same as before the reset.

5.4.1.2 Hardware Setup

Prior to enabling the OSD, the hardware must be properly configured via register writes. Table 61 identifies the register parameters that must be programmed before enabling the OSD. Note that the default settings may be appropriate values so explicit register write may not be needed to all indicated registers/fields.

Table 61. OSD Hardware Setup

Function	Configuration Required	Description
Global Configuration	MODE.CS	CB/CY order
	MODE.FSINV	Field signal inverse
	MODE.VVRSZ	Video window vertical 9/8 resize
	MODE.VHRSZ	Video window horizontal 6/5 resize
	MODE.OVRSZ	Bitmap window vertical 9/8 resize
	MODE.OHRSZ	Bitmap window horizontal 6/5 resize
Background color	MODE.BCLUT	Background CLUT (ROM/RAM)
	MODE.CABG	Background color
OSD display frame	BASEPX	Base pixel X
	BASEPY	Base pixel Y
ROM CLUT	MISCCTL.RSEL	ROM CLUT selection
RGB565 Transparency	TRANSPVAL.RGBTRANS	RGB565 Transparency value

5.4.1.3 Color Look-Up Table Setup

The User defined RAM Color Look-Up Table (CLUT) must be programmed before is can be used. For additional details, see Section 4.3.5.1.

5.4.1.4 Window Setup

Before an individual window can be displayed, appropriate data must be made available in DDR2 and the appropriate window settings be made. The data formats are described above and the window configuration settings are described in Table 62.

Table 62. OSD Window Configuration

Function	Configuration Options
All Windows	Position offset relative to BASEPX/Y
	Window display size
	DDR2 data pointer
	DDR2 Offset (size in 32-byte increments of each data line)
	Field/Frame settings
	Horizontal/vertical Zoom factor
Video Windows	Expansion filter coefficient settings
	Window display data (that is, 24-bit RGB data in MISCCTL, if used)
	Ping-pong settings (Video Window 0 only)

Table 62. OSD Window Configuration (continued)

Function	Configuration Options
Bitmap Windows	YUV attenuation enable
	RGB565 display mode (one window only)
	CLUT selection (ROM/RAM)
	Bitmap Data width (1,2,4, or 8)
	CLUT mapping if bit depth < 8-bits
	Blend factor
	Transparency enable
Attribute Window	Blinking (ON/OFF)
	Blink Rate
Cursor Window	Size
	Thickness
	Color

5.4.2 Enable/Disable Hardware

Note: The OSD windows should be enabled prior to enabling the VENC (VMOD.VENC = 1).

The OSD has no separate hardware enable/disable but each window has a separate display enable/disable (Table 63).

Table 63. OSD Window Enable/Disable

Window	Display Enable
Video Window 0	VIDWINMD.ACT0
Video Window 0	VIDWINMD.ACT1
Bitmap Window 0	OSDWIN0MD.OACT0
Bitmap Window 1	OSDWIN1MD.OACT1
Attribute Window	None – always active when in attribute mode
Cursor Window	RECTCUR.RCACT

5.4.3 Events and Status Checking

The VPBE generates a frame sync interrupt. This can be used as a trigger to update any frame dependent registers. The OSD generates no events or status other than the indicator that a CLUT write is pending.

5.4.4 Register Accessibility During Frame Display

Some registers/fields are shadowed during the frame display time and any writes to these locations are not applied until the next frame period. These are noted in Table 64.

Table 64. OSD Window Registers/Field Shadowing

Register.Field	Description
MODE.CS	Cb/Cr or Cr/Cb Format
MODE.OVRSZ	OSD Window Vertical Expansion Enable
MODE.OHRSZ	OSD Window Horizontal Expansion Enable
MODE.EF (1)	Expansion Filter Enable
MODE.VVRSZ (1)	Video Window Vertical Expansion Enable
MODE.VHRSZ (1)	Video Window Horizontal Expansion Enable
MODE.FSINV (1)	Field Signal Inversion
MODE.BCLUT (1)	Background CLUT Selection
MODE.CABG	Background Color CLUT
VIDWINMD.V1EFC	Video Window 1 Expansion Filter Coefficient
VIDWINMD.VHZ1 (1)	Video Window 0 Horizontal Direction Zoom
VIDWINMD.VVZ1 (1)	Video Window 0 Vertical Direction Zoom
VIDWINMD.VFF1 (1)	Video Window 0 Display Mode
VIDWINMD.ACT1 (1)	Sets Image Display On/Off Video Window 0
VIDWINMD.V0EFC	Video Window 0 Expansion Filter Coefficient
VIDWINMD.VHZ0 (1)	Video Window 0 Horizontal Direction Zoom
VIDWINMD.VVZ0 (1)	Video Window 0 Vertical Direction Zoom
VIDWINMD.VFF0 (1)	Video Window 0 Display Mode
VIDWINMD.ACT0 (1)	Sets Image Display On/Off Video Window 0
OSDWIN0MD.RGB0E	RGB Input for Window 0 Enable
OSDWIN0MD.CLUTS0 (1)	CLUT Select for OSD Window 0
OSDWIN0MD.OHZ0 (1)	OSD Window 0 Horizontal Zoom
OSDWIN0MD.OVZ0 (1)	OSD Window 0 Vertical Zoom
OSDWIN0MD.BMW0 (1)	Bitmap Bit Width for OSD Window 0
OSDWIN0MD.BLND0 (1)	Blending Ratio for OSD Window 0
OSDWIN0MD.TE0 (1)	Transparency Enable for OSD Window 0
OSDWIN0MD.OFF0 (1)	OSD Window 0 Display Mode
OSDWIN0MD.OACT0 (1)	OSD Window 0 Active (displayed)
OSDWIN1MD.OASW (1)	OSD Window 1 Attribute Mode Enable
OSDWIN1MD.RGB1E	RGB Input for Window 1 Enable
OSDWIN1MD.CLUTS1	CLUT Select for OSD Window 1
OSDWIN1MD.OHZ1 (1)	OSD Window 1 Horizontal Zoom
OSDWIN1MD.OVZ1 (1)	OSD Window 1 Vertical Zoom
OSDWIN1MD.BMW1 (1)	Bitmap Bit Width for OSD Window 1
OSDWIN1MD.BLND1 (1)	Blending Ratio for OSD Window 1
OSDWIN1MD.TE1 (1)	Transparency Enable for OSD Window 1
OSDWIN1MD.OFF1 (1)	OSD Window 1 Display Mode
OSDWIN1MD.OACT1 (1)	OSD Window 1 Active (displayed)
OSDATRMD.OASW (1)	OSD Window 1 Attribute Mode Enable
OSDATRMD.OHZA (1)	OSD Attribute Window Horizontal Zoom
OSDATRMD.OVZA (1)	OSD Window 0 or Attribute Window Vertical Zoom

(1) This register/field is shadowed during the frame display time and any writes to this location is not applied until the next frame period.

Table 64. OSD Window Registers/Field Shadowing (continued)

Register.Field	Description
OSDATRMD.BLNKINT[(1)]	Blinking Interval
OSDATRMD.OFFA[(1)]	OSD Attribute Window Display Mode
OSDATRMD.BLNK[(1)]	OSD Attribute Window Blink Enable
RECTCUR.RCAD	Rectangular Cursor Color Palette Address
RECTCUR.CLUTSR[(1)]	CLUT Select
RECTCUR.RCHW[(1)]	Rectangular Cursor Horizontal Line Width
RECTCUR.RCVW[(1)]	Rectangular Cursor Vertical Line Width
RECTCUR.RCACT[(1)]	Rectangular Cursor Active (displayed)
VIDWIN0OFST.V0LO[(1)]	Video Window 0 Line Offset
VIDWIN1OFST.V1LO[(1)]	Video Window 1 Line Offset
OSDWIN0OFST.O0LO[(1)]	OSD Window 0 Line Offset
OSDWIN1OFST.O1LO[(1)]	OSD Window 1 Line Offset
VIDWIN0ADR.VIDWIN0ADR[(1)]	Video Window 0 SDRAM Source Address
VIDWIN1ADR.VIDWIN1ADR[(1)]	Video Window 1 SDRAM Source Address
OSDWIN0ADR.OSDWIN0ADR[(1)]	OSD Window 0 SDRAM Source Address
OSDWIN1ADR.OSDWIN1ADR[(1)]	OSD Window 1 SDRAM Source Address
BASEPX.BPX[(1)]	Base Pixel in X
BASEPY.BPY[(1)]	Base Pixel(Line) in Y
VIDWIN0XP.V0X[(1)]	Video Window 0 X-Position
VIDWIN0YP.V0Y[(1)]	Video Window 0 Y-Position
VIDWIN0XL.V0W[(1)]	Video Window 0 X-Width
VIDWIN0YL.V0H[(1)]	Video Window 0 Y-Height
VIDWIN1XP.V1X[(1)]	Video Window 1 X-Position
VIDWIN1YP.V1Y[(1)]	Video Window 1 Y-Position
VIDWIN1XL.V1W[(1)]	Video Window 1 X-Width
VIDWIN1YL.V1H[(1)]	Video Window 1 Y-Height
OSDWIN0XP.W0X[(1)]	OSD Window 0 X-Position
OSDWIN0YP.W0Y[(1)]	OSD Window 0 Y-Position
OSDWIN0XL.W0W[(1)]	OSD Window 0 X-Width
OSDWIN0YL.W0H[(1)]	OSD Window 0 Y-Height
OSDWIN1XP.W1X[(1)]	OSD Window 1 X-Position
OSDWIN1YP.W1Y[(1)]	OSD Window 1 Y-Position
OSDWIN1XL.W1W[(1)]	OSD Window 1 X-Width
OSDWIN1YL.W1H[(1)]	OSD Window 1 Y-Height
CURXP.RCSX[(1)]	Rectangular Cursor Window X-Position
CURYP.RCSY[(1)]	Rectangular Cursor Window Y-Position
CURXL.RCSW[(1)]	Rectangular Cursor Window X-Width
CURYL.RCSH[(1)]	Rectangular Cursor Window Y-Height
W0BMP01.PAL01	Palette Address for Bitmap Value [1,x,x] - OSD Window 0
W0BMP01.PAL00	Palette Address for Bitmap Value [0,0,0] - OSD Window 0
W0BMP23.PAL03	Palette Address for Bitmap Value [3,x,x] - OSD Window 0
W0BMP23.PAL02	Palette Address for Bitmap Value [2,x,x] - OSD Window 0
W0BMP45.PAL05	Palette Address for Bitmap Value [5,1,x] - OSD Window 0
W0BMP45.PAL04	Palette Address for Bitmap Value [4,x,x] - OSD Window 0
W0BMP67.PAL07	Palette Address for Bitmap Value [7,x,x] - OSD Window 0
W0BMP67.PAL06	Palette Address for Bitmap Value [6,x,x] - OSD Window 0

Table 64. OSD Window Registers/Field Shadowing (continued)

Register.Field	Description
W0BMP89.PAL09	Palette Address for Bitmap Value [9,x,x] - OSD Window 0
W0BMP89.PAL08	Palette Address for Bitmap Value [8,x,x] - OSD Window 0
W0BMPAB.PAL11	Palette Address for Bitmap Value [B,x,x] - OSD Window 0
W0BMPAB.PAL10	Palette Address for Bitmap Value [A,2,x] - OSD Window 0
W0BMPCD.PAL13	Palette Address for Bitmap Value [D,x,x] - OSD Window 0
W0BMPCD.PAL12	Palette Address for Bitmap Value [C,x,x] - OSD Window 0
W0BMPEF.PAL15	Palette Address for Bitmap Value [F,3,1] - OSD Window 0
W0BMPEF.PAL14	Palette Address for Bitmap Value [E,x,x] - OSD Window 0
W1BMP01.PAL01	Palette Address for Bitmap Value [1,x,x] - OSD Window 1
W1BMP01.PAL00	Palette Address for Bitmap Value [0,0,0] - OSD Window 1
W1BMP23.PAL03	Palette Address for Bitmap Value [3,x,x] - OSD Window 1
W1BMP23.PAL02	Palette Address for Bitmap Value [2,x,x] - OSD Window 1
W1BMP45.PAL05	Palette Address for Bitmap Value [5,1,x] - OSD Window 1
W1BMP45.PAL04	Palette Address for Bitmap Value [4,x,x] - OSD Window 1
W1BMP67.PAL07	Palette Address for Bitmap Value [7,x,x] - OSD Window 1
W1BMP67.PAL06	Palette Address for Bitmap Value [6,x,x] - OSD Window 1
W1BMP89.PAL09	Palette Address for Bitmap Value [9,x,x] - OSD Window 1
W1BMP89.PAL08	Palette Address for Bitmap Value [8,x,x] - OSD Window 1
W1BMPAB.PAL11	Palette Address for Bitmap Value [B,x,x] - OSD Window 1
W1BMPAB.PAL10	Palette Address for Bitmap Value [A,2,x] - OSD Window 1
W1BMPCD.PAL13	Palette Address for Bitmap Value [D,x,x] - OSD Window 1
W1BMPCD.PAL12	Palette Address for Bitmap Value [C,x,x] - OSD Window 1
W1BMPEF.PAL15	Palette Address for Bitmap Value [F,3,1] - OSD Window 1
W1BMPEF.PAL14	Palette Address for Bitmap Value [E,x,x] - OSD Window 1
MISCCTL.VFINV	Video Window 0/1 Expansion Filter Coefficient Inverse
MISCCTL.ATN0E	Attenuation Enable for REC601
MISCCTL.ATN1E	Attenuation Enable for REC601
MISCCTL.RGBEN	Video Window RGB Mode Enable
MISCCTL.RGBWIN	Video Window to Use for RGB Mode
MISCCTL.RSEL	CLUT ROM Selection
MISCCTL.CPBSY	CLUT Write Busy
MISCCTL.PPSW	Ping-Pong Buffer Toggle Select
MISCCTL.PPRV	Ping Pong Buffer Reverse
CLUTRAMYCB.Y	Write Data (Y) Into Built-In CLUT RAM
CLUTRAMYCB.CB	Write Data (Cb) Into Built-In CLUT RAM
CLUTRAMCR.CR	Write Data (Cr) Into Built-In CLUT RAM
CLUTRAMCR.CADDR	CLUT Write Pallette Address
TRANSPVAL.RGBTRANS	OSD Window Transparency Value for RGB565 Input Mode
PPVWIN0ADR.PPVWIN0ADR [(1)]	Ping-Pong Video Window 0 Address

5.4.5 Summary of Constraints

The following restrictions exist in the OSD module.

- Both the OSD windows and VIDWIN1 should be fully contained inside VIDWIN0. This means that both the Y and X position of either the OSD windows or VIDWIN1 should be greater (not equal) to the Y and X position of VIDWIN0.
- If the vertical resize filter is enabled for either of the video windows, the maximum horizontal window dimension cannot be greater than 720 currently. This is due to the limitation in the size of the line memory.
- It is not possible to use both of the CLUT ROMs at the same time. However, a window can use RAM while another chooses ROM.
- The 24-bit RGB input mode is only valid for one of the two video windows (programmable) and does not apply to the OSD windows.

5.5 Programming the VENC

This section discusses issues related to the software control of the VENC module (Video Encoder/Digital LCD Controller). It lists registers that are required to be programmed in different modes, how to enable and disable the VENC, discusses the different register access types, and enumerates several programming constraints.

5.5.1 Hardware Setup/Initialization

This section discusses the configuration of the VENC module required before the module can be used. Note that in addition to this initialization, the OSD module must also be configured and enabled prior to enabling the VENC module before any display output is produced by the DM643x DMP.

5.5.1.1 Reset Behavior

Upon hardware reset of the VPSS, all of the registers in the VENC are reset to their reset values. If the reset is a chip-level power-on reset (reset after power is applied), then the contents of the RAM tables are unknown. If the reset is a VPSS module reset (when power remains active) then the contents of the RAM table remains the same as before the reset.

5.5.1.2 Hardware Setup

Prior to enabling the VENC, the hardware must be properly configured via register writes. Essentially all of the VENC programming is related to hardware setup and little to no interaction is required once the desired display operating condition is set. Table 65 shows which register/field affects the available display modes.

Note that the analog output is only available in standard (NTSC/PAL) timing mode, but the digital outputs are available in either mode. Therefore, if the digital display device supports standard mode timing, the analog and digital outputs can be available simultaneously, if desired.

Table 65. VPBE Global Registers for Hardware Setup[(1)]

Register.Field	Description	Analog SDTV	Analog EDTV	YCC16	YCC8	Parallel RGB
VMOD.VDMD	Digital Video Output Mode					
VMOD.ITLCL	Non-Interlace Line Number Select	O				
VMOD.ITLC	Interlaced Scan Mode Enable	O				
VMOD.NSIT	Non-standard Interlace Mode			O	O	O
VMOD.HDMD	HDTV Mode		R			
VMOD.TVTYP	TV Format Type Select	Sets mode				
VMOD.SLAVE	Master-Slave Select	M/S		Master or Slave		
VMOD.VMD	Video Timing	Standard		Standard or Non-Standard		
VMOD.BLNK	Blanking Enable	O	O			
VMOD.VIE	Composite Analog Output Enable	O				
VMOD.VENC	Video Encoder Enable	R	R			
VIDCTL.VCLKP	VCLK Output Polarity			O	O	O
VIDCTL.VCLKE	VCLK Output Enable			R	R	R
VIDCTL.VCLKZ	VCLK Pin Output Enable			R	R	R
VIDCTL.SYDIR	Horizontal/Vertical Sync Pin I/O Control			Enable in Master mode		
VIDCTL.DOMD	Digital Data Output Mode			R	R	R
VIDCTL.YCSWAP	Swaps YOUT/COUT Pins			O	O	
VIDCTL.YCOL	YOUT/COUT Pin Output Level			O	O	
VDPRO.PFLTC	C Prefilter Select			O	O	
VDPRO.PFLTY	Y Prefilter Select			O	O	
VDPRO.PFLTR	Prefilter Sampling Frequency			O	O	
VDPRO.CBTYP	Color Bar Type	O	O			
VDPRO.CBMD	Color Bar Mode	O	O			
VDPRO.ATRGB	Input Video Attenuation Control for RGB					O
VDPRO.ATYCC	Input Video Attenuation Control for YCbCr			O	O	
VDPRO.ATCOM	Input Video Attenuation Control for Composite	O				
VDPRO.DAFRQ	DAC Operating Frequency		R			
VDPRO.DAUPS	DAC ×2 Up-Sampling Enable		O			
VDPRO.CUPS	C Signal Up-Sampling Enable	O	R			
VDPRO.YUPS	Y Signal Up-Sampling Enable	O	R			
SYNCCTL.OVD	OSD vsync Delay	O	O			
SYNCCTL.EXFMD	External Field Detection Mode			SL	SL	SL
SYNCCTL.EXFIV	External Field Input Inversion			SL	SL	SL
SYNCCTL.EXSYNC	External Sync Select			SL	SL	SL
SYNCCTL.EXVIV	External Vertical Sync Input Polarity			SL	SL	SL
SYNCCTL.EXHIV	External Horizontal Sync Input Polarity			SL	SL	SL
SYNCCTL.CSP	Composite Signal Output Polarity			SL	SL	SL
SYNCCTL.CSE	Composite Signal Output Enable			SL	SL	SL
SYNCCTL.SYSW	Output Sync Select			SL	SL	SL
SYNCCTL.VSYNCS	Vertical Sync Output Signal			SL	SL	SL
SYNCCTL.VPL	Vertical Sync Output Polarity			SL	SL	SL
SYNCCTL.HPL	Horizontal Sync Output Polarity			SL	SL	SL
SYNCCTL.SYEV	Vertical Sync Output Enable			SL	SL	SL
SYNCCTL.SYEH	Horizontal Sync Output Enable			SL	SL	SL

(1) R = Required, O = Optional, M = Master Mode, SL = Slave Mode, r = Read-Only Status

Table 65. VPBE Global Registers for Hardware Setup (continued)

Register.Field	Description	Analog SDTV	Analog EDTV	YCC16	YCC8	Parallel RGB
HSPLS.HSPLS	Horizontal Sync Pulse Width (number of ENC clocks)	M	M	M	M	M
VSPLS.VSPLS	Vertical Sync Pulse Width (number of ENC clocks)	M	M	M	M	M
HINT.HINT	Horizontal Interval (number of ENC clocks)	M	M	M	M	M
HSTART.HSTART	Horizontal Valid Data Start Position	M	M	M	M	M
HVALID.HVALID	Horizontal Data Valid Range	M	M	M	M	M
VINT.VINT	Vertical Interval (number of lines)	M	M	M	M	M
VSTART.VSTART	Vertical Valid Data Start Position	M	M	M	M	M
VVALID.VVALID	Vertical Data Valid Range	M	M	M	M	M
HSDLY.HSDLY	Output Delay of Horizontal Sync Signal	M	M	M	M	M
VSDLY.VSDLY	Output Delay of Vertical Sync Signal	M	M	M	M	M
YCCCTL.CHM	Chroma Output Mode			O	O	
YCCCTL.YCP	YC Output Order			O	O	
YCCCTL.R656	REC656 Mode (Standard Mode timing only)				O	
RGBCTL.DFLTR	RGB LPF Sampling Frequency					O
RGBCTL.DFLTS	RGB LPF Select					O
RGBCLP.UCLIP	Upper Clip Level for RGB Output					O
RGBCLP.OFST	Offset Level for RGB Output					O
LINECTL.VSTF	Vertical Data Valid Start Position Field Mode					
LINECTL.VCLID	Vertical Culling Line Position					
LINECTL.VCLRD	Vertical Culling Counter Reset Mode					
LINECTL.VCL56	Digital Output Vertical Culling					
LINECTL.HLDF	Digital Output Field Hold					
LINECTL.HLDL	Digital Output Line Hold					
LINECTL.LINID	Start Line ID Control in Even Field					
LINECTL.DCKCLP	DCLK Pattern Switching by Culling Line ID					
LINECTL.DCKCLI	DCLK Polarity Inversion by Culling Line ID					
LINECTL.RGBCL	RGB Output Order Switching by Culling Line ID					
CULLLINE.CLOF	Culling Line ID Toggle Position (Odd field)					
CULLLINE.CLEF	Culling Line ID Toggle Position (Even field)					
CULLLINE.CULI	Culling Line ID Inversion Interval					
LCDOUT.FIDS	Output Signal Select					O
LCDOUT.FIDP	Field ID Output Polarity					O
LCDOUT.PWMP	PWM Output Pulse Polarity					O
LCDOUT.PWME	PWM Output Control					O
LCDOUT.ACE	LCD_AC Output Control					O
LCDOUT.BRP	BRIGHT Output Polarity					O
LCDOUT.BRE	BRIGHT Output Control					O
LCDOUT.OEP	LCD_OE Output Polarity			O	O	O
LCDOUT.OEE	LCD_OE Output Control			O	O	O
BRTS.BRTS	BRIGHT Pulse Start Position					O
BRTW.BRTW	BRIGHT Pulse Width					O
ACCTL.ACTF	LCD_AC Toggle Interval					O

Table 65. VPBE Global Registers for Hardware Setup (continued)

Register.Field	Description	Analog SDTV	Analog EDTV	YCC16	YCC8	Parallel RGB
ACCTL.ACTH	LCD_AC Toggle Horizontal Position					O
PWMP.PWMP	PWM Output Period					O
PWMW.PWMW	PWM Output Pulse Width					O
DCLKCTL.DCKIM	DCLK Internal Mode					
DCLKCTL.DOFST	DCLK Output Offset					
DCLKCTL.DCKEC	DCLK Pattern Mode					R
DCLKCTL.DCKME	DCLK Mask Control					
DCLKCTL.DCKOH	DCLK Output Divide					
DCLKCTL.DCKIH	Internal DCLK Output Divide					
DCLKCTL.DCKPW	DCLK Pattern Valid Bit Width					R
DCLKPTN0.DCPTN0	DCLK Pattern					R
DCLKPTN1.DCPTN1	DCLK Pattern					R
DCLKPTN2.DCPTN2	DCLK Pattern					R
DCLKPTN3.DCPTN3	DCLK Pattern					R
DCLKPTN0A.DCPTN0A	DCLK Pattern (auxiliary)					
DCLKPTN1A.DCPTN1A	DCLK Pattern (auxiliary)					
DCLKPTN2A.DCPTN2A	DCLK Pattern (auxiliary)					
DCLKPTN3A.DCPTN3A	DCLK Pattern (auxiliary)					
DCLKHS.DCHS	Horizontal DCLK Mask Start Position					
DCLKHSA.DCHS	Horizontal DCLK (auxiliary) Mask Start Position					
DCLKHR.DCHR	Horizontal DCLK Mask Range					
DCLKVS.DCVS	Vertical DCLK Mask Start Position					
DCLKVR.DCVR	Vertical DCLK Mask Range					
CAPCTL.CADF	Closed Caption Default Data Register	O	O			
CAPCTL.CAPF	Closed Caption Field Select	O	O			
CAPDO.CADO0	Closed Caption Default Data0 (odd field)	O	O			
CAPDO.CADO1	Closed Caption Default Data1 (odd field)	O	O			
CAPDE.CADE0	Closed Caption Default Data0 (even field)	O	O			
CAPDE.CADE1	Closed Caption Default Data1 (even field)	O	O			
ATR0.ATR0	Video Attribute Data Register 0	O	O			
ATR1.ATR1	Video Attribute Data Register 1	O	O			
ATR2.ATR2	Video Attribute Data Register 2	O	O			
VSTAT.CAEST	Closed Caption Status (even field)	r	r			
VSTAT.CAOST	Closed Caption Status (odd field)	r	r			
VSTAT.FIDST	Field ID Monitor	r	r	r	r	r
VSTAT.UDBAL	uDisplay 'Balance Signal' Monitor					
VSTAT.UDFUL	uDisplay 'Full' Signal Monitor					
DACTST.DAPD3	DAC3 Power-Down	O	O			
DACTST.DAPD2	DAC2 Power-Down	O	O			
DACTST.DAPD1	DAC1 Power-Down	O	O			
DACTST.DAPD0	DAC0 Power-Down	O	O			
YCOLVL.YLVL	YOUT DC Level			O	O	
YCOLVL.CLVL	COUT DC Level			O	O	
SCPROG.SCSD	Sub-Carrier Initial Phase Value	O	O			

Table 65. VPBE Global Registers for Hardware Setup (continued)

Register.Field	Description	Analog SDTV	Analog EDTV	YCC16	YCC8	Parallel RGB
CVBS.YCDLY	Delay Adjustment of Y Signal in Composite Signal	O				
CVBS.CVLVL	Composite Video Level (sync/white)	O				
CVBS.CSTUP	Setup Level at NTSC Output	O				
CVBS.CBLS	Blanking Shape Disable	O				
CVBS.CBBLD	Blanking Build-Up Time for Composite Output	O				
CVBS.CSBLD	Sync Build-Up Time for Composite Output	O				
CMPNT.MRGB	RGB Mode Select for Component Output		O			
CMPNT.MYDLY	Delay Adjustment of Y Signal in Component Mode		O			
CMPNT.MSYR	Sync on Pr (or R)		O			
CMPNT.MSYB	Sync on Pb (or B)		O			
CMPNT.MSYG	Sync on Y (or G)		O			
CMPNT.MCLVL	Chroma Level for Component YPbPr		O			
CMPNT.MYLVL	Luma Level (sync/white) for Component YPbPr		O			
CMPNT.MSTUP	Setup for Component YPbPr		O			
CMPNT.MBLS	Blanking Shape Disable		O			
CMPNT.MBBLD	Blanking Build-Up Time for Component Output		O			
CMPNT.MSBLD	Sync Build-Up Time for Component Output		O			
ETMG0.CEPW	Equalizing Pulse Width Offset for Composite Output	O				
ETMG0.CFSW	Field Sync Pulse Width Offset for Composite Output	O				
ETMG0.CLSW	Line Sync Pulse Width Offset for Composite Output	O				
ETMG1.CBSE	Burst End Position Offset for Composite Output	O				
ETMG1.CBST	Burst Start Position Offset for Composite Output	O				
ETMG1.CFPW	Front Porch Position Offset for Composite Output	O				
ETMG1.CLBI	Line Blanking End Position Offset for Composite Output	O				
ETMG2.MEPW	Equalizing Pulse Width Offset for Component Output		O			
ETMG2.MFSW	Field Sync Pulse Width Offset for Component Output		O			
ETMG2.MLSW	Line Sync Pulse Width Offset for Component Output		O			
ETMG3.CFPW	Front Porch Position Offset for Component Output		O			
ETMG3.CLBI	Line Blanking End Position Offset for Component Output		O			
DACSEL.DA3S	DAC3 Output Select	R	R			
DACSEL.DA2S	DAC2 Output Select	R	R			
DACSEL.DA1S	DAC1 Output Select	R	R			
DACSEL.DA0S	DAC0 Output Select	R	R			

Table 65. VPBE Global Registers for Hardware Setup (continued)

Register.Field	Description	Analog SDTV	Analog EDTV	YCC16	YCC8	Parallel RGB
ARGBX0.AGY	YCbCr->RGB Matrix Coefficient GY for Analog RGB Out		O			
ARGBX1.ARV	YCbCr->RGB Matrix Coefficient RV for Analog RGB Out		O			
ARGBX2.AGU	YCbCr->RGB Matrix Coefficient GU for Analog RGB Out		O			
ARGBX3.AGV	YCbCr->RGB Matrix Coefficient GV for Analog RGB Out		O			
ARGBX4.ABU	YCbCr->RGB Matrix Coefficient BU for Analog RGB Out		O			
DRGBX0.DGY	YCbCr->RGB Matrix Coefficient GY for Digital RGB Out					R
DRGBX1.DRV	YCbCr->RGB Matrix Coefficient RV for Digital RGB Out					R
DRGBX2.DGU	YCbCr->RGB Matrix Coefficient GU for Digital RGB Out					R
DRGBX3.DGV	YCbCr->RGB Matrix Coefficient GV for Digital RGB Out					R
DRGBX4.DBU	YCbCr->RGB Matrix Coefficient BU for Digital RGB Out					R
VSTARTA.VSTARTA	Vertical Data Valid Start Position for Even Field					
OSDCLK0.OCPW	OSD Clock Pattern Bit Width		R			
OSDCLK1.OCPT	OSD Clock Pattern		R			
HVLDCL0.HCM	Horizontal Valid Culling Mode					
HVLDCL0.HCPW	Horizontal Valid Culling Pattern Bit Width					
HVLDCL1.HCPT	Horizontal Culling Pattern					
OSDHADV.OHAD	OSD Horizontal Sync Advance					

5.5.2 Enable/Disable Hardware

Note: The OSD windows should be enabled prior to enabling the VENC (VMOD.VENC = 1).

The VENC has several module enables as described in Table 66.

Table 66. OSD Window Enable/Disable

Module	Display Enable
VPBE	VPBE.CLK_OFF
VENC	VMOD.VIE
Composite Analog Out	VMOD.VIE
Digital Output	VIDCLT.DOMD

6 Video Processing Back End (VPBE) Registers

This section discusses the registers in the video processor back end (VPBE).

6.1 *VPBE Global Registers*

Table 67 lists the memory-mapped global registers for the VPBE. See the device-specific data manual for the memory address of these registers.

Table 67. Video Processor Back End (VPBE) Global Registers

Offset	Acronym	Register Description	Section
2780h	PID	Peripheral Revision and Class Information Register	Section 6.1.1
2784h	PCR	Peripheral Control Register	Section 6.1.2

6.1.1 Peripheral Revision and Class Information (PID)

The peripheral revision and class information register (PID) is shown in Figure 77 and described in Table 68.

Figure 77. Peripheral Revision and Class Information Register (PID)

31–24	23–16
Reserved	TID
R-0	R-BEh

15–8	7–0
CID	PREV
R-4h	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 68. Peripheral Revision and Class Information Register (PID) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Reserved
23-16	TID	0-FFh	Peripheral identification
		BEh	VPBE module
15-8	CID	0-FFh	Class identification
		4h	
7-0	PREV	0-FFh	Peripheral revision number
		0	Initial revision

6.1.2 Peripheral Control Register (PCR)

The peripheral control register (PCR) is shown in Figure 78 and described in Table 69.

Figure 78. Peripheral Control Register (PCR)

31–16
Reserved
R-0

15–2	1	0
Reserved	VENC_DIV	CLK_OFF
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 69. Peripheral Control Register (PCR) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Reserved
1	VENC_DIV		Video Encoder Clock Divisor: If you select a 54-MHz clock (for the DAC) by programming the clock controller register, then the VENC_DIV field must be set to 1.
		0	Use Video Encoder Clock selected in System Module
		1	Use 1/2 Video Encoder Clock selected in System Module
0	CLK_OFF		Gate VPBE clocks for power savings: Only set this bit to 1 when the VPBE is not operational. Clear this bit to 0 prior to any other operations on the VPBE (including writing to other registers).
		0	Normal operation (clocks on)
		1	Clocks are disabled

6.2 Video Encoder/Digital LCD Subsystem (VENC) Registers

Table 70 lists the memory-mapped registers for the video encoder/digital LCD (VENC). See the device-specific data manual for the memory address of these registers. All other register offset addresses not listed in Table 70 should be considered as reserved locations and the register contents should not be modified.

Table 70. Video Encoder/Digital LCD (VENC) Registers

Offset	Acronym	Register Description	Section
2400h	VMOD	Video Mode Register	Section 6.2.1
2404h	VIDCTL	Video Interface I/O Control Register	Section 6.2.2
2408h	VDPRO	Video Data Processing Register	Section 6.2.3
240Ch	SYNCCTL	Sync Control Register	Section 6.2.4
2410h	HSPLS	Horizontal Sync Pulse Width Register	Section 6.2.5
2414h	VSPLS	Vertical Sync Pulse Width Register	Section 6.2.6
2418h	HINT	Horizontal Interval Register	Section 6.2.7
241Ch	HSTART	Horizontal Valid Data Start Position Register	Section 6.2.8
2420h	HVALID	Horizontal Data Valid Range Register	Section 6.2.9
2424h	VINT	Vertical Interval Register	Section 6.2.10
2428h	VSTART	Vertical Valid Data Start Position Register	Section 6.2.11
242Ch	VVALID	Vertical Data Valid Range Register	Section 6.2.12
2430h	HSDLY	Horizontal Sync Delay Register	Section 6.2.13
2434h	VSDLY	Vertical Sync Delay Register	Section 6.2.14
2438h	YCCTL	YCbCr Control Register	Section 6.2.15
243Ch	RGBCTL	RGB Control Register	Section 6.2.16
2440h	RGBCLP	RGB Level Clipping Register	Section 6.2.17
2444h	LINECTL	Line Identification Control Register	Section 6.2.18
2448h	CULLLINE	Culling Line Control Register	Section 6.2.19
244Ch	LCDOUT	LCD Output Signal Control Register	Section 6.2.20
2450h	BRTS	Brightness Start Position Signal Control Register	Section 6.2.21
2454h	BRTW	Brightness Width Signal Control Register	Section 6.2.22
2458h	ACCTL	LCD_AC Signal Control Register	Section 6.2.23
245Ch	PWMP	PWM Start Position Signal Control Register	Section 6.2.24
2460h	PWMW	PWM Width Signal Control Register	Section 6.2.25
2464h	DCLKCTL	DCLK Control Register	Section 6.2.26
2468h	DCLKPTN0	DCLK Pattern 0 Register	Section 6.2.27
246Ch	DCLKPTN1	DCLK Pattern 1 Register	Section 6.2.27
2470h	DCLKPTN2	DCLK Pattern 2 Register	Section 6.2.27
2474h	DCLKPTN3	DCLK Pattern 3 Register	Section 6.2.27
2478h	DCLKPTN0A	DCLK Auxiliary Pattern 0 Register	Section 6.2.28
247Ch	DCLKPTN1A	DCLK Auxiliary Pattern 1 Register	Section 6.2.28
2480h	DCLKPTN2A	DCLK Auxiliary Pattern 2 Register	Section 6.2.28
2484h	DCLKPTN3A	DCLK Auxiliary Pattern 3 Register	Section 6.2.28
2488h	DCLKHS	Horizontal DCLK Mask Start Register	Section 6.2.29
248Ch	DCLKHSA	Horizontal Auxiliary DCLK Mask Start Register	Section 6.2.30
2490h	DCLKHR	Horizontal DCLK Mask Range Register	Section 6.2.31
2494h	DCLKVS	Vertical DCLK Mask Start Register	Section 6.2.32
2498h	DCLKVR	Vertical DCLK Mask Range Register	Section 6.2.33
249Ch	CAPCTL	Caption Control Register	Section 6.2.34
24A0h	CAPDO	Caption Data Odd Field Register	Section 6.2.35

Table 70. Video Encoder/Digital LCD (VENC) Registers (continued)

Offset	Acronym	Register Description	Section
24A4h	CAPDE	Caption Data Even Field Register	Section 6.2.36
24A8h	ATR0	Video Attribute Data 0 Register	Section 6.2.37
24ACh	ATR1	Video Attribute Data 1 Register	Section 6.2.38
24B0h	ATR2	Video Attribute Data 2 Register	Section 6.2.39
24B8h	VSTAT	Video Status Register	Section 6.2.40
24C4h	DACTST	DAC Test Register	Section 6.2.41
24C8h	YCOLVL	YOUT and COUT Levels Register	Section 6.2.42
24CCh	SCPROG	Sub-Carrier Programming Register	Section 6.2.43
24DCh	CVBS	Composite Mode Register	Section 6.2.44
24E0h	CMPNT	Component Mode Register	Section 6.2.45
24E4h	ETMG0	CVBS Timing Control 0 Register	Section 6.2.46
24E8h	ETMG1	CVBS Timing Control 1 Register	Section 6.2.47
24ECh	ETMG2	Component Timing Control 0 Register	Section 6.2.48
24F0h	ETMG3	Component Timing Control 1 Register	Section 6.2.49
24F4h	DACSEL	DAC Output Select Register	Section 6.2.50
2500h	ARGBX0	Analog RGB Matrix 0 Register	Section 6.2.51
2504h	ARGBX1	Analog RGB Matrix 1 Register	Section 6.2.52
2508h	ARGBX2	Analog RGB Matrix 2 Register	Section 6.2.53
250Ch	ARGBX3	Analog RGB Matrix 3 Register	Section 6.2.54
2510h	ARGBX4	Analog RGB Matrix 4 Register	Section 6.2.55
2514h	DRGBX0	Digital RGB Matrix 0 Register	Section 6.2.56
2518h	DRGBX1	Digital RGB Matrix 1 Register	Section 6.2.57
251Ch	DRGBX2	Digital RGB Matrix 2 Register	Section 6.2.58
2520h	DRGBX3	Digital RGB Matrix 3 Register	Section 6.2.59
2524h	DRGBX4	Digital RGB Matrix 4 Register	Section 6.2.60
2528h	VSTARTA	Vertical Data Valid Start Position Register (for Even Field)	Section 6.2.61
252Ch	OSDCLK0	OSD Clock Control 0 Register	Section 6.2.62
2530h	OSDCLK1	OSD Clock Control 1 Register	Section 6.2.63
2534h	HVLDCL0	Horizontal Valid Culling Control 0 Register	Section 6.2.64
2538h	HVLDCL1	Horizontal Valid Culling Control 1 Register	Section 6.2.65
253Ch	OSDHADV	OSD Horizontal Sync Advance Register	Section 6.2.66
25F4h	VMISC	VENC Miscellaneous Register	Section 6.2.67

6.2.1 Video Mode Register (VMOD)

The video mode register (VMOD) is shown in Figure 79 and described in Table 71.

Figure 79. Video Mode Register (VMOD)

31–16
Reserved
R-0

15–12	11	10	9	8	7–6	5	4	3	2	1	0
VDMD	ITLCL	ITLC	NSIT	HDMD	TVTYP	SLAVE	VMD	BLNK	Rsvd	VIE	VENC
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 71. Video Mode Register (VMOD) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-12	VDMD	0-Fh	Digital video output mode.
		0	16-bit YCbCr output mode. Y and C are output separately on 16-bit bus.
		1h	8-bit YCbCr output mode.
		2h	Parallel RGB mode to output RGB separately.
		3h-Fh	Reserved
11	ITLCL		Non-interlace line number select. Effective in standard SDTV non-interlace mode (VMD = 0, HDMD = 0, and ITLC = 1).
		0	262 line (NTSC) or 312 line (PAL)
		1	263 line (NTSC) or 313 line (PAL)
10	ITLC		Interlaced Scan Mode Enable. Effective in standard SDTV mode (VMD = 0 and HDMD = 0).
		0	Interlace
		1	Non-interlace
9	NSIT		Non-standard interlace mode. Effective in non-standard mode (VMD = 1).
		0	Progressive
		1	Interlace
8	HDMD		HDTV mode. Effective in standard mode (VMD = 0).
		0	SDTV
		1	HDTV
7-6	TVTYP	0-3h	TV Format Type Select. Effective in standard mode (VMD = 0).
			In SDTV mode (HDMD = 0):
		0	NTSC
		1h	PAL
		2h-3h	Reserved
			In HDTV mode (HDMD = 1):
		0	525P
		1h	625P
		2h-3h	Reserved
5	SLAVE		Master-slave select.
		0	Master mode
		1	Slave mode
4	VMD		Video timing.
		0	NTSC/PAL timing
		1	Not NTSC/PAL timing

Table 71. Video Mode Register (VMOD) Field Descriptions (continued)

Bit	Field	Value	Description
3	BLNK		Blanking enable. Sync signal and color burst are still output.
		0	Normal
		1	Force blanking
2	Reserved	0	Reserved
1	VIE		Composite Analog Output Enable.
		0	Fixed low-level output
		1	Normal composite output
0	VENC		Video Encoder Enable.
		0	Disable
		1	Enable

6.2.2 Video Interface I/O Control Register (VIDCTL)

The video interface I/O control register (VIDCTL) is shown in Figure 80 and described in Table 72.

Figure 80. Video Interface I/O Control Register (VIDCTL)

31–16
Reserved
R-0

15	14	13	12	11–9	8	7–6	5–4	3	2	1	0
Rsvd	VCLKP	VCLKE	VCLKZ	Reserved	SYDIR	Reserved	DOMD	YCSWAP	YCOL	Rsvd	YCDIR
R-0	R/W-0	R/W-0	R/W-1	R-0	R/W-1	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 72. Video Interface I/O Control Register (VIDCTL) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Reserved
14	VCLKP		VCLK output polarity.
		0	Non-inverse
		1	Inverse
13	VCLKE		VCLK output enable. Setting to 1 outputs DCLK from VCLK pin. When 0 VCLKP setting is still available.
		0	Off
		1	On
12	VCLKZ		VCLK pin output enable.
		0	Output
		1	High impedance
11-9	Reserved	0	Reserved
8	SYDIR		Horizontal/Vertical Sync pin I/O control. Set to 1 when external syncs are input.
		0	Output
		1	Input
7-6	Reserved	0	Reserved
5-4	DOMD	0-3h	Digital data output mode.
		0	Normal output
		1h	Inverse output
		2h	Low-level output
		3h	High-level output
3	YCSWAP		Swaps YOUT/COUT pins. Interchanges the output data of YOUT and COUT.
		0	Normal output
		1	Interchange YOUT and COUT
2	YCOL		YOUT/COUT pin output level. Setting DC out option will output the value in the YCOLVL register on YOUT/COUT pins. Effective only when YOUT/COUT pin is set as output.
		0	Normal output
		1	DC level output
1	Reserved	0	Reserved. Always write a 0 to this bit.
0	YCDIR		YOUT/COUT pin direction. YOUT/COUT pin is used as Y/C data input pin (reserved). Clear to 0 for digital video output.
		0	Output
		1	Reserved (output disabled)

6.2.3 Video Data Processing Register (VDPRO)

The video data processing register (VDPRO) is shown in Figure 81 and described in Table 73.

Figure 81. Video Data Processing Register (VDPRO)

31–16
Reserved
R-0

15–14	13–12	11	10	9	8	7	6	5	4	3	2	1	0
PFLTC	PFLTY	PFLTR	Reserved	CBTYP	CBMD	Reserved	ATRGB	ATYCC	ATCOM	DAFRQ	DAUPS	CUPS	YUPS
R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 73. Video Data Processing Register (VDPRO) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-14	PFLTC	0-3h	C prefilter select: when PFLTR and PFLTC are 1, use PFLTY to 1 to adjust the delay between Y and C. When other combinations are selected, the hardware automatically adjusts the delay.
		0	No filter
		1h	1+1
		2h	1+2+1
		3h	Reserved
13-12	PFLTY		Y prefilter select: when PFLTR and PFLTY are 1, use PFLTC to 1 to adjust the delay between Y and C. When other combinations are selected, the hardware automatically adjusts the delay.
		0	No filter
		1h	1+1
		2h	1+2+1
		3h	Reserved
11	PFLTR		Prefilter sampling frequency
		0	ENC clock / 2
		1	ENC clock
10	Reserved	0	Reserved
9	CBTYP		Color bar type
		0	75%
		1	100%
8	CBMD		Color bar mode
		0	Normal output
		1	Color bar output
7	Reserved	0	Reserved
6	ATRGB		Input video: attenuation control for RGB
		0	No Attenuation
		1	0-255 => REC601 specified level
5	ATYCC		Input video. attenuation control for YCbCr
		0	No Attenuation
		1	0-255 => REC601 specified level
4	ATCOM		Input video: attenuation control for composite
		0	No Attenuation
		1	0-255 => REC601 specified level

Table 73. Video Data Processing Register (VDPRO) Field Descriptions (continued)

Bit	Field	Value	Description
3	DAFRQ		DAC operating frequency: must be configured according to DAC operating frequency.
		0	27-MHz DAC Clock
		1	54-MHz DAC Clock
2	DAUPS		DAC x2 up-sampling enable
		0	Off
		1	On
1	CUPS		C signal up-sampling enable
		0	Off
		1	On
0	YUPS		Y signal up-sampling enable
		0	Off
		1	On

6.2.4 Sync Control Register (SYNCCTL)

The sync control register (SYNCCTL) is shown in Figure 82 and described in Table 74.

Figure 82. Sync Control Register (SYNCCTL)

31–16
Reserved
R-0

15	14	13–12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	OVD	EXFMD	EXFIV	EXSYNC	EXVIV	EXHIV	CSP	CSE	SYSW	VSYNCS	VPL	HPL	SYEV	SYEH
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 74. Sync Control Register (SYNCCTL) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Reserved
14	OVD		OSD vsync delay
		0	No delay
		1	Delay 0.5H
13-12	EXFMD	0-3h	External field detection mode: effective in slave operation (SLAVE=1).
		0	Latch external field at external VD rising edge
		1h	Use raw external field
		2h	Use external vsync as field ID
		3h	Detect external vsync phase
11	EXFIV		External field input inversion: effective in slave operation (SLAVE=1).
		0	Non-inverse
		1	Inverse
10	EXSYNC		External sync select
		0	HSYNC/VSYNC pin
		1	CCD sync signal
9	EXVIV		External vertical sync input polarity
		0	Active H
		1	Active L
8	EXHIV		External horizontal sync input polarity
		0	Active H
		1	Active L
7	CSP		Composite signal output polarity: specifies composite signal output polarity from COUT3 pin in YCC8 or RGB8 mode.
		0	Active H
		1	Active L
6	CSE		Composite signal output enable: specifies composite signal output polarity from COUT3 pin in YCC8 or RGB8 mode.
		0	Off
		1	On
5	SYSW		Output sync select: applicable to standard mode only. Setting the SYSW to 1 in standard mode outputs the pulse width that the SYNCPLS register processes as an output sync signal.
		0	Normal
		1	Sync pulse width processing mode

Table 74. Sync Control Register (SYNCCTL) Field Descriptions (continued)

Bit	Field	Value	Description
4	VSYNCS		Vertical sync output signal
		0	Vertical sync signal
		1	Composite sync signal
3	VPL		Vertical sync output polarity
		0	Active H
		1	Active L
2	HPL		Horizontal sync output polarity.
		0	Active H
		1	Active L
1	SYEV		Vertical sync output enable: The output turns ON when the SYEV is set to 1, and the signal that the VSSW selects is output from the VSYNC pin. Setting to 0 outputs an inactive level that VPL determines.
		0	Off
		1	On
0	SYEH		Horizontal sync output enable: The output turns ON when SYEH is set to 1, and the signal that the VSSW selects is output from HSYNC pin. Setting to 0 outputs inactive level that HPL determines.
		0	Off
		1	On

6.2.5 Horizontal Sync Pulse Width Register (HSPLS)

The horizontal sync pulse width register (HSPLS) is shown in Figure 83 and described in Table 75.

Figure 83. Horizontal Sync Pulse Width Register (HSPLS)

31	16
Reserved	
R-0	

15-13	12-0
Reserved	HSPLS
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 75. Horizontal Sync Pulse Width Register (HSPLS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	HSPLS	0-1FFFh	Horizontal sync pulse width (number of ENC clocks). Effective in non-standard mode or sync processing mode (SYSW = 1).

6.2.6 Vertical Sync Pulse Width Register (VSPLS)

The vertical sync pulse width register (VSPLS) is shown in Figure 84 and described in Table 76.

Figure 84. Vertical Sync Pulse Width Register (VSPLS)

31	16
Reserved	
R-0	

15-13	12-0
Reserved	VSPLS
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 76. Vertical Sync Pulse Width Register (VSPLS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	VSPLS	0-1FFFh	Vertical sync pulse width (number of ENC clocks) - effective in non-standard mode or sync processing mode (SYSW = 1).

6.2.7 Horizontal Interval Register (HINT)

The horizontal interval register (HINT) is shown in Figure 85 and described in Table 77.

Figure 85. Horizontal Interval Register (HINT)

31–16
Reserved
R-0

15–13	12–0
Reserved	HINT
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 77. Horizontal Interval Register (HINT) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	HINT	0-1FFFh	Horizontal interval (number of ENC clocks) - effective in non-standard mode, if the OSD clock is (ENC clock / 2), specify even values. The interval is HINT + 1.

6.2.8 Horizontal Valid Data Start Position Register (HSTART)

The horizontal valid data start position register (HSTART) is shown in Figure 86 and described in Table 78.

Figure 86. Horizontal Valid Data Start Position Register (HSTART)

31–16
Reserved
R-0

15–13	12–0
Reserved	HSTART
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 78. Horizontal Valid Data Start Position Register (HSTART) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	HSTART	0-1FFFh	Horizontal valid data start position: specify the number of ENC clocks from the start of the horizontal sync. LCD_OE is asserted at the position specified here and the data output starts.

6.2.9 Horizontal Data Valid Range Register (HVALID)

The horizontal data valid range register (HVALID) is shown in Figure 87 and described in Table 79.

Figure 87. Horizontal Data Valid Range Register (HVALID)

31–16
Reserved
R-0

15–13	12–0
Reserved	HVALID
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 79. Horizontal Data Valid Range Register (HVALID) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	HVALID	0-1FFFh	Horizontal data valid range: specify the number of ENC clocks. The LCD_OE is asserted during the period specified here and valid data is output. The data outside of the valid range is output in L.

6.2.10 Vertical Interval Register (VINT)

The vertical interval register (VINT) is shown in Figure 88 and described in Table 80.

Figure 88. Vertical Interval Register (VINT)

31–16
Reserved
R-0

15–13	12–0
Reserved	VINT
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 80. Vertical Interval Register (VINT) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	VINT	0-1FFFh	Vertical interval (number of lines): effective in non-standard mode. The interval is represented by VINT + 1.

6.2.11 Vertical Valid Data Start Position Register (VSTART)

The vertical valid data start position register (VSTART) is shown in Figure 89 and described in Table 81.

Figure 89. Vertical Valid Data Start Position Register (VSTART)

31–16
Reserved
R-0

15–13	12–0
Reserved	VSTART
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 81. Vertical Valid Data Start Position Register (VSTART) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	VSTART	0-1FFFh	Vertical valid data start position: specify the number of lines.

6.2.12 Vertical Data Valid Range Register (VVALID)

The vertical data valid range register (VVALID) is shown in Figure 90 and described in Table 82.

Figure 90. Vertical Data Valid Range Register (VVALID)

31–16
Reserved
R-0

15–13	12–0
Reserved	VVALID
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 82. Vertical Data Valid Range Register (VVALID) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	VVALID	0-1FFFh	Vertical data valid range: specify the number of lines.

6.2.13 Horizontal Sync Delay Register (HSDLY)

The horizontal sync delay register (HSDLY) is shown in Figure 91 and described in Table 83.

Figure 91. Horizontal Sync Delay Register (HSDLY)

31		16
Reserved		
R-0		

15 - 13	12 - 0
Reserved	HSDLY
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 83. Horizontal Sync Delay Register (HSDLY) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	HSDLY	0-1FFFh	Output delay of the horizontal sync signal. This delays the HSYNC signal by the ENC clock.

6.2.14 Vertical Sync Delay Register (VSDLY)

The vertical sync delay register (VSDLY) is shown in Figure 92 and described in Table 84.

Figure 92. Vertical Sync Delay Register (VSDLY)

31		16
Reserved		
R-0		

15 - 13	12 - 0
Reserved	VSDLY
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 84. Vertical Sync Delay Register (VSDLY) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	VSDLY	0-1FFFh	Output delay of vertical sync signal. This delays the VSYNC signal by ENC clock.

6.2.15 YCbCr Control Register (YCCTL)

The YCbCr control register (YCCTL) is shown in Figure 93 and described in Table 85.

Figure 93. YCbCr Control Register (YCCTL)

31–16
Reserved
R-0

15–5	4	3–2	1	0
Reserved	CHM	YCP	Rsvd	R656
R-0	R/W-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 85. YCbCr Control Register (YCCTL) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Reserved
4	CHM		Chroma output mode. Effective in YCC16/YCC8 mode.
		0	Chroma not latched at first pixel
		1	Latch chroma at first pixel
3-2	YCP		YC output order based on YCC mode.
			In YCC16 mode (VMOD.VDMD = 0):
		0	YCC16 mode - CbCr
		1h	YCC16 mode - CrCb
		2h-3h	Reserved
			In YCC8 mode (VMOD.VDMD = 1):
		0	YCC8 mode - Cb-Y-Cr-Y
		1h	YCC8 mode - Y-Cr-Y-Cb
		2h	YCC8 mode - Cr-Y-Cb-Y
		3h	YCC8 mode - Y-Cb-Y-Cr
1	Reserved	0	Reserved
0	R656		REC656 mode: This is in ITU-R BT.656 format and is effective when the OSD clock runs at ENC clock/2.
		0	Normal
		1	REC656 mode

6.2.16 RGB Control Register (RGBCTL)

The RGB control register (RGBCTL) is shown in Figure 94 and described in Table 86.

Figure 94. RGB Control Register (RGBCTL)

31–16
Reserved
R-0

15–11	10	9–8	7–0
Reserved	DFLTR	DFLTS	Reserved
R-0	R/W-0	R/W-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 86. RGB Control Register (RGBCTL) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10	DFLTR		RGB LPF sampling frequency: effective in all digital output modes with RGB output. Effective in all digital modes with RGB output.
		0	ENC clock / 2
		1	ENC clock
9-8	DFLTS	0-3h	RGB LPF select. Effective in all digital modes with RGB output.
		0	No filter
		1h	1+2+1
		2h	1+2+4+2+1
		3h	Reserved
7-0	Reserved	0	Reserved

6.2.17 RGB Level Clipping Register (RGBCLP)

The RGB level clipping register (RGBCLP) is shown in Figure 95 and described in Table 87.

Figure 95. RGB Level Clipping Register (RGBCLP)

31–16
Reserved
R-0

15–8	7–0
UCLIP	OFST
R/W-FFh	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 87. RGB Level Clipping Register (RGBCLP) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	UCLIP	0-FFh	Upper clip level for RGB output: effective in all digital output modes with RGB output. Clipping is performed following offset addition.
7-0	OFST	0-FFh	Offset level for RGB output: effective in all digital output modes with the RGB output. You can add the offset specified here to RGB (converted from YCbCr).

6.2.18 Line Identification Control Register (LINECTL)

The line identification control register (LINECTL) is shown in Figure 96 and described in Table 88.

Figure 96. Line Identification Control Register (LINECTL)

31–16
Reserved
R-0

15–12		11	10–8
Reserved		VSTF	VCLID
R/W-0	R-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
VCLRD	VCL56	HLDF	HLDL	LINID	DCKCLP	DCKCLI	RGBCL
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 88. Line Identification Control Register (LINECTL) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reserved
11	VSTF		Vertical data valid start position field mode.
		0	Normal mode
		1	Field mode. Different start line can be specified for vertical data valid start position by VSTARTA register.
10-8	VCLID	0-7h	Vertical culling line position. Specifies which line will be culled of every six lines. No culling will be applied when VCLID is greater than 5. Effective when VCL56 = 1.
7	VCLRD		Vertical culling counter reset mode. Effective when VCL56 = 1.
		0	Counter for vertical culling is reset to zero at vertical sync.
		1	Reset to a random value at vertical sync.
6	VCL56		Digital output vertical culling. Enabling discards one line of video output every six lines. This can be used to output NTSC valid lines with PAL timing.
		0	No culling
		1	5/6 culling
5	HLDF		Digital output field hold. Effective in non-standard mode. Enabling suspends the video output when current field output is completed. Reading the data from OSD is suspended during this period.
		0	Normal
		1	Output hold
4	HLDL		Digital output line hold. Effective in non-standard mode. Enabling suspends the video output when current line output is completed. Reading the data from OSD is suspended during this period.
		0	Normal
		1	Output hold
3	LINID		Start line ID control in even field.
		0	Line ID = 0
		1	Line ID = 1
2	DCKCLP		DCLK pattern switching by culling line ID. When this is enabled, the DCLK pattern can be switched according to the culling line ID set by the CULLLINE register. The DCLK pattern on each line is specified by the DCLKPTN and DCLKPTNA registers.
		0	Off
		1	On

Table 88. Line Identification Control Register (LINECTL) Field Descriptions (continued)

Bit	Field	Value	Description
1	DCKCLI		DCLK polarity inversion by culling line ID. When this is disabled, the DCLK polarity is fixed anytime as specified by the VCLKP register. Enabling inverts this polarity according to the culling line ID set by the CULLLINE register.
		0	Off
		1	On
0	RGBCL		RGB output order switching by culling line ID. Disabling switches RGB output order every line. Enabling switches this order according to the XORed signal of the line ID and the culling line ID set by the CULLLINE register.
		0	Off
		1	On

6.2.19 Culling Line Control Register (CULLLINE)

The culling line control register (CULLLINE) is shown in Figure 97 and described in Table 89.

Figure 97. Culling Line Control Register (CULLLINE)

31–16
Reserved
R-0

15–12	11–8	7–4	3–0
CLOF	CLEF	Reserved	CULI
R/W-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 89. Culling Line Control Register (CULLLINE) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-12	CLOF	0-Fh	Culling line ID toggle position (odd field).
11-8	CLEF	0-Fh	Culling line ID toggle position (even field).
7-4	Reserved	0	Reserved
3-0	CULI	0-Fh	Culling line ID inversion interval.

6.2.20 LCD Output Signal Control Register (LCDOUT)

The LCD output signal control register (LCDOUT) is shown in Figure 98 and described in Table 90.

Figure 98. LCD Output Signal Control Register (LCDOUT)

31–16
Reserved
R-0

15–9	8	7	6	5	4	3	2	1	0
Reserved	FIDS	FIDP	PWMP	PWME	ACE	BRP	BRE	OEP	OEE
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 90. LCD Output Signal Control Register (LCDOUT) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8	FIDS		Output signal select. Selected in the PINMUX0 register in the System Module.
		0	LCD_OE
		1	BRIGHT
7	FIDP		Field ID output polarity.
		0	Non-inverse
		1	Inverse
6	PWMP		PWM output pulse polarity.
		0	Active high
		1	Active low
5	PWME		PWM output control.
		0	Off
		1	On
4	ACE		LCD_AC output control.
		0	Off
		1	On
3	BRP		BRIGHT output polarity.
		0	Non-inverse
		1	Inverse
2	BRE		BRIGHT output control.
		0	Off
		1	On
1	OEP		LCD_OE output polarity.
		0	Active high
		1	Active low
0	OEE		LCD_OE output control.
		0	Off
		1	LCD_OE appears on the GP[13] pin when FIDS = 0. In YCC8 mode, LCD_OE appears on COUT6.

6.2.21 Brightness Start Position Signal Control Register (BRTS)

The brightness start position signal control register (BRTS) is shown in Figure 99 and described in Table 91.

Figure 99. Brightness Start Position Signal Control Register (BRTS)

31–16
Reserved
R-0

15–13	12–0
Reserved	BRTS
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 91. Brightness Start Position Signal Control Register (BRTS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	BRTS	0-1FFFh	BRIGHT pulse start position: specify the number of ENC cycles from the HSYNC signal.

6.2.22 Brightness Width Signal Control Register (BRTW)

The brightness width signal control register (BRTW) is shown in Figure 100 and described in Table 92.

Figure 100. Brightness Width Signal Control Register (BRTW)

31–16
Reserved
R-0

15–13	12–0
Reserved	BRTW
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 92. Brightness Width Signal Control Register (BRTW) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	BRTW	0-1FFFh	BRIGHT pulse width: specify the number of ENC cycles.

6.2.23 LCD_AC Signal Control Register (ACCTL)

The LCD_AC signal control register (ACCTL) is shown in Figure 101 and described in Table 93.

Figure 101. LCD_AC Signal Control Register (ACCTL)

31–16
Reserved
R-0

15–13	12–0
ACTF	ACTH
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 93. LCD_AC Signal Control Register (ACCTL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-13	ACTF	0-7h	LCD_AC toggle interval. LCD_AC is toggled every field specified here.
12-0	ACTH	0-1FFFh	LCD_AC toggle horizontal position. LCD_AC is toggled by the number of ENC clocks from the rising edge of horizontal sync signal.

6.2.24 PWM Start Position Signal Control Register (PWMP)

The PWM start position signal control register (PWMP) is shown in Figure 102 and described in Table 94.

Figure 102. PWM Start Position Signal Control Register (PWMP)

31	16
Reserved	
R-0	

15–13	12–0
Reserved	PWMP
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 94. PWM Start Position Signal Control Register (PWMP) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	PWMP	0-1FFFh	PWM output period. Specify the number of ENC clocks. Period is PWMP + 1.

6.2.25 PWM Width Signal Control Register (PWMW)

The PWM width signal control register (PWMW) is shown in Figure 103 and described in Table 95.

Figure 103. PWM Width Signal Control Register (PWMW)

31	16
Reserved	
R-0	

15–13	12–0
Reserved	PWMW
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 95. PWM Width Signal Control Register (PWMW) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	PWMW	0-1FFFh	PWM output pulse width. Specify the H pulse width by ENC clock. Setting to 0 makes PWM output L level always. Setting bigger value than PWMP sets to H level always.

6.2.26 DCLK Control Register (DCLKCTL)

The DCLK control register (DCLKCTL) is shown in Figure 104 and described in Table 96.

Figure 104. DCLK Control Register (DCLKCTL)

31-16
Reserved
R-0

15	14	13-12	11	10	9	8
DCKIM	Reserved	DOFST	DCKEC	DCKME	DCKOH	DCKIH
R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7-6	5-0
Reserved	DCKPW
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 96. DCLK Control Register (DCLKCTL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15	DCKIM		DCLK internal mode. When enabled, a different pattern can be specified for the internal DCLK from the output DCLK. In this mode, DCLKPTN0A-PCLKPTN3A and DCLKHSTTA are used to specify the internal DCLK pattern and its pattern valid bit width, respectively. The DCLK pattern switching by culling line ID (LINECTL.DCKCLP = 1) is no longer available in this mode.
		0	Off
		1	On
14	Reserved	0	Reserved
13-12	DOFST	0-3h	DCLK output offset. To adjust the DCLK delay output from the VCLK pin by the ENC clock. When the DCLK output is configured as ENC clock gating with DCKEC = 1 and DCKOH = 0, these bits have no meaning.
		0	0
		1h	-0.5
		2h	0.5
		3h	1
11	DCKEC		DCLK pattern mode.
		0	Specified value in DCLKPTN (or DCLKPTNA) becomes the clock level of DCLK.
		1	DCLKPTN works as the clock enable for ENC clock.
10	DCKME		DCLK mask control. Masks are specified by the DCLKHSTT, DCLKHVLD, DCLKVSTT, and DCLKVVLD registers.
		0	Mask is OFF and outputs DCLK directly.
		1	Mask is ON and outputs the clock in specified valid area.
9	DCKOH		DCLK output divide. Enabling divides the clock by 2 and outputs it from the VCLK pin. RGB data is output by the rising of internal DCLK and only divided clock output is output. Thus, this can be used to connect to the LCD that captures the data.
		0	Divide by 1
		1	Divide by 2
8	DCKIH		Internal DCLK output divide. Enabling divides the internal DCLK clock by 2. When the clock output is divided by 1 (DCKOH = 0), two clocks can be output per one data. Thus, this can be used to connect to the LCD that requires double clock frequency.
		0	Divide by 1
		1	Divide by 2
7-6	Reserved	0	Reserved
5-0	DCKPW	0-3Fh	DCLK pattern valid bit width. Set the width of valid bits among the 64 bits in the DCLKPTN0-DCLKPTN3 registers.

6.2.27 DCLK Pattern *n* Registers (DCLKPTN0-DCLKPTN3)

The DCLK pattern *n* register (DCLKPTN*n*) is shown in Figure 105 and described in Table 97.

Figure 105. DCLK Pattern *n* Register (DCLKPTN*n*)

31	16
Reserved	
R-0	

15	0
DCPTN*n*	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 97. DLCK Pattern *n* Register (DCLKPTN*n*) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	DCPTN*n*	0-FFFFh	DCLK pattern. The specified bit pattern is output in resolution of ENC clock units.

6.2.28 DCLK Auxiliary Pattern *n* Registers (DCLKPTN0A-DCLKPTN3A)

The DCLK auxiliary pattern *n* register (DCLKPTN*n*A) is shown in Figure 106 and described in Table 98.

Figure 106. DCLK Auxiliary Pattern *n* Register (DCLKPTN*n*A)

31	16
Reserved	
R-0	

15	0
DCPTN*n*A	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 98. DLCK Auxiliary Pattern *n* Register (DCLKPTN*n*A) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	DCPTN*n*A	0-FFFFh	DCLK auxiliary pattern. The specified bit pattern is output in resolution of ENC clock units.

6.2.29 Horizontal DCLK Mask Start Register (DCLKHS)

The horizontal DCLK mask start register (DCLKHS) is shown in Figure 107 and described in Table 99.

Figure 107. Horizontal DCLK Mask Start Register (DCLKHS)

31–16
Reserved
R-0

15–13	12–0
Reserved	DCHS
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 99. Horizontal DCLK Mask Start Register (DCLKHS) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	DCHS	0-1FFFh	Horizontal DCLK mask start position. This is specified in number of ENC clocks from start of the horizontal sync signal.

6.2.30 Horizontal Auxiliary DCLK Mask Start Register (DCLKHSA)

The horizontal auxiliary DCLK mask start register (DCLKHSA) is shown in Figure 108 and described in Table 100.

Figure 108. Horizontal Auxiliary DCLK Mask Start Register (DCLKHSA)

31–16
Reserved
R-0

15–13	12–0
Reserved	DCHS
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 100. Horizontal Auxiliary DCLK Mask Start Register (DCLKHSA) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	DCHS	0-1FFFh	Horizontal auxiliary DCLK mask start position. This is specified in number of ENC clocks from start of the horizontal sync signal.

6.2.31 Horizontal DCLK Mask Range Register (DCLKHR)

The horizontal DCLK mask range register (DCLKHR) is shown in Figure 109 and described in Table 101.

Figure 109. Horizontal DCLK Mask Range Register (DCLKHR)

31–16
Reserved
R-0

15–13	12–0
Reserved	DCHR
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 101. Horizontal DCLK Mask Range Register (DCLKHR) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	DCHR	0-1FFFh	Horizontal DCLK mask range. This is specified in number of ENC clocks.

6.2.32 Vertical DCLK Mask Start Register (DCLKVS)

The vertical DCLK mask start register (DCLKVS) is shown in Figure 110 and described in Table 102.

Figure 110. Vertical DCLK Mask Start Register (DCLKVS)

31–16
Reserved
R-0

15–13	12–0
Reserved	DCVS
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 102. Vertical DCLK Mask Start Register (DCLKVS) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	DCVS	0-1FFFh	Vertical DCLK mask start position. This is specified in lines from vertical sync signal.

6.2.33 Vertical DCLK Mask Range Register (DCLKVR)

The vertical DCLK mask range register (DCLKVR) is shown in Figure 111 and described in Table 103.

Figure 111. Vertical DCLK Mask Range Register (DCLKVR)

31–16
Reserved
R-0

15–13	12–0
Reserved	DCVR
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 103. Vertical DCLK Mask Range Register (DCLKVR) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	DCVR	0-1FFFh	Vertical DCLK mask range. This is specified in number of lines.

6.2.34 Caption Control Register (CAPCTL)

The caption control register (CAPTCTL) is shown in Figure 112 and described in Table 104.

Figure 112. Caption Control Register (CAPCTL)

31–16
Reserved
R-0

15	14–8	7–2	1–0
Reserved	CADF	Reserved	CAPF
R-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 104. Caption Control Register (CAPCTL) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Reserved
14-8	CADF	0-7Fh	Closed caption default data register. When the caption data register (CAPDO or CAPDE) is not updated before the caption data transmission timing for the corresponding field, the ASCII code specified by this register is automatically transmitted for closed caption data.
7-2	Reserved	0	Reserved
1-0	CAPF	0-3h	Closed caption field select.
		0	No data output
		1h	Odd field
		2h	Even field
		3h	Both odd and even fields

6.2.35 Caption Data Odd Field Register (CAPDO)

The caption data odd field register (CAPDO) is shown in Figure 113 and described in Table 105.

Figure 113. Caption Data Odd Field Register (CAPDO)

31-16
Reserved
R-0

15	14-8	7	6-0
Reserved	CADO0	Reserved	CADO1
R-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 105. Caption Data Odd Field Register (CAPDO) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Reserved
14-8	CADO0	0-7Fh	Closed caption default data0 (odd field). Specify the ASCII code of the 1st byte to be transmitted in closed captioning for odd field. Parity bit is automatically calculated.
7	Reserved	0	Reserved
6-0	CADO1	0-7Fh	Closed caption default data1 (odd field). Specify the ASCII code of the 2nd byte to be transmitted in closed captioning for odd field. Parity bit is automatically calculated.

6.2.36 Caption Data Even Field Register (CAPDE)

The caption data even field register (CAPDE) is shown in Figure 114 and described in Table 106.

Figure 114. Caption Data Even Field Register (CAPDE)

31-16
Reserved
R-0

15	14-8	7	6-0
Reserved	CADE0	Reserved	CADE1
R-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 106. Caption Data Even Field Register (CAPDE) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Reserved
14-8	CADE0	0-7Fh	Closed caption default data0 (even field). Specify the ASCII code of the 1st byte to be transmitted in closed captioning for odd field. Parity bit is automatically calculated.
7	Reserved	0	Reserved
6-0	CADE1	0-7Fh	Closed caption default data1 (even field). Specify the ASCII code of the 2nd byte to be transmitted in closed captioning for odd field. Parity bit is automatically calculated.

6.2.37 Video Attribute Data #0 Register (ATR0)

The video attribute data #0 register (ATR0) is shown in Figure 115 and described in Table 107.

Figure 115. Video Attribute Data #0 Register (ATR0)

31–16	
Reserved	
R-0	

15–8	7–0
Reserved	ATR0
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 107. Video Attribute Data #0 Register (ATR0) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Reserved
7-0	ATR0	0-FFh	Video attribute data register 0. NTSC - Set the WORD0 data. - Bit7-6 is unused, - Bit5-3 is WORD0-B, - Bit2-0 is WORD0-A PAL - not used.

6.2.38 Video Attribute Data #1 Register (ATR1)

The video attribute data #1 register (ATR1) is shown in Figure 116 and described in Table 108.

Figure 116. Video Attribute Data #1 Register (ATR1)

31–16	
Reserved	
R-0	

15–8	7–0
Reserved	ATR1
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 108. Video Attribute Data #1 Register (ATR1) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Reserved
7-0	ATR1	0-FFh	Video attribute data register 1. NTSC - Set the WORD1 and WORD2 data - Bit7-4 is WORD2, - Bit3-0 is WORD1 PAL - Set the GROUP1 and GROUP2 data. - Bit7-4 is GROUP2, - Bit3-0 is GROUP1.

6.2.39 Video Attribute Data #2 Register (ATR2)

The video attribute data #2 register (ATR2) is shown in Figure 117 and described in Table 109.

Figure 117. Video Attribute Data #2 Register (ATR2)

31–16
Reserved
R-0

15–8	7–0
Reserved	ATR2
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 109. Video Attribute Data #2 Register (ATR2) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Reserved
7-0	ATR2	0-FFh	Video attribute data register 2. NTSC - Set CRC data and enable attribute insertion. - Bit7 is ATR_EN, - Bit6 is unused, - Bit5-0 is CRC PAL - Set GROUP3 and GROU4 data and enable attribute insertion. - Bit7 is ATR_EN, - Bit6 is unused, - Bit5-3 is GROUP4 and - Bit2-0 is GROUP3 ATR_EN: Attribute data insertion enable 0: No insertion 1: Insertion.

6.2.40 Video Status Register (VSTAT)

The video status register (VSTAT) is shown in Figure 118 and described in Table 110.

Figure 118. Video Status Register (VSTAT)

31–16
Reserved
R-0

15–10	9	8	7–5	4	3–2	1	0
Reserved	CAEST	CAOST	Reserved	FIDST	Reserved	UDBAL	UDFUL
R-0	R-0	R-0	R-0	R/W-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 110. Video Status Register (VSTAT) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Reserved
9	CAEST	0-1	Closed caption status (even field)
8	CAOST	0-1	Closed caption status (odd field)
7-5	Reserved	0	Reserved
4	FIDST	0-1	Field ID monitor
3-2	Reserved	0	Reserved
1	UDBAL	0-1	µDisplay 'Balance signal' monitor
0	UDFUL	0-1	µDisplay 'Full' signal monitor

6.2.41 DAC Test Register (DACTST)

The DAC test register (DACTST) is shown in Figure 119 and described in Table 111.

Figure 119. DAC Test Register (DACTST)

31–16
Reserved
R-0

15	14	13	12	11–0
DAPD3	DAPD2	DAPD1	DAPD0	Reserved
R/W-1	R/W-1	R/W-1	R/W-1	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 111. DAC Test Register (DACTST) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15	DAPD3		DAC3 power-down
		0	Normal mode
		1	Power-down mode
14	DAPD2		DAC2 power-down
		0	Normal mode
		1	Power-down mode
13	DAPD1		DAC1 power-down
		0	Normal mode
		1	Power-down mode
12	DAPD0		DAC0 power-down
		0	Normal mode
		1	Power-down mode
11-0	Reserved	0	Reserved

6.2.42 YOUT and COUT Levels Register (YCOLVL)

The YOUT and COUT levels register (YCOLVL) is shown in Figure 120 and described in Table 112.

Figure 120. YOUT and COUT Levels Register (YCOLVL)

31 - 16
Reserved
R-0

15 - 8	7 - 0
YLVL	CLVL
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 112. YOUT and COUT Levels Register (YCOLVL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	YLVL	0-FFh	YOUT DC level
7-0	CLVL	0-FFh	COUT DC level

6.2.43 Sub-Carrier Programming Register (SCPROG)

The sub-carrier programming register (SCPROG) is shown in Figure 121 and described in Table 113.

Figure 121. Sub-Carrier Programming Register (SCPROG)

31 - 16
Reserved
R-0

15 - 10	9 - 0
Reserved	SCSD
R-0	R/W-17Ah

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 113. Sub-Carrier Programming Register (SCPROG) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Reserved
9-0	SCSD	0-3FFh	Sub-carrier initial phase value. Phase in degrees specified by SCSD/1024 $\times$ 360.

6.2.44 Composite Mode Register (CVBS)

The composite mode register (CVBS) is shown in Figure 122 and described in Table 114

Figure 122. Composite Mode Register (CVBS)

31–16
Reserved
R-0

15	14–12	11–6	5	4	3	2	1	0
Reserved	YCDLY	Reserved	CVLVL	CSTUP	CBLS	Rsvd	CBBLD	CSBLD
R-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 114. Composite Mode Register (CVBS) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Reserved
14-12	YCDLY	0-7h	Delay adjustment of the Y signal in the composite signal. The value represented is 2's complement.
		0	0
		1h	1
		2h	2
		3h	3
		4h	-4
		5h	-3
		6h	-2
		7h	-1
11-6	Reserved	0	Reserved
5	CVLVL		Composite video level (sync/white)
		0	286mV/714mV
		1	300mV/700mV
4	CSTUP		Setup level at NTSC output
		0	0%
		1	7.5%
3	CBLS		Blanking shape disable
		0	Enable
		1	Disable
2	Reserved	0	Reserved
1	CBBLD		Blanking build-up time for composite output
		0	140 µs
		1	300 µs
0	CSBLD		Sync build-up time for composite output
		0	140 µs
		1	200 µs

6.2.45 Component Mode Register (CMPNT)

The component mode register (CMPNT) is shown in Figure 123 and described in Table 115.

Figure 123. Component Mode Register (CMPNT)

31–16
Reserved
R-0

15	14–12	11	10	9	8	7–6	5	4	3	2	1	0
MRGB	MYDLY	Reserved	MSYR	MSYB	MSYG	MCLVL	MYLVL	MSTUP	MBLS	Reserved	MBBLD	MSBLD
R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 115. Component Mode Register (CMPNT) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15	MRGB		RGB mode select for component output.
		0	YPbPr
		1	RGB
14-12	MYDLY	0-7h	Delay adjustment of Y signal in component mode. The value represented is 2's complement.
		0	0
		1h	1
		2h	2
		3h	3
		4h	-4
		5h	-3
		6h	-2
		7h	-1
11	Reserved	0	Reserved
10	MSYR		Sync on Pr (or R).
		0	No sync
		1	Sync on
9	MSYB		Sync on Pb (or B).
		0	No sync
		1	Sync on
8	MSYG		Sync on Y (or G).
		0	No sync
		1	Sync on
7-6	MCLVL	0-3h	Chroma level for component YPbPr.
		0	350mV (SMPTE N10)
		1h	467mV (Betacam)
		2h	324mV (MII)
		3h	Reserved
5	MYLVL		Luma level (sync/white) for component YPbPr.
		0	286mV/714mV
		1	300mV/700mV
4	MSTUP		Setup for component YPbPr.
		0	0%
		1	7.5%

Table 115. Component Mode Register (CMPNT) Field Descriptions (continued)

Bit	Field	Value	Description
3	MBLS		Blanking shape disable. When set to 1, blanking shaping feature is disabled.
		0	Enable
		1	Disable
2	Reserved	0	Reserved
1	MBBLD		Blanking build-up time for component output.
			Interlaced:
		0	140 µs
		1	300 µs
			Progressive:
		0	70 µs
		1	150 µs
0	MSBLD		Sync build-up time for component output.
			Interlaced:
		0	140 µs
		1	200 µs
			Progressive:
		0	70 µs
		1	100 µs

6.2.46 CVBS Timing Control 0 Register (ETMG0)

The CVBS timing control 0 register (ETMG0) is shown in Figure 124 and described in Table 116.

Figure 124. CVBS Timing Control 0 Register (ETMG0)

31–16
Reserved
R-0

15–12	11–8	7–4	3–0
Reserved	CEPW	CFSW	CLSW
R-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 116. CVBS Timing Control 0 Register (ETMG0) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reserved
11-8	CEPW	0-Fh	Equalizing pulse width offset for composite output .This is set by ENC clock. This register is represented as signed-integer (2's complement).
7-4	CFSW	0-Fh	Field sync pulse width offset for composite output. This is set by ENC clock. This register is represented as signed-integer (2's complement).
3-0	CLSW	0-Fh	Line sync pulse width offset for composite output. This is set by ENC clock. This register is represented as signed-integer (2's complement).

6.2.47 CVBS Timing Control 1 Register (ETMG1)

The CVBS timing control 1 register (ETMG1) is shown in Figure 125 and described in Table 117.

Figure 125. CVBS Timing Control 1 Register (ETMG1)

31–16
Reserved
R-0

15–12	11–8	7–4	3–0
CBSE	CBST	CFPW	CLBI
R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 117. CVBS Timing Control 1 Register (ETMG1) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-12	CBSE	0-Fh	Burst end position offset for composite output. This is set by ENC clock. This register is represented as signed-integer (2's complement).
11-8	CBST	0-Fh	Burst start position offset for composite output. This is set by ENC clock. This register is represented as signed-integer (2's complement).
7-4	CFPW	0-Fh	Front porch position offset for composite output. This is set by ENC clock. This register is represented as signed-integer (2's complement).
3-0	CLBI	0-Fh	Line blanking end position offset for composite output. This is set by ENC clock. This register is represented as signed-integer (2's complement).

6.2.48 Component Timing Control 0 Register (ETMG2)

The component timing control 0 register (ETMG2) is shown in Figure 126 and described in Table 118.

Figure 126. Component Timing Control 0 Register (ETMG2)

31–16
Reserved
R-0

15–12	11–8	7–4	3–0
Reserved	MEPW	MFSW	MLSW
R-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 118. Component Timing Control 0 Register (ETMG2) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reserved
11-8	MEPW	0-Fh	Equalizing pulse width offset for component output. This is set by ENC clock. This register is represented as signed-integer (2's complement).
7-4	MFSW	0-Fh	Field sync pulse width offset for component output. This is set by ENC clock. This register is represented as signed-integer (2's complement).
3-0	MLSW	0-Fh	Line sync pulse width offset for component output. This is set by ENC clock. This register is represented as signed-integer (2's complement).

6.2.49 Component Timing Control 1 Register (ETMG3)

The component timing control 1 register (ETMG3) is shown in Figure 127 and described in Table 119.

Figure 127. Component Timing Control 1 Register (ETMG3)

31–16
Reserved
R-0

15–8	7–4	3–0
Reserved	CFPW	CLBI
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 119. Component Timing Control 1 Register (ETMG3) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Reserved
7-4	CFPW	0-Fh	Front porch position offset for component output. This is set by ENC clock. This register is represented as signed-integer (2's complement).
3-0	CLBI	0-Fh	Line blanking end position offset for component output. This is set by ENC clock. This register is represented as signed-integer (2's complement).

6.2.50 DAC Output Select Register (DACSEL)

The DAC output select register (DACSEL) is shown in Figure 128 and described in Table 120.

Figure 128. DAC Output Select Register (DACSEL)

31–16
Reserved
R-0

15–12	11–8	7–4	3–0
DA3S	DA2S	DA1S	DA0S
R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 120. DAC Output Select Register (DACSEL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-12	DA3S	0-7Fh	DAC3 output select
		0	CVBS
		1h	S-Video Y
		2h	S-Video C
		3h	Y/G
		4h	Pb/B
		5h	Pr/R
		6h-7Fh	Reserved
11-8	DA2S	0-7Fh	DAC2 output select
		0	CVBS
		1h	S-Video Y
		2h	S-Video C
		3h	Y/G
		4h	Pb/B
		5h	Pr/R
		6h-7Fh	Reserved
7-4	DA1S	0-7Fh	DAC1 output select
		0	CVBS
		1h	S-Video Y
		2h	S-Video C
		3h	Y/G
		4h	Pb/B
		5h	Pr/R
		6h-7Fh	Reserved
3-0	DA0S	0-7Fh	DAC0 output select
		0	CVBS
		1h	S-Video Y
		2h	S-Video C
		3h	Y/G
		4h	Pb/B
		5h	Pr/R
		6h-7Fh	Reserved

6.2.51 Analog RGB Matrix 0 Register (ARGBX0)

The analog RGB matrix 0 register (ARGBX0) is shown in Figure 129 and described in Table 121.

Figure 129. Analog RGB Matrix 0 Register (ARGBX0)

31–16		
Reserved		
R-0		
15–11	**10–0**	
Reserved	AGY	
R-0	R/W-400h	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 121. Analog RGB Matrix 0 Register (ARGBX0) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	AGY	0-7FFh	YCbCr->RGB matrix coefficient GY for analog RGB out. Equation: $$\begin{vmatrix} R \\ G \\ B \end{vmatrix} = 1/1024 \begin{vmatrix} GY & 0 & RV \\ GY & -GU & -GV \\ GY & BU & 0 \end{vmatrix} \begin{vmatrix} Y-16 \\ Cb-128 \\ Cr-128 \end{vmatrix}$$ Default: $$\begin{vmatrix} R \\ G \\ B \end{vmatrix} = 1/1024 \begin{vmatrix} 1024 & 0 & 1404 \\ 1024 & -345 & -715 \\ 1024 & 1774 & 0 \end{vmatrix} \begin{vmatrix} Y-16 \\ Cb-128 \\ Cr-128 \end{vmatrix}$$

6.2.52 Analog RGB Matrix 1 Register (ARGBX1)

The analog RGB matrix 1 register (ARGBX1) is shown in Figure 130 and described in Table 122.

Figure 130. Analog RGB Matrix 1 Register (ARGBX1)

31–16	
Reserved	
R-0	
15–11	**10–0**
Reserved	ARV
R-0	R/W-57Ch

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 122. Analog RGB Matrix 1 Register (ARGBX1) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	ARV	0-7FFh	YCbCr->RGB matrix coefficient RV for analog RGB out.

6.2.53 Analog RGB Matrix 2 Register (ARGBX2)

The analog RGB matrix 2 register (ARGBX2) is shown in Figure 131 and described in Table 123.

Figure 131. Analog RGB Matrix 2 Register (ARGBX2)

31	16
Reserved	
R-0	

15 11	10 0
Reserved	AGU
R-0	R/W-159h

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 123. Analog RGB Matrix 2 Register (ARGBX2) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	AGU	0-7FFh	YCbCr->RGB matrix coefficient GU for analog RGB out

6.2.54 Analog RGB Matrix 3 Register (ARGBX3)

The analog RGB matrix 3 register (ARGBX3) is shown in Figure 132 and described in Table 124.

Figure 132. Analog RGB Matrix 3 Register (ARGBX3)

31	16
Reserved	
R-0	

15 11	10 0
Reserved	AGV
R-0	R/W-2CBh

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 124. Analog RGB Matrix 3 Register (ARGBX3) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	AGV	0-7FFh	YCbCr->RGB matrix coefficient GV for analog RGB out.

6.2.55 Analog RGB Matrix 4 Register (ARGBX4)

The analog RGB matrix 4 register (ARGBX4) is shown in Figure 133 and described in Table 125.

Figure 133. Analog RGB Matrix 4 Register (ARGBX4)

31–16
Reserved
R-0

15–11	10–0
Reserved	ABU
R-0	R/W-6EEh

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 125. Analog RGB Matrix 4 Register (ARGBX4) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	ABU	0-7FFh	YCbCr->RGB matrix coefficient BU for analog RGB out.

6.2.56 Digital RGB Matrix 0 Register (DRGBX0)

The digital RGB matrix 0 register (DRGBX0) is shown in Figure 134 and described in Table 126.

Figure 134. Digital RGB Matrix 0 Register (DRGBX0)

31–16
Reserved
R-0

15–11	10–0
Reserved	DGY
R-0	R/W-400h

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 126. Digital RGB Matrix 0 Register (DRGBX0) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	DGY	0-7FFh	YCbCr->RGB matrix coefficient GY for digital RGB out. Equation: $\begin{vmatrix} R \\ G \\ B \end{vmatrix} = 1/1024 \begin{vmatrix} GY & 0 & RV \\ GY & -GU & -GV \\ GY & BU & 0 \end{vmatrix} \begin{vmatrix} Y-16 \\ Cb-128 \\ Cr-128 \end{vmatrix}$ Default: $\begin{vmatrix} R \\ G \\ B \end{vmatrix} = 1/1024 \begin{vmatrix} 1024 & 0 & 1404 \\ 1024 & -345 & -715 \\ 1024 & 1774 & 0 \end{vmatrix} \begin{vmatrix} Y-16 \\ Cb-128 \\ Cr-128 \end{vmatrix}$

6.2.57 Digital RGB Matrix 1 Register (DRGBX1)

The digital RGB matrix 1 register (DRGBX1) is shown in Figure 135 and described in Table 127.

Figure 135. Digital RGB Matrix 1 Register (DRGBX1)

31–16
Reserved
R-0

15–11	10–0
Reserved	DRV
R-0	R/W-57Ch

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 127. Digital RGB Matrix 1 Register (DRGBX1) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	DRV	0-7FFh	YCbCr->RGB matrix coefficient RV for digital RGB out

6.2.58 Digital RGB Matrix 2 Register (DRGBX2)

The digital RGB matrix 2 register (DRGBX2) is shown in Figure 136 and described in Table 128.

Figure 136. Digital RGB Matrix 2 Register (DRGBX2)

31–16
Reserved
R-0

15–11	10–0
Reserved	DGU
R-0	R/W-159h

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 128. Digital RGB Matrix 2 Register (DRGBX2) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	DGU	0-7FFh	YCbCr->RGB matrix coefficient GU for digital RGB out

6.2.59 Digital RGB Matrix 3 Register (DRGBX3)

The digital RGB matrix 3 register (DRGBX3) is shown in Figure 137 and described in Table 129.

Figure 137. Digital RGB Matrix 3 Register (DRGBX3)

31–16
Reserved
R-0

15–11	10–0
Reserved	DGV
R-0	R/W-2CBh

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 129. Digital RGB Matrix 3 Register (DRGBX3) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	DGV	0-7FFh	YCbCr->RGB matrix coefficient GV for digital RGB out.

6.2.60 Digital RGB Matrix 4 Register (DRGBX4)

The digital RGB matrix 4 register (DRGBX4) is shown in Figure 138 and described in Table 130.

Figure 138. Digital RGB Matrix 4 Register (DRGBX4)

31–16
Reserved
R-0

15–11	10–0
Reserved	DBU
R-0	R/W-6EEh

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 130. Digital RGB Matrix 4 Register (DRGBX4) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	DBU	0-7FFh	YCbCr->RGB matrix coefficient BU for digital RGB out.

6.2.61 Vertical Data Valid Start Position for Even Field Register (VSTARTA)

The vertical data valid start position for even field register (VSTARTA) is shown in Figure 139 and described in Table 131.

Figure 139. Vertical Data Valid Start Position for Even Field Register (VSTARTA)

31 – 16
Reserved
R-0

15 – 13	12 – 0
Reserved	VSTARTA
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 131. Vertical Data Valid Start Position for Even Field Register (VSTARTA) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	VSTARTA	0-1FFFh	Vertical data valid start position for even field. Specify the number of lines.

6.2.62 OSD Clock Control 0 Register (OSDCLK0)

The OSD clock control 0 register (OSDCLK0) is shown in Figure 140 and described in Table 132.

Figure 140. OSD Clock Control 0 Register (OSDCLK0)

31 – 16
Reserved
R-0

15 – 4	3 – 0
Reserved	OCPW
R-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 132. OSD Clock Control 0 Register (OSDCLK0) Field Descriptions

Bit	Field	Value	Description
31-4	Reserved	0	Reserved
3-0	OCPW	0-Fh	OSD clock pattern bit width. Sets the width of valid bit among all 16 bits in the OSDCLK1 register. The number of the valid bits is counted from LSB side to MSB side of the OSDCLK1.

6.2.63 OSD Clock Control 1 Register (OSDCLK1)

The OSD clock control 1 register (OSDCLK1) is shown in Figure 141 and described in Table 133.

Figure 141. OSD Clock Control 1 Register (OSDCLK1)

31–16
Reserved
R-0

15–0
OCPT
R/W-2h

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 133. OSD Clock Control 1 Register (OSDCLK1) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	OCPT	0-FFFFh	OSD clock pattern.

6.2.64 Horizontal Valid Culling Control 0 Register (HVLDCL0)

The horizontal valid culling control 0 register (HVLDCL0) is shown in Figure 142 and described in Table 134.

Figure 142. Horizontal Valid Culling Control 0 Register (HVLDCL0)

31–16
Reserved
R- 0

15–5	4	3–0
Reserved	HCM	HCPW
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 134. Horizontal Valid Culling Control 0 Register (HVLDCL0) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Reserved
4	HCM		Horizontal valid culling mode When enabled, the LCD_OE signal is gated by the pattern specified by HCPT register.
		0	Normal mode
		1	Horizontal valid culling mode
3-0	HCPW	0-Fh	Horizontal valid culling pattern bit width Set the width of valid bit among all 16 bits in the HVLDCL1 register. The number of the valid bits is counted from LSB side to MSB side of the HVLDCL1.

6.2.65 Horizontal Valid Culling Control 1 Register (HVLDCL1)

The horizontal valid culling control 1 register (HVLDCL1) is shown in Figure 143 and described in Table 135.

Figure 143. Horizontal Valid Culling Control 1 Register (HVLDCL1)

31–16
Reserved
R- 0

15–0
HCPT
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 135. Horizontal Valid Culling Control 1 Register (HVLDCL1) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	HCPT	0-FFFFh	Horizontal culling pattern.

6.2.66 OSD Horizontal Sync Advance Register (OSDHADV)

The OSD horizontal sync advance register (OSDHADV) is shown in Figure 144 and described in Table 136.

Figure 144. OSD Horizontal Sync Advance Register (OSDHADV)

31–16
Reserved
R-0

15–8	7–0
Reserved	OHAD
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 136. OSD Horizontal Sync Advance Register (OSDHADV) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Reserved
7-0	OHAD	0-FFh	OSD horizontal sync advance. OSD horizontal sync assertion timing can be advanced by this register. By default, the timing is adjusted so that OSD timing related registers and VENC timing related registers are aligned. Specify the number of ENC clocks.

6.2.67 VENC Miscellaneous Register (VMISC)

The VENC miscellaneous register (VMISC) is shown in Figure 145 and described in Table 137.

Figure 145. VENC Miscellaneous Register (VMISC)

31–16
Reserved
R/W-0

15–1	0
Reserved	YUPF
R/W-0	R/W-0

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 137. VENC Miscellaneous Register (VMISC) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved. You should not write to these bits, but always maintain the default value.
0	YUPF		Luma upsampling filter select.
		0	Reserved
		1	[1 2 1], must be used when VDPRO.YUPS = 1.

6.3 On-Screen Display (OSD) Registers

Table 138 lists the registers for the OSD module. See the device-specific data manual for the memory address of these registers. All other register offset addresses not listed in Table 138 should be considered as reserved locations and the register contents should not be modified.

Some registers/fields are shadowed during the frame display time and any writes to these locations are not applied until the next frame period. These are noted in Table 64.

Table 138. On-Screen Display (OSD) Registers

Offset	Register	Description	Section
2600h	MODE	OSD Mode Register	Section 6.3.1
2604h	VIDWINMD	Video Window Mode Setup Register	Section 6.3.2
2608h	OSDWIN0MD	OSD Window Mode Setup Register	Section 6.3.3
260Ch	OSDWIN1MD	OSD Window 1 Mode Setup Register (when used as a second OSD window)	Section 6.3.4
260Ch	OSDATRMD	OSD Attribute Window Mode Setup (when used as an attribute window)	Section 6.3.5
2610h	RECTCUR	Rectangular Cursor Setup Register	Section 6.3.6
2618h	VIDWIN0OFST	Video Window 0 Offset Register	Section 6.3.7
261Ch	VIDWIN1OFST	Video Window 1 Offset Register	Section 6.3.8
2620h	OSDWIN0OFST	OSD Window 0 Offset Register	Section 6.3.9
2624h	OSDWIN1OFST	OSD Window 1 Offset Register	Section 6.3.10
262Ch	VIDWIN0ADR	Video Window 0 Address Register	Section 6.3.11
2630h	VIDWIN1ADR	Video Window 1 Address Register	Section 6.3.12
2638h	OSDWIN0ADR	OSD Window 0 Address Register	Section 6.3.13
263Ch	OSDWIN1ADR	OSD Window 1 Address Register	Section 6.3.14
2640h	BASEPX	Base Pixel X Register	Section 6.3.15
2644h	BASEPY	Base Pixel Y Register	Section 6.3.16
2648h	VIDWIN0XP	Video Window 0 X-Position Register	Section 6.3.17
264Ch	VIDWIN0YP	Video Window 0 Y-Position Register	Section 6.3.18
2650h	VIDWIN0XL	Video Window 0 X-Size Register	Section 6.3.19
2654h	VIDWIN0YL	Video Window 0 Y-Size Register	Section 6.3.20
2658h	VIDWIN1XP	Video Window 1 X-Position Register	Section 6.3.21
265Ch	VIDWIN1YP	Video Window 1 Y-Position Register	Section 6.3.22
2660h	VIDWIN1XL	Video Window 1 X-Size Register	Section 6.3.23
2664h	VIDWIN1YL	Video Window 1 Y-Size Register	Section 6.3.24
2668h	OSDWIN0XP	OSD Bitmap Window 0 X-Position Register	Section 6.3.25
266Ch	OSDWIN0YP	OSD Bitmap Window 0 Y-Position Register	Section 6.3.26
2670h	OSDWIN0XL	OSD Bitmap Window 0 X-Size Register	Section 6.3.27
2674h	OSDWIN0YL	OSD Bitmap Window 0 Y-Size Register	Section 6.3.28
2678h	OSDWIN1XP	OSD Bitmap Window 1 X-Position Register	Section 6.3.29
267Ch	OSDWIN1YP	OSD Bitmap Window 1 Y-Position Register	Section 6.3.30
2680h	OSDWIN1XL	OSD Bitmap Window 1 X-Size Register	Section 6.3.31
2684h	OSDWIN1YL	OSD Bitmap Window 1 Y-Size Register	Section 6.3.32
2688h	CURXP	Rectangular Cursor Window X-Position Register	Section 6.3.33
268Ch	CURYP	Rectangular Cursor Window Y-Position Register	Section 6.3.34
2690h	CURXL	Rectangular Cursor Window X-Size Register	Section 6.3.35
2694h	CURYL	Rectangular Cursor Window Y-Size Register	Section 6.3.36
26A0h	W0BMP01	Window 0 Bitmap Value to Palette Map 0/1 Register	Section 6.3.37
26A4h	W0BMP23	Window 0 Bitmap Value to Palette Map 2/3 Register	Section 6.3.38

Table 138. On-Screen Display (OSD) Registers (continued)

Offset	Register	Description	Section
26A8h	W0BMP45	Window 0 Bitmap Value to Palette Map 4/5 Register	Section 6.3.39
26ACh	W0BMP67	Window 0 Bitmap Value to Palette Map 6/7 Register	Section 6.3.40
26B0h	W0BMP89	Window 0 Bitmap Value to Palette Map 8/9 Register	Section 6.3.41
26B4h	W0BMPAB	Window 0 Bitmap Value to Palette Map A/B Register	Section 6.3.42
26B8h	W0BMPCD	Window 0 Bitmap Value to Palette Map C/D Register	Section 6.3.43
26BCh	W0BMPEF	Window 0 Bitmap Value to Palette Map E/F Register	Section 6.3.44
26C0h	W1BMP01	Window 1 Bitmap Value to Palette Map 0/1 Register	Section 6.3.45
26C4h	W1BMP23	Window 1 Bitmap Value to Palette Map 2/3 Register	Section 6.3.46
26C8h	W1BMP45	Window 1 Bitmap Value to Palette Map 4/5 Register	Section 6.3.47
26CCh	W1BMP67	Window 1 Bitmap Value to Palette Map 6/7 Register	Section 6.3.48
26D0h	W1BMP89	Window 1 Bitmap Value to Palette Map 8/9 Register	Section 6.3.49
26D4h	W1BMPAB	Window 1 Bitmap Value to Palette Map A/B Register	Section 6.3.50
26D8h	W1BMPCD	Window 1 Bitmap Value to Palette Map C/D Register	Section 6.3.51
26DCh	W1BMPEF	Window 1 Bitmap Value to Palette Map E/F Register	Section 6.3.52
26E8h	MISCCTL	Miscellaneous Control Register	Section 6.3.53
26ECh	CLUTRAMYCB	CLUT RAMYCB Setup Register	Section 6.3.54
26F0h	CLUTRAMCR	CLUT RAM Setup Register	Section 6.3.55
26F4h	TRANSPVAL	Transparency Value Setup Register	Section 6.3.56
26FCh	PPVWIN0ADR	Ping-Pong Video Window 0 Address Register	Section 6.3.57

6.3.1 OSD Mode Register (MODE)

The OSD mode register (MODE) is shown in Figure 146 and described in Table 139.

Figure 146. OSD Mode Register (MODE)

31–16
Reserved
R-0

15	14	13	12	11	10	9	8	7–0
CS	OVRSZ	OHRSZ	EF	VVRSZ	VHRSZ	FSINV	BCLUT	CABG
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 139. OSD Mode Register (MODE) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15	CS		Cb/Cr or Cr/Cb format. This bit selects the order of the input data relative to the placement of the Cb and Cr components.
		0	Cb/Cr
		1	Cr/Cb
14	OVRSZ		OSD window vertical expansion enable. When enabled, the bitmap window images are stretched by a factor of 6/5 in the vertical direction. Results in proper vertical sizing to display a normal VGA (640 × 480) image on a PAL television (720 × 576); that is, 480 × 6/5 = 576.
		0	× 1
		1	× 6/5
13	OHRSZ		OSD window horizontal expansion enable. When enabled, the bitmap window images are stretched by a factor of 9/8 in the horizontal direction. Results in proper horizontal sizing to display a normal VGA (640 × 480) image on a PAL / NTSC television (720).
		0	× 1
		1	× 9/8
12	EF		Expansion filter enable. Valid when either VVRSZ or VHRSZ is on, or video window smoothing is set. Caution is required when using the filter since expansion filter memory can only correspond to 720 horizontal pixels. VD latches this bit.
		0	Off
		1	On
11	VVRSZ		Video window vertical expansion enable. When enabled, the video window images are stretched by a factor of 6/5 in the vertical direction. Results in proper vertical sizing to display a normal VGA (640 × 480) image on a PAL television (720 × 576); that is, 480 × 6/5 = 576. VD latches this bit.
		0	× 1
		1	× 6/5
10	VHRSZ		Video window horizontal expansion enable. When enabled, the video window images are stretched by a factor of 9/8 in the horizontal direction. Results in proper horizontal sizing to display a normal VGA (640 × 480) image on an NTSC/PAL television (720 × n); that is, 640 × 9/8 = 720. VD latches this bit.
		0	× 1
		1	× 9/8
9	FSINV		Field signal inversion. VD latches this bit.
		0	Noninverted
		1	Inverted
8	BCLUT		Background CLUT selection. Selects look-up table for background color display. VD latches this bit.
		0	ROM
		1	RAM
7-0	CABG	0-FFh	Background color CLUT. Specifies the image display background color by CLUT address. In parts that do not display the image, color specified by this register is displayed.

6.3.2 Video Window Mode Setup Register (VIDWINMD)

The video window mode setup register (VIDWINMD) is shown in Figure 147 and described in Table 140.

Figure 147. Video Window Mode Setup Register (VIDWINMD)

31–16
Reserved
R-0

15	14	13–12	11–10	9	8	7	6	5–4	3–2	1	0
Rsvd	V1EFC	VHZ1	VVZ1	VFF1	ACT1	Rsvd	V0EFC	VHZ0	VVZ0	VFF0	ACT0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 140. Video Window Mode Setup Register (VIDWINMD) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15	Reserved	0	Reserved. Always write 0 to this bit.
14	V1EFC		Video window 1 expansion filter coefficient. When VVRSZ and EF are set to 1, this bit is valid.
		0	Same coefficients for field-0 and field-1.
		1	Different coefficients for field-0 and field-1.
13-12	VHZ1	0-3h	Video Window 1 horizontal direction zoom. VD latches this bit.
		0	× 1
		1h	× 2
		2h	× 4
		3h	Reserved (same as 0)
11-10	VVZ1	0-3h	Video window 1 vertical direction zoom. VD latches this bit.
		0	× 1
		1h	× 2
		2h	× 4
		3h	Reserved (same as 0)
9	VFF1		Video window 1 display mode. In Field mode, only the number of lines in a field, as specified in VIDWIN1YL, will be read from display memory and the data is repeated for each field sent to the VENC module. In Frame mode, 2× the number of lines in a field, as specified in VIDWIN1YL, will be read from display memory, with the data being interleaved for each field sent to the VENC module. This provides full vertical resolution of 2× VIDWIN1YL. VD latches this bit.
		0	Field mode
		1	Frame mode
8	ACT1		Sets image display on/off video window 1. VD latches this bit.
		0	Off
		1	On
7	Reserved	0	Reserved
6	V0EFC		Video window 0 expansion filter coefficient. When VVRSZ and EF are set to 1, this bit is valid.
		0	Same coefficients for field-0 and field-1.
		1	Different coefficients for field-0 and field-1.
5-4	VHZ0	0-3h	Video window 0 horizontal direction zoom. VD latches this bit.
		0	× 1
		1h	× 2
		2h	× 4
		3h	Reserved (same as 0)

Table 140. Video Window Mode Setup Register (VIDWINMD) Field Descriptions (continued)

Bit	Field	Value	Description
3-2	VVZ0	0-3h	Video window 0 vertical direction zoom. VD latches this bit.
		0	× 1
		1h	× 2
		2h	× 4
		3h	Reserved (same as 0)
1	VFF0		Video window 0 display mode. In Field mode, only the number of lines in a field, as specified in VIDWIN0YL, will be read from display memory and the data is repeated for each field sent to the VENC module. In Frame mode, 2× the number of lines in a field, as specified in VIDWIN0YL, will be read from display memory, with the data being interleaved for each field sent to the VENC module. This provides full vertical resolution of 2× VIDWIN0YL. VD latches this bit.
		0	Field mode
		1	Frame mode
0	ACT0		Sets image display on/off video window 0. VD latches this bit.
		0	Off
		1	On

6.3.3 OSD Window 0 Mode Setup Register (OSDWIN0MD)

The OSD window 0 mode setup register (OSDWIN0MD) is shown in Figure 148 and described in Table 141.

Figure 148. OSD Window 0 Mode Setup Register (OSDWIN0MD)

31–16
Reserved
R-0

15–14	13	12	11–10	9–8	7–6	5–3	2	1	0
Reserved	RGB0E	CLUTS0	OHZ0	OVZ0	BMW0	BLND0	TE0	OFF0	OACT0
R-0 (15), R/W-0 (14)	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 141. OSD Window 0 Mode Setup Register (OSDWIN0MD) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Reserved
14	Reserved	0	Reserved. Always write 0 to this bit.
13	RGB0E		RGB input for window 0 enable. When RGB0E bit in OSDWIN0MD is set/enabled, RGB1E should not be set to 1 (parallel use is not allowed). The following equation is used to calculate YCbCr when RGB0E is set to 1. $Y = 0.2990 \times R + 0.5870 \times G + 0.1140 \times B$ $Cb = -0.1687 \times R - 0.3313 \times G + 0.5000 \times B + Offset(128)$ $Cr = 0.5000 \times R - 0.4187 \times G - 0.0813 \times B + Offset(128)$
		0	Bitmap input
		1	16-bit RGB mode
12	CLUTS0		CLUT select for OSD window 0. Selects look-up table that is used for OSD window 0. VD latches this bit.
		0	ROM-look-up table
		1	RAM-look-up table
11-10	OHZ0	0-3h	OSD window 0 horizontal zoom. VD latches this bit.
		0	$\times 1$
		1h	$\times 2$
		2h	$\times 4$
		3h	Reserved (same as 0)
9-8	OVZ0	0-3h	OSD window 0 vertical zoom. VD latches this bit.
		0	$\times 1$
		1h	$\times 2$
		2h	$\times 4$
		3h	Reserved (same as 0)
7-6	BMW0	0-3h	Bitmap bit width for OSD window 0. VD latches this bit. This is valid only for bitmap type. When the OSD window is in RGB input mode, bit width is automatically set to 16-bit and this register setting is ignored.
		0	1 bit
		1h	2 bits
		2h	4 bits
		3h	8 bits

Table 141. OSD Window 0 Mode Setup Register (OSDWIN0MD) Field Descriptions (continued)

Bit	Field	Value	Description
5-3	BLND0	0-7h	Blending ratio for OSD window 0. Sets blending ratio of OSD window 0 and any Video Window 0. VD latches this bit.
		0	W0-0 V0-1
		1h	W0-1/8 V0-7/8
		2h	W0-2/8 V0-6/8
		3h	W0-3/8 V0-5/8
		4h	W0-4/8 V0-4/8
		5h	W0-5/8 V0-3/8
		6h	W0-6/8 V0-2/8
		7h	W0-1 V0-0
2	TE0		Transparency enable for OSD window 0. When Transparency is disabled, the entire bitmap window is blended with the video windows according to BLND0. Bitmap Mode When Transparency is enabled, Transparency is only performed for pixels whose bitmap value is 0, according to BLND0. RGB Mode When Transparency is enabled and the pixel value is the same as TRANSPVAL, the YCbCr data converted from RGB value and video windows are blended according to the blending ratio specified in BLND0. VD latches this bit.
		0	Disable
		1	Enable
1	OFF0		OSD window 0 display mode. In Field mode, only the number of lines in a field, as specified in OSDWIN0YL, will be read from display memory and the data is repeated for each field sent to the VENC module. In Frame mode, 2× the number of lines in a field, as specified in OSDWIN0YL, will be read from display memory, with the data being interleaved for each field sent to the VENC module. This provides full vertical resolution of 2× OSDWIN0YL. VD latches this bit.
		0	Field mode
		1	Frame mode
0	OACT0		OSD window 0 active (displayed). VD latches this bit.
		0	Off
		1	On

6.3.4 OSD Window 1 Mode Setup Register (OSDWIN1MD)

The OSD window 1 mode setup register (OSDWIN1MD) is shown in Figure 149 and described in Table 142.

Figure 149. OSD Window 1 Mode Setup Register (OSDWIN1MD)

31–16
Reserved
R-0

15	14	13	12	11–10	9–8	7–6	5–3	2	1	0
OASW	Rsvd	RGB1E	CLUTS1	OHZ1	OVZ1	BMW1	BLND1	TE1	OFF1	OACT1
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 142. OSD Window 1 Mode Setup Register (OSDWIN1MD) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15	OASW		OSD window 1 attribute mode enable. This bit enables attribute mode for OSD window 0. This bit is latched by VD.
		0	OSD window 0
		1	Attribute window
14	Reserved	0	Reserved. Always write 0 to this bit.
13	RGB1E		RGB input for window 1 enable. OASW = 0. When RGB0E bit in OSDWIN1MD is set/enabled, RGB0E should not be set to 1 (parallel use is not allowed). The following equation is used to calculate YCbCr when RGB1E is set to 1. $Y = 0.2990 \times R + 0.5870 \times G + 0.1140 \times B$ $Cb = -0.1687 \times R - 0.3313 \times G + 0.5000 \times B + Offset(128)$ $Cr = 0.5000 \times R - 0.4187 \times G - 0.0813 \times B + Offset(128)$
		0	Bitmap input
		1	16-bit RGB mode
12	CLUTS1		CLUT select for OSD window 1. OASW = 0. Selects look-up table that is used for OSD window 0.
		0	ROM-look-up table
		1	RAM-look-up table
11-10	OHZ1	0-3h	OSD window 1 horizontal zoom. OASW = 0. VD latches this bit.
		0	× 1
		1h	× 2
		2h	× 4
		3h	Reserved (same as 0)
9-8	OVZ1	0-3h	OSD window 1 vertical zoom. OASW = 0. VD latches this bit.
		0	× 1
		1h	× 2
		2h	× 4
		3h	Reserved (same as 0)
7-6	BMW1	0-3h	Bitmap bit width for OSD window 1. OASW = 0. Bitmap bit width for OSD window 0. VD latches this bit.
		0	1 bit
		1h	2 bits
		2h	4 bits
		3h	8 bits

Table 142. OSD Window 1 Mode Setup Register (OSDWIN1MD) Field Descriptions (continued)

Bit	Field	Value	Description
5-3	BLND1	0-7h	Blending ratio for OSD window 1. OASW = 0. Sets blending ratio of OSD window 1 and Video Window 0. VD latches this bit.
		0	W0-0 V0-1
		1h	W0-1/8 V0-7/8
		2h	W0-2/8 V0-6/8
		3h	W0-3/8 V0-5/8
		4h	W0-4/8 V0-4/8
		5h	W0-5/8 V0-3/8
		6h	W0-6/8 V0-2/8
		7h	W0-1 V0-0
2	TE1		Transparency enable for OSD window 1. OASW = 0. When Transparency is disabled, the entire bitmap window is blended with the video windows according to BLND1. Bitmap Mode When Transparency is enabled, blending is only performed for pixels whose bitmap value is 0, according to BLND1. RGB Mode When Transparency is enabled and the pixel value is the same as TRANSPVAL, the YCbCr data converted from RGB value and video windows are blended according to the blending ratio specified in BLND1. VD latches this bit.
		0	Disable
		1	Enable
1	OFF1		OSD window 1 display mode. OASW = 0. In Field mode, only the number of lines in a field, as specified in OSDWIN1YL, will be read from display memory and the data is repeated for each field sent to the VENC module. In Frame mode, 2× the number of lines in a field, as specified in OSDWIN1YL, will be read from display memory, with the data being interleaved for each field sent to the VENC module. This provides full vertical resolution of 2× OSDWIN1YL. VD latches this it.
		0	Field mode
		1	Frame mode
0	OACT1		OSD window 1 active (displayed). OASW = 0. VD latches this bit.
		0	Off
		1	On

6.3.5 OSD Attribute Window Mode Setup Register (OSDATRMD)

The OSD attribute window mode setup register (OSDATRMD) is shown in Figure 150 and described in Table 143.

Figure 150. OSD Attribute Window Mode Setup Register (OSDATRMD)

31–16
Reserved
R-0

15	14–12	11–10	9–8	7–6	5–2	1	0
OASW	Reserved	OHZA	OVZA	BLNKINT	Reserved	OFFA	BLNK
R/W-0	R-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 143. OSD Attribute Window Mode Setup Register (OSDATRMD) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15	OASW		OSD window 1 attribute mode enable. This bit enables attribute mode for OSD window 0. VD latches this bit.
		0	OSD window 0
		1	Attribute window
14-12	Reserved	0	Reserved
11-10	OHZA	0-3h	OSD attribute window horizontal zoom (when OASW = 1). VD latches this bit.
		0	× 1
		1h	× 2
		2h	× 4
		3h	Reserved (same as 0)
9-8	OVZA	0-3h	OSD attribute window vertical zoom (when OASW = 1). VD latches this bit.
		0	× 1
		1h	× 2
		2h	× 4
		3h	Reserved (same as 0)
7-6	BLNKINT	0-3h	Blinking interval (when OASW = 1). Specifies the blinking interval of the attribute window in units of 8 VD pulses. VD latches this bit.
		0	1 unit
		1h	2 units
		2h	3 units
		3h	4 units
5-2	Reserved	0	Reserved
1	OFFA		OSD attribute window display mode (when OASW = 1). VD latches this bit.
		0	Field mode
		1	Frame mode
0	BLNK		OSD attribute window blink enable (when OASW = 1). VD latches this bit.
		0	Off
		1	On

6.3.6 Rectangular Cursor Setup Register (RECTCUR)

The rectangular cursor setup register (RECTCUR) is shown in Figure 151 and described in Table 144.

Figure 151. Rectangular Cursor Setup Register (RECTCUR)

31–16
Reserved
R-0

15–8	7	6–4	3–1	0
RCAD	CLUTSR	RCHW	RCVW	RCACT
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 144. Rectangular Cursor Setup Register (RECTCUR) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	RCAD	0-FFh	Rectangular cursor color palette address.
7	CLUTSR		CLUT select. This bit is latched by VD.
		0	ROM-look-up table
		1	RAM-look-up table
6-4	RCHW	0-7h	Rectangular cursor horizontal line width. Width is 4 pixels × RCHW. VD latches this bit.
		0	1 pixel
		1h	4 pixels
		2h	8 pixels
		3h	12 pixels
		4h	16 pixels
		5h	20 pixels
		6h	24 pixels
		7h	28 pixels
3-1	RCVW	0-7h	Rectangular cursor vertical line width. Width is 2 lines × RCVW. VD latches this bit.
		0	1 line
		1h	2 lines
		2h	4 lines
		3h	6 lines
		4h	8 lines
		5h	10 lines
		6h	12 lines
		7h	14 lines
0	RCACT		Rectangular cursor active (displayed). VD latches this bit.
		0	Off
		1	On

6.3.7 Video Window 0 Offset Register (VIDWIN0OFST)

The video window 0 offset register (VIDWIN0OFST) is shown in Figure 152 and described in Table 145.

Figure 152. Video Window 0 Offset Register (VIDWIN0OFST)

31–16	
Reserved	
R-0	

15–9	8–0
Reserved	V0LO
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 145. Video Window 0 Offset Register (VIDWIN0OFST) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	V0LO	0-1FFh	Video window 0 line offset. Number of burst transfers (32-bytes) in a horizontal line. Video data format is YCbYCr, or 32-bits per 2 pixels, which gives 16-pixels/burst: Line width in pixels/16; for example, 720/16 = 45 (2Dh). If line width setting for the window result in a non-integer value, round the value up to the next larger integer and organize the data in SDRAM so that each line begins on a burst boundary. VD latches this bit.

6.3.8 Video Window 1 Offset Register (VIDWIN1OFST)

The video window 1 offset register (VIDWIN1OFST) is shown in Figure 153 and described in Table 146.

Figure 153. Video Window 1 Offset Register (VIDWIN1OFST)

31–16	
Reserved	
R-0	

15–9	8–0
Reserved	V1LO
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 146. Video Window 1 Offset Register (VIDWIN1OFST) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	V1LO	0-1FFh	Video window 1 line offset. Number of burst transfers (32-bytes) in a horizontal line. Video data format is YCbYCr, or 32-bits per 2 pixels, which gives 16-pixels/burst: Line width in pixels/16; for example, 720/16 = 45 (2Dh). If line width setting for the window result in a non-integer value, round the value up to the next larger integer and organize the data in SDRAM so that each line begins on a burst boundary. VD latches this bit.

6.3.9 OSD Window 0 Offset Register (OSDWIN0OFST)

The OSD window 0 offset register (OSDWIN0OFST) is shown in Figure 154 and described in Table 147.

Figure 154. OSD Window 0 Offset Register (OSDWIN0OFST)

31–16
Reserved
R-0

15–9	8–0
Reserved	O0LO
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 147. OSD Window 0 Offset Register (OSDWIN0OFST) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	O0LO	0-1FFh	OSD window 0 line offset. Number of burst transfers (32-bytes) in a horizontal line. This depends on OSD window bit depth: Line width in (pixels × bitdepth)/256-bits/burst; for example, (64 × 8)/256 = 2. If line width and bitdepth settings for the window result in a non-integer value, round the value up to the next larger integer and organize the data in SDRAM so that each line begins on a burst boundary. VD latches this bit. Examples: Offsets for 256 pixels horizontal: 1-bit mode: ((256 × 1)/8)/32 = 1(0001h); 2-bit mode: ((256 × 2)/8)/32 = 2(0002h); 4-bit mode: ((256 × 4)/8)/32 = 4(0004h); 8-bit mode: ((256 × 8)/8)/32 = 8(0008h); RGB565 mode: ((256 × 16)/8)/32 = 16(0010h)

6.3.10 OSD Window 1 Offset Register (OSDWIN1OFST)

The OSD window 1 offset register (OSDWIN1OFST) is shown in Figure 155 and described in Table 148.

Figure 155. OSD Window 1 Offset Register (OSDWIN1OFST)

31–16
Reserved
R-0

15–9	8–0
Reserved	O1LO
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 148. OSD Window 1 Offset Register (OSDWIN1OFST) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	O1LO	0-1FFh	OSD window 1 line offset. Number of burst transfers (32-bytes) in a horizontal line. This depends on OSD window bit depth: Line width in (pixels × bitdepth)/256-bits/burst; for example, (64 × 8)/256 = 2. If line width and bitdepth settings for the window result in a non-integer value, round the value up to the next larger integer and organize the data in SDRAM so that each line begins on a burst boundary. VD latches this bit. Examples: Offsets for 256 pixels horizontal: 1-bit mode: ((256 × 1)/8)/32 = 1(0001h); 2-bit mode: ((256 × 2)/8)/32 = 2(0002h); 4-bit mode: ((256 × 4)/8)/32 = 4(0004h); 8-bit mode: ((256 × 8)/8)/32 = 8(0008h); RGB565 mode: ((256 × 16)/8)/32 = 16(0010h).

6.3.11 Video Window 0 Address Register (VIDWIN0ADR)

The video window 0 address register (VIDWIN0ADR) is shown in Figure 156 and described in Table 149.

Figure 156. Video Window 0 Address Register (VIDWIN0ADR)

31 … 0
VIDWIN0ADR
R/W-0

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 149. Video Window 0 Address Register (VIDWIN0ADR) Field Descriptions

Bit	Field	Value	Description
31-0	VIDWIN0ADR	0-FFFF FFFFh	Video window 0 SDRAM source address. The SDRAM source address is an absolute byte address. Note that the address should be aligned on a 32-byte (burst) boundary. As a result, the 5 LSBs are ignored and reading this register will always show the 5 LSBs as 0. VD latches this bit.

6.3.12 Video Window 1 Address Register (VIDWIN1ADR)

The video window 1 address register (VIDWIN1ADR) is shown in Figure 157 and described in Table 150.

Figure 157. Video Window 1 Address Register (VIDWIN1ADR)

31 … 0
VIDWIN1ADR
R/W-0

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 150. Video Window 1 Address Register (VIDWIN1ADR) Field Descriptions

Bit	Field	Value	Description
31-0	VIDWIN1ADR	0-FFFF FFFFh	Video window 1 SDRAM source address. The SDRAM source address is an absolute byte address. Note that the address should be aligned on a 32-byte (burst) boundary. As a result, the 5 LSBs are ignored and reading this register will always show the 5 LSBs as 0. VD latches this bit.

6.3.13 OSD Window 0 Address Register (OSDWIN0ADR)

The OSD window 0 address register (OSDWIN0ADR) is shown in Figure 158 and described in Table 151.

Figure 158. OSD Window 0 Address Register (OSDWIN0ADR)

31 ... 0
OSDWIN0ADR
R/W-0

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 151. OSD Window 0 Address Register (OSDWIN0ADR) Field Descriptions

Bit	Field	Value	Description
31-0	OSDWIN0ADR	0-FFFF FFFFh	OSD window 0 SDRAM source address. The SDRAM source address is an absolute byte address. Note that the address should be aligned on a 32-byte (burst) boundary. As a result, the 5 LSBs are ignored and reading this register will always show the 5 LSBs as 0. VD latches this bit.

6.3.14 OSD Window 1 Address Register (OSDWIN1ADR)

The OSD window 1 address register (OSDWIN1ADR) is shown in Figure 159 and described in Table 152.

Figure 159. OSD Window 1 Address Register (OSDWIN1ADR)

31 ... 0
OSDWIN1ADR
R/W-0

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 152. OSD Window 1 Address Register (OSDWIN1ADR) Field Descriptions

Bit	Field	Value	Description
31-0	OSDWIN1ADR	0-FFFF FFFFh	OSD window 1 SDRAM source address. The SDRAM source address is an absolute byte address. Note that the address should be aligned on a 32-byte (burst) boundary. As a result, the 5 LSBs are ignored and reading this register will always show the 5 LSBs as 0. VD latches this bit.

6.3.15 Base Pixel X Register (BASEPX)

The base pixel X register (BASEPX) is shown Figure 160 and described in Table 153.

Figure 160. Base Pixel X Register (BASEPX)

31–16
Reserved
R-0

15–10	9–0
Reserved	BPX
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 153. Base Pixel X Register (BASEPX) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Reserved
9-0	BPX	0-3FFh	Base pixel in X. Horizontal base display reference position for all windows. Specified as number of pixels from HD. Value is 24-512. VD latches this bit.

6.3.16 Base Pixel Y Register (BASEPY)

The base pixel Y register (BASEPY) is shown in Figure 161 and described in Table 154.

Figure 161. Base Pixel Y Register (BASEPY)

31–16
Reserved
R-0

15–9	8–0
Reserved	BPY
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 154. Base Pixel Y Register (BASEPY) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	BPY	0-1FFh	Base pixel (Line) in Y. Vertical base display reference position for all windows. Specified as number of pixels (lines) from VD. Value used is MAX(BPY,1); for example, minimum value is 1. VD latches this bit.

6.3.17 Video Window 0 X-Position Register (VIDWIN0XP)

The video window 0 X-position register (VIDWIN0XP) is shown in Figure 162 and described in Table 155.

Figure 162. Video Window 0 X-Position Register (VIDWIN0XP)

31–16
Reserved
R-0

15–10	9–0
Reserved	V0X
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 155. Video Window 0 X-Position Register (VIDWIN0XP) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Reserved
9-0	V0X	0-3FFh	Video window 0 X-position. Horizontal display start position. Number of pixels from display reference position (BASEPX). VD latches this bit.

6.3.18 Video Window 0 Y-Position Register (VIDWIN0YP)

The video window 0 Y-position register (VIDWIN0YP) is shown in Figure 163 and described in Table 156.

Figure 163. Video Window 0 Y-Position Register (VIDWIN0YP)

31–16
Reserved
R-0

15–9	8–0
Reserved	V0Y
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 156. Video Window 0 Y-Position Register (VIDWIN0YP) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	V0Y	0-1FFh	Video window 0 Y-position. Vertical display start position. Number of pixels/lines from display reference position (BASEPY). This bit is latched by VD.

6.3.19 Video Window 0 X-Size Register (VIDWIN0XL)

The video window 0 X-size register (VIDWIN0XL) is shown in Figure 164 and described in Table 157.

Figure 164. Video Window 0 X-Size Register (VIDWIN0XL)

31–16
Reserved
R-0

15–12	11–0
Reserved	V0W
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 157. Video Window 0 X-Size Register (VIDWIN0XL) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reserved
11-0	V0W	0-FFFh	Video window 0 X-width. Horizontal display width in pixels. VD latches this bit.

6.3.20 Video Window 0 Y-Size Register (VIDWIN0YL)

The video window 0 Y-size register (VIDWIN0YL) is shown in Figure 165 and described in Table 158.

Figure 165. Video Window 0 Y-Size Register (VIDWIN0YL)

31–16
Reserved
R-0

15–11	10–0
Reserved	V0H
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 158. Video Window 0 Y-Size Register (VIDWIN0YL) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	V0H	0-7FFh	Video window 0 Y-height. Vertical display height in pixels/lines. In frame mode, specify in terms of lines/field. VD latches this bit.

6.3.21 Video Window 1 X-Position Register (VIDWIN1XP)

The video window 1 X-position register (VIDWIN1XP) is shown in Figure 166 and described in Table 159.

Figure 166. Video Window 1 X-Position Register (VIDWIN1XP)

31–16
Reserved
R-0

15–10	9–0
Reserved	V1X
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 159. Video Window 1 X-Position Register (VIDWIN1XP) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Reserved
9-0	V1X	0-3FFh	Video window 1 X-position. Horizontal display start position. Number of pixels from display reference position (BASEPX). VD latches this bit.

6.3.22 Video Window 1 Y-Position Register (VIDWIN1YP)

The video window 1 Y-position register (VIDWIN1YP) is shown in Figure 167 and described in Table 160.

Figure 167. Video Window 1 Y-Position Register (VIDWIN1YP)

31–16
Reserved
R-0

15–9	8–0
Reserved	V1Y
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 160. Video Window 1 Y-Position Register (VIDWIN1YP) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	V1Y	0-1FFh	Video window 1 Y-position. Vertical display start position. Number of pixels/lines from display reference position (BASEPY). VD latches this bit.

6.3.23 Video Window 1 X-Size Register (VIDWIN1XL)

The video window 1 X-size register (VIDWIN1XL) is shown in Figure 168 and described in Table 161.

Figure 168. Video Window 1 X-Size Register (VIDWIN1XL)

31	16
Reserved	
R-0	

15 – 12	11 – 0
Reserved	V1W
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 161. Video Window 1 X-Size Register (VIDWIN1XL) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reserved
11-0	V1W	0-FFFh	Video window 1 X-width. Horizontal display width in pixels. VD latches this bit.

6.3.24 Video Window 1 Y-Size Register (VIDWIN1YL)

The video window 1 Y-size register (VIDWIN1YL) is shown in Figure 169 and described in Table 162.

Figure 169. Video Window 1 Y-Size Register (VIDWIN1YL)

31	16
Reserved	
R-0	

15 – 11	10 – 0
Reserved	V1H
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 162. Video Window 1 Y-Size Register (VIDWIN1YL) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	V1H	0-7FFh	Video window 1 Y-height. Vertical display height in pixels/lines. In frame mode, specify in terms of lines/field. VD latches this bit.

6.3.25 OSD Bitmap Window 0 X-Position Register (OSDWIN0XP)

The OSD bitmap window 0 X-position register (OSDWIN0XP) is shown in Figure 170 and described in Table 163.

Figure 170. OSD Bitmap Window 0 X-Position Register (OSDWIN0XP)

31–16
Reserved
R-0

15–10	9–0
Reserved	W0X
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 163. OSD Bitmap Window 0 X-Position Register (OSDWIN0XP) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Reserved
9-0	W0X	0-3FFh	OSD window 0 X-position. Horizontal display start position. Number of pixels from display reference position (BASEPX). VD latches this bit.

6.3.26 OSD Bitmap Window 0 Y-Position Register (OSDWIN0YP)

The OSD bitmap window 0 Y-position register (OSDWIN0YP) is shown in Figure 171 and described in Table 164.

Figure 171. OSD Bitmap Window 0 Y-Position Register (OSDWIN0YP)

31–16
Reserved
R-0

15–9	8–0
Reserved	W0Y
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 164. OSD Bitmap Window 0 Y-Position Register (OSDWIN0YP) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	W0Y	0-1FFh	OSD window 0 Y-position. Vertical display start position. Number of pixels/lines from display reference position (BASEPY). VD latches this bit.

6.3.27 OSD Bitmap Window 0 X-Size Register (OSDWIN0XL)

The OSD bitmap window 0 X-size register (OSDWIN0XL) is shown in Figure 172 and described in Table 165.

Figure 172. OSD Bitmap Window 0 X-Size Register (OSDWIN0XL)

31–16
Reserved
R-0

15–12	11–0
Reserved	W0W
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 165. OSD Bitmap Window 0 X-Size Register (OSDWIN0XL) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reserved
11-0	W0W	0-FFFh	OSD window 0 X-width. Horizontal display width in pixels. VD latches this bit.

6.3.28 OSD Bitmap Window 0 Y-Size Register (OSDWIN0YL)

The OSD Bitmap Window 0 Y-Size Register (OSDWIN0YL) is shown in Figure 173 and described in Table 166.

Figure 173. OSD Bitmap Window 0 Y-Size Register (OSDWIN0YL)

31–16
Reserved
R-0

15–11	10–0
Reserved	W0H
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 166. OSD Bitmap Window 0 Y-Size Register (OSDWIN0YL) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	W0H	0-7FFh	OSD window 0 Y-height. Vertical display height in pixels/lines. In frame mode, specify in terms of lines/field. This bit is latched by VD.

6.3.29 OSD Bitmap Window 1 X-Position Register (OSDWIN1XP)

The OSD bitmap window 1 X-position register (OSDWIN1XP) is shown in Figure 174 and described in Table 167.

Figure 174. OSD Bitmap Window 1 X-Position Register (OSDWIN1XP)

31–16
Reserved
R-0

15–10	9–0
Reserved	W1X
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 167. OSD Bitmap Window 1 X-Position Register (OSDWIN1XP) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Reserved
9-0	W1X	0-FF	OSD window 1 X-position. Horizontal display start position. Number of pixels from display reference position (BASEPX). VD latches this bit.

6.3.30 OSD Bitmap Window 1 Y-Position Register (OSDWIN1YP)

The OSD bitmap window 1 Y-position register (OSDWIN1YP) is shown in Figure 175 and described in Table 168.

Figure 175. OSD Bitmap Window 1 Y-Position Register (OSDWIN1YP)

31–16
Reserved
R-0

15–9	8–0
Reserved	W1Y
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 168. OSD Bitmap Window 1 Y-Position Register (OSDWIN1YP) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	W1Y	0-1FFh	OSD window 1 Y-position. Vertical display start position. Number of pixels/lines from display reference position (BASEPY). This bit is latched by VD.

6.3.31 OSD Bitmap Window 1 X-Size Register (OSDWIN1XL)

The OSD bitmap window 1 X-size register (OSDWIN1XL) is shown in Figure 176 and described in Table 169.

Figure 176. OSD Bitmap Window 1 X-Size Register (OSDWIN1XL)

31–16
Reserved
R-0

15–12	11–0
Reserved	W1W
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 169. OSD Bitmap Window 1 X-Size Register (OSDWIN1XL) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reserved
11-0	W1W	0-FFFh	OSD window 1 X-width. Horizontal display width in pixels. This bit is latched by VD.

6.3.32 OSD Bitmap Window 1 Y-Size Register (OSDWIN1YL)

The OSD bitmap window 1 Y-size register (OSDWIN1YL) is shown in Figure 177 and described in Table 170.

Figure 177. OSD Bitmap Window 1 Y-Size Register (OSDWIN1YL)

31–16
Reserved
R-0

15–11	10–0
Reserved	W1H
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 170. OSD Bitmap Window 1 Y-Size Register (OSDWIN1YL) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	W1H	0-7FFh	OSD window 1 Y-height. Vertical display height in pixels/lines. In frame mode, specify in terms of lines/field. VD latches this bit.

6.3.33 Rectangular Cursor Window X-Position Register (CURXP)

The rectangular cursor window X-position register (CURXP) is shown in Figure 178 and described in Table 171.

Figure 178. Rectangular Cursor Window X-Position Register (CURXP)

31	16
Reserved	
R-0	

15 - 10	9 - 0
Reserved	RCSX
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 171. Rectangular Cursor Window X-Position Register (CURXP) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Reserved
9-0	RCSX	0-3FFh	Rectangular cursor window X-position. Horizontal display start position. Number of pixels from display reference position (BASEPX). This bit is latched by VD.

6.3.34 Rectangular Cursor Window Y-Position Register (CURYP)

The rectangular cursor window Y-position register (CURYP) is shown in Figure 179 and described in Table 172.

Figure 179. Rectangular Cursor Window Y-Position Register (CURYP)

31	16
Reserved	
R-0	

15 - 9	8 - 0
Reserved	RCSY
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 172. Rectangular Cursor Window Y-Position Register (CURYP) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	RCSY	0-1FFh	Rectangular cursor window Y-position. Vertical display start position. Number of pixels from display reference position (BASEPY). This bit is latched by VD.

6.3.35 Rectangular Cursor Window X-Size Register (CURXL)

The rectangular cursor window X-size register (CURXL) is shown in Figure 180 and described in Table 173.

Figure 180. Rectangular Cursor Window X-Size Register (CURXL)

31	16
Reserved	
R-0	

15	12	11	0
Reserved		RCSW	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 173. Rectangular Cursor Window X-Size Register (CURXL) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reserved
11-0	RCSW	0-FFFh	Rectangular cursor window X-width. Horizontal display width in pixels. VD latches this bit.

6.3.36 Rectangular Cursor Window Y-Size Register (CURYL)

The rectangular cursor window Y-size register (CURYL) is shown in Figure 181 and described in Table 174.

Figure 181. Rectangular Cursor Window Y-Size Register (CURYL)

31	16
Reserved	
R-0	

15	11	10	0
Reserved		RCSH	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 174. Rectangular Cursor Window Y-Size Register (CURYL) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	RCSH	0-7FFh	Rectangular cursor window Y-height. Vertical display height in pixels/lines. In frame mode, specify in terms of lines/field. VD latches this bit.

6.3.37 Window 0 Bitmap Value to Palette Map 0/1 Register (W0BMP01)

The window 0 bitmap value to palette map 0/1 register (W0BMP01) is shown in Figure 182 and described in Table 175.

Figure 182. Window 0 Bitmap Value to Palette Map 0/1 Register (W0BMP01)

31–16	
Reserved	
R-0	

15–8	7–0
PAL01	PAL00
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 175. Window 0 Bitmap Value to Palette Map 0/1 Register (W0BMP01) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL01	0-FFh	Palette address for bitmap value [1,x,x] - OSD window 0 [4-bit, 2-bit, 1-bit]
7-0	PAL00	0-FFh	Palette address for bitmap value [0,0,0] - OSD window 0 [4-bit, 2-bit, 1-bit]

6.3.38 Window 0 Bitmap Value to Palette Map 2/3 Register (W0BMP23)

The window 0 bitmap value to palette map 2/3 register (W0BMP23) is shown in Figure 183 and described in Table 176.

Figure 183. Window 0 Bitmap Value to Palette Map 2/3 Register (W0BMP23)

31–16	
Reserved	
R-0	

15–8	7–0
PAL03	PAL02
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 176. Window 0 Bitmap Value to Palette Map 2/3 Register (W0BMP23) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL03	0-FFh	Palette address for bitmap value [3,x,x] - OSD window 0 [4-bit, 2-bit, 1-bit]
7-0	PAL02	0-FFh	Palette address for bitmap value [2,x,x] - OSD window 0 [4-bit, 2-bit, 1-bit]

6.3.39 Window 0 Bitmap Value to Palette Map 4/5 Register (W0BMP45)

The window 0 bitmap value to palette map 4/5 register (W0BMP45) is shown in Figure 184 and described in Table 177.

Figure 184. Window 0 Bitmap Value to Palette Map 4/5 Register (W0BMP45)

31–16
Reserved
R-0

15–8	7–0
PAL05	PAL04
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 177. Window 0 Bitmap Value to Palette Map 4/5 Register (W0BMP45) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL05	0-FFh	Palette address for bitmap value [5,1,x] - OSD window 0 [4-bit, 2-bit, 1-bit]
7-0	PAL04	0-FFh	Palette address for bitmap value [4,x,x] - OSD window 0 [4-bit, 2-bit, 1-bit]

6.3.40 Window 0 Bitmap Value to Palette Map 6/7 Register (W0BMP67)

The window 0 bitmap value to palette map 6/7 register (W0BMP67) is shown in Figure 185 and described in Table 178.

Figure 185. Window 0 Bitmap Value to Palette Map 6/7 Register (W0BMP67)

31–16
Reserved
R-0

15–8	7–0
PAL07	PAL06
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 178. Window 0 Bitmap Value to Palette Map 6/7 Register (W0BMP67) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL07	0-FFh	Palette address for bitmap value [7,x,x] - OSD window 0 [4-bit, 2-bit, 1-bit]
7-0	PAL06	0-FFh	Palette address for bitmap value [6,x,x] - OSD window 0 [4-bit, 2-bit, 1-bit]

6.3.41 Window 0 Bitmap Value to Palette Map 8/9 Register (W0BMP89)

The window 0 bitmap value to palette map 8/9 register (W0BMP89) is shown in Figure 186 and described in Table 179.

Figure 186. Window 0 Bitmap Value to Palette Map 8/9 Register (W0BMP89)

31–16
Reserved
R-0

15–8	7–0
PAL09	PAL08
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 179. Window 0 Bitmap Value to Palette Map 8/9 Register (W0BMP89) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL09	0-FFh	Palette address for bitmap value [9,x,x] - OSD window 0 [4-bit, 2-bit, 1-bit]
7-0	PAL08	0-FFh	Palette address for bitmap value [8,x,x] - OSD window 0 [4-bit, 2-bit, 1-bit]

6.3.42 Window 0 Bitmap Value to Palette Map A/B Register (W0BMPAB)

The window 0 bitmap value to palette map A/B register (W0BMPAB) is shown in Figure 187 and described in Table 180.

Figure 187. Window 0 Bitmap Value to Palette Map A/B Register (W0BMPAB)

31–16
Reserved
R-0

15–8	7–0
PAL11	PAL10
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 180. Window 0 Bitmap Value to Palette Map A/B Register (W0BMPAB) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL11	0-FFh	Palette address for bitmap value [B,x,x] - OSD window 0 [4-bit, 2-bit, 1-bit]
7-0	PAL10	0-FFh	Palette address for bitmap value [A,2,x] - OSD window 0 [4-bit, 2-bit, 1-bit]

6.3.43 Window 0 Bitmap Value to Palette Map C/D Register (W0BMPCD)

The window 0 bitmap value to palette map C/D register (W0BMPCD) is shown in Figure 188 and described in Table 181.

Figure 188. Window 0 Bitmap Value to Palette Map C/D Register (W0BMPCD)

31–16
Reserved
R-0

15–8	7–0
PAL13	PAL12
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 181. Window 0 Bitmap Value to Palette Map C/D Register (W0BMPCD) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL13	0-FFh	Palette address for bitmap value [D,x,x] - OSD window 0 [4-bit, 2-bit, 1-bit]
7-0	PAL12	0-FFh	Palette address for bitmap value [C,x,x] - OSD window 0 [4-bit, 2-bit, 1-bit]

6.3.44 Window 0 Bitmap Value to Palette Map E/F Register (W0BMPEF)

The window 0 bitmap value to palette map E/F register (W0BMPEF) is shown in Figure 189 and described in Table 182.

Figure 189. Window 0 Bitmap Value to Palette Map E/F Register (W0BMPEF)

31–16
Reserved
R-0

15–8	7–0
PAL15	PAL14
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 182. Window 0 Bitmap Value to Palette Map E/F Register (W0BMPEF) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL15	0-FFh	Palette address for bitmap value [F,3,1] - OSD window 0 [4-bit, 2-bit, 1-bit]
7-0	PAL14	0-FFh	Palette address for bitmap value [E,x,x] - OSD window 0 [4-bit, 2-bit, 1-bit]

6.3.45 Window 1 Bitmap Value to Palette Map 0/1 Register (W1BMP01)

The window 1 bitmap value to palette map 0/1 register (W1BMP01) is shown in Figure 190 and described in Table 183.

Figure 190. Window 1 Bitmap Value to Palette Map 0/1 Register (W1BMP01)

31–16
Reserved
R-0

15–8	7–0
PAL01	PAL00
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 183. Window 1 Bitmap Value to Palette Map 0/1 Register (W1BMP01) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL01	0-FFh	Palette address for bitmap value [1,x,x] - OSD window 1 [4-bit, 2-bit, 1-bit]
7-0	PAL00	0-FFh	Palette address for bitmap value [0,0,0] - OSD window 1 [4-bit, 2-bit, 1-bit]

6.3.46 Window 1 Bitmap Value to Palette Map 2/3 Register (W1BMP23)

The window 1 bitmap value to palette map 2/3 register (W1BMP23) is shown in Figure 191 and described in Table 184.

Figure 191. Window 1 Bitmap Value to Palette Map 2/3 Register (W1BMP23)

31–16
Reserved
R-0

15–8	7–0
PAL03	PAL02
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 184. Window 1 Bitmap Value to Palette Map 2/3 Register (W1BMP23) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL03	0-FFh	Palette address for bitmap value [3,x,x] - OSD window 1 [4-bit, 2-bit, 1-bit]
7-0	PAL02	0-FFh	Palette address for bitmap value [2,x,x] - OSD window 1 [4-bit, 2-bit, 1-bit]

6.3.47 Window 1 Bitmap Value to Palette Map 4/5 Register (W1BMP45)

The window 1 bitmap value to palette map 4/5 register (W1BMP45) is shown in Figure 192 and described in Table 185.

Figure 192. Window 1 Bitmap Value to Palette Map 4/5 Register (W1BMP45)

31–16
Reserved
R-0

15–8	7–0
PAL05	PAL04
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 185. Window 1 Bitmap Value to Palette Map 4/5 Register (W1BMP45) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL05	0-FFh	Palette address for bitmap value [5,1,x] - OSD window 1 [4-bit, 2-bit, 1-bit]
7-0	PAL04	0-FFh	Palette address for bitmap value [4,x,x] - OSD window 1 [4-bit, 2-bit, 1-bit]

6.3.48 Window 1 Bitmap Value to Palette Map 6/7 Register (W1BMP67)

The window 1 bitmap value to palette map 6/7 register (W1BMP67) is shown in Figure 193 and described in Table 186.

Figure 193. Window 1 Bitmap Value to Palette Map 6/7 Register (W1BMP67)

31–16
Reserved
R-0

15–8	7–0
PAL07	PAL06
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 186. Window 1 Bitmap Value to Palette Map 6/7 Register (W1BMP67) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL07	0-FFh	Palette address for bitmap value [7,x,x] - OSD window 1 [4-bit, 2-bit, 1-bit]
7-0	PAL06	0-FFh	Palette address for bitmap value [6,x,x] - OSD window 1 [4-bit, 2-bit, 1-bit]

6.3.49 Window 1 Bitmap Value to Palette Map 8/9 Register (W1BMP89)

The window 1 bitmap value to palette map 8/9 register (W1BMP89) is shown in Figure 194 and described in Table 187.

Figure 194. Window 1 Bitmap Value to Palette Map 8/9 Register (W1BMP89)

31		16
	Reserved	
	R-0	

15	8	7	0
PAL09		PAL08	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 187. Window 1 Bitmap Value to Palette Map 8/9 Register (W1BMP89) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL09	0-FFh	Palette address for bitmap value [9,x,x] - OSD window 1 [4-bit, 2-bit, 1-bit]
7-0	PAL08	0-FFh	Palette address for bitmap value [8,x,x] - OSD window 1 [4-bit, 2-bit, 1-bit]

6.3.50 Window 1 Bitmap Value to Palette Map A/B Register (W1BMPAB)

The window 1 bitmap value to palette map A/B register (W1BMPAB) is shown in Figure 195 and described in Table 188.

Figure 195. Window 1 Bitmap Value to Palette Map A/B Register (W1BMPAB)

31		16
	Reserved	
	R-0	

15	8	7	0
PAL11		PAL10	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 188. Window 1 Bitmap Value to Palette Map A/B Register (W1BMPAB) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL11	0-FFh	Palette address for bitmap value [B,x,x] - OSD window 1 [4-bit, 2-bit, 1-bit]
7-0	PAL10	0-FFh	Palette address for bitmap value [A,2,x] - OSD window 1 [4-bit, 2-bit, 1-bit]

6.3.51 Window 1 Bitmap Value to Palette Map C/D Register (W1BMPCD)

The window 1 bitmap value to palette map C/D register (W1BMPCD) is shown in Figure 196 and described in Table 189.

Figure 196. Window 1 Bitmap Value to Palette Map C/D Register (W1BMPCD)

31–16
Reserved
R-0

15–8	7–0
PAL13	PAL12
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 189. Window 1 Bitmap Value to Palette Map C/D Register (W1BMPCD) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL13	0-FFh	Palette address for bitmap value [D,x,x] - OSD window 1 [4-bit, 2-bit, 1-bit]
7-0	PAL12	0-FFh	Palette address for bitmap value [C,x,x] - OSD window 1 [4-bit, 2-bit, 1-bit]

6.3.52 Window 1 Bitmap Value to Palette Map E/F Register (W1BMPEF)

The window 1 bitmap value to palette map E/F register (W1BMPEF) is shown in Figure 197 and described in Table 190.

Figure 197. Window 1 Bitmap Value to Palette Map E/F Register (W1BMPEF)

31–16
Reserved
R-0

15–8	7–0
PAL15	PAL14
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 190. Window 1 Bitmap Value to Palette Map E/F Register (W1BMPEF) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	PAL15	0-FFh	Palette address for bitmap value [F,3,1] - OSD window 1 [4-bit, 2-bit, 1-bit]
7-0	PAL14	0-FFh	Palette address for bitmap value [E,x,x] - OSD window 1 [4-bit, 2-bit, 1-bit]

6.3.53 Miscellaneous Control Register (MISCCTL)

The miscellaneous control register (MISCCTL) is shown in Figure 198 and described in Table 191.

Figure 198. Miscellaneous Control Register (MISCCTL)

31–16
Reserved
R-0

15–13	12	11	10	9	8
Reserved	VIDOVRLMODE	VFINV	Reserved	ATN0E	ATN1E
R-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
RGBEN	RGBWIN	Reserved	RSEL	CPBSY	PPSW	PPRV	Reserved
R/W-0	R/W-0	R-0	R/W-0	R-0	R/W-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 191. Miscellaneous Control Register (MISCCTL) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12	VIDOVRLMODE		Controls the mask signal that can stop assertion of the data request signal to DDR of the hidden area of video window 0. This bit is effective if video window 0 and video window 1 are displayed with shared area.
			Note that if the video window overlay mode is disabled (VIDOVRLMODE = 0), the position of video window 0 (VIDWIN0) may be shifted when overlaid by certain sizes of video window 1 (VIDWIN1) at certain locations.
		0	Shared data between VIDWIN0 and VIDWIN1 is not fetched from memory.
		1	Shared data between VIDWIN0 and VIDWIN1 is fetched from memory.
11	VFINV		Video window 0/1 expansion filter coefficient inverse. When V1EFC or V0EFC is set, this bit is valid.
		0	Inversed
		1	Normal
10	Reserved	0	Reserved
9	ATN0E		Attenuation enable for REC601.
		0	Normal levels (Y 0-255, Cr 0-255, Cb 0-255)
		1	Attenuated levels (Y 16-235, Cr 16-240, Cb 16-240), only active when OSDWIN1 is not setup as an attribute window.
8	ATN1E		Attenuation enable for REC601. OASW = 0 in the OSD window 1 mode setup register (OSDWIN1MD).
		0	Normal levels (Y 0-255, Cr 0-255, Cb 0-255)
		1	Attenuated levels (Y 16-235, Cr 16-240, Cb 16-240)
7	RGBEN		Video window RGB mode enable.
		0	Disable
		1	Enable
6	RGBWIN		Video window to use for RGB mode.
		0	Video window 0
		1	Video window 1
5	Reserved	0	Reserved
4	RSEL		CLUT ROM selection.
		0	CLUT0
		1	CLUT1

Table 191. Miscellaneous Control Register (MISCCTL) Field Descriptions (continued)

Bit	Field	Value	Description
3	CPBSY		CLUT write busy. Used when writing CLUT data to RAM.
		0	Not busy, okay to write
		1	Busy, do not write
2	PPSW		Ping-pong buffer toggle select.
			When PPRV = 0:
		0	Use address in VIDWIN0ADR
		1	Use address in PPVWIN0ADR
			When PPRV = 1:
		0	Use address in PPVWIN0ADR
		1	Use address in VIDWIN0ADR
1	PPRV		Ping-pong buffer reverse. Inverts polarity of internal select signal. Affects PPSW bit.
0	Reserved	0	Reserved

6.3.54 CLUT RAMYCB Setup Register (CLUTRAMYCB)

The CLUT RAMYCB setup register (CLUTRAMYCB) is shown in Figure 199 and described in Table 192.

Figure 199. CLUT RAMYCB Setup Register (CLUTRAMYCB)

31–16
Reserved
R-0

15–8	7–0
Y	CB
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 192. CLUT RAMYCB Setup Register (CLUTRAMYCB) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	Y	0-FFh	Write data (Y) into built-in CLUT RAM.
7-0	CB	0-FFh	Write data (Cb) into built-in CLUT RAM.

6.3.55 CLUT RAMCR Setup Register (CLUTRAMCR)

The CLUT RAMCR setup register (CLUTRAMCR) is shown in Figure 200 and described in Table 193.

Figure 200. CLUT RAMCR Setup Register (CLUTRAMCR)

31–16
Reserved
R-0

15–8	7–0
CR	CADDR
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 193. CLUT RAMCR Setup Register (CLUTRAMCR) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-8	CR	0-FFh	Write data (Cr) into built-in CLUT RAM.
7-0	CADDR	0-FFh	CLUT write pallette address.

6.3.56 Transparency Value Setup Register (TRANSPVAL)

The transparency value setup register (TRANSPVAL) is shown in Figure 201 and described in Table 194.

Figure 201. Transparency Value Setup Register (TRANSPVAL)

31–16
Reserved
R-0

15–0
RGBTRANS
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 194. Transparency Value Setup Register (TRANSPVAL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-0	RGBTRANS	0-FFFFh	OSD window transparency value for RGB565 input mode.

6.3.57 Ping-Pong Video Window 0 Address Register (PPVWIN0ADR)

The ping-pong video window 0 address register (PPVWIN0ADR) is shown in Figure 202 and described in Table 195.

Figure 202. Ping-Pong Video Window 0 Address Register (PPVWIN0ADR)

31–0
PPVWIN0ADR
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 195. Ping-Pong Video Window 0 Address Register (PPVWIN0ADR) Field Descriptions

Bit	Field	Value	Description
31-0	PPVWIN0ADR	0-FFFF FFFFh	Ping-pong video window 0 address. The SDRAM source address is an absolute byte address. Note that the address should be aligned on a 32-byte (burst) boundary. As a result, the 5 LSBs are ignored and reading this register will always show the 5 LSBs as 0. VD latches this bit.

7 Video Processing Subsystem (VPSS) Registers

This section discusses the registers in the video processor subsystem (VPSS). Table 196 lists the memory-mapped registers for the VPSS. See the device-specific data manual for the memory address of these registers.

Table 196. Video Processing Subsystem (VPSS) Registers

Offset	Acronym	Register Description	Section
3400h	PID	VPSS Peripheral Revision and Class Information	Section 7.1
3404h	PCR	VPSS Peripheral Control Register	Section 7.2
3508h	SDR_REQ_EXP	SDRAM Non-Real-Time Read Request Expand Register	Section 7.3

7.1 *VPSS Peripheral Revision and Class Information Register (PID)*

The VPSS peripheral revision and class information register (PID) is shown in Figure 203 and described in Table 197.

Figure 203. VPSS Peripheral Revision and Class Information Register (PID)

31–24	23–16
Reserved	TID
R-0	R-1

15–8	7–0
CID	PREV
R-FBh	R-0

LEGEND: R = Read only; -*n* = value after reset

Table 197. VPSS Peripheral Revision and Class Information Register (PID) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Reserved
23-16	TID	0-FFh	Peripheral identification
		1	VPSS
15-8	CID	0-FFh	Class identification
		FBh	VPSS
7-0	PREV	0-FFh	Peripheral revision number
		0	Initial revision

7.2 VPSS Peripheral Control Register (PCR)

The VPSS peripheral control register (PCR) is shown in Figure 204 and described in Table 198.

Figure 204. VPSS Peripheral Control Register (PCR)

31–24							
Reserved							
R-0							

23	22	21	20	19	18	17	16
CCDC_WBL_O	PRV_WBL_O	RSZ1_WBL_O	RSZ2_WBL_O	RSZ3_WBL_O	RSZ4_WBL_O	AF_WBL_O	AEW_WBL_O
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

15–4	3–0
Reserved	DMA_PRI
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 198. VPSS Peripheral Control Register (PCR) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Reserved
23	CCDC_WBL_O		Write buffer memory overflow (CCDC). All data units have been filled and not yet transferred to SDRAM before the next data unit is to be filled from the WBL. Software has to clear the bit.
		0	No overflow.
		1	Overflow (fail).
22	PRV_WBL_O		Write buffer memory overflow (Preview engine). All data units have been filled and not yet transferred to SDRAM before the next data unit is to be filled from the WBL. Software has to clear the bit.
		0	No overflow.
		1	Overflow (fail).
21	RSZ1_WBL_O		Write buffer memory overflow (Resizer line 1). All data units have been filled and not yet transferred to SDRAM before the next data unit is to be filled from the WBL. Software has to clear the bit.
		0	No overflow.
		1	Overflow (fail).
20	RSZ2_WBL_O		Write buffer memory overflow (Resizer line 2). All data units have been filled and not yet transferred to SDRAM before the next data unit is to be filled from the WBL. Software has to clear the bit.
		0	No overflow.
		1	Overflow (fail).
19	RSZ3_WBL_O		Write buffer memory overflow (Resizer line 3). All data units have been filled and not yet transferred to SDRAM before the next data unit is to be filled from the WBL. Software has to clear the bit.
		0	No overflow.
		1	Overflow (fail).
18	RSZ4_WBL_O		Write buffer memory overflow (Resizer line 4). All data units have been filled and not yet transferred to SDRAM before the next data unit is to be filled from the WBL. Software has to clear the bit.
		0	No overflow.
		1	Overflow (fail).
17	AF_WBL_O		Write buffer memory overflow (AF). All data units have been filled and not yet transferred to SDRAM before the next data unit is to be filled from the WBL. Software has to clear the bit.
		0	No overflow.
		1	Overflow (fail).

Table 198. VPSS Peripheral Control Register (PCR) Field Descriptions (continued)

Bit	Field	Value	Description
16	AEW_WBL_O		Write buffer memory overflow (AE/AWB). All data units have been filled and not yet transferred to SDRAM before the next data unit is to be filled from the WBL. Software has to clear the bit.
		0	No overflow.
		1	Overflow (fail).
15-4	Reserved	0	Reserved
3-0	DMI_PRI	0-Fh	VBUSM priority in the system to the DDR EMIF. The default should be the highest priority in the system.

7.3 SDRAM Non-Real-Time Read Request Expand Register (SDR_REQ_EXP)

The SDRAM non real-time read request expand (SDR_REQ_EXP) register is shown in Figure 205 and described in Table 199.

Figure 205. SDRAM Non-Real-Time Read Request Expand Register (SDR_REQ_EXP)

31-30	29-20	19-16
Reserved	PRV_EXP	RESZ_EXP
R-0	R/W-0	R/W-0

15-10	9-0
RESZ_EXP	HIST_EXP
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 199. SDRAM Non-Real-Time Read Request Expand Register (SDR_REQ_EXP) Field Descriptions

Bit	Field	Value	Description
31-30	Reserved	0	Reserved
29-20	PRV_EXP	0-3FFh	Preview read request expand. Delay to allow between consecutive read requests from the preview module. Units are in VPSS clock cycles (153/198 MHz in Normal/Turbo modes). Since the VPSS DMA priority is typically set to the highest for real-time requirements, this is for spreading any non-real-time reads with respect to the other traffic in the system. This minimizes the potential of locking out other requests for the duration of a frame being read from DDR/SDR.
19-10	RESZ_EXP	0-3FFh	Resizer read request expand. Delay to allow between consecutive read requests from the resizer module. Units are 32 VPSS clock cycles (153/198 MHz in Normal/Turbo modes). The delay is RESZ_EXP × 32 VPSS clock cycles. Since the VPSS DMA priority is typically set to the highest for real-time requirements, this is for spreading any non-real-time reads with respect to the other traffic in the system. This minimizes the potential of locking out other requests for the duration of a frame being read from DDR/SDR.
9-0	HIST_EXP	0-3FFh	Histogram read request expand. Delay to allow between consecutive read requests from the histogram module. Units are in VPSS clock cycles (153/198 MHz in Normal/Turbo modes). Since the VPSS DMA priority is typically set to the highest for real-time requirements, this is for spreading any non-real-time reads with respect to the other traffic in the system. This minimizes the potential of locking out other requests for the duration of a frame being read from DDR/SDR.

Appendix A Revision History

Table A-1 lists the changes made since the previous version of this document.

Table A-1. Document Revision History

Reference	Additions/Modifications/Deletions
Section 1.2	Added second paragraph.
Section 1.2.1	Changed first bulleted item in second paragraph (restrictions).
Section 1.2.2	Added NOTE.
Table 8	Deleted CSYNC from COUT3 pin.
Section 2.2.1.1	Changed third paragraph.
Section 2.2.2.1	Deleted fourth paragraph.
Section 2.2.3.1	Changed second paragraph.
Figure 18	Changed RGB output signal.
Table 29	Added NOTE.
Table 32	Added table. Subsequent tables renumbered.
Table 35	Added table. Subsequent tables renumbered.
Section 4.4.1.2	Added NOTE.
	Changed paragraph.
Section 4.4.3.2	Changed paragraphs.
Figure 46	Changed figure.
Figure 66	Changed figure.
Section 5.4.1	Changed paragraph.
Section 5.4.2	Added NOTE.
Section 5.4.5	Changed first bulleted item.
	Deleted second and third bulleted item.
Section 5.5.1	Changed paragraph.
Section 5.5.2	Added NOTE.
Table 71	Changed Description of VDMD bit.
Figure 80	Changed bits 1-0.
Table 72	Changed bits 1-0.
Table 90	Changed Description of OEE bit.
Section 6.2.67	Added subsection. Subsequent figures and tables renumbered.
Table 140	Changed Description of VHZ1, VVZ1, VFF1, and ACT1 bits.
Figure 156	Changed bits to R/W.
Figure 157	Changed bits to R/W.
Figure 158	Changed bits to R/W.
Figure 159	Changed bits to R/W.
Figure 198	Added bit 12.
Table 191	Added Description for VIDOVRLMODE bit.
	Changed Description of ATN0E bit.
Figure 204	Changed figure.
Table 198	Changed table.