TMS320C672x DSP Software-Programmable Phase-Locked Loop (PLL) Controller

Reference Guide

TEXAS
INSTRUMENTS

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About This Manual

This document describes the operation of the software-programmable phase-locked loop (PLL) controller in the TMS320C672x™ digital signal processors (DSPs) of the TMS320C6000™ DSP family. Refer to the device-specific data manual to determine if the PLL controller is used on a particular device.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the C6000™ devices and related support tools. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the C6000 devices, related peripherals, and other technical collateral, is available in the C6000 DSP product folder at: www.ti.com/c6000.

TMS320C67x/C67x+ DSP CPU and Instruction Set Reference Guide (literature number SPRU733) describes the TMS320C67x™ CPU architecture, instruction set, pipeline, and interrupts for these digital signal processors.

TMS320C672x DSP Peripherals Overview Reference Guide (literature number SPRU723) describes the peripherals available on the TMS320C672x™ DSPs.

TMS320C6000 Technical Brief (literature number SPRU197) gives an introduction to the TMS320C62x™ and TMS320C67x™ DSPs, development tools, and third-party support.

TMS320C6000 Programmer's Guide (literature number SPRU198) describes ways to optimize C and assembly code for the TMS320C6000™ DSPs and includes application program examples.

TMS320C6000 Code Composer Studio Tutorial (literature number SPRU301) introduces the Code Composer Studio™ integrated development environment and software tools.

Code Composer Studio Application Programming Interface Reference Guide (literature number SPRU321) describes the Code Composer Studio™ application programming interface (API), which allows you to program custom plug-ins for Code Composer.

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Phase-Locked Loop (PLL) Controller

This document describes the operation of the software-programmable phase-locked loop (PLL) controller in the TMS320C672x™ digital signal processors (DSP).

1   Overview

The PLL controller (Figure 1) features software-configurable PLL multiplier controller (PLLM), dividers (D0, D1, D2, and D3), and reset controller. The PLL controller accepts an input clock from the CLKIN pin or from the on-chip oscillator output signal OSCIN. The PLL controller offers flexibility and convenience by way of software-configurable multiplier and dividers to modify the input signal internally. The resulting clock outputs are passed to the DSP core, peripherals, and other modules inside the DSP.

- The input reference clocks to the PLL controller:
    - CLKIN: input signal from external oscillator (3.3V)
    - OSCIN: output signal from on-chip oscillator (1.2V)
- The resulting output clocks from the PLL controller:
    - AUXCLK: internal clock output signal directly from CLKIN or OSCIN.
    - SYSCLK1: internal clock output of divider D1.
    - SYSCLK2: internal clock output of divider D2.
    - SYSCLK3: internal clock output of divider D3.

Refer to your device-specific data manual on how these inputs and outputs of the PLL controller are used.

Figure 1. PLL Controller Block Diagram
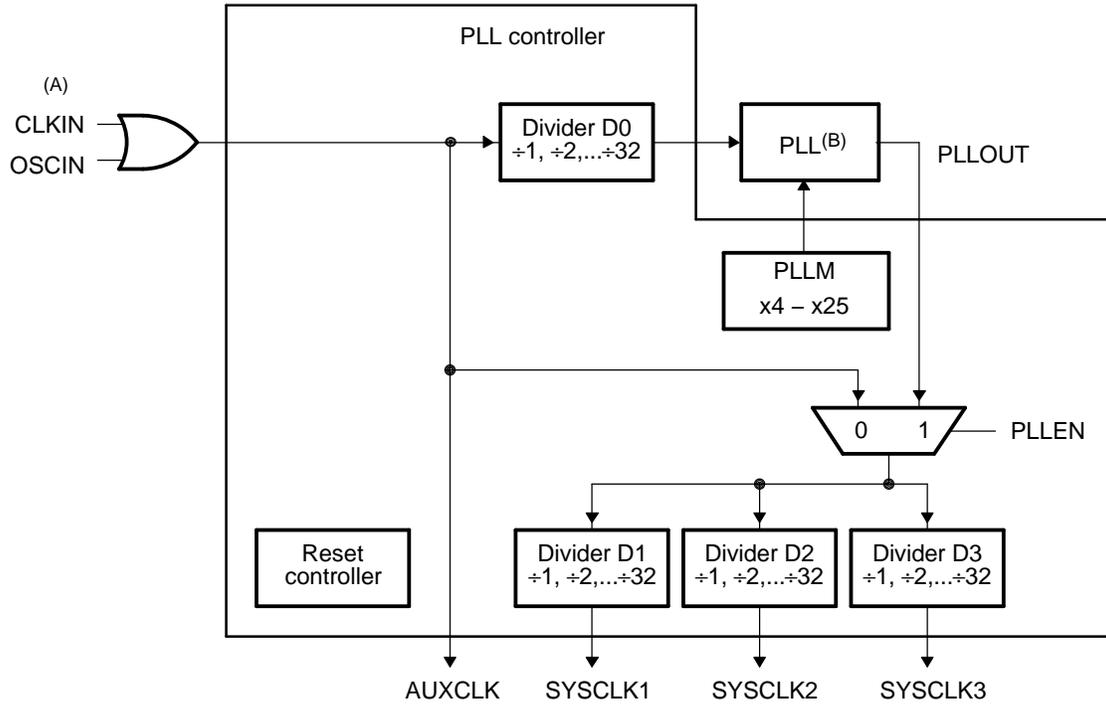
A   See Appendix A for details on how to select between CLKIN and OSCIN.

B   See the device-specific data manual for more detail about the PLL.

2 Functional Description

The following sections describe the multiplier, dividers, and reset controller in the PLL controller.

2.1 Multiplier and Dividers

The PLL controller is capable of programming the PLL through the PLL multiplier control register (PLLM) from a ×4 to ×25 multiplier rate. The clock dividers (D0, D1, D2, and D3) are programmable from a ÷1 to ÷32 divider ratio and may be disabled. When a clock divider is disabled, no clock is output from that clock divider. A divider only outputs a clock when it is enabled in the corresponding PLLDIV*n* register.

The input reference clock (either CLKIN or OSCIN) is directly output as the auxiliary clock (AUXCLK) for use by some peripherals. For example, the multichannel audio serial port (McASP) can use AUXCLK to generate audio clocks.

The divider D0 and the PLL may also be bypassed. The PLL enable bit (PLLEN) in the PLL control/status register (PLLCSR) determines the PLL controller mode. When PLLEN = 1, PLL mode, D0 and PLL are used; when PLLEN = 0, bypass mode, D0 and PLL are bypassed and the input reference clock is directly input to dividers D1, D2, and D3. On the C672x™ DSP, the PLL defaults to bypass mode (PLLEN = 0).

When in PLL mode (PLLEN = 1), the input reference clock is supplied to divider D0. Divider D0 must be enabled (D0EN = 1) in PLL mode. When divider D0 is enabled, the input reference clock is divided down by the value in the PLL divider ratio bits (RATIO) in PLLDIV0. The output from divider D0 is input to the PLL. The PLL multiplies the clock by the value in the PLL multiplier bits (PLLM) in the PLL multiplier control register (PLLM). The output from the PLL (PLLOUT) is input to dividers D1, D2, and D3.

When enabled (D*n*EN = 1), the dividers D1, D2, and D3 divide-down by the RATIO value in PLLDIV*n* the output clock of the PLL. The output clocks of dividers D1, D2, and D3 have 50% duty cycle and are SYSCLK1, SYSCLK2, and SYSCLK3, respectively.

2.2 Reset Controller

At power up, the device $\overline{\text{RESET}}$ signal may not be asserted long enough to wait for the on-chip or off-chip oscillator to stabilize. This means the input reference clock (either CLKIN or OSCIN) may not be a stable clock when a device $\overline{\text{RESET}}$ signal is deasserted high. After $\overline{\text{RESET}}$ is deasserted, the reset controller lengthens the asynchronous internal reset signal to ensure that the input clock source is stable. The reset controller resides within the PLL controller and the main function is to internally lengthen the reset signal from the $\overline{\text{RESET}}$ input pin until the input clock source is stable (after 4096 CLKIN or OSCIN cycles). This is to ensure that the rest of the device will see the internal reset deasserted only after the input clock is stabilized. Figure 2 shows the lengthening of the internal reset signal.

The PLL controller multiplier and dividers are bypassed when the internal reset signal is low. The frequency of all clock outputs of the PLL controller (AUXCLK, SYSCLK1, SYSCLK2, and SYSCLK3) are fixed to the input reference clock (CLKIN or OSCIN) divided by 8. After 4096 CLKIN or OSCIN cycles, the reset controller brings the device out of reset and sets the oscillator input stable bit (STABLE) in the PLL control/status register (PLLCSR). The dividers are used after this point and are set to their default divide ratio.

Values are latched into the registers at the rising edge of $\overline{\text{RESET}}$.

Figure 2. Reset Controller Lengthening the Internal Reset Signal
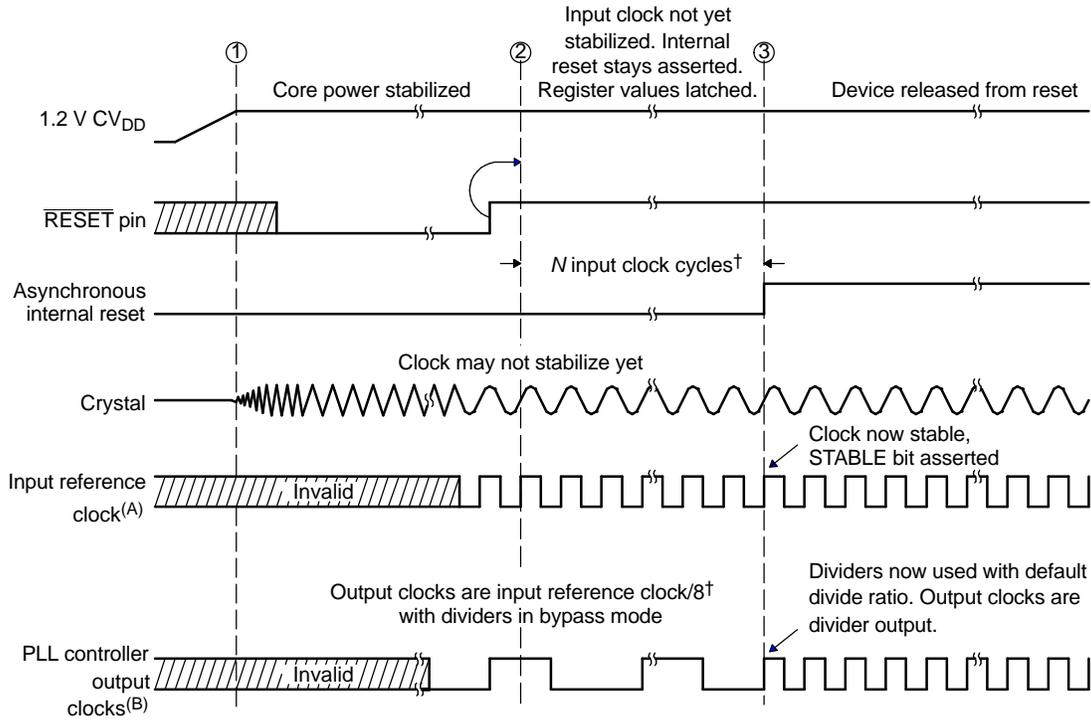
A   N = 4096 × input reference clock (CLKIN or OSCIN cycles)

B   Output clocks include AUXCLK, SYSCLK1, SYSCLK2, and SYSCLK3 at the PLL controller boundary. Refer to the device-specific data manual for clock behavior at the device pins.

3 Configuration

The following sections provide procedures for initialization, power down, and wake up of the PLL controller.

3.1 Initialization

The PLL and PLL controller are to be initialized by software after reset. The PLL controller registers should be modified only by the CPU or via emulation. The HPI should not be used to directly access the PLL controller registers. The initialization of the PLL controller should be performed as soon as possible at the beginning of the program, before initializing any peripherals. Upon device reset, one of the following two software initialization procedures must be done to properly set up the PLL and PLL controller.

3.1.1 Initialization to PLL Mode (PLLEN = 1)

This section shows the initialization sequence, if the system intends to use divider D0 and PLL. This section also shows when you should program the multipliers and dividers, if needed.

1. In PLLCSR, write PLLEN = 0 (bypass mode).
2. Wait 4 cycles of the slowest of PLLOUT or reference clock source (CLKIN or OSCIN).
3. In PLLCSR, write PLLRST = 1 (PLL is reset).
4. If necessary, program PLLDIV0 and PLLM.
5. If necessary, program PLLDIV1-*n*. Note that you must apply the GO operation to change these dividers to new ratios. See Section 3.2.1.
6. Wait for PLL to properly reset. See device-specific data manual for PLL reset time.
7. In PLLCSR, write PLLRST = 0 to bring PLL out of reset.
8. Wait for PLL to lock. See device-specific data manual for PLL lock time.
9. In PLLCSR, write PLLEN = 1 to enable PLL mode.

Steps 1, 2, and 3 are required when PLLEN and PLLRST bits are not already 0 and 1, respectively. These steps are not required when the device is coming out of reset (by default, PLLEN and PLLRST bits are 0 and 1, respectively).

3.1.2 Initialization to Bypass Mode (PLLEN = 0)

This section shows the initialization sequence, if the system intends to bypass divider D0 and PLL. This section also shows when you should program the multipliers and dividers, if needed.

1. In PLLCSR, write PLLEN = 0 (bypass mode).
2. Wait 4 cycles of the slowest of PLLOUT or reference clock source (CLKIN or OSCIN).
3. In PLLCSR, write PLLRST = 1 (PLL is reset).
4. It is not necessary to program PLLDIV0 and PLLM.
5. If necessary, program PLLDIV1-*n*. Note that you must apply the GO operation to change these dividers to new ratios. See Section 3.2.1.

Steps 1, 2, and 3 are required when PLLEN and PLLRST bits are not already 0 and 1, respectively. These steps are not required when the device is coming out of reset (by default, PLLEN and PLLRST bits are 0 and 1, respectively).

3.2 Changing Divider/Multiplier Ratio

This section discusses how to change the various divider/multiplier ratios.

3.2.1 Divider *n* (D1 to D*n*) and GO Operation

The GO operation is required to change the divider ratios of D1 to D*n*. Section 3.2.1.1 discusses the GO operation. Section 3.2.1.2 gives the software steps required to change the divider ratios.

3.2.1.1 GO Operation

Writes to the RATIO field in PLLDIV1-PLLDIV3 do not change the dividers' actual divide ratios immediately. The PLLDIV*n* dividers only change to the new RATIO rates during a GO operation. This section discusses the GO operation and how the SYSCLKs are aligned.

The PLL controller clock align control register (ALNCTL) determines which SYSCLKs must be aligned. Before a GO operation, you must program ALNCTL according to the device-specific data manual requirement so that the appropriate clocks are aligned during the GO operation. All SYSCLKs must be aligned; therefore, the ALN*n* bits in ALNCTL should always be set to 1 before a GO operation.

A GO operation is initiated by setting the GOSET bit in PLLCMD to 1. During a GO operation:

- Any SYSCLK*n* with the corresponding ALN*n* bit in ALNCTL set to 1 is paused at the low edge. Then the PLL controller restarts all these SYSCLKs simultaneously, aligned at the rising edge. When the SYSCLKs are restarted, SYSCLK*n* toggles at the rate programmed in the RATIO field in PLLDIV*n*.
- Any SYSCLK*n* with the corresponding ALN*n* bit in ALNCTL cleared to 0 remains free-running during a GO operation. SYSCLK*n* is not modified to the new RATIO rate in PLLDIV*n*. SYSCLK*n* is not aligned to other SYSCLKs.
- The GOSTAT bit in PLLSTAT is set to 1 throughout the duration of a GO operation.

Figure 3 shows how the clocks are rising-edge aligned during a GO operation. Even though SYSCLK3 ratio remains the same, you must still program ALN3 = 1 in ALNCTL so that during the GO operation the PLL controller aligns SYSCLK3 to SYSCLK1 and SYSCLK2.

Figure 3. Clock Ratio Change and Alignment with GO Operation
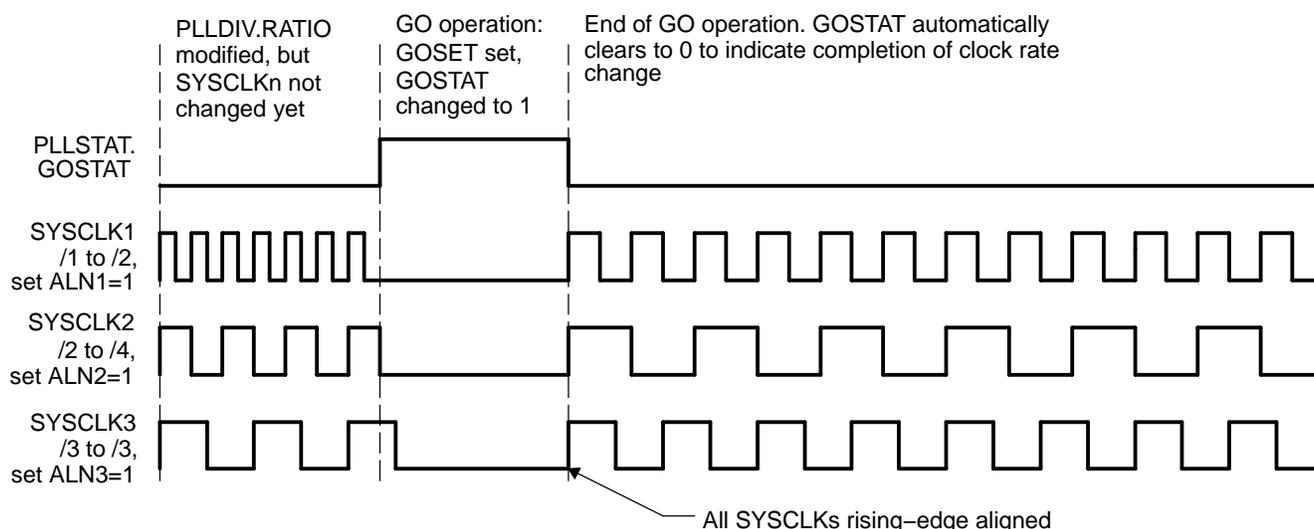
3.2.1.2 Software Steps to Modify PLLDIVn Ratios

Perform the following steps to modify PLLDIV*n*.

1. Check that the GOSTAT bit in PLLSTAT is cleared to 0 to show that no GO operation is currently in progress.
2. Program the RATIO field in PLLDIV*n* to the desired new divide-down rate.
3. Set the ALN1-3 bits in ALNCTL to 1 so that SYSCLK1-3 are aligned after the GO operation.
4. Set the GOSET bit in PLLCMD to 1 to initiate the GO operation to change the divide values and align SYSCLK1-3.
5. Read the GOSTAT bit in PLLSTAT to make sure the bit goes back to 0 to indicate that the GO operation has completed.

3.2.2 Divider 0 and PLL Multiplier (PLLM)

To change the values of D0 or PLLM, the PLL controller must first be placed in bypass mode. Perform the following steps to modify D0 or PLLM ratios.

1. In PLLCSR, write PLLEN = 0 to place the PLL in bypass mode.
2. Modify D0 and/or PLLM ratios
3. Wait for PLL to relock.
4. In PLLCSR, write PLLEN = 1 to switch from bypass mode to PLL mode.

3.3 PLL Power Down

The PLL may be powered down, in which case the PLL controller is in bypass mode and the DSP runs from a divided down version of the input reference clock. The DSP is still able to respond to events because it is still being clocked by the bypass clock (directly from CLKIN or OSCIN), although at a lower frequency.

Perform the following procedure to power down the PLL.

1. In PLLCSR, write PLLEN = 0 (bypass mode).
2. Wait 4 cycles of the slowest of PLLOUT or reference clock source (CLKIN or OSCIN).
3. In PLLCSR, write PLLPWRDN = 1 to power down the PLL.

3.4 PLL Wake Up

Perform the following procedure to wake up the PLL from its power-down mode.

1. Check to be sure PLL is already in bypass mode (PLLEN = 0).
2. In PLLCSR, write PLLPWRDN = 0 to wake up the PLL.
3. Follow the PLL reset sequence in Section 3.1.1 (steps 3 to 9) to reset the PLL. Wait for the PLL to lock and to switch from bypass to PLL mode.

3.5 Oscillator Power Down

Perform the following procedure to power down the oscillator.

1. In PLLCSR, write PLLEN = 0 (bypass mode).
2. Wait 4 cycles of the slowest of PLLOUT or reference clock source (CLKIN or OSCIN).
3. (Optional) Because the PLL is not used, you may place the PLL in power-down mode by writing PLLPWRDN = 1 in PLLCSR.
4. In PLLCSR, write OSCPWRDN = 1 to power down the oscillator.

A chip reset is required to wake up the device from oscillator power-down mode.

4   Registers

The PLL controller registers configure the operation of the PLL controller. The PLL controller registers are listed in Table 1. See the device-specific data manual for the memory address of these registers. All other register offset addresses not listed in Table 1 should be considerd as reserved locations and the register contents should not be modified.

Table 1. PLL Controller Registers

Offset	Acronym	Register Description	Section
000h	PLLPID	PLL controller peripheral identification register	Section 4.1
100h	PLLCSR	PLL control/status register	Section 4.2
110h	PLLM	PLL multiplier control register	Section 4.3
114h	PLLDIV0	PLL controller divider register 0	Section 4.4
118h	PLLDIV1	PLL controller divider register 1	Section 4.4
11Ch	PLLDIV2	PLL controller divider register 2	Section 4.4
120h	PLLDIV3	PLL controller divider register 3	Section 4.4
138h	PLLCMD	PLL controller command register	Section 4.5
13Ch	PLLSTAT	PLL controller status register	Section 4.6
140h	ALNCTL	PLL controller clock align control register	Section 4.7
148h	CKEN	Clock enable control register	Section 4.8
14Ch	CKSTAT	Clock status register	Section 4.9
150h	SYSTAT	SYSCLK status register	Section 4.10

4.1   PLL Controller Peripheral Identification Register (PLLPID)

The PLL controller peripheral identification register (PLLPID) contains identification code for the PLL controller. PLLPID is shown in Figure 4 and described in Table 2.

Figure 4. PLL Controller Peripheral Identification Register (PLLPID) [Offset 000h]

31		24	23		16
Reserved			TYPE		
R-0			R-01h		

15		8	7		0
CLASS			REV		
R-08h			R-01h		

LEGEND: R = Read only; -*n* = value after reset

Table 2. PLL Controller Peripheral Identification Register (PLLPID) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Reserved
23-16	TYPE		Identifies type of peripheral
		01h	PLL controller
15-8	CLASS		Identifies class of peripheral
		08h	Serial port
7-0	REV		Identifies revision of peripheral.
		01h	Current revision of peripheral.

4.2 PLL Control/Status Register (PLLCSR)

The PLL control/status register (PLLCSR) is shown in Figure 5 and described in Table 3.

Figure 5. PLL Control/Status Register (PLLCSR) [Offset 100h]

31										16
Reserved										
R-0										

15	7	6	5	4	3	2	1	0
Reserved		STABLE	Rsvd	PLLPWRDN	PLLRST	OSCPWRDN	Rsvd	PLLEN
R-0		R-1	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 3. PLL Control/Status Register (PLLCSR) Field Descriptions

Bit	Field	Value	Description
31-7	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
6	STABLE		Oscillator input stable bit. Indicates if the OSCIN/CLKIN input has stabilized. The STABLE bit is set to 1 after the reset controller counts 4096 OSCIN or CLKIN input clock cycles after the RESET signal is asserted high. It is assumed that the OSCIN/CLKIN input is stabilized after this number of cycles.
		0	OSCIN/CLKIN input is not yet stable. Oscillator counter is not finished counting.
		1	Oscillator counter is done counting and OSCIN/CLKIN input is assumed to be stable.
5	Reserved	0	Reserved. The reserved bit location is always read as 0. Always write a 0 to this location.
4	PLLPWRDN		PLL power-down mode select bit.
		0	PLL is operational.
		1	PLL is placed in power-down state.
3	PLLRST		PLL reset bit.
		0	PLL reset is released.
		1	PLL reset is asserted.
2	OSCPWRDN		Oscillator power-down mode command bit.
		0	No effect. Write of 0 clears bit to 0.
		1	Oscillator power-down command. Write of 1 causes oscillator power-down command. Once set, OSCPWRDN remains set but further writes of 1 can reinitiate the oscillator power-down command.
1	Reserved	0	Reserved. The reserved bit location is always read as 0. Always write a 0 to this location.
0	PLLEN		PLL enable bit.
		0	Bypass mode. Divider D0 and PLL are bypassed. SYSCLK1/SYSCLK2/SYSCLK3 are divided down directly from input reference clock.
		1	PLL mode. Divider D0 and PLL are not bypassed. PLL output path is enabled. SYSCLK1/SYSCLK2/SYSCLK3 are divided down from PLL output.

4.3 PLL Multiplier Control Register (PLLM)

The PLL multiplier control register (PLLM) is shown in Figure 6 and described in Table 4. The PLLM defines the input reference clock frequency multiplier in conjunction with the PLL divider ratio bits (RATIO) in the PLL controller divider 0 register (PLLDIV0).

Figure 6. PLL Multiplier Control Register (PLLM) [Offset 110h]

31	16
Reserved	
R-0	

15	5	4	0
Reserved		PLLM	
R-0		R/W-Dh	
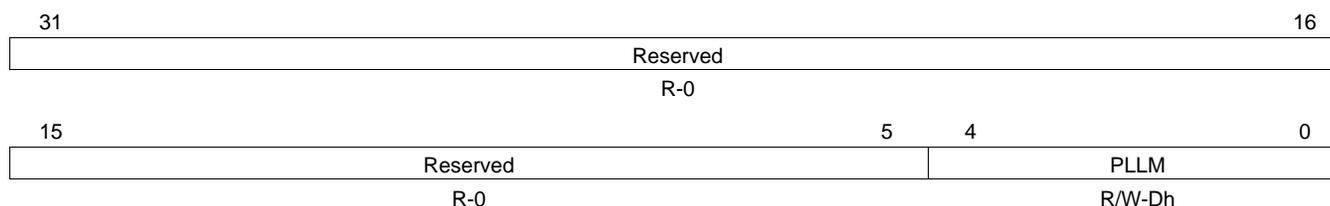
LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4. PLL Multiplier Control Register (PLLM) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
4-0	PLLM	0-1Fh	PLL multiplier bits. Defines the frequency multiplier of the input reference clock in conjunction with the PLL divider ratio bits (RATIO) in PLLDIV0.
		0-3h	Reserved
		4h	×4 multiplier rate
		5h	×5 multiplier rate
		6h-19h	×6 multiplier rate to ×25 multiplier rate
		1Ah-1Fh	Reserved

4.4 PLL Controller Divider Registers (PLLDIV0-PLLDIV3)

The PLL controller divider register (PLLDIV0-PLLDIV3) is shown in Figure 7 and described in Table 5.

Figure 7. PLL Controller Divider Register (PLLDIV*n*) [Offset 114h, 118h, 11Ch, 120h]

31		16
	Reserved	
	R-0	

15	14		5	4		0
D*n*EN		Reserved			RATIO(A)	
R/W-1		R-0			R/W-n	
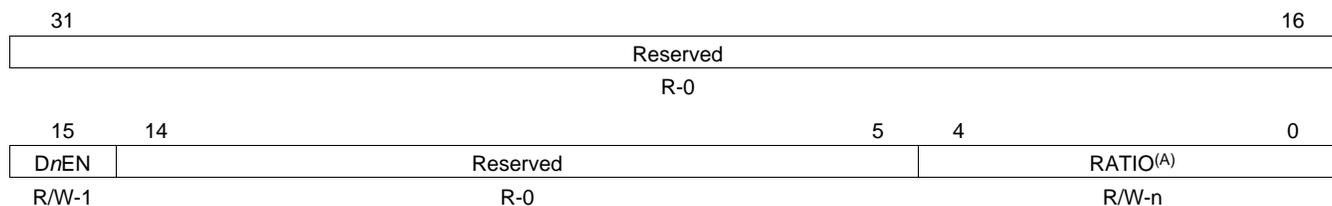
LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

A For DIV0 and DIV1, the default value is 0h (÷1); for DIV2, the default value is 1h (÷2); for DIV3, the default value is 2h (÷3).

Table 5. PLL Controller Divider Register (PLLDIV*n*) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
15	D*n*EN		Divider D*n* enable bit.
		0	Divider *n* is disabled. No clock output.
		1	Divider *n* is enabled.
14-5	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
4-0	RATIO	0-1Fh	Divider ratio bits.
		0	÷1. Divide frequency by 1.
		1h	÷2. Divide frequency by 2.
		2h	÷3. Divide frequency by 3.
		3h-1Fh	÷4 to ÷32. Divide frequency by 4 to divide frequency by 32.

4.5 PLL Controller Command Register (PLLCMD)

The PLL controller command register (PLLCMD) contains the command bit for GO operation. PLLCMD is shown in Figure 8 and described in Table 6.

Figure 8. PLL Controller Command Register (PLLCMD) [Offset 138h]

31	16
Reserved	
R-0	

15	1	0
Reserved		GOSET
R-0		R/W-0
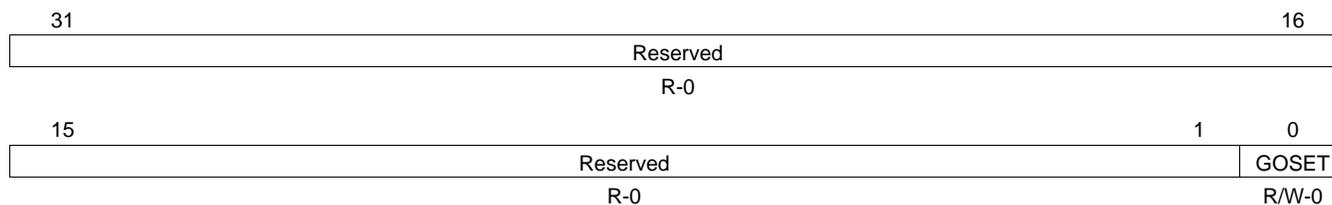
LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6. PLL Controller Command Register (PLLCMD) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
0	GOSET		GO operation command for SYSCLK rate change and phase alignment.
		0	No effect. Write of 0 clears bit to 0.
		1	Initiates GO operation. Write of 1 initiates GO operation. Once set, GOSET remains set but further writes of 1 can reinitiate the GO operation.

4.6 PLL Controller Status Register (PLLSTAT)

The PLL controller status register (PLLSTAT) shows the PLL controller status. PLLSTAT is shown in Figure 9 and described in Table 7.

Figure 9. PLL Controller Status Register (PLLSTAT) [Offset 13Ch]

31		16
	Reserved	
	R-0	

15		1	0
	Reserved		GOSTAT
	R-0		R-0
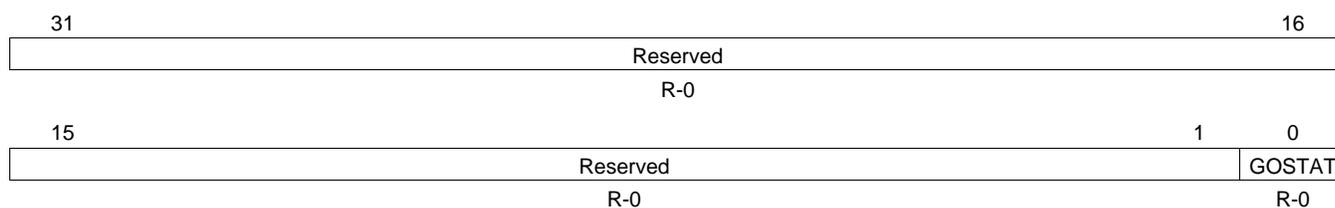
LEGEND: R = Read only; -*n* = value after reset

Table 7. PLL Controller Status Register (PLLSTAT) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
0	GOSTAT		GO operation status.
		0	GO operation is not in progress. SYSCLK divide ratios are not being changed.
		1	GO operation is in progress. SYSCLK divide ratios are being changed and SYSCLKs are being aligned.

4.7 PLL Controller Clock Align Control Register (ALNCTL)

The PLL controller clock align control register (ALNCTL) is shown in Figure 10 and described in Table 8.

Figure 10. PLL Controller Clock Align Control Register (ALNCTL) [Offset 140h]

31	16
Reserved	
R-0	

15	3	2	1	0
Reserved		ALN3	ALN2	ALN1
R-0		R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 8. PLL Controller Clock Align Control Register (ALNCTL) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
2	ALN3		SYSCLK3 alignment.
		0	**Do not use this setting.** Do not change SYSCLK3 divide ratio nor align SYSCLK3 to other SYSCLKs during GO operation. SYSCLK3 is left free-running when the GOSET bit in PLLCMD is set to 1.
		1	**Use this setting.** Align SYSCLK3 to other SYSCLKs selected in ALNCTL when the GOSET bit in PLLCMD is set to 1. Change SYSCLK3 rate to the ratio programmed in the RATIO bit in PLLDIV3.
1	ALN2		SYSCLK2 alignment.
		0	**Do not use this setting.** Do not change SYSCLK2 divide ratio nor align SYSCLK2 to other SYSCLKs during GO operation. SYSCLK2 is left free-running when the GOSET bit in PLLCMD is set to 1.
		1	**Use this setting.** Align SYSCLK2 to other SYSCLKs selected in ALNCTL when the GOSET bit in PLLCMD is set to 1. Change SYSCLK2 rate to the ratio programmed in the RATIO bit in PLLDIV2.
0	ALN1		SYSCLK1 alignment.
		0	**Do not use this setting.** Do not change SYSCLK1 divide ratio nor align SYSCLK1 to other SYSCLKs during GO operation. SYSCLK1 is left free-running when the GOSET bit in PLLCMD is set to 1.
		1	**Use this setting.** Align SYSCLK1 to other SYSCLKs selected in ALNCTL when the GOSET bit in PLLCMD is set to 1. Change SYSCLK1 rate to the ratio programmed in the RATIO bit in PLLDIV1.

4.8 Clock Enable Control Register (CKEN)

The clock enable control register (CKEN) enables/disables the PLL controller output clock, AUXCLK. CKEN is shown in Figure 11 and described in Table 9.

Figure 11. Clock Enable Control Register (CKEN) [Offset 148h]

31					16
Reserved					
R-0					

15			3	2	1	0
Reserved				Reserved		AUXEN
R-0				R/W-1		R/W-1
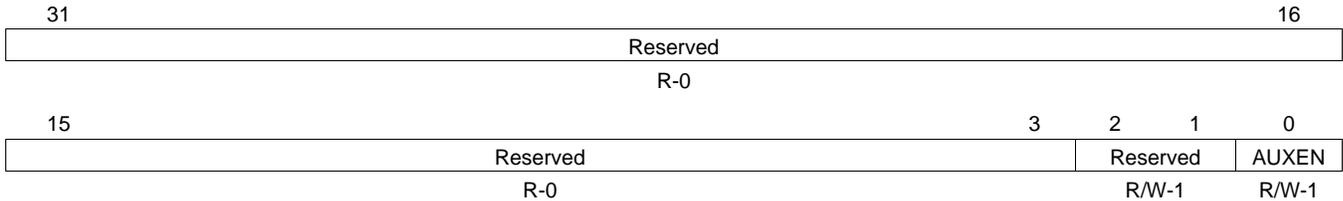
LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 9. Clock Enable Control Register (CKEN) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
2-1	Reserved	1	Reserved. The reserved bit location is always read as 1. Always write a 1 to this location.
0	AUXEN		AUXCLK enable control.
		0	Disable AUXCLK.
		1	Enable AUXCLK.

4.9 *Clock Status Register (CKSTAT)*

The clock status register (CKEN) shows the status of all PLL controller output clock, AUXCLK. CKSTAT is shown in Figure 12 and described in Table 10.

Figure 12. Clock Status Register (CKSTAT) [Offset 14Ch]

31		16
	Reserved	
	R-0	

15	3	2 1	0
Reserved		Reserved	AUXON
R-0		R-1	R-1
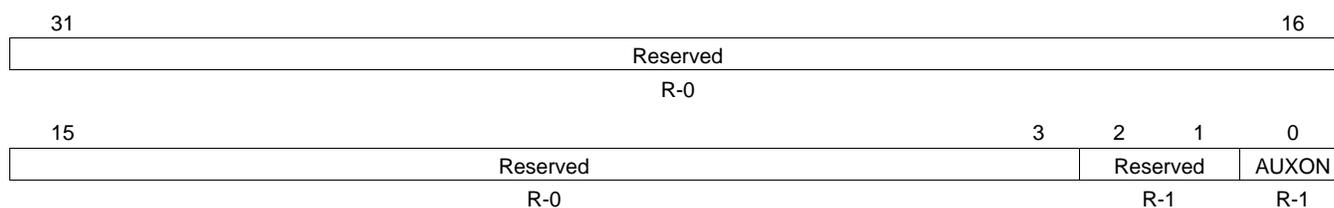
LEGEND: R = Read only; -*n* = value after reset

Table 10. Clock Status Register (CKSTAT) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
2-1	Reserved	1	Reserved. The reserved bit location is always read as 1. A value written to this field has no effect.
0	AUXON		AUXCLK on status.
		0	AUXCLK is gated.
		1	AUXCLK is on.

4.10 SYSCLK Status Register (SYSTAT)

The SYSCLK status register (SYSTAT) shows the status of SYSCLK1, SYSCLK2, and SYSCLK3. SYSTAT is shown in Figure 13 and described in Table 11.

Figure 13. SYSCLK Status Register (SYSTAT) [Offset 150h]

31				16
		Reserved		
		R-0		

15		3	2	1	0
Reserved			SYS3ON	SYS2ON	SYS1ON
R-0			R-1	R-1	R-1
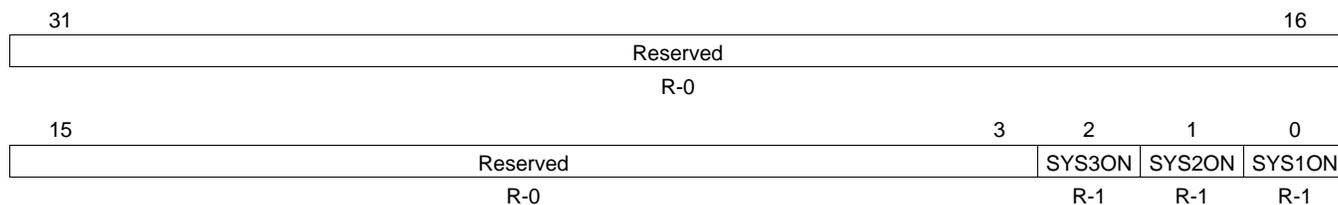
LEGEND: R = Read only; -*n* = value after reset

Table 11. SYSCLK Status Register (SYSTAT) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
2	SYS3ON		SYSCLK3 on status.
		0	SYSCLK3 is gated.
		1	SYSCLK3 is on.
1	SYS2ON		SYSCLK2 on status.
		0	SYSCLK2 is gated.
		1	SYSCLK2 is on.
0	SYS1ON		SYSCLK1 on status.
		0	SYSCLK1 is gated.
		1	SYSCLK1 is on.

Appendix A   Board Connections to Select CLKIN or OSCIN as Reference Clock Source

The following figures show the board connections to select CLKIN or OSCIN as the reference clock source to the PLL controller. Figure A-1 shows the case when the CLKIN pin is used as the reference clock source. Figure A-2 shows the case when the OSCIN pin is used as the reference clock source.

**Figure A-1. CLKIN Pin Used as Reference Clock Source**
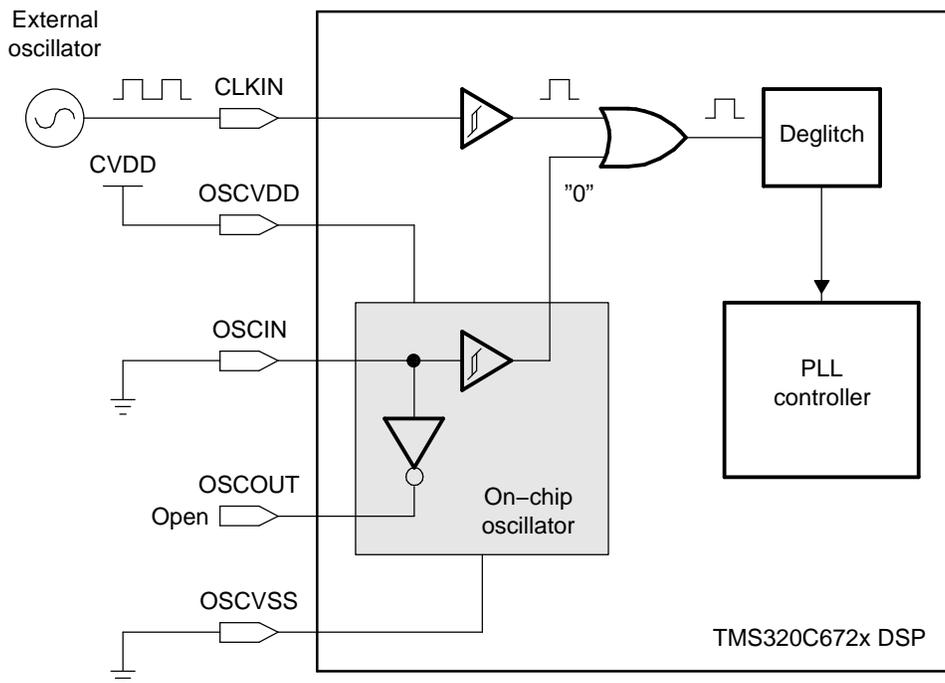
Figure A-2. OSCIN Pin Used as Reference Clock Source
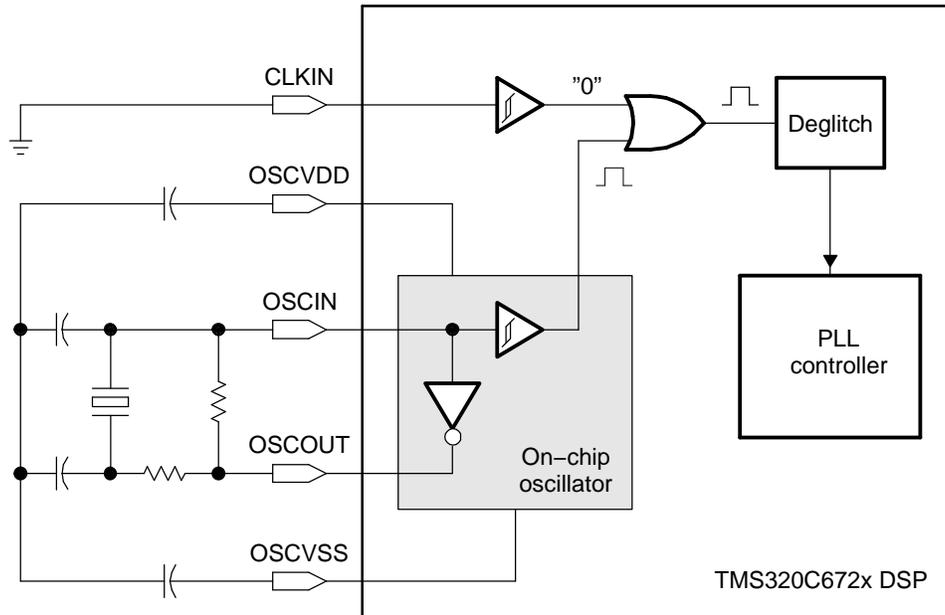
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