TMS320C6472/TMS320TCI648x DSP General-Purpose Input/Output (GPIO)

User's Guide

Literature Number: SPRU725A
December 2005–Revised October 2009

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About This Manual

This document describes the general-purpose input/output (GPIO) peripheral in the TMS320TCI648x/TMS320C6472 digital signal processors (DSPs).

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the C6000™ devices and related support tools. Copies of these documents are available on the Internet. *Tip:* Enter the literature number in the search box provided at www.ti.com.

SPRU189 — *TMS320C6000 DSP CPU and Instruction Set Reference Guide.* Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C6000 digital signal processors (DSPs).

SPRU198 — *TMS320C6000 Programmer's Guide.* Describes ways to optimize C and assembly code for the TMS320C6000™ DSPs and includes application program examples.

SPRU301 — *TMS320C6000 Code Composer Studio Tutorial.* Introduces the Code Composer Studio™ integrated development environment and software tools.

SPRU321 — *Code Composer Studio Application Programming Interface Reference Guide.* Describes the Code Composer Studio™ application programming interface (API), which allows you to program custom plug-ins for Code Composer.

SPRU871 — *TMS320C64x+ Megamodule Reference Guide.* Describes the TMS320C64x+ digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

User's Guide

SPRU725A–December 2005–Revised October 2009

C6472/TCI648x GPIO

1 Overview

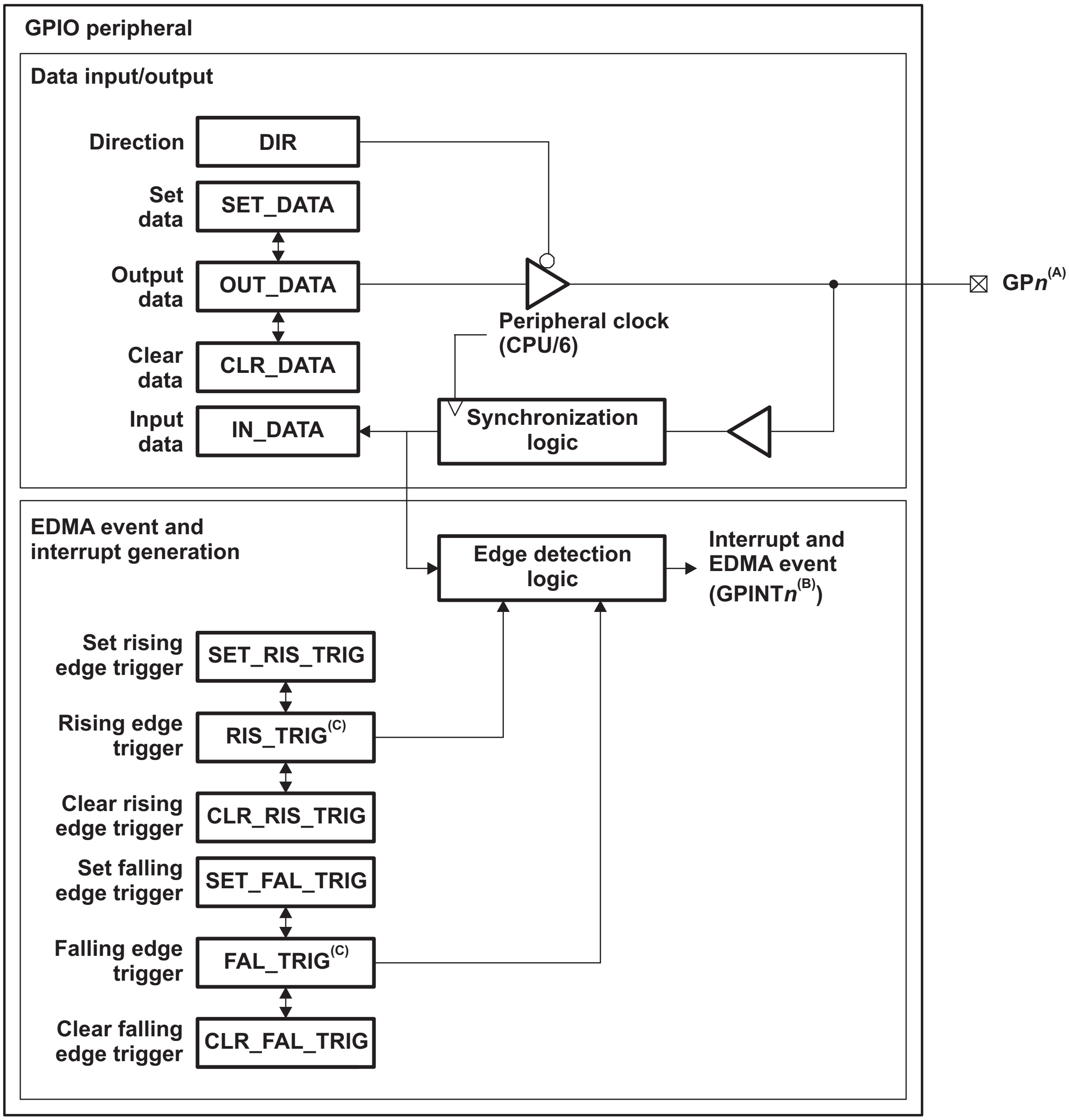
The general-purpose input/output (GPIO) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, you can write to an internal register to control the state driven on the output pin. When configured as an input, you can detect the state of the input by reading the state of an internal register.

In addition, the GPIO peripheral can produce CPU interrupts and EDMA synchronization events in different interrupt/event generation modes.

Figure 1 shows the GPIO peripheral block diagram. For an illustration of the GPIO peripheral in the DSP block diagram, see the device-specific data manual.

Some GPIO pins are muxed with other device pins. For details on specific muxing and for the availability of the register bits, see the device-specific data manual. GPINT[0:15] are all available as synchronization events to the EDMA and as interrupt sources to the CPU.

Figure 1. GPIO Peripheral Block Diagram



A Some of the GP*n* pins are muxed with other device signals. For details, see the device-specific data manual.

B All GPINT*n* can be used as CPU interrupts and synchronization events to the EDMA.

C The RIS_TRIG and FAL_TRIG registers are internal to the GPIO module and are not visible to the CPU.

2 GPIO Function

You can independently configure each GPIO pin (GPn) as either an input or an output using the GPIO direction registers. The GPIO direction register (DIR) specifies the direction of each GPIO signal. Logic 0 indicates the GPIO pin is configured as output, and logic 1 indicates input.

When configured as output, writing a 1 to a bit in the set data register drives the corresponding GPn to a logic-high state. Writing a 1 to a bit in the clear data register drives the corresponding GPn to a logic-low state. The output state of each GPn can also be directly controlled by writing to the output data register. For example, to set GP8 to a logic-high state, the software can perform one of the following:

- Write 0x100 to the SET_DATA register
- Read in OUT_DATA register, change the eighth bit to 1, and write the new value back to OUT_DATA

To set GP8 to a logic-low state, the software can perform one of the following:

- Write 0x100 to the CLR_DATA register
- Read in OUT_DATA register, change the eighth bit to 0, and write the new value back to OUT_DATA

Note that writing a 0 to bits in the set data and clear data registers does not affect the GPIO pin state. Also, for GPIO pins configured as input, writing to the set data, clear data, or output data registers does not affect the pin state.

For a GPIO pin configured as input, reading the input data register (IN_DATA) will return the pin state.

Reading the SET_DATA register or the CLR_DATA data register will return the value in OUT_DATA, not the actual pin state. The pin state is available by reading the input data register.

3 Interrupt and Event Generation

Each GPIO pin (GPn) can be configured to generate a CPU interrupt (GPINTn) and a synchronization event to the EDMA (GPINTn). The interrupt and EDMA event can be generated on the rising-edge, falling-edge, or on both edges of the GPIO signal. The edge detection logic is synchronized to the GPIO peripheral clock.

The direction of the GPIO pin does not need to be input when using the pin to generate the interrupt and EDMA event. When the GPIO pin is configured as input, transitions on the pin trigger interrupts and EDMA events. When the GPIO pin is configured as output, software can toggle the GPIO output register to change the pin state and in turn trigger the interrupt and EDMA event.

Two internal registers, RIS_TRIG and FAL_TRIG, specify which edge of the GPn signal generates an interrupt and EDMA event. Each bit in these two registers corresponds to a GPn pin. Table 1 describes the CPU interrupt and EDMA event generation of GPn pin based on the bit settings of the RIS_TRIG and FAL_TRIG registers.

Table 1. GPIO Interrupt and EDMA Event Configuration Options

RIS_TRIG bit n	FAL_TRIG bit n	CPU Interrupt and EDMA Event Generation
0	0	GPINTn interrupt and EDMA event is disabled
0	1	GPINTn interrupt and EDMA event is triggered on falling edge of GPn signal
1	0	GPINTn interrupt and EDMA event is triggered on rising edge of GPn signal
1	1	GPINTn interrupt and EDMA event is triggered on both rising and falling edge of GPn signal

RIS_TRIG and FAL_TRIG are not directly accessible or visible to the CPU. These registers are accessed indirectly through four registers: SET_RIS_TRIG, CLR_RIS_TRIG, SET_FAL_TRIG, and CLR_FAL_TRIG. Writing 1 to a bit on the SET_RIS_TRIG register sets the corresponding bit on the RIS_TRIG register. Writing 1 to a bit of CLR_RIS_TRIG register clears the corresponding bit on the RIS_TRIG register. Writing to SET_FAL_TRIG and CLR_FAL_TRIG works the same way on the FAL_TRIG register.

Reading the SET_RIS_TRIG or CLR_RIS_TRIG register returns the value of RIS_TRIG register. Reading from SET_FAL_TRIG and CLR_FAL_TRIG register returns the value of FAL_TRIG register.

To use the GPIO pins as sources for CPU interrupts and EDMA events, bit 0 in the bank interrupt enable register (BINTEN) must be set to 1.

4 Emulation Halt Operation

The GPIO peripheral is not affected by emulation halts.

5 Registers

The GPIO peripheral is configured through the registers listed in Table 2. For the memory address of these registers, see the device-specific data manual.

Table 2. GPIO Registers

Offsets	Acronym	Register Name	See
0008	BINTEN	Interrupt Per-Bank Enable Register	Section 5.1
0010	DIR	Direction Register	Section 5.2
0014	OUT_DATA	Output Data Register	Section 5.3
0018	SET_DATA	Set Data Register	Section 5.4
001C	CLR_DATA	Clear Data Register	Section 5.5
0020	IN_DATA	Input Data Register	Section 5.6
0024	SET_RIS_TRIG	Set Rising Edge Interrupt Register	Section 5.7
0028	CLR_RIS_TRIG	Clear Rising Edge Interrupt Register	Section 5.8
002C	SET_FAL_TRIG	Set Falling Edge Interrupt Register	Section 5.9
0030	CLR_FAL_TRIG	Clear Falling Edge Interrupt Register	Section 5.10

5.1 Interrupt Per-Bank Enable Register (BINTEN)

To use the GPIO pins as sources for CPU interrupts and EDMA events, bit 0 in the bank interrupt enable register (BINTEN) must be set. BINTEN is shown in Figure 2 and described in Table 3.

Figure 2. Interrupt Per-Bank Enable Register (BINTEN)

31	1	0
Reserved		EN
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 3. Interrupt Per-Bank Enable Register (BINTEN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
0	EN		Enables all GPIO pins as interrupt sources to the DSP CPU.
		0	Disables GPIO interrupts
		1	Enables GPIO interrupts

5.2 Direction Register (DIR)

The GPIO direction register (DIR) determines if a given GPIO pin is an input or an output. The GPDIR is shown in Figure 3 and described in Table 4. By default, all the GPIO pins are configured as input pins.

When GPIO pins are configured as output pins, the GPIO output buffer drives the GPIO pin. If it is necessary to place the GPIO output buffer in a high-impedance state, the GPIO pin must be configured as an input pin (DIRn = 0). At reset, GPIO pins default to input mode.

Figure 3. Direction Register (DIR)

31–16
Reserved
R-0

15	14	13	12	11	10	9	8
DIR15	DIR14	DIR13	DIR12	DIR11	DIR10	DIR9	DIR8
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

7	6	5	4	3	2	1	0
DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4. Direction Register (DIR) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
15-0	DIRn		Controls the direction of the GPn pin.
		0	GPn pin configured as output pin
		1	GPn pin configured as input pin

5.3 Output Data Register (OUT_DATA)

The GPIO output data register (OUT_DATA) indicates the value to be driven on a given GPIO output pin. The OUT_DATA registers are shown in Figure 4 and described in Table 5.

Figure 4. Output Data Register (OUT_DATA)

31	16
Reserved	
R-0	

15	14	13	12	11	10	9	8
OUT15	OUT14	OUT13	OUT12	OUT11	OUT10	OUT9	OUT8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 5. Output Data Register (OUT_DATA) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
15-0	OUTn		Controls the drive state of the corresponding GPn pin. These bits do not affect the state of the pin when the pin is configured as an input. Reading these bits returns the value of this register, not the state of the pin.

5.4 Set Data Register (SET_DATA)

The GPIO set data register (SET_DATA) is shown in Figure 5 and described in Table 6. SET_DATA provides an alternate means of driving GPIO outputs high. Writing a 1 to a bit of SET_DATA sets the corresponding bit in OUT_DATA. Writing a 0 has no effect. Reading SET_DATA returns the contents of OUT_DATA.

Figure 5. Set Data Register (SET_DATA)

31–16
Reserved
R-0

15	14	13	12	11	10	9	8
SET15	SET14	SET13	SET12	SET11	SET10	SET9	SET8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
SET7	SET6	SET5	SET4	SET3	SET2	SET1	SET0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6. Set Data Register (SET_DATA) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
15-0	SETn		Writing 1 sets the corresponding bit the OUT_DATA register. Reading this register returns the contents of the OUT_DATA register. Writing a 0 has no effect.
		0	No effect
		1	Sets the corresponding bit in OUT_DATA

5.5 Clear Data Register (CLR_DATA)

The GPIO clear data register (CLR_DATA) is shown in Figure 6 and described in Table 7. CLR_DATA provides an alternate means of driving GPIO outputs low. Writing a 1 to a bit of CLR_DATA clears the corresponding bit in OUT_DATA. Writing a 0 has no effect. Reading CLR_DATA returns the contents of OUT_DATA.

Figure 6. Clear Data Register (CLR_DATA)

31	16
Reserved	
R-0	

15	14	13	12	11	10	9	8
CLR15	CLR14	CLR13	CLR12	CLR11	CLR10	CLR9	CLR8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
CLR7	CLR6	CLR5	CLR4	CLR3	CLR2	CLR1	CLR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 7. Clear Data Register (CLR_DATA) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
15-0	CLRn		Writing 1 clears the corresponding bit the OUT_DATA register. Reading this register returns the contents of the OUT_DATA register. Writing a 0 has no effect.
		0	No effect
		1	Clears the corresponding bit in OUT_DATA

5.6 Input Data Register (IN_DATA)

The GPIO input data register (IN_DATA) reflects the state of the GPIO pins. The IN_DATA register is shown in Figure 7 and described in Table 8. When read, IN_DATA returns the state of the GPIO pins regardless of the state of the corresponding bits in the DIR and OUT_DATA registers.

Figure 7. Input Data Register (IN_DATA)

31	16
Reserved	
R-0	

15	14	13	12	11	10	9	8
IN15	IN14	IN13	IN12	IN11	IN10	IN9	IN8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

7	6	5	4	3	2	1	0
IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R = Read only; -*n* = value after reset

Table 8. Input Data Register (IN_DATA) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
15-0	INn		Returns the status of the corresponding GPn pin.

5.7 Set Rising Edge Interrupt Register (SET_RIS_TRIG)

The GPIO rising trigger register (RIS_TRIG) configures the edge detection logic to trigger GPIO interrupts and EDMA events on the rising edge of GPIO signals. Setting a bit to 1 in RIS_TRIG causes the corresponding GPIO interrupt and EDMA event (GPINTn) to be generated on the rising edge of GPn. RIS_TRIG is not directly accessible by the CPU; it must be configured using the GPIO set rising trigger and clear rising trigger registers.

The GPIO set rising trigger register (SET_RIS_TRIG) is shown in Figure 8 and described in Table 9. Writing a 1 to a bit of SET_RIS_TRIG sets the corresponding bit in RIS_TRIG. Writing a 0 has no effect. Reading SET_RIS_TRIG returns the value in RIS_TRIG.

Figure 8. Set Rising Edge Interrupt Register (SET_RIS_TRIG)

31-16
Reserved
R-0

15	14	13	12	11	10	9	8
SETRIS15	SETRIS14	SETRIS13	SETRIS12	SETRIS11	SETRIS10	SETRIS9	SETRIS8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
SETRIS7	SETRIS6	SETRIS5	SETRIS4	SETRIS3	SETRIS2	SETRIS1	SETRIS0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 9. Set Rising Edge Interrupt Register (SET_RIS_TRIG) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
15-0	SETRISn		Writing a 1 enables the rising edge detection for the corresponding GPn pin. Reading this register returns the state of the RIS_TRIG register.
		0	No effect
		1	Sets the corresponding bit in RIS_TRIG

5.8 Clear Rising Edge Interrupt Register (CLR_RIS_TRIG)

The GPIO rising trigger register (RIS_TRIG) configures the edge detection logic to trigger GPIO interrupts and EDMA events on the rising edge of GPIO signals. Setting a bit to 1 in RIS_TRIG causes the corresponding GPIO interrupt and EDMA event (GPINTn) to be generated on the rising edge of GPn. RIS_TRIG is not directly accessible by the CPU; it must be configured using the GPIO set rising trigger and clear rising trigger registers.

The GPIO clear rising trigger register (CLR_RIS_TRIG) is shown in Figure 9 and described in Table 10. Writing a 1 to a bit of CLR_RIS_TRIG clears the corresponding bit in RIS_TRIG. Writing a 0 has no effect. Reading CLR_RIS_TRIG returns the value in RIS_TRIG.

Figure 9. Clear Rising Edge Interrupt Register (CLR_RIS_TRIG)

31	16
Reserved	
R-0	

15	14	13	12	11	10	9	8
CLRRIS15	CLRRIS14	CLRRIS13	CLRRIS12	CLRRIS11	CLRRIS10	CLRRIS9	CLRRIS8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
CLRRIS7	CLRRIS6	CLRRIS5	CLRRIS4	CLRRIS3	CLRRIS2	CLRRIS1	CLRRIS0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 10. Clear Rising Edge Interrupt Register (CLR_RIS_TRIG) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
15-0	CLRRISn		Writing a 1 disables rising edge detection for the corresponding GPn pin. Reading this register returns the state of the RIS_TRIG register.
		0	No effect
		1	Clears the corresponding bit in RIS_TRIG

5.9 Set Falling Edge Interrupt Register (SET_FAL_TRIG)

The GPIO falling trigger register (FAL_TRIG) configures the edge detection logic to trigger GPIO interrupts and EDMA events on the falling edge of GPIO signals. Setting a bit to 1 in FAL_TRIG causes the corresponding GPIO interrupt and EDMA event (GPINTn) to be generated on the falling edge of GPn. FAL_TRIG is not directly accessible by the CPU; it must be configured using the GPIO set falling trigger and clear falling trigger registers.

The GPIO set falling trigger register (SET_FAL_TRIG) is shown in Figure 10 and described in Table 11. Writing a 1 to a bit of SET_FAL_TRIG sets the corresponding bit in FAL_TRIG. Writing a 0 has no effect. Reading SET_FAL_TRIG returns the value in FAL_TRIG.

Figure 10. Set Falling Edge Interrupt Register (SET_FAL_TRIG)

31	16
Reserved	
R-0	

15	14	13	12	11	10	9	8
SETFAL15	SETFAL14	SETFAL13	SETFAL12	SETFAL11	SETFAL10	SETFAL9	SETFAL8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
SETFAL7	SETFAL6	SETFAL5	SETFAL4	SETFAL3	SETFAL2	SETFAL1	SETFAL0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 11. Set Falling Edge Interrupt Register (SET_FAL_TRIG) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
15-0	SETFALn		Writing a 1 enables the falling edge detection for the corresponding GPn pin. Reading this register returns the state of the FAL_TRIG register.
		0	No effect
		1	Sets the corresponding bit in FAL_TRIG

5.10 Clear Falling Edge Interrupt Register (CLR_FAL_TRIG)

The GPIO falling trigger register (FAL_TRIG) configures the edge detection logic to trigger GPIO interrupts and EDMA events on the falling edge of GPIO signals. Setting a bit to 1 in FAL_TRIG causes the corresponding GPIO interrupt and EDMA event (GPINTn) to be generated on the falling edge of GPn. FAL_TRIG is not directly accessible by the CPU; it must be configured using the GPIO set falling trigger and clear falling trigger registers.

The GPIO clear falling trigger register (CLR_FAL_TRIG) is shown in Figure 11 and described in Table 12. Writing a 1 to a bit of CLR_FAL_TRIG clears the corresponding bit in FAL_TRIG. Writing a 0 has no effect. Reading CLR_FAL_TRIG returns the value in FAL_TRIG.

Figure 11. Clear Rising Edge Interrupt Register (CLR_RIS_TRIG)

31 - 16
Reserved
R-0

15	14	13	12	11	10	9	8
CLRFAL15	CLRFAL14	CLRFAL13	CLRFAL12	CLRFAL11	CLRFAL10	CLRFAL9	CLRFAL8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
CLRFAL7	CLRFAL6	CLRFAL5	CLRFAL4	CLRFAL3	CLRFAL2	CLRFAL1	CLRFAL0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 12. Clear Rising Edge Interrupt Register (CLR_RIS_TRIG) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
15-0	CLRFALn		Writing a 1 disables falling edge detection for the corresponding GPn pin. Reading this register returns the state of the FAL_TRIG register.
		0	No effect
		1	Clears the corresponding bit in FAL_TRIG

Appendix A Revision History

This revision history highlights the technical changes made to the document in this revision.

Table 13. TCI648x/C6472 GPIO Revision History

See	Additions/Modifications/Deletions
Global	Added C6472 device
Section 1	Deleted block diagram and added reference to device-specific data manual

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