TMS320C672x DSP Peripherals Overview

Reference Guide

Literature Number: SPRU723B
June 2007

Texas Instruments

Contents

List of Tables

Trademarks

TMS320C672x, TMS320C6000, VelociTI, C672x are trademarks of Texas Instruments.

TMS320C672x DSP Peripherals Overview

This document provides an overview and briefly describes the peripherals available on the TMS320C672x™ digital signal processors (DSPs) of the TMS320C6000™ family. For a description of the C67x/C67x+ CPU, see the *TMS320C67x/C67x+ DSP CPU and Instruction Set Reference Guide* (literature number SPRU733).

1 Overview

The TMS320C672x™ platform of devices use advanced very long instruction word (VLIW) to achieve high performance through increased instruction-level parallelism. The VelociTI™ VLIW architecture uses multiple execution units operating in parallel to execute multiple instructions during a single clock cycle. Parallelism is the key to extremely high performance, taking these devices well beyond the performance capabilities of traditional designs.

The user-accessible peripherals available on the C672x™ devices are configured using a set of memory-mapped control registers. The peripheral bus controller performs the arbitration for accesses of on-chip peripherals.

Peripherals available on the C672x devices and their associated literature number are listed in Table 1.

Table 1. TMS320C672x DSP Peripherals Documentation

			C672x DSP			
Peripheral	**Acronym**	**Lit #**	**C6720**	**C6722, C6722B**	**C6726, C6726B**	**C6727, C6727B**
Dual Data Movement Accelerator	dMAX	SPRU795	√	√	√	√
External Memory Interface	EMIF	SPRU711	√	√	√	√
Inter-Integrated Circuit	I2C	SPRU877	√	√	√	√
Multichannel Audio Serial Port	McASP	SPRU878	√	√	√	√
Phase-Locked Loop Controller and Clock Generation	PLL	SPRU879	√	√	√	√
Real-Time Interrupt	RTI	SPRU717	√	√	√	√
Serial Peripheral Interface	SPI	SPRU718	√	√	√	√
Universal Host Port Interface	UHPI	SPRU719				√

2 Dual Data Movement Accelerator (dMAX)

The dual data movement accelerator (dMAX) controller is described in SPRU795. The dMAX is a module designed to perform data movement acceleration. The dMAX controller handles user-programmed data transfers between the internal data memory controller and the device peripherals on the C672x DSPs. The dMAX allows movement of data to/from any addressable memory space including internal memory, peripherals, and external memory.

The dMAX controller includes features such as the capability to perform 3-dimensional data transfers for advanced data sorting, and the capability to manage a section of the memory as a circular buffer/FIFO with delay-tap based reading and writing of data. The dMAX controller is capable of concurrently processing two transfer requests (provided that they are to/from different source/destinations).

3 External Memory Interface (EMIF)

The external memory interface (EMIF) is described in SPRU711. The EMIF supports a single bank of SDRAM and a single bank of asynchronous memory. The EMIF data width is 16-bits wide on the C6726, C6726B, C6722, C6722B, and C6720 DSPs, and 32-bits wide on the C6727 and C6727B DSPs.

SDRAM support includes ı16 and ′2 SDRAM devices with 1, 2, or 4 banks.

The C6726, C6726B, C6722, C6722B, and C6720 DSPs support SDRAM devices up to 128 Mbits.

The C6727 and C6727B DSPs extend SDRAM support to 256-Mbit and 512-Mbit devices.

Asynchronous memory support is typically used to boot from a parallel nonmultiplexed NOR flash device that can be 8-bits, 16-bits, or 32-bits wide. Booting from larger flash devices than are natively supported by the dedicated EMIF address lines is accomplished by using general-purpose I/O pins for upper address lines.

4 Inter-Integrated Circuit (I2C) Module

The inter-integrated circuit (I2C) module is described in SPRU877. The C672x DSP includes two I2C serial ports. A typical application is to configure one I2C serial port as a slave to an external user-interface microcontroller. The other I2C serial port may provide an interface between the C672x device and I2C-compatible devices connected by way of the I2C serial bus. External components, such as a CODEC or network controller, attached to the I2C bus serially transmit/receive up to 8-bit data to/from the C672x device through the 2-wire I2C interface.

The I2C module has the following features:

- Compliance with the Philips Semiconductors I2C-bus specification (version 2.1):
  - Support for byte format transfer
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers
  - Support for multiple slave-transmitters and master-receivers
  - Combined master transmit/receive and receive/transmit mode
  - Data transfer rate of from 10 kbps up to 400 kbps (Philips Fast-mode rate)
- One interrupt that can be used by the CPU. This interrupt can be generated as a result of one of the following conditions: transmit-data ready, receive-data ready, register-access ready, no-acknowledgement received, arbitration lost.
- Module enable/disable capability
- Free data format mode
- The SDA and SCL pins can be used for general-purpose input/output (GPIO)
- Two different ways to generate a transmit data ready interrupt when operating in slave-transmitter mode and enabled by the I2C extended mode register (I2CEMDR).

5 Multichannel Audio Serial Port (McASP)

The multichannel audio serial port (McASP) is described in SPRU878. The C672x DSP includes up to three McASPs (McASP2 is not available on the C6722, C6722B, and C6720 DSPs). The McASP functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP is useful for both Inter-Integrated Sound (IIS) protocols and intercomponent digital audio interface transmission (DIT).

Features of the McASP include:

- Two independent clock generator modules for transmit and receive
  - Clocking flexibility allows the McASP to receive and transmit at different rates. For example, the McASP can receive data at 48 kHz but output up-sampled data at 96 kHz or 192 kHz.
- Independent transmit and receive modules, each includes:
  - Programmable clock and frame sync generator
  - TDM streams from 2 to 32, and 384 time slots
  - Support for time slot sizes of 8, 12, 16, 20, 24, 28, and 32 bits
  - Data formatter for bit manipulation
- Individually assignable serial data pins (up to 16 pins)
- Glueless connection to audio analog-to-digital converters (ADC), digital-to-analog converters (DAC), codec, digital audio interface receiver (DIR), and S/PDIF transmit physical layer components
- Wide variety of I2S and similar bit-stream format
- Integrated digital audio interface transmitter (DIT) supports:
  - S/PDIF, IEC60958-1, AES-3 formats
  - Up to 16 transmit pins
  - Enhanced channel status/user data RAM
- 384-slot TDM with external digital audio interface receiver (DIR) device
  - For DIR reception, an external DIR receiver integrated circuit should be used with I2S output format and connected to the McASP receive section.
- Extensive error checking and recovery
  - Transmit underruns and receiver overruns due to the system not meeting real-time requirements
  - Early or late frame sync in TDM mode
  - Out-of-range high-frequency master clock for both transmit and receive
  - External error signal coming into the AMUTEIN input
  - DMA error due to incorrect programming

6 Phase-Locked Loop (PLL) Controller

The phase-locked loop (PLL) controller and clock generation are described in SPRU879. The PLL controller features software-configurable PLL multiplier controller, dividers (D0, D1, D2, and D3), and reset controller. The PLL controller accepts an input clock from the CLKIN pin or from the on-chip oscillator output signal OSCIN. The PLL controller offers flexibility and convenience by way of software-configurable multiplier and dividers to modify the input signal internally. The resulting clock outputs are passed to the DSP core, peripherals, and other modules inside the DSP.

- The input reference clocks to the PLL controller:
  - CLKIN: input signal from external oscillator (3.3V)
  - OSCIN: output signal from on-chip oscillator (1.2V)
- The resulting output clocks from the PLL controller:
  - AUXCLK: internal clock output signal directly from CLKIN or OSCIN.
  - SYSCLK1: internal clock output of divider D1.
  - SYSCLK2: internal clock output of divider D2.
  - SYSCLK3: internal clock output of divider D3.

SYSCLK1 is used by the CPU, memory controller, and memories. SYSCLK2 is used by the peripheral subsystem and dMAX. SYSCLK3 is used exclusively for the EMIF.

7 Program and Data Memory Controller

The program and data memory controller is designed to support a flat memory architecture for data accesses and a one-level cached memory architecture for program fetches. The data memory controller does not contain the on-chip SRAM/ROM, but supports glueless interfaces to ASIC single-port compiler memories organized in specific banking arrangements. To this effect, the program and data memory controller includes a ROM controller, a RAM controller, and an instruction cache (including cache storage memory). The memory controller supports single-cycle data accesses from the C672x CPU to the RAM and ROM. Up to three parallel accesses to the internal RAM and ROM from three of the following four sources is supported:

- Two 64-bit data accesses from the C672x CPU
- One 256-bit program fetch from the core and program cache
- One 32-bit data access from the peripheral system (either dMAX or UHPI)

8 Real-Time Interrupt Timer (RTI)

The real-time interrupt timer (RTI) is described in SPRU717. The real-time interrupt timer includes:

- Two 32-bit counter/prescaler pairs
- Two input captures (tied to McASP DMA events for sample rate measurement)
- Four compares with automatic update capability
- Digital watchdog timer (optional) for enhanced system robustness

9 Serial Peripheral Interface (SPI) Port

The C672x DSP includes two serial peripheral interface (SPI) ports, described in SPRU718. This allows one SPI port to be configured as a slave and used to control the DSP while the other SPI port is used by the DSP to control external peripherals.

The SPI ports support a basic 3-pin mode as well as optional 4-pin and 5-pin modes. The optional pins include a slave chip-select pin and an enable pin that implements handshaking automatically in hardware for maximum SPI throughput.

The SPI0 port is pin multiplexed with the two I2C serial ports (I2C0 and I2C1). The SPI1 serial port is pin multiplexed with five of the serial data pins from McASP0 and McASP1.

10 Universal Host Port Interface (UHPI)

The universal host port interface (UHPI), described in SPRU719, is only available on the C6727 and C6727B DSPs. The UHPI is a parallel interface through which an external host CPU can access memories on the DSP. Three modes are supported by the UHPI:

- Multiplexed address/data - halfword (16-bit wide) mode
- Multiplexed address/data - full word (32-bit wide) mode
- Nonmultiplexed mode - 16-bit address and 32-bit data bus

The UHPI can also be restricted to accessing a single page (64K bytes) of memory anywhere in the address space of the C672x DSP (this page can be changed, but only by the C672x CPU). This feature allows the UHPI to be used for high-speed data transfers even in systems where security is an important requirement.

Appendix A Revision History

Table A-1 lists the changes made since the previous version of this document.

Table A-1. Document Revision History

Reference	Additions/Modifications/Deletions
Table 1	Added Revision 1.2 devices (C6727B, C6726B, C6722B, and C6720)
Section 3	Updated section with information pertaining to the Revision 1.2 devices (C6727B, C6726B, C6722B, and C6720)
Section 5	Updated section with information pertaining to the Revision 1.2 devices (C6727B, C6726B, C6722B, and C6720)
Section 10	Updated section with information pertaining to the Revision 1.2 devices (C6727B, C6726B, C6722B, and C6720)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
Low Power Wireless	www.ti.com/lpw	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265